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OPERATING MANUAL

MODEL 6465

Dual Channel, 65 MHz, 12-bit,
A/D Converter for VMEbus Systems

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Pentek Model 6465 Operating Manual
Revision History

Date	Rev	Applicable Serial #'s	Comments
03/03/99	Preliminary	9824000 - Forward	Initial product release
03/23/99	Preliminary	9824000 - Forward	Sec. 1.4, corrected; only TTL is accepted as clock in. Replaced former sec. 2.2.5 with new sec.2.2.3, Jumper Blocks 1 & 2. Sec. 2.3.2, removed references to Option 019; corrected information on cabling.
03/03/00	A	9934001 - Forward	Changed Figures 2-2 to reflect PC board changes (references throughout the entire manual also reflect these changes). Sec. 2.2.1, jumper blocks are now located outside the cans. Sec. 2.2.2, JP5 is now a three pin jumper.
11/10/00	A.1	9934001 - Forward	Added Sect. 1.6, describing Option 031. Added Appendix A, Performance Characteristics of Option 031.

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Chapter 1: Overview

1.1 Introduction

Pentek's Model 6465 is a dual channel, high−speed, 12−bit A/D converter board that operates at sampling rates up to 65 MHz. It is a single−slot, 6U VMEbus board, and includes signal conditioning and clock generation circuitry. The two channels are identical and operate from the same sample clock.

Among its other uses, the Model 6465 is intended as a front end for the Pentek Models 4271, 4272 and 65xx Digital Receivers. Connections between the Model 6465 and these receivers are made with a standard 80−conductor, 0.025 in. pitch, flat ribbon cable, using supplied mating connectors. Cable assemblies are also available from Pentek.

1.2 Signal Conditioning

Each analog input accepts a ±1.0 V full scale signal from a front panel SMA connector with a 50 Ω input termination. A buffer amplifier then delivers the signal to a high−order Chebyscheff, low−pass anti−aliasing filter, which restricts input bandwidth to approximately 26 MHz. Other input filter characteristics are available on special order.

For systems in which the input signal is already bandlimited, the on−board anti−aliasing filter can be bypassed.

1.3 A/D Conversion

The Model 6465's A/D converter has resolution of 12 bits. Digitized data from both channels are available on each of two front panel 80-pin connectors. In the standard configuration of this device, separate differential ECL drivers are provided for each channel to support more flexible connectivity to different configurations of digital receivers.

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1.4 Sample Rate Control

The sample clock generator is a 64 MHz crystal oscillator, in a standard DIP package. This oscillator is socketed, allowing you to replace it, if needed, for special frequencies.

Alternatively, an external TTL, ECL or analog sample clock signal can be supplied through a front panel SMA connector. The A/D converter used on this unit is specified to operate at sample frequencies up to 41 MHz. This maximum sample rate is achievable only by using the external clock input. Selection of the internal oscillator or the external clock is made with an on−board DIPswitch.



NOTE

The Minimum Sample Rate on the Model 6465 is 5 MHz.

1.5 VME Interface

The VMEbus interface is used only to supply power to the Model 6465. No VMEbus signals are used on the board, and no VME-programmable functions exist in the unit. The board does, however, pass along the daisy-chained VMEbus signals.

1.6 Option 031

Model 6465 Option 031 provides additional shielding and removes the low pass filter. Other specification changes are:

Input full scale voltage:	2 Vp-p +/- 5%
Large Signal BW:	80 MHz
Small Signal BW:	120 MHz
SNR:	60 dB
Intermodulation Distortion:	-80 dBFS

Appendix A contains figures which illustrate some of the performance characteristics of Model 6465 Option 031.

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1.7 Block Diagram

A block diagram of the Pentek Model 6465, Dual-Channel, 65 MHz, 12-bit A/D Converter for VMEbus systems is presented in Figure 1-1, below.

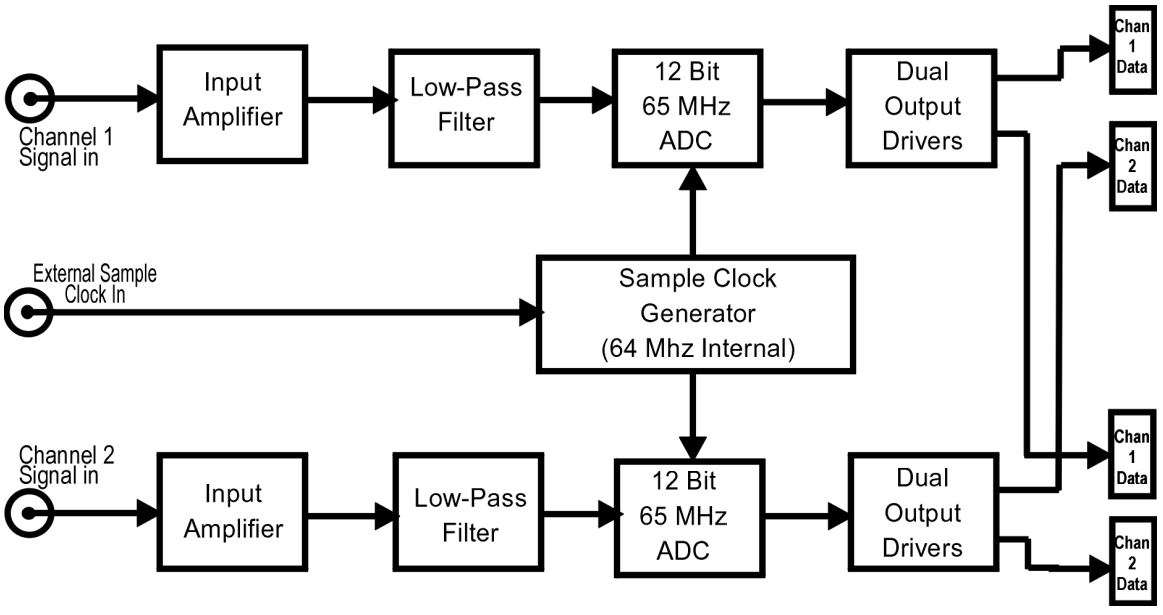


Figure 1-1: Model 6465 –Block Diagram

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1.8 Specifications

Analog Inputs:

Number:	2
Type:	Single-Ended, SMA connector
Full Scale Signal:	± 1 V ± 2 V (Option 031)
Impedance:	50 Ω
Coupling:	AC
Input Signal Bandwidth:	10 kHz - 70 MHz

Input Filters:

Number:	2
Passband:	DC ≥ *f* ≥ 26 MHz
Passband Flatness:	± 1.0 dB
Stopband:	*f* ≥ 38 MHz
Stopband Attenuation:	> 50 dB
Bypassing:	may be inserted or removed from circuit through jumper placement

Analog to Digital Converters:

Number:	2 (one on option 001; single channel)
Type:	Analog Devices AD6640
Resolution:	12 bits
Sampling Rates:	5 MHz to 65 MHz
Spurious Components:	– 70 dB
SINAD:	> 60 dB
Signal/Noise Ratio:	> 50 dB > 60 dB (Option 031)

Sampling Clock:

Internal:	64 MHz crystal oscillator installed, jumper selectable and user replaceable. Other frequencies available by special order.
External:	
Connector:	Front Panel SMA
Input Impedance:	50 Ω
Coupling:	AC
Bandwidth:	10 - 65 MHz
Signal Levels:	Single-Ended or Differential (Jumper selection) Positive, negative or bipolar signals can be applied.
Amplitude:	min: 500 mV_{P-P} max: 5 V_{P-P}
Logic:	TTL, ECL or Analog Signal

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1.8 Specifications (continued)

Power:

+ 5 V_{DC}:	1.00 A
+12 V_{DC}:	0.75 A
– 12 V_{DC}:	1.00 A

Dimensions:	Standard 6U VMEbus board
Depth:	160.0 mm (6.3 in.)
Height:	233.5 mm (9.2 in.)
Panel Width:	20.3 mm (0.8 in.)

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Chapter 2: Installation and Connections

2.1 Inspection

After unpacking the unit, inspect it carefully for possible damage to connectors or components. If you discover any damage, please contact Pentek immediately, at (201) 818–5900. Please save the original shipping container and packing material, in case reshipment is required.

2.2 Jumper and Switch Configurations

All user–selectable operating parameters of the Model 6465 are controlled by the settings of jumper blocks and DIPswitches on the PC board. Jumper blocks JP1, JP2, JP3, JP4 and JP6 are dual–inline, surface–mounted components. Jumper Blocks JP5, JP7 and JP8 (there is no jumper block JP8 on Option 008) are single–in–line surface–mount. Pin 1, for both styles of jumper blocks, is indicated on the board both by the numeral '1' and by a notched corner on the screened symbol beneath the block.

The pin numbering scheme for the dual–inline surface–mount jumper blocks is shown in Figure 2–1, below. The shorting jumpers used with these jumper blocks are low profile, and have their pins spaced on 2 mm centers. The Pentek part number for the jumpers that fit these blocks is 356.00015.

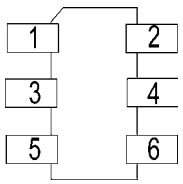


Figure 2–1: Model 6465 –Dual–In–Line Jumper Block Pin Numbering

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2.2 Jumper and Switch Configurations (continued)

The shorting jumpers used with single inline surface-mount jumper blocks have their pins spaced on 0.1 inch centers. The Pentek part number for the jumpers that fit these blocks is 356.00001.

If the jumpers supplied with your unit should become lost, contact Pentek at (201) 818–5900, and we will gladly replace them for you.

The Model 6465 contains two jumper blocks for each channel that determine whether or not the low-pass, anti-aliasing input filter is present in the circuit. Another jumper block, common to both channels, configures the board to accept either a single-ended or differential reference clock signal from the front panel's EXT CLK IN connector (if this signal path is enabled). Some configurations have an additional jumper block that determines whether the output data is registered or not. One of the two DIPswitch blocks (SW1) determines the quantity that the reference clock will be divided by to create the sampling clock frequency, and the other (SW2) performs several configuration functions. The locations of the jumper blocks, DIPswitches, and other circuit elements of interest for the TTL, FPDP and ECL options are shown in Figures 2–2, on Page 13, respectively. Settings for the jumper blocks and DIPswitches will be discussed in the following sections.

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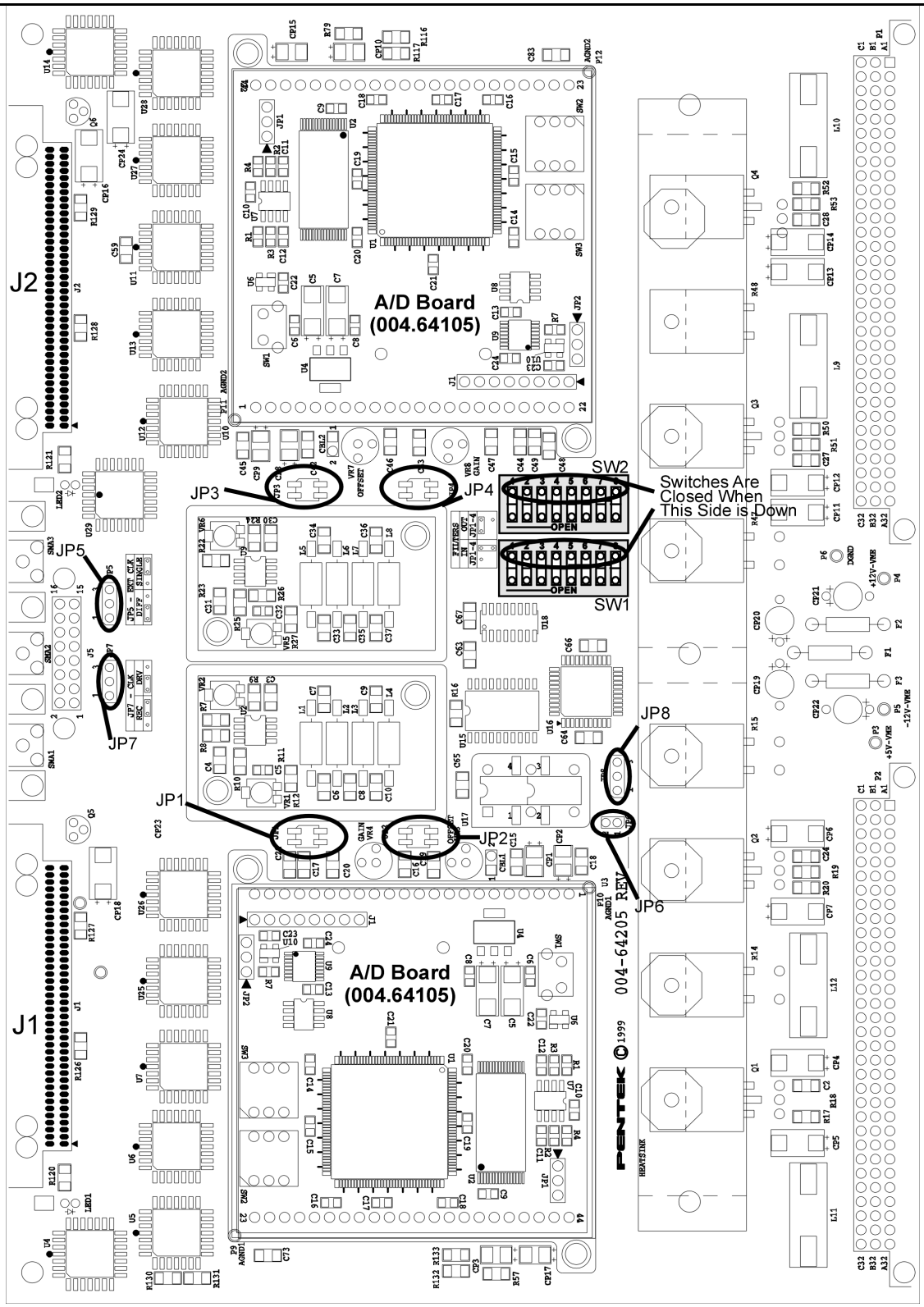


Figure 2-2: Model 6465 –PC Board drawing showing jumper block and component locations

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2.2 Jumper and Switch Configurations (continued)

2.2.1 Filter Install/Bypass Jumper Blocks - JP1 thru JP4

The factory default configuration of these jumper blocks is to have the filters installed. This means that jumpers are installed between pins 1 & 2 of all four of these jumper blocks (JP1 & JP2 for channel 1, and JP3 & JP4 for channel 2). To bypass the filter (i.e., remove it from the circuit and allow the full band-width of the input signal to pass), place the jumpers between pins 1 & 3 at all four locations. The fourth pin on these jumper blocks is unused. Figure 2-3, below, shows how the jumpers are positioned in the input circuit. Table 2-1, below the figure, summarizes the settings. There also is a chart included on the 6465 PC card, between the DIPswitches and the filter for channel 2, that shows how to set these jumpers.

A jumper **MUST** be installed on each of these four jumper blocks, and both jumper blocks for a given channel must have the jumper installed in the same position, or no signal will be delivered to the A/D Converter.

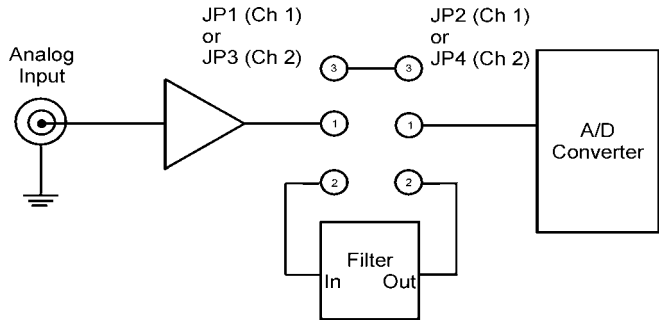


Figure 2-3: Model 6465 –Filter Install/Bypass Jumpers

Table 2-1: Model 6465 –Filter Install/Bypass Jumpers –JP1 & JP2 (Channel 1) and JP3 & JP4 (Channel 2)

Jumper Position	Filter State
1 –2*	Installed*
1 –3	Bypassed
* –Factory default Setting **Note:** Pin 4 is unused on all four jumper blocks.	

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2.2 Jumper and Switch Configurations (continued)

2.2.2 Clock Input Type Select Jumper Block - JP5

Jumper block JP5 allows you to configure the board for either a single-ended or differential clock input signal. If a jumper is installed between pins 1 & 2 of JP5, the shielded, outer portion of the front panel's EXT CLK IN connector is isolated from ground and connected to the "–" input of a line receiver. This allows the Model 6465 to receive a differential clock signal. (The above is also true if no jumper is installed on JP5.)

If a jumper is installed between pins 2 & 3 of JP5, then the shield of the input connector and the "–" input of the line receiver are grounded. In this configu–ration, the Model 6465 accepts single–ended signals at this connector. Note that if this input connector will be used, a jumper MUST be installed in one of the two positions on this jumper block. If no jumper is installed on JP5, the shield and the receiver's "–" input simply float, which will result in poor sig–nal integrity.Table 2–2, below, summarizes the settings of jumper block JP5. There is also a chart on the 6465 PC card, between the front panel EXT CLK IN connector and the filter networks, that shows how to set this jumper.

Table 2-2: Model 6465 –External Clock Type Select Jumper –JP5

Signal Type	Jumper position
Single-Ended*	2 –3*
Differential	1 –2
* Factory Default Setting	

2.2.3 Oscillator Disable Jumper - JP6

JP6 is a 2-pin jumper block which, when a jumper is installed, connects the on-board crystal oscillator to the +5 V supply rail. When using the A/D converter with an external clock signal, this jumper should be removed to disable the on-card oscillator, which can add unwanted frequency components to the digitized output signal if left active. Table 2-3, below, summarizes the settings of JP6.

Table 2-3: Model 6465 –Oscillator Disable Jumper –JP6

Jumper Installed*	Jumper removed
Oscillator Enabled*	Oscillator Disabled
Install to use Internal Sample Clock	Remove to use External Sample Clock
* –Factory default setting	

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2.2 Jumper and Switch Configurations (continued)

2.2.4 Sample Rate Divider DIPswitch - SW1

The sampling clock for the Model 6465 is created by passing a reference clock signal through a frequency divider. The reference clock signal is either the on-board crystal oscillator, whose frequency is 64 MHz in the standard configuration, or a signal applied to the EXT CLK IN connector on the unit's front panel. The reference clock is selected by one of the switches on the SW2 DIPswitch block, and will be discussed in the Section 2.2.5 on Page 18. The divider is set by SW1.

SW1 is a DIPswitch block containing eight switches. Each of these eight switches carries a binary weight, from 2^0 (=1, the switch closest to the filters) to 2^7 (=128, the switch closest to the heatsink). A switch in the SW1 block is closed when the side of the switch nearest to SW2 is down. The locations of SW1 and SW2 is shown in Figure 2-2 on Page 13. Closing a switch clears the bit associated with it to the logic '0' state, and opening a switch sets the associated bit to the logic '1' state.

The clock divisor is equal to the binary value of the settings of these eight switches plus one. Thus, there are 256 different divisor settings that can be achieved with this switch, from 1 to 256. If the on-card, 64 MHz oscillator is used as the reference clock source, this allows for 256 different sample clock rate settings, from 64 MHz to 250.00 kHz. Table 2-4 on Page 17, gives the switch settings for the 16 highest frequencies available using the on-card oscillator, the frequencies that will be obtained when each of the upper four switches is the only one opened, and when all are opened.



NOTE

The Minimum Sample Rate on the Model 6465 is 5 MHz.

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2.2 Jumper and Switch Configurations (continued)

2.2.4 Sample Rate Divider DIPswitch - SW1 (continued)

Table 2-4: Model 6465 –Sample Clock Divider –DIPswitch SW1 –Sample Frequencies Using 64.00 MHz Reference Clock

Switch # & Setting (0 = Closed, 1 = Open)								Clock Divider	Sample Frequency
8	7	6	5	4	3	2	1		
0	0	0	0	0	0	0	0	1	64.000 MHz
0	0	0	0	0	0	0	1	2	32.000 MHz
0	0	0	0	0	0	1	0	3	21.333 MHz
0	0	0	0	0	0	1	1	4	16.000 MHz
0	0	0	0	0	1	0	0	5	12.800 MHz
0	0	0	0	0	1	0	1	6	10.667 MHz
0	0	0	0	0	1	1	0	7	9.143 MHz
0	0	0	0	0	1	1	1	8	8.000 MHz
0	0	0	0	1	0	0	0	9	7.111 MHz
0	0	0	0	1	0	0	1	10	6.400 MHz
0	0	0	0	1	0	1	0	11	5.818 MHz
0	0	0	0	1	0	1	1	12	5.333 MHz
0	0	0	0	1	1	0	0	13	4.923 MHz
0	0	0	0	1	1	0	1	14	4.571 MHz
0	0	0	0	1	1	1	0	15	4.267 MHz
0	0	0	0	1	1	1	1	16	4.000 MHz
0	0	0	1	0	0	0	0	17	3.765 MHz
0	0	1	0	0	0	0	0	33	1.939 MHz
0	1	0	0	0	0	0	0	65	984.615 kHz
1	0	0	0	0	0	0	0	129	496.124 kHz
1	1	1	1	1	1	1	1	256	250.000 kHz

NOTE

The Minimum Sample Rate on the Model 6465 is 5 MHz.

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2.2 Jumper and Switch Configurations (continued)

2.2.5 Device Configuration DIPswitch - SW2

The DIPswitch labeled SW2 may be used to configure certain operating modes of the Model 6465. SW2 Switch 6 and 8 are unused. Settings for the remaining switches are dependent on the digital receiver used.

A switch in the SW2 DIPswitch block is closed when the side farthest from SW1 is pressed down. For reference, Switch 8 is closest to the heatsink. The subsections below describe the functions of each switch in the SW2 DIPswitch block. Switches 1 and 7 are discussed first, since there are conditions in which their combined settings are important. Factory default settings for SW2 are shown in Table 2-5, below.

Table 2-5: Model 6465 –Device Specific, Factory Preset DIPswitch Settings –SW2

Switch #	Function	Setting
1	Reference Clock Select	Closed (0)
2 & 3	Time & Channel Packing (Opt. 008 Only)	Open (1)
4	Channel 1 Edge Select	Closed (0)
5	Channel 2 Edge Select	Closed (0)
6	Reserved	Closed (0)
7	External Input Function Select	Open (1)
8	Reserved	Open (1)

2.2.5.1 Reference Clock Select - SW2, Switch 1

This switch determines whether the internal, 40 MHz crystal oscillator or a signal applied to the front panel's EXT CLK IN connector is used as the source of the reference clock. The reference clock is delivered to the clock divider, programmed by SW1 (see Section 2.2.4 for details), whose output is used as the sampling clock signal.

To select the 40 MHz on-card oscillator as the reference clock source, switch 1 on the SW2 DIPswitch must be closed. To select the signal applied to the EXT CLK IN connector on the front panel, switch 1 on the SW2 DIPswitch must be open. Note that if the external source is to be used as the reference, switch 7 of SW2 must be open, to select the clock reference function for the input (see Section 2.2.5.2).

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2.2 Jumper and Switch Configurations (continued)

2.2.5 Device Configuration DIPswitch - SW2 (continued)

2.2.5.2 Center Connector Function Select - SW2, switch 7

The SMA connector at the center of the Model 6465's front panel, labeled EXT CLK IN, can function either as a clock reference input, a sample clock output, or as an enabling gate signal for the internal sampling clock. The setting of the second switch from the end of the SW2 DIPswitch helps to determine the function of this connector.

To use the EXT CLK IN connector as a reference clock input or as a sampling clock output, switch 7 on SW2 must be open, to select the reference function for the input. See Section 2.2.2 for further information about selecting the reference clock input or sample clock output functions for this connector.

To use the EXT CLK IN connector as a sampling gate signal input, switch 7 of SW2 must be closed. In this case (unless your unit includes Option 101), the internal clock reference must be selected (since a clock reference signal and a gate signal cannot both be delivered through the same connector), by closing switch 1 of SW2.

Table 2-6, below, summarizes the settings of switches 1 and 7 of DIPswitch block SW2.

Table 2-6: Model 6465 –Reference Clock and External Input Function Select Switch Settings –SW2, Switches 1 & 7

Switch 1 Setting	Switch7 Setting	Reference Source	Ext. Input Function	Sample Clock Operating Mode
Closed (0)	Closed (0)	Internal	Gate	Gated Internal Clock
Closed (0)	Open (1)	Internal	Reference	Internal Clocking-No Gate
Open (1)	Closed (0)	External	Gate	Gated External Clock **(Option 101 Only)**
Open (1)	Open (1)	External	Reference	External Clocking - No Gate

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2.2 Jumper and Switch Configurations (continued)

2.2.5 Device Configuration DIPswitch - SW2 (continued)

2.2.5.3 Data Transfer Edge Select - SW2, Switches 4 & 5

Switches 4 and 5 are used to invert the Output Clock with respect to the data outputs. These switches are factory set according to the clock edge on which the data is transferred from the A/D Converter chip used on the card.

Setting switch 4 to the open position (1) inverts the Output Clock of Channel 1. Setting switch 5 to the open position (1) inverts the Output Clock of Channel 2. This function may be useful for custom interfacing.

The Model 6465 provides a registered output mode, in which the output timing relationships are fixed.

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2.3 Model 6465 Front Panel

The Model 6465's Front Panel contains three coaxial SMA connectors. One of these is for a common, externally applied reference clock or sampling gate signal, and the other two are the analog signal input connectors for the two channels. Also available through the front panel are two male, 80-pin flat ribbon cable connectors, each of which carries the data outputs from both channels. The subsections below discuss the characteristics of the signals that may be applied to the input connectors, as well as those available at the output connectors.

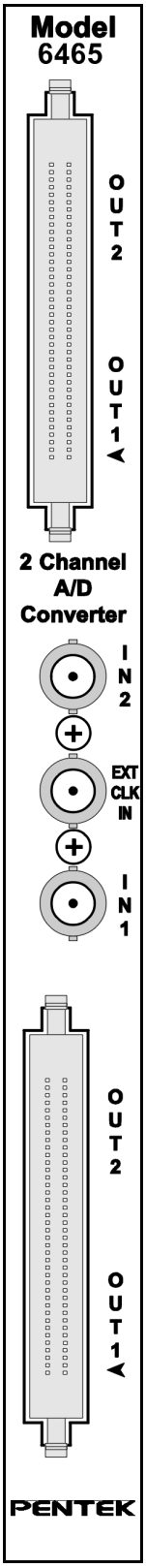


Figure 2-4: Model 6465 - Standard Front Panel

2.3.1 Analog Input Connectors

The Front Panel SMA connectors labeled IN1 and IN2 are the Analog inputs to the Model 6465. The SMA connector nearer to the top of the panel is the input to ADC channel 2, and the one nearer the bottom of the panel is the input to ADC channel 1.

The load impedance presented by these input connectors is 50 Ω. With low impedance devices, like the Model 6465, it is not necessary to use a terminator on unused analog input channels to prevent signal interference. The input signal range is ± 1 V, i.e., a signal level of + 1 V produces full scale positive output data (0x7FF), and a signal level of – 1 V produces full scale negative output data (0x800). (See Section 2.3.3 for details about output data coding.) Input signal bandwidth for specified performance is from 10 kHz to 32.5 MHz with the input filter bypassed (see Section 2.2.1). With the input filter installed, input bandwidth is reduced to 26 MHz.

2.3.2 External Clock Input

The SMA connector at the center of the Model 6465's front panel, labeled EXT CLK IN, is for an external reference signal, which may be frequency divided to produce the sample clock. This input is selected as the ADC's sample clock when switch 1 of DIPswitch block SW2 is open (see Section 2.2.5).

This input connector is terminated in a 50 Ω impedance and biased at ≅ 2.5 V_{DC}. The level shifted signal then drives the input of a TTL receiver, which produces the CONVERT signals sent to the A/D Converter card.

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2.3 Model 6465 Front Panel (continued)

2.3.2 External Clock Input (continued)

Here, the CONVERT signal is delivered to a transformer which produces the ENCODE and $\overline{\text{ENCODE}}$ signals used by the ADC chip.

The network described previously allows the 6465's clock input to be driven with either ECL, TTL , or an RF sinusoidal signal. The minimum recommended signal amplitude at this input is 2 V_{P-P}, and the maximum amplitude is 5 V_{P-P}. The minimum external clock rate is typically 5 MHz (to obtain specified performance), and the maximum frequency for an external reference clock signal to the Model 6465 is 65 MHz.

The 6465's external clock or enabling gate input may be driven by either TTL or ECL level logic signals, or by an analog signal. At frequencies greater than 20 MHz it may be necessary to AC couple the clock. (AC coupling termination in BNC or SMA packages are widely available).

2.3.3 Data Outputs

The data output connectors on the standard configuration of Pentek's Model 6465 are designed to mate with the Narrowband data input connectors (Channels A & B) on Multiband Digital Receiver Module models 6514 (option 012), 6526 (option 002) and 6532 (option 012). The pin assignments for this configuration are shown in the table at the left side of Figure 2-5 on Page 24. This figure also shows the connector pin numbering scheme and gives part numbers for the mating connectors. An 80-wire ribbon cable with two 80-pin connectors is available from Pentek as Model 2117.

While the Model 6465 is a 12-bit A/D converter, models 6514 (option 012), 6526 (option 002) and 6532 (option 012) have a 16-bit input stages. For this reason, the output data lines have been arranged at the data connector such that the 12 most significant input bits of the digital receivers are driven by the outputs from the 6465. In other words, the D11 output from a 6465 drives the D15 input of these digital receivers, and the 6465's D0 outputs drive the D4 inputs.

The 6465 can also be used with the Model 4271 (Option 012) Digital Receiver MIX Module, and the standard version of the Model 4272 (Option 012), if a special cable is used. This is necessary because the 6465's connectors contain 80 pins each, while those on the digital receivers contain only 68 pins. An 80-pin to 68-pin ribbon cable is available from Pentek as Model 2119; this cable can also be used to connect the 6465 to Pentek Models 6504 and 6509 Digital Receivers. This cable may also be used to connect to the Wideband input (Channel C) on the 4272 (Option 012); **IF AND ONLY IF THE OUTPUT STAGE OF THE 4272 (Option 012) IS DISABLED**. If you will be using the 6465 as a front end for a 4272 (Option 012) and need to drive the Wideband input and use the outputs, please contact our factory at the phone number shown on this manual's cover page to discuss custom cabling.

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2.3 Model 6465 Front Panel (continued)

2.3.3 Data Outputs (continued)

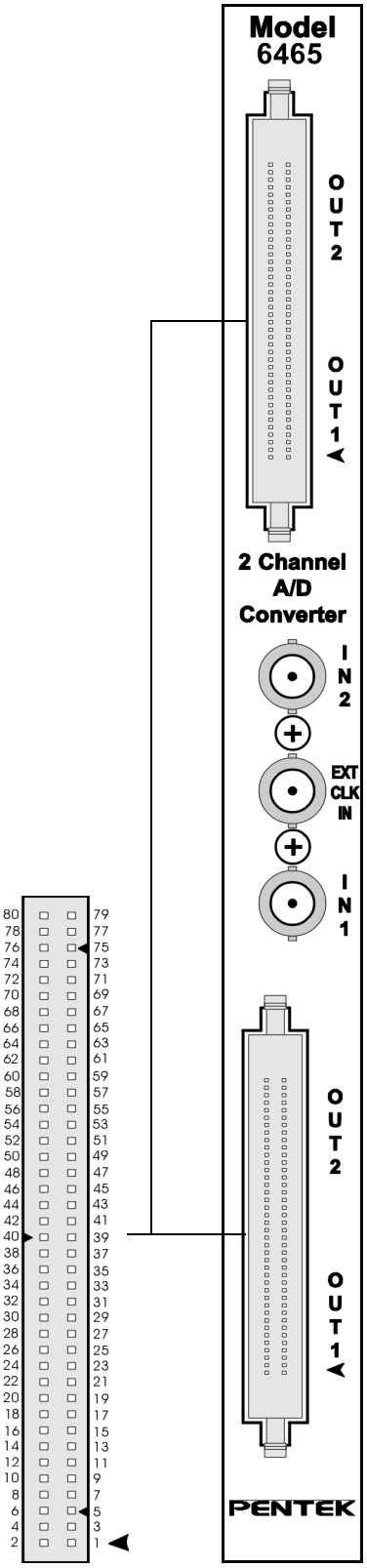
Table 2-7: Model 6465 –Output Data Coding

Input Voltage (DC, Nominal)	Binary Output Code (D11 –D0)	Hexadecimal Output Code
–1.00000 V	1000 0000 0000	0x800
-0.99951 V	1000 0000 0001	0x801
-0.99902 V	1000 0000 0010	0x802
⋮	⋮	⋮
-0.00049 V	1111 1111 1110	0xFFE
0.00000 V	1111 1111 1111	0xFFF
+0.00049 V	0000 0000 0000	0x000
+0.00098 V	0000 0000 0001	0x001
⋮	⋮	⋮
+0.99902 V	0111 1111 1101	0x7FD
+0.99951 V	0111 1111 1110	0x7FE
+1.00000 V	0111 1111 1111	0x7FF

The output devices on the standard Model 6465 are 74FCT-type gates. The output data is encoded in true 2's complement format. The MSB (D11) is used as a sign bit and indicates a negative input voltage when set to the logic '1' state. All 12 bits are set to the '1' state to indicate a half scale input (i.e., 0 V_{DC}). The 11 LSB's are decremented to indicate increasing negative input voltages with the maximum negative input voltage (– 1 V_{DC} for the standard input signal range) resulting in an output data code of 1000 0000 0000 (0x800). An input exactly one step above half scale (≅ + 490 μV_{DC} for the standard input signal range) produces an output code of all 12 bits cleared to the logic '0' state and a full-scale positive input voltage (+ 1 V_{DC} for the standard input signal range) produces an output data code of 0111 1111 1111 (0x7FF). Table 2-7, at the top of this page, summarizes the output data coding scheme used by the Model 6465.

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Pin Assignments for 6465 Top and Bottom Output Connectors			
80	ECL High	79	ECL Low
78	ECL High	77	ECL Low
76	ECL High	75	ECL Low
74	GND	73	GND
72	ECL High	71	ECL Low
70	ch 2 –$\overline{CK}$	69	ch 2 –CK
68	ch 2 –$\overline{AS}$	67	ch 2 –AS
66	ch 2 –$\overline{SS}$	65	ch 2 –SS
64	ch 2 –$\overline{D11}$ out (MSB)	63	ch 2 –D11 out (MSB)
62	ch 2 –$\overline{D10}$ out	61	ch 2 –D10 out
60	ch 2 –$\overline{D9}$ out	59	ch 2 –D9 out
58	ch 2 –$\overline{D8}$ out	57	ch 2 –D8 out
56	ch 2 –$\overline{D7}$ out	55	ch 2 –D7 out
54	ch 2 –$\overline{D6}$ out	53	ch 2 –D6 out
52	ch 2 –$\overline{D5}$ out	51	ch 2 –D5 out
50	ch 2 –$\overline{D4}$ out	49	ch 2 –D4 out
48	ch 2 –$\overline{D3}$ out	47	ch 2 –D3 out
46	ch 2 –$\overline{D2}$ out	45	ch 2 –D2 out
44	ch 2 –$\overline{D1}$ out	43	ch 2 –D1 out
42	ch 2 –$\overline{D0}$ out (LSB)	41	ch 2 –D0 out (LSB)
40	GND	39	GND
38	ECL High	37	ECL Low
36	ch 1 –$\overline{CK}$	35	ch 1 –CK
34	ch 1 –$\overline{AS}$	33	ch 1 –AS
32	ch 1 –$\overline{SS}$	31	ch 1 –SS
30	ch 1 –$\overline{D11}$ out (MSB)	29	ch 1 –D11 out (MSB)
28	ch 1 –$\overline{D10}$ out	27	ch 1 –D10 out
26	ch 1 –$\overline{D9}$ out	25	ch 1 –D9 out
24	ch 1 –$\overline{D8}$ out	23	ch 1 –D8 out
22	ch 1 –$\overline{D7}$ out	21	ch 1 –D7 out
20	ch 1 –$\overline{D6}$ out	19	ch 1 –D6 out
18	ch 1 –$\overline{D5}$ out	17	ch 1 –D5 out
16	ch 1 –$\overline{D4}$ out	15	ch 1 –D4 out
14	ch 1 –$\overline{D3}$ out	13	ch 1 –D3 out
12	ch 1 –$\overline{D2}$ out	11	ch 1 –D2 out
10	ch 1 –$\overline{D1}$ out	9	ch 1 –D1 out
8	ch 1 –$\overline{D0}$ out (LSB)	7	ch 1 –D0 out (LSB)
6	ECL High	5	ECL Low
4	ECL High	3	ECL Low
2	ECL High	1	ECL Low



The mating flat cable socket connector is 3M #82080-6006, and the strain relief is 3M #3858-080.

Two of each of these items are supplied with the Model 6441.

The recommended 0.025" pitch flat cable is 3M #3756/80

Figure 2-5: Model 6465 –Front Panel Output Connectors

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2.4 Single Channel Model 6465 A/D Converter - Option 001

Model 6465 can also be ordered in a single channel version as option 001.

2.5 Inserting the Model 6465 in the VMEbus Card Cage

Align the Model 6465 card edge with the card cage guides and push evenly on both ejector handles until the front panel seats against the upper and lower rails. Secure the unit to the cage by tightening the upper and lower retainer screws in the front panel.

2.6 Removing the Model 6465 from the VMEbus Card Cage

Loosen the upper and lower retaining screws; they are captive screws and will remain part of the panel assembly. Gently push both ejector handles apart (away from the center of the panel) until the unit unseats itself from the cage connectors. Then pull outward to remove the unit.



Never insert or remove the Model 6465 while power is applied in the card cage

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AppendixA: Model 6465 Option 031

A.1 Option 031

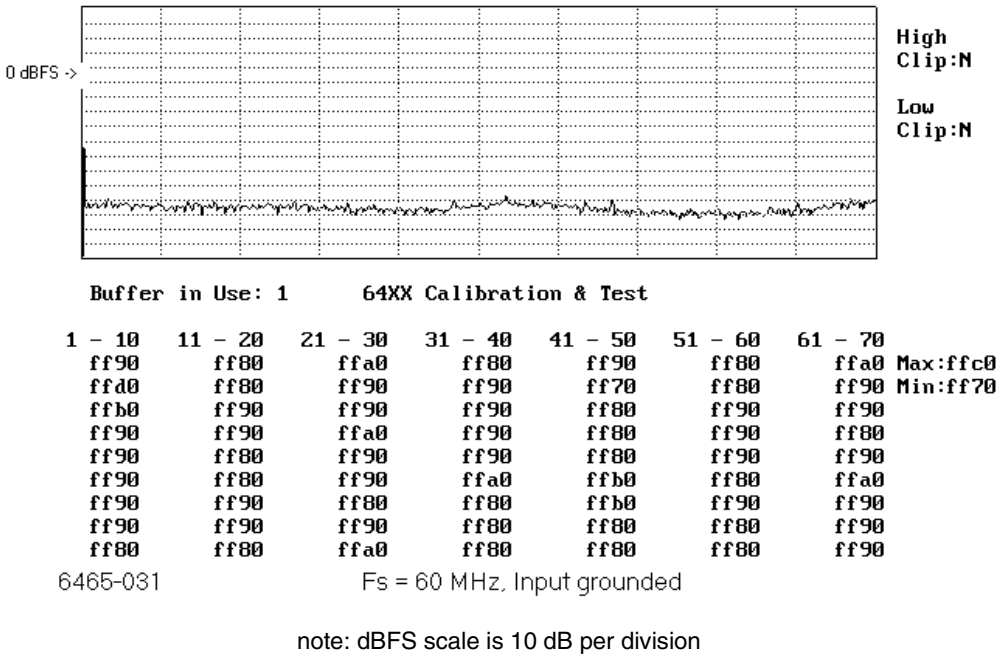
Model 6465 Option 031 provides additional shielding and removes the low pass filter. Other specification changes are:

Input full scale voltage:	2 Vp-p +/- 5%
Large Signal BW:	80 MHz
Small Signal BW:	120 MHz
SNR:	60 dB
Intermodulation Distortion:	-80 dBFS

The following sections contain figures which illustrate some of the performance characteristics of Model 6465 Option 031. These characteristics are provided for reference only; the given results should be considered typical, but, cannot be guaranteed. For further information on Option 031 please contact Pentek at (201) 818-5900.

A.1.1 Model 6465 - Option 031 - Ground Noise LevelGround Noise Level

Figure A-1, below, shows a reference noise level of the Model 6465 Option 031 with the inputs grounded.



note: dBFS scale is 10 dB per division

Figure A–1: Model 6465 –Option 031 –Ground Noise Level

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A.1 Option 031 (Continued)

A.1.2 4 MHz

Figure A-2, below, shows a 4MHz input frequency sampled near the highest sample rate to show the noise content inherent in the input signal

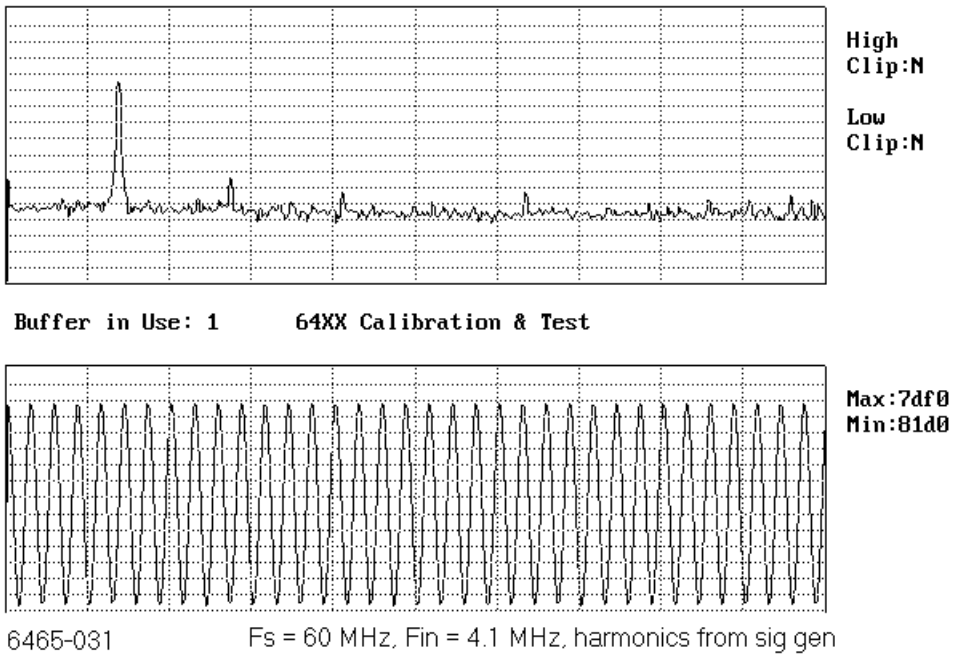


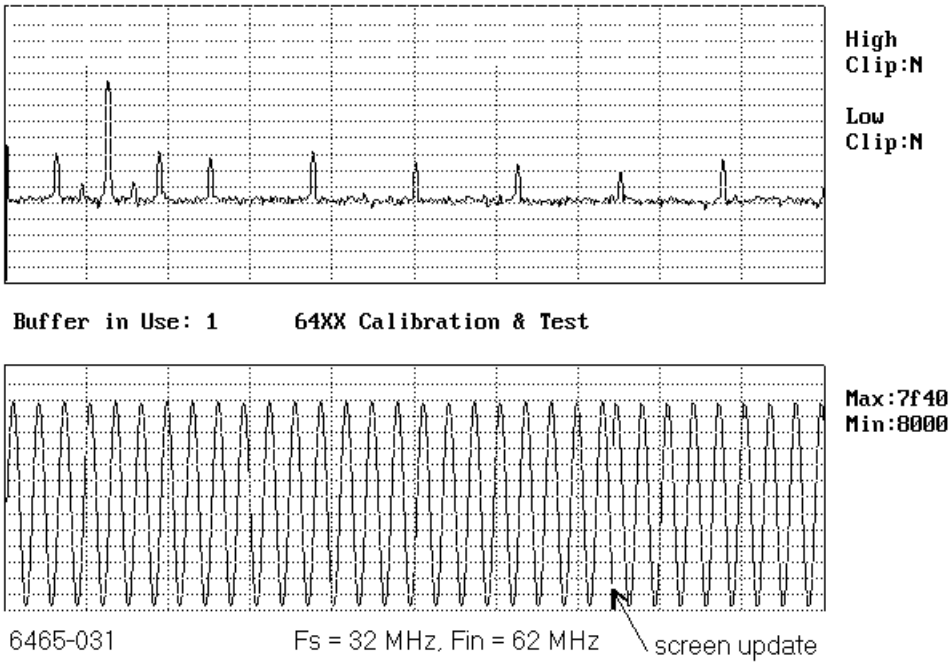
Figure A-2: Model 6465 –Option 031 – 4 MHz

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A.1 **Option 031** (Continued)

A.1.3 62 MHz

Figure A-3, below, shows the noise content inherent a 62MHz input frequency.



note: dBFS scale is 10 dB per unit division

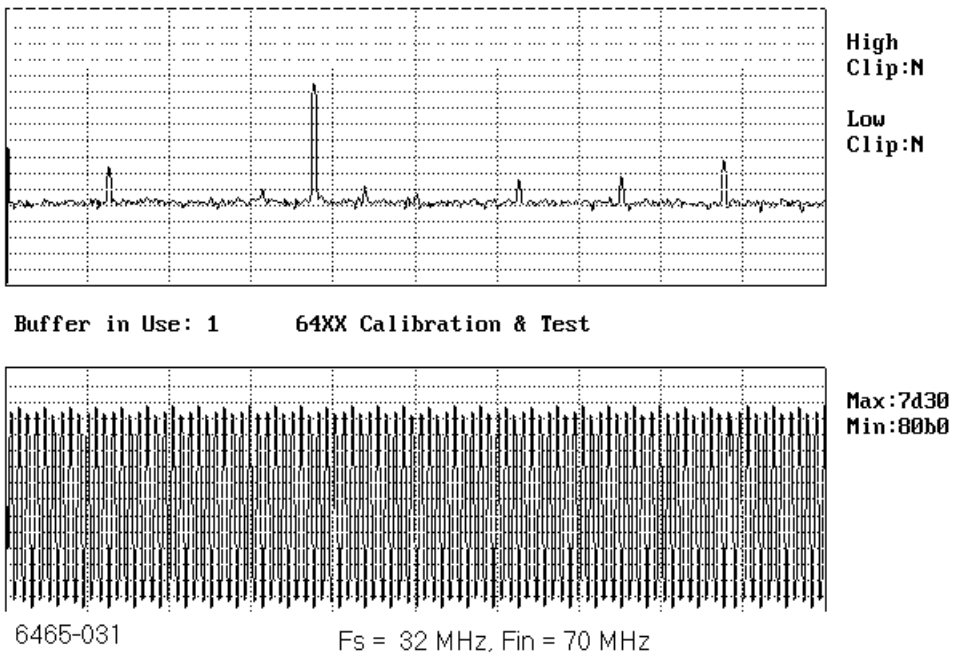
Figure A-3: Model 6465 –Option 031 – 62 MHz

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A.1 **Option 031** (Continued)

A.1.4 70 MHz

Figure A-4, below, shows the noise content inherent a70 MHz input frequency.



note: dBFS scale is 10 dB per division

Figure A-4: Model 6465 –Option 031 – 70 MHz

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A.1 **Option 031** (Continued)

A.1.5 f_1 high

Figure A-5, below, shows the largest harmonic of a 57 MHz signal.

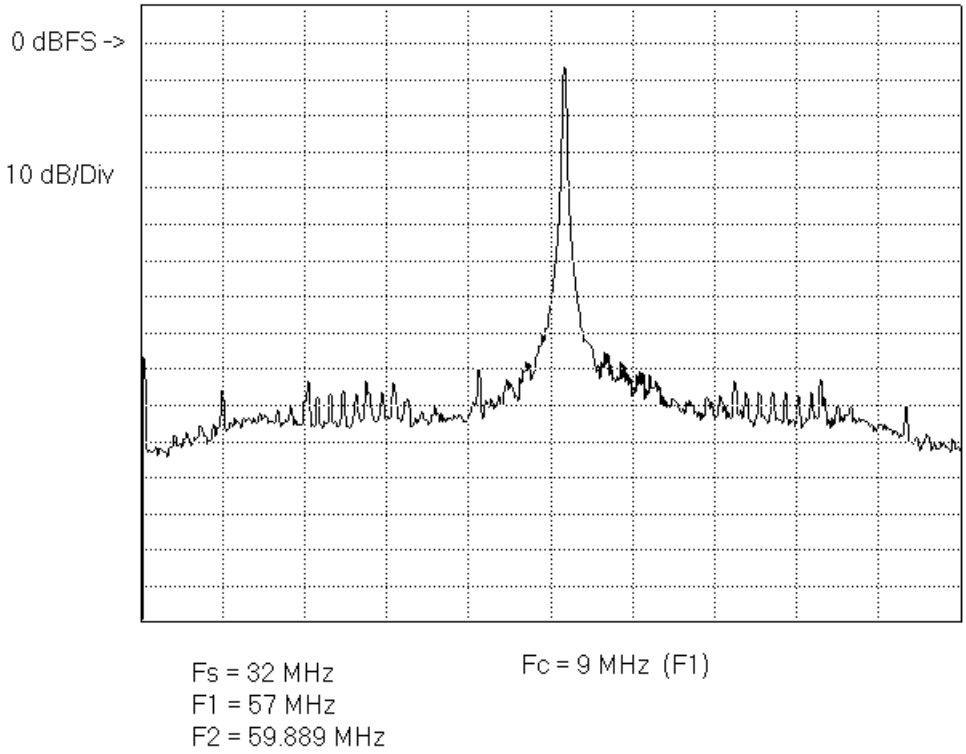


Figure A-5: Model 6465 –Option 031 – f_1 high

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A.1 Option 031 (Continued)

A.1.6 f_2 high

Figure A-6, below, shows the largest harmonic of the 59.889 MHz signal.

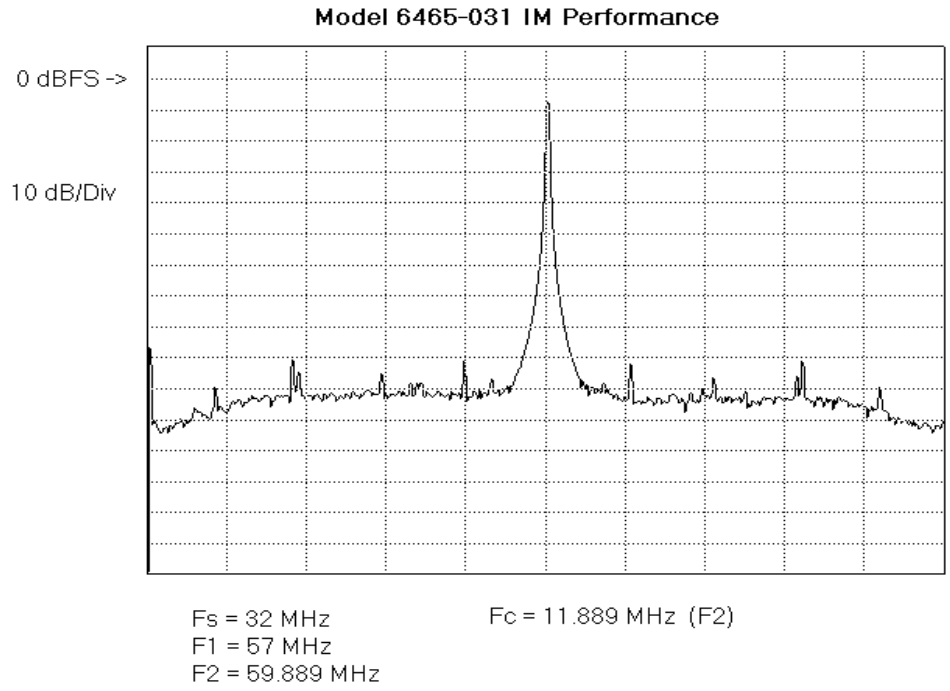


Figure A-6: Model 6465 –Option 031 – f_2 high

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A.1 **Option 031** (Continued)

A.1.7 $f_2 - f_1$ high

Figure A-7, below, shows the largest harmonic resulting from the difference 57 MHz and 59.889 MHz signal.

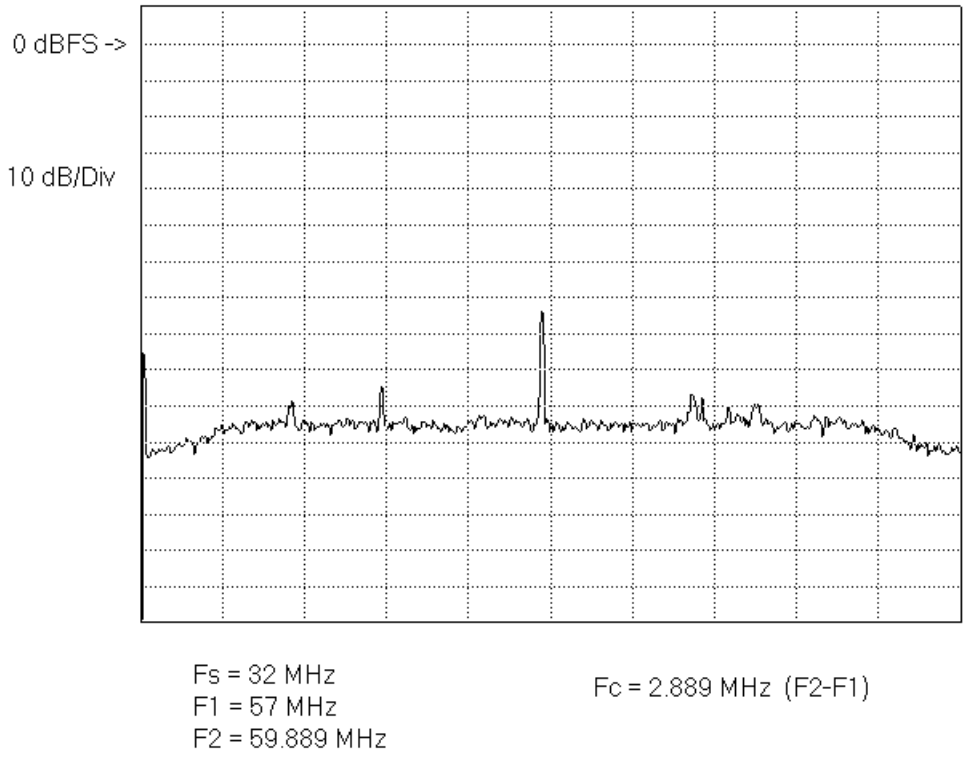


Figure A-7: Model 6465 –Option 031 – f_2 –f_1 high

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A.1 Option 031 (Continued)

A.1.8 $f_1 + f_2$ high

Figure A-8, below, shows the largest harmonic resulting from the sum of 57 MHz and 59.889 MHz signal.

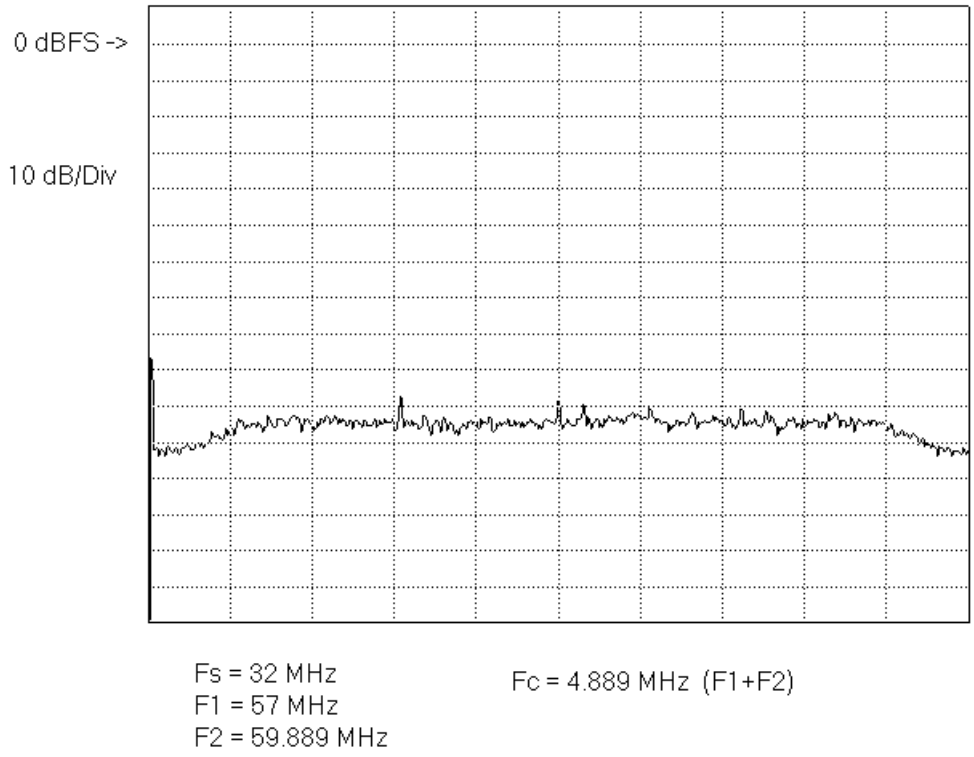


Figure A-8: Model 6465 –Option 031 – $f_1 + f_2$ high

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A.1 **Option 031** (Continued)

A.1.9 $2f_1 - f_2$ high

Figure A-9, below, shows the largest harmonic resulting from the difference of (2 * 57 MHz) and 59.889 MHz signal.

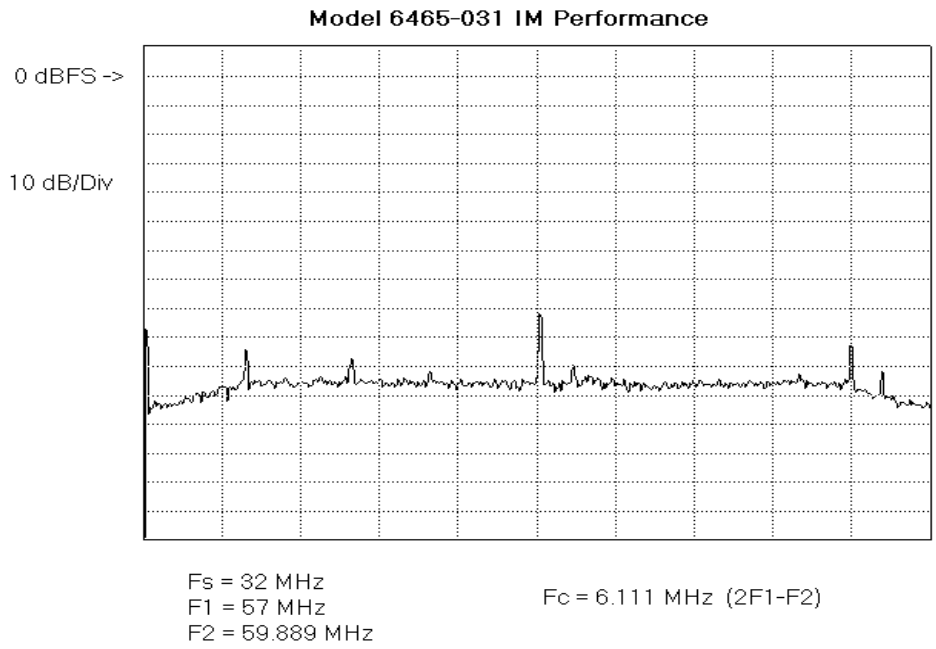


Figure A-9: Model 6465 –Option 031 – $2f_1 - f_2$ high

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A.1 Option 031 (Continued)

A.1.10 $2f_2 - f_1$ high

Figure A-10, below, shows the largest harmonic resulting from the difference of (2 * 59.889 MHz) and 57 MHz signal.

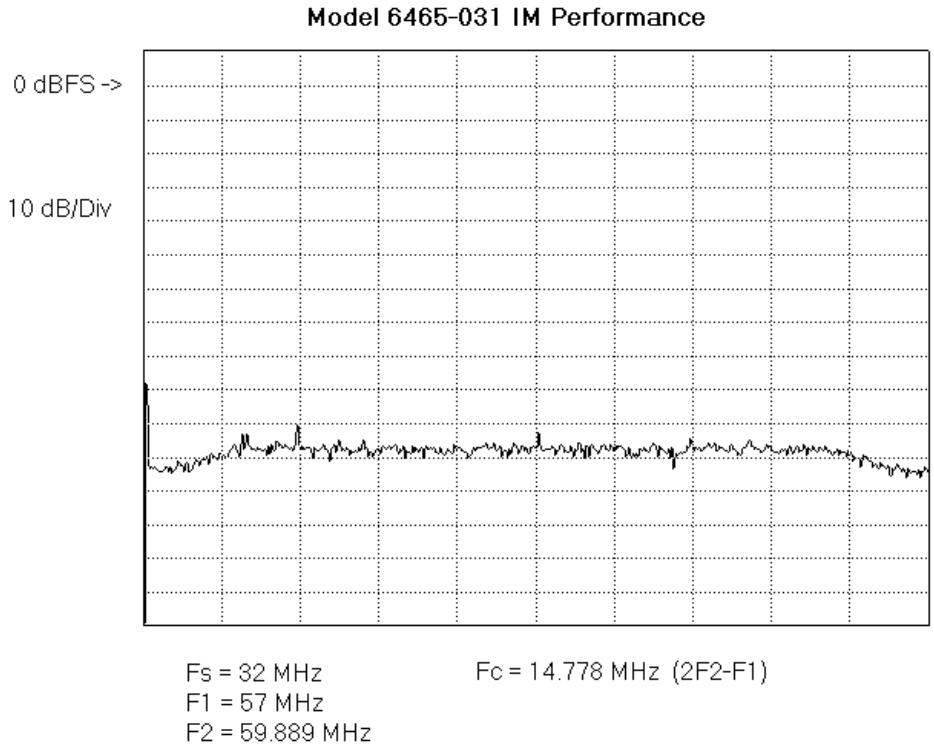


Figure A-10: Model 6465 –Option 031 – $2f_2 - f_1$ high

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A.1 **Option 031** (Continued)

A.1.11 $f_2 + f_1$ low

Figure A-11, below, shows the highest harmonic resulting from the sum of 3.953 MHz and 5.017 MHz signal.

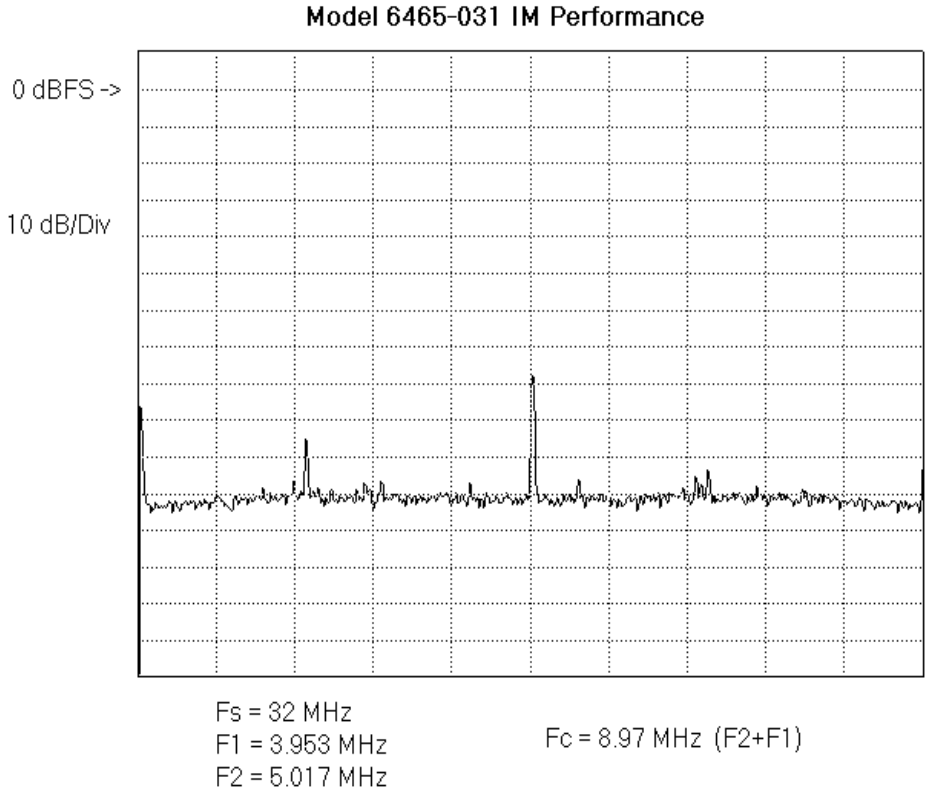


Figure A–11: Model 6465 –Option 031 – $f_2 + f_1$ low

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A.1 **Option 031** (Continued)

A.1.12 $f_2 - f_1$ low

Figure A-12, below, shows the highest harmonic resulting from the difference of 3.953 MHz and 5.017 MHz signal.

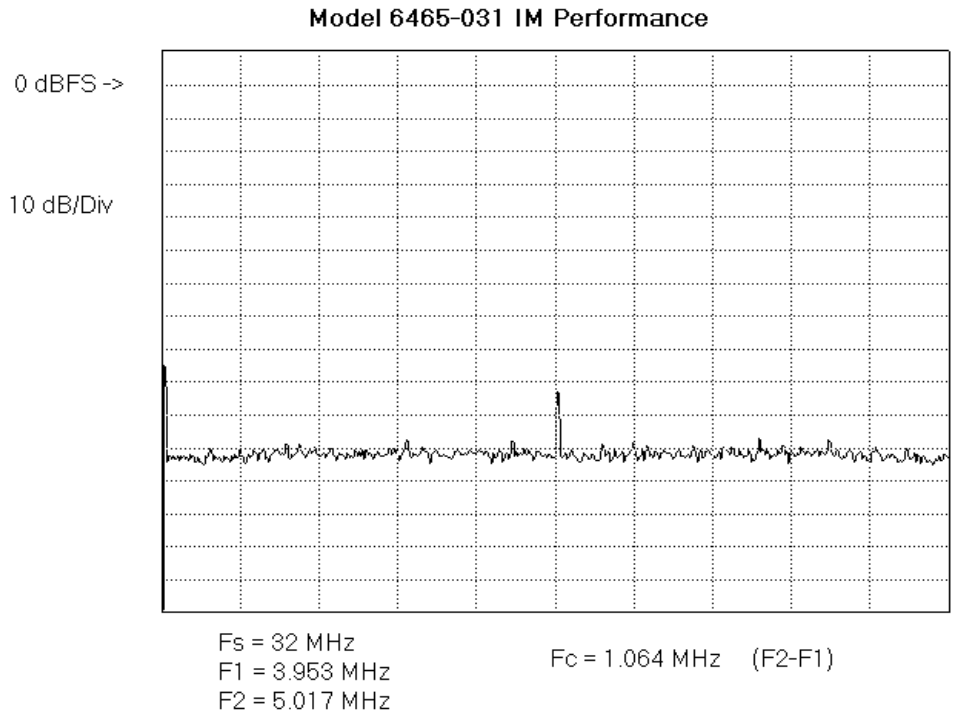


Figure A-12: Model 6465 –Option 031 – f_2 –f_1 low

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A.1 **Option 031** (Continued)

A.1.13 $2f_2 - f_1$ low

Figure A-13, below, shows the highest harmonic resulting from the difference of (2*5.017 MHz) and a 3.953 MHz signal.

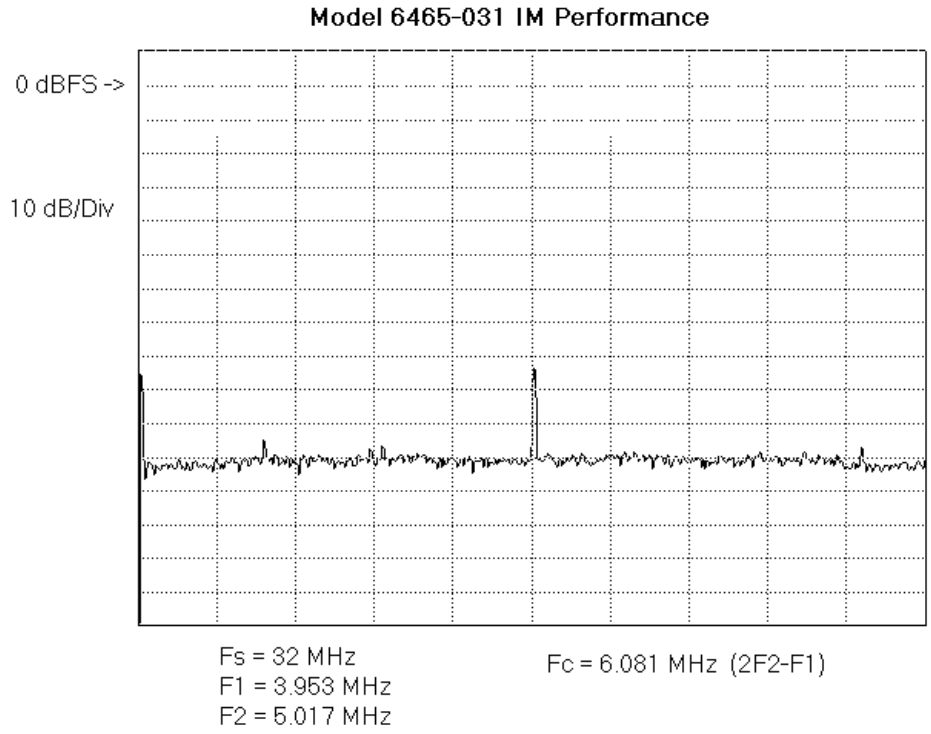


Figure A-13: Model 6465 –Option 031 $-2f_2 - f_1$ low

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A.1 **Option 031** (Continued)

A.1.14 $2f_2 - f_1$ low

Figure A-14, below, shows the highest harmonic resulting from the difference of (2*5.017 MHz) and 3.953 MHz signal.

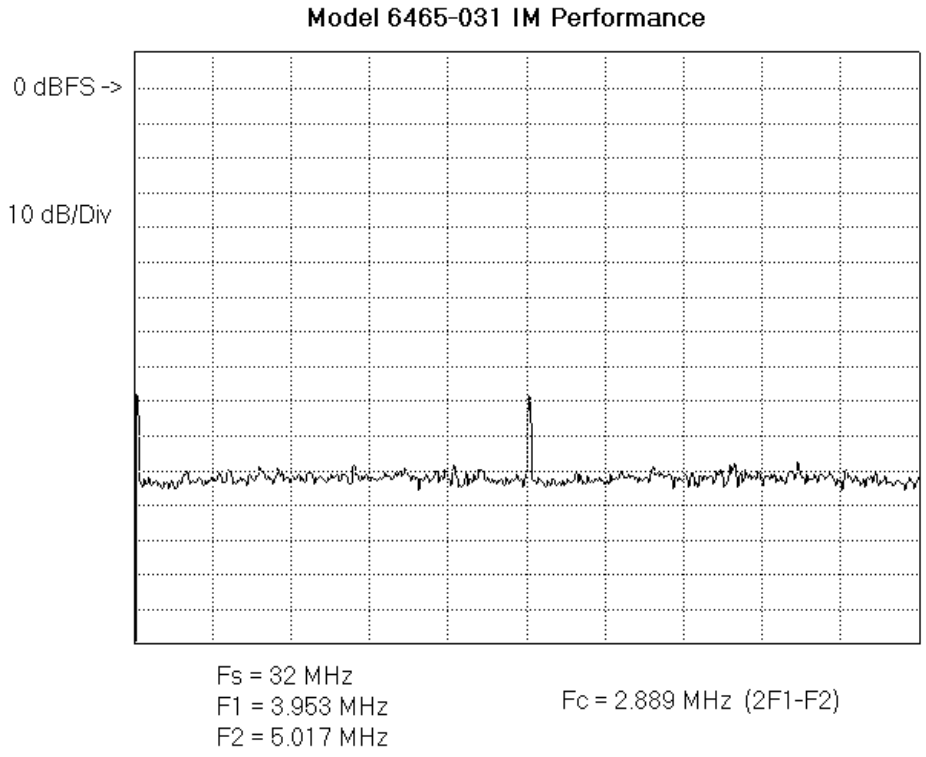


Figure A-14: Model 6465 –Option 031 – $2f_2 - f_1$ low

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