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Pentek Model 7106 - RACEway Interface PMC Module

P.1 General Information

The Model 7106 is a PMC (PCI Mezzanine Card) module incorporating a complete RACEway interface to the PCI bus. It is designed to be installed on a VMEbus board equipped with a PMC module site whose PMC P4 connector is routed to the VMEbus P2 connector, per the PMC module specification.

This device utilizes the PXB Bridge chip, from Mercury Computer Systems and Cypress Semiconductor. Complete programming information for this device can be obtained from Mercury's PXB Bridge Specification, included with this shipment

P.1.1 PCI Interface

The PCI bus is the electrical interface between the PMC module and the VME board circuitry, often supporting a CPU running a popular operating system such as VxWorks or UNIX. The electrical characteristics of the PCI bus, commonly used in desktop personal computers, define the 32-bit parallel synchronous bus operating at peak rates of 132 MBytes/sec.

P.1.2 RACEway Interface

RACEway is a high-speed synchronous backplane bus capable of delivering 32-bit words between VME boards at a peak rate of 160 MBytes/sec. Data is typically sent in packets of 2 Kbytes, with each packet containing the necessary routing and destination address information to steer it to a unique destination.

RACEway offers a significant advantage for VMEbus systems by providing an independent, high-speed data channel completely independent of the VMEbus. RACEway utilizes the 64 user-defined pins of VME P2 backplane connector, which are normally unconnected pins in most backplane designs.

In order to join the RACEway busses of two or more boards, a circuit board containing RACEway data switches and sockets which mate with the 64 pins of P2 must be installed. These assemblies are called RACEway Interlink Modules (ILKs) and come in sizes which bridge 4, 8, and 16 VMEbus slots.

The RACEway switches on the ILKs are called RACEway Crosspoint switches. Each crosspoint switch connects six separate RACEway busses, automatically routing the data packets from one bus to any other based on the routing header in the packet. The ILKs can support multiple 160 MByte/sec RACEway transfers simultaneously, depending on the number of slots and crosspoint switches utilized.

P.1 General Information (continued)

P.1.3 Applications

The Model 7106 can provide a high-speed RACEway interface for a variety of popular host PMC carriers including Alpha, PowerPC, Pentium, SPARC, and DSP processor boards for VMEbus.

P.2 Jumper Block Settings

The subsections beginning at the top of the next page describe those operating conditions on the Pentek Model 7106 that are defined by the placement of jumpers on the printed circuit board. Figure P-1, below, is a picture of the 7106 board, showing the locations of the jumper blocks discussed in the subsequent sections. The arrows in the figure point to pin 1 of the jumper blocks. With the board oriented as shown in the figure below, the odd-numbered pins in the dual inline jumper blocks (JB1 - JB3) are in the top row, and the even-numbered pins are on the bottom.

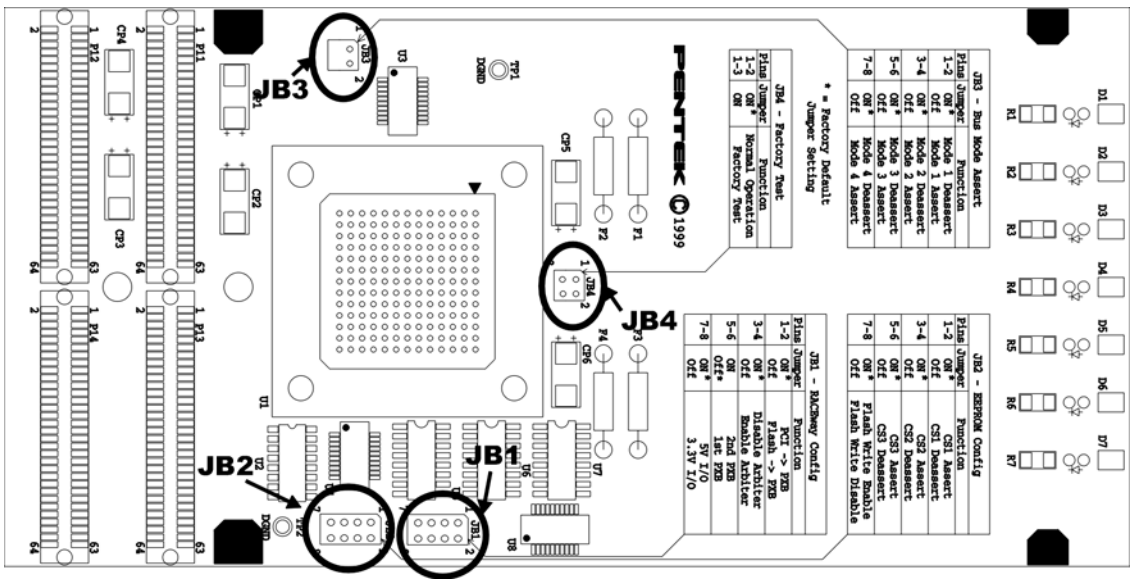


Figure P-1: Model 7106 PC board, showing Jumper Block locations

P.2 Jumper Block Settings (continued)

P.2.1 RACEway Configuration Jumper Block (JB1)

Jumper block JB1 contains four jumper positions that affect the initialization and operation of the RACEway interface. The individual jumper positions are discussed in the subsections below, and are summarized in Table P-1, at the top of the next page.

P.2.1.1 PXB Load Source Select Jumper (Pins 1 - 2)

Pins 1 and 2 on jumper block JB1 select the source of configuration data for the PXB bridge. When a jumper is installed between these two pins, configuration data is loaded from the PCI bus. When this jumper is removed, configuration data is loaded from the on-card Flash EEPROM. The factory default setting for this jumper is installed, selecting PCI as the configuration source.

P.2.1.2 Internal Arbiter Disable Jumper (Pins 3 - 4)

Pins 3 and 4 on jumper block JB1 are used to enable or disable the PXB chip's internal arbiter. The arbiter is disabled when a jumper is installed between these two pins, and is enabled when the jumper is removed. The factory default setting for this jumper is installed, disabling the internal arbiter.

P.2.1.3 Primary PXB Select Jumper (Pins 5 - 6)

Pins 5 and 6 on jumper block JB1 are used to determine whether the PXB chip on a given 7106 is the primary PXB device in a given system. The factory default setting for this jumper is removed, indicating that this card is the primary PXB bridge. Install a jumper here if another device will be the primary PXB Bridge, and this card will act as a Secondary Bridge.

P.2.1.4 RACEway Interface I/O Level Select Jumper (Pins 7 - 8)

Pins 7 and 8 on jumper block JB1 select the logic levels used for I/O signals on the RACEway Interface. The factory default setting for this jumper, installed, selects 5V RACEway logic levels. Remove this jumper if your interlinks require 3.3V logic levels.

P.2 Jumper Block Settings (continued)

P.2.1 RACEway Configuration Jumper Block (continued)

Table P-1: Model 7106 - RACEway Configuration Jumper Block - JB1			
Jumper Pins	**Jumper State**	**Configuration**	**Default**
1 - 2	Installed	**Load PXB from PCI**	Installed
	Removed	Load PXB From Flash EEPROM	
3 - 4	Installed	**Disable Internal Arbiter**	Installed
	Removed	Enable Internal Arbiter	
5 - 6	Installed	Secondary PXB	Removed
	Removed	**Primary PXB**	
7 - 8	Installed	**5V RACEway I/O**	Installed
	Removed	3.3V RACEway I/O	

P.2.2 Flash EEPROM Jumpers (JB2)

The four jumper positions on jumper block JB2 determine the operating parameters for the Flash EEPROM on the Model 7106, which is a type 24F128. The three jumpers at pins 1 - 2, 3 - 4 and 5 - 6 are connected to the three EEPROM chip selects, and must all be installed to select the EEPROM (this is the factory default setting). Removing any of these three jumpers will de-select the EEPROM. The jumper at pins 7 - 8 is connected to the Flash EEPROM's Program Protect input. By default, a jumper is installed here, allowing write operations to the Flash EEPROM. To enable Program protection (i. e., disable writes), remove this jumper.

P.2.3 PCI Bus Mode Select Jumper (JB3)

Jumper block JB3 selects the PCI bus Mode. Installing a jumper asserts the $\overline{\text{Bus Mode}}$ signal (i. e., pulls it low), and removing the jumper de-asserts the signal (pulls it high).

Table P-2: Model 7106 - Bus Mode Jumpers (JB3)			
Jumper Pins	**Bus Mode Signal**	**Default**	**Function**
1 - 2	$\overline{\text{Bus Mode 1}}$	Installed	Jumper On = Signal High (de-asserted); Jumper Off = Signal Low (asserted)

⚠ CAUTION: **Some earlier revisions of the Model 7106 may have pins 3 though 8 on JB3; these should not be used and may cause damage to the board if a jumper is installed between any of them. Other revisions may have directions for installing jumpers for pins 3 through 8 printed on the board, but no pins available. These directions may be disregarded.**

P.2 Jumper Block Settings (continued)

P.2.4 Factory Testing Jumper (JB4)

Jumper block JB4 is reserved for factory testing purposes. For normal use, the jumper on this block should always be positioned between pins 1 and 2.

P.3 Initialization Code

```
#define VME_FIFO_PMC_1  0xb0010000
#define VME_FIFO_PMC_2  0xb0014000
#define RACEway_port_B 0xb0100000
#define RACEway_port_C 0xb0140000
#define RACEway_port_D 0xb0180000
#define RACEway_pci_port_B 0x400000
#define RACEway_pci_port_C 0x500000
#define RACEway_pci_port_D 0x600000
   if (device_id1 == 0x00010000)
   {
       if (bridge_mode == 1)
       {
          swap_write_cfg(pmc1_addr+0x10,0x10880827L);
                                                  /* PXB bridge control */
          swap_write_cfg(pmc1_addr+0x11,0x00700000L);
                                               /* Mem map internal base */
          swap_write_cfg(pmc1_addr+0x12,0x00001113L);
                                                 /* BAR size register  */
          swap_write_cfg(pmc1_addr+0x13,0x00000000L);
          swap_write_cfg(pmc1_addr+0x14,0x00000000L);
          swap_write_cfg(pmc1_addr+0x15,0x00000000L);
          swap_write_cfg(pmc1_addr+0x16,0x00000000L);
          swap_write_cfg(pmc1_addr+0x17,0x00000000L);
          swap_write_cfg(pmc1_addr+0x18,0x710612f0L);
          swap_write_cfg(pmc1_addr+0x19,0x00000200L);
          swap_write_cfg(pmc1_addr+0x1a,0x00000000L);
          swap_write_cfg(pmc1_addr+0x00,0x00011134L);
          swap_write_cfg(pmc1_addr+0x01,0x04800007L);
          swap_write_cfg(pmc1_addr+0x02,0x06000000L);
          swap_write_cfg(pmc1_addr+0x03,0x00010000L);
          swap_write_cfg(pmc1_addr+0x06,0x00030100L);
          swap_write_cfg(pmc1_addr+0x07,0x04800111L);
          swap_write_cfg(pmc1_addr+0x08,0x00800070L);
          swap_write_cfg(pmc1_addr+0x09,0x00600040L);
          swap_write_cfg(pmc1_addr+0x0a,0x00000000L);
          swap_write_cfg(pmc1_addr+0x0b,0x00000000L);
          swap_write_cfg(pmc1_addr+0x0c,0x00000000L);
          swap_write_cfg(pmc1_addr+0x0d,0x00000000L);
          swap_write_cfg(pmc1_addr+0x0e,0x00000000L);
          swap_write_cfg(pmc1_addr+0x0f,0x00000100L);
          swap_write_cfg(pmc1_addr+0x104,0x00004000L);
                                                    /* Allow 2k burst */
```

P.3 Initialization Code (continued)

```
        for (i=0; i<16; i++)
        {
           swap_write_cfg(pmc1_addr+0x140+(i*0x4),0xc0000000L);
           swap_write_cfg(pmc1_addr+0x142+(i*0x4),0xe0000000L+(long)i);
        }
        swap_write_cfg(pmc1_addr+0x150,0xc0000000L);
                                                  /* Route "B" page 0 */
        swap_write_cfg(pmc1_addr+0x152,0x80000004L);
                                                  /* Return route "D" */
        swap_write_cfg(pmc1_addr+0x154,0xa0000000L);
                                                  /* Route "C" page 1 */
        swap_write_cfg(pmc1_addr+0x156,0x80000005L);
                                                  /* Return route "D" */
        swap_write_cfg(pmc1_addr+0x158,0x80000000L);
                                                  /* Route "D" page 2 */
        swap_write_cfg(pmc1_addr+0x159,0x80000006L);
                                                  /* Return route "D" */
    }
}
```

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