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OPERATING MANUAL

MODEL 7140

Dual–Channel Multiband Transceiver
PMC/XMC Module

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Manual Revision History

Date	Revision	Comments
6/30/05	Preliminary	Initial release.
7/29/05 to 1/17/08		Updated Sync Bus diagram & description. Board/Channel Reset Reg, removed all channel reset bits. DMA Command/Status Regs, added bit D06, Burst Mode. Reorganized Chapter 6 by functional area. Misc. Control Reg, removed bit D00, Test FIFO Enable. Defined User bits in System Interrupt Regs. Added Trigger Capture bit D05 to ADC, DDC, & DAC FIFO Status & Interrupt Mask Regs. Added ADC Pre Trigger Count Capture Regs. Removed Delay Memory Trigger Length Regs. Moved Vendor Datasheets to a separate document, 809.71400. Application Interrupt Regs, changed bit D10 to 'TRIGGER CAPTURE'. Added Delay Memory Bank 2 Last Address Registers. Miscellaneous Control Reg, changed bit D02 name to Endianness. Added Core Option Register. Corrected Option 100 Clock Spec. Corrected Virtex Config Register bits. DMA Descriptor Transfer Count Regs, added note to Chain bit D31. Added Flag bits to FIFO Status Registers. DMA Command/Status Reg, added DAC Buffering bit D15. Updated LM83 & ADM1024 sensor limits. Added Delay Memory Trigger Address Registers. Changed SYNC/GATE connector ERNI part number per KBCase 1308. Changed description of DMA operation. Added bit D01 Test Ramp to Misc Control Reg. Corrected Memory Bank Depth. **For 7140 boards with PCI7140 revision date of 6/20/06 or greater (PCI7140 Revision Reg., Sect 5.5):** Chapter 5, removed Local Interrupt Flag & Enable Registers, added PCI DCM Control Register, added Local DMA Request Status Register, added DMA PCI Interrupt Enable/Flag Register. Added bit D14, PCI Address, & changed bit D06, Burst Mode, in DMA Command/Status Reg. Corrected DAC FIFO sizes. Sect 1.14, updated baseline FPGA usage percentages. Sect 1.17, corrected input clock range to 1 to 300 MHz. Sect 2.3.3, updated XMC connector specs and pinout. Sect 6.14, added description of GC4016 internal register address space. Sect 2.5, corrected Pentek part # for JTAG PCB to 004.71402. Table 7–10, corrected DAC data format.
11/10/08	A	Manual released, Revision A. Sect 2.5, added Xilinx JTAG J4 connector for Pentek JTAG PC Rev B.
10/16/09	A.1	Sect 2.4, added note for 3.3V and 5V power supplies. Sect 2.5, updated for Rev B JTAG PCB. Sect 5.17.3, corrected Transfer Interval Count description.
2/8/10	A.2	Sect 4.7, corrected and expanded description of Delay Memory Operation. Sect 6.17.3, corrected and expanded description of Delay Memory R/W Address Registers. Table 6–70 & Table 6–71, added information.
9/9/10	A.3	Sect 6.10.1.9 & 6.10.4.9, added note about selecting an external clock per KBCase 1361.
9/14/12	A.4	Sect 5.6.7, clarified use of bits D0 & D1 for FPGA reconfiguring.

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Chapter 1: Introduction

1.1 General Description

The Pentek Model 7140 is a complete software radio transceiver suitable for connection to HF or IF ports of a communications system. Using the PMC (PCI Mezzanine Card) module format, it includes two A/D and two D/A converters capable of bandwidths greater than 40 MHz. The Model 7140 supports the emerging VITA 42 XMC standard with optional switched fabric interfaces.

The Model 7140 module can be attached directly to any digital signal processing (DSP) baseboard equipped with a PMC expansion site, such as the Pentek Models 4205 and 4295 VMEbus baseboards.

1.2 Features

- ❑ Complete Software Radio Transceiver
- ❑ VITA 42.0 XMC compatible with switched fabric interfaces
- ❑ Two 80–MHz or 105–MHz, 14–bit A/D converters
- ❑ Four digital downconverters
- ❑ One digital upconverter with two 500–MSPS, 16–bit D/A converters
- ❑ 512 MBytes of DDR SDRAM
- ❑ Xilinx® Virtex–II Pro™ Series FPGA
- ❑ Up to 2.56 seconds of delay or data capture at 100 MHz
- ❑ Dual timing buses for independent input and output clock rates
- ❑ LVDS timing bus can synchronize multiple modules
- ❑ 32 pairs of LVDS connections to the Virtex–II Pro FPGA for custom I/O
- ❑ Extended temperature and conduction–cooled versions available
- ❑ PMC Module format compatible with VME, cPCI, and PCI platforms

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1.3 Block Diagram

The following is a simplified block diagram of the Model 7140 digital transceiver.

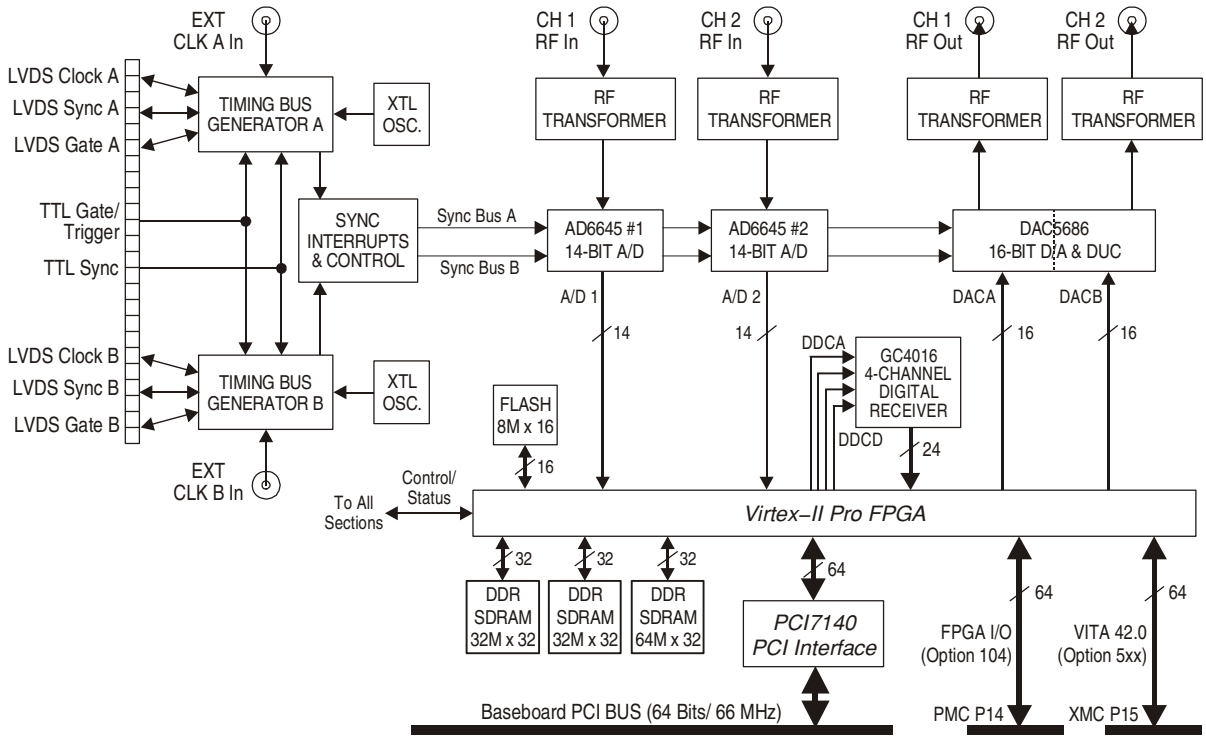


Figure 1–1: Model 7140 Block Diagram

The following defines the different uses of the term 'Channel' in this manual (refer also to the block diagram above).

- **Analog Input Channels** — There are two analog input channels, one for each analog RF input, identified as A/D 1 and A/D 2, corresponding to the RF inputs labeled CH 1 and CH 2 IN on the front panel.

- **Digital Receiver Channels** — There are four digital receiver channels in the TI Graychip GC4016 DDC, identified as DDC A through DDC D.

- **Analog Output Channels** — There are two digital upconverter output channels in the DAC5686, identified as DAC A and DAC B, corresponding to the RF outputs labeled CH 1 and CH 2 OUT on the front panel.

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1.4 Principle of Operation

The Model 7140 is a complete software radio transceiver suitable for direct connection to HF or IF ports of a communications system. Using the popular PMC/XMC module format, it includes two A/D and two D/A converters.

The 7140 is compatible with VITA 42 XMC carrier boards. This emerging standard provides up to four 4x serial data links between the XMC and the carrier. These links support Serial RapidI/O, PCI Express and Aurora protocols and provide a dedicated high−speed streaming data path.

The 7140 features a Xilinx® Virtex−II Pro™ XC2VP50 Field−Programmable Gate Array. The FPGA can be pre−configured with one of a variety of optional IP cores to provide signal translation, processing and time delay functions. In addition to pre−configured functions, user−created FPGA programming is supported by Pentek's GateFlow® Designer's Kit, Model 4953 Option 140. FPGA I/O connections are provided through the optional PMC P4 connector (Option 104).

The 7140 includes a large 512−MByte block of DDR SDRAM. This memory is con−trolled by the FPGA and is organized as two 128−MByte banks, 32 Mbyte deep by 32 bits wide and one 256−MByte bank, 64 Mbytes deep and 32 bits wide. Separate banks (separate address and data per bank) allow simultaneous access to all banks. This memory can be used as buffer memory when transferring data between board resource or to off−board resources.

Dual A/D converters provide input to a FPGA, where the data can be formatted, pro−cessed or routed to board resources including the GC4016 quad digital downconverter. The board design provides a dual channel feedback path between the FPGA and the digital downconverter, allowing signals that have been processed or time delayed inside of the FPGA to be sent to the digital downconverter's input.

Dual D/A converters include both interpolation filters and an upconverter stage capa−ble of producing base band I & Q, quadrature modulation, and single−sideband upconversion analog output.

The module includes dual onboard crystal oscillators for clocking, but can also accept external clocks through a pair of front panel MMCX connectors. The 7140 is equipped with a dual LVDS front panel clock and sync bus that can synchronize up to eight modules with built−in master/termination functions. The bus format is compatible with other Pentek PMC and VIM modules and will work with the Model 9190 Clock and Sync Distribution Amplifier for synchronizing up to 80 modules.

The 7140 is available in extended temperature and conduction−cooled ruggedized ver−sions (Option 70x).

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1.5 Analog to Digital Input Conversion

The Model 7140 is designed for a maximum input sampling frequency of 105 MHz, with a minimum sampling rate of 30 MHz. It accepts two analog RF inputs at +4dBm full scale into 50 ohms on front panel MMCX connectors. Each of the two inputs is transformer coupled, and digitized by an Analog Devices AD6645 14−bit, 80−MHz (optionally 105−MHz) A/D converter. The outputs of the A/Ds are delivered, in par−allel, to the FPGA through two 14−bit paths.

1.6 Digital Receivers

The Model 7140 includes one Texas Instruments Graychip GC4016 quad narrowband digital receiver chip. The GC4016 accepts four 14−bit parallel or three 16−bit inputs from the FPGA. The FPGA provides data paths to the GC4016 and supports both 14−bit and 16−bit input modes. A crossbar switch inside the GC4016 allows each of the four receiver channels to independently select any input source. The FPGA determines the source of GC4016 input data. These sources include the A/D converters, FPGA signal processing engines, SDRAM delay memory, and data sources on the PCI bus.

The GC4016 delivers a real or complex parallel data stream into the FPGA for process−ing and formatting. This path allows raw A/D data to be routed to the GC4016, or sig−nals that have been processed or time delayed inside of the FPGA to be sent to the digital downconverter's input. This architecture supports applications like tracking receivers.

The maximum input sampling rate, Fs, for the GC4016 is specified at 100 MHz. The receiver includes four independently tunable receiver channels capable of tuning throughout the DC to Fs/2 range with output bandwidths ranging from 0.8·Fs/N (for the standard 80% FIR filter), where the decimation factor, N, ranges from 32 to 16,384. For an input sampling clock of 100 MHz, this bandwidth range becomes approximately 5 kHz to 2.5 MHz. By combining two or four channels, output bandwidth of up to 5 to 10 MHz can be achieved.

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1.7 Digital to Analog Output Conversion

The Model 7140 is designed with a maximum output sample rate of 320 MHz in upconverter mode and 500 MSPS in D/A only mode. One Texas Instruments DAC5686 is used to produce a pair of analog outputs capable of operating in D/A only, quadrature modulation, and single−sideband upconversion modes. The D/A has built−in interpolation filters settable to 2x, 4x, 8x, and 16x.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs through two 320 MHz 16−bit D/A converters to two front panel MMCX connectors at +4dBm full scale into 50 ohms.

In D/A only mode the DAC5686 acts as a dual interpolating 16−bit D/A producing two independent outputs with output sampling rates up to 500 MSPS. In modes that include frequency translation, the DAC5686 accepts real or complex inputs and produces an upconverted and interpolated, real or complex single output.

1.8 FPGA Digital Interfaces

The Model 7140 includes one Xilinx Model XC2VP50 Virtex−II Pro Field−Programmable Gate Array (FPGA). The FPGA connects to the PMC PCI interface on the baseboard, and serves as a control and status engine for the module with data and programming interfaces to each of the onboard resources including the two AD6645 A/D converters, the GC4016 DDC, and the DAC5686 D/A converter.

Each AD6645 A/D delivers real or complex parallel data streams into the FPGA, where data is formatted and multiplexed for delivery across the PCI interface to any processor on the PMC baseboard. The AD6645 digital outputs can be routed directly to the GC4016 DDC for digital downconverting.

The FPGA also receives digital data across the PCI interface from the baseboard. The FPGA then formats the 16−bit digital samples for delivery to a Texas Instruments DAC5686 Digital to Analog Converter.

The FPGA is factory programmed by Pentek to implement the standard data multiplexing, channel selection, data packing, gating, triggering, and memory control functions specified in this document. The FPGA can be re−programmed from a PMC baseboard processor. Refer to Section 1.14, FPGA Configuration, for additional information about gate array configuration programming.

With Option 104, 32 pairs of LVDS connections are routed from the FPGA to PMC connector P4. These are available to the user for custom I/O.

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1.9 PMC Baseboard Interface

The FPGA is connected to the PMC baseboard through a PCI Master/Slave interface (Standard PCI 2.2 Interface), the Pentek PCI7140. The PCI7140 is a Xilinx Virtex−II XC2V3000 running the Xilinx REAL−PCI 64/66 core.

Through this PCI interface, any processor on the PMC baseboard can receive data from either AD6645, or from any of the four receiver channels from the GC4016. In addition, any processor on the PMC baseboard can send data to the DAC5686 for two channels of output. Any PCI Bus Master can control all programmable features on the board, the two AD6645s, the GC4016, the DAC5686, and all FPGA memory map registers. Data widths of 32 or 64 bits and data rates of 33 or 66 MHz guarantee compatibility with PMC, VME, cPCI, and PCI platforms.

1.10 XMC Baseboard Interface (Option 5xx)

Model 7140 Option 5xx is compatible with VITA 42.0 XMC carrier boards. This emerg−ing standard provides a 4x 2.5 GHz data link between the XMC and the carrier. This link can support switched interconnect protocols including Serial RapidIO and PCI Express. The interface provides a dedicated high−speed streaming data path indepen−dent of the PCI interface.

1.11 Memory

Three independent banks of DDR SDRAM are available for use as delay memory to support transient capture or popular applications such as tracking receivers. Two banks are 128 MBytes each and one bank is 256 MBytes for a total of 512 MBytes of available memory. These banks can be used in cascade or in parallel to support various delay scenarios. For example, with a 100−MHz A/D sample clock, up to 2.56 seconds of delay is available for a single A/D data channel.

Custom user−installed functions within the FPGA can take advantage of the standard SDRAM interface for many other purposes.

The SDRAMs are also available as a resource for the two PowerPC® processor cores within the FPGA. A 16−MByte flash memory supports booting and program store for these processors.

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1.12 Timing and Synchronization

Clocking and synchronization is achieved by using two independent internal timing buses, Sync Bus A and B. These support different clock rates for the input and output signals. Each timing bus includes one clock, one sync, and one gate or trigger signal. Signals from either Sync Bus A or B can be selected as the timing source for the A/Ds, the GC4016 downconverter, the upconverter and D/As.

Two external reference clocks are accepted on front panel MMCX connectors, one for each Sync Bus. Two internal crystal oscillators may be used to supply internal clocks for each Sync Bus.

A front panel 26−pin LVDS Sync Bus connector allows multiple modules to be synchronized.

- In the slave mode, it accepts differential LVDS inputs that drive the clock, sync, and gate signals for the two internal timing buses.

- In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses, for synchronizing multiple modules.

Up to seven slave 7140 modules can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected modules. Up to 80 modules may be synchronized with a Model 9190 Clock and Sync Generator. In addition to the LVDS timing bus, the Model 7140 can receive front panel TTL input signals for gate and trigger functions.

1.13 Interrupts

The Model 7140 has several maskable interrupt sources. PCI interrupts may be generated by A/D converter overload, DMA transfers, FIFO flags, transitions on Sync Bus gate or sync signals, clock loss on either Sync Bus, or a hardware over−temperature or power supply over−voltage.

Onboard sensors constant monitoring of critical voltages and temperatures on the Model 7140 PCB. The sensors are programmable for voltage and temperature limits. If the voltage/temperature fall outside of the set limits, an interrupt can be generated.

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1.14 FPGA Configuration

The Model 7140 includes a Xilinx Model XC2VP50 Virtex−II Pro Field−Programmable Gate Array (FPGA). The Model 7140 is shipped with a default set of logic functions for this FPGA, on JTAG−programmable serial EEPROMs. Upon power−up, this set of default functions is loaded into the FPGA. The baseline functionality consumes about 42% of the XC2VP50.

The XC2VP50 FPGA can be configured with user functions in one of several ways:

- The default configuration is serial configuration from a 32−Mbit configuration EEPROM. This is the mode that the board will come up in at power up. Reprogramming may also be forced at any time through the PMC / PCI interface (see Section 5.6).

- The second method is byte−wide upload from a PMC baseboard processor. This is done by writing the configuration data one byte at a time to the FPGA configuration data register (see Section 5.6). In this way, the FPGA can be rapidly configured for the user's requirement.

- The third method is to configure the FPGA directly via JTAG with a Xilinx Parallel III or MultiLINX™ cable.

- The last method is to overwrite the default configuration by reprogramming the EEPROM at the JTAG interface, and then use the default EEPROM configuration upload.

  NOTE: This last method will permanently overwrite the default configuration supplied by Pentek. The default configuration is supplied with the available GateFlow FPGA Design Kit so that it can be restored if necessary.

The user may modify, add to, or replace the default logic functions on the EEPROMs with user−defined functions. In this way, additional custom hardware signal process−ing can be accomplished. Pentek has an available GateFlow® FPGA Design Kit that provides information that a user requires to modify the programmable logic functions for the FPGA. Pentek offers this as a separate development package, Model 4953 Option 140. Contact Pentek at (201) 818−5900 for details about this package.

With Option 104, the Model 7140 provides I/O connections from 64 FPGA spare pins to the VMEbus through a PMC connector, as described in Section 2.3.2.

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1.15 Board Support Software

The Pentek GateFlow® FPGA Design Kit (Model 4953 Option 140) facilitates user–installed FPGA functions using the Xilinx ISE Foundation tool suite. The FPGA Design Kit allows the user to configure FPGAs for implementing preprocessing functions such as convolution, framing, pattern recognition or decompression. The Pentek GateFlow IP Core Libraries include high–performance receivers, FFTs and pulse compression algorithms. Factory installed IP Cores are available.

Several Pentek software packages are available to speed development tasks for the Model 7140. Pentek's Model 4999 Option 140 ReadyFlow® Board Support Libraries contain a set of C–language routines for the Model 7140 module. Refer to the Ready–Flow documentation for the Model 7140, Pentek part #801.71400.

The following available software drivers allow high–level programming for various workstation platforms. Refer to the software documentation indicated for each.

- Pentek Model 4994 Option 140 Linux® Driver, Pentek document #806.71400.
- Pentek Model 4995 Option 140 Windows® Driver, Pentek document #805.71400.
- Pentek Model 4996 Option 140 VxWorks® Driver, Pentek document #803.71400.

1.16 Supporting Documentation

In addition to the operating instructions provided in this manual, copies of the follow–ing datasheets for the programmable devices on the Model 7140 are provided in the Pentek Model 7140 Supplemental Manual, part number 809.71400. This document is available on the CD provided by Pentek, in file **`80971400.pdf`** (PDF format).

- ❑ Analog Devices, Inc.

  AD6645 A/D Converter Data Sheet, C02647

  ADM1024 System Hardware Monitor Data Sheet, C00059

- ❑ Texas Instruments

  CG4016 QUAD DDC Chip Data Sheet, SLWS133A

  DAC5686 Digital–to–Analog Converter Data Sheet, SLWS147C

- ❑ National Semiconductor Corporation

  LM83 Digital Temperature Sensor Data Sheet, DS101058

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1.17 Specifications

Analog Signal Inputs

Quantity: Two signal inputs, one per A/D converter
Connector Type: Front panel MMCX connectors
Input Type: Single−ended, non−inverting
Full Scale Input: +4 dBm
Coupling: AC
Input Impedance: 50Ω
Analog Input RF Transformers:
Quantity: Two (one per input channel)
Type: Mini−Circuits ADT4−5WT
3dB Passband: 300 kHz to 270 MHz
Input Return Loss: 8.72 dB min., 31.13 dB max.

Analog/Digital Converters

Quantity: Two devices
Device:
Standard: Analog Devices AD6645−80
Option 100: Analog Devices AD6645−105
(see Section 1.16 for data sheet)
Sampling Rate:
Standard: 30 MHz to 80 MHz
Option 100: 30 MHz to 105 MHz
Resolution: 14 bits
Sample Clock Source: Clock from Sync bus A or B, each bus clock source can be from onboard crystal oscillator, front panel external clock, or LVDS clock, selectable via software

AD6645 Notes:

Input Range:

The AD6645 has a 2.2 volt fullscale input with a +/−10% gain error. That means its fullscale input can range from 1.98 V to 2.42 Vp−p.
The AD6645 input impedance is nominally 1K ohm. A 250 Ohm resistor is installed in parallel, which makes its input impedance 200 Ohms.
A 4:1 transformer produces a 4 to 1 impedance change and 2 to 1 voltage change. This makes the input impedance 50 Ohms and the input fullscale voltage range from 0.99 to 1.21 Vp−p.
By definition 0 dBm is 1 mW RMS into 50 Ohms, so:
P = V*2/R or V = sqr(PR) = 1e−3(50) = 0.223 Vrms.
Vpeak = 1.414Vrms = 0.223(1.414) = 0.316 Vpeak
Vp−p = 2 Vpeak = 0.316(2) = 0.632 Vp−p.
Thus, 0 dBm = 0.632 Vp−p into 50 Ohms.
Thus the fullscale ranges from: 20*log(0.99/0.632) = 3.898 dBm
to: 20*log(1.21/0.632) = 5.64 dBm

Offset: An offset in the data is typical for the AD6645 A/D converter.
The AD6645 has a typical voltage offset accuracy of 1.2 mV, max +/− 10mV.
Since its fullscale voltage is 2.2 Vp−p, this represents 1.2e−3/2.2 = 0.000545 V.
The offset can appear to be nominally about 30 counts out of 65536 (which is what the driver returns in bypass mode because the 14−bit ADC data is left justified in a 16 bit field). This represents 30/65536 = 0.000457 V offset.

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1.17 Specifications (continued)

Digital Receivers

Quantity:	One quad receiver chip (four receiver channels)
Device:	Texas Instruments Graychip GC4016 (see Section 1.16)
Decimation:	32 to 16,384 — Decimation by 8 or 16 can also be achieved by combining channels in packed data modes
Data Source:	FPGA, A/D, PCI Interface
Clock Source:	Clock from Sync bus A or B, each bus clock source can be from onboard crystal oscillator, front panel external clock, or LVDS clock, selectable via software
Sync:	Maskable inside each GC4016 chip
Output:	Parallel data (GC4016 must be set for parallel output mode, frame sync mode = 2)
Bypass Mode:	Data from the A/D converters can be written directly into the FPGA at a sample rate equal to the A/D clock decimated by any integer between 1 and 4096

Analog Signal Outputs

Quantity:	Two signal outputs, one per D/A upconverter
Connector Type:	Front panel MMCX connectors
Output Type:	Single−ended, non−inverting
Coupling:	AC
Output Impedance:	50Ω
Standard Output Transformers:	
Type:	Mini−Circuits ADT4−5WT
3dB Passband:	300 kHz to 500 MHz
Output Power:	+4 dBm into 50 ohms
Option 002 Output Transformers:	
Transformer:	Mini−Circuits ADT1−1WT
3 dB Passband:	400 kHz to 800 MHz
Output Power:	−2 dBm into 50 ohms

Digital/Analog Upconverter

Quantity:	One, with two D/A channels
Device:	Texas Instruments DAC5686
Sampling Rate:	320 MSPS in upconvert mode, 500 MSPS in D/A only mode
DAC Resolution:	16 bits
Input Data Rate:	160M 32−bit words per second
Coupling:	Transformer coupled
Output IF:	DC to 160 MHz *
Output Signal:	Analog, real or quadrature
Interpolation filters:	2x, 4x, 8x, 16x
Clock Source:	Clock from Sync bus A or B, each bus clock source can be from onboard crystal oscillator, front panel external clock, or LVDS clock, selectable via software

* Since maximum data bandwidth is 160 MHz, synthesizing IF signals at this limit is not practical

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1.17 Specifications (continued)

External Clock Inputs

Quantity:	Two signal inputs, one per clock channel
Connector Type:	Front panel MMCX connectors
Signal Type:	Sine wave, 45–55% duty cycle
Frequency Range:	1 to 300 MHz *
Voltage Range:	0 to +10 dBm
Coupling:	AC coupled
Input Impedance:	50Ω

* Limited by ADC or DAC characteristics

Sync/Gate Bus Inputs/Outputs

Connector Type:	Front panel 26–pin connector
Signals:	Clock In/Out: 4 pins (two LVDS pairs, Clk A & Clk B) Sync In/Out: 4 pins (two LVDS pairs, Sync A & Sync B) Gates In/Out: 4 pins (two LVDS pairs, Gate A & Gate B) TTL Sync In: 1 pin (single–ended) TTL Gate/Trigger In: 1 pin (single–ended)

Clocks

Quantity:	Two
Clock Sources:	Separately selectable from external clocks or onboard crystal oscillator
External Clocks:	Front panel LVDS Sync Bus (two Clock inputs) or front panel MMCX connector inputs
Internal Clocks	
Standard:	80 MHz crystal oscillator, 100 ppm
Option 100:	100 MHz crystal oscillator, 100 ppm

Gates

Quantity:	Two
Gate Sources:	Separately selectable from external or internal gates
External Gates:	Front panel LVDS Sync Bus (two Gate inputs) or TTL Gate/Trigger input
Internal Gates:	Generated from programmable registers (one for each gate)
Gate Polarity:	Programmable polarity for external gates
Gate Disable:	Each gate can be disabled; when gate is disabled, writes default to enabled
Triggering:	Each gate can be programmed as a trigger, programmable trigger length up to 16,383 FIFO writes

Syncs

Quantity:	Two
Sync Source:	Separately selectable from external or internal syncs
External Sync:	Front panel LVDS Sync Bus (two Sync inputs) or TTL Sync input
Internal Sync:	Generated from programmable register
Sync Pulse Width:	2 clock cycles, minimum

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1.17 Specifications (continued)

Field–Programmable Gate Array

Device: Xilinx® Virtex–II Pro™ XC2VP50
Configuration: Factory programmed by Pentek (see Section 1.14)
FPGA I/O (Option 104)**:** PMC P4 connector, with 64 I/O lines to FPGA

DDR SDRAM memory

Size: 512 MBytes, organized as two banks of 128 MBytes, and one bank of 256 MBytes

FLASH memory

Size: One bank of 16 MBytes

PCI Interface

Device: Pentek PCI7140
Compliance: Standard PCI 2.2 Interface
Support for 3.3V signal logic only
PCI Bus: 64 bit, 66 MHz (can support 32 bit and/or 33 MHz)
Local Bus: 64 bit, 66 MHz
Data Transfer Modes: Direct Slave Mode and DMA Master/Slave Mode, 9–channel demand–mode and chaining controller
Control: Any PCI bus master (such as a PMC baseboard processor) can control both sync buses, the AD6645s, GC4016, DAC5686, the FPGA, and all onboard registers.

XMC Interface (Option 5xx)

Compliance: VITA 42.0–2005 XMC draft standard
XMC Connector: 114–pin (Samtec ASP–105885–01 or equivalent)
Protocol: ANSI/VITA 42.2–2006 XMC SerialRapidIO standard

Power

Current Draw:	**3.3V**	**5V**	**+12V**	**–12V**
Option 050,100:	1.07A	2.58A	0.2A	0.2A
(105 MHz A/D and standard FPGA functions)				
Option 050,100,430:	1.10A	3.37A	0.2A	0.2A
(105 MHz A/D and GateFlow Core installed – i.e., heavy FPGA usage) (±12V only connected to voltage test circuit)				

Total Power:
Option 050,100: 16.91 W
Option 050,100,430: 20.96 W
(Note: FPGA power consumption will vary based on usage)

Physical

Dimensions: Standard PMC module
Depth: 149.0 mm (5.87 in)
Height: 74 mm (2.91 in)
Weight: 127.6 grams (4.5 oz)

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1.17 **Specifications** (continued)

Environmental

Commercial Applications – Level L0

Cooling Method (operational):	Forced Air
Operating Temperature:	0° to 50°C
Storage Temperature:	–20° to 90°C
Relative Humidity:	0 to 95% non–condensing

Pentek Ruggedization Level L1

Option Number:	–701
Cooling Method (operational):	Forced Air
Operating Temperature:	0° to 50° C
Storage Temperature:	–40° C to +100° C
Sine Vibration:	2g, 20–500 Hz
Random Vibration:	$0.01g^2$/Hz, 20–2000 Hz
Shock:	10g, 11ms
Relative Humidity:	
No conformal coating:	0% to 95% non–condensing
Conformal coating (Option 720):	0% to 100% non–condensing

Pentek Ruggedization Level L2

Option Number:	–702
Cooling Method (operational):	Forced Air
Operating Temperature:	–20° to 65° C
Storage Temperature:	–40° C to +100° C
Sine Vibration:	2g, 20–500 Hz
Random Vibration:	$0.04g^2$/Hz, 20–2000 Hz
Shock:	20g, 11ms
Relative Humidity:	
No conformal coating:	0% to 95% non–condensing
Conformal coating (Option 720):	0% to 100% non–condensing

Pentek Ruggedization Level L3

Call Pentek

Pentek Ruggedization Level L4

Call Pentek

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Chapter 2: Installation and Connections

2.1 Inspection

After unpacking, inspect the unit carefully for possible damage to connectors or components. If any damage is discovered, contact Pentek immediately at (201) 818–5900. Please save the shipping container and packing material in case reshipment is required.

An assembly drawing of the component side of the Model 7140 PCB is provided below, showing all connectors on the board.

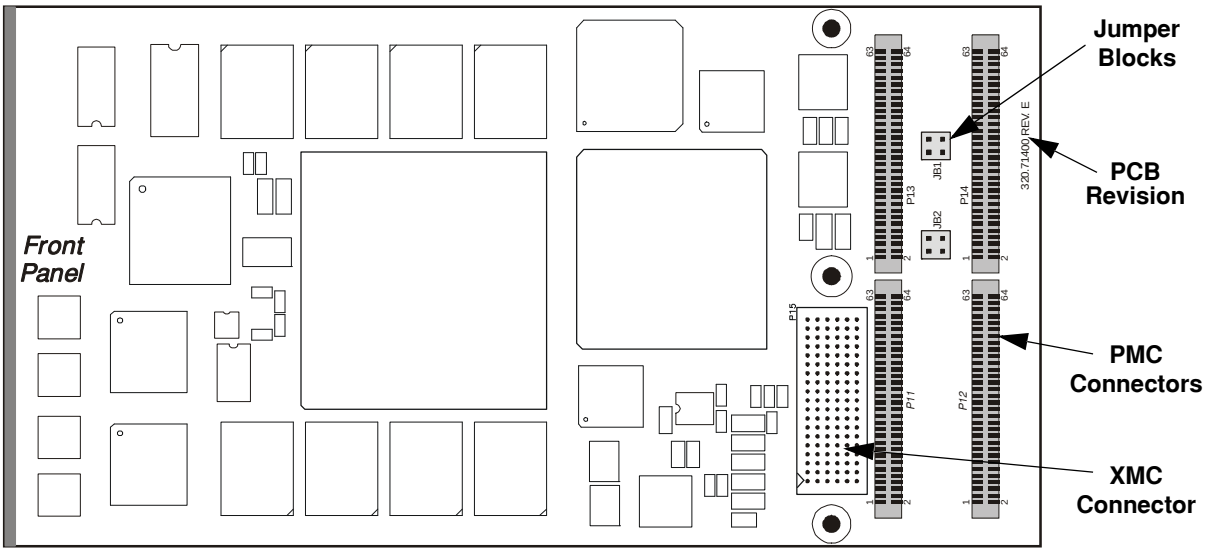


Figure 2–1: Model 7140 PCB Assembly Drawing, Component Side

2.2 Jumper Block Settings

Jumper blocks **JB1** and **JB2,** located on the solder side of the PCB (see Figure 2–1), are for factory use only and should not be changed by the user.

NOTE: Jumper block **JB2** is present only on 7140 PCBs identified as **Rev B** or greater.



DO NOT change the Factory Default jumper settings!

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2.3 Baseboard Connectors

The following subsections identify the baseboard PMC/XMC connectors on the Model 7140 PCB. Refer to Figure 2–1 for the location of these connectors on the PCB.

2.3.1 PMC Connectors

The Model 7140 PMC is connected to a PMC baseboard using four 64–pin connectors, designated **P11**, **P12**, **P13**, and **P14** (see Figure 2–1). These connectors are defined by the PMC standard, as follows:

- **P11** and **P12** (PMC Pn1 and Pn2 respectively) contain the 32–bit PCI bus interface plus associated power, ground, reserved pins, and other necessary signals.
- **P13** (PMC Pn3) supports expansion to the 64–bit PCI bus interface.
- **P14** (PMC Pn4) supports user–defined I/O (see Section 2.3.2 below). Standard PMC–VME baseboards route the 64 signals from the **P14** connector directly to the VMEbus backplane **P2** connector.

2.3.2 PMC FPGA I/O Connections (Option 104)

Option 104 for the Model 7140 provides connections from spare pins on the XC2VP50 FPGA to the VMEbus using PMC connector **P14**. These connections are programmed for low–voltage differential signals (LVDS) in the default FPGA configuration—the user can reconfigure these pins with custom FPGA programming (see Section 1.14, FPGA Configuration).

With Option 104, 32 pairs of LVDS connections are routed from the XC2VP50 FPGA to PMC connector **P14**. These are available to the user for custom I/O. Table 2–1, on the following page, identifies the LVDS signals that are connected from the FPGA to the PMC **P14** connector pins, and thus to the VMEbus **P2** connector pins on standard PMC–VME baseboards.

Use the FPGA Data In/Out Registers, Section 6.3, to read and write data using this connector.

- The LVDS_OUT signals in Table 2–1 are outputs from the FPGA Data Out Register, with LVDS_OUT_x0 from bit D0 and LVDS_OUT_x15 from bit D15.
- The LVDS_IN signals in Table 2–1 are inputs to the FPGA Data In Register, with LVDS_IN_x0 from bit D0 and LVDS_IN_x15 from bit D15.

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2.3 Baseboard Connectors (continued)

2.3.2 PMC FPGA I/O Connections (continued)

Table 2–1: Option 104 PMC FPGA I/O Pin Connections

FPGA Signal	PMC P14 Pin	VME P2 Pin	FPGA Signal	PMC P14 Pin	VME P2 Pin
LVDS_OUT_N0	1	USER–C1	LVDS_OUT_N8	33	USER–C17
LVDS_IN_N0	2	USER–A1	LVDS_IN_N8	34	USER–A17
LVDS_ OUT _P0	3	USER–C2	LVDS_ OUT _P8	35	USER–C18
LVDS_IN_P0	4	USER–A2	LVDS_IN_P8	36	USER–A18
LVDS_ OUT _N1	5	USER–C3	LVDS_ OUT _N9	37	USER–C19
LVDS_IN_N1	6	USER–A3	LVDS_IN_N9	38	USER–A19
LVDS_ OUT _P1	7	USER–C4	LVDS_ OUT _P9	39	USER–C20
LVDS_IN_P1	8	USER–A4	LVDS_IN_P9	40	USER–A20
LVDS_ OUT _N2	9	USER–C5	LVDS_ OUT _N10	41	USER–C21
LVDS_IN_N2	10	USER–A5	LVDS_IN_N10	42	USER–A21
LVDS_ OUT _P2	11	USER–C6	LVDS_ OUT _P10	43	USER–C22
LVDS_IN_P2	12	USER–A6	LVDS_IN_P10	44	USER–A22
LVDS_ OUT _N3	13	USER–C7	LVDS_ OUT _N11	45	USER–C23
LVDS_IN_N3	14	USER–A7	LVDS_IN_N11	46	USER–A23
LVDS_ OUT _P3	15	USER–C8	LVDS_ OUT _P11	47	USER–C24
LVDS_IN_P3	16	USER–A8	LVDS_IN_P11	48	USER–A24
LVDS_ OUT _N4	17	USER–C9	LVDS_ OUT _N12	49	USER–C25
LVDS_IN_N4	18	USER–A9	LVDS_IN_N12	50	USER–A25
LVDS_ OUT _P4	19	USER–C10	LVDS_ OUT _P12	51	USER–C26
LVDS_IN_P4	20	USER–A10	LVDS_IN_P12	52	USER–A26
LVDS_ OUT _N5	21	USER–C11	LVDS_ OUT _N13	53	USER–C27
LVDS_IN_N5	22	USER–A11	LVDS_IN_N13	54	USER–A27
LVDS_ OUT _P5	23	USER–C12	LVDS_ OUT _P13	55	USER–C28
LVDS_IN_P5	24	USER–A12	LVDS_IN_P13	56	USER–A28
LVDS_ OUT _N6	25	USER–C13	LVDS_ OUT _N14	57	USER–C29
LVDS_IN_N6	26	USER–A13	LVDS_IN_N14	58	USER–A29
LVDS_ OUT _P6	27	USER–C14	LVDS_ OUT _P14	59	USER–C30
LVDS_IN_P6	28	USER–A14	LVDS_IN_P14	60	USER–A30
LVDS_ OUT _N7	29	USER–C15	LVDS_ OUT _N15	61	USER–C31
LVDS_IN_N7	30	USER–A15	LVDS_IN_N15	62	USER–A31
LVDS_ OUT _P7	31	USER–C16	LVDS_ OUT _P15	63	USER–C32
LVDS_IN_P7	32	USER–A16	LVDS_IN_P15	64	USER–A32

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2.3 Baseboard Connectors (continued)

2.3.3 XMC Connector (Option 5xx)

Option 5xx for the Model 7140 provides an XMC connector that follows the VITA 42.0–2005 XMC Switched Mezzanine Card Auxiliary Standard (draft). See Figure 2–1 for location of this connector, **P15**, on the PCB.

2.3.3.1 Communication Protocol

The 7140 XMC interface uses the ANSI/VITA 42.2–2006 standard for Serial RapidIO as the communication protocol, which provides two 4x data streaming interfaces to the XMC carrier board.

2.3.3.2 Connector Pin–out

The 114–pin XMC connector is Samtec ASP–105885–01 or equivalent. The following table shows the connector pin definitions.

Table 2–2: XMC P15 (Primary) Connector Pin–out

Pin	A	B	C	D	E	F
01	DP00+ (S0_TD0+)	DP00- (S0_TD0-)	3.3V	DP01+ (S0_TD1+)	DP01- (S0_TD1-)	VPWR
02	GND	GND	TRST#	GND	GND	MRSTI#
03	DP02+ (S0_TD2+)	DP02- (S0_TD2-)	3.3V	DP03+ (S0_TD3+)	DP03- (S0_TD3-)	VPWR
04	GND	GND	TCK	GND	GND	MRSTO#
05	DP04+ (S1_TD0+)	DP04- (S1_TD0-)	3.3V	DP05+ (S1_TD1+)	DP05- (S1_TD1-)	VPWR
06	GND	GND	TMS	GND	GND	+12V
07	DP06+ (S1_TD2+)	DP06- (S1_TD2-)	3.3V	DP07+ (S1_TD3+)	DP07- (S1_TD3-)	VPWR
08	GND	GND	TDI	GND	GND	-12V
09	DP08+ (RFU)	DP08- (RFU)	RPS (UD)	DP09+ (RFU)	DP09- (RFU)	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	DP10+ (S0_RD0+)	DP10- (S0_RD0-)	MBIST#	DP11+ (S0_RD1+)	DP11- (S0_RD1-)	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	DP12+ (S0_RD2+)	DP12- (S0_RD2-)	3.3V AUX	DP13+ (S0_RD3+)	DP13- (S0_RD3-)	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	DP14+ (S1_RD0+)	DP14- (S1_RD0-)	RPS (UD)	DP15+ (S1_RD1+)	DP15- (S1_RD1-)	VPWR
16	GND	GND	MVMRO	GND	GND	MSCL
17	DP16+ (S1_RD2+)	DP16- (S1_RD2-)	RFU	DP17+ (S1_RD3+)	DP17- (S1_RD3-)	RFU
18	GND	GND	RPS (UD)	GND	GND	RPS (UD)
19	DP18+ (RFU)	DP18- (RFU)	RPS (UD)	DP19+ (RFU)	DP19- (RFU)	RPS (UD)

Signal names of Serial RapidIO implementation per VITA 42.2–2006 shown in parentheses.
See Section 2.3.3.3, next page, for definition of these Serial RapidIO signals.

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2.3 Baseboard Connectors (continued)

2.3.3 XMC Connector (continued)

2.3.3.3 Serial RapidIO Signals

The following XMC connector signals are defined by the XMC Serial RapidIO Protocol Layer Standard, ANSI/VITA 42.2–2006.

- S0_RD[0..3] – Link 0 Differential Receive

  These signals are used by the XMC to receive high–speed protocol–specific data from the carrier over Link 0. These signals shall tolerate EIA–644 signal levels. If the XMC implements a 1X link over Link 0, signal S0_RD[0] shall be used.

- S0_TD[0..3] – Link 0 Differential Transmit

  These signals are used by the XMC to transmit high–speed protocol–specific data from the carrier over Link 0. These signals shall tolerate EIA–644 signal levels. If the XMC implements a 1X link over Link 0, signal S0_TD[0] shall be used.

- S1_RD[0..3] – Link 1 Differential Receive

  These signals are used by the XMC to receive high–speed protocol–specific data from the carrier over Link 1. These signals shall tolerate EIA–644 signal levels. If the XMC implements a 1X link over Link 1, signal S1_RD[0] shall be used.

- S1_TD[0..3] – Link 1 Differential Transmit

  These signals are used by the XMC to transmit high–speed protocol–specific data from the carrier over Link 1. These signals shall tolerate EIA–644 signal levels. If the XMC implements a 1X link over Link 1, signal S1_TD[0] shall be used.

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2.4 Installing the Model 7140 on a PMC Baseboard

The Model 7140 mounts on the component (top) side of a PMC/XMC baseboard or carrier. Refer to the operating manual supplied with your PMC baseboard for any specific instructions. A typical PMC/XMC baseboard is illustrated in Figure 2–2 below.

CAUTION

REMOVE POWER to the PMC/XMC baseboard before installation!

DO NOT plug the Model 7140 into a baseboard or carrier that uses any PMC signal voltage level other than 3.3 volts. (Note that the PMC key in Figure 2–2 below is in the 3.3V position.)

Note

The Model 7140 requires both a 3.3V and a 5V power supply.

Ensure that the PMC/XMC baseboard or carrier you are using has both a 3.3V and a 5V power supply.

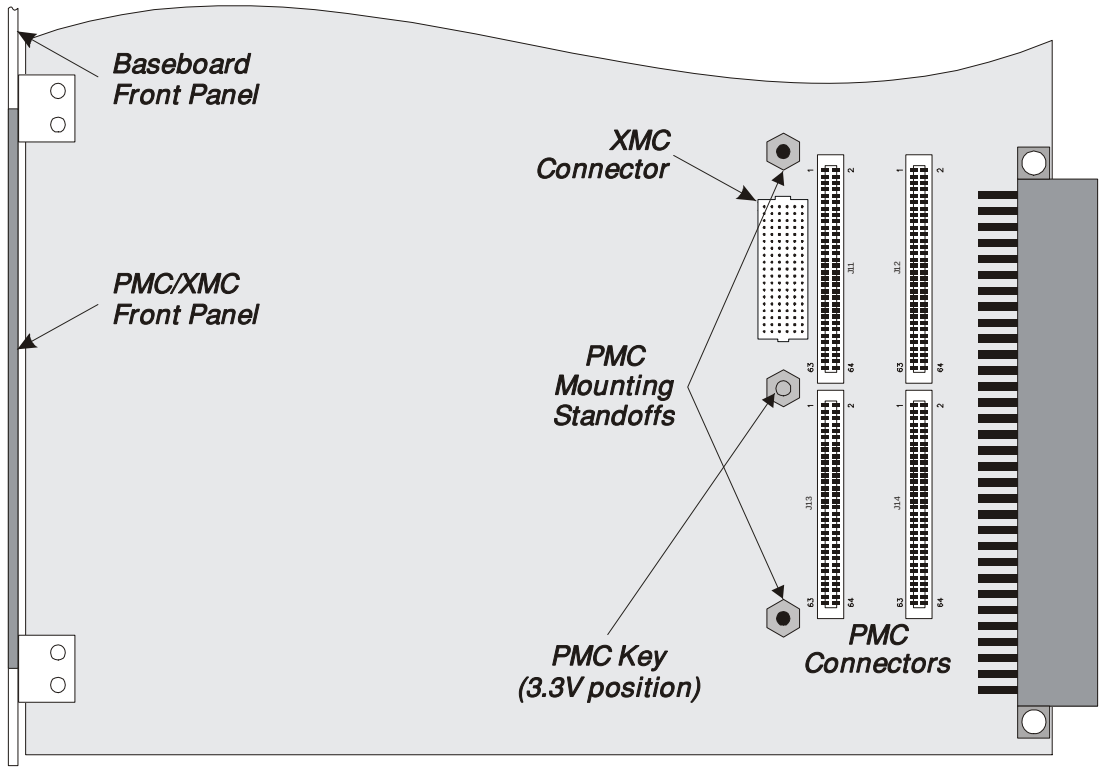


Figure 2–2: Typical PMC/XMC Baseboard – Connectors & Mounting Hardware

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2.4 Installing the Model 7140 on a PMC Baseboard (continued)

CAUTION

Attach an ESD strap to your wrist—attach the other end to a ground source. The ESD strap must be secured both to your wrist and to ground throughout the procedure.

Pentek PMC baseboards are supplied with PMC standoffs, PMC voltage key, and mounting screws. Ensure that the standoffs and key are installed on the baseboard at the locations shown in Figure 2–3 below.

1) Remove the blank PMC front panel from the front panel of the PMC baseboard (see Figure 2–2 on the prior page).

2) Position the Model 7140 front panel into the opening from behind the PMC baseboard front panel, and position the module so that the PMC card's key hole is over the PMC key on the baseboard (see illustration below).

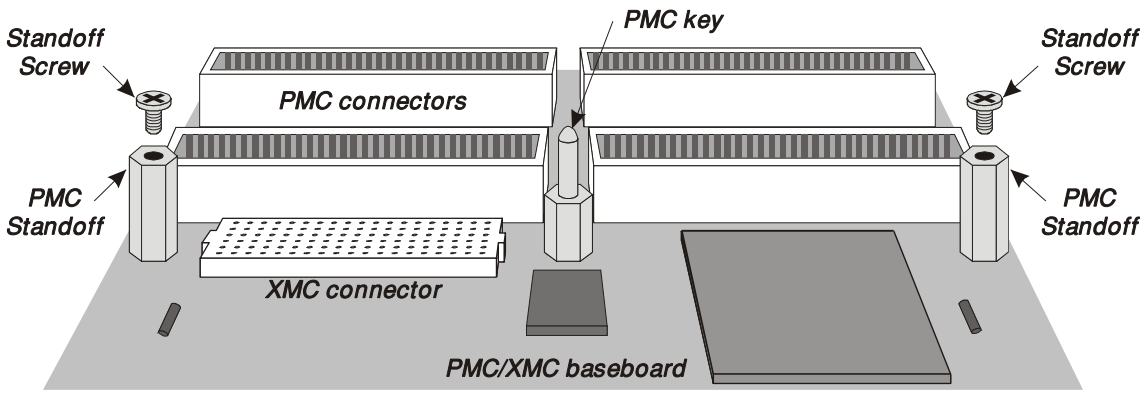


Figure 2–3: PMC Baseboard PMC Connections

3) **GENTLY but firmly**, press down on the areas of the PMC card opposite the connectors to fully seat the module's connectors into the baseboard. The connectors on the underside of the PMC card should connect smoothly with the corresponding PMC connectors on the baseboard.

4) Using two flat–head Phillips screws (supplied with the 7140), secure the Model 7140 PCB to the baseboard standoffs, through the PCB's standoff holes.

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2.5 Installing the Pentek JTAG PC Assembly

If you need to use JTAG connections to the Model 7140 (e.g., to download code to the configuration EEPROMs or to the PowerPC core), a special JTAG connector PC assembly, Pentek part # 004.71402, must be mounted onto the 7140 board. This unit may be mounted onto the 7140 after the 7140 has been mounted onto a PMC baseboard.

An assembly drawing of the Model 7140 is provided below, mounted onto a PMC baseboard, showing the JTAG PC assembly mounting orientation.

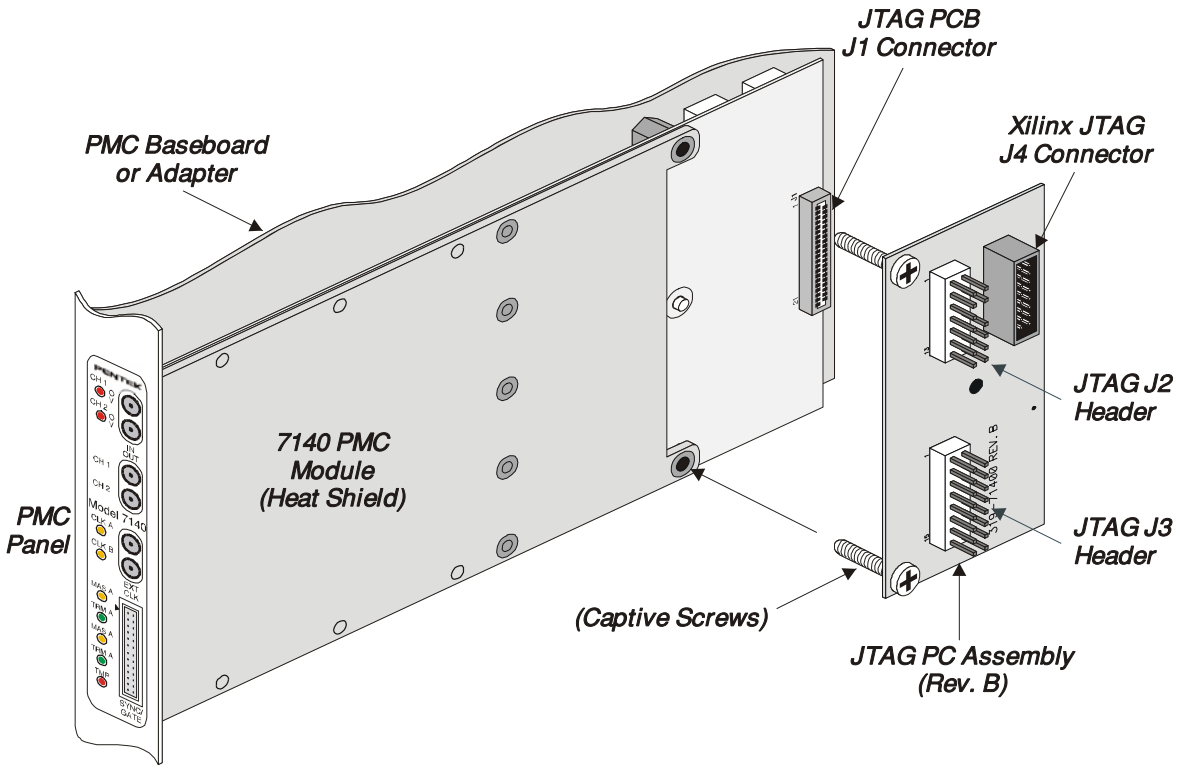


Figure 2–4: Model 7140 – JTAG PC Assembly Mounting

To mount the JTAG PC assembly onto the 7140:

1) First remove the two flat–head mounting screws that secure the Model 7140 PCB to the baseboard standoffs (those used in the last step in Section 2.4).

2) Plug the JTAG PC assembly into the connector **J1** on the 7140 (see figure above), and secure to the 7140 and baseboard using the two captive screws on the JTAG board.

The JTAG **J2**, **J3**, and **J4** connectors are described on the following pages.

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2.5 Installing the Pentek JTAG PC Assembly (continued)

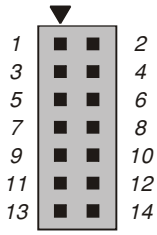
The following subsections describe the JTAG connectors on the 004.71402 PC assembly. Refer to Figure 2.5 for the location of these connectors on the JTAG PC assembly.

2.5.1 JTAG J2 Connector

The JTAG **J2** In–Circuit Program Chain (ISP) connector provides a connection to download programs and to perform boundary scan tests on 7140 PCB devices. This connector is reserved for Pentek factory use only. The pinout for this 14–pin header is given in the following table.

Table 2–3: JTAG J2 Connector

Signal	Pin Number		Pin Number	Signal
TMS	1		2	No Connection
TDI	3		4	GND
+3.3 V	5		6	Key
TDO	7		8	GND
TCK_RET	9		10	No Connection
TCK	11		12	GND
No Connection	13		14	No Connection

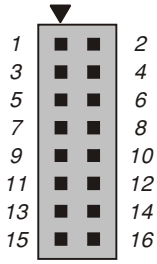


2.5.2 JTAG J3 Connector

The JTAG **J3** connector provides a connection to download programs and to control the execution of those programs on the PowerPC core in the FPGA. This connector is reserved for Pentek factory use only. The pinout for this 16–pin header is given in the following table.

Table 2–4: JTAG J3 Connector

Signal	Pin Number		Pin Number	Signal
PPC_TDO	1		2	No Connection
PPC_TDI	3		4	PPC_TRST_N
No Connection	5		6	+ 3.3 V
PPC_TCK	7		8	No Connection
PPC_TMS	9		10	No Connection
PPC_HALT_N	11		12	No Connection
No Connection	13		14	No Connection
No Connection	15		16	GND



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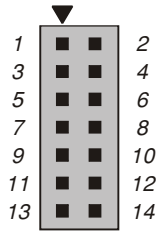
2.5 Installing the Pentek JTAG PC Assembly (continued)

2.5.3 Xilinx JTAG J4 Connector

The Xilinx JTAG **J4** connector provides a connection to a Xilinx standard JTAG cable interface to download programs and perform boundary scan tests on 7140 PCB devices. This connector is reserved for Pentek factory use only. The pinout for this 14–pin connector is given in the following table.

Table 2–5: Xilinx JTAG J4 Connector

Signal	Pin Number		Pin Number	Signal
GND	1		2	+3.3 V
GND	3		4	TMS
GND	5		6	TCK
GND	7		8	TDO
GND	9		10	TDI
GND	11		12	No Connection
GND	13		14	No Connection



NOTE: The Xilinx JTAG J4 connector is provided only on Revision B of the Pentek 004.71402 JTAG PC assembly. For Revision A JTAG PC assembly, use the JTAG **J2** connector, Section 2.5.1, to download programs and perform boundary scan tests.

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2.6 Front Panel Connections

The Model 7140 PMC front panel is illustrated in the figure at the right. The front panel includes six MMCX microminiature coaxial connectors for input/output of analog and clock signals, and a 26–pin Sync Bus connector. These connectors are described in the following subsections.

The front panel also includes nine LED indicators, described in Section 2.7, on page 43.

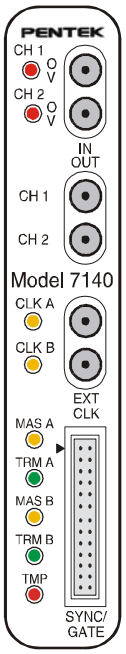


Figure 2–5: Model 7140 Front Panel

2.6.1 Analog Input Connectors CH1 IN, CH2 IN

The front panel has two MMCX coaxial receptacles for analog signal inputs, one for each A/D input channel, labeled **CH 1** and **CH 2 IN**.

The analog input signal must be +4 dBm full scale. Each input drives an RF transformer, with 50 Ω input impedance.

2.6.2 Analog Output Connectors CH1 OUT, CH2 OUT

The front panel has two MMCX coaxial receptacles for analog signal outputs, labeled **CH 1** and **CH 2 OUT**, one for each D/A output channel.

The analog output signal of each channel is within the range of +4 dBm (–2 dBm with Option 002). Each output is driven by an RF transformer with 50 Ω output impedance.

2.6.3 Clock Input Connectors EXT CLK A, B

The front panel has two MMCX coaxial receptacles, labeled **EXT CLK A** and **CLK B**, for input of external sample clocks.

The external clock signals must be a sine wave of 0 to 10 dBm, with a frequency from 30 to 105 MHz for ADC use, or from 1 to 300 MHz for DAC use.

The clocks can be used as the reference signal to derive the sample clock signal for the A/D converters and digital receivers. This input is enabled using the Master Control Register SEL CLK bit (see Section 6.10.1.9 or 6.10.4.9).

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2.6 Front Panel Connections (continued)

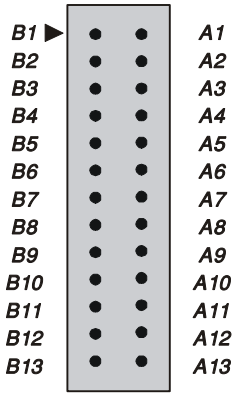
2.6.4 SYNC/GATE Connector SYNC/GATE

The 26–pin **SYNC/GATE** front panel connector provides two independent sets of clock, sync, and gate input/output pins for the low–voltage differential signal (LVDS) timing buses. When the Model 7140 is a bus Master, these pins output the buses to other slave units. When the 7140 is a bus Slave, these pins input all LVDS bus signals from a bus Master. This connector also provides two TTL Gate/Sync inputs. The mating 26–pin connector is Pentek part # 353.02607 (ERNI # 214346).

The following table shows the connector pin configuration.

Table 2–6: SYNC/GATE Connector Pins

Signal	Pin		Pin	Signal
TTL GATE	B1		A1	GND
TTL SYNC	B2		A2	GND
GATE A–	B3		A3	GATE A+
GND	B4		A4	GND
SYNC A–	B5		A5	SYNC A+
GND	B6		A6	GND
CLK A–	B7		A7	CLK A+
GND	B8		A8	GND
GATE B–	B9		A9	GATE B+
GND	B10		A10	GND
SYNC B–	B11		A11	SYNC B+
GND	B12		A12	GND
CLK B–	B13		A13	CLK B+



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2.7 Front Panel LEDs

The Model 7140 front panel has nine LED indicators, illustrated in Figure 2–5.

2.7.1 Overload LEDs **CH1 OV, CH2 OV**

There are two red overload LEDs, one for each A/D input, labeled **CH1 OV** and **CH2 OV**. Each LED is an indicator for an A/D overload detection function in each AD6645 A/D converter. When an overload indication is set by the AD6645, the associated OVLD LED illuminates. In addition, an OVLD interrupt may be generated from each A/D overload indication to a PMC baseboard processor (see Table 6–23, page 140).

2.7.2 Clock LEDs **CLK A, CLK B**

There are two green **CLK** LEDs, one for each Sync Bus (**A** or **B**). The green **CLK** LED illuminates when a valid sample clock signal is detected on the Sync Bus. If this LED is not illuminated, then no clock has been detected and no data from the input stream can be processed.

2.7.3 Master LEDs **MAS A, MAS B**

There are two yellow **MAS** LEDs, one for each Sync Bus (**A** or **B**). The **MAS** LED illuminates when this Model 7140 is the bus Master (MASTR bit D00 = 1, Master Bus A/B Control Register, Section 6.10.1.11 or 6.10.4.11). The bus Master generates all sync/gate/clock signals on the LVDS bus. When only a single 7140 is used, it must be a Master.

2.7.4 Terminate LEDs **TRM A, TRM B**

There are two yellow **TRM** LEDs, one for each Sync Bus (**A** or **B**). The yellow **TRM** LED illuminates when this Model 7140 bus is terminated (TERM bit D01 = 1, Master Bus A/B Control Register, Section 6.10.1.11 or 6.10.4.11). When this 7140 is the last Slave unit or only unit on the Sync Bus, you must enable bus termination.

2.7.5 Over Temperature LED **TMP**

There are several temperature/voltage sensors on the Model 7140 PCB. The sensor thresholds are set by a PMC baseboard processor (see TWSI Port Register, Section 6.4). When an over–temperature or over–voltage condition is indicated, the red **TMP** LED illuminates on the front panel. In addition, an over–temperature/voltage interrupt is available to any processor on the PMC baseboard (see Table 6–23, page 140).

NOTE: You must set up the temperature/voltage sensors' serial port following power on of the PMC baseboard (see TWSI Port Register, Section 6.4).

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Chapter 3: Model 7140 Memory Maps

3.1 Overview

This chapter describes access to the Model 7140 resources and control registers from a PMC baseboard processor. Memory maps to these resources are given from the base–board processor's viewpoint.

3.2 Model 7140 Address Mapping

The Model 7140 is controlled from the PMC baseboard through a PCI Bus interface, the Pentek PCI7140 chip. All 7140 resources are configured to be available in PCI Address Space. Table 3–1, below, provides a memory map for these resources, relative to PCI Base Address Registers BAR0, BAR1, and BAR2 in the PCI7140. (See Appendix A for a summary of the PCI Configuration Space Registers for the Model 7140.)

Table 3–1: Model 7140 PCI Memory Map

PCI Bus Address *	Resource	Information
BAR0 + **0x0000 – 0xFFFF**	PCI7140 Registers	Section 3.3.1
BAR1 + **0x00000 – 0x7FFFF**	Reserved	–
BAR2 + **0x0000 – 0xFFFF**	FPGA Registers	Section 3.3.2

* Refer to the operating manual or instructions supplied with your PMC baseboard or carrier for the PCI Base Address settings.

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3.3 Memory Maps

3.3.1 PCI7140 Memory Map

The following is the memory map of the PCI7140 internal registers accessible from a PMC baseboard processor. All PCI7140 registers are 32 bits wide, however since the PCI local bus is a 64–bit data path, the register addresses are in increments of 64 bits (8 bytes). Refer to Chapter 5 for description of these registers.

NOTE: Access these registers using PCI Base Address Register 0 (**BAR0**).

Table 3–2: PCI7140 Registers Memory Map

Address Offset *	Register	Access	Information
Interrupt Control Registers			
0x0000	PCI Interrupt Flag	R/Clr	Section 5.2
0x0008	Reserved	–	–
0x0010	PCI Interrupt A Enable	R/W	Section 5.3
0x0018	PCI Interrupt B Enable	R/W	
0x0020	PCI Interrupt C Enable	R/W	
0x0028	PCI Interrupt D Enable	R/W	
0x0030 - 0x0068	Reserved	–	–
PCI7140 Control Registers			
0x0070	Board/Channel Reset	R/W	Section 5.4
0x0078	PCI7140 Revision	R.O.	Section 5.5
0x0080	Virtex Config Register	R/W	Section 5.6
0x0088	PCI DCM Control	R/W	Section 5.7
0x0090	Local DMA Request Status	R.O.	Section 5.8
0x0098	Reserved	–	–
0x00A0	PCI Bus Status	R.O.	Section 5.9
0x00A8	DMA PCI Interrupt Enable/Flag	R/Clr	Section 5.10
0x00B0	Local DMA In Base Address Remap	R/W	Section 5.11
0x00B8	Local DMA Out Base Address Remap	R/W	Section 5.12

* Offset from PCI Base Address Register 0 (**BAR0**), see Table 3–1

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3.3 Memory Maps (continued)

3.3.1 PCI7140 Memory Map (continued)

NOTE: Access these registers using PCI Base Address Register 0 (**BAR0**).

Table 3–2: PCI7140 Registers Memory Map (continued)

Address Offset *	Register	Access	Information
DMA Control Registers			
0x0100	DMA Command	R/W	Section 5.13
0x0108	Reserved	–	–
0x0110	DMA0 Current Transfer Counter	R.O.	Section 5.14
0x0118	DMA0 Current PCI Address	R.O.	Section 5.15
0x0120	DMA1 Current Transfer Counter	R.O.	Section 5.14
0x0128	DMA1 Current PCI Address	R.O.	Section 5.15
0x0130	DMA2 Current Transfer Counter	R.O.	Section 5.14
0x0138	DMA2 Current PCI Address	R.O.	Section 5.15
0x0140	DMA3 Current Transfer Counter	R.O.	Section 5.14
0x0148	DMA3 Current PCI Address	R.O.	Section 5.15
0x0150	DMA4 Current Transfer Counter	R.O.	Section 5.14
0x0158	DMA4 Current PCI Address	R.O.	Section 5.15
0x0168	DMA5 Current Transfer Counter	R.O.	Section 5.14
0x0168	DMA5 Current PCI Address	R.O.	Section 5.15
0x0170	DMA6 Current Transfer Counter	R.O.	Section 5.14
0x0178	DMA6 Current PCI Address	R.O.	Section 5.15
0x0188	DMA7 Current Transfer Counter	R.O.	Section 5.14
0x0188	DMA7 Current PCI Address	R.O.	Section 5.15
0x0190	DMA8 Current Transfer Counter	R.O.	Section 5.14
0x0198	DMA8 Current PCI Address	R.O.	Section 5.15

* Offset from PCI Base Address Register 0 (**BAR0**), see Table 3–1

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3.3 Memory Maps (continued)

3.3.1 PCI7140 Memory Map (continued)

NOTE: Access these registers using PCI Base Address Register 0 (**BAR0**).

Table 3–2: PCI7140 Registers Memory Map (continued)

Address Offset *	Register	Access	Information
DMA Descriptor Registers			
0x1000	DMA0 Command/Status	R/W	Section 5.16
0x1008	DMA0 Transfer Interval Counter	R/W	Section 5.17
0x1010	DMA0 Descriptor 0 Transfer Count	R/W	Section 5.18
0x1018	DMA0 Descriptor 0 PCI Address	R/W	Section 5.19
0x1020	DMA0 Descriptor1 Transfer Count	R/W	Section 5.18
0x1028	DMA0 Descriptor 1 PCI Address	R/W	Section 5.19
0x1030	DMA0 Descriptor 2 Transfer Count	R/W	Section 5.18
0x1038	DMA0 Descriptor 2 PCI Address	R/W	Section 5.19
0x1040	DMA0 Descriptor 3 Transfer Count	R/W	Section 5.18
0x1048	DMA0 Descriptor 3 PCI Address	R/W	Section 5.19
0x1050 - 0x1FFF	Reserved	–	–
0x2000 - 0x2048	DMA1 (same as above ten DMA0 registers)	R/W	(see above)
0x2050 - 0x2FFF	Reserved	–	–
0x3000 - 0x3048	DMA2 (same as above ten DMA0 registers)	R/W	(see above)
0x3050 - 0x3FFF	Reserved	–	–
0x4000 - 0x4048	DMA3 (same as above ten DMA0 registers)	R/W	(see above)
0x4050 - 0x4FFF	Reserved	–	–
0x5000 - 0x5048	DMA4 (same as above ten DMA0 registers)	R/W	(see above)
0x5050 - 0x5FFF	Reserved	–	–
0x6000 - 0x6048	DMA5 (same as above ten DMA0 registers)	R/W	(see above)
0x6050 - 0x6FFF	Reserved	–	–
0x7000 - 0x7048	DMA6 (same as above ten DMA0 registers)	R/W	(see above)
0x7050 - 0x7FFF	Reserved	–	–
0x8000 - 0x8048	DMA7 (same as above ten DMA0 registers)	R/W	(see above)
0x8050 - 0x8FFF	Reserved	–	–
0x9000 - 0x9048	DMA8 (same as above ten DMA0 registers)	R/W	(see above)
0x9050 - 0xAFFF	Reserved	–	–

* Offset from PCI Base Address Register 0 (**BAR0**), see Table 3–1

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3.3 Memory Maps (continued)

3.3.2 FPGA Memory Map

The following is the memory map of the FPGA registers accessible from a PMC baseboard. All FPGA registers are 16 bits wide, however since the PCI local bus is a 64–bit data path, the register addresses are in increments of 64 bits (8 bytes). Refer to Chapter 6 for description of these registers.

NOTE: Access these registers using PCI Base Address Register 2 (**BAR2**).

Table 3–3: FPGA Registers Memory Map

Address Offset *	Register	Access	Information
0x0000 - 0x7fff	Flash Memory	R/W	Section 4.10
Global Registers			
0x8000	ID Readout	R/W	Section 6.2
0x8008	FPGA Data In	R.O.	Section 6.3
0x8010	FPGA Data Out	R/W	
0x8018	TWSI Port	R/W	Section 6.4
0x8020	DCM Control	R/W	Section 6.5
0x8028	Miscellaneous Control	R/W	Section 6.6
0x8030	FLASH Page	R/W	Section 6.7
0x8038	FPGA Revision 1	R.O.	Section 6.8
0x8040	FPGA Revision 2	R.O.	
0x8048	Core Option	R.O.	Section 6.9
0x8050 - 0x8078	Reserved	–	–
Clock/Sync/Gate Registers			
0x8080	Master Bus A Control	R/W	Section 6.10.1
0x8088	Sync A Generator	R/W	Section 6.10.2
0x8090	Gate A Generator	R/W	Section 6.10.3
0x8098	Master Bus B Control	R/W	Section 6.10.4
0x80a0	Sync B Generator	R/W	Section 6.10.5
0x80a8	Gate B Generator	R/W	Section 6.10.6
0x80b0	Sync Mask	R/W	Section 6.10.7
0x80b8 - 0x80f8	Reserved	–	–

* Offset from PCI Base Address Register 2 (**BAR2**), see Table 3–1

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3.3 Memory Maps (continued)

3.3.2 FPGA Memory Maps (continued)

NOTE: Access these registers using PCI Base Address Register 2 (**BAR2**).

Table 3–3: FPGA Registers Memory Map (continued)

Address Offset *	Register	Access	Information
Interrupt Registers			
0x8100	System Interrupt Enable	R/W	Section 6.11.1
0x8108	System Interrupt Flag	R/Clr	Section 6.11.2
0x8110	System Interrupt Status	R.O.	Section 6.11.3
0x8118	Application Interrupt Lint0 Enable	R/W	Section 6.11.4
0x8120	Application Interrupt Lint1 Enable	R/W	
0x8128	Application Interrupt Lint2 Enable	R/W	
0x8130	Application Interrupt Lint3 Enable	R/W	
0x8138	Application Interrupt Flag	R/Clr	Section 6.11.5
0x8140	Application Interrupt Status	R.O.	Section 6.11.6
FIFO Status Registers			
0x8148	DDC A FIFO Status	R.O.	Section 6.13.2
0x8150	DDC B FIFO Status	R.O.	
0x8158	DDC C FIFO Status	R.O.	
0x8160	DDC D FIFO Status	R.O.	
0x8168	ADC 1 FIFO Status	R.O.	Section 6.12.2
0x8170	ADC 2 FIFO Status	R.O.	
0x8178	DAC A FIFO Status	R.O.	Section 6.15.2
0x8180	DAC B FIFO Status	R.O.	
0x8188	Delay Memory Read FIFO Status	R.O.	Section 6.17.8
0x8190	Delay Memory Write FIFO Status	R.O.	
0x8198	Test FIFO Status	R.O.	Section 6.18.2
0x81a0 - 0x83f8	Reserved	–	–

* Offset from PCI Base Address Register 2 (**BAR2**), see Table 3–1

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3.3 Memory Maps (continued)

3.3.2 FPGA Memory Maps (continued)

NOTE: Access these registers using PCI Base Address Register 2 (**BAR2**).

Table 3–3: FPGA Registers Memory Map (continued)

Address Offset *	Register	Access	Information
D/A, UpConverter Registers			
0x8400	D/A Sync Bus Select	R/W	Section 6.10.8
0x8408	DAC Control / Status	R/W	Section 6.15.8
0x8410	DAC FIFO A Control	R/W	Section 6.15.1
0x8418	DAC A Trigger Length LSB	R/W	Section 6.15.5
0x8420	DAC A Trigger Length MSB	R/W	
0x8428	DAC FIFO A Interrupt Mask	R/W	Section 6.15.3
0x8430	DAC FIFO A Almost Empty Level	R/W	Section 6.15.6
0x8438	DAC FIFO A Almost Full Level	R/W	Section 6.15.7
0x8440	DAC FIFO B Control	R/W	Section 6.15.1
0x8448	DAC B Trigger Length LSB	R/W	Section 6.15.5
0x8450	DAC B Trigger Length MSB	R/W	
0x8458	DAC FIFO B Interrupt Mask	R/W	Section 6.15.3
0x8460	DAC FIFO B Almost Empty Level	R/W	Section 6.15.6
0x8468	DAC FIFO B Almost Full Level	R/W	Section 6.15.7
0x8470	DAC Read	R.O	Section 6.16
0x8478	DAC Write	W.O	
0x8480- 0x87f8	Reserved	–	–
Application Registers			
0x8800	Delay Memory Control	R/W	Section 6.17.1
0x8808	Delay Memory Bank 0 Depth LSB	R/W	Section 6.17.2
0x8810	Delay Memory Bank 0 Depth MSB	R/W	
0x8818	Delay Memory Bank 1 Depth LSB	R/W	
0x8820	Delay Memory Bank 1 Depth MSB	R/W	
0x8828	Delay Memory Bank 2 Depth LSB	R/W	
0x8830	Delay Memory Bank 2 Depth MSB	R/W	
0x8838	Delay Memory Bank 0 R/W Address LSB	R/W	Section 6.17.3
0x8840	Delay Memory Bank 0 R/W Address MSB	R/W	

* Offset from PCI Base Address Register 2 (**BAR2**), see Table 3–1

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3.3 Memory Maps (continued)

3.3.2 FPGA Memory Maps (continued)

NOTE: Access these registers using PCI Base Address Register 2 (**BAR2**).

Table 3–3: FPGA Registers Memory Map (continued)

Address Offset *	Register	Access	Information
Application Registers (continued)			
0x8848	Delay Memory Bank 1 R/W Address LSB	R/W	Section 6.17.3
0x8850	Delay Memory Bank 1 R/W Address MSB	R/W	
0x8858	Delay Memory Bank 2 R/W Address LSB	R/W	
0x8860	Delay Memory Bank 2 R/W Address MSB	R/W	
0x8868	Delay Memory Bank 0 Capture End Address LSB	R.O.	Section 6.17.4
0x8870	Delay Memory Bank 0 Capture End Address MSB	R.O.	
0x8878	Delay Memory Bank 1 Capture End Address LSB	R.O.	
0x8880	Delay Memory Bank 1 Capture End Address MSB	R.O.	
0x8888	ADC 1 Post Trigger Count LSB	R/W	Section 6.12.4
0x8890	ADC 1 Post Trigger Count MSB	R/W	
0x8898	ADC 2 Post Trigger Count LSB	R/W	
0x88a0	ADC 2 Post Trigger Count MSB	R/W	
0x88a8	DAC A Post Trigger Count LSB	R/W	Section 6.15.4
0x88b0	DAC A Post Trigger Count MSB	R/W	
0x88b8	DAC B Post Trigger Count LSB	R/W	
0x88c0	DAC B Post Trigger Count MSB	R/W	
0x88c8	DDC C Post Trigger Count LSB	R/W	Section 6.13.4
0x88d0	DDC C Post Trigger Count MSB	R/W	
0x88d8	DDC D Post Trigger Count LSB	R/W	
0x88e0	DDC D Post Trigger Count MSB	R/W	
0x88e8	ADC 1 Pre Trigger Count Capture LSB	R.O.	Section 6.12.5
0x88f0	ADC 1 Pre Trigger Count Capture MSB	R.O.	
0x88f8	ADC 2 Pre Trigger Count Capture LSB	R.O.	
0x8900	ADC 2 Pre Trigger Count Capture MSB	R.O.	
0x8908	Delay Memory Bank 2 Last Address LSB	R.O.	Section 6.17.5
0x8910	Delay Memory Bank 2 Last Address MSB	R.O.	
0x8918	Delay Memory Bank 0 Trigger Address LSB	R.O.	Section 6.17.6
0x8920	Delay Memory Bank 0 Trigger Address MSB	R.O.	
0x8928	Delay Memory Bank 1 Trigger Address LSB	R.O.	
0x8930	Delay Memory Bank 1 Trigger Address MSB	R.O.	
0x8938 - 0x8bf8	Reserved	–	–

* Offset from PCI Base Address Register 2 (**BAR2**), see Table 3–1

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3.3 Memory Maps (continued)

3.3.2 FPGA Memory Maps (continued)

NOTE: Access these registers using PCI Base Address Register 2 (**BAR2**).

Table 3–3: FPGA Registers Memory Map (continued)

Address Offset *	Register	Access	Information
A/D, DownConverter Registers			
0x8c00	A/D Sync Bus Select	R/W	Section 6.10.9
0x8c08	DDC FIFO A Control	R/W	Section 6.13.1
0x8c10	DDC A Trigger Length LSB	R/W	Section 6.13.5
0x8c18	DDC A Trigger Length MSB	R/W	
0x8c20	DDC FIFO A Interrupt Mask	R/W	Section 6.13.3
0x8c28	DDC FIFO A Almost Empty Level	R/W	Section 6.13.6
0x8c30	DDC FIFO A Almost Full Level	R/W	Section 6.13.7
0x8c38	DDC FIFO B Control	R/W	Section 6.13.1
0x8c40	DDC B Trigger Length LSB	R/W	Section 6.13.5
0x8c48	DDC B Trigger Length MSB	R/W	
0x8c50	DDC FIFO B Interrupt Mask	R/W	Section 6.13.3
0x8c58	DDC FIFO B Almost Empty Level	R/W	Section 6.13.6
0x8c60	DDC FIFO B Almost Full Level	R/W	Section 6.13.7
0x8c68	DDC FIFO C Control	R/W	Section 6.13.1
0x8c70	DDC C Trigger Length LSB	R/W	Section 6.13.5
0x8c78	DDC C Trigger Length MSB	R/W	
0x8c80	DDC FIFO C Interrupt Mask	R/W	Section 6.13.3
0x8c88	DDC FIFO C Almost Empty Level	R/W	Section 6.13.6
0x8c90	DDC FIFO C Almost Full Level	R/W	Section 6.13.7
0x8c98	DDC FIFO D Control	R/W	Section 6.13.1
0x8ca0	DDC D Trigger Length LSB	R/W	Section 6.13.5
0x8ca8	DDC D Trigger Length MSB	R/W	
0x8cb0	DDC FIFO D Interrupt Mask	R/W	Section 6.13.3
0x8cb8	DDC FIFO D Almost Empty Level	R/W	Section 6.13.6
0x8cc0	DDC FIFO D Almost Full Level	R/W	Section 6.13.7

* Offset from PCI Base Address Register 2 (**BAR2**), see Table 3–1

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3.3 Memory Maps (continued)

3.3.2 FPGA Memory Maps (continued)

NOTE: Access these registers using PCI Base Address Register 2 (**BAR2**).

Table 3–3: FPGA Registers Memory Map (continued)

Address Offset *	Register	Access	Information
A/D, DownConverter Registers (continued)			
0x8cc8	ADC 1 FIFO Control	R/W	Section 6.12.1
0x8cd0	ADC 1 Trigger Length LSB	R/W	Section 6.12.6
0x8cd8	ADC 1 Trigger Length MSB	R/W	
0x8ce0	ADC 1 FIFO Interrupt Mask	R/W	Section 6.12.3
0x8ce8	ADC 1 FIFO Almost Empty Level	R/W	Section 6.12.7
0x8cf0	ADC 1 FIFO Almost Full Level	R/W	Section 6.12.8
0x8cf8	ADC 1 FIFO Decimation Divider	R/W	Section 6.12.9
0x8d00	ADC 2 FIFO Control	R/W	Section 6.12.1
0x8d08	ADC 2 Trigger Length LSB	R/W	Section 6.12.6
0x8d10	ADC 2 Trigger Length MSB	R/W	
0x8d18	ADC 2 FIFO Interrupt Mask	R/W	Section 6.12.3
0x8d20	ADC 2 FIFO Almost Empty Level	R/W	Section 6.12.7
0x8d28	ADC 2 FIFO Almost Full Level	R/W	Section 6.12.8
0x8d30	ADC 2 FIFO Decimation Divider	R/W	Section 6.12.9
0x8d38	Test FIFO Control	R/W	Section 6.18.1
0x8d40	Test FIFO Flags Interrupt Mask	R/W	Section 6.18.3
0x8d48	Test FIFO Almost Empty Level	R/W	Section 6.18.4
0x8d50	Test FIFO Almost Full Level	R/W	Section 6.18.5
0x8d58	Delay Memory Read FIFO Control	R/W	Section 6.17.7
0x8d60 - 0x8d68	Reserved	–	–
0x8d70	Delay Memory Read FIFO Flags Interrupt Mask	R/W	Section 6.17.9
0x8d78	Delay Memory Read FIFO Almost Empty Level	R/W	Section 6.17.10
0x8d80	Delay Memory Read FIFO Almost Full Level	R/W	Section 6.17.11
0x8d88	Delay Memory Write FIFO Control	R/W	Section 6.17.7
0x8d90 - 0x8d98	Reserved	–	–
0x8da0	Delay Memory Write FIFO Flags Interrupt Mask	R/W	Section 6.17.9
0x8da8	Delay Memory Write FIFO Almost Empty Level	R/W	Section 6.17.10
0x8db0	Delay Memory Write FIFO Almost Full Level	R/W	Section 6.17.11
0x8db8 - 0xbff8	Reserved	–	–
0xc000 - 0xcff8	GC4016 Registers 0–31	R/W	Section 6.14

* Offset from PCI Base Address Register 2 (**BAR2**), see Table 3–1

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Chapter 4: Model 7140 Resource Operation

4.1 Overview

This chapter describes operation of the Model 7140 resources from a PMC baseboard processor. Routines for programming these resources are available in the ReadyFlow board support software for the Model 7140 (see Section 1.15).

4.2 Analog to Digital Input Conversion

The Model 7140 is designed for a maximum input sampling frequency of 105 MHz, with a minimum sampling rate of 30 MHz. It accepts two analog RF inputs at +4dBm full scale into 50 ohms on front panel MMCX connectors. Each of the two inputs is transformer coupled, and digitized by an Analog Devices AD6645 14−bit, 80−MHz (optionally 105−MHz) A/D converter. Refer to the Analog Devices AD6645 data sheet (see Section 1.16) for description of the A/D converter operation. There are no user−programmable registers for the AD6645 on the Model 7140.

The outputs of the A/Ds are delivered, in parallel, to the FPGA through two 14−bit paths. Each of these data paths is routed to the TI Graychip GC4016 DDC as follows:

- A/D 1 (Front Panel CH 1 IN) output to DDC channels A and C (switchable)
- A/D 2 (Front Panel CH 2 IN) output to DDC channels B and D (switchable)

See Section 4.3 for description of DDC Operation.

In addition, the outputs of the two A/Ds are routed to two PCI Interface FIFOs:

- A/D 1 output to ADC 1 FIFO
- A/D 2 output to ADC 2 FIFO

Refer to Section 7.3, ADC Data Routing and Formatting, for additional information about the formatting of this data. See Section 4.5 for description of FIFO Operation.

Each A/D output is also routed to the Delay Memory, see Section 4.7.

When TEST RAMP is enabled, each A/D output to the FIFOs and Delay Memory is replaced by a test pattern. TEST RAMP does not affect the routing of A/D data to the DDC channels. See TEST RAMP in the Miscellaneous Control Register, Section 6.6.

The clock source for the A/D converters can be selected from one of two different sources, Sync Bus A or Sync Bus B. See Section 4.8 for description of the board's Timing and Synchronization.

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4.3 Digital Downconversion

The Model 7140 includes one TI Graychip GC4016 quad narrowband digital receiver chip. The GC4016 accepts four 14−bit parallel or three 16−bit inputs from the FPGA. The FPGA provides data paths to the GC4016 and supports both 14−bit and 16−bit input modes. A crossbar switch inside the GC4016 allows each of the four receiver channels to independently select any input source.

The FPGA determines the source of GC4016 input data. These sources include the A/D converters, FPGA signal processing engines, SDRAM delay memory, and data sources on the PCI bus. This path allows raw A/D data to be routed to the GC4016, or signals that have been processed or time−delayed inside of the FPGA to be sent to the digital downconverter's input.

The outputs of the two Analog Devices AD6645 A/Ds are routed by default to the Graychip GC4016 DDC as follows:

- A/D 1 output to DDC channels A and C; the C input can be switched to a Delay Memory output
- A/D 2 output to DDC channels B and D; the D input can be switched to a Delay Memory output

Refer to the TI Graychip GC4016 data sheet (see Section 1.16) for description of the DDC operating modes. Setup and operation of the GC4016 is controlled from the 7140 by a set of FPGA registers, described in Section 6.14. The GC4016 must be set up for parallel output mode (**SFS_MODE**=2) at the full clock rate. The GC4016 **RDY** signal indicates the start of a data frame and the **SFS** signal denotes valid data samples. The data is collected from the GC4016 as 24−bit parallel words, regardless of whether the GC4016 is set for 16− or 24−bit mode.

The GC4016 can be set up for 2 or 4−bit tagging (see Section 1.16 for GC4016 Data Sheet), as follows. If you set GC4016 control bit **TAG_EN**=1, four tag bits replace the four LSBs of the 24−bit output word. If you set GC4016 control bit **TAG_22**=1, two tag bits replace the two LSBs of the 24−bit output word. The 7140 FPGA uses this tag to route the 24−bit data word (including the tag) to the applicable DDC FIFO.

The GC4016 delivers a real or complex parallel data stream to the FPGA for formatting and routing. The FPGA provides unpacked and packed data formats. The formatted DDC data is then routed to the DDC FIFOs (DDC A, B, C, and D FIFO) for access from the PMC baseboard. Refer to Section 7.4, DDC Data Routing and Formatting, for addi−tional information about the data packing modes and formats. See Section 4.5 for description of FIFO Operation.

The clock and sync signal source for the GC4016 digital receiver is the same as the clock source for the A/D converters. Choosing the A/D source selects the digital receiver source automatically. See Section 4.8 for description of the board's Timing and Syn−chronization.

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4.4 Digital To Analog Output

The Model 7140 is designed with a maximum output sample rate of 320 MHz in upconverter mode and 500 MSPS in D/A only mode. One Texas Instruments 16–bit DAC5686 is used to produce a pair of analog outputs capable of operating in D/A only, quadrature modulation, and single–sideband upconversion modes. The D/A has built–in interpolation filters settable to 2x, 4x, 8x, and 16x.

When operating as an upconverter, it interpolates and translates real or complex base–band input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs through two 320 MHz 16–bit D/A converters to two front panel MMCX connectors at +4dBm full scale into 50 ohms.

In D/A only mode the DAC5686 acts as a dual interpolating 16–bit D/A producing two independent outputs with output sampling rates up to 500 MSPS. In modes that include frequency translation, the DAC5686 accepts real or complex inputs and pro–duces an upconverted and interpolated, real or complex single output.

Refer to the Texas Instruments DAC5686 data sheet (see Section 1.16) for description of DAC operation. Setup and operation of the DAC5686 is controlled by a set of FPGA registers, described in Section 6.16.

The FPGA routes data from two DAC FIFOs to the DAC channels A and B, as follows:

- DAC A FIFO to DAC channel A (Front Panel CH 1 OUT)
- DAC B FIFO to DAC channel B (Front Panel CH 2 OUT)

In certain data packing modes, only DAC A FIFO is used both DAC5686 input chan–nels. Refer to Section 7.5, DAC Data Routing and Formatting, for additional informa–tion about these data packing modes and formats.

The clock and sync signals for the D/A converters can be selected from one of two dif–ferent sources, Sync Bus A or Sync Bus B. See Section 4.8 for description of the board's Timing and Synchronization.

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4.4 Digital To Analog Output (continued)

4.4.1 DAC5686 Digital Input Modes

Two digital data input modes are defined by the DAC5686. Data (I and Q) can be input to the DAC5686 from the FPGA as separate parallel streams on two data buses (**Dual Bus Mode**), or as a single interleaved data stream on one data bus (**Interleaved Bus Mode**). Refer to the Texas Instruments DAC5686 data sheet (see Section 1.16) for detailed descriptions of these input modes.

The FPGA provides four packing modes of DAC FIFO data that support these input modes. Refer to Section 7.5, DAC Data Routing and Formatting, for additional information about these data packing modes and formats. See Section 4.5 for description of FIFO Operation.

4.4.2 DAC5686 Operating Modes

The DAC5686 provides three modes of operation:

- In **Dual−channel Baseband I&Q Transmission** mode, interpolation filtering increases the DAC update rate, which reduces sinx/x roll−off and enables the use of relaxed analog post−filtering.

- **Single−sideband Up−conversion** mode provides optimum interfacing to analog quadrature modulators. Channel carrier selection is performed at baseband by mixing in the FPGA. Baseband I and Q from the FPGA are input to the DAC5686, which in turn performs a complex mix, resulting in Hilbert Transform pairs at the outputs of each DAC5686 chip's two DACs. An external RF quadrature modulator then performs the final single sideband up−conversion. DAC5686 complex mixing frequencies are flexibly chosen with the 32−bit programmable NCO. Unmatched gains and offsets at the RF quadrature modulator result in unwanted sideband and local oscillator feed−through. Each DAC in the DAC5686 has an 11−bit offset adjustment and 12−bit gain adjustment, which compensate for quadrature modulator input imbalances, thus reducing RF filtering requirements.

- In **Quadrature Modulation** mode, on−chip mixing provides baseband−to−IF up−conversion. Mixing frequencies are flexibly chosen with a 32−bit programmable NCO. Channel carrier selection is performed at baseband by complex mixing in the FPGA. Baseband I and Q from the FPGA are input to the DAC5686, which interpolates the low date rate signal to higher data rates. The single DAC output from DAC5686 is the final IF single−sideband spectrum presented to RF.

Refer to the Texas Instruments DAC5686 data sheet (see Section 1.16) for detailed descriptions of these operating modes.

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4.5 FIFO Operation

There are eleven user−programmable PCI Interface FIFOs in the FPGA, which provide direct high−speed data transfer between the PMC baseboard PCI bus and various resources on the 7140.

NOTE: PCI bus interface FIFOs are 64 bits wide. In this manual, data formats are described in reference to 32−bit words. Thus, whenever data is read from or written to the FIFOs, it is formatted as two 32−bit words for each FIFO word.

- Each DDC, ADC, Memory, and Test FIFO is 8 KBytes deep (1K x 64 on PCI bus side, 2K x 32 on device side).
- Each DAC FIFO is 64 KBytes deep (8K x 64 on PCI bus side, 16K x 32 on DAC side).

The following block diagram illustrates the interfaces and data flow for the 7140 FIFOs.

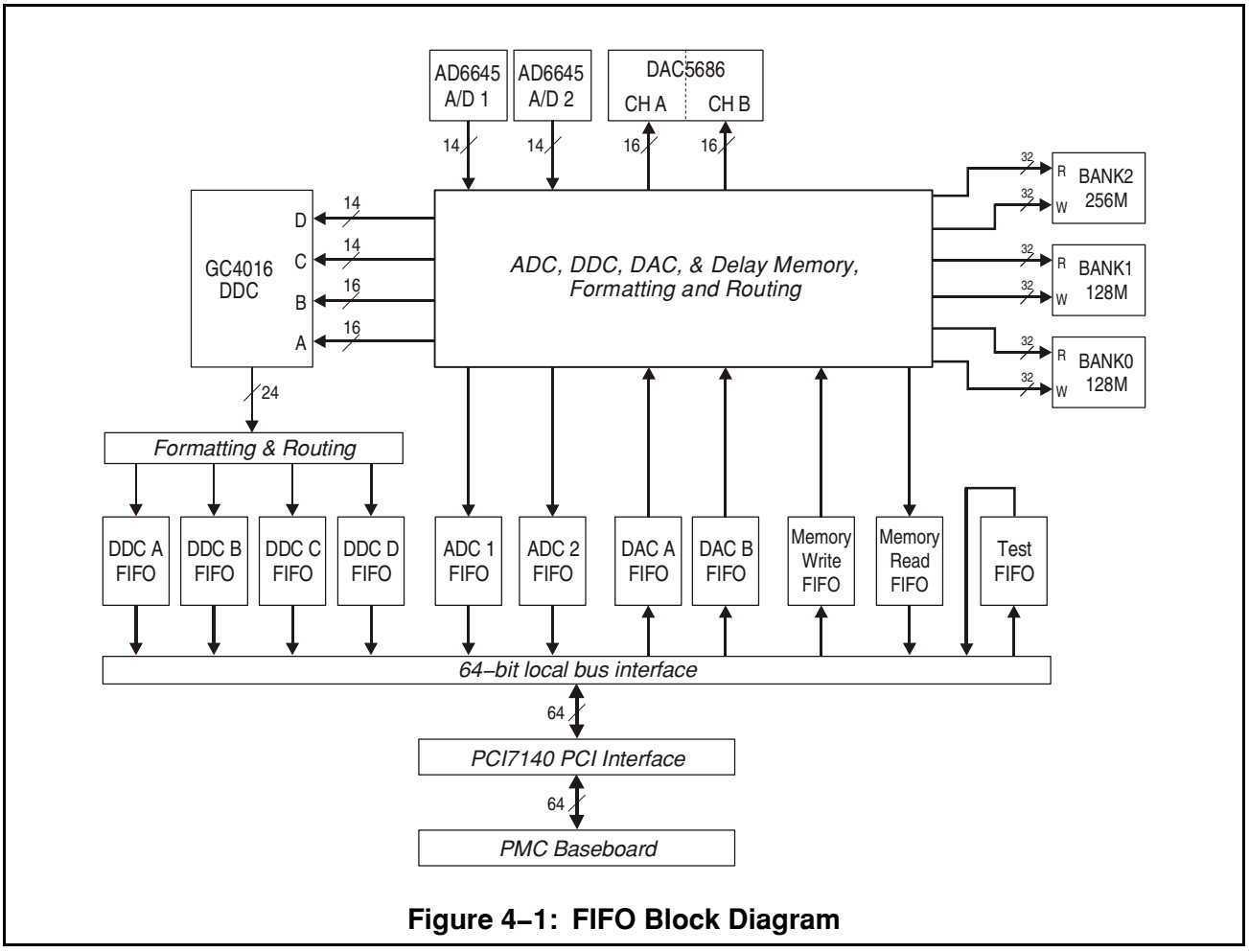


Figure 4−1: FIFO Block Diagram

The following pages identify the 7140 registers used for setting the FIFO boundary flag levels, enabling interrupts from FIFO flags, and monitoring FIFO status bits.

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4.5 FIFO Operation (continued)

4.5.1 Initializing the FIFOs

1) First, set the programmable Almost Full and Almost Empty boundary flag levels using the applicable FIFO AE/AF Level Registers, as listed below.

FIFO	Register	Reference
DDC A FIFO	DDC FIFO A AE/AF Levels	Sections 6.13.6, 6.13.7
DDC B FIFO	DDC FIFO B AE/AF Levels	
DDC C FIFO	DDC FIFO C AE/AF Levels	
DDC D FIFO	DDC FIFO D AE/AF Levels	
ADC 1 FIFO	ADC 1 FIFO AE/AF Levels	Sections 6.12.7, 6.12.8
ADC 2 FIFO	ADC 2 FIFO AE/AF Levels	
DAC A FIFO	DAC FIFO A AE/AF Levels	Sections 6.15.6, 6.15.7
DAC B FIFO	DAC FIFO B AE/AF Levels	
Delay Memory Read FIFO	Delay Memory Read FIFO AE/AF Levels	Sections 6.17.10, 6.17.11
Delay Memory Write FIFO	Delay Memory Write FIFO AE/AF Levels	
Test FIFO	Test FIFO AE/AF Levels	Sections 6.18.4, 6.18.5

2) Next, reset the FIFO using bit D01 of the applicable FIFO Control Register, listed below.

FIFO	Register	Reference
DDC A FIFO	DDC FIFO A Control	Section 6.13.1
DDC B FIFO	DDC FIFO B Control	
DDC C FIFO	DDC FIFO C Control	
DDC D FIFO	DDC FIFO D Control	
ADC 1 FIFO	ADC 1 FIFO Control	Section 6.12.1
ADC 2 FIFO	ADC 2 FIFO Control	
DAC A FIFO	DAC FIFO A Control	Section 6.15.1
DAC B FIFO	DAC FIFO B Control	
Delay Memory Read FIFO	Delay Memory Read FIFO Control	Section 6.17.7
Delay Memory Write FIFO	Delay Memory Write FIFO Control	
Test FIFO	Test FIFO Control	Section 6.18.1

NOTE: While the FIFO is in reset, you cannot read or write to the FIFO. You must clear the FIFO Reset bit (bit D01 of the applicable register, above) and then wait four clock cycles before you can write to the FIFO.

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4.5 FIFO Operation (continued)

4.5.1 Initializing the FIFOs (continued)

3) Next, enable the desired boundary flag interrupts using the applicable FIFO Interrupt Mask Register, as listed below.

FIFO	Register	Reference
DDC A FIFO	DDC FIFO A Interrupt Mask	Section 6.13.3
DDC B FIFO	DDC FIFO B Interrupt Mask	
DDC C FIFO	DDC FIFO C Interrupt Mask	
DDC D FIFO	DDC FIFO D Interrupt Mask	
ADC 1 FIFO	ADC 1 FIFO Interrupt Mask	Section 6.12.3
ADC 2 FIFO	ADC 2 FIFO Interrupt Mask	
DAC A FIFO	DAC FIFO A Interrupt Mask	Section 6.15.3
DAC B FIFO	DAC FIFO B Interrupt Mask	
Delay Memory Read FIFO	Delay Memory Read FIFO Interrupt Mask	Section 6.17.9
Delay Memory Write FIFO	Delay Memory Write FIFO Interrupt Mask	
Test FIFO	Test FIFO Interrupt Mask	Section 6.18.3

4) Next, select the source and characteristics of the gates used to control the FIFO writes using the applicable FIFO Control Register, as listed below.

FIFO	Register	Reference
DDC A FIFO	DDC FIFO A Control	Section 6.13.1
DDC B FIFO	DDC FIFO B Control	
DDC C FIFO	DDC FIFO C Control	
DDC D FIFO	DDC FIFO D Control	
ADC 1 FIFO	ADC 1 FIFO Control	Section 6.12.1
ADC 2 FIFO	ADC 2 FIFO Control	
DAC A FIFO	DAC FIFO A Control	Section 6.15.1
DAC B FIFO	DAC FIFO B Control	
Delay Memory Read FIFO	Delay Memory Read FIFO Control	NA
Delay Memory Write FIFO	Delay Memory Write FIFO Control	
Test FIFO	Test FIFO Control	

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4.5 FIFO Operation (continued)

4.5.1 Initializing the FIFOs (continued)

5) Next, if using trigger mode, set the Trigger Length using the applicable FIFO Trigger Length Registers, as listed below.

FIFO	Register	Reference
DDC A FIFO	DDC FIFO A Trigger Length	Section 6.13.5
DDC B FIFO	DDC FIFO B Trigger Length	
DDC C FIFO	DDC FIFO C Trigger Length	
DDC D FIFO	DDC FIFO D Trigger Length	
ADC 1 FIFO	ADC 1 FIFO Trigger Length	Section 6.12.6
ADC 2 FIFO	ADC 2 FIFO Trigger Length	
DAC A FIFO	DAC FIFO A Trigger Length	Section 6.15.5
DAC B FIFO	DAC FIFO B Trigger Length	
Delay Memory Read FIFO	Delay Memory Read FIFO Trigger Length	NA
Delay Memory Write FIFO	Delay Memory Write FIFO Trigger Length	
Test FIFO	Test FIFO Trigger Length	

6) Finally, enable the FIFO operation using the applicable FIFO Control Register, as listed below.

FIFO	Register	Reference
DDC A FIFO	DDC FIFO A Control	Section 6.13.1
DDC B FIFO	DDC FIFO B Control	
DDC C FIFO	DDC FIFO C Control	
DDC D FIFO	DDC FIFO D Control	
ADC 1 FIFO	ADC 1 FIFO Control	Section 6.12.1
ADC 2 FIFO	ADC 2 FIFO Control	
DAC A FIFO	DAC FIFO A Control	Section 6.15.1
DAC B FIFO	DAC FIFO B Control	
Delay Memory Read FIFO	Delay Memory Read FIFO Control	Section 6.17.7
Delay Memory Write FIFO	Delay Memory Write FIFO Control	
Test FIFO	Test FIFO Control	Section 6.18.1

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4.5 FIFO Operation (continued)

4.5.2 FIFO Data Transfers

Following FIFO Initialization as described in Section 4.5.1, the FIFO is ready for data transfers. The PMC baseboard performs FIFO reads and writes using DMA Operation. Refer to Section 4.6 on the next page for a description of DMA Operation.

PMC baseboard data reads occur from an Incoming FIFO and writes occur to an Outgoing FIFO. Read and write operations will cause the appropriate FIFO status flags to be set and cleared when the data reaches the programmed boundary conditions.

You can monitor the FIFO operation using the applicable FIFO Status Register, as listed below.

Table 4–1: FIFO Status Registers

FIFO	Register	Reference
DDC A FIFO	DDC FIFO A Status	Section 6.13.2
DDC B FIFO	DDC FIFO B Status	
DDC C FIFO	DDC FIFO C Status	
DDC D FIFO	DDC FIFO D Status	
ADC 1 FIFO	ADC 1 FIFO Status	Section 6.12.2
ADC 2 FIFO	ADC 2 FIFO Status	
DAC A FIFO	DAC FIFO A Status	Section 6.15.2
DAC B FIFO	DAC FIFO B Status	
Delay Memory Read FIFO	Delay Memory Read FIFO Status	Section 6.17.8
Delay Memory Write FIFO	Delay Memory Write FIFO Status	
Test FIFO	Test FIFO Status	Section 6.18.2

Read and write operations will also cause the appropriate FIFO status flags to assert PCI interrupts if enabled. See Section 4.9 for description of the Interrupt Operation using the FIFO flag bits.

See Section 7.3, ADC Data Routing and Formats, for additional information about the formatting of ADC FIFO data. See Section 7.4, DDC Data Routing and Formats, for DDC FIFO data formats. See Section 7.5, DAC Data Routing and Formats, for DAC FIFO packing modes and formats.

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4.6 DMA Operation

The PMC baseboard performs FIFO reads and writes using DMA operation. The PCI7140 incorporates nine high−performance DMA channels. The nine DMA channels (DMA0 through DMA8) are assigned to the PCI Interface FIFOs (Section 4.5) as shown in the following table:

Table 4–2: DMA Use by FIFOs

DMA Channel	FIFO	Direction *
DMA0	DDC A FIFO	Incoming
DMA1	DDC B FIFO	Incoming
DMA2	DDC C FIFO	Incoming
DMA3	DDC D FIFO	Incoming
DMA4	ADC 1 FIFO	Incoming
DMA5	ADC 2 FIFO	Incoming
DMA6	DAC A FIFO	Outgoing
DMA7	DAC B FIFO	Outgoing
DMA8	Delay Memory Read FIFO	Incoming

* The FIFO direction, Incoming or Outgoing, is labeled in reference to the controlling PMC baseboard processor; that is, 'Incoming' refers to data flow from the 7140 devices to the PMC baseboard

Each DMA channel has the capability to transfer data between PCI devices, SDRAM, or 7140 devices. The DMA uses the FIFOs for temporary DMA data storage. These FIFOs allows all DMA channels to work concurrently since each channel utilizes a separate FIFO. For example, DMA0 transfers data from DDC channel A to the PCI bus using one FIFO, while DMA6 transfers data from the PCI bus to DAC output channel A using another FIFO.

The DMA channels are programmable by PCI masters using DMA Descriptors. Each DMA channel has four Descriptors that can be chained. Each Descriptor is loaded by the DMA controller into the channel's working registers while the DMA transaction is active.

DMA Demand mode is the recommended mode of DMA operation for the FIFOs, as described in Section 4.6.1.

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4.6 DMA Operation (continued)

4.6.1 DMA Demand Mode Operation

DMA demand mode operation uses the FIFO flags to gate the DMA control–ler on and off to ensure no loss of data.

To use DMA Demand Mode, set the following programmable flags and val–ues:

- In the DMA Command Status Register, Section 5.16, set Demand Mode to 1 (Enable) and set the Maximum Burst Count greater than 0.
- In the applicable FIFO Almost Full register (Section 6.12.8 for ADC FIFOs, Section 6.13.7 for DDC FIFOs, Section 6.15.7 for DAC FIFOs), set the FIFO Almost Full level greater than the burst length.
- In the applicable FIFO Almost Empty register (Section 6.12.7 for ADC FIFOs, Section 6.13.6 for DDC FIFOs, Section 6.15.6 for DAC FIFOs), set the FIFO Almost Empty level to the Almost Full level (above) minus 32.

The following shows the Pentek–recommended settings for each FIFO.

Table 4–3: Recommended Demand Mode Settings

FIFO	Max. Burst Count	Almost Full	Almost Empty
ADC/DDC FIFOs	512	544	512
DAC FIFOs	2048	6176	6144

Demand Mode operates as follows when set up as described above:

a) Reading from an ADC/DDC FIFO – When the ADC/DDC FIFO Almost Full condition occurs, a DMA Request is asserted to transfer data from the FIFO to the programmed destination address. When the Almost Empty occurs, the DMA Request is cleared.

b) Writing to a DAC FIFO – When the DAC FIFO Almost Empty condition occurs, a DMA Request is asserted to transfer data from the programmed source address to the FIFO. When the Almost Full occurs, the DMA Request is cleared.

Once the DMA transfers starts it will run until the Burst Count completes.

Figure 4–2 on the next page illustrates the DMA operation signal timing.

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4.6 DMA Operation (continued)

4.6.1 DMA Demand Mode Operation (continued)

Figure 4–2 below illustrates the DMA operation signal timing.

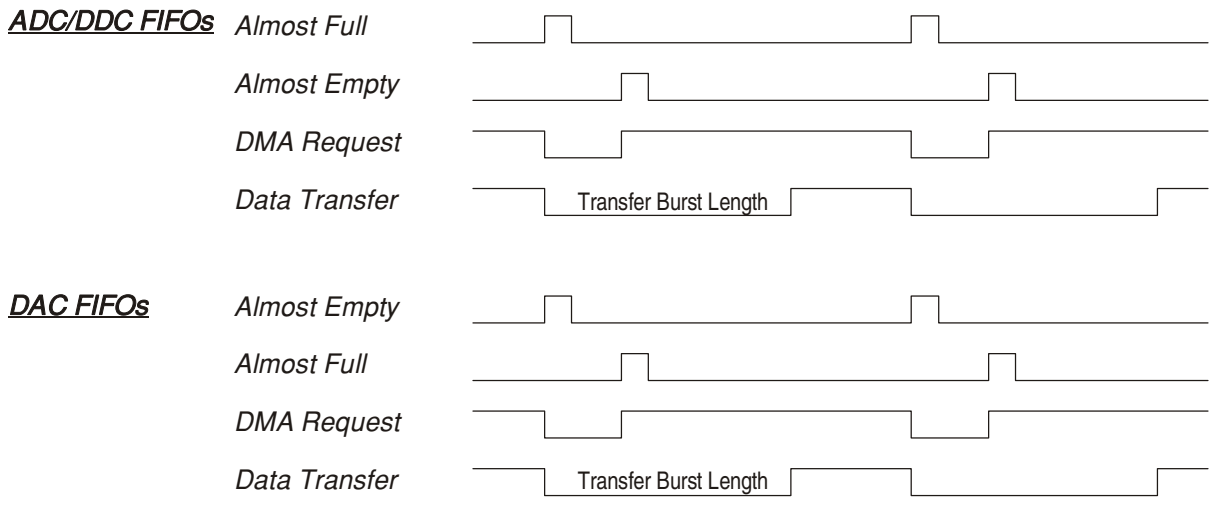


Figure 4–2: FIFO DMA Timing (2 cycles)

4.6.2 DMA Non–Demand Mode Operation

To use non–demand mode DMA operation, set the following programmable flags and values:

- In the DMA Command Status Register, Section 5.16, set Demand Mode to 0 (Disable) and set the Transfer Count Register, Section 5.18, equal to or less than the size of the applicable FIFO.
- Set the Maximum Burst Count in the DMA Command Status Register, Section 5.16, for non–demand mode as follows:
  - If the Maximum Burst Count = 0, the burst length will be the size of the Transfer Count.
  - If the Maximum Burst Count is greater than 0, the Burst Count (and Transfer Count) must be equal to or less than the size of the applicable FIFO.

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4.6 DMA Operation (continued)

4.6.3 DMA Channel Programming

Each DMA channel can programmed for separate, independent DMA transfers using the associated DMA Command/Status Register, Section 5.16, DMA Transfer Interval Counter Register, Section 5.17, and DMA Descriptor Registers. There are four Descriptors for each DMA channel, identified as Descriptor 0 through 3, and there are two registers for each descriptor, the DMA Descriptor Transfer Count Register, Section 5.18, and the DMA Descriptor PCI Address Register, Section 5.19.

To setup a DMA channel for operation (note that each set of registers used must be for the same DMA channel):

1) Use the DMA Command/Status Register, Section 5.16, to set the operating mode for the channel.

2) Use the DMA Descriptor Transfer Count Registers, Section 5.18, and the DMA Descriptor PCI Address Registers, Section 5.19, to specify the transfer count and PCI (source or destination) address for each Descriptor to be used for this data transfer. If using several descriptors, be sure to set the Chain bit D31=1 in each Descriptor Transfer Count Register. Setting bit D31=1 in the last Descriptor will cause the chain to go back to Descriptor 0.

3) If DMA interrupts are desired, enable the applicable interrupt bits in the PCI Interrupt Enable Register, Section 5.3. The types of DMA interrupts that can be generated by a DMA Channel are described in Section 4.6.4.

   If a DMA Chain Finish interrupt is desired, you must also enable the end of chain interrupt (bit D30) for that DMA channel in the DMA Descriptor Transfer Count Registers, Section 5.18.

4) Start the DMA operation using the DMA Command/Status Register, Section 5.16.

5) Use the DMA Current Transfer Count Register, Section 5.14, and the DMA Current PCI Address Register, Section 5.15, to monitor the progress of the data transfer.

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4.6 DMA Operation (continued)

4.6.4 DMA Interrupts

There are three types of DMA interrupts that can be generated during DMA operation. Each DMA channel (0 through 8) has a separate set of bits for generating, enabling, and monitoring each of these interrupts.

- DMA Chain Finish

  This interrupt is generated at the end of the last Descriptor transfer specified in the DMA Descriptor Transfer Count Registers, Section 5.18, when the Chain bit D31 is set to '0', End of Chain. This signifies completion of the entire linked chain of data transfers.

- DMA Descriptor Finish

  This interrupt is generated at the end of the Descriptor transfer count specified in each DMA Descriptor Transfer Count Register, Section 5.18. This signifies completion of just one of the Descriptor's data transfer.

- DMA Xfer Interval Count Finish

  This interrupt is generated at the end of the transfer interval count specified in the DMA Transfer Interval Counter Register, Section 5.17. This signifies completion of a designated portion of the data transfer. The DMA Transfer Interval Counter Register records a count of these interrupts.

  Transfer Interval Count is specified in words. Words are either 32 or 64 bits wide, as specified by Data Width, bit D07, in the DMA Command/ Status Register, Section 5.16.

When any of one of these conditions is generated, the applicable Flag bit is set in the PCI Interrupt Flag Register, Section 5.2, and an interrupt is gener–ated if enabled by the associated PCI Interrupt Enable Register, Section 5.3.

In addition, an interrupt can be generated during DMA operation if a buffer overrun has occurred on any DMA channel. When this condition occurs, the applicable Flag bit is set in the DMA PCI Interrupt Enable/Flag Register, Section 5.10, and a PCI interrupt is generated to the PCI bus if enabled by the associated Enable bit in this register.

See Section 4.9 for description of the board's Interrupt Operation.

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4.7 Delay Memory Operation

Three independent banks of DDR SDRAM are available for use as delay memory to support transient capture or popular applications such as tracking receivers. Two banks are 128 MBytes each and one bank is 256 MBytes for a total of 512 MBytes of available memory.

Use the Delay Memory Registers, Sections 6.17.1 through 6.17.6, to setup and control the operation of all Delay Memory data transfers.

Each memory bank has a set of registers to define a start point and an end point in the bank, to control the amount of memory to be accessed. The start point is set via the Delay Memory R/W Address LSB and Delay Memory R/W Address registers. The end point is set via the Delay Memory Depth LSB and Delay Memory Depth MSB registers.

The address applied to the address registers is a 32−bit offset from the memory base, in steps of eight 32−bit words. For example, to define a block of memory that starts 2048 bytes from the base of the memory, the R/W address registers would be set to 0x0200 (512). The next start address that could be set would be 0x208 (520), or 2080 bytes from the base.

The depth registers are also set with 32−bit values, with a step size of eight 32−bit words. For example, to define a 4096 byte block of memory that starts 2048 bytes from the base of memory, the R/W address registers would be set to 0x0200 (512) and the depth registers would be set to 0x0400 (1024). If the start address and depth results in a memory block that extends past the end of memory, the block of memory available will be from the current start address to the physical end of memory.

Once start and depth are defined, all memory accesses are restricted to that block of memory.

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4.7 **Delay Memory Operation** (continued)

The following is a simplified block diagram of the Delay Memory interfaces and control logic.

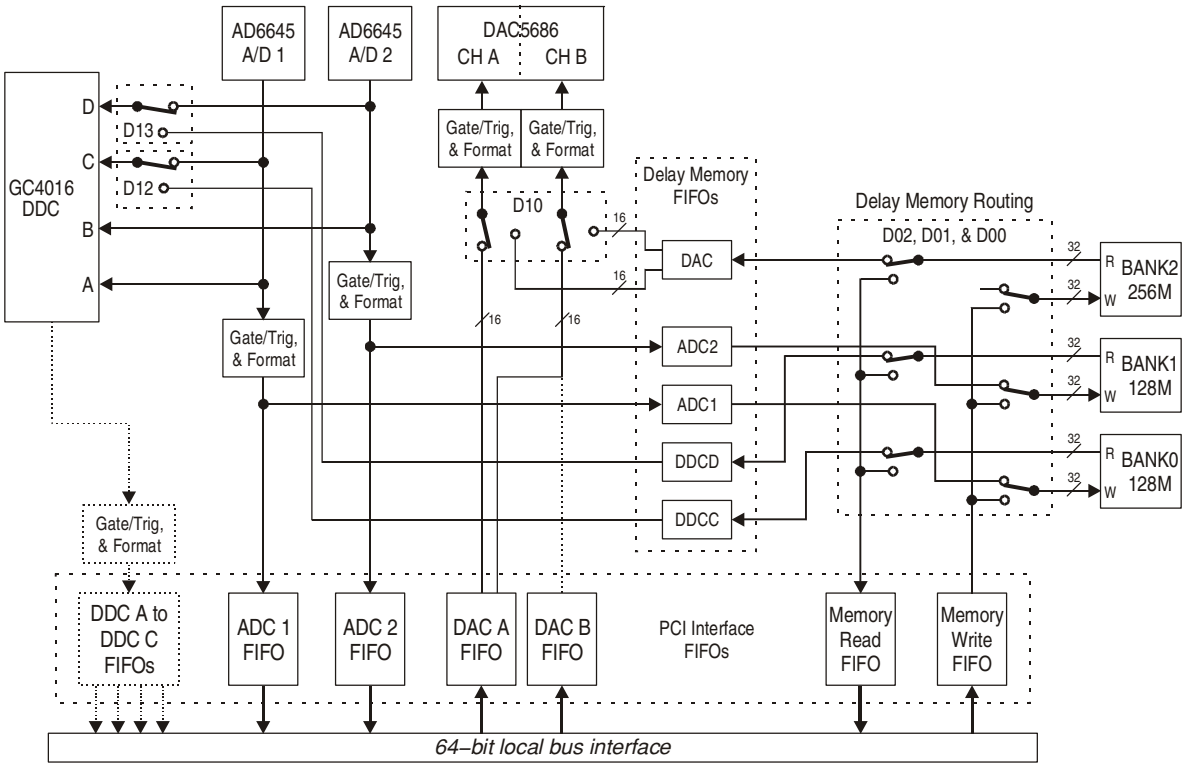


Figure 4–3: Delay Memory Control Logic
(Delay Memory Control Register bits indicated by Dxx – default position shown)

NOTE: The registers used for programming the PCI Interface ADC, DDC, and DAC FIFOs (Section 4.5) also set the same programming parameters for the associated Delay Memory ADC, DDC, and DAC FIFOs.

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4.7 Delay Memory Operation (continued)

4.7.1 Delay Memory FIFOs

There are five Delay Memory FIFOs on the Model 7140. Each FIFO size is 8 KBytes (2 KWord by 32 bits) and provides direct high−speed data transfer between the Delay Memory Banks (0, 1, and 2) and certain resources on the 7140. These FIFOs are used for data transfers from the ADC inputs to Delay Memory, or from Delay Memory to DDC inputs or DAC output, if enabled by the Delay Memory Control Register, Section 6.17.1.

NOTE: The Delay Memory interface FIFOs are 32 bits wide. Thus, whenever data is read from or written to these FIFOs, it is formatted as a single 32−bit word.

Figure 4−3 on the prior page illustrates the interfaces and data flow for the Delay Memory FIFOs. The following table lists the Delay Memory FIFOs and their use.

Table 4−4: Delay Memory FIFOs Use

Delay Memory FIFO	FIFO Use
DDCC FIFO	From Bank 0 to GC4016 DDC Channel C
DDCD FIFO	From Bank 1 to GC4016 DDC Channel D
ADC1 FIFO	From AD6645 Channel 1 to Bank 0
ADC2 FIFO	From AD6645 Channel 2 to Bank 1
DAC FIFO	From Bank 2 to DAC5686 Channels A and B

The registers used for programming the PCI Interface ADC, DDC, and DAC FIFOs (Section 4.5) also set the same programming parameters for the asso−ciated Delay Memory ADC, DDC, and DAC FIFOs.

4.7.2 Delay Memory Triggering

There are two types of triggering modes provided for data capture using the delay memory FIFOs, Pre−Trigger and Post−Trigger. These triggering modes are described in Section 4.8.4.

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4.8 Timing and Synchronization

The Model 7140 provides two internal timing buses, Sync Bus A and Sync Bus B, which provide two independent sets of clock, sync, and gate signals. The clock, sync, and gate signals can go out or in on the front panel LVDS Sync Bus connector (Section 2.6.4). This connector also provides two TTL Gate/Sync inputs that can be used by either Sync Bus. In addition, the front panel has two coaxial MMCX microminiature socket receptacles for input of external sample clocks. See Figure 4–4 on the next page for a logic diagram of these signals.

The LVDS Sync Bus includes two independent sets of clock, sync, and gate signals. The Sync Bus connector (Section 2.6.4) has signals for Bus A and Bus B. It allows one Model 7140 to act as a bus master, driving the sample clock, sync, and gate signals out to the connector using LVDS differential signaling. Additionally, the connector interface can be split to allow board–to–board interface of two independent buses: Bus A and Bus B. Up to seven slave 7140's can be driven on each bus, supporting synchronous sampling and sync functions across all connected boards. If more than seven boards need to be synchronized, Pentek's Model 9190 Clock and Sync Generator allows synchronization of up 80 I/O modules.

Each LVDS Sync Bus interface is connected to the board's internal sync buses. On each 7140, clock and sync signals for the A/D and DDC receiver can be driven from either Bus A or Bus B. Similarly the D/A section of each board can be driven from either sync bus, allowing the A/D, receiver, and upconverter sections to operate asynchronously if a different sync bus is used for each, or for the A/D, receiver, and upconverter sections to operate synchronously if the same bus is chosen for both.

Setup and operation of the Sync Buses is controlled by a set of FPGA registers, described in Section 6.10.

4.8.1 Sync

Sync signals are provided to the SYNC A input on the GC4016 DDC and to the Phase Synchronization input (PHSTR) on the DAC5686. Each sync can be driven directly from the front panel LVDS Sync Bus SYNC A or B signal (Section 2.6.4) if the Model 7140 is a Sync Bus Slave, or from a sync signal generated on the board.

Each onboard sync can be selected from a register write (Sync A/B Generator Register, Section 6.10.2 or Section 6.10.5), or the external TTL SYNC input (Section 2.6.4) can be selected for both syncs. The polarity of the external TTL SYNC input is programmable.

When the Model 7140 is a Sync Bus Master, the onboard generated sync is output to the respective LVDS Sync Bus.

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4.8 Timing and Synchronization (continued)

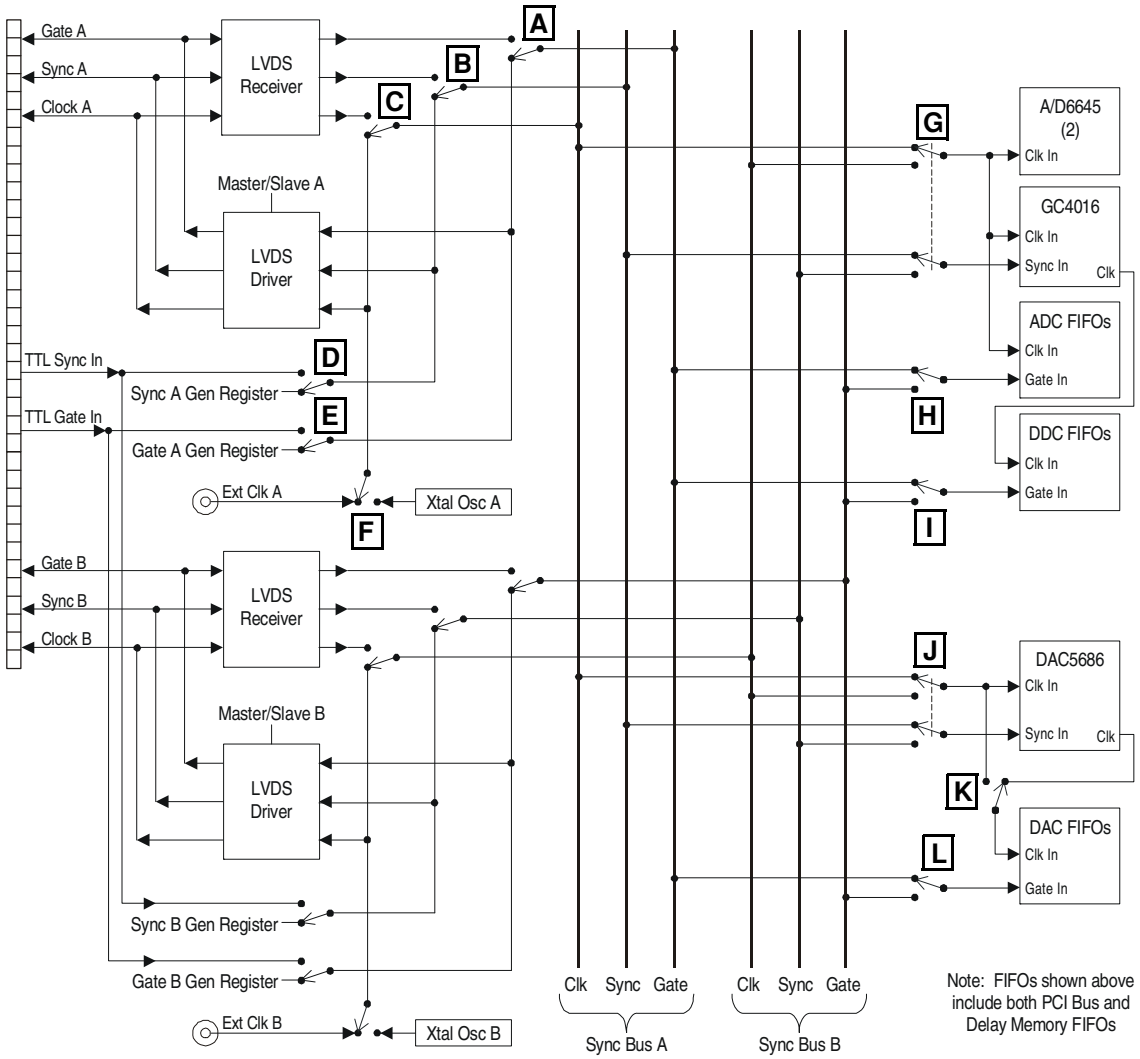


Figure 4–4: Gate/Sync/Clock Logic Diagram

Switches:
A – Master Bus Control Register, Section 6.10.1, bit D09, GATE SRC
B – Master Bus Control Register, Section 6.10.1, bit D06, SYNC SRC
C – Master Bus Control Register, Section 6.10.1, bit D04, CLK SRC
D – Master Bus Control Register, Section 6.10.1, bit D08, SEL GATE
E – Master Bus Control Register, Section 6.10.1, bit D05, SEL SYNC
F – Master Bus Control Register, Section 6.10.1, bit D02, SEL CLK
G – A/D Sync Bus Select Register, Section 6.10.9, bit D00, SEL
H – ADC FIFO Control Register, Section 6.12.1, bit D07, GATE SEL
I – DDC FIFO Control Register, Section 6.13.1, bit D07, GATE SEL
J– D/A Sync Bus Select Register, Section 6.10.8, bit D00, SEL
K – DAC Control/Status Register, Section 6.15.8, bit D03, DAC CLK
L – DAC FIFO Control Register, Section 6.15.1, bit D07, GATE SEL
(Only Sync Bus A references illustrated – See Section 6.10.4 for Sync Bus B control bits)

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4.8 Timing and Synchronization (continued)

4.8.2 Clocks

The clocks for all board functions (AD6645 A/Ds, GC4016 DDC, DAC5686, and FPGA FIFOs) can be driven from the front panel LVDS Sync Bus CLK A or B signal (Section 2.6.4) if the Model 7140 is a Sync Bus Slave, or from a clock generated on the board.

Each onboard clock can be selected either from an external MMCX CLK input (Section 2.6.3) or from the onboard crystal oscillators (selected by the Master Bus A/B Control Register, Section 6.10.1 or Section 6.10.4).

When the Model 7140 is a Sync Bus Master, the onboard clock is output to the respective LVDS Sync Bus.

4.8.3 Gates

Gates are used to enable writes to the PCI bus interface FIFOs and the Delay Memory FIFOs (ADC, DDC, and DAC FIFOs). Gate selection is controlled by the Master Bus A/B Control Register, Section 6.10.1 or 6.10.4, and by the individual FIFO Control Registers, Sections 6.12.1 (ADC FIFOs), 6.13.1 (DDC FIFOs), and 6.15.1 (DAC FIFOs). Gates may be individually disabled, in which case FIFO writes are always enabled.

Each gate can be driven directly from the front panel LVDS Sync Bus GATE A or B signal (Section 2.6.4) if the Model 7140 is a Sync Bus Slave, or from a gate signal generated on the board.

Each onboard generated gate can be selected from a register write (Gate A/B Generator Register, Section 6.10.3 or 6.10.6), or the external TTL GATE input (Section 2.6.4) can be selected for both gates. The polarity of each external TTL GATE input is programmable.

When the Model 7140 is a Sync Bus Master, the gate generated onboard is output to the respective LVDS Sync Bus.

Each gate may be programmed to act as a trigger (Trigger mode) using the FIFO Control Registers, Sections 6.12.1, 6.13.1, and 6.15.1. In this case, the gate is generated after a desired polarity logic transition on the external gate source or register write, and the resulting gate continues either indefinitely (Hold mode) or for a programmed number of FIFO writes up to 16,383 (Trigger Length). At any time the triggered gate may be asynchronously disabled by a control register write.

When Trigger mode is selected for a Gate signal, Pre– or Post–Triggering can be used for certain FIFOs, as described in the following subsection.

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4.8 Timing and Synchronization (continued)

4.8.4 Pre/Post–Triggering

When Trigger mode is selected for a Gate signal, Pre– or Post–Triggering can be used for certain FIFO data transfers. Use the applicable Trigger Length Registers, Sections 6.12.6, 6.13.5, and 6.15.5 to specify the trigger length.

Do not use Trigger HOLD mode with these functions.

- Post–Triggering (the default mode, ADC/DDC/DAC FIFOs)

  Post–Triggering allows you to specify a number of data samples to delay, after receipt of a trigger, before the data is actually transferred (written to or read from the associated FIFO). At the end of this delay, the data samples are transferred until the number of samples defined by the Trigger Length are transferred. Use the Post Trigger Count Registers, Sections 6.12.4, 6.13.4, and 6.15.4 to specify the post–trigger count.

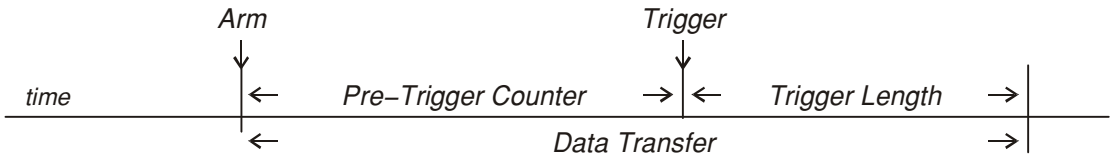
  Post–Triggering is illustrated below.



- Pre–Triggering (ADC FIFOs only)

  Pre–Triggering allows you to transfer data samples (write to the ADC FIFO) before receipt of the trigger. This transfer starts when you ARM the trigger with the ADC FIFO Control Register, Section 6.12.1. After the trigger is received, the data samples continue to be transferred until the number of samples defined by the Trigger Length are transferred, in addition to the Pre–Trigger count. Use the Pre Trigger Count Capture Registers, Section 6.12.5, to determine the actual number of A/D data samples stored in the ADC FIFO before receipt of the trigger.

  Pre–Triggering is illustrated below.



  Pre–Triggering is only provided for the ADC FIFOs, and should only be used for ADC writes to the Delay Memory, Section 4.7.

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4.9 Interrupt Operation

The 7140 PMC module can generate four PCI interrupt outputs, INTA through INTD, on the PCI bus to the PMC baseboard. Refer to the Operating Manual supplied with your PMC baseboard for description of the board's interrupt response operation.

The 7140 can handle four Local bus interrupt inputs, LINTi0 through LINTi3, received on the local PCI bus from 7140 resources.

The following logic diagram illustrates the interrupt signal routing on the Model 7140.

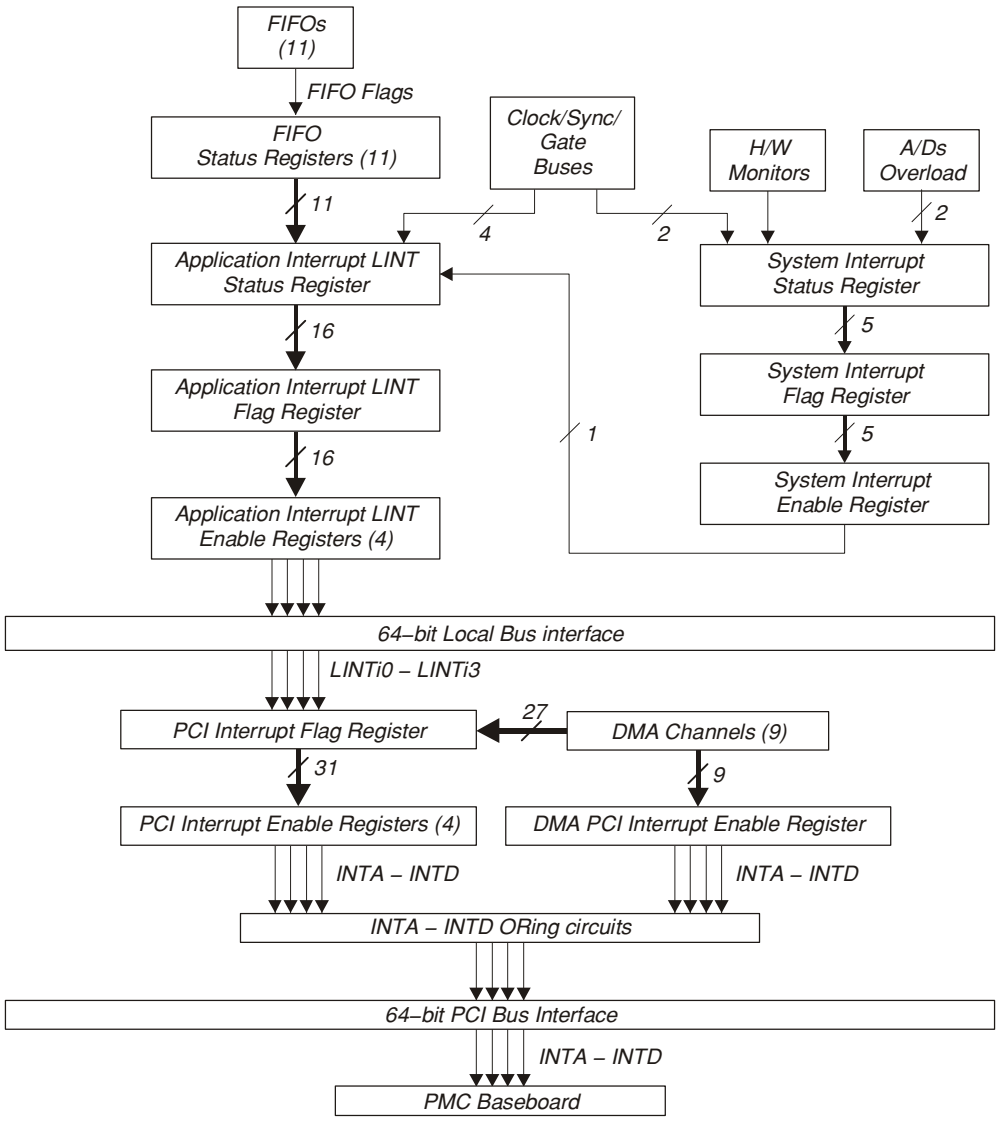


Figure 4–5: Interrupt Signal Logic Diagram

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4.9 Interrupt Operation (continued)

4.9.1 System Interrupts

The System Interrupt Registers (Sections 6.11.1 to 6.11.3) contain interrupt status, flag, and enable bits for several system interrupt conditions. The System Interrupts include the following signals/conditions:

- VOLT/TEMP – This interrupt is associated with a temperature/voltage limit interrupt from the LM83 or ADM1024 sensors. (To determine the sensor causing the interrupt, use the TWSI Port Register, Section 6.4.)
- CLK A LOSS, CLK B LOSS – Each of these interrupts is associated with a Clock loss interrupt from one of the 7140 Sync Buses, A or B.
- OVLD CH2, OVLD CH1 – Each of these interrupts is associated with an analog input overload interrupt from one of the A/D converters (A/D2 or A/D1).

In response to these interrupt signals, the System Interrupt Enable Register, Section 6.11.1, can be enabled to assert an interrupt to the Application Interrupt Registers, identified in Section 4.9.2 below.

4.9.2 Application Interrupts

The set of Application Interrupt Registers (Sections 6.11.4 to 6.11.6) contain interrupt status, flag, and enable bits for the FIFO Flags and the System Interrupt conditions. The Application Interrupts include the following signals/conditions:

- SYS INT – This interrupt is associated with an interrupt from the System Interrupt Enable Register, identified in Section 4.9.1 above.
- GATE B, GATE A – Each of these interrupts is associated with a Sync Bus GATE (A or B) interrupt. The interrupt occurs at the start of the respective gate signal.
- SYNC B, SYNC A – Each of these interrupts is associated with a Sync Bus SYNC (A or B) interrupt. The interrupt occurs at the start of the respective Sync pulse.

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4.9 Interrupt Operation (continued)

4.9.2 Application Interrupts (continued)

- TRIGGER CAPTURE – This interrupt is associated with an interrupt from the OR'ed result of the ADC, DDC, and DAC FIFO Trigger Capture bits. Use the applicable FIFO Status Registers, Sections 6.12.2, 6.13.2, and 6.15.2, to determine the interrupting FIFO.

- DELAY MEMORY READ FIFO – This interrupt is associated with a FIFO flag condition from the Delay Memory Read FIFO. Use the Delay Memory Read FIFO Status Registers, Section 6.17.8, to determine the interrupting condition from this FIFO.

- DELAY MEMORY WRITE FIFO – This interrupt is associated with a FIFO flag condition from the Delay Memory Write FIFO. Use the Delay Memory Write FIFO Status Registers, Section 6.17.8, to determine the interrupting condition from this FIFO.

- DAC A FIFO, DAC B FIFO – Each of these interrupts is associated with a FIFO flag condition from one of the DAC FIFOs (A or B). Use the DAC FIFO Status Registers, Section 6.15.2, to determine the interrupting condition from the associated FIFO.

- ADC 1 FIFO, ADC 2 FIFO – Each of these interrupts is associated with a FIFO flag condition from one of the ADC FIFOs (1 or 2). Use the ADC FIFO Status Registers, Section 6.12.2, to determine the interrupting condition from the associated FIFO.

- DDC A FIFO, DDC B FIFO, DDC C FIFO, DDC D FIFO – Each of these interrupts is associated with a FIFO flag condition from one of the DDC FIFOs (A, B, C, or D). Use the DDC FIFO Status Registers, Section 6.13.2, to determine the interrupting condition from the associated FIFO.

In response to these interrupt signals, any of the four Application Interrupt LINT Enable Registers, Section 6.11.4, can be enabled to assert any of the four local bus interrupt inputs, LINTi0 to LINTi3, to the PCI Interrupt Flag Registers, identified in Section 4.9.3 below.

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4.9 Interrupt Operation (continued)

4.9.3 Local Bus PCI Interrupts

The PCI Interrupt Registers (Section 5.2 and Section 5.3) contain interrupt flag and enable bits for the DMA Channels and the Application Interrupt conditions. The PCI Interrupts include the following signals/conditions:

- LINTix – Each of these interrupts is associated with one of the PCI local bus interrupt inputs, LINTi0 through LINTi3, from the Application Interrupt Enable Register, identified in Section 4.9.2 above.

- DMAn Chain Finish – Each of these interrupts is associated with a DMA Chain finish interrupt from the associated DMA channel. This interrupt is generated at the end of the last descriptor transfer specified in the DMA Descriptor Transfer Count Registers, Section 5.18, when the Chain bit D31 is set to '0', End of Chain.

- DMAn Descriptor Finish – Each of these interrupts is associated with a DMA Descriptor finish interrupt from the associated DMA. This interrupt is generated at the end of the descriptor transfer count specified in each DMA Descriptor Transfer Count Register, Section 5.18.

- DMAn Xfer Interval Count Finish – Each of these interrupts is associated with a DMA Xfer Interval Count Finish interrupt from that DMA. This interrupt is generated at the end of the transfer interval count specified in the DMA Transfer Interval Counter Register, Section 5.17.

  (See also Section 4.6.4 for further description of these DMA Interrupts.)

In response to these interrupt signals, any of the four PCI Interrupt Enable Registers, Section 5.3, can be enabled to assert any PCI bus interrupt output, INTA to INTD, to the PCI Bus, as identified in Section 4.9.5 below.

4.9.4 DMA PCI Interrupts

The DMA PCI Interrupt Enable/Flag Register (Section 5.10) contains interrupt flag and enable bits for DMA channel overrun conditions. In response to these conditions, this register can enabled assertion of any PCI bus interrupt output, INTA to INTD, to the PCI Bus, as described in Section 4.9.5 below.

Note that the PCI bus interrupts from this register are ORed with the PCI interrupts from the PCI Interrupt Enable Registers, Section 4.9.3, on the applicable PCI interrupt signal line (INTA to INTD).

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4.9 Interrupt Operation (continued)

4.9.5 PCI Bus Interrupt Outputs

Four PCI Bus interrupts, INTA to INTD, are associated with interrupt signals from the PCI Interrupt Flag Register, identified in Section 4.9.3 above, OR'ed with interrupt signals from the DMA PCI Interrupt Enable/Flag Register identified in Section 4.9.4 above.

Any of the four PCI Interrupt Enable Registers, Section 5.3, can be enabled to generate an interrupt from the OR'ed result of the flag bits, to the applicable PCI interrupt output, INTA to INTD. In addition any of the four PCI Bus interrupts can be enabled from the DMA PCI Interrupt Enable/Flag Register, Section 5.10. The PCI bus interrupt signals from both sets of registers are OR'ed on the applicable PCI interrupt line (INTA to INTD).

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4.10 Flash Memory Operation

A 16–MByte bank of FLASH memory is available to the FPGA and is organized as 8 M by 16 bits wide. FLASH memory provides nonvolatile storage for the PowerPC core in the FPGA.

The user can access this FLASH memory at memory address offset **0x0000** – **0x7fff**, using PCI Base Address Register 2 (**BAR2**). The Flash Page Register, Section 6.7, selects the page of FLASH memory to be addressed.

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Chapter 5: PCI7140 Registers

5.1 Overview

The XC2VP50 FPGA is connected to the PMC baseboard through a PCI Master/Slave interface (Standard PCI 2.2), the Pentek PCI7140. This interface provides direct Slave Mode and DMA Master/Slave Mode, 9−channel demand−mode, and chaining controller. Through this interface, any PCI Bus Master can control all programmable features on the board, the two AD6645s, the GC4016, the DAC5686, and all FPGA memory map registers. Data widths of 32 or 64 bits and data rates of 33 or 66 MHz guarantee compatibility with PMC, VME, cPCI, and PCI platforms.

This chapter describes the PCI7140 internal registers accessible from a PMC baseboard processor. All descriptions are given from the baseboard processor's viewpoint. All PCI7140 registers are 32 bits wide—however since the PCI local bus is a 64−bit data path, the register addresses are in increments of 64 bits (8 bytes). Refer to Section 3.3.1 for the memory map of all PCI7140 registers.

The following is a simplified block diagram of the PCI7140 interfaces, indicating the location of the PCI7140 internal registers. (See Figure 6−1 for a simplified block diagram of the XC2VP50 FPGA interfaces and its registers.)

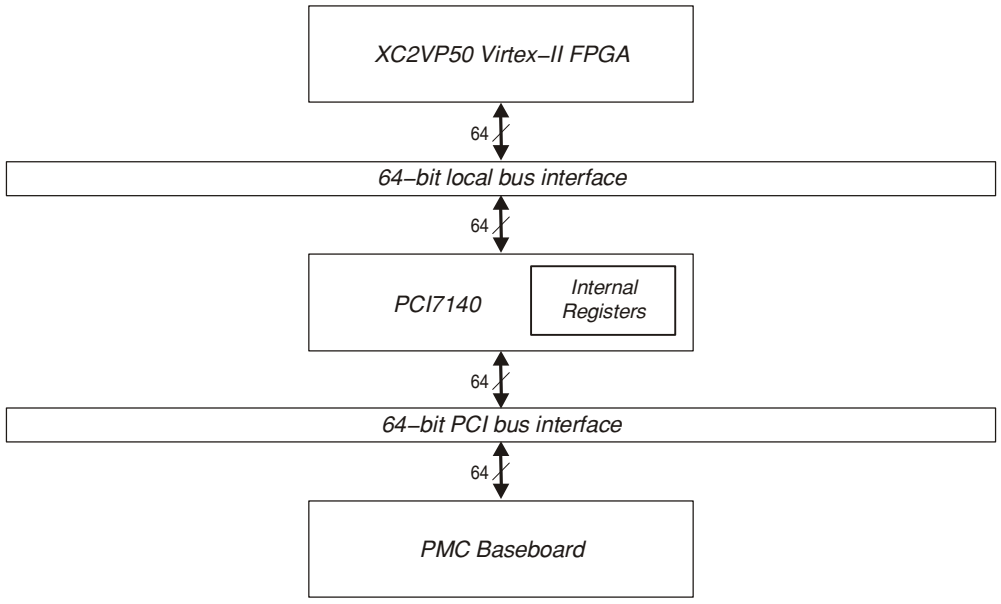


Figure 5−1: PCI7140 Interface Diagram

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5.2 PCI Interrupt Flag Register

The PCI Interrupt Flag Register has one read/clear bit associated with each interrupt condition from various 7140 resources.

The following table shows which bit in this register is associated with each interrupt condition. The paragraphs following the table provide descriptions of these bits.

Table 5–1: PCI Interrupt Flag Register
R/Clr @ BAR0+0x0000

	D31	D30	D29	D28	D27	D26	D25	D24
Bit Name	Reserved	LINTi3	LINTi2	LINTi1	LINTi0	DMA8 Xfer Interval Count Finish	DMA8 Descriptor Finish	DMA8 Chain Finish
Function	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch							
	D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
Bit Name	DMA7 Xfer Interval Count Finish	DMA7 Descriptor Finish	DMA7 Chain Finish	DMA6 Xfer Interval Count Finish	DMA6 Descriptor Finish	DMA6 Chain Finish	DMA5 Xfer Interval Count Finish	DMA5 Descriptor Finish
Function	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch							
	D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D09**	**D08**
Bit Name	DMA5 Chain Finish	DMA4 Xfer Interval Count Finish	DMA4 Descriptor Finish	DMA4 Chain Finish	DM3 Xfer Interval Count Finish	DMA3 Descriptor Finish	DMA3 Chain Finish	DMA2 Xfer Interval Count Finish
Function	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch							
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	DMA2 Descriptor Finish	DMA2 Chain Finish	DMA1 Xfer Interval Count Finish	DMA1 Descriptor Finish	DMA1 Chain Finish	DMA0 Xfer Interval Count Finish	DMA0 Descriptor Finish	DMA0 Chain Finish
Function	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch							

IMPORTANT! When reset, including power–up, the state of this register is unknown. You should clear this register before using it, by writing '1's into all bits.

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5.2 PCI Interrupt Flag Register (continued)

Each bit of this register latches an interrupt occurrence. A logic '1' in any bit in this register indicates that an interrupt has occurred.

Since these bits latch in response to an interrupt, to detect subsequent interrupts, you must clear the bits in this register. To clear any bit in this register that is set to logic '1' you must write a '1' to that bit.

The following table describes the interrupt condition associated with each bit of the PCI Interrupt Flag register.

Table 5–2: PCI Interrupt Flag Register Bits

Bit Name	Bit Positions	Interrupt Function
DMAn Chain Finish	D0, D3, D6, D9, D12 D15, D18, D21, D24	Each of these flag bits is associated with a DMA Chain finish interrupt on the PCI bus from the associated DMA. This interrupt is generated at the end of the last descriptor transfer specified in the DMA Descriptor Transfer Count Register, Section 5.18, when the Chain bit D31 is set to '0', End of Chain.
DMAn Descriptor Finish	D1, D4, D7, D10, D13 D16, D19, D22, D25	Each of these flag bits is associated with a DMA Descriptor finish interrupt on the PCI bus from the associated DMA. This interrupt is generated at the end of the descriptor transfer count specified in each DMA Descriptor Transfer Count Register, Section 5.18.
DMAn Xfer Interval Count Finish	D2, D5, D8, D11, D14 D17, D20, D23, D26	Each of these flag bits is associated with a DMA Transfer Interval Count finish interrupt on the PCI bus from the associated DMA. This interrupt is generated at the end of the transfer interval count specified in the DMA Transfer Interval Counter Register, Section 5.17.
LINTin	D27, D28, D29, D30	Each of these flag bits is associated with one of the PCI local bus interrupt inputs, LINTi0 through LINTi3. The PCI local bus interrupts are associated with the Application Interrupt LINT Enable Registers, Section 6.11.4.

Refer to Interrupt Operation, Section 4.9, for further description of interrupt routing and operation on the Model 7140.

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5.3 PCI Interrupt Enable Registers

The PCI Interrupt Enable Registers contains enable bits for each interrupt condition defined in the PCI Interrupt Flag Register, Section 5.2. Each bit enables or disables the generation of a PCI interrupt output to the PMC baseboard in response to these interrupts. There are four PCI Interrupt Enable Registers, one for each PCI bus interrupt (INTA to INTD). Each register enables interrupts for the respective PCI bus interrupt to the PMC baseboard.

The following table shows which bit in this register is associated with each interrupt condition. The paragraphs following the table provide descriptions of these bits.

Table 5–3: PCI Interrupt Enable Registers

INTA: R/W @ BAR0+0x0010
INTB: R/W @ BAR0+0x0018
INTC: R/W @ BAR0+0x0020
INTD: R/W @ BAR0+0x0028

	D31	D30	D29	D28	D27	D26	D25	D24
Bit Name	PCI INTx	LINTi3	LINTi2	LINTi1	LINTi0	DMA8 Xfer Interval Count Finish	DMA8 Descriptor Finish	DMA8 Chain Finish
Function	0 = Disable Interrupt 1 = Enable Interrupt							
	D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
Bit Name	DMA7 Xfer Interval Count Finish	DMA7 Descriptor Finish	DMA7 Chain Finish	DMA6 Xfer Interval Count Finish	DMA6 Descriptor Finish	DMA6 Chain Finish	DMA5 Xfer Interval Count Finish	DMA5 Descriptor Finish
Function	0 = Disable Interrupt 1 = Enable Interrupt							
	D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D09**	**D08**
Bit Name	DMA5 Chain Finish	DMA4 Xfer Interval Count Finish	DMA4 Descriptor Finish	DMA4 Chain Finish	DM3 Xfer Interval Count Finish	DMA3 Descriptor Finish	DMA3 Chain Finish	DMA2 Xfer Interval Count Finish
Function	0 = Disable Interrupt 1 = Enable Interrupt							
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	DMA2 Descriptor Finish	DMA2 Chain Finish	DMA1 Xfer Interval Count Finish	DMA1 Descriptor Finish	DMA1 Chain Finish	DMA0 Xfer Interval Count Finish	DMA0 Descriptor Finish	DMA0 Chain Finish
Function	0 = Disable Interrupt 1 = Enable Interrupt							

All bits default to the logic '0' state at power on and reset

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5.3 PCI Interrupt Enable Register (continued)

Each bit of this register enables or disables the generation of a PCI bus interrupt (INTA to INTD, depending on the register used) to the PMC baseboard. Setting the bit associated with a given interrupt to logic '1' enables the generation of a PCI bus interrupt when that interrupt condition occurs. When a bit is cleared to logic '0' (its default state), the PCI bus interrupt will not be generated by the defined interrupt condition.

The following table describes the interrupt condition associated with each bit of the PCI Interrupt Enable register.

Table 5–4: PCI Interrupt Enable Register Bits

Bit Name	Bit Positions	Interrupt Function
DMAn Chain Finish	D0, D3, D6, D9, D12 D15, D18, D21, D24	Each of these enable bits is associated with a DMA Chain finish interrupt on the PCI bus from the associated DMA. This interrupt is generated at the end of the last descriptor transfer specified in the DMA Descriptor Transfer Count Register, Section 5.18, when the Chain bit D31 is set to '0', End of Chain.
DMAn Descriptor Finish	D1, D4, D7, D10, D13 D16, D19, D22, D25	Each of these enable bits is associated with a DMA Descriptor finish interrupt on the PCI bus from the associated DMA. This interrupt is generated at the end of the descriptor transfer count specified in each DMA Descriptor Transfer Count Register, Section 5.18.
DMAn Xfer Interval Count Finish	D2, D5, D8, D11, D14 D17, D20, D23, D26	Each of these enable bits is associated with a DMA Transfer Interval Count finish interrupt on the PCI bus from the associated DMA. This interrupt is generated at the end of the transfer interval count specified in the DMA Transfer Interval Counter Register, Section 5.17.
LINTin	D27, D28, D29, D30	Each of these enable bits is associated with one of the local bus input interrupts, LINTi0 through LINTi3, from the FPGA. The PCI local bus interrupts are generated using the Application Interrupt LINT Enable Registers, Section 6.11.4.
PCI INTx	D31	This bit enables the PCI Interrupt output for the associated register, INTA through INTD.

Refer to Interrupt Operation, Section 4.9, for further description of interrupt routing and operation on the Model 7140.

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5.4 Board/Channel Reset Register

The Board/Channel Reset Register provides a reset for the entire 7140 PMC module.

The following table shows the contents of this register. The paragraphs following the table provide descriptions of the bits in this register.

Table 5–5: Board/Channel Reset Register
R/W @ BAR0+0x0070

	D31 – D16	
Bit Name	Not used	
Function	Write with zeros, Mask when reading	
	D15	**D14 – D00**
Bit Name	Board Reset	Reserved
Function	0 =Run 1 =Reset	Write with zeros, Mask when reading
All bits default to the logic '0' state at power on and reset		

Bit D15 issues a reset to the entire Model 7140 PMC module. When the bit is set to logic '1', the 7140 is in reset. When the bit is cleared to logic '0' (its default state), the 7140 is in a normal run state.

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5.5 PCI7140 Revision Register

The PCI7140 Revision Register identifies the Pentek version number and the date of the code currently installed in the PCI7140.

The following table shows the contents of this register. The paragraphs below PCI7140 Revision Register describe the contents of the register.

Table 5–6: PCI7140 Revision Register
R.O. @ BAR0+0x0078

	D31 – D28	D27 – D24	D23 – D20	D19 – D16
Bit Name	YEAR		MONTH	
Function	3rd Digit of Year	4th Digit of Year	1st Digit of Month	2nd Digit of Month
	D15 – D12	**D11 – D08**	**D07 – D00**	
Bit Name	DAY		PCI7140 CODE REVISION	
Function	1st Digit of Day	2nd Digit of Day	PCI7140 Pentek Code Revision Number	

The PCI7140 revision date is coded as six hexadecimal characters, as follows:

Year: Bits D31 – D28, 3rd digit of Year
Bits D27 – D24, 4th digit of Year

Month: Bits D23 – D20, 1st digit of Month
Bits D19 – D16, 2nd digit of Month

Day: Bits D15 – D12, 1st digit of Day
Bits D11 – D08, 2nd digit of Day

The PCI7140 Code Revision number (bits D07 – D00) is a binary value that identifies the Pentek version number of the code in the Pentek PCI7140 PCI interface chip, starting at revision 0.

For example, the date of **August 9, 2007** (8/9/07), with a code revision of '**G**', would appear as follows in the PCI7140 Revision Register.

PCI7140 Revision Register = **0x07080907**

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5.6 Virtex Config Register

The Virtex Config Register is used to reconfigure/reprogram the XC2VP50 FPGA. The bits in this register allow you to read and set the status of the FPGA configuration cycle, and to control uploading the configuration to the FPGA from a PMC baseboard processor. Refer to Section 1.14, FPGA Configuration, for additional information about configuring the FPGA.

The following table shows the contents of the Virtex Config Register. The subsections following the table provide descriptions of the bits in this register.

Table 5–7: Virtex Config Register
R/W @ BAR0+0x0080

	D31 – D16							
Bit Name	Not used							
Function	Write with zeros, Mask when reading							
	D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D09**	**D08**
Bit Name	D7	D6	D5	D4	D3	D2	D1	D0
Function	FPGA Configuration Data							
	D07	**D06**	**D05**	**D04**	**D03 ***	**D02 ***	**D01**	**D00**
Bit Name	WRITE STROBE	Reserved	DIRECTION	Reserved	$\overline{\text{INIT}}$	DONE	PRGM	LD SRC
Function	0 = Disable 1 = Enable	Write 0s, Mask read	0 = Read 1 = Write	Write 0s, Mask read	0 = Initializing 1 = Done	0 = Configuring 1 = Done	0 = Disable 1 = Reprogram	0 = EEPROM 1 = Upload

* These bits are Read Only
All bits default to the logic '0' state at power on and reset

5.6.1 Configuration Data [D7:D0] Bits D15 – D08

These eight bits contain the data to be written to the FPGA.

5.6.2 WRITE STROBE Bit D07

This bit enables the write strobe to the Virtex Config Data Register. When you set this bit to logic '1', you can write configuration data to the FPGA. Clear the bit to logic '0' (its default state) to disable writing configuration data to the FPGA.

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5.6 Virtex Config Register (continued)

5.6.3 DIRECTION Bit D05

This bit sets the read/write access of the Virtex Config Data Register. Clear the bit to logic '0' (its default state) to read configuration data from the FPGA. When you set this bit to logic '1', you can write configuration data to the FPGA. To write with the Virtex Config Data Register, you must also enable configuration upload (LD SRC bit D00 = 1, Section 5.6.7).

5.6.4 $\overline{\text{INIT}}$ Bit D03

This read–only bit indicates the status of the FPGA's '$\overline{\text{INIT}}$' pin. At initial–ization of a configuration cycle this bit goes to logic '0', then logic '1'. It remains at logic '0' if an error in configuration data is detected. When read as logic '1', initialization is done.

5.6.5 DONE Bit D02

This read–only bit indicates the status of the FPGA's 'DONE' pin. When read as logic '0', the FPGA is in the configuration cycle. When read as logic '1', the FPGA has completed configuration.

5.6.6 PRGM Bit D01

This bit starts the FPGA configuration reprogramming. The FPGA begins a configuration reprogramming cycle after you transition this bit from logic logic '1' to logic '0' while in Serial EEPROM or Processor Upload mode (see LD SRC, below, for proper sequence of setting bits D01 & D00).

5.6.7 LD SRC Bit D00

This bit selects the source of the FPGA configuration data. When you clear this bit to logic '0' (its default state), the FPGA selects the configuration data from the onboard Serial EEPROMs. When you set this bit to logic '1', the FPGA is in Processor Upload mode, and you can upload the configuration data using the Configuration Data bits (D15 – D08) in this register.

The sequence of setting bits D01 & D00 is shown below for each source.

Sequence	Processor Upload	Serial EEPROM
1)	Set D01:D00 = **11**	Set D01:D00 = **11**
2)	Set D01:D00 = **01**	Set D01:D00 = **00**
3)	Write data, bits D15:D08	
4)	Set D01:D00 = **00**	

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5.7 PCI DCM Control Register

The PCI DCM Control Register controls the Digital Clock Managers (DCM) on the PCI7140.

The following table shows the contents of the DCM Register. The subsections following the table provide descriptions of each control bit in this register.

Table 5–8: PCI DCM Control Register
R/W @ BAR0+0x0088

	D31 – D08							
Bit Name	Not used							
Function	Write with zeros, Mask when reading							
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01 ***	**D00 ***
Bit Name	Reserved					DCM RST	LOCKD 1	LOCKD 0
Function	Write with zeros, Mask when reading					0 =Run 1 =Reset	0 =Not locked 1 =Locked	0 =Not locked 1 =Locked

* These bits are Read Only
All bits default to the logic '0' state at power on and reset

5.7.1 DCM RST

Bit D02

This bit resets both DCM clocks 0 and 1. Set the bit to logic '1' to reset the DCM clocks. Clear the bit to logic '0' (its default state) to return the DCM clocks to normal operation.

5.7.2 LOCKD 1/0

Bits D01, D00

Each of these read–only bits indicates the locked status of a DCM clock. When read as logic '0' the DCM clock output is not locked. When read as logic '1' the DCM clock output is locked.

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5.8 Local DMA Request Status Register

The read–only Local DMA Request Status Register reads the DMA Request status of each DMA request. The following table shows the contents of this register.

NOTE: This register is for Pentek factory use only.

Table 5–9: Local DMA Request Status Register
R.O. @ BAR0+0x0090

	D31 – D16							
Bit Name	Not used							
Function	Write with zeros, Mask when reading							
	D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D09**	**D08**
Bit Name	Reserved				TEST FIFO Write	TEST FIFO Read	Delay Memory Write FIFO	Delay Memory Read FIFO
Function	Write with zeros, Mask when reading				Factory use only			
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	DAC B FIFO	DAC A FIFO	ADC 2 FIFO	ADC 1 FIFO	DDC D FIFO	DDC C FIFO	DDC B FIFO	DDC A FIFO
Function	Factory use only							
All bits default to the logic '0' state at power on and reset								

Register Bit	DMA Request Number	FIFO
D00	DMA Request 0	DDC A FIFO
D01	DMA Request 1	DDC B FIFO
D02	DMA Request 2	DDC C FIFO
D03	DMA Request 3	DDC D FIFO
D04	DMA Request 4	ADC 1 FIFO
D05	DMA Request 5	ADC 2 FIFO
D06	DMA Request 6	DAC A FIFO
D07	DMA Request 7	DAC B FIFO
D08	DMA Request 8	Delay Memory Read FIFO
D09	DMA Request 9	Delay Memory Write FIFO
D10	DMA Request 10	Test FIFO Read
D11	DMA Request 11	Test FIFO Write

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5.9 PCI Bus Status Register

The PCI Bus Status Register is a read–only register that indicates the speed of the PMC bus that the 7140 is connected to on the PMC baseboard, 33 MHz or 66 MHz.

The following table shows the contents of this register.

Table 5–10: PCI Bus Status Register
R.O. @ BAR0+0x00A0

	D31 – D01	D00
Bit Name	Reserved	Bus Speed
Function	Write with zeros, Mask when reading	0 = 33 MHz 1 = 66 MHz
All bits default to the logic '0' state at power on and reset		

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5.10 DMA PCI Interrupt Enable/Flag Register

The DMA PCI Interrupt Enable/Flag Register enables or disables assertion of a PCI interrupt to the PMC baseboard in response to a DMA channel buffer overrun.

The following table shows the contents of this register. The subsections following the table provide descriptions of the bits in this register.

Table 5–11: DMA PCI Interrupt Enable/Flag Register
R/Clr @ BAR0+0x00A8

	D31	D30	D29	D28	D27	D26	D25	D24
Bit Name	Reserved							
Function	Write with zeros, Mask when reading							
	D23	**D22**	**D21 ***	**D20**	**D19 ***	**D18**	**D17 ***	**D16**
Bit Name	Reserved		INTD	INTC	INTB	INTA	DMA8 FLAG	DMA8 EN
Function	Write with zeros, Mask when reading		0 = Disable 1 = Enable				0 = OK 1 = Overrun	0 = Disable 1 = Enable
	D15 *	**D14**	**D13 ***	**D12**	**D11 ***	**D10**	**D09 ***	**D08**
Bit Name	DMA7 FLAG	DMA7 EN	DMA6 FLAG	DMA6 EN	DMA5 FLAG	DMA5 EN	DMA4 FLAG	DMA4 EN
Function	0 = OK 1 = Overrun	0 = Disable 1 = Enable	0 = OK 1 = Overrun	0 = Disable 1 = Enable	0 = OK 1 = Overrun	0 = Disable 1 = Enable	0 = OK 1 = Overrun	0 = Disable 1 = Enable
	D07 *	**D06**	**D05 ***	**D04**	**D03 ***	**D02**	**D01 ***	**D00**
Bit Name	DMA3 FLAG	DMA3 EN	DMA2 FLAG	DMA2 EN	DMA1 FLAG	DMA1 EN	DMA0 FLAG	DMA0 EN
Function	0 = OK 1 = Overrun	0 = Disable 1 = Enable	0 = OK 1 = Overrun	0 = Disable 1 = Enable	0 = OK 1 = Overrun	0 = Disable 1 = Enable	0 = OK 1 = Overrun	0 = Disable 1 = Enable

* These bits are Read/Clear Flag bits. Each bit can be cleared only by writing a '1' to that bit.

IMPORTANT! When reset, including power–up, the state of the Read/Clear bits are unknown. You should clear this register before using it, by writing '1's into all FLAG bits.

Register Bits	DMA Channel	Associated FIFO
D00, D01	DMA0	DDC A FIFO
D02, D03	DMA1	DDC B FIFO
D04, D05	DMA2	DDC C FIFO
D06, D07	DMA3	DDC D FIFO
D08, D09	DMA4	ADC 1 FIFO
D10, D11	DMA5	ADC 2 FIFO
D12, D13	DMA6	DAC A FIFO
D14, D15	DMA7	DAC B FIFO
D16, D17	DMA8	Delay Memory Read FIFO

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5.10 DMA PCI Interrupt Enable/Flag Register (continued)

5.10.1 INTD/C/B/A Bits D21 – D18

Each of these four bits enables or disables the generation of a PCI bus interrupt (INTA to INTD, depending on the bit) to the PMC baseboard in response to a DMA channel buffer overrun. Setting a bit to logic '1' enables the generation of the associated PCI bus interrupt when any DMA FLAG bit in this register (Section 5.10.2 below) is set to '1' and the associated DMA EN bit in this register (Section 5.10.3 below) is set to '1'. When a bit is cleared to logic '0' (its default state), that PCI bus interrupt will not be generated.

Note that the PCI bus interrupt is ORed with the PCI interrupt from the PCI Interrupt Enable Registers, Section 5.3, on the applicable PCI interrupt signal line (INTA to INTD).

5.10.2 DMAn FLAG Bits D17/D15/D13/D11/D09/D07/D05/D03/D01

Each of these read/clear bits latches a buffer overrun condition for the respective DMA channel. Logic '1' in any bit indicates that a channel buffer overrun has occurred. Logic '0' indicates no buffer overrun. When one of these bits changes to '1' a PCI bus interrupt can be asserted if the associated DMA EN bit (Section 5.10.3 below) is enabled and one of the INTA/D bits is enabled (Section 5.10.1 above).

Since these bits latch in response to an interrupt, to detect a subsequent channel buffer overrun, you must clear the FLAG bits in this register. To clear any FLAG bit in this register that is set to logic '1' you must write a '1' to that bit.

5.10.3 DMAn EN Bits D16/D14/D12/D10/D08/D06/D04/D02/D00

Each of these bits enables or disables a DMA buffer overrun interrupt to the PCI Interrupt line enabled (INTD to INTA, Section 5.10.1 above). Setting the bit associated with a given DMA channel to '1' enables the interrupt when that channel overrun occurs. When a bit is cleared to logic '0' (its default state), the interrupt will not be generated by the channel overrun.

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5.11 Local DMA In Address Remap Register

The Local DMA In Address Remap Register permits remapping each incoming DMA channel for use with a different incoming FIFO.

The following table shows the contents of this register.

Table 5–12: Local DMA In Address Remap Register
R/W @ BAR0+0x00B0

	D31 – D28	D27 – D24	D23 – D20	D19 – D16	D15 – D12	D11 – D08	D07 – D04	D03 – D00
Bit Name	Reserved	DMA8	DMA5	DMA4	DMA3	DMA2	DMA1	DMA0
Function	Write 0s, Mask read	FIFO Codes, see below						
All bits default to the default FIFOs at power on and reset (see Table 5–13, below)								

Each incoming DMA channel has a four–bit field in this register that maps an incoming FIFO to that channel. The mapping code for the four bits in each field is as follows, in hex:

0x0 = DDC A FIFO
0x1 = DDC B FIFO
0x2 = DDC C FIFO
0x3 = DDC D FIFO
0x4 = ADC 1 FIFO
0x5 = ADC 2 FIFO
0x8 = Delay Memory Read FIFO
0xC = Test FIFO Read

The default mapping is shown in the following table:

Table 5–13: Default DMA In Mapping

DMA Channel	FIFO	Register Bits	Code
DMA0	DDC A FIFO	D03 – D00	**0**
DMA1	DDC B FIFO	D04 – D07	**1**
DMA2	DDC C FIFO	D08 – D11	**2**
DMA3	DDC D FIFO	D12 – D15	**3**
DMA4	ADC 1 FIFO	D16 – D19	**4**
DMA5	ADC 2 FIFO	D20 – D23	**5**
DMA8	Delay Memory Read FIFO	D24 – D27	**8**

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5.12 Local DMA Out Address Remap Register

The Local DMA Out Address Remap Register permits remapping each outgoing DMA channel for use with a different outgoing FIFO.

The following table shows the contents of this register.

Table 5–14: Local DMA Out Address Remap Register
R/W @ BAR0+0x00B8

	D31 – D08	D07 – D04	D03 – D00
Bit Name	Reserved	DMA7	DMA6
Function	Write with zeros, Mask when reading	FIFO Codes, see below	
All bits default to the default FIFOs at power on and reset (see Table 5–15, below)			

Each outgoing DMA channel has a four–bit field in this register that maps an outgoing FIFO to that channel. The mapping code for the four bits in each field is as follows, in hex:

0x6 = DAC A FIFO
0x7 = DAC B FIFO
0x9 = Delay Memory Write FIFO
0xD = Test FIFO Write

The default mapping is shown in the following table:

Table 5–15: Default DMA Out Mapping

DMA Channel	FIFO	Register Bits	Code
DMA6	DAC A FIFO	D03 – D00	**6**
DMA7	DAC B FIFO	D07 – D04	**7**

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5.13 DMA Command Register

The DMA Command Register specifies the type of PCI Bus read and write commands used for DMA operations.

The following table shows the contents of this register.

Table 5–16: DMA Command Register
R/W @ BAR0+0x0100

	D31 – D08	D07 – D04	D03 – D00
Bit Name	Reserved	PCI Write Command Code for DMA	PCI Read Command Code for DMA
Function	Write with zeros, Mask when reading	0111	(See below)
All bits default to the state indicated above at power on and reset			

The PCI Write command (bits D07 – D04) is fixed at code '0111', Memory Write.

The PCI Read command (bits D03 – D00) defaults to code '1100', Memory Read Multiple. The following codes are valid for the PCI Read command:

0110 – Memory Read
1100 – Memory Read Multiple
1110 – Memory Read Line

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5.14 DMAx Current Transfer Counter Register

The read–only DMA Current Transfer Counter Register indicates the current status and data transfer count for the applicable DMA channel. There are nine DMA Current Transfer Count registers, one for each DMA channel (0 through 8), which support nine data transfer FIFOs.

The following table shows the contents of this DMA Current Transfer Counter Register. The subsections following the table provide descriptions of the bits in this register.

Table 5–17: DMAx Current Transfer Counter Register

DMA0: R.O. @ BAR0+0x0110
DMA1: R.O. @ BAR0+0x0120
DMA2: R.O. @ BAR0+0x0130
DMA3: R.O. @ BAR0+0x0140
DMA4: R.O. @ BAR0+0x0150
DMA5: R.O. @ BAR0+0x0160
DMA6: R.O. @ BAR0+0x0170
DMA7: R.O. @ BAR0+0x0180
DMA8: R.O. @ BAR0+0x0190

	D31	D30	D29 – D28	D27 – D00
Bit Name	DMA Active	Reserved	Descriptor Pointer	Transfer Count
Function	0 = DMA Active 1 = No DMA	Write 0s, Mask read	Current Descriptor number	Current data transfer count, in words (32–bit or 64–bit, see Section 5.14.3)
When reset, including power–up, the state of this register is unknown.				

In the default configuration, the nine DMA channels are assigned to the following FIFOs (note that the Direction given is from the PMC baseboard):

DMA Channel	FIFO	Direction
DMA0	DDC A FIFO	Incoming
DMA1	DDC B FIFO	Incoming
DMA2	DDC C FIFO	Incoming
DMA3	DDC D FIFO	Incoming
DMA4	ADC 1 FIFO	Incoming
DMA5	ADC 2 FIFO	Incoming
DMA6	DAC A FIFO	Outgoing
DMA7	DAC B FIFO	Outgoing
DMA8	Delay Memory Read FIFO	Incoming

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5.14 DMAx Current Transfer Status Register (continued)

5.14.1 DMA Active Bit D31

This bit indicates the current active status of the applicable DMA channel, depending on the register accessed. When read as logic '0' the DMA channel is active (a data transfer is running). When read as logic '1' the DMA channel is not active.

5.14.2 Descriptor Pointer Bits D29 – D28

These two bits indicate the number of the current Descriptor that is active for the applicable DMA channel, depending on the register accessed. There are four Descriptors for each DMA channel, identified as 0 through 3.

The four Descriptors can programmed for separate DMA transfers using the DMA Command/Status Register, Transfer Interval Counter Register, four Descriptor Transfer Count Registers, and four Descriptor PCI Address Registers (see Sections 5.16 to 5.19).

5.14.3 Transfer Count Bits D27 – D00

This field indicates the current transfer count of the applicable DMA channel, depending on the register accessed. The Transfer Count is a 28–bit binary value, with bit D27 the MSB. Words are either 32 or 64 bits wide, as specified by Data Width, bit D07, in the DMA Command/Status Register, Section 5.16.10.

This register field is loaded with the programmed Transfer Interval Count, Section 5.17.3, at the start of the DMA, and decrements to zero during the transfer.

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5.15 DMAx Current PCI Address Register

The read–only DMA Current PCI Address indicates the current PCI address for the applicable DMA channel. There are nine DMA Current PCI Address registers, one for each DMA channel (0 through 8).

The following table shows the contents of this register.

Table 5–18: DMAx Current PCI Address Register

DMA0: R.O. @ BAR0+0x0118
DMA1: R.O. @ BAR0+0x0128
DMA2: R.O. @ BAR0+0x0138
DMA3: R.O. @ BAR0+0x0148
DMA4: R.O. @ BAR0+0x0158
DMA5: R.O. @ BAR0+0x0168
DMA6: R.O. @ BAR0+0x0178
DMA7: R.O. @ BAR0+0x0188
DMA8: R.O. @ BAR0+0x0198

	D31 – D00
Bit Name	PCI Address
Function	Current PCI Address for DMAx
When reset, including power–up, the state of this register is unknown.	

In the default configuration, the DMA channels are assigned to the following FIFOs:

DMA Channel	FIFO
DMA0	DDC A FIFO
DMA1	DDC B FIFO
DMA2	DDC C FIFO
DMA3	DDC D FIFO
DMA4	ADC 1 FIFO
DMA5	ADC 2 FIFO
DMA6	DAC A FIFO
DMA7	DAC B FIFO
DMA8	Delay Memory Read FIFO

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5.16 DMAx Command/Status Register

The DMA Command/Status Register is used to control DMA operation for the appli–cable DMA channel. There are nine DMA Command/Status Count registers, one for each DMA channel (0 through 8). The bits in this register allow you to set and monitor the operating mode of the DMA channel and the PCI bus data transfer associated with that DMA operation.

The following table shows the contents of the DMA Command/Status Register. The subsections following the table provide descriptions of the bits in this register.

Table 5–19: DMAx Command/Status Register

DMA0: R/W @ BAR0+0x1000
DMA1: R/W @ BAR0+0x2000
DMA2: R/W @ BAR0+0x3000
DMA3: R/W @ BAR0+0x4000
DMA4: R/W @ BAR0+0x5000
DMA5: R/W @ BAR0+0x6000
DMA6: R/W @ BAR0+0x7000
DMA7: R/W @ BAR0+0x8000
DMA8: R/W @ BAR0+0x9000

	D31 – D16							
Bit Name	Maximum Burst Count							
Function	Burst Count, in words							
	D15 ***	**D14**	**D13 ****	**D12 ****	**D11 ****	**D10 ****	**D09 ****	**D08 ****
Bit Name	DAC Buffering	PCI Address	Detected Parity Error Flag	Signaled System Error Flag	Received Master Abort Flag	Received Target Abort Flag	Signaled Target Abort Flag	Data Parity Error Flag
Function	0 = Enable 1 = Disable	0 = Increment 1 = Hold	0 = No Error 1 = Error	0 = No Error 1 = Error	0 = No Abort 1 = Abort	0 = No Abort 1 = Abort	0 = No Abort 1 = Abort	0 = No Parity 1 = Parity
	D07	**D06**	**D05**	**D04 ****	**D03**	**D02**	**D01 ***	**D00**
Bit Name	Data Width	Burst Mode	Demand Mode	DMA Status	DMA Channel Buffer Reset	DMA Abort	DMA Start	DMA Enable
Function	0 = 32 1 = 64	1 = Enable	0 = Disable 1 = Enable	0 = DMA Active 1 = Done	0 = Run 1 = Reset	0 = N/A 1 = Abort DMA	0 = Stop 1 = Start	0 = Disable 1 = Enable

* Bit D01 is Write Only
** These bits are Read Only
*** Bit D15 applies only to DMA Channels 6 and 7 (DMA6 & DMA7).

At power on and reset, bits D31 – D16 default to 0x0020, bit D06 defaults to logic '1', and all other bits default to logic '0'.

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5.16 DMAx Command/Status Register (continued)

5.16.1 Maximum Burst Count — Bits D31 – D16

The burst count is a 16–bit binary value, with bit D31 the MSB. This value specifies the maximum data transfer burst length, in words, for the applicable DMA channel. At power on or reset this value defaults to **0x20**. See Data Width, Section 5.16.10 below, for the word size of each transfer, 32–bit or 64–bit. See Sections 4.6.1 and 4.6.2 for description of Burst Mode operation.

NOTE: When in 32–bit mode, the burst count must be an even value.

5.16.2 DAC Buffering — Bit D15

This bit enables or disables buffering of the data transfer for the applicable DMA channel PCI bus data transfer. When set to logic '0' buffering is enabled to the output device. When set to logic '1' the DMA channel does not buffer the data transfer to this device. Typically, this should be set to '1' to disable buffering.

NOTE: This bit is applicable only to DMA channels 6 and 7 (DAC output).

5.16.3 PCI Address — Bit D14

This bit sets the PCI address to increment or hold for the applicable DMA channel PCI bus data transfer. When set to logic '0' the PCI address increments. When set to logic '1' the DMA address holds and does not increment.

5.16.4 Detected Parity Error Flag — Bit D13

This read–only bit indicates the PCI bus Parity Error status for the applicable DMA channel PCI bus data transfer. When read as logic '0' the DMA channel did not detect a PCI bus parity error. When read as logic '1' the DMA channel detected a PCI bus parity error.

5.16.5 Signaled System Error Flag — Bit D12

This read–only bit indicates the PCI bus SERR pin status for the applicable DMA channel PCI bus data transfer. When read as logic '0' the DMA channel did not detect a PCI bus SERR error. When read as logic '1' the DMA channel detected a PCI bus SERR error.

5.16.6 Received Master Abort Flag — Bit D11

This read–only bit indicates the current Master Abort status for the applicable DMA channel PCI bus data transfer. When read as logic '0' a PCI Bus Master did not terminate the data transfer. When read as logic '1' a PCI Bus Master did terminate the data transfer by a bus Master Abort.

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5.16 DMAx Command/Status Register (continued)

5.16.7 Received Target Abort Flag Bit D10

This read−only bit indicates the current Target Abort status for the applica−ble DMA channel PCI bus data transfer. When read as logic '0' a Target Abort did not terminate the data transfer. When read as logic '1' a Target Abort has terminates the bus master's data transfer.

5.16.8 Signaled Target Abort Flag Bit D09

This read−only bit indicates the current Target Abort status of the Target device for the applicable DMA channel PCI bus data transfer. When read as logic '0' the Target device did not terminate the transaction with a Target Abort. When read as logic '1' the Target device terminated the transaction with a Target Abort.

5.16.9 Data Parity Error Flag Bit D08

This read−only bit indicates the enabled PCI bus PERR pin status for the applicable DMA channel PCI bus data transfer. When read as logic '0' the no PCI bus parity errors have occurred. When read as logic '1' the DMA chan−nel detected a PERR parity error from the bus Master. This error flag can only be set if the Parity Error Response (bit 6 of the bus master's Command Register) is enabled.

5.16.10 Data Width Bit D07

This bit sets the PCI bus data width of the DMA transfer for the applicable DMA channel. When set to logic '0', the PCI bus data width is 32−bits. When set to logic '1', the PCI bus data width is 64−bits.

The setting of this bit affects the Maximum Burst Count, Section 5.16.1. When this bit is cleared to 0, the burst count is the number of 32−bit words; when this bit is set to 1, the burst count is the number of 64−bit words.

5.16.11 Burst Mode Bit D06

This bit sets Burst Mode DMA operation for the applicable DMA channel. When set to logic '1', each data transfer is in multiple bursts, and Maximum Burst Count, Section 5.16.1, specifies the maximum transfer of each burst.

NOTE: This bit cannot be cleared to logic '0'.

See Sections 4.6.1 and 4.6.2 for description of Burst Mode DMA operation.

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5.16 DMAx Command/Status Register (continued)

5.16.12 Demand Mode Bit D05

This bit sets Demand Mode DMA operation for the applicable DMA chan–nel. When set to logic '0', the Demand Mode is not enabled. When set to logic '1', Demand Mode is enabled. See Section 4.6.1 for description of Demand Mode Operation.

5.16.13 DMA Status Bit D04

This read–only bit indicates the current active status for the applicable DMA channel. When read as logic '0' the DMA channel is active (a data transfer is running). When read as logic '1' the DMA channel is not active.

5.16.14 DMA Channel Buffer Reset Bit D03

This bits issues a reset to one of the DMA channel buffers in the PCI7140. This reset flushes any remaining data from the respective buffer in the PCI7140 (this reset does not clear or reset the associated FIFO in the FPGA). When the bit is set to logic '1', the channel is in reset. When the bit is cleared to logic '0' (its default state), the channel is in a normal run state.

5.16.15 DMA Abort Bit D02

This bit aborts DMA operation for the applicable DMA channel. When this bit is set to logic '1', the DMA channel aborts the current transfer. This bit cannot be cleared to logic '0' by the user—the DMA channel logic clears this bit when it aborts the channel.

5.16.16 DMA Start Bit D01

This bit starts DMA operation for the applicable DMA channel. When this bit is set to logic '1', the channel starts transferring data if the channel is enabled.

5.16.17 DMA Enable Bit D00

This bit enables the applicable DMA channel. Writing a logic '1' enables the channel to transfer data. Writing a logic '0' disables the channel from start–ing a DMA transfer, and if in the process of transferring data, suspends the transfer (pause).

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5.17 DMAx Transfer Interval Counter Register

The DMA Transfer Interval Counter Register is used to setup and monitor DMA Count Interrupt operation for the applicable DMA channel. There are nine DMA Transfer Interval Counter registers, one for each DMA channel (0 through 8). The following table shows the contents of the DMA Transfer Interval Counter Register. The subsec–tions following the table provide descriptions of the bits in this register.

Table 5–20: DMAx Transfer Interval Counter Register

DMA0: R/W @ BAR0+0x1008
DMA1: R/W @ BAR0+0x2008
DMA2: R/W @ BAR0+0x3008
DMA3: R/W @ BAR0+0x4008
DMA4: R/W @ BAR0+0x5008
DMA5: R/W @ BAR0+0x6008
DMA6: R/W @ BAR0+0x7008
DMA7: R/W @ BAR0+0x8008
DMA8: R/W @ BAR0+0x9008

	D31	D30 – D28	D27 – D24 *	D23 – D00
Bit Name	Reset	Reserved	Interrupt Counter	Transfer Interval Count
Function	0 =Run 1 =Reset	Write with zeros, Mask when reading	Current Interrupt Count	Transfer Count, in words–1, see Section 5.17.3

* These bits are Read Only
All bits default to the logic '0' state at power on and reset

5.17.1 Reset Bit D31

This bit resets both the Interrupt Counter and the Transfer Interval Counter. When the bit is set to logic '1', the counters are in reset (reset does not clear this register). When the bit is cleared to logic '0' (its default state), the coun–ters are released for counting (run state).

5.17.2 Interrupt Counter Bits D27 – D24

The Interrupt Counter is a 4–bit read–only binary value, with bit D27 the MSB. This value indicates the current count of the number of DMA Count interrupts that has been generated.

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5.17 DMAx Transfer Interval Counter Registers (continued)

5.17.3 Transfer Interval Count Bits D23 – D00

Transfer Interval Count is a 24–bit binary value, with bit D23 the MSB. This value specifies the count that will generate a DMA Transfer Interval Count Finish interrupt to the PCI Interrupt Flag Register, Section 5.2.

This transfer count is calculated as the desired number of data words (which must be a power of 2) minus one. Data words are either 32 or 64 bits wide, as specified by Data Width, bit D07, in the DMA Command/Status Register, Section 5.16.10. The valid transfer interval count values are:

Table 5–21: Valid Transfer Interval Count Values

Data Word Count	Transfer Interval Count	Bits D23 – D00
4 words	3	**0x3**
8 words	7	**0x7**
16 words	15	**0xF**
32 words	31	**0x1F**
64 words	63	**0x3F**
128 words	127	**0x7F**
256 words	255	**0xFF**
512 words	511	**0x1FF**
1,024 words	1023	**0x3FF**
2,048 words	2047	**0x7FF**
4,096 words	4095	**0xFFF**
8,192 words	8191	**0x1FFF**
16,384 words	16383	**0x3FFF**
32,768 words	32767	**0x7FFF**
65,536 words	65535	**0xFFFF**
131,072 words	131071	**0x1 FFFF**
262,144 words	262143	**0x3 FFFF**
524,288 words	524287	**0x7 FFFF**
1,048,576 words	1048575	**0xF FFFF**
2,097,152 words	2097151	**0x1F FFFF**
4,194,304 words	4194303	**0x3F FFFF**
8, 388,608 words	8,388,607	**0x7F FFFF**
16,777,216 words	16,777,215	**0xFF FFFF**

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5.18 DMAx Descriptor Transfer Count Registers

The DMA Descriptor Transfer Count Registers are used to setup the DMA operation Descriptors of the applicable DMA channel. There are nine DMA channels, DMA (0 through 8), and four Descriptors for each DMA channel, for a total of 36 DMA Descriptor Transfer Count Registers. Each of these registers has an associated DMA Descriptor PCI Address Register, Section 5.19, that must be programmed at the same time.

The following table shows the contents of the DMA Transfer Count Register. The subsections following the table provide descriptions of the bits in this register.

Table 5–22: DMAx Descriptor Transfer Count Registers

	Descriptor 0	Descriptor 1	Descriptor 2	Descriptor 3
DMA0: R/W @	BAR0+0x1010	BAR0+0x1020	BAR0+0x1030	BAR0+0x1040
DMA1: R/W @	BAR0+0x2010	BAR0+0x2020	BAR0+0x2030	BAR0+0x2040
DMA2: R/W @	BAR0+0x3010	BAR0+0x3020	BAR0+0x3030	BAR0+0x3040
DMA3: R/W @	BAR0+0x4010	BAR0+0x4020	BAR0+0x4030	BAR0+0x4040
DMA4: R/W @	BAR0+0x5010	BAR0+0x5020	BAR0+0x5030	BAR0+0x5040
DMA5: R/W @	BAR0+0x6010	BAR0+0x6020	BAR0+0x6030	BAR0+0x6040
DMA6: R/W @	BAR0+0x7010	BAR0+0x7020	BAR0+0x7030	BAR0+0x7040
DMA7: R/W @	BAR0+0x8010	BAR0+0x8020	BAR0+0x8030	BAR0+0x8040
DMA8: R/W @	BAR0+0x9010	BAR0+0x9020	BAR0+0x9030	BAR0+0x9040

	D31	D30	D29– D28	D27 – D00
Bit Name	Chain	Interrupt	Reserved	Transfer Count
Function	0 = End 1 = Next	0 = Disable 1 = Enable	Write with zeros, Mask when reading	Transfer Count, In Bytes (see Section 5.18.3 for bits D02 – D00)

All bits default to the logic '0' state at power on and reset

5.18.1 Chain Bit D31

This bit enables the next Descriptor in the chain for the applicable DMA channel, depending on the register accessed. When you clear this bit to logic '0' (its default state), the descriptor chain ends at this Descriptor. Set the bit to logic '1' to continue (link) the data transfer to the next Descriptor.

When you set this bit to '1' for Descriptor 3, the data transfer continues, restarting at Descriptor 0, for a continuous transfer. A continuous transfer can only be stopped using the DMA Abort bit, Section 5.16.15, for this DMA channel.

NOTE: If you setup a DMA channel for a continuous data transfer (Chain bit D31 = 1 in all four Descriptors), you must ensure that the gating signal used for the transfer is not stopped before you stop the transfer or the channel may hang up.

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5.18 DMAx Descriptor Transfer Count Register (continued)

5.18.2 Interrupt — Bit D30

This bit enables an end of chain interrupt for the applicable DMA channel. When set to logic '0', the end of chain interrupt is not enabled. When set to logic '1', an end of chain interrupt is enabled.

When enabled, at the end of the last descriptor transfer count specified for this channel a DMA Chain Finish interrupt will be asserted to the PCI Interrupt Flag Register, Section 5.2. You must enable the applicable DMA Chain Finish bit in the PCI Interrupt Enable Register, Section 5.3, to route this interrupt to the PCI or Local bus.

5.18.3 Transfer Count — Bits D27 – D00

The Transfer Count is a 28–bit binary value, with bit D27 the MSB. This value indicates the data transfer count, in bytes, for this Descriptor.

The Transfer Count must be an even number of bytes for the word size specified, 32–bit or 64–bit. Thus, if 32–bit transfers are specified, Transfer Count bits D01 and D00 must be '0'; if 64–bit transfers are specified, bits D02, D01, and D00 must be '0'. See Data Width, Section 5.16.10, for the word size.

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5.19 DMAx Descriptor PCI Address Registers

The DMA Descriptor PCI Address Registers are used to setup the DMA operation Descriptors of the applicable DMA channel. There are nine DMA channels, DMA (0 through 8), and four Descriptors for each DMA channel, for a total of 36 DMA Descrip–tor PCI Address Registers. Each of these registers has an associated DMA Descriptor Transfer Count Register, Section 5.18, that must be programmed at the same time.

The following table shows the contents of the DMA Descriptor PCI Address Register. The paragraphs following the table provide descriptions of the bits in this register.

Table 5–23: DMAx Descriptor PCI Address Registers

	Descriptor 0	Descriptor 1	Descriptor 2	Descriptor 3
DMA0: R/W @	BAR0+0x1018	BAR0+0x1028	BAR0+0x1038	BAR0+0x1048
DMA1: R/W @	BAR0+0x2018	BAR0+0x2028	BAR0+0x2038	BAR0+0x2048
DMA2: R/W @	BAR0+0x3018	BAR0+0x3028	BAR0+0x3038	BAR0+0x3048
DMA3: R/W @	BAR0+0x4018	BAR0+0x4028	BAR0+0x4038	BAR0+0x4048
DMA4: R/W @	BAR0+0x5018	BAR0+0x5028	BAR0+0x5038	BAR0+0x5048
DMA5: R/W @	BAR0+0x6018	BAR0+0x6028	BAR0+0x6038	BAR0+0x6048
DMA6: R/W @	BAR0+0x7018	BAR0+0x7028	BAR0+0x7038	BAR0+0x7048
DMA7: R/W @	BAR0+0x8018	BAR0+0x8028	BAR0+0x8038	BAR0+0x8048
DMA8: R/W @	BAR0+0x9018	BAR0+0x9028	BAR0+0x9038	BAR0+0x9048

	D31 – D00
Bit Name	PCI Address
Function	Source/Destination PCI Address
All bits default to the logic '0' state at power on and reset	

The PCI Address specifies the source or destination PCI bus address (depending on the associated FIFO's direction) for the data transfer. The PCI address is a 32–bit address.

NOTE: Each DMA channel has four possible Descriptors that can be linked to provide a continuous data transfer. There are two registers for each Descriptor, the DMA Descriptor PCI Address Register, above, and the DMA Descriptor Transfer Count Register, Section 5.18.

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Chapter 6: FPGA Registers

6.1 Overview

The XC2VP50 Virtex–II Pro FPGA is connected to the PMC baseboard through the Pentek PCI7140. Through this PCI interface, any processor on the PMC baseboard can receive data from either AD6645, or from any of the four receiver channels from the GC4016. In addition, any processor on the PMC baseboard can send data to the DAC5686 for two channels of output. Any PCI Bus Master can control all programmable features on the board, the two AD6645s, the GC4016, the DAC5686, and all FPGA memory map registers.

This chapter describes the FPGA registers accessible from a PMC baseboard processor. All descriptions are given from the baseboard processor's viewpoint. All FPGA registers are 16 bits wide, however since the PCI local bus is a 64–bit data path, the register addresses are in increments of 64 bits (8 bytes). Refer to Section 3.3.2 for the memory map of all FPGA registers in the Model 7140.

The following is a simplified block diagram of the 7140 FPGA interfaces, indicating the location of the FPGA internal registers. (See Section 6.17.1, Figure 6–3 on page 190 for illustration of the FPGA 'Switching and Routing' between the FIFOs and the A/Ds, DDC, DAC, and Delay memory. See Figure 5–1 for a simplified block diagram of the PCI7140 interfaces.)

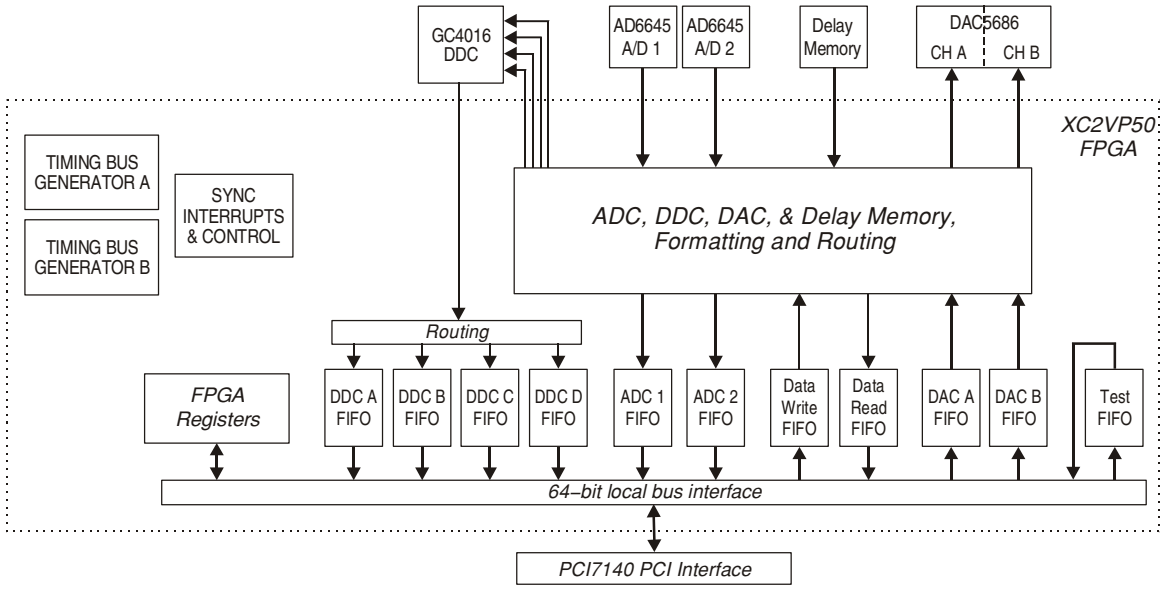


Figure 6–1: FPGA Interface Diagram

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6.2 ID Readout Register

The ID Readout Register is a read–only register that provides the Model 7140 PMC board identification. When read, it always returns a value of **0x7140**.

Table 6–1: ID Readout Register
R.O. @ BAR2+0x8000

	D15 – D12	D11 – D08	D07 – D04	D03 – D00
Bit Name	Board Identification			
Function	0 1 1 1	0 0 0 1	0 1 0 0	0 0 0 0

6.3 FPGA Data In/Data Out Registers

The FPGA Data In/Data Out registers allow reading from or writing to the VMEbus using FPGA spare pins. Standard PMC–VME baseboards route these I/O signals from the FPGA through PMC **P14** connector directly to the VMEbus backplane **P2** connector. This capability is provided only with Option 104 (see Section 2.3.2).

The following table shows the contents of these registers.

Table 6–2: FPGA Data In/Data Out Registers
Data In: R.O. @ BAR2+0x8008
Data Out: R/W @ BAR2+0x8010

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Bit Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	0 = '0' 1 = '1'															
All bits default to the logic '0' state at power on and reset																

Bits D0 through D15 correspond to the LVDS input and output signals described for Option 104 in Section 2.3.2. The LVDS_OUT signals shown in Table 2–1 are from the FPGA Data Out Register, with LVDS_OUT_x0 from bit D0 and LVDS_OUT_x15 from bit D15. The LVDS_IN signals are for the FPGA Data In Register, with LVDS_IN_x0 from bit D0 and LVDS_IN_x15 from bit D15.

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6.4 TWSI Port Register

The TWSI Port Register allows you to program the voltage/temperature sensor thresholds over the board's serial TWSI (Two–Wire Serial Interface) bus.

The board's voltage/temperature sensors provide constant monitoring of critical voltages and temperatures on the PCB. When an over–temperature or over–voltage condition is indicated, the red **TMP** LED is illuminated on the front panel, and an over–temperature/voltage interrupt is available to a baseboard processor (see Table 6–23).

The following table shows this register's bit layout. The paragraphs following this table describe these bits.

Table 6–3: TWSI Port Register
R/W @ BAR2+0x8018

	D15 – D03	D02	D01	D00
Bit Name	Reserved	SER DIR	SER CLK	SER DAT
Function	Write with zeros, Mask when reading	0 = Write 1 = Read	Serial Clock	Serial Data
All bits default to the logic '0' state at power on and reset				

The TWSI Port Register contains three bits: one bit sets the read/write direction of the register (SER DIR) and the other two provide the serial clock (SER CLK) and data (SER DATA) to/from the serial TWSI bus.

NOTE: You must set up the TWSI bus devices following power on of the Model 7140. The following paragraphs describe the setup of these devices. Routines for programming these devices are provided in the ReadyFlow board support software for the Model 7140 (Pentek part #801.71400).

The devices on the TWSI bus include an Analog Devices ADM1024 Hardware Monitor and a National Semiconductor LM83 Temperature Sensor. You can program these devices from the Temperature/Voltage Sense Register, using internal registers in each device, as described in the following paragraphs.

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6.4 TWSI Port Register (continued)

Each device on the TWSI bus has a separate bus address, as listed in the following table. The bus address is sent first, as serial data.

Table 6–4: TWSI Bus Addresses

Device	Write Address	Read Address
LM83 Temperature Sensor	**0x30**	**0x31**
ADM1024 Hardware Monitor	**0x58**	**0x59**

The TWSI bus addresses consist of the 7–bit serial bus address of the device in the first seven most significant bits, plus the least significant bit = 0/1 for write/read.

6.4.1 LM83 Temperature Sensor

There are several temperature sensors in the LM83 that can be programmed on the serial TWSI bus, using LM83 internal registers (refer to the LM83 data sheet, see Section 1.16, for description of these registers).

The following table lists the programmable sensors on the LM83:

Table 6–5: LM83 Programmable Sensors

Monitored Condition	LM83 Input	ReadyFlow Limits *
PCI7140 Temperature	D1	60° C
FPGA Temperature	D2	70° C
PCB Temperature	D3	60° C
LM83 Local	(internal)	50° C

* These limits are programmed if you run the Pentek ReadyFlow 7140 Hardware Monitor routines for the LM83 using the default values.

A red front panel LED labeled **TEMP** (Section 2.7.5) is illuminated by the LM83 during an over–temperature condition—when any of the four inputs exceeds the HIGH setpoint limit.

A separate over–temperature interrupt signal is provided from the LM83 to the Interrupt Status Register, Section 6.11.3, based on over–temperature of the four programmed limits.

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6.4 TWSI Port Register (continued)

6.4.2 ADM1024 Hardware Monitor

The board uses several voltage sensor inputs in the ADM1024 that can be programmed on the serial TWSI bus, using ADM1024 internal registers (refer to the ADM1024 data sheet, see Section 1.16, for description of the registers associated with these inputs).

The following table lists the programmable voltage sensors on the ADM1024:

Table 6–6: ADM1024 Programmable Sensors

Monitored Condition	ADM1024 Input	ReadyFlow Limits *
+5 Volt supply	+5 VIN	+5 Volts, ±10%
+12 Volt supply	+12 VIN	+12 Volts, ±10%
+3.3 Volt supply	VCC	+3.3 Volts, ±10%
+1.5 Volt supply A	+VCCP1	+1.5 Volts, ±10%
+1.25 Volt supply	AIN1	+1.25 Volt, ±10%
+2.5 Volt RapidIO supply	AIN2	+2.5 Volt, ±10%
+2.5 Volt supply	+2.5 VIN	+2.5 Volt, ±10%
+1.8 Volt supply	VCCP2	+1.8 Volt, ±10%

* These limits are programmed if you run the Pentek ReadyFlow 7140 Hardware Monitor routines for the ADM1024 using the default values.

An interrupt indicating voltage out of limit is also provided from the ADM1024 to the Interrupt Status Register, Section 6.11.3.

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6.5 DCM Control Register

The DCM Control Register controls each Digital Clock Manager (DCM) on the FPGA. The following table shows the contents of the DCM Register. The subsections following the table provide descriptions of each control bit in this register.

Table 6–7: DCM Control Register
R/W @ BAR2+0x8020

	D15	D14	D13	D12	D11 *	D10	D09	D08 *
Bit Name	Reserved				LOCKD D	DCM RST D	CLK SEL D	LOCKD C
Function	Write with zeros, Mask when reading				0 =Not locked 1 =Locked	0 =Run 1 =Reset	0 =Input clock 1 =DCM	0 =Not locked 1 =Locked
	D07	**D06**	**D05 ***	**D04**	**D03**	**D02 ***	**D01**	**D00**
Bit Name	DCM RST C	CLK SEL C	LOCKD B	DCM RST B	CLK SEL B	LOCKD A	DCM RST A	CLK SEL A
Function	0 =Run 1 =Reset	0 =Input clock 1 =DCM	0 =Not locked 1 =Locked	0 =Run 1 =Reset	0 =Input clock 1 =DCM	0 =Not locked 1 =Locked	0 =Run 1 =Reset	0 =Input clock 1 =DCM

* These bits are Read Only
All bits default to the logic '0' state at power on and reset

6.5.1 LOCKD D/C/B/A

Bits D11, D08, D05, D02

Each of these read–only bits indicates the locked status of a DCM clock. When read as logic '0' the DCM clock output is not locked. When read as logic '1' the DCM clock output is locked.

6.5.2 DCM RST D/C/B/A

Bits D10, D07, D04, D01

Each of these bits resets a DCM clock. Set the bit to logic '1' to reset the DCM clock. Clear the bit to logic '0' (its default state) to return the A/D DCM clock to normal operation.

6.5.3 CLK SEL D/C/B/A

Bits D09, D06, D03, D00

Each of these bits selects a DCM clock. Clear the bit to logic '0' (its default state), the input clock is the clock source and the DCM is bypassed. Set the bit to logic '1', the DCM is the clock source (use only above 24 MHz)

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6.6 Miscellaneous Control Register

The Miscellaneous Control Register sets the Endian byte swap mode of the board and controls test pattern generation for the ADC data.

The following table shows the contents of this register. The subsections following the table provide descriptions of each control bit in this register.

Table 6–8: Miscellaneous Control Register
R/W @ BAR2+0x8028

	D15 – D03	D02	D01	D00
Bit Name	Reserved	ENDIANNESS	TEST RAMP	Reserved
Function	Write with zeros, Mask when reading	0 = Little Endian 1 = Big Endian	0 = Disable 1 = Enable	Write 0, Mask read
All bits default to the logic '0' state at power on and reset				

6.6.1 ENDIANNESS Bit D02

This bit configures all FIFO transfers across the PCI bus to operate in big or little endian mode. When the bit is cleared to logic '0' (its default state), the FIFO transfers are in little Endian mode. When this bit is set to logic '1', the FIFO transfers are in big Endian mode and the eight bytes of each FIFO 64–bit word are reversed in order.

6.6.2 TEST RAMP Bit D01

This bit enables or disables test pattern generation for ADC data. When this bit is cleared to logic '0' (its default state), the test pattern is disabled and the AD6645 outputs are used. When this bit is set to logic '1', the test pattern replaces the AD6645 data.

The test pattern is a repetitive, incrementing digital signal that can be used for ADC data instead of the AD6645 outputs. When TEST RAMP is enabled, the output of each AD6645 to the ADC FIFOs and Delay Memory is replaced by this test pattern. The test pattern signal can be controlled by the Trigger/Gate and Formatting functions applicable to the ADC FIFOs and data routing formats.

TEST RAMP does not affect the routing of AD6645 data to the DDC channels.

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6.7 Flash Page Register

A 16–MByte bank of FLASH memory (8 M by 16 bits wide) is available to the FPGA. FLASH memory provides nonvolatile storage for the PowerPC core in the FPGA.

The user can access this FLASH memory at memory address offset **0x0000** – **0x7fff**, using PCI Base Address Register 2 (**BAR2**). This address range accesses only one page of FLASH at a time. There are 2048 pages in FLASH memory. The Flash Page Register selects the page of FLASH memory to be addressed at this address range.

The following table shows the contents of the Flash Page Register. The paragraphs following the table provide description of this register.

Table 6–9: Flash Page Register
R/W @ BAR2+0x8030

	D15 – D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Bit Name	Reserved	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14
Function	Write 0s, Mask read	Flash Memory Page										
All bits default to the logic '0' state at power on and reset												

The Flash Memory Page is an 11–bit binary value, with D10 the most significant bit. This value specifies the page to access, from 0 to 2047. You can read/write from/to this page of FLASH memory at memory address offset **0x0000** – **0x7fff**, using PCI Base Address Register 2 (**BAR2**).

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6.8 FPGA Revision Registers

The two FPGA Revision Registers identify the Pentek version number and the date of the FPGA code currently installed in the XC2VP50 FPGA on this board.

The following tables show the contents of these two registers. The paragraphs below FPGA Revision Register describe the contents of these registers.

Table 6–10: FPGA Revision Register 1
R.O. @ BAR2+0x8038

	D15 – D12	D11 – D08	D07 – D04	D03 – D00
Bit Name	YEAR		MONTH	
Function	3rd Digit of Year	4th Digit of Year	1st Digit of Month	2nd Digit of Month

Table 6–11: FPGA Revision Register 2
R.O. @ BAR2+0x8040

	D15 – D12	D11 – D08	D07 – D04	D03 – D00
Bit Name	DAY		FPGA CODE REVISION	
Function	1st Digit of Day	2nd Digit of Day	FPGA Pentek Code Revision Number	

The FPGA code revision date is coded as six hexadecimal characters in the two registers as follows:

Year: FPGA Revision Register 1, bits D15 – D12, 3rd digit of Year
FPGA Revision Register 1, bits D11 – D08, 4th digit of Year

Month: FPGA Revision Register 1, bits D07 – D04, 1st digit of Month
FPGA Revision Register 1, bits D03 – D00, 2nd digit of Month

Day: FPGA Revision Register 2, bits D15 – D12, 1st digit of Day
FPGA Revision Register 2, bits D11 – D08, 2nd digit of Day

The FPGA Code Revision number (FPGA Revision Register 2, bits D07 – D00) is a binary value, starting at revision 0.

For example, the date of **August 9, 2007** (8/9/07), with a code revision of '**G**', would appear as follows in the two registers.

FPGA Revision Register 1 = **0x0708**
FPGA Revision Register 2 = **0x0907**

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6.9 Core Option Register

The read–only Core Option Register identifies the Pentek Option number of the FPGA IP Core programmed in the XC2VP50 FPGA.

The following table shows the contents of this register. The paragraphs below describe the contents of this register.

Table 6–12: Core Option Register
R.O. @ BAR2+0x8048

	D15 – D12	D11 – D08	D07 – D04	D03 – D00
Bit Name	D15 – D12	D11 – D8	D7 – D4	D3 – D0
Function	4th digit of Option Number	3rd digit of Option Number	2nd digit of Option Number	1st digit of Option Number
All bits default to the number of the installed Core at power on and reset				

The Option Number is coded as four hexadecimal characters as follows:

Bits D15 – D12, 4th digit of Option Number
Bits D11 – D08, 3rd digit of Option Number
Bits D07 – D04, 2nd digit of Option Number
Bits D03 – D00, 1st digit of Option Number

For example, Option 430 would appear as follows in this register: **0x0430**. If no Pentek FPGA IP Core is provided with the board, this register will read **0x0000**.

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6.10 Sync Bus Registers

The following subsections describe the FPGA registers that control Sync Buses A and B. Refer to Section 4.8, Timing and Synchronization, for additional information about the sync, gate, and clock signals. The following diagram illustrates the Sync Bus logic.

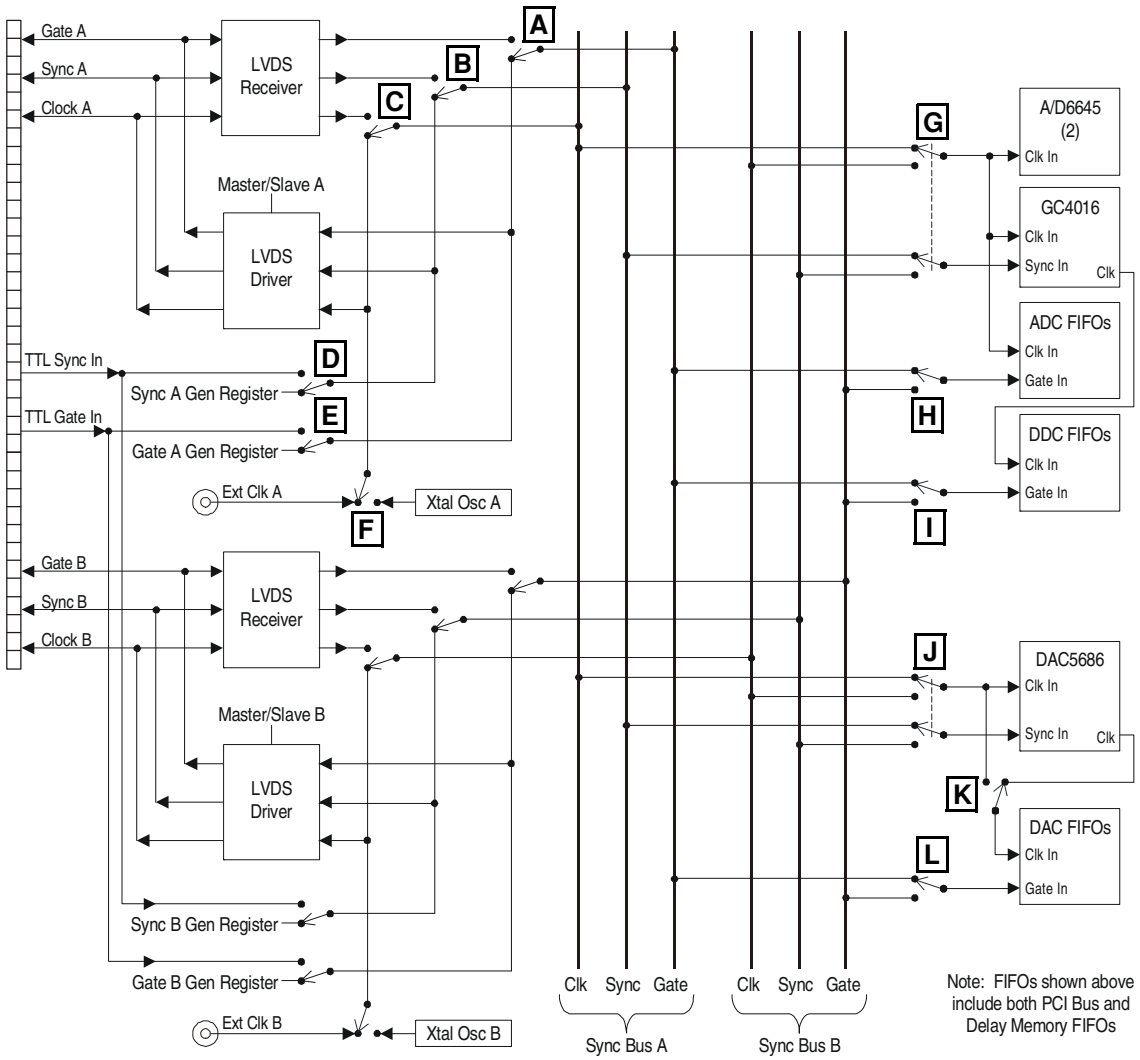


Figure 6–2: Gate/Sync/Clock Logic Diagram

Switches:
A – Master Bus Control Register, Section 6.10.1, bit D09, GATE SRC
B – Master Bus Control Register, Section 6.10.1, bit D06, SYNC SRC
C – Master Bus Control Register, Section 6.10.1, bit D04, CLK SRC
D – Master Bus Control Register, Section 6.10.1, bit D08, SEL GATE
E – Master Bus Control Register, Section 6.10.1, bit D05, SEL SYNC
F – Master Bus Control Register, Section 6.10.1, bit D02, SEL CLK
G – A/D Sync Bus Select Register, Section 6.10.9, bit D00, SEL
H – ADC FIFO Control Register, Section 6.12.1, bit D07, GATE SEL
I – DDC FIFO Control Register, Section 6.13.1, bit D07, GATE SEL
J– D/A Sync Bus Select Register, Section 6.10.8, bit D00, SEL
K – DAC Control/Status Register, Section 6.15.8, bit D03, DAC CLK
L – DAC FIFO Control Register, Section 6.15.1, bit D07, GATE SEL
(Only Sync Bus A references illustrated – See Section 6.10.4 for Sync Bus B control bits)

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6.10 Sync Bus Registers (continued)

6.10.1 Master Bus A Control Register

The Master Bus A Control Register allows you to configure the Model 7140 Sync Bus A as a Master or Slave on the LVDS Sync Bus, toggle the onboard sync bus termination, select the source of the clock, select the source and polarity of the sync, and enable the onboard oscillator.

The following table shows the contents of the Master Control Register. The subsections following the table provide descriptions of each control bit in this register.

Table 6–13: Master Bus A Control Register
R/W @ BAR2+0x8080

	D15 – D11	D10	D09	D08
Bit Name	Reserved	GATE POL	GATE SRC	SEL GATE
Function	Write with zeros, Mask when reading	0 = Negative 1 = Positive	0 = Use SEL GATE (D08) 1= LVDS Bus	0 = Register 1 = Ext TTL Gate

	D07	D06	D05	D04	D03	D02	D01	D00
Bit Name	SYNC POL	SYNC SRC	SEL SYNC	CLK SRC	OSC DSBL	SEL CLK	TERM	MASTR
Function	0 = Negative 1 = Positive	0 = Use SEL SYNC (D05) 1= LVDS Bus	0 = Register 1 = Ext TTL Sync	0 = Use SEL CLK (D02) 1= LVDS Bus	0 = Enable 1 = Disable	0 = Oscillator 1 = Ext Clock	0 = None 1 = Terminated	0 = Slave 1 = Master

All bits default to the logic '0' state at power on and reset

6.10.1.1 GATE POL Bit D10

This bit selects the polarity of the External TTL GATE input selected for sync bus A (see GATE SRC, below). When the bit is cleared to logic '0' (its default state), a negative input enables FIFO input in Gate mode or triggers on a negative–going edge in Trigger mode. When the bit is set to logic '1', a positive input enables FIFO inputs in Gate mode or triggers on a positive–going edge in Trigger mode.

Polarity does not apply to the LVDS Gate/Trigger input nor to a gate generated by the onboard register (Section 6.10.3).

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6.10 Sync Bus Registers (continued)

6.10.1 Master Bus A Control Register (continued)

6.10.1.2 GATE SRC Bit D09

This bit selects the source of the sync bus A GATE signal from either the LVDS Sync Bus or an on−board sync signal. When this bit is cleared to logic '0' (its default state), the gate is selected by SEL GATE, bit D08. When the bit is set to logic '1', the LVDS Sync Bus (SYNC/GATE connector, Section 2.6.4) is the source.

6.10.1.3 SEL GATE Bit D08

When Sync Bus A on this 7140 is the Sync Bus Master (MASTR bit D00 = 1) or when the LVDS Sync Bus' gate input is not used (GATE SRC bit D09 = 0), this bit selects the gate signal for sync bus A from either a register or the external TTL SYNC input. When this bit is cleared to logic '0' (its default state), the Gate A Generator Register, Section 6.10.3, is the source of the gate. When the bit is set to logic '1', the external TTL gate input (SYNC/ GATE connector, Section 2.6.4) is the source of the gate.

6.10.1.4 SYNC POL Bit D07

This bit selects the polarity of the External TTL SYNC input selected for sync bus A (see SYNC SRC, below) for resetting the GC4016 DDC. Polarity does not apply to the LVDS Sync input nor to a gate generated by the onboard register (Section 6.10.2). When this bit is cleared to logic '0' (its default state), a negative sync resets the GC4016. When the bit is set to logic '1', a positive sync resets the GC4016.

6.10.1.5 SYNC SRC Bit D06

This bit selects the source of the sync bus A SYNC signal from either the LVDS Sync Bus or an on−board sync signal. When this bit is cleared to logic '0' (its default state), the sync is selected by SEL SYNC bit D05. When the bit is set to logic '1', the LVDS Sync Bus (SYNC/GATE connector, Section 2.6.4) is the source.

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6.10 Sync Bus Registers (continued)

6.10.1 Master Bus A Control Register (continued)

6.10.1.6 SEL SYNC Bit D05

When Sync Bus A on this 7140 is the Sync Bus Master (MASTR bit D00 = 1) or when the LVDS Sync Bus' sync input is not used (SYNC SRC bit D06 = 0), this bit selects the sync bus A sync signal from either a register or the external TTL SYNC input. When this bit is cleared to logic '0' (its default state), the Sync A Generator Register, Section 6.10.2, is the source of the sync. When the bit is set to logic '1', the external TTL sync input (SYNC/GATE connectors, Section 2.6.4) is the source of the sync.

6.10.1.7 CLK SRC Bit D04

This bit selects the source of the sync bus A clock from either the LVDS Sync Bus or an onboard clock source. When the bit is cleared to logic '0' (its default state), the LVDS Sync Bus is bypassed and the clock is selected by SEL CLK bit D02, below. When this bit is set to logic '1', the EXT LVDS CLK A input (SYNC/GATE connector, Section 2.6.4) is the source of the clock.

6.10.1.8 OSC DSBL Bit D03

This bit enables or disables the output from the onboard crystal oscillator A. When the bit is cleared to logic '0' (its default state), the onboard oscillator (Oscillator A) is enabled. When this bit is set to logic '1', the onboard oscillator is disabled. When using the external MMCX clock input (SEL CLK bit D02 = 1, below), you must disable the oscillator.

6.10.1.9 SEL CLK Bit D02

When Sync Bus A on this 7140 is the Sync Bus Master (MASTR bit D00 = 1) or when the LVDS Sync Bus clock input is not used (CLK SRC bit D04 = 0), this bit selects the sync bus A clock signal from either the onboard oscillator or the external clock input. When this bit is cleared to logic '0' (its default state), the onboard oscillator is selected (for this setting, OSC DSBL bit D03, above, must be cleared to logic '0' to enable the oscillator). When the bit is set to logic '1', the external clock input is used (MMCX CLK A connector, Section 2.6.3).

NOTE: When you select the external clock, you must provide a delay of 50 mS or more for "device settling" time. ReadyFlow high–level functions already include this delay but low–level macros do not.

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6.10 Sync Bus Registers (continued)

6.10.1 Master Bus A Control Register (continued)

6.10.1.10 TERM Bit D01

This bit enables termination of LVDS Sync Bus A by a Slave, or by a Master if it is the only unit on the bus. When the bit is cleared to logic '0' (its default state), the sync bus is not terminated. When the bit is set to logic '1', the bus is terminated. The sync bus must be terminated when this Model 7140 is the last (or only) Slave on the bus, or if it is a Master or the only unit on the bus.

6.10.1.11 MASTR Bit D00

This bit sets this Model 7140 as either Master or Slave on LVDS Sync Bus A. When the bit is cleared to logic '0' (its default state), this 7140 is a Slave. When bit is set to logic '1', this 7140 is the Sync Bus A Master. When only one 7140 is used it must be set as a Master.

When set as a Sync Bus Master, this Model 7140 Sync Bus A is the source of the sync, clock, and gate signals output to the LVDS Sync Bus. You must select these sources using control bits SYNC SRC (bits D05, D06), CK SRC (bit D04), and GATE SRC (bits D09, D08), and if needed, generate the sync and/or gate signals using the Gate A Generator Register (Section 6.10.3) and Sync A Generator Register (Section 6.10.2).

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6.10 Sync Bus Registers (continued)

6.10.2 Sync A Generator Register

The Sync A Generator Register is used on a 7140 that is configured as a Sync Bus Master (MASTR = 1, Master Bus A Control Register, Section 6.10.1.11), or on a 7140 that is not connected to an external LVDS Sync Bus.

The following table shows the contents of the Sync Generator Register.

Table 6–14: Sync A Generator Register
R/W @ BAR2+0x8088

	D15 – D01	D00
Bit Name	Reserved	$\overline{\text{SYNC}}$
Function	Write with zeros, Mask when reading	0 = Reset 1 = Release
Bit D00 defaults to the logic '1' state at power on and reset		

If the sync source is set to the onboard register (SYNC SRC= 00, Master Bus A Control Register, Section 6.10.1.5), the $\overline{\text{SYNC}}$ bit in this register creates the sync signal (SYNC A) for the board, and for output to the LVDS Sync Bus (SYNC/GATE connector, Section 2.6.4) for a Sync Bus Master.

The Sync A signal can be enabled and routed to different devices on the board using the Sync Mask Register, Section 6.10.7, D/A Sync Bus Select Register, Section 6.10.8, and the A/D Sync Bus Select Register, Section 6.10.9.

When the bit is cleared to logic '0', the device is in reset. When the bit is set to logic '1' (its default state), the device is released for normal operation.

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6.10 Sync Bus Registers (continued)

6.10.3 Gate A Generator Register

The Gate A Generator Register is used on a 7140 that is configured as a Sync Bus Master (MASTR = 1, Master Bus A Control Register, Section 6.10.1.11), or on a 7140 that is not connected to an external LVDS Sync Bus.

The following table shows the contents of the Gate Generator Register.

Table 6–15: Gate A Generator Register
R/W @ BAR2+0x8090

	D15 – D01	D00
Bit Name	Reserved	$\overline{\text{GATE}}$
Function	Write with zeros, Mask when reading	0 = Enable 1 = Disable
Bit D00 defaults to the logic '1' state at power on and reset		

If the gate source is set to the onboard register (GATE SRC= 00, Master Bus A Control Register, Section 6.10.1.2), the $\overline{\text{GATE}}$ bit in this register creates the gate signal (Gate A) for FIFO writing control, and for output to the LVDS Sync Bus (SYNC/GATE connector, Section 2.6.4) for a Sync Bus Master.

When the bit is cleared to logic '0', FIFO writes are enabled. When the bit is set to logic '1' (its default state), FIFO writes are disabled.

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6.10 Sync Bus Registers (continued)

6.10.4 Master Bus B Control Register

The Master Bus B Control Register allows you to configure the Model 7140 sync bus B as a Master or Slave on the LVDS Sync Bus, toggle the onboard sync bus termination, select the source of the clock, select the source and polarity of the sync, and enable the onboard oscillator.

The following table shows the contents of the Master Control Register. The subsections following the table provide descriptions of each control bit in this register.

Table 6–16: Master Bus B Control Register
R/W @ BAR2+0x8098

	D15 – D11	D10	D09	D08
Bit Name	Reserved	GATE POL	GATE SRC	SEL GATE
Function	Write with zeros, Mask when reading	0 = Negative 1 = Positive	0 = Use SEL GATE (D08) 1= LVDS Bus	0 = Register 1 = Ext TTL Gate

	D07	D06	D05	D04	D03	D02	D01	D00
Bit Name	SYNC POL	SYNC SRC	SEL SYNC	CLK SRC	OSC DSBL	SEL CLK	TERM	MASTR
Function	0 = Negative 1 = Positive	0 = Use SEL SYNC (D05) 1= LVDS Bus	0 = Register 1 = Ext TTL Sync	0 = Use SEL CLK (D02) 1= LVDS Bus	0 = Enable 1 = Disable	0 = Oscillator 1 = Ext Clock	0 = None 1 = Terminated	0 = Slave 1 = Master

All bits default to the logic '0' state at power on and reset

6.10.4.1 GATE POL Bit D10

This bit selects the polarity of the External TTL GATE input selected for sync bus B (see GATE SRC, below). When the bit is cleared to logic '0' (its default state), a negative input enables FIFO input in Gate mode or triggers on a negative–going edge in Trigger mode. When the bit is set to logic '1', a positive input enables FIFO inputs in Gate mode or triggers on a positive–going edge in Trigger mode.

Polarity does not apply to the LVDS Gate/Trigger input nor to a gate generated by the onboard register (Section 6.10.6).

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6.10 Sync Bus Registers (continued)

6.10.4 Master Bus B Control Register (continued)

6.10.4.2 GATE SRC Bit D09

This bit selects the source of the sync bus B GATE signal from either the LVDS Sync Bus or an on−board sync signal. When this bit is cleared to logic '0' (its default state), the gate is selected by SEL GATE, bit D08. When the bit is set to logic '1', the LVDS Sync Bus (SYNC/GATE connector, Section 2.6.4) is the source.

6.10.4.3 SEL GATE Bit D08

When Sync Bus B on this 7140 is the Sync Bus Master (MASTR bit D00 = 1) or when the LVDS Sync Bus' gate input is not used (GATE SRC bit D09 = 0), this bit selects the gate signal for sync bus B from either a register or the external TTL SYNC input. When this bit is cleared to logic '0' (its default state), the Gate B Generator Register, Section 6.10.6, is the source of the gate. When the bit is set to logic '1', the external TTL gate input (SYNC/ GATE connector, Section 2.6.4) is the source of the gate.

6.10.4.4 SYNC POL Bit D07

This bit selects the polarity of the External TTL SYNC input selected for sync bus B (see SYNC SRC, below) for resetting the GC4016 DDC. Polarity does not apply to the LVDS Sync input nor to a gate generated by the onboard register (Section 6.10.5). When this bit is cleared to logic '0' (its default state), a negative sync resets the GC4016. When the bit is set to logic '1', a positive sync resets the GC4016.

6.10.4.5 SYNC SRC Bit D06

This bit selects the source of the sync bus B SYNC signal from either the LVDS Sync Bus or an on−board sync signal. When this bit is cleared to logic '0' (its default state), the sync is selected by SEL SYNC bit D05. When the bit is set to logic '1', the LVDS Sync Bus (SYNC/GATE connector, Section 2.6.4) is the source.

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6.10 Sync Bus Registers (continued)

6.10.4 Master Bus B Control Register (continued)

6.10.4.6 SEL SYNC Bit D05

When Sync Bus B on this 7140 is the Sync Bus Master (MASTR bit D00 = 1) or when the LVDS Sync Bus' sync input is not used (SYNC SRC bit D06 = 0), this bit selects the sync bus B sync signal from either a register or the external TTL SYNC input. When this bit is cleared to logic '0' (its default state), the Sync A Generator Register, Section 6.10.5, is the source of the sync. When the bit is set to logic '1', the external TTL sync input (SYNC/GATE connectors, Section 2.6.4) is the source of the sync.

6.10.4.7 CLK SRC Bit D04

This bit selects the source of the sync bus B clock from either the LVDS Sync Bus or an onboard clock source. When the bit is cleared to logic '0' (its default state), the LVDS Sync Bus is bypassed and the clock is selected by SEL CLK bit D02, below. When this bit is set to logic '1', the EXT LVDS CLK A input (SYNC/GATE connector, Section 2.6.4) is the source of the clock.

6.10.4.8 OSC DSBL Bit D03

This bit enables or disables the output from the onboard crystal oscillator B. When the bit is cleared to logic '0' (its default state), the onboard oscillator (Oscillator B) is enabled. When this bit is set to logic '1', the onboard oscillator is disabled. When using the external MMCX clock input (SEL CLK bit D02 = 1, below), you must disable the oscillator.

6.10.4.9 SEL CLK Bit D02

When Sync Bus B on this 7140 is the Sync Bus Master (MASTR bit D00 = 1) or when the LVDS Sync Bus clock input is not used (CLK SRC bit D04 = 0), this bit selects the sync bus B clock signal from either the onboard oscillator or the external clock input. When this bit is cleared to logic '0' (its default state), the onboard oscillator is selected (for this setting, OSC DSBL bit D03, above, must be cleared to logic '0' to enable the oscillator). When the bit is set to logic '1', the external clock input is used (MMCX CLK A connector, Section 2.6.3).

NOTE: When you select the external clock, you must provide a delay of 50 mS or more for "device settling" time. ReadyFlow high–level functions already include this delay but low–level macros do not.

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6.10 Sync Bus Registers (continued)

6.10.4 Master Bus B Control Register (continued)

6.10.4.10 TERM Bit D01

This bit enables termination of LVDS Sync Bus B by a Slave, or by a Master if it is the only unit on the bus. When the bit is cleared to logic '0' (its default state), the sync bus is not terminated. When the bit is set to logic '1', the bus is terminated. The sync bus must be terminated when this Model 7140 is the last (or only) Slave on the bus, or if it is a Master or the only unit on the bus.

6.10.4.11 MASTR Bit D00

This bit sets this Model 7140 as either Master or Slave on LVDS Sync Bus B. When the bit is cleared to logic '0' (its default state), this 7140 is a Slave. When bit is set to logic '1', this 7140 is the Sync Bus B Master. When only one 7140 is used it must be set as a Master.

When set as a Sync Bus Master, this Model 7140 Sync Bus B is the source of the sync, clock, and gate signals output to the LVDS Sync Bus. You must select these sources using control bits SYNC SRC (bits D05, D06), CK SRC (bit D04), and GATE SRC (bits D09, D08), and if needed, generate the sync and/or gate signals using the Gate B Generator Register (Section 6.10.6) and Sync B Gener–ator Register (Section 6.10.5).

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6.10 Sync Bus Registers (continued)

6.10.5 Sync B Generator Register

The Sync B Generator Register is used on a 7140 that is configured as a Sync Bus Master (MASTR = 1, Master Bus B Control Register, Section 6.10.4.11), or on a 7140 that is not connected to an external LVDS Sync Bus.

The following table shows the contents of the Sync Generator Register.

Table 6–17: Sync B Generator Register
R/W @ BAR2+0x80A0

	D15 – D01	D00
Bit Name	Reserved	$\overline{\text{SYNC}}$
Function	Write with zeros, Mask when reading	0 = Reset 1 = Release
Bit D00 defaults to the logic '1' state at power on and reset		

If the sync source is set to the onboard register (SYNC SRC= 00, Master Bus B Control Register, Section 6.10.4.5), the $\overline{\text{SYNC}}$ bit in this register creates the sync signal (SYNC B) for the board, and for output to the LVDS Sync Bus (SYNC/GATE connector, Section 2.6.4) for a Sync Bus Master.

The Sync B signal can be enabled and routed to different devices on the board using the Sync Mask Register, Section 6.10.7, D/A Sync Bus Select Register, Section 6.10.8, and the A/D Sync Bus Select Register, Section 6.10.9.

When the bit is cleared to logic '0', the device is in reset. When the bit is set to logic '1' (its default state), the device is released for normal operation.

NOTE: When using Sync B, the DAC clock must be set up properly using the DAC Control/Status Register, Section 6.15.8.

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6.10 Sync Bus Registers (continued)

6.10.6 Gate B Generator Register

The Gate B Generator Register is used on a 7140 that is configured as a Sync Bus Master (MASTR = 1, Master Bus B Control Register, Section 6.10.4.11), or on a 7140 that is not connected to an external LVDS Sync Bus.

The following table shows the contents of the Gate Generator Register.

Table 6–18: Gate B Generator Register
R/W @ BAR2+0x80A8

	D15 – D01	D00
Bit Name	Reserved	$\overline{\text{GATE}}$
Function	Write with zeros, Mask when reading	0 = Enable 1 = Disable
Bit D00 defaults to the logic '1' state at power on and reset		

If the gate source is set to the onboard register (GATE SRC= 00, Master Bus B Control Register, Section 6.10.4.2), the $\overline{\text{GATE}}$ bit in this register creates the gate signal (Gate B) for FIFO writing control, and for output to the LVDS Sync Bus (SYNC/GATE connector, Section 2.6.4) for a Sync Bus Master.

When the bit is cleared to logic '0', FIFO writes are enabled. When the bit is set to logic '1' (its default state), FIFO writes are disabled.

NOTE: When using Gate B, the DAC clock must be set up properly using the DAC Control/Status Register, Section 6.15.8.

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6.10 Sync Bus Registers (continued)

6.10.7 Sync Mask Register

This register enables a sync signal to be applied to the GC4016 DDC and/or the DAC 5686 Upconverter. The sync signal is derived from the either Sync Bus A or Sync Bus B depending on the setting of A/D Sync Bus Select Register (for the GC4016, Section 6.10.9) and the D/A Sync Bus Select Register (for the DAC 5686, Section 6.10.8).

The following table shows the contents of the Sync Mask Register.

Table 6–19: Sync Mask Register
R/W @ BAR2+0x80B0

	D15 – D02	D01	D00
Bit Name	Reserved	DAC	DDC
Function	Write with zeros, Mask when reading	0 = Disable 1 = Enable	
Bit D00 defaults to the logic '1' state at power on and reset			

6.10.7.1 DAC Bit D01

When the bit is set to logic '1', the sync signal is enabled to the Phase synchronization input (PHSTR) for both DAC channels on the DAC5686. When the bit is cleared to logic '0', the sync is not enabled for the DAC5686.

6.10.7.2 DDC Bit D00

When the bit is set to logic '1', the sync signal is enabled to the SYNC input to the GC4016 DDC. When the bit is cleared to logic '0', the sync is not enabled for the GC4016.

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6.10 Sync Bus Registers (continued)

6.10.8 D/A Sync Bus Select Register

The D/A Sync Bus Select Register selects either Sync Bus A or Sync Bus B to be used as the clock and sync signal source for the digital–to–analog output processing, including the DAC5686 and the DAC FIFOs. (The clock for the DAC FIFOs is also controlled by the DAC CLK bit in the DAC Control/Status Register, Section 6.15.8.)

Refer to the Master Bus A/B Control Register, Section 6.10.1 or 6.10.4, to configure these signals for the selected Sync Bus.

The following table shows the contents of this register.

Table 6–20: D/A Sync Bus Select Register
R/W @ BAR2+0x8400

	D15 – D01	D00
Bit Name	Reserved	SEL
Function	Write with zeros, Mask when reading	0 = Bus A 1 = Bus B
Bit D00 defaults to the logic '1' state at power on and reset		

Setting this bit to logic '0' selects Sync Bus A, setting to '1' selects Sync Bus B.

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6.10 Sync Bus Registers (continued)

6.10.9 A/D Sync Bus Select Register

The A/D Sync Bus Select Register selects either Sync Bus A or Sync Bus B to be used as the clock and sync signal source for the analog–to–digital input processing, including the AD6645s, GC4016 DDC, and ADC FIFOs. (The clock input to the DDC FIFOs is routed from the GC4016 output clock.)

Refer to the Master Bus A/B Control Register, Section 6.10.1 or 6.10.4, to configure these signals for the selected Sync Bus.

The following table shows the contents of this register.

Table 6–21: A/D Sync Bus Select Register
R/W @ BAR2+0x8C00

	D15 – D01	D00
Bit Name	Reserved	SEL
Function	Write with zeros, Mask when reading	0 = Bus A 1 = Bus B
Bit D00 defaults to the logic '1' state at power on and reset		

Setting this bit to logic '0' selects Sync Bus A, setting to '1' selects Sync Bus B.

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6.11 Interrupt Registers

The following subsections describe the FPGA registers that control the FGGA interrupts. Refer to Section 4.9, Interrupt Operation, for additional information about the use and programming of interrupts.

6.11.1 System Interrupt Enable Register

The System Interrupt Enable Register contains enable bits for several system interrupt conditions. Each bit enables or disables the generation of an interrupt to the Application Interrupt Status Registers, Section 6.11.6. The four Application Interrupt LINT Enable Registers, Section 6.11.4, can be configured to generate any of the four local bus interrupt inputs (LINTi0 to LINTi3) to the PCI7140 in response to these interrupts.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–22: System Interrupt Enable Register
R/W @ BAR2+0x8100

	D15 – D08					
Bit Name	D15 – D08					
Function	User–Defined Read/Write					
	D07 – D05	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	Reserved	VOLT/TEMP	CLK B LOSS	CLK A LOSS	OVRLD CH2	OVRLD CH1
Function	Write with zeros, Mask when reading	0 = Disable Interrupt 1 = Enable Interrupt				
All bits default to the logic '0' state at power on and reset						

Each bit of this register enables or disables an interrupt to the Application Interrupt Status Registers for a particular system interrupt condition. Setting a bit to logic '1' enables generation of a local interrupt when that interrupt condition occurs. When a bit is cleared to logic '0' (its default state), the interrupt will not be generated by the associated interrupt condition.

Table 6–23, on the next page, provides descriptions of the interrupt condition associated with each of these bits.

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6.11 Interrupt Registers (continued)

6.11.1 System Interrupt Enable Register (continued)

The following table describes the interrupt condition associated with each bit of the System Interrupt register.

Table 6–23: System Interrupt Register Bits

Bit Name	Bit Position	Interrupt Function
User–Defined	D15 – D08	These bits are reserved for user–defined interrupt functions
VOLT/TEMP	D04	This bit is associated with a temperature/voltage limit interrupt from the LM83 or ADM1024 sensors. (To determine the sensor causing the interrupt, use the TWSI Port Register, Section 6.4.)
CLK A LOSS CLK B LOSS	D03 D02	This bit is associated with a Clock loss interrupt from one of the Sync Buses, A or B.
OVLD CH2 OVLD CH1	D01 D00	Each of these bits is associated with an analog input overload interrupt from one of the A/D converters (A/D2 or A/D1).

Note: These bit assignments and definitions apply to System Interrupt Enable Register, Section 6.11.1, System Interrupt Flag Register, Section 6.11.2, and System Interrupt Status Register, Section 6.11.3

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6.11 Interrupt Registers (continued)

6.11.2 System Interrupt Flag Register

The System Interrupt Flag Register has one read/clear bit associated with each system interrupt condition (the same bit associations as in the System Interrupt Status Register, Section 6.11.3).

The following table shows which bit in this register is associated with each interrupt condition. Table 6–23, on the prior page, provides description of the interrupt condition associated with each of these bits.

Table 6–24: System Interrupt Flag Register
R/Clr @ BAR2+0x8108

	D15 – D08					
Bit Name	D15 – D08					
Function	User–Defined Read/Clear					
	D07 – D05	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	Reserved	VOLT/TEMP	CLK B LOSS	CLK A LOSS	OVRLD CH2	OVRLD CH1
Function	Write with zeros, Mask when reading	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch				

IMPORTANT! When reset, including power–up, the state of this register is unknown. You should clear this register before using it, by writing '1's into all bits.

Read:

Each bit of this register latches an interrupt occurrence. Logic '1' in any bit in this register indicates that an interrupt has occurred. Note that when any bit in the System Interrupt Status Register (Section 6.11.3) changes to logic '1', the corresponding bit in this register will also be set to logic '1'. However, when a bit in the System Interrupt Status Register changes from logic '1' to logic '0', the corresponding latched bit in this register does not clear, but remains at the logic '1' state.

Clear:

Since these bits latch in response to an interrupt, to detect subsequent interrupts, you must clear the bits in this register. To clear any bit in this register that is set to logic '1' you must write a '1' to that bit.

Refer to Interrupt Operation, Section 4.9, for further description of interrupt routing and operation on the Model 7140.

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6.11 Interrupt Registers (continued)

6.11.3 System Interrupt Status Register

The System Interrupt Status Register has one read–only bit associated with each system interrupt condition (the same bit associations as in the System Interrupt Flag Register, Section 6.11.2).

The following table shows which bit in this register is associated with each interrupt condition. Table 6–23, on page 140, provides description of the interrupt condition associated with each of these bits.

Table 6–25: System Interrupt Status Register
R.O. @ BAR2+0x8110

	D15 – D08					
Bit Name	D15 – D08					
Function	User–Defined Read Only					
	D07 – D05	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	Reserved	VOLT/TEMP	CLK B LOSS	CLK A LOSS	OVRLD CH2	OVRLD CH1
Function	Write with zeros, Mask when reading	0 = No interrupt 1 = Overtemp	0 = No interrupt 1 = No Clock	0 = No interrupt 1 = No Clock	0 = No interrupt 1 = Overload	0 = No interrupt 1 = Overload
When reset, including power–up, the state of this register is unknown.						

Each bit in this register changes whenever the associated interrupt indication changes.

- A status bit changes to logic '1' whenever the interrupt indication occurs. Note that when any status bit in this register changes to logic '1', the corresponding bit in the System Interrupt Flag Register, Section 6.11.2, will also be set to logic '1'.

- A status bit in this register clears to logic '0' when that interrupt condition clears, whereas the associated bit in the System Interrupt Flag Register remains latched at logic '1' until it is cleared by that register's clear action, Section 6.11.2.

If the corresponding bit has been set to logic '1' in the System Interrupt Enable Register (Section 6.11.1), then an System Interrupt Status Register bit transition from logic '0' to logic '1' will also generate a local bus interrupt to the PCI interface. If you do not want an interrupt to occur and have set the corresponding interrupt enable bit to '0', you may poll the System Interrupt Status Register bit to determine if such an event has occurred.

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6.11 Interrupt Registers (continued)

6.11.4 Application Interrupt LINT Enable Registers

The Application Interrupt LINT Enable Registers contain enable bits for each application interrupt condition defined. Each bit enables or disables the generation of a local bus interrupt input (LINTix) to the PCI7140.

There are four Application Interrupt LINT Enable Registers, one for each local bus interrupt input (LINTi0 to LINTi3). Each register enables interrupts for the respective local bus interrupt. The PCI7140 can be configured, using the PCI Interrupt Enable Registers, Section 5.3, to route any of the four local bus interrupts (LINTi0 to LINTi3) to PCI interrupts (INTA to INTD).

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–26: Application Interrupt LINT Enable Registers
LINTi0: R/W @ BAR2+0x8118
LINTi1: R/W @ BAR2+0x8120
LINTi2: R/W @ BAR2+0x8128
LINTi3: R/W @ BAR2+0x8130

	D15	D14	D13	D12	D11	D10	D09	D08
Bit Name	SYS INT	GATE B	GATE A	SYNC B	SYNC A	TRIGGER CAPTURE	DELAY MEMORY READ FIFO	DELAY MEMORY WRITE FIFO
Function	0 = Disable Interrupt 1 = Enable Interrupt							
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	DAC B FIFO	DAC A FIFO	ADC 2 FIFO	ADC 1 FIFO	DDC FIFO D	DDC FIFO C	DDC FIFO B	DDC FIFO A
Function	0 = Disable Interrupt 1 = Enable Interrupt							

All bits default to the logic '0' state at power on and reset

Each bit of this register enables or disables the generation of a local bus interrupt (LINT0 to LINT3, depending on the register used) for a particular interrupt condition. Setting the bit associated with a given interrupt to logic '1' enables the generation of a local bus interrupt when that interrupt condition occurs. When a bit is cleared to logic '0' (its default state), the local bus interrupt will not be generated by the defined interrupt condition.

Table 6–27, on the next page, provides descriptions of the interrupt condition associated with each of these bits.

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6.11 Interrupt Registers (continued)

6.11.4 Application Interrupt LINT Enable Registers (continued)

The following table describes the interrupt condition associated with each bit of the four Application Interrupt Enable registers.

Table 6–27: Application Interrupt Register Bits

Bit Name	Bit Position	Interrupt Function
SYS INT	D15	This bit is associated with an interrupt from the OR'ed result of any of the enabled interrupts in the System Interrupt Enable Register (Section 6.11.1).
GATE B GATE A	D14 D13	Each of these bits is associated with an Sync Bus GATE (A or B) interrupt. The interrupt occurs at the start of the respective gate signal.
SYNC B SYNC A	D12 D11	Each of these bits is associated with an Sync Bus SYNC (A or B) interrupt. The interrupt occurs at the start of the respective Sync pulse.
TRIGGER CAPTURE	D10	This bit is associated with an interrupt from the OR'ed result of the ADC/DDC/DAC FIFO Trigger Capture bits. Use the applicable FIFO Status Registers, Sections 6.12.2, 6.13.2, or 6.15.2, to determine the interrupting FIFO.
DELAY MEMORY READ FIFO	D09	This bit is associated with an interrupt from the Delay Memory Read FIFO status flags (Full, Almost Full, Almost Empty, Empty). Use the Delay Memory Read FIFO Status Registers, Section 6.17.8, to determine the interrupting condition from this FIFO.
DELAY MEMORY WRITE FIFO	D08	This bit is associated with an interrupt from the Delay Memory Write FIFO status flags (Full, Almost Full, Almost Empty, Empty). Use the Delay Memory Write FIFO Status Registers, Section 6.17.8, to determine the interrupting condition from this FIFO.
DAC B FIFO DAC A FIFO	D07 D06	Each of these bits is associated with an interrupt from the DAC x FIFO status flags (Full, Almost Full, Almost Empty, Empty). Use the DAC FIFO Status Registers, Section 6.15.2, to determine the interrupting condition from the associated FIFO.
ADC 2 FIFO ADC 1 FIFO	D05 D04	Each of these bits is associated with an interrupt from the ADC n FIFO status flags (Full, Almost Full, Almost Empty, Empty). Use the ADC FIFO Status Registers, Section 6.12.2, to determine the interrupting condition from the associated FIFO.
DDC FIFO D DDC FIFO C DDC FIFO B DDC FIFO A	D03 D02 D01 D00	Each of these bits is associated with an interrupt from the DDC x FIFO status flags (Full, Almost Full, Almost Empty, Empty). Use the DDC FIFO Status Registers, Section 6.13.2, to determine the interrupting condition from the associated FIFO.
These bit assignments and definitions apply to Application Interrupt Enable Register, Section 6.11.4, Interrupt Flag Register, Section 6.11.5, and Interrupt Status Register, Section 6.11.6		

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6.11 Interrupt Registers (continued)

6.11.5 Application Interrupt Flag Register

The Application Interrupt Flag Register has one read/clear bit associated with each application interrupt condition (the same bit associations as the Application Interrupt LINT Enable Register, Section 6.11.4).

The following table shows which bit in this register is associated with each interrupt condition. Table 6–27, on page 144, provides descriptions of the interrupt condition associated with each of these bits.

Table 6–28: Application Interrupt Flag Register
R/Clr @ BAR2+0x8138

	D15	D14	D13	D12	D11	D10	D09	D08
Bit Name	SYS INT	GATE B	GATE A	SYNC B	SYNC A	TRIGGER CAPTURE	DELAY MEMORY READ FIFO	DELAY MEMORY WRITE FIFO
Function	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch							
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	DAC B FIFO	DAC A FIFO	ADC 2 FIFO	ADC 1 FIFO	DDC FIFO D	DDC FIFO C	DDC FIFO B	DDC FIFO A
Function	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch							

IMPORTANT! When reset, including power–up, the state of this register is unknown. You should clear this register before using it, by writing '1's into all bits.

Read: Each bit of this register latches an interrupt occurrence. Logic '1' in any bit in this register indicates that an interrupt has occurred. Note that when any bit in the Application Interrupt Status Register (Section 6.11.6) changes to logic '1', the corresponding bit in this register will also be set to logic '1'. However, when a bit in the Application Interrupt Status Register changes from logic '1' to logic '0', the corresponding latched bit in this regis–ter does not clear, but remains at the logic '1' state.

Clear: Since these bits latch in response to an interrupt, to detect subsequent interrupts, you must clear the bits in this register. To clear any bit in this register that is set to logic '1' you must write a '1' to that bit.

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6.11 Interrupt Registers (continued)

6.11.6 Application Interrupt Status Register

The Application Interrupt Status Register has one read–only bit associated with each application interrupt condition (the same bit associations as the Application Interrupt LINT Enable Register, Section 6.11.4).

The following table shows which bit in this register is associated with each interrupt condition. Table 6–27, on page 144, provides descriptions of the interrupt condition associated with each of these bits.

Table 6–29: Application Interrupt Status Register
R.O. @ BAR2+0x8140

	D15	D14	D13	D12	D11	D10	D09	D08
Bit Name	SYS INT	GATE B	GATE A	SYNC B	SYNC A	TRIGGER CAPTURE	DELAY MEMORY READ FIFO	DELAY MEMORY WRITE FIFO
Function	0 = No Interrupt 1 = Interrupt condition asserted							
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	DAC B FIFO	DAC A FIFO	ADC 2 FIFO	ADC 1 FIFO	DDC FIFO D	DDC FIFO C	DDC FIFO B	DDC FIFO A
Function	0 = No Interrupt 1 = Interrupt condition asserted							
When reset, including power–up, the state of this register is unknown.								

Each bit in this register changes whenever the associated interrupt indication changes.

- A status bit changes to logic '1' whenever the interrupt indication occurs. Note that when any status bit in this register changes to logic '1', the corresponding bit in the Application Interrupt Flag Register, Section 6.11.5, will also be set to logic '1'.

- A status bit in this register clears to logic '0' when that interrupt condition clears, whereas the associated bit in the Application Interrupt Flag Register remains latched at logic '1' until it is cleared by that register's clear action, Section 6.11.5.

If the corresponding bit in any of the Application Interrupt LINT Enable Registers (Section 6.11.4) has been set to logic '1', then a transition from logic '0' to logic '1' will also generate that local bus interrupt to the PCI interface. If you do not want an interrupt to occur and have set the corresponding interrupt enable bit to '0', you may poll the Application Interrupt Status Register bit to determine if such an event has occurred.

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6.12 ADC Registers

The following subsections describe the FPGA registers that control analog to digital input data routing, including the AD6645 data outputs. There are no user−program−mable registers for the AD6645.

6.12.1 ADC FIFO Control Registers

There are two ADC FIFO Control Registers, one for each ADC channel, 1 and 2. This register contains bits that select the data packing modes and the source and characteristics of the gate/trigger used to control writing data samples from the AD6645's to the PCI Interface ADC FIFOs and the Delay Memory ADC FIFOs, and bits that specify the format of the data samples written to these FIFOs.

NOTE: The ADC FIFO register bit settings also control the same packing modes and operating characteristics of the Delay Memory ADC FIFOs (see Figure 6−3 on page 190).

The following table shows the contents of these registers. The subsections following the table provide descriptions of the bits in this register.

Table 6−30: ADC FIFO Control Registers
ADC 1: R/W @ BAR2+0x8CC8
ADC 2: R/W @ BAR2+0x8D00

	D15 – D14		D13	D12	D11	D10	D09	D08
Bit Name	Reserved		ARM	PRE/POST TRIGGER	Reserved	WORD SWAP	Reserved	PACK MODE
Function	Write with zeros, Mask when reading		0 = Not Armed 1 = Arm	0 = Post 1 = Pre	Write 0, Mask read	0 = No Swap 1 = Swap	Write 0, Mask read	0 = No Pack 1 = Pack
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	GATE SEL	Reserved	GATE CONTROL	TRIG CLEAR	HOLD MODE	GATE/TRIG	FIFO RESET	FIFO ENABLE
Function	0 = Gate A 1 = Gate B	Write 0, Mask read	0 = Enable 1 = Disable	0 = None 1 = Force Gate Inactive	0 = None 1 = Hold	0 = Gate 1 = Trigger	0 = Run 1 = Reset	0 = Disable 1 = Enable
All bits default to the logic '0' state at power on and reset								

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6.12 ADC Registers (continued)

6.12.1 ADC FIFO Control Registers (continued)

6.12.1.1 ARM Bit D13

This bit arms the trigger for data transfers from the ADC channel (1 or 2 depending on the register used) to the associated ADC PCI Interface and Delay Memory FIFOs. When the bit is cleared to logic '0' (its default state), the trigger is not armed. When the bit is set to logic '1', the trigger is armed and the data transfer can be controlled by the next trigger.

Use the PRE/POST TRIGGER bit D12, Section 6.12.1.2, to specify the trigger delay mode for data transfers. When you select PRE trigger counting mode, you must ARM the trigger to start the transfer of data.

6.12.1.2 PRE/POST TRIGGER Bit D12

This bit selects a trigger mode for data transfers from the ADC channel (1 or 2 depending on the register used) to the associated ADC PCI Interface and Delay Memory FIFOs. When the bit is cleared to logic '0' (its default state), POST trigger delay mode is selected. When the bit is set to logic '1', PRE trigger counting mode is selected.

- For POST trigger delay mode, use the Post Trigger Count Registers, Section 6.12.4, to specify the POST trigger delay count.

- For PRE trigger counting mode, you must ARM the trigger, bit D13 Section 6.12.1.1, to start the transfer of data. Use the Pre Trigger Count Capture Registers, Section 6.12.5, to return the number of PRE trigger samples stored.

When using PRE/POST trigger modes, you must select Trigger mode using the GATE/TRIG bit D02, Section 6.12.1.9, and you must set a trigger length using the associated Trigger Length Register, Section 6.12.6.

See Section 4.8.4 for additional information on Pre/Post Trigger.

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6.12 ADC Registers (continued)

6.12.1 ADC FIFO Control Registers (continued)

6.12.1.3 WORD SWAP Bit D10

This bit selects the 16−bit word swapping mode for writing data samples to the ADC FIFO (1 or 2). When the bit is cleared to logic '0' (its default state), the data is not swapped, and the first data sample (in A/D packed mode, see below) is in the lowest 16 bits of the 64−bit FIFO word. When the bit is set to logic '1', word swapping is enabled and each pair of 16−bit samples (in packed mode) are swapped in the 64−bit FIFO word, as follows:

Bits D00:15 are swapped with bits D16:31,
Bits D32:47 are swapped with bits D48:63.

6.12.1.4 PACK MODE Bit D08

This bit selects the data packing mode for writing data samples to the ADC FIFO (1 or 2). When the bit is cleared to logic '0' (its default state), the data is unpacked; when the bit is set to logic '1', the A/D data is packed.

Refer to Section 7.3, ADC Data Routing and Formats, for addi−tional information about the ADC data packing modes.

6.12.1.5 GATE SEL Bit D07

This bit selects the source of the gate for writes to the ADC FIFO (1 or 2). When the bit is cleared to logic '0' (its default state), Gate A is the source; when the bit is set to logic '1', Gate B is the source.

6.12.1.6 GATE CONTROL Bit D05

This bit enables Gate operation on the ADC FIFO (1 or 2). When the bit is cleared to '0' (the default state), the FIFO is controlled by the Gate (gate control is Enabled). When the bit is set to '1', the FIFO is free running (gate control Disabled).

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6.12 ADC Registers (continued)

6.12.1 ADC FIFO Control Registers (continued)

6.12.1.7 TRIG CLEAR Bit D04

This bit forces the selected gate to the inactive state in Trigger mode (GATE/TRIG bit D02 = 1, below). When this bit is cleared to logic '0' (its default state), there is no effect on the gate. When the bit is set to logic '1', the gate is forced to inactive (ADC FIFO writes disabled), regardless of the trigger length specified (Trigger Length Register, Section 6.12.6), and the TRIGGER CAPTURE bit D05 is cleared in the ADC FIFO Status Register, Section 6.12.2.

6.12.1.8 HOLD MODE Bit D03

This bit enables a gate Hold after the trigger is received in Trigger mode (GATE/TRIG bit D02 = 1, below). When the bit is cleared to logic '0' (its default state), the selected gate is active (ADC FIFO writes enabled) for the specified trigger length after the trigger (specified using the Trigger Length Register, Section 6.12.6), and then goes inactive (ADC FIFO writes disabled). When the bit is set to logic '1', HOLD is enabled and the gate remains active (ADC FIFO writes enabled) after the trigger is received until the Trigger is cleared using the TRIG CLEAR bit D04, above.

Note that when HOLD is enabled, you must set the Trigger Length to any number greater than zero.

6.12.1.9 GATE/TRIG Bit D02

This bit selects Gate or Trigger mode for the gate selected by GATE SEL (bit D07) for enabling ADC FIFO writes. When this bit is cleared to logic '0' (its default state), Gate mode is selected. When this bit is set to logic '1', Trigger mode is selected, and you must set a trigger length using the Trigger Length Register, Section 6.12.6, or enable trigger Hold (HOLD MODE bit D03 above).

6.12.1.10 FIFO RESET Bit D01

This bit resets the ADC PCI interface FIFO (1 or 2). When the bit is cleared to logic '0' (its default state), the FIFO is in run. When the bit is set to logic '1', the FIFO is in reset.

6.12.1.11 FIFO ENABLE Bit D00

This bit enables the ADC PCI interface FIFO (1 or 2). When the bit is cleared to logic '0' (its default state), the FIFO is disabled. When the bit is set to logic '1', the FIFO is enabled.

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6.12 ADC Registers (continued)

6.12.2 ADC FIFO Status Registers

There are two ADC FIFO Status Registers, one for each ADC channel, 1 and 2. The ADC FIFO Status Registers have several flag and status bits associated with data transfers from each ADC channel. The following table shows the bit layout of this register. The subsections following the table describe these bits.

Table 6–31: ADC FIFO Status Registers
ADC 1 FIFO: R/Clr @ BAR2+0x8168
ADC 2 FIFO: R/Clr @ BAR2+0x8170

	D15 – D12	D11	D10	D09	D08
Bit Name	Reserved	FULL FLAG	ALMOST FULL FLAG	ALMOST EMPTY FLAG	EMPTY FLAG
Function	Write with zeros, Mask when reading	**Read:** 0 = FIFO flag condition not active 1 = FIFO flag condition latched **Clear:** 1 = Clear latch			

	D07 – D06	D05 *	D04 *	D03 *	D02 *	D01 *	D00 *
Bit Name	Reserved	TRIGGER CAPTURE	FIFO WRITE ENABLED	FULL	ALMOST FULL	ALMOST EMPTY	EMPTY
Function	Write with zeros, Mask when reading	0 - Not done 1 - Done	0 - Not En 1 - Enabled	0 = FIFO flag condition not active 1 = FIFO flag condition active			

* These bits are Read Only
When reset, including power–up, the state of this register is unknown.
You should clear the register flag bits before using it, by writing '1's into bits D11 – D08.

6.12.2.1 FIFO Flag Bits — Bits D11 – D08

Read: Each bit latches a FIFO flag occurrence. Logic '1' in any bit indicates that a FIFO flag has been active. Note that when any status bit in this register (Section 6.12.2.4) changes to logic '1', the corresponding flag bit will also be set to logic '1'. However, when a status bit changes from '1' to '0', the corresponding latched bit in this register does not clear, but remains at the logic '1' state.

Clear: Since these bits latch in response to a FIFO flag occurrence, to detect subsequent FIFO flags, you must clear the bits in this register. To clear any bit in this register that is set to logic '1' you must write a '1' to that bit.

NOTE: These four FIFO flag bits are present only in boards with an FPGA revision date greater that 10/12/05 (see Section 6.8).

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6.12 ADC Registers (continued)

6.12.2 ADC FIFO Status Registers (continued)

6.12.2.2 TRIGGER CAPTURE Bit D05

This bit indicates the trigger capture status of the data transfer (ADC 1 or 2, depending on the register being accessed). When read as logic '0' the trigger has not completed. When read as logic '1' the trigger length is completed.

6.12.2.3 FIFO WRITE ENABLED Bit D04

This bit indicates the write enable status of the FIFO (ADC 1 or 2 FIFO, depending on the register being accessed). When read as logic '0' the FIFO is not write enabled. When read as logic '1' the FIFO is write enabled.

6.12.2.4 FIFO Status Bits Bits D03 – D00

Each status bit is a non−latched version of the associated FIFO flag condition. When read as logic '1', the associated FIFO flag condition is active (true). When read as logic '0', the associated FIFO flag condition is inactive.

Note that when any status bit changes to logic '1', the corre−sponding flag bit in this register (Section 6.12.2.1) will also be set to logic '1'. However, when a status bit changes from '1' to '0', the corresponding latched bit in this register does not clear, but remains at the logic '1' state.

The Almost Full and Almost Empty FIFO levels are set using the ADC FIFO Almost Full and Almost Empty Level Registers, Sec−tions 6.12.7 and 6.12.8.

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6.12 ADC Registers (continued)

6.12.3 ADC FIFO Interrupt Mask Registers

There are two ADC FIFO Interrupt Mask Registers, one for each ADC channel, 1 and 2. The Interrupt Mask Registers contain enable bits for each interrupt condition defined. Each bit enables or disables the generation of a local bus interrupt (LINTix) to the PCI7140.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–32: ADC FIFO Interrupt Mask Registers
ADC 1 FIFO: R/W @ BAR2+0x8CE0
ADC 2 FIFO: R/W @ BAR2+0x8D18

	D15 – D06	D05	D04	D03	D02	D01	D00
Bit Name	Reserved	TRIGGER CAPTURE	Reserved	FULL	ALMOST FULL	ALMOST EMPTY	EMPTY
Function	Write with zeros, Mask when reading	0 = Disable Interrupt 1 = Enable Interrupt					
All bits default to the logic '0' state at power on and reset							

Each bit of this register enables or disables the generation of a local bus interrupt to the PCI7140, when interrupts are enabled for this register in the Application Interrupt Enable LINTx Registers, Section 6.11.4.

Setting the bit associated with a given interrupt to the logic '1' state enables the generation of a local bus interrupt when that interrupt condition occurs. When a bit is cleared to logic '0' (its default state), the local bus interrupt will not be generated by the associated interrupt condition.

The interrupt conditions are:

D05 – Trigger Capture, Trigger Length has been counted down to zero
D03 – FIFO is Full
D02 – FIFO is at the Almost Full level
D01 – FIFO is at the Almost Empty level
D00 – FIFO is Empty

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6.12 ADC Registers (continued)

6.12.4 ADC Post Trigger Count Registers

There are four ADC Post Trigger Count Registers, two registers for each AD6645 input channel, 1 and 2. These registers specify the delay in storing data samples to the applicable ADC FIFO after the trigger is received. These registers are valid only when the associated ADC FIFO Control Register, Section 6.12.1, is set for POST trigger mode.

Each ADC channel's delay count is specified using two registers, one for the least significant 16 bits (LSB) and one for the most significant 16 bits (MSB). The following tables show the format of these registers.

Table 6–33: ADC Post Trigger Count LSB Registers
ADC 1: R/W @ BAR2+0x8888
ADC 2: R/W @ BAR2+0x8898

	D15 – D00
Bit Name	D15 – D0
Function	Post Trigger Count least significant bits (LSB)
All bits default to the logic '0' state at power on and reset	

Table 6–34: ADC Post Trigger Count MSB Registers
ADC 1: R/W @ BAR2+0x8890
ADC 2: R/W @ BAR2+0x88A0

	D15 – D00
Bit Name	D31– D16
Function	Post Trigger Count most significant bits (MSB)
All bits default to the logic '0' state at power on and reset	

The Post Trigger Count is a 32–bit binary value, with the most significant bit (D31) in bit D15 of the MSB register. This value specifies the number of samples to delay, after the trigger is received, before writing A/D samples to the applicable ADC FIFO. See Section 4.8.4 for additional information on Post Triggering.

NOTE: When specifying a Post Trigger Count for an ADC channel, be sure to write to BOTH registers for that ADC channel.

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6.12 ADC Registers (continued)

6.12.5 ADC Pre Trigger Count Capture Registers

There are four ADC Pre Trigger Count Capture Registers, two registers for each AD6645 input channel, 1 and 2. These read–only registers return the number of data samples stored in the applicable ADC FIFO before the trig–ger is received. These registers are valid only when the associated ADC FIFO Control Register, Section 6.12.1, is set for PRE trigger mode.

Each ADC channel's pre trigger count is returned using two registers, one for the least significant 16 bits (LSB) and one for the most significant 16 bits (MSB). The following tables show the format of these registers.

Table 6–35: ADC Pre Trigger Count Capture LSB Registers
ADC 1: R.O. @ BAR2+0x88E8
ADC 2: R.O. @ BAR2+0x88F8

	D15 – D00
Bit Name	D15 – D0
Function	Pre Trigger Count Capture least significant bits (LSB)
All bits default to the logic '0' state at power on and reset	

Table 6–36: ADC Pre Trigger Count Capture MSB Registers
ADC 1: R.O. @ BAR2+0x88F0
ADC 2: R.O. @ BAR2+0x8900

	D15 – D14	D13	D12 – D00
Bit Name	Reserved	WRAP	D28 – D16
Function	Mask read	0 = No wrap 1 = Wrap	Pre Trigger Count Capture most significant bits (MSB)
All bits default to the logic '0' state at power on and reset			

The Pre Trigger Count Capture is a 29–bit binary value, with the most sig–nificant bit (D29) in bit D12 of the MSB register. This value indicates the actual number of A/D data samples stored into the applicable ADC FIFO before the trigger is received. When bit D13 of the MSB register reads as logic '1' the number of data samples stored has exceeded the 29–bit Pre Trigger Count Capture field and has wrapped around. See Section 4.8.4 for addi–tional information on Pre Triggering.

NOTE: When reading a Pre Trigger Count for an ADC channel, be sure to read BOTH registers for that ADC channel.

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6.12 ADC Registers (continued)

6.12.6 ADC Trigger Length Registers

There are four ADC Trigger Length Registers, two registers for each ADC channel, 1 and 2. Each Trigger Length is specified using two registers, one for the least significant 16 bits (LSB) and one for the most significant 16 bits (MSB).

When Trigger mode is selected for a FIFO gate (GATE/TRIG = 1, ADC FIFO Control Register, Section 6.12.1.9), these registers set the length that the gate is active (FIFO writes enabled) after receipt of the trigger.

The following tables show the contents of the Trigger Length Registers.

Table 6–37: ADC Trigger Length LSB Registers
ADC 1: R/W @ BAR2+0x8CD0
ADC 2: R/W @ BAR2+0x8D08

	D15 – D00
Bit Name	D15 – D0
Function	Trigger Length (N–1) least significant bits (LSB)
All bits default to the logic '0' state at power on and reset	

Table 6–38: ADC Trigger Length MSB Registers
ADC 1: R/W @ BAR2+0x8CD8
ADC 2: R/W @ BAR2+0x8D10

	D15 – D00
Bit Name	D31– D16
Function	Trigger Length (N–1) most significant bits (MSB)
All bits default to the logic '0' state at power on and reset	

The trigger length is a 32–bit binary value, with the most significant bit (D31) in bit D15 of the MSB register. This value specifies the length of the write gate after the trigger as the number of FIFO writes, up to 65,535. To specify a trigger length of N FIFO writes, set this register to N–1.

See Section 4.8.4 for information on ADC Pre/Post Triggering.

Each ADC channel's registers apply to data transfers from the AD6645 to both the FPGA PCI bus ADC FIFO and the Delay Memory ADC FIFO.

NOTE: When specifying a trigger length, be sure to write to BOTH Trigger Length Registers for that ADC channel.

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6.12 ADC Registers (continued)

6.12.7 ADC FIFO Almost Empty Level Registers

There are two ADC FIFO Almost Empty Level Registers, one for each ADC FIFO, 1 and 2. This register sets the programmable boundary flag level of the Almost Empty flag for the associated FIFO.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–39: ADC FIFO Almost Empty Level Registers
ADC 1 FIFO: R/W @ BAR2+0x8CE8
ADC 2 FIFO: R/W @ BAR2+0x8D20

	D15 – D10	D09 – D00
Bit Name	Reserved	D9 – D0
Function	Write with zeros, Mask when reading	FIFO Almost Empty Level
All bits default to the logic '0' state at power on and reset		

The Almost Empty Level is a 10–bit binary value, with bit D09 the MSB. This value specifies the FIFO Almost Empty flag depth.

NOTE: All 7140 FIFOs are 64 bits wide. Thus, the FIFO level programmed into this register indicates the level of 64–bit words. For example, if you set this register to a level of 12, the FIFO sets a boundary flag when the data transfer reaches 24 32–bit words.

While the FIFO is being read, when the data is at or below the Almost Empty level, the FIFO sets the Almost Empty Flag.

- The FIFO Almost Empty Flag is routed to the associated ADC FIFO Status Register, Section 6.12.2.
- If the Almost Empty Flag is enabled by the associated ADC FIFO Interrupt Mask Register, Section 6.12.3, a local bus interrupt will be asserted to the PCI7140.

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6.12 ADC Registers (continued)

6.12.8 ADC FIFO Almost Full Level Registers

There are two ADC FIFO Almost Full Level Registers, one for each ADC FIFO, 1 and 2. This register sets the programmable boundary flag level of the Almost Full flag for the associated FIFO.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–40: ADC FIFO Almost Full Level Registers
ADC 1 FIFO: R/W @ BAR2+0x8CF0
ADC 2 FIFO: R/W @ BAR2+0x8D28

	D15 – D10	D09 – D00
Bit Name	Reserved	D9 – D0
Function	Write with zeros, Mask when reading	FIFO Almost Full Level
All bits default to the logic '0' state at power on and reset		

The Almost Full Level is a 10–bit binary value, with bit D09 the MSB. This value specifies the FIFO Almost Full flag depth.

NOTE: All 7140 FIFOs are 64 bits wide. Thus, the FIFO level programmed into this register indicates the level of 64–bit words. For example, if you set this register to a level of 12, the FIFO sets a boundary flag when the data transfer reaches 24 32–bit words.

While the FIFO is being written to, when the data is at or above the Almost Full level, the FIFO sets the Almost Full Flag.

- The FIFO Almost Full Flag is routed to the associated ADC FIFO Status Register, Section 6.12.2.
- If the Almost Full Flag is enabled by the associated ADC FIFO Interrupt Mask Register, Section 6.12.3, a local bus interrupt will be asserted to the PCI7140.

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6.12 ADC Registers (continued)

6.12.9 ADC FIFO Decimation Divide Registers

There are two ADC Decimation Divide Registers, one for each ADC FIFO, 1 and 2. This register sets the decimation rate of data samples written to the applicable ADC FIFO (1 or 2).

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–41: ADC FIFO Decimation Divide Register
ADC 1 FIFO: R/W @ BAR2+0x8CF8
ADC 2 FIFO: R/W @ BAR2+0x8D30

	D15 – D12	D11 – D00
Bit Name	Reserved	B11 – B0
Function	Write with zeros, Mask when reading	12–bit rate divider 'N–1'
All bits default to the logic '0' state at power on and reset		

The rate divider is a 12–bit binary value, with bit D11 the MSB. To take every Nth sample, where N is any value between 1 and 4096, set this register to N–1.

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6.13 DDC Registers

The following subsections describe the FPGA registers that control the digital down–conversion processing, except for the GC4016. The GC4016 contains internal program–mable status and control registers. All reads and writes to these DAC5686 internal registers are programmed using the FPGA's GC4016 Registers defined in Section 6.14.

6.13.1 DDC FIFO Control Registers

There are four DDC FIFO Control Registers, one for each DDC channel, A, B, C, and D. Each register contains bits that select the source and characteris–tics of the gates used to control writing data samples from the GC4016 to the DDC FIFO.

NOTE: The DDC FIFO register bit settings also control the same packing modes and operating characteristics of the Delay Memory DDC FIFOs (see Figure 6–3 on page 190).

The following table shows the contents of the DDC FIFO Control Registers. The subsections following the table describe these bits.

Table 6–42: DDC FIFO Control Registers

DDC A FIFO: R/W @ BAR2+0x8C08
DDC B FIFO: R/W @ BAR2+0x8C38
DDC C FIFO: R/W @ BAR2+0x8C68
DDC D FIFO: R/W @ BAR2+0x8C98

	D15 – D12				D11	D10	D09	D08
Bit Name	Reserved				REAL MODE	WORD SWAP	TAG MODE	PACK MODE
Function	Write with zeros, Mask when reading				0 = Disable 1 = Enable	0 = No Swap 1 = Swap	0 = Disable 1 = Enable	0 = Unpack 1 = Pack I&Q
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	GATE SEL	Reserved	GATE CONTROL	TRIG CLEAR	HOLD MODE	GATE/TRIG	FIFO RESET	FIFO ENABLE
Function	0 = Gate A 1 = Gate B	Write 0, Mask read	0 = Enable 1 = Disable	0 = None 1 = Force Gate Inactive	0 = None 1 = Hold	0 = Gate 1 = Trigger	0 = Run 1 = Reset	0 = Disable 1 = Enable
All bits default to the logic '0' state at power on and reset								

6.13.1.1 REAL MODE D11

This bit enables Real data to be written to the DDC FIFO (A, B, C, or D) from the GC4016. When the bit is cleared to logic '0' (its default state), both I and Q data are written. When this bit is set to logic '1', only Real data (I output) is transferred to the FIFO.

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6.13 DDC Registers (continued)

6.13.1 DDC FIFO Control Registers (continued)

6.13.1.2 WORD SWAP Bit D10

This bit selects Word Swap mode for writing to a DDC FIFO (A, B, C, or D). When the bit is cleared to logic '0' (its default state), the data is not swapped. When the bit is set to logic '1', word swapping is enabled and each pair of 16−bit samples (each pair of I and Q values in packed mode) are swapped in the 64−bit FIFO word, as follows:

Bits D00:15 are swapped with bits D16:31,
Bits D32:47 are swapped with bits D48:63.

6.13.1.3 TAG MODE Bit D09

This bit enables the tagging mode for writes to the DDC FIFO (A, B, C, or D). When the bit is cleared to logic '0' (its default state), tagging is disabled. When the bit is set to logic '1', the DDC data includes a CG4016 tag.

NOTE: When tag mode is enabled, tagging (4−bit or 2−bit) must be set ON in the GC4016 (see Section 6.14 for the GC4016 registers). See Section 7.4 for DDC formatting.

6.13.1.4 PACK MODE Bit D08

This bit selects the I and Q data packing mode for writes to the DDC FIFO (A, B, C, or D). When the bit is cleared to logic '0' (its default state), I and Q data is unpacked; when the bit is set to logic '1', I and Q data is packed. Refer to Section 7.4, DDC Data Routing and Formats, for additional information about the DDC data packing modes.

6.13.1.5 GATE SEL Bit D07

This bit selects the source of the gate for writes to the DDC FIFO (A, B, C, or D). When the bit is cleared to logic '0' (its default state), Gate A is the source; when the bit is set to logic '1', Gate B is the source.

6.13.1.6 GATE CONTROL Bit D05

This bit enables Gate operation on the DDC FIFO (A, B, C, or D). When the bit is cleared to '0' (the default state), the FIFO is con−trolled by the Gate (gate control is Enabled). When the bit is set to '1', the FIFO is free running (gate control Disabled).

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6.13 DDC Registers (continued)

6.13.1 DDC FIFO Control Registers (continued)

6.13.1.7 TRIG CLEAR Bit D04

This bit forces the selected gate to the inactive state in Trigger mode (GATE/TRIG bit D02 = 1, below). When this bit is cleared to logic '0' (its default state), there is no effect on the gate. When the bit is set to logic '1', the gate is forced to inactive (DDC FIFO writes disabled), regardless of the trigger length specified (Trigger Length Register, Section 6.13.5), and the TRIGGER CAPTURE bit D05 is cleared in the DDC FIFO Status Register, Section 6.13.2.

6.13.1.8 HOLD MODE Bit D03

This bit enables a gate Hold after the trigger is received in Trigger mode (GATE/TRIG bit D02 = 1, below). When the bit is cleared to logic '0' (its default state), the selected gate is active (DDC FIFO writes enabled) for the specified trigger length after the trigger (specified using the Trigger Length Register, Section 6.13.5), and then goes inactive (DDC FIFO writes disabled). When the bit is set to logic '1', HOLD is enabled and the gate remains active (DDC FIFO writes enabled) after the trigger is received until the Trigger is cleared using the TRIG CLEAR bit D04, above.

Note that when HOLD is enabled, you must set the Trigger Length to any number greater than zero.

6.13.1.9 GATE/TRIG Bit D02

This bit selects Gate or Trigger mode for the gate selected by GATE SEL (bit D07) for enabling DDC FIFO writes. When this bit is cleared to logic '0' (its default state), Gate mode is selected. When this bit is set to logic '1', Trigger mode is selected, and you must set a trigger length using the Trigger Length Register, Section 6.13.5, or enable trigger Hold (HOLD MODE bit D03 above).

6.13.1.10 FIFO RESET Bit D01

This bit resets the DDC FIFO (A, B, C, or D). When the bit is cleared to logic '0' (its default state), the FIFO is in run; when the bit is set to logic '1', the FIFO is in reset.

6.13.1.11 FIFO ENABLE Bit D00

This bit enables the DDC FIFO (A, B, C, or D). When the bit is cleared to logic '0' (its default state), the FIFO is disabled; when the bit is set to logic '1', the FIFO is enabled.

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6.13 DDC Registers (continued)

6.13.2 DDC FIFO Status Registers

There are four DDC FIFO Status Registers, one for each DDC channel (A, B, C, and D). Each register contains several flag and status bits associated with data transfers from each DDC FIFO.

The following table shows the bit layout of this register. The subsections following the table describe these bits.

Table 6–43: DDC FIFO Status Registers

DDC A FIFO: R/Clr @ BAR2+0x8148
DDC B FIFO: R/Clr @ BAR2+0x8150
DDC C FIFO: R/Clr @ BAR2+0x8158
DDC D FIFO: R/Clr @ BAR2+0x8160

	D15 – D12	D11	D10	D09	D08
Bit Name	Reserved	FULL FLAG	ALMOST FULL FLAG	ALMOST EMPTY FLAG	EMPTY FLAG
Function	Write with zeros, Mask when reading	**Read:** 0 = FIFO flag condition not active 1 = FIFO flag condition latched **Clear:** 1 = Clear latch			

	D07 – D06	D05 *	D04 *	D03 *	D02 *	D01 *	D00 *
Bit Name	Reserved	TRIGGER CAPTURE	FIFO WRITE ENABLED	FULL	ALMOST FULL	ALMOST EMPTY	EMPTY
Function	Write with zeros, Mask when reading	0 - Not done 1 - Done	0 - Not En 1 - Enabled	0 = FIFO flag condition not active 1 = FIFO flag condition active			

* These bits are Read Only
When reset, including power–up, the state of this register is unknown.
You should clear the register flag bits before using it, by writing '1's into bits D11 – D08.

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6.13 DDC Registers (continued)

6.13.2 DDC FIFO Status Registers (continued)

6.13.2.1 FIFO Flag Bits — Bits D11 – D08

Read: Each bit latches a FIFO flag occurrence. Logic '1' in any bit indicates that a FIFO flag has been active. Note that when any status bit in this register (Section 6.13.2.4) changes to logic '1', the corresponding flag bit will also be set to logic '1'. However, when a status bit changes from '1' to '0', the corresponding latched bit in this register does not clear, but remains at the logic '1' state.

Clear: Since these bits latch in response to a FIFO flag occurrence, to detect subsequent FIFO flags, you must clear the bits in this register. To clear any bit in this register that is set to logic '1' you must write a '1' to that bit.

NOTE: These four FIFO flag bits are present only in boards with an FPGA revision date greater that 10/12/05 (see Section 6.8).

6.13.2.2 TRIGGER CAPTURE — Bit D05

This bit indicates the trigger capture status of the data transfer (DDC A, B, C, or D, depending on the register being accessed). When read as logic '0' the trigger has not completed. When read as logic '1' the trigger length is completed.

6.13.2.3 FIFO WRITE ENABLED — Bit D04

This bit indicates the write enable status of the FIFO (DDC A, B, C, or D FIFO, depending on the register being accessed). When read as logic '0' the FIFO is not write enabled. When read as logic '1' the FIFO is write enabled.

6.13.2.4 FIFO Status Bits — Bits D03 – D00

Each status bit is a non–latched version of the associated FIFO flag condition. When read as logic '1', the associated FIFO flag condition is active (true). When read as logic '0', the associated FIFO flag condition is inactive. Note that when any status bit changes to logic '1', the corresponding flag bit in this register (Section 6.13.2.1) will also be set to logic '1'.

The Almost Full and Almost Empty FIFO levels are set using the DDC FIFO Almost Full and Almost Empty Level Registers, Sections 6.13.6 and 6.13.7.

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6.13 DDC Registers (continued)

6.13.3 DDC FIFO Interrupt Mask Registers

There are four DDC FIFO Interrupt Mask Registers, one for each DDC Channel, DDC A, DDC B, DDC C, and DDC D. The DDC FIFO Interrupt Mask Registers contain enable bits for each interrupt condition defined. Each bit enables or disables the generation of a local bus interrupt (LINTix) to the PCI7140.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–44: DDC FIFO Interrupt Mask Registers
DDC A FIFO: R/W @ BAR2+0x8C20
DDC B FIFO: R/W @ BAR2+0x8C50
DDC C FIFO: R/W @ BAR2+0x8C80
DDC D FIFO: R/W @ BAR2+0x8CB0

	D15 – D06	D05	D04	D03	D02	D01	D00
Bit Name	Reserved	TRIGGER CAPTURE	Reserved	FULL	ALMOST FULL	ALMOST EMPTY	EMPTY
Function	Write with zeros, Mask when reading	0 = Disable Interrupt 1 = Enable Interrupt					
All bits default to the logic '0' state at power on and reset							

Each bit of this register enables or disables the generation of a local bus interrupt to the PCI7140, when interrupts are enabled for this register in the Application Interrupt Enable LINTx Registers, Section 6.11.4.

Setting the bit associated with a given interrupt to the logic '1' state enables the generation of a local bus interrupt when that interrupt condition occurs. When a bit is cleared to logic '0' (its default state), the local bus interrupt will not be generated by the associated interrupt condition.

The interrupt conditions are:

D05 – Trigger Capture, Trigger Length has been counted down to zero
D03 – FIFO is Full
D02 – FIFO is at the Almost Full level
D01 – FIFO is at the Almost Empty level
D00 – FIFO is Empty

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6.13 DDC Registers (continued)

6.13.4 DDC Post Trigger Count Registers

There are four DDC Post Trigger Count Registers, two each for DDC input channels C and D. These registers specify the delay in writing data samples to the applicable DDC FIFO, after the trigger.

Each channel's delay count is specified using two registers, one for the least significant 16 bits (LSB) and one for the most significant 16 bits (MSB). The following tables show the format of these registers.

Table 6–45: DDC Post Trigger Count LSB Registers
DDCC: R/W @ BAR2+0x88C8
DDCD: R/W @ BAR2+0x88D8

	D15 – D00
Bit Name	D15 – D0
Function	Post Trigger Count least significant bits (LSB)
All bits default to the logic '0' state at power on and reset	

Table 6–46: DDC Post Trigger Count MSB Registers
DDCC: R/W @ BAR2+0x88D0
DDCD: R/W @ BAR2+0x88E0

	D15 – D00
Bit Name	D31– D16
Function	Post Trigger Count most significant bits (MSB)
All bits default to the logic '0' state at power on and reset	

The Post Trigger Count is a 32–bit binary value, with the most significant bit (D31) in bit D15 of the MSB register. This value specifies the number of samples to delay after the trigger before writing to the applicable DDC FIFO. See Section 4.8.4 for additional information on Post Triggering.

NOTE: When specifying a Post Trigger Count for a DDC channel, be sure to write to BOTH registers for that DDC channel.

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6.13 DDC Registers (continued)

6.13.5 DDC Trigger Length Registers

There are eight DDC Trigger Length Registers, two registers for each DDC channel, DDC A, DDC B, DDC C, and DDC D. Each Trigger Length is specified using two registers, one for the least significant 16 bits (LSB) and one for the most significant 16 bits (MSB).

When Trigger mode is selected for a FIFO gate (GATE/TRIG = 1, DDC FIFO Control Register, Section 6.13.1.9), these registers set the length that the gate is active (FIFO writes enabled) after receipt of the trigger.

The following tables show the contents of the Trigger Length Registers.

Table 6–47: DDC Trigger Length LSB Registers
DDC A: R/W @ BAR2+0x8C10
DDC B: R/W @ BAR2+0x8C40
DDC C: R/W @ BAR2+0x8C70
DDC D: R/W @ BAR2+0x8CA0

	D15 – D00
Bit Name	D15 – D0
Function	Trigger Length (N–1) least significant bits (LSB)
All bits default to the logic '0' state at power on and reset	

Table 6–48: DDC Trigger Length MSB Registers
DDC A: R/W @ BAR2+0x8C18
DDC B: R/W @ BAR2+0x8C48
DDC C: R/W @ BAR2+0x8C78
DDC D: R/W @ BAR2+0x8CA8

	D15 – D00
Bit Name	D31– D16
Function	Trigger Length (N–1) most significant bits (MSB)
All bits default to the logic '0' state at power on and reset	

The trigger length is a 32–bit binary value, with the most significant bit (D31) in bit D15 of the MSB register. This value specifies the length of the write gate after the trigger as the number of FIFO writes, up to 65,535. To specify a trigger length of N FIFO writes, set this register to N–1.

See Section 4.8.4 for information on DDC Post Triggering.

NOTE: When specifying a trigger length, be sure to write to BOTH Trigger Length Registers for that DDC channel.

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6.13 DDC Registers (continued)

6.13.6 DDC FIFO Almost Empty Level Registers

There are four DDC FIFO Almost Empty Level Registers, one for each FIFO, DDC A, DDC B, DDC C, and DDC D. This register sets the programmable boundary flag level of the Almost Empty flag for the associated FIFO.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–49: DDC FIFO Almost Empty Level Registers
DDC A FIFO: R/W @ BAR2+0x8C28
DDC B FIFO: R/W @ BAR2+0x8C58
DDC C FIFO: R/W @ BAR2+0x8C88
DDC D FIFO: R/W @ BAR2+0x8CB8

	D15 – D10	D09 – D00
Bit Name	Reserved	D9 – D0
Function	Write with zeros, Mask when reading	FIFO Almost Empty Level
All bits default to the logic '0' state at power on and reset		

The Almost Empty Level is a 10–bit binary value, with bit D09 the MSB. This value specifies the FIFO Almost Empty flag depth.

NOTE: All 7140 FIFOs are 64 bits wide. Thus, the FIFO level programmed into this register indicates the level of 64–bit words. For example, if you set this register to a level of 12, the FIFO sets a boundary flag when the data transfer reaches 24 32–bit words.

While the FIFO is being read, when the data is at or below the Almost Empty level, the FIFO sets the Almost Empty Flag.

- The FIFO Almost Empty Flag is routed to the associated DDC FIFO Status Register, Section 6.13.2.
- If the Almost Empty Flag is enabled by the associated DDC FIFO Interrupt Mask Register, Section 6.13.3, a local bus interrupt will be asserted to the PCI7140.

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6.13 DDC Registers (continued)

6.13.7 DDC FIFO Almost Full Level Registers

There are four DDC FIFO Almost Full Level Registers, one for each FIFO, DDC A, DDC B, DDC C, and DDC D. This register sets the programmable boundary flag level of the Almost Full flag for the associated FIFO.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–50: DDC FIFO Almost Full Level Registers
DDC A FIFO: R/W @ BAR2+0x8C30
DDC B FIFO: R/W @ BAR2+0x8C60
DDC C FIFO: R/W @ BAR2+0x8C90
DDC D FIFO: R/W @ BAR2+0x8CC0

	D15 – D10	D09 – D00
Bit Name	Reserved	D9 – D0
Function	Write with zeros, Mask when reading	FIFO Almost Full Level
All bits default to the logic '0' state at power on and reset		

The Almost Full Level is a 10–bit binary value, with bit D09 the MSB. This value specifies the FIFO Almost Full flag depth.

NOTE: All 7140 FIFOs are 64 bits wide. Thus, the FIFO level programmed into this register indicates the level of 64–bit words. For example, if you set this register to a level of 12, the FIFO sets a boundary flag when the data transfer reaches 24 32–bit words.

While the FIFO is being written to, when the data is at or above the Almost Full level, the FIFO sets the Almost Full Flag.

- The FIFO Almost Full Flag is routed to the associated DDC FIFO Status Register, Section 6.13.2.
- If the Almost Full Flag is enabled by the associated DDC FIFO Interrupt Mask Register, Section 6.13.3, a local bus interrupt will be asserted to the PCI7140.

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6.14 GC4016 Registers

The Graychip GC4016 contains internal programmable status and control registers. The Model 7140 FPGA allocates a block of addresses for registers that allow you to read or write data from/to these GC4016 internal registers.

This address space is split into eight global registers (relative addresses 0–7), eight unused registers (addresses 8–15), and 16 paged registers (addresses 16–31). The global registers are available from each page. Address 2 is the Page Register, which selects which control registers are accessed by addresses 16 through 31.

FPGA Address	CG4016 Register
BAR2+0xC000 to 0xC007	Global Control Registers 0–7
BAR2+0xC008 to 0xC00F	Unused
BAR2+0xC010 to 0xC01F	Paged Registers 16–31

The following table shows the bit layout of each FPGA register. You can read or write one byte at a time to each register.

Table 6–51: GC4016 Registers
R/W @ BAR2+0xC000 to 0xCFFF

	D15 – D08	D07	D06	D05	D04	D03	D02	D01	D00
Bit Name	Not used	D7	D6	D5	D4	D3	D2	D1	D0
Function	Write zeros, Mask read	Eight bits (one byte) of data to/from GC4016							
When reset, including power–up, the state of these registers is unknown.									



When you select a DDC Data Format Mode (DDC FIFO Control Registers, Section 6.13.1), ensure that the GC4016 is configured accordingly using the above GC4016 registers.

NOTE: The minimum decimation factor for each GC4016 channel is normally 32, but can be decreased to 16 or 8 by combining two or four channels on the GC4016 chip using the above GC4016 registers.

Refer to the TI Graychip GC4016 Data Sheet (see Section 1.16) for detailed information on these registers.

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6.15 DAC Registers

The following subsections describe the FPGA registers that control digital to analog output processing, except for the DAC5686. The DAC5686 contains internal programmable status and control registers. All reads and writes to these DAC5686 internal registers use the DAC5686 Registers defined in Section 6.16.

6.15.1 DAC FIFO Control Registers

There are two DAC FIFO Control Registers, one for each DAC56586 input channel, A and B. This register contains bits that select the data packing modes and the source and characteristics of the gates used to control reading data samples from the PCI Interface DAC A and B FIFOs or from the Delay Memory DAC FIFO for the DAC5686.

NOTE: The DAC A FIFO register bit settings also control the same packing modes and operating characteristics of the Delay Memory DAC FIFO (see Figure 6–3 on page 190).

The following table shows the contents of the DAC FIFO Control Registers. The subsections following the table describe the bits in this register.

Table 6–52: DAC FIFO Control Registers
DAC A FIFO: R/W @ BAR2+0x8410
DAC B FIFO: R/W @ BAR2+0x8440

	D15 – D11	D10	D09	D08
Bit Name	Reserved	WORD SWAP *	CHANNEL PACK *	PACK MODE *
Function	Write with zeros, Mask when reading	0 = No Swap 1 = Swap	0 = Enable 1 = Disable	0 = No Pack 1 = Time PacK

	D07	D06	D05	D04	D03	D02	D01	D00
Bit Name	GATE SEL	Reserved	GATE CONTROL	TRIG CLEAR	HOLD MODE	GATE/TRIG	FIFO RESET	FIFO ENABLE
Function	0 = Gate A 1 = Gate B	Write 0, Mask read	0 = Enable 1 = Disable	0 = None 1 = Force Gate Inactive	0 = None 1 = Hold	0 = Gate 1 = Trigger	0 = Run 1 = Reset	0 = Disable 1 = Enable

* Applicable only for DAC A FIFO register
All bits default to the logic '0' state at power on and reset

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6.15 DAC Registers (continued)

6.15.1 DAC FIFO Control Registers (continued)

6.15.1.1 WORD SWAP Bit D10

This bit sets the 16−bit word swapping mode for reading from both DAC FIFOs (this bit is only in the DAC A FIFO register and controls both FIFOs). When the bit is cleared to logic '0' (its default state), the data is not swapped, and the first 16−bit data sample is in the lowest 16 bits of the 64−bit FIFO word. When the bit is set to logic '1', word swapping is enabled and each pair of 16−bit samples are swapped in the 64−bit FIFO word, as follows:

Bits D00:15 are swapped with bits D16:31,
Bits D32:47 are swapped with bits D48:63.

Refer to Section 7.2, FIFO Word Swap Formats, for additional information about the word swap modes.

6.15.1.2 CHANNEL PACK Bit D09

This bit sets the data routing mode for both DAC FIFOs (this bit is only in the DAC A FIFO register and controls both DAC FIFOs). When cleared to logic '0' (its default state), the FPGA reads data samples for both DAC output channels from DAC A FIFO only (Channel Packed). DAC B FIFO is not used in this mode. When set to logic '1', the FPGA reads data samples from each DAC FIFO for the associated DAC channel (DAC A FIFO for DAC channel A, DAC B FIFO for DAC channel B).

NOTE: When the Delay Memory DAC FIFO is routed to the DAC5686 (see Section 6.17.1.2), this bit must be set to '0' (Channel Packed).

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6.15 DAC Registers (continued)

6.15.1 DAC FIFO Control Registers (continued)

6.15.1.3 PACK MODE Bit D08

This bit sets the packing mode for reading from both DAC FIFOs (this bit is only in the DAC A FIFO register and controls both DAC FIFOs).

When PACK MODE is cleared to logic '0' (its default state):

- if CHANNEL PACK (bit D09) is logic '0', four 16–bit samples are read from each 64–bit word of DAC A FIFO (16–bit Channel Packed).
- if CHANNEL PACK is logic '1', two 16–bit samples are read from each 64–bit word of the respective DAC A or B FIFO (Unpacked).

When PACK MODE is set to logic '1':

- if CHANNEL PACK (bit D09) is logic '0', eight 8–bit samples are read from each 64–bit word of DAC A FIFO (8–bit Channel/Time Packed).
- if CHANNEL PACK is logic '1', four 16–bit data samples are read from each 64–bit word of the respective DAC A or B FIFO (16–bit Time Packed).

The settings for the two packing mode bits (D09 & D08) are:

00	16–bit Channel Packed
01	8–bit Channel/Time–Packed
10	16–bit Unpacked
11	16–bit Time–Packed

WORD SWAP, Section 6.15.1.1, can be applied to any of these packing modes. Refer to Section 7.5, DAC Data Routing and Formats.

6.15.1.4 GATE SEL Bit D07

This bit selects the source of the gate for reads from the selected DAC FIFO (DAC FIFO A or B). When the bit is cleared to logic '0' (its default state), Gate A is the source; when the bit is set to logic '1', Gate B is the source.

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6.15 DAC Registers (continued)

6.15.1 DAC FIFO Control Registers (continued)

6.15.1.5 GATE CONTROL Bit D05

This bit enables Gate operation on the selected DAC FIFO (DAC A or DAC B). When the bit is cleared to '0' (the default state), the FIFO is controlled by the Gate (gate control is Enabled). When the bit is set to '1', the FIFO is free running (gate control Disabled).

6.15.1.6 TRIG CLEAR Bit D04

This bit forces the selected gate to the inactive state in Trigger mode (GATE/TRIG bit D02 = 1, below). When this bit is cleared to logic '0' (its default state), there is no effect on the gate. When the bit is set to logic '1', the gate is forced to inactive (DAC FIFO reads disabled), regardless of the trigger length specified (Trigger Length Register, Section 6.15.5), and the TRIGGER CAPTURE bit D05 is cleared in the DAC FIFO Status Register, Section 6.15.2.

6.15.1.7 HOLD MODE Bit D03

This bit enables a gate Hold after the trigger is received in Trigger mode (GATE/TRIG bit D02 = 1, below). When the bit is cleared to logic '0' (its default state), the selected gate is active (DAC FIFO reads enabled) for the specified trigger length after the trigger (specified using the Trigger Length Register, Section 6.15.5), and then goes inactive (DAC FIFO reads disabled). When the bit is set to logic '1', HOLD is enabled and the gate remains active (DAC FIFO reads enabled) after the trigger is received until the Trigger is cleared using the TRIG CLEAR bit D04, above.

Note that when HOLD is enabled, you must set the Trigger Length to any number greater than zero.

6.15.1.8 GATE/TRIG Bit D02

This bit selects Gate or Trigger mode for the gate selected by GATE SEL (bit D07) for enabling DAC FIFO reads. When this bit is cleared to logic '0' (its default state), Gate mode is selected. When this bit is set to logic '1', Trigger mode is selected, and you must set a trigger length using the Trigger Length Register, Section 6.15.5, or enable trigger Hold (HOLD MODE bit D03 above).

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6.15 DAC Registers (continued)

6.15.1 DAC FIFO Control Registers (continued)

6.15.1.9 FIFO RESET Bit D01

This bit resets the selected DAC FIFO (DAC A or DAC B). When the bit is cleared to logic '0' (its default state), the FIFO is in run; when the bit is set to logic '1', the FIFO is in reset.

6.15.1.10 FIFO ENABLE Bit D00

This bit enables the selected DAC FIFO (DAC A or DAC B). When the bit is cleared to logic '0' (its default state), the FIFO is disabled; when the bit is set to logic '1', the FIFO is enabled.

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6.15 DAC Registers (continued)

6.15.2 DAC FIFO Status Registers

There are two DAC FIFO Status Registers, one for each DAC channel (A and B). Each register contains several flag and status bits associated with data transfers to each DAC channel. The following table shows the bit layout of this register. The subsections following the table describe these bits.

Table 6–53: DAC FIFO Status Registers
DAC A FIFO: R/Clr @ BAR2+0x8178
DAC B FIFO: R/Clr @ BAR2+0x8180

	D15 – D12			D11	D10	D09	D08
Bit Name	Reserved			FULL FLAG	ALMOST FULL FLAG	ALMOST EMPTY FLAG	EMPTY FLAG
Function	Write with zeros, Mask when reading			**Read:** 0 = FIFO flag condition not active 1 = FIFO flag condition latched **Clear:** 1 = Clear latch			
	D07 – D06	**D05 ***	**D04 ***	**D03 ***	**D02 ***	**D01 ***	**D00 ***
Bit Name	Reserved	TRIGGER CAPTURE	FIFO WRITE ENABLED	FULL	ALMOST FULL	ALMOST EMPTY	EMPTY
Function	Write with zeros, Mask when reading	0 - Not done 1 - Done	0 - Not En 1 - Enabled	0 = FIFO flag condition not active 1 = FIFO flag condition active			

* These bits are Read Only
When reset, including power–up, the state of this register is unknown.
You should clear the register flag bits before using it, by writing '1's into bits D11 – D08.

6.15.2.1 FIFO Flag Bits — Bits D11 – D08

Read: Each bit latches a FIFO flag occurrence. Logic '1' in any bit indicates that a FIFO flag has been active. Note that when any status bit in this register (Section 6.15.2.4) changes to logic '1', the corresponding flag bit will also be set to logic '1'. However, when a status bit changes from '1' to '0', the corresponding latched bit in this register does not clear, but remains at the logic '1' state.

Clear: Since these bits latch in response to a FIFO flag occur–rence, to detect subsequent FIFO flags, you must clear the bits in this register. To clear any bit in this register that is set to logic '1' you must write a '1' to that bit.

NOTE: These four FIFO flag bits are present only in boards with an FPGA revision date greater that 10/12/05 (see Section 6.8).

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6.15 DAC Registers (continued)

6.15.2 DAC FIFO Status Registers (continued)

6.15.2.2 TRIGGER CAPTURE Bit D05

This bit indicates the trigger capture status of the data transfer (DAC A or B, depending on the register being accessed). When read as logic '0' the trigger has not completed. When read as logic '1' the trigger length is completed.

6.15.2.3 FIFO WRITE ENABLED Bit D04

This bit indicates the write enable status of the FIFO (DAC A or B FIFO, depending on the register being accessed). When read as logic '0' the FIFO is not write enabled. When read as logic '1' the FIFO is write enabled.

6.15.2.4 FIFO Status Bits Bits D03 – D00

Each status bit is a non–latched version of the associated FIFO flag condition. When read as logic '1', the associated FIFO flag condition is active (true). When read as logic '0', the associated FIFO flag condition is inactive.

Note that when any status bit changes to '1', the corresponding flag bit in this register (Section 6.15.2.1) will also be set to '1'. However, when a status bit changes from '1' to '0', the corre–sponding latched bit in this register does not clear, but remains at the logic '1' state.

The Almost Full and Almost Empty FIFO levels are set using the DAC A/B FIFO Almost Full and Almost Empty Level Registers, Sections 6.15.6 and 6.15.7.

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6.15 DAC Registers (continued)

6.15.3 DAC FIFO Interrupt Mask Registers

There are two DAC FIFO Interrupt Mask Registers, one for each DAC channel, A and B. The DAC FIFO Interrupt Mask Registers contain enable bits for each interrupt condition defined. Each bit enables or disables the generation of a local bus interrupt (LINTix) to the PCI7140.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–54: DAC FIFO Interrupt Mask Registers
DAC A FIFO: R/W @ BAR2+0x8428
DAC B FIFO: R/W @ BAR2+0x8458

	D15 – D06	D05	D04	D03	D02	D01	D00
Bit Name	Reserved	TRIGGER CAPTURE	Reserved	FULL	ALMOST FULL	ALMOST EMPTY	EMPTY
Function	Write with zeros, Mask when reading	0 = Disable Interrupt 1 = Enable Interrupt					
All bits default to the logic '0' state at power on and reset							

Each bit of this register enables or disables the generation of a local bus interrupt to the PCI7140, when interrupts are enabled for this register in the Application Interrupt Enable LINTx Registers, Section 6.11.4.

Setting the bit associated with a given interrupt to the logic '1' state enables the generation of a local bus interrupt when that interrupt condition occurs. When a bit is cleared to logic '0' (its default state), the local bus interrupt will not be generated by the associated interrupt condition.

The interrupt conditions are:

D05 – Trigger Capture, Trigger Length has been counted down to zero
D03 – FIFO is Full
D02 – FIFO is at the Almost Full level
D01 – FIFO is at the Almost Empty level
D00 – FIFO is Empty

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6.15 DAC Registers (continued)

6.15.4 DAC Post Trigger Count Registers

There are four DAC Post Trigger Count Registers, two each for DAC output channels A and B. These registers specify the delay in reading data samples from the applicable DAC FIFO, after the trigger.

Each channel's delay count is specified using two registers, one for the least significant 16 bits (LSB) and one for the most significant 16 bits (MSB). The following tables show the format of these registers.

Table 6–55: DAC Post Trigger Count LSB Registers
DACA: R/W @ BAR2+0x88A8
DACB: R/W @ BAR2+0x88B8

	D15 – D00
Bit Name	D15 – D0
Function	Post Trigger Count least significant bits (LSB)
All bits default to the logic '0' state at power on and reset	

Table 6–56: DAC Post Trigger Count MSB Registers
DACA: R/W @ BAR2+0x88B0
DACB: R/W @ BAR2+0x88C0

	D15 – D00
Bit Name	D31– D16
Function	Post Trigger Count most significant bits (MSB)
All bits default to the logic '0' state at power on and reset	

The Post Trigger Count is a 32–bit binary value, with the most significant bit (D31) in bit D15 of the MSB register. This value specifies the number of samples to delay after the trigger before reading from the applicable DAC FIFO. See Section 4.8.4 for additional information on Post Triggering.

NOTE: When specifying a Post Trigger Count for a DAC channel, be sure to write to BOTH registers for that DAC channel.

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6.15 DAC Registers (continued)

6.15.5 DAC Trigger Length Registers

There are four DAC Trigger Length Registers, two registers for each DAC channel, A and B. Each trigger length is specified using two registers, one for the least significant 16 bits (LSB) and one for the most significant 16 bits (MSB).

When Trigger mode is selected for a FIFO gate (GATE/TRIG = 1, DAC FIFO Control Register, Section 6.15.1.8), these registers set the length that the gate is active (DAC FIFO reads enabled) after receipt of the trigger.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–57: DAC Trigger Length LSB Registers
DAC A: R/W @ BAR2+0x8418
DAC B: R/W @ BAR2+0x8448

	D15 – D00
Bit Name	D15 – D0
Function	Trigger Length (N–1) least significant bits (LSB)
All bits default to the logic '0' state at power on and reset	

Table 6–58: DAC Trigger Length MSB Registers
DAC A: R/W @ BAR2+0x8420
DAC B: R/W @ BAR2+0x8450

	D15 – D00
Bit Name	D31– D16
Function	Trigger Length (N–1) most significant bits (MSB)
All bits default to the logic '0' state at power on and reset	

The trigger length is a 32–bit binary value, with the most significant bit (D31) in bit D15 of the MSB register. This value specifies the length of the read gate after the trigger as the number of FIFO reads, up to 65,535. To specify a trigger length of N FIFO reads, set this register to N–1.

See Section 4.8.4 for information on DAC Post Triggering.

NOTE: When specifying a trigger length, be sure to write to BOTH Trigger Length Registers for that DAC channel.

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6.15 DAC Registers (continued)

6.15.6 DAC FIFO Almost Empty Level Registers

There are two DAC FIFO Almost Empty Level Registers, one for each FIFO, DAC A and DAC B. This register sets the programmable boundary flag level of the Almost Empty flag for the associated DAC FIFO.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–59: DAC FIFO Almost Empty Level Registers
DAC A FIFO: R/W @ BAR2+0x8430
DAC B FIFO: R/W @ BAR2+0x8460

	D15 – D14	D13 – D00
Bit Name	Reserved	D13 – D0
Function	Write with zeros, Mask when reading	FIFO Almost Empty Level
All bits default to the logic '0' state at power on and reset		

The Almost Empty Level is a 14–bit binary value, with bit D13 the MSB. This value specifies the FIFO Almost Empty flag depth.

NOTE: All 7140 FIFOs are 64 bits wide. Thus, the FIFO level programmed into this register indicates the level of 64–bit words. For example, if you set this register to a level of 12, the FIFO sets a boundary flag when the data transfer reaches 24 32–bit words.

While the FIFO is being read, when the data is at or below the Almost Empty level, the FIFO sets the Almost Empty Flag.

- The FIFO Almost Empty Flag is routed to the associated DAC FIFO Status Register, Section 6.15.2.
- If the Almost Empty Flag is enabled by the associated DAC FIFO Interrupt Mask Register, Section 6.15.3, a local bus interrupt will be asserted to the PCI7140.

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6.15 DAC Registers (continued)

6.15.7 DAC FIFO Almost Full Level Registers

There are two DAC FIFO Almost Full Level Registers, one for each FIFO, DAC A and DAC B. This register sets the programmable boundary flag level of the Almost Full flag for the associated DAC FIFO.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–60: DAC FIFO Almost Full Level Registers
DAC A FIFO: R/W @ BAR2+0x8438
DAC B FIFO: R/W @ BAR2+0x8468

	D15 – D14	D13 – D00
Bit Name	Reserved	D13 – D0
Function	Write with zeros, Mask when reading	FIFO Almost Full Level
All bits default to the logic '0' state at power on and reset		

The Almost Full Level is a 14–bit binary value, with bit D13 the MSB. This value specifies the FIFO Almost Full flag depth.

NOTE: All 7140 FIFOs are 64 bits wide. Thus, the FIFO level programmed into this register indicates the level of 64–bit words. For example, if you set this register to a level of 12, the FIFO sets a boundary flag when the data transfer reaches 24 32–bit words.

While the FIFO is being written to, when the data is at or above the Almost Full level, the FIFO sets the Almost Full Flag.

- The FIFO Almost Full Flag is routed to the associated DAC FIFO Status Register, Section 6.15.2.
- If the Almost Full Flag is enabled by the associated DAC FIFO Interrupt Mask Register, Section 6.15.3, a local bus interrupt will be asserted to the PCI7140.

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6.15 DAC Registers (continued)

6.15.8 DAC Control/Status Register

The DAC Control/Status Register provides several control and status bits that control the interface to the DAC5686.

The DAC5686 contains internal programmable status and control registers. All reads and writes to these DAC5686 internal registers are programmed using the DAC5686 Registers defined in Section 6.16.

The following table shows the contents of the DAC Control/Status Register. The subsections following the table describe the use of each bit.

Table 6–61: DAC Control/Status Register
R/W @ BAR2+0x8408

	D15 – D04	D03	D02	D01	D00 *
Bit Name	Reserved	DAC CLK	PLL VDD	DAC RESET	PLL LOCK
Function	Write with zeros	0 = Select 1 = Bypass	0 = Disable 1 = Enable	0 = Run 1 = Reset	0 = Unlocked 1 = Locked

* This bit is Read Only
Bits D03 to D01 default to the logic '0' state at power on and reset.

6.15.8.1 DAC CLK Bit D03

This bit selects the clock source for the DAC FIFOs. When the bit is cleared to logic '0' (its default state), the clock output from the DAC5686 PLLLOCK pin is routed to the DAC FIFOs. When set to logic '1', the clock output from the PLLLOCK pin of DAC5686 is bypassed and the module's clock (selected by CLK SRC, Master Bus A/B Control Register, Section 6.10.1 or 6.10.4) is routed to the DAC FIFOs.

The following table shows the valid states for the PLLLOCK pin.

Table 6–62: DAC Control/Status Register States

DAC CLK (D03)	PLL VDD (D02)	PLL LOCK (D00)	Condition
0	0	invalid	DAC clock from PLLLOCK pin is selected. PLL is disabled.
0	1	valid	Invalid DAC CLK and PLL VDD selection.
1	0	invalid	DAC clock from PLLLOCK pin is bypassed. PLL is disabled. Used for DAC dual clock/full bypass modes.
1	1	valid	DAC clock from PLLLOCK pin is bypassed. PLL is enabled.

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6.15 DAC Registers (continued)

6.15.8 DAC Control/Status Register (continued)

6.15.8.2 PLL VDD Bit D02

This bit enables the PLL supply voltage on the DAC5686. When the bit is cleared to logic '0' (its default state), the PLL is disabled on the DAC5686. When set to logic '1', the PLL is enabled on the DAC5686. When PLL VDD is enabled, the PLLLOCK pin indicates lock status (Section 6.15.8.4) and DAC CLK (above) must be set to Bypass.

6.15.8.3 DAC RESET Bit D01

This bit issues a reset to the DAC5686. When the bit is cleared to logic '0' (its default state), the DAC is in a normal run state. When the bit is set to logic '1', the DAC is in reset.

6.15.8.4 PLL LOCK Bit D00

This read−only bit is the status of the PLLLOCK pin on the DAC5686. The PLLLOCK pin output is only valid when PLL VDD is enabled (bit D03 set to logic '1'). Refer to the DAC5686 data sheet (see Section 1.16) for description of PLL Mode operation.

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6.16 DAC5686 Registers

The DAC5686 chip contains internal programmable status and control registers. All reads and writes to these DAC5686 internal registers are programmed through the Model 7140 FPGA. You can read and write data to the DAC5686 using the Model 7140 DAC Registers defined in the FPGA.

The FPGA defines two DAC Registers, one for read accesses (DAC Read Register) and one for write accesses (DAC Write Register). The formats of these DAC Registers are provided in Sections 6.16.1 and 6.16.2, respectively, on the following two pages.

Each DAC Write Register access to the DAC5686 internal registers consists of data and a register address offset value to steer the data to the correct internal register. There are 16 DAC5686 internal registers that can be accessed in this manner. The offset values of these internal registers are provided in Section 6.16.3.

Writing data to a DAC5686 internal register is a single step.

- Write to the DAC Write Register (Section 6.16.2) with DATA DIRECTION = 0, REG OFFSET [4:0] = the offset of the DAC5686 internal register, DATA [7:0] = the data to be written, and the remaining bits = 0.

Reading a DAC5686 internal register consists of two steps.

1) First, write to the DAC Write Register (Section 6.16.2) with DATA DIRECTION = 1, REG OFFSET [4:0] = the offset of the DAC5686 internal register, and the remaining bits = 0. This identifies, to the DAC5686, the address of the register to be accessed during the read operation.

2) Then, read the DAC Read Register (Section 6.16.1). The value of the identified DAC5686 internal register is contained in DATA [7:0], where STATUS = 0 indicates a valid value.

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6.16 DAC5686 Registers (continued)

6.16.1 DAC Read Register

The following table shows the contents of the DAC Read Register, and the paragraphs following this table provide descriptions of these bits.

Table 6–63: DAC Read Register
R.O. @ BAR2+0x8470

	D15	D14	D13	D12	D11	D10	D09	D08
Bit Name	STATUS	Reserved						
Function	0 = Valid 1 = Busy	Mask when reading						
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
Function	Data read from the DAC register (when STATUS = 0)							
All bits default to the logic '0' state at power on and reset.								

6.16.1.1 STATUS Bit D15

This bit indicates the read/write status of the DAC registers.

When you write to the DAC Write Register, Section 6.16.2, this bit goes to logic '1' while the data is sent (serially). If you requested a Read (by setting Bit D15 = 1 in the DAC Write Register), this STATUS bit stays at '1' until the read from the DAC is complete.

When this STATUS bit reads logic '0', both registers are not busy, and if the DAC Write Register was set for a Read (Bit D15 = 1 in the DAC Write Register) the DATA bits contain valid data read from the DAC5686 internal register.

6.16.1.2 DATA Bits D7 to D0

These bits contains the data read from the DAC5686 internal register selected by the DAC Write Register, Section 6.16.2. This data is valid only when STATUS, bit D15, = 0.

NOTE: Before you can access a DAC register, you must set the **sif4** bit in the **config_msb** DAC register, and specify a register offset to read, using the DAC Write Register.

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6.16 DAC5686 Registers (continued)

6.16.2 DAC Write Register

The following table shows the contents of the DAC Write Register, and the paragraphs following this table provide descriptions of these bits.

Table 6–64: DAC Write Register
W.O. @ BAR2+0x8478

	D15	D14	D13	D12	D11	D10	D09	D08
Bit Name	DATA DIRECTION	N1	N0	REG OFFSET 4	REG OFFSET 3	REG OFFSET 2	REG OFFSET 1	REG OFFSET 0
Function	0 = Write 1 = Read	Write with zeros		Offset of DAC register to write to				
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
Function	When DATA DIRECTION = 0, data to write to the DAC register at offset REG OFFSET[4..0]. When DATA DIRECTION = 1, these bits are do not care.							
All bits default to the logic '0' state at power on and reset.								

6.16.2.1 DATA DIRECTION — Bit D15

This bit indicates the read/write direction of the DATA [7:0] bits. Clear this bit to logic '0' (its default state) to indicate the DATA bits contain a valid value to write to the specified DAC5686 internal register. Set the bit to logic '1' to indicate the DATA bits are do not care, and the REG OFFSET is for a subsequent read by the DAC Read Register, Section 6.16.2.

6.16.2.2 N1, N0 — Bits D14 to D13

These bits must be cleared to logic '0' (their default state).

6.16.2.3 REG OFFSET — Bits D12 to D8

Set these bits to the (address) offset of the DAC5686 internal register (see Table 6–65, page 188) to write to.

6.16.2.4 DATA — Bits D7 to D0

These bits contain data to write to the DAC5686 internal register. This data is valid only when DATA DIRECTION, bit D15, = 0.

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6.16 DAC5686 Registers (continued)

6.16.3 DAC5686 Internal Registers

There are 16 DAC5686 internal registers that can be accessed from a base–board processor using the preceding Model 7140 DAC Read and Write Reg–isters. Refer to the Texas Instruments DAC5686 data sheet (see Section 1.16) for descriptions of these registers.

Each access to the DAC5686 internal registers requires an address offset value (see DAC Read and Write Registers, Table 6–63 and Table 6–64) to steer the data access to the correct register. The following table lists the DAC5686 internal registers, showing their address offsets (REG OFFSET).

Table 6–65: DAC5686 Internal Registers

DAC5686 Register	Address Offset (REG OFFSET)
chip_ver	0x00
freq_lsb	0x01
freq_lmidsb	0x02
freq_umidsb	0x03
freq_msb	0x04
phase_lsb	0x05
phase_msb	0x06
config_lsb	0x07
config_msb	0x08
config_usb	0x09
daca_offset_lsb	0x0A
daca_gain_lsb	0x0B
daca_offset_gain_msb	0x0C
dacb_offset_lsb	0x0D
dacb_gain_lsb	0x0E
dacb_offset_gain_msb	0x0F

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6.17 Delay Memory Registers

The following subsections describe the FPGA registers that control the Delay Memory operations. See Figure 6–3 on the next page for illustration of the Delay Memory Control logic.

6.17.1 Delay Memory Control Register

The Delay Memory Control register contains bits that select the source and destination and control the operation of all Delay Memory data transfers. See Section 4.7 for additional information on Delay Memory Operation.

The following table shows the contents of the Delay Memory Control Register. The subsections following the table provide descriptions of the bits in this register.

Table 6–66: Delay Memory Control Register
R/W @ BAR2+0x8800

	D15 – D14		D13	D12	D11	D10	D09	D08
Bit Name	Reserved		DDC D SOURCE	DDC C SOURCE	Reserved	DAC SOURCE	Reserved	Reserved
Function	Write with zeros, Mask when reading		0 = ADC2 1 = Memory	0 = ADC1 1 = Memory	Write 0, Mask read	0 = DAC FIFO 1 = Memory	Write 0, Mask read	Write 0, Mask read
	D07	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
Bit Name	Reserved	BANK 2 ENABLE	BANK 1 ENABLE	BANK 0 ENABLE	Reserved	BANK R/W	BANK SELECT	
Function	Write 0, Mask read	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Disable 1 = Enable	Write 0, Mask read	0 = Read 1 = Write	See Section 6.17.1.5	
All bits default to the logic '0' state at power on and reset								

6.17.1.1 DDC x SOURCE — Bits D13, D12

Each of these bits selects the source for a GC4016 DDC input data channel (DDC channel D or DDC channel C, depending on the bit accessed). When cleared to logic '0' (the default state) the associated ADC channel is routed directly to a GC4016 DDC input channel (ADC1 to GC4016 DDC C input, or ADC2 to GC4016 DDC D input). When set to logic '1' the associated Delay Memory FIFO (DDCC or DDCD) is routed to the DDC input.

Note that ADC channels 1 and 2 are always routed to GC4016 DDC input channels A and B respectively in addition to this switched input.

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6.17 Delay Memory Registers (continued)

6.17.1 Delay Memory Control Register (continued)

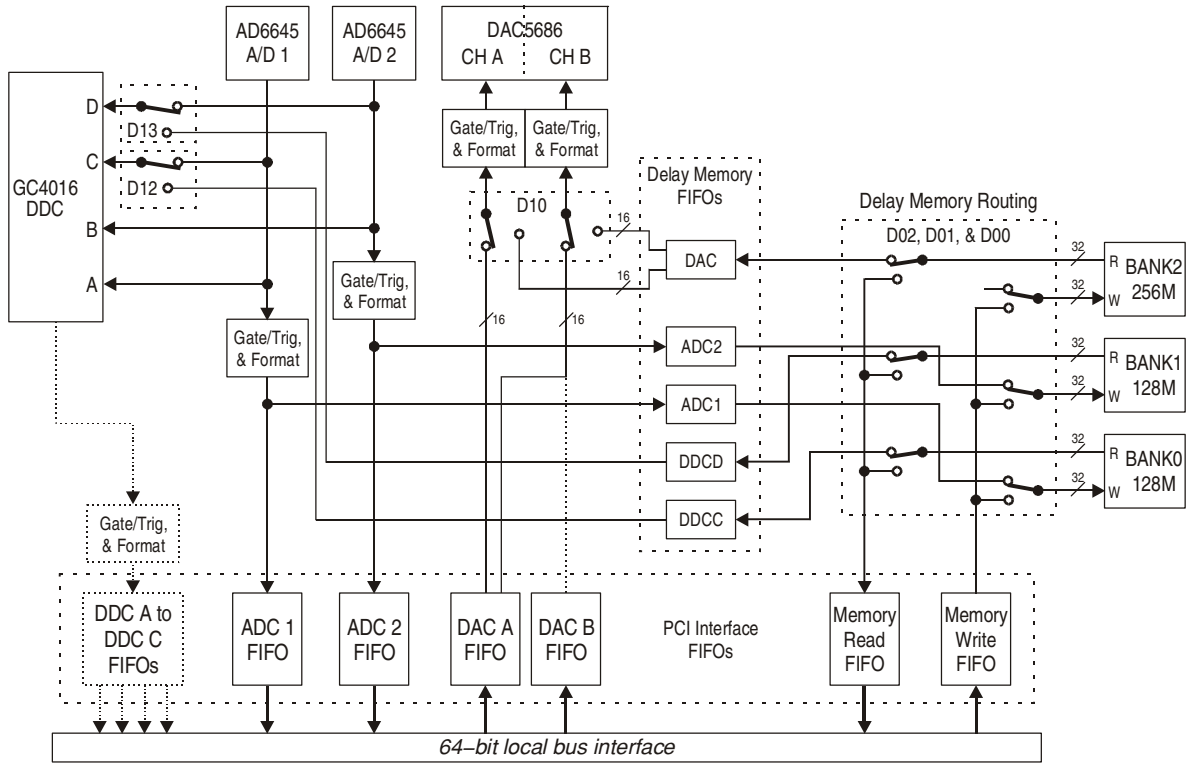


Figure 6–3: Delay Memory Control Logic
(Delay Memory Control Register bits indicated by Dxx – default position shown)



Refer to Section 6.12.1 for setup and control of the Delay Memory ADC FIFOs.
Refer to Section 6.13.1 for setup and control of the Delay Memory DDC FIFOs.
Refer to Section 6.15.1 for setup and control of the Delay Memory DAC FIFOs.

6.17.1.2 DAC SOURCE Bits D10

This bit selects the source for the DAC5686 output channels (both DACA and DACB). When cleared to logic '0' (the default state) the PCI interface DAC FIFOs are routed to the two DAC5686 channels. When set to logic '1' the Delay Memory Bank (DAC FIFO) is routed to the two DAC5686 channels. When set to '1' (Memory), you must set the CHANNEL PACK mode bit in the DAC A FIFO register to '0' (Channel Packed), Section 6.15.1.2.

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6.17 Delay Memory Registers (continued)

6.17.1 Delay Memory Control Register (continued)

6.17.1.3 BANK x ENABLE — Bits D06, D05, D04

Each of these bits enables operation of the respective memory bank (0, 1, or 2 depending on the bit accessed). When cleared to logic '0' (the default state) the bank is Disabled. When set to logic '1' the bank is Enabled and the data transfer specified for that memory bank is initiated, starting with a memory bank read, fol–lowed by a memory bank write.

NOTE: Before you change the Delay Memory Bank settings in bits D02, D01, or D00, you must first Disable the associated memory bank using the applicable BANK ENABLE bit. After making such a change, then Enable that memory bank.

6.17.1.4 BANK R/W — Bit D02

This bit selects the direction of data transfer, using the Memory Read or Memory Write FIFO, for the delay memory bank selected in the BANK SELECT bits, D01:D00, below. When cleared to logic '0' (the default state) the transfer is a read from the selected memory bank using the Memory Read PCI interface FIFO. When set to logic '1' the transfer is a write to the selected memory bank using the Memory Write PCI interface FIFO.

6.17.1.5 BANK SELECT — Bits D01, D00

These two bits select the delay memory bank for the Memory Read or Memory Write FIFO data transfer. The settings for these two bits are:

00	none (default)
01	BANK 0
10	BANK 1
11	BANK 2

The direction of the data transfer, and the PCI interface FIFO used, are specified using the BANK R/W bit, D02, above. Note that when you access a selected memory bank with the Memory Read or Memory Write FIFO you can only perform one memory bank transfer at a time, either read or write, and you cannot access that memory bank from any other device.

See Table 6–67 on the next page for the possible delay memory bank data routing paths.

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6.17 Delay Memory Registers (continued)

6.17.1 Delay Memory Control Register (continued)

Data routing through the delay memory banks is as follows:

Table 6–67: Delay Memory Bank Data Paths

D02	D01	D00	Memory Bank Writes	Memory Bank Reads
0	0	0	ADC1 to BANK 0 ADC2 to BANK 1	BANK 0 to DDCC BANK 1 to DDCD BANK 2 to DACA/DACB
0	0	1	ADC2 to BANK 1	BANK 0 to Mem. Read FIFO BANK 1 to DDCD BANK 2 to DACA/DACB
0	1	0	ADC1 to BANK 0	BANK 0 to DDCC BANK 1 to Mem. Read FIFO BANK 2 to DACA/DACB
0	1	1	ADC1 to BANK 0 ADC2 to BANK 1	BANK 0 to DDCC BANK 1 to DDCD BANK 2 to Mem. Read FIFO
1	0	0	ADC1 to BANK 0 ADC2 to BANK 1	BANK 0 to DDCC BANK 1 to DDCD BANK 2 to DACA/DACB
1	0	1	Mem. Write FIFO to BANK 0 ADC2 to BANK 1	BANK 1 to DDCD BANK 2 to DACA/DACB
1	1	0	ADC1 to BANK 0 Mem. Write FIFO to BANK 1	BANK 0 to DDCC BANK 2 to DACA/DACB
1	1	1	ADC1 to BANK 0 ADC2 to BANK 1 Mem. Write FIFO to BANK 2	BANK 0 to DDCC BANK 1 to DDCD



The ADC FIFO register settings, Section 6.12.1, control the packing modes and operating characteristics of the Delay Memory ADC FIFOs (see Figure 6–3). Thus, note the following settings for the ADC FIFOs:

1) If you enable a Delay Memory Bank for transfer from an ADC channel, you must also 'Enable' the associated ADC FIFO, Section 6.12.1.

2) For transfers from an ADC channel to Delay Memory, you should set PACK MODE to 'Pack' for the associated ADC FIFO, Section 6.12.1.

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6.17 Delay Memory Registers (continued)

6.17.2 Delay Memory Depth Registers

There are six Delay Memory Depth Registers, two registers for each memory bank, 0, 1, and 2. These registers specify the amount of 32–bit words in each memory bank, in 8–word increments, to be used for data input and output.

Each memory bank's depth is specified using two registers, one for the least significant 16 bits (LSB) and one for the most significant 16 bits (MSB). The following tables show the contents of these registers.

Table 6–68: Delay Memory Depth LSB Registers
Bank 0: R/W @ BAR2+0x8808
Bank 1: R/W @ BAR2+0x8818
Bank 2: R/W @ BAR2+0x8828

	D15 – D03	D02 – D00
Bit Name	D15 – D3	D2 – D0
Function	Memory Bank Depth least significant bits (LSB)	Must write zeros
All bits default to the logic '0' state at power on and reset		

Table 6–69: Delay Memory Depth MSB Registers
Bank 0: R/W @ BAR2+0x8810
Bank 1: R/W @ BAR2+0x8820
Bank 2: R/W @ BAR2+0x8830

	D15 – D00
Bit Name	D31– D16
Function	Memory Bank Depth most significant bits (MSB)
All bits default to the logic '0' state at power on and reset	

The Memory Bank Depth is a 32–bit binary value, with the most significant bit (D31) in bit D15 of the MSB register. This value specifies the number of 32–bit words, in multiples of eight words, up to a maximum of 33,554,432 (**0x0200 0000**) words in Bank 0 or 1, or a maximum of 67,108,864 (**0x0400 0000**) words in Bank 2.

A Memory Bank Depth value of 0 (**0x0**) is not valid.

NOTE: When specifying a Memory Bank Depth for a memory bank, be sure to write to BOTH registers for that bank.

The use of these registers is described on the following page.

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6.17 Delay Memory Registers (continued)

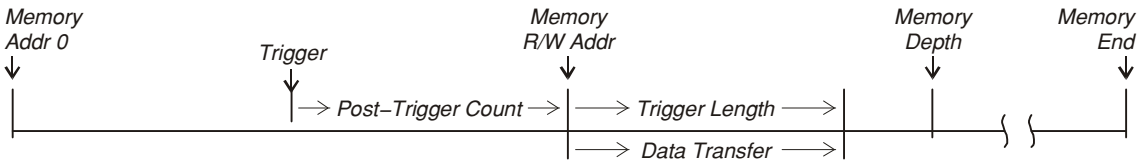
6.17.2 Delay Memory Depth Registers (continued)

Using the default ADC to memory bank to DDC data path, Section 6.17.1, the Delay Memory Depth Registers specify the number of samples to delay ADC data inputs through memory bank 1 or 2 to the DDC input channels. After a memory bank is Enabled (Section 6.17.1.3), the 7140 initiates the designated data transfer for that memory bank, starting with a memory bank read, followed by a memory bank write. This read–then–write sequence repeats until the specified Memory Bank Depth is reached, where the data read/write restarts at the specified starting address of the memory bank. This data transfer sequence will continue indefinitely, recycling through the memory bank, until the memory bank is disabled.

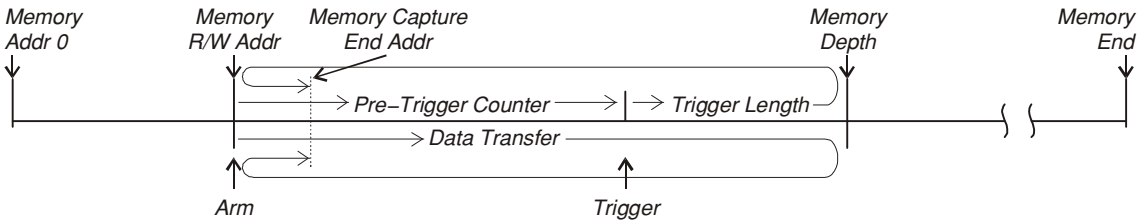
When a memory bank is accessed by a Memory Read or Memory Write PCI interface FIFO, the Memory Bank Depth specifies only the length of the data input or output since you cannot access that memory bank from another device while you are reading or writing from the PCI interface FIFO.

Note that the Memory Bank Depth must be large enough to accommodate the data transfer specified by the Trigger Length. Two types of triggering are provided for ADC and DAC FIFOs, Pre–Trigger and Post–Trigger.

- Post–Triggering – With Post–Triggering (the default), the data transfer starts at the R/W Address at the end of the Post–Trigger count (if there is one), and continues until the end of the Trigger Length.



- Pre–Triggering (ADC channels to Memory only) – In Pre–Triggering, data storage starts at the R/W Address when the ADC FIFO is ARMed and continues, wrapping around at the Memory Bank Depth, until the end of the Trigger Length. The Memory Capture End Address, Section 6.17.4, reports the address of the last data sample stored. (Note that the pre–trigger data storage may wrap around multiple times prior to receipt of the trigger—only one wrap around is illustrated below).



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6.17 Delay Memory Registers (continued)

6.17.3 Delay Memory R/W Address Registers

There are six Delay Memory R/W Address Registers, two registers for each memory bank, 0, 1, and 2. These registers specify the starting address, in 32–bit words, of the data to be read from or written to the respective memory bank, in 8–word increments.

Each memory bank's address is specified using two registers, one for the least significant 16 bits (LSB) and one for the most significant 16 bits (MSB). The following tables show the format of these registers.

Table 6–70: Delay Memory R/W Address LSB Registers
Bank 0: R/W @ BAR2+0x8838
Bank 1: R/W @ BAR2+0x8848
Bank 2: R/W @ BAR2+0x8858

	D15 – D00	D02 – D00
Bit Name	D15 – D0	D2–D0
Function	Memory Bank Address least significant bits (LSB)	Must be zero
All bits default to the logic '0' state at power on and reset		

Table 6–71: Delay Memory R/W Address MSB Registers
Bank 0: R/W @ BAR2+0x8840
Bank 1: R/W @ BAR2+0x8850

	D15 – D10	D09 – D00
Bit Name	D31 – D26	D25– D16
Function	Must be zero	Memory Bank Address most significant bits (MSB)
Bank 2: R/W @ BAR2+0x8860		
	D15 – D11	**D10 – D00**
Bit Name	D31 – D27	D26– D16
Function	Must be zero	Memory Bank Address most significant bits (MSB)
All bits default to the logic '0' state at power on and reset		

Memory Bank Address is a 26–bit (Banks 0 and 1) or 27–bit (Bank 2) binary value, with the most significant bit in bit 9 or 10 of the MSB register.

NOTE: When specifying a Memory Bank Address for a memory bank, be sure to write to BOTH registers for that bank.

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6.17 Delay Memory Registers (continued)

6.17.3 Delay Memory R/W Address Registers (continued)

For Memory Write transfers, these bank registers specify the address to start writing data to the memory bank. For Memory Read transfers, these registers specify the address to start reading data from the memory bank.

NOTE: This address must be within the Memory Bank Depth specified for the associated memory bank by the Delay Memory Depth Registers, Section 6.17.2.

The address applied to these address registers is a 32−bit offset from the memory base, in steps of eight 32−bit words. The upper six bits (Banks 0 and 1) or five bits (Bank 2) must be set to zero. For example, to define a block of memory that starts 2048 bytes from the base of the memory, the R/W address registers would be set to 0x0200 (512). The next start address that could be set would be 0x208 (520), or 2080 bytes from the base.

The Delay Memory Depth Registers are also set with 32−bit values, with a step size of eight 32−bit words. For example, to define a 4096 byte block of memory that starts 2048 bytes from the base of memory, the R/W address registers would be set to 0x0200 (512) and the depth registers would be set to 0x0400 (1024). If the start address and depth results in a memory block that extends past the end of memory, the block of memory available will be from the current start address to the physical end of memory.

Once start and depth are defined, all memory accesses are restricted to that block of memory.

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6.17 Delay Memory Registers (continued)

6.17.4 Delay Memory Capture End Address Registers

There are four Delay Memory Capture End Address Registers, two registers for each ADC input channel, 1 and 2. Each read–only register reports the memory address of the last data sample stored in the applicable delay memory bank (Bank 0 for ADC1, Bank 1 for ADC2) after the completion of the transfer (at the end of the Trigger Length specified).

Each memory bank's end address is reported using two registers, one for the least significant 16 bits (LSB) and one for the most significant 16 bits (MSB). The following tables show the format of these registers.

Table 6–72: Delay Memory Capture End Address LSB Registers
ADC 1 / Bank 0: R.O. @ BAR2+0x8868
ADC 2 / Bank 1: R.O. @ BAR2+0x8878

	D15 – D00
Bit Name	D15 – D0
Function	Delay Memory End Address least significant bits (LSB)
All bits default to the logic '0' state at power on and reset	

Table 6–73: Delay Memory Capture End Address MSB Registers
ADC 1 / Bank 0: R.O. @ BAR2+0x8870
ADC 2 / Bank 1: R.O. @ BAR2+0x8880

	D15 – D00
Bit Name	D31– D16
Function	Delay Memory End Address most significant bits (MSB)
All bits default to the logic '0' state at power on and reset	

The Delay Memory End Address is a 32–bit binary value, with the most sig–nificant bit (D31) in bit D15 of the MSB register. This value specifies the last memory bank address that was written, from the associated ADC channel, at the end of the trigger length specified by the ADC FIFO Trigger Length Registers, Section 6.12.6.

Note that these registers are only valid for data transfers from an ADC input channel to the associated delay memory bank (Bank 0 for ADC1, Bank 1 for ADC2).

NOTE: When specifying a Capture End Address for an ADC channel, be sure to write to BOTH registers for that channel/memory bank.

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6.17 Delay Memory Registers (continued)

6.17.5 Delay Memory 2 Last Address Registers

There are two Delay Memory 2 Last Address Registers. Each read–only register reports the memory address of the last data sample stored in the Delay Memory Bank 2 after the completion of a transfer from the Memory Write PCI interface FIFO.

These registers are valid only for data transfers from the Memory Write FIFO to Delay Memory Bank 2.

This address is reported using two registers, one for the least significant 16 bits (LSB) and one for the most significant 16 bits (MSB). The following tables show the format of these registers.

Table 6–74: Delay Memory 2 Last Address LSB Register
Bank 2: R.O. @ BAR2+0x8908

	D15 – D00
Bit Name	D15 – D0
Function	Delay Memory 2 Last Address least significant bits (LSB)
All bits default to the logic '0' state at power on and reset	

Table 6–75: Delay Memory 2 Last Address MSB Register
Bank 2: R.O. @ BAR2+0x8910

	D15 – D00
Bit Name	D31– D16
Function	Delay Memory 2 Last Address most significant bits (MSB)
All bits default to the logic '0' state at power on and reset	

The Delay Memory 2 Last Address is a 32–bit binary value, with the most significant bit (D31) in bit D15 of the MSB register. This value specifies the last memory bank address that was written to Bank 2 from the Memory Write FIFO.

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6.17 Delay Memory Registers (continued)

6.17.6 Delay Memory Trigger Address Registers

There are four Delay Memory Trigger Registers, two registers for each memory bank, 0 and 1. Each read–only register reports the starting memory address in the Delay Memory Bank at receipt of the trigger for a transfer to the Memory Read PCI interface FIFO.

These registers are valid only for data transfers from Delay Memory Bank 0 or 1 to the Memory Read FIFO.

This address is reported using two registers, one for the least significant 16 bits (LSB) and one for the most significant 16 bits (MSB). The following tables show the format of these registers.

Table 6–76: Delay Memory Trigger Address LSB Registers
Bank 0: R.O. @ BAR2+0x8918
Bank 1: R.O. @ BAR2+0x8928

	D15 – D00
Bit Name	D15 – D0
Function	Delay Memory Trigger Address least significant bits (LSB)
All bits default to the logic '0' state at power on and reset	

Table 6–77: Delay Memory Trigger Address MSB Registers
Bank 0: R.O. @ BAR2+0x8920
Bank 1: R.O. @ BAR2+0x8930

	D15 – D00
Bit Name	D31– D16
Function	Delay Memory Trigger Address most significant bits (MSB)
All bits default to the logic '0' state at power on and reset	

The Delay Memory Trigger Address is a 32–bit binary value, with the most significant bit (D31) in bit D15 of the MSB register. This value specifies the starting memory bank address at receipt of the trigger for a transfer from this memory bank to the Memory Read PCI interface FIFO.

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6.17 Delay Memory Registers (continued)

6.17.7 Delay Memory FIFO Control Registers

There are two FIFO Control Registers for the Delay Memory, one each for the Delay Memory Read and Delay Memory Write FIFOs. Each register contains bits that control the Delay Memory FIFO.

The following table shows the contents of these registers. The subsections following the table provide descriptions of the bits in this register.

Table 6–78: Delay Memory FIFO Control Registers
Delay Memory Read FIFO: R/W @ BAR2+0x8D58
Delay Memory Write FIFO: R/W @ BAR2+0x8D88

	D15 – D02	D01	D00
Bit Name	Reserved	FIFO RESET	FIFO ENABLE
Function	Write with zeros, Mask when reading	0 = Run 1 = Reset	0 = Disable 1 = Enable
All bits default to the logic '0' state at power on and reset			

6.17.7.1 FIFO RESET Bit D01

This bit resets the Delay Memory Read or Delay Memory Write FIFO. When the bit is cleared to logic '0' (its default state), the FIFO is in run; when the bit is set to logic '1', the FIFO is in reset.

6.17.7.2 FIFO ENABLE Bit D00

This bit enables the Delay Memory Read or Delay Memory Write FIFO. When the bit is cleared to logic '0' (its default state), the FIFO is disabled; when the bit is set to logic '1', the FIFO is enabled.

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6.17 Delay Memory Registers (continued)

6.17.8 Delay Memory FIFO Status Registers

There are two Delay Memory FIFO Status Registers, one each for the Delay Memory Read and Delay Memory Write FIFOs. Each register has several flag and status bits associated with the respective Delay Memory FIFO. The following table shows the bit layout of this register. The subsections following the table provide descriptions of these bits.

Table 6–79: Delay Memory FIFO Status Registers
Delay Memory Read FIFO: R/Clr @ BAR2+0x8188
Delay Memory Write FIFO: R/Clr @ BAR2+0x8190

	D15 – D12	D11	D10	D09	D08
Bit Name	Reserved	FULL FLAG	ALMOST FULL FLAG	ALMOST EMPTY FLAG	EMPTY FLAG
Function	Write with zeros, Mask when reading	**Read:** 0 = FIFO flag condition not active 1 = FIFO flag condition latched **Clear:** 1 = Clear latch			
	D07 – D04	**D03 ***	**D02 ***	**D01 ***	**D00 ***
Bit Name	Reserved	FULL	ALMOST FULL	ALMOST EMPTY	EMPTY
Function	Write with zeros, Mask when reading	0 = FIFO flag condition not active 1 = FIFO flag condition active			

* These bits are Read Only
When reset, including power–up, the state of this register is unknown.
You should clear the register flag bits before using it, by writing '1's into bits D11 – D08.

6.17.8.1 FIFO Flag Bits — Bits D11 – D08

Read: Each bit latches a FIFO flag occurrence. Logic '1' in any bit indicates that a FIFO flag has been active. Note that when any status bit in this register (Section 6.17.8.2) changes to logic '1', the corresponding flag bit will also be set to logic '1'. However, when a status bit changes from '1' to '0', the corresponding latched bit in this register does not clear, but remains at the logic '1' state.

Clear: Since these bits latch in response to a FIFO flag occurrence, to detect subsequent FIFO flags, you must clear the bits in this register. To clear any bit in this register that is set to logic '1' you must write a '1' to that bit.

NOTE: These four FIFO flag bits are present only in boards with an FPGA revision date greater that 10/12/05 (see Section 6.8).

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6.17 Delay Memory Registers (continued)

6.17.8 Delay Memory FIFO Status Registers (continued)

6.17.8.2 FIFO Status Bits — Bits D03 – D00

Each status bit is a non−latched version of the associated FIFO flag condition. When read as logic '1', the associated FIFO flag condition is active (true). When read as logic '0', the associated FIFO flag condition is inactive.

Note that when any status bit changes to logic '1', the corresponding flag bit in this register (Section 6.17.8.1) will also be set to logic '1'. However, when a status bit changes from '1' to '0', the corresponding latched bit in this register does not clear, but remains at the logic '1' state.

The Almost Full and Almost Empty FIFO levels are set using the Delay Memory FIFO Almost Full and Almost Empty Level Registers, Sections 6.17.10 and 6.17.11.

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6.17 Delay Memory Registers (continued)

6.17.9 Delay Memory FIFO Interrupt Mask Registers

There are two FIFO Interrupt Mask Registers for the Delay Memory, one each for the Delay Memory Read and Delay Memory Write FIFOs. The FIFO Interrupt Mask Registers contain enable bits for each FIFO interrupt condition defined. Each bit enables or disables the generation of a local bus interrupt (LINTix) to the PCI7140.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–80: Delay Memory FIFO Interrupt Mask Registers
Delay Memory Read FIFO: R/W @ BAR2+0x8D70
Delay Memory Write FIFO: R/W @ BAR2+0x8DA0

	D15 – D04	D03	D02	D01	D00
Bit Name	Reserved	FULL	ALMOST FULL	ALMOST EMPTY	EMPTY
Function	Write with zeros, Mask when reading	0 = Disable Interrupt 1 = Enable Interrupt			
All bits default to the logic '0' state at power on and reset					

Each bit of this register enables or disables the generation of a local bus interrupt to the PCI7140, when interrupts are enabled for this register in the Application Interrupt Enable LINTx Registers, Section 6.11.4.

Setting the bit associated with a given interrupt to the logic '1' state enables the generation of a local bus interrupt when that interrupt condition occurs. When a bit is cleared to logic '0' (its default state), the local bus interrupt will not be generated by the associated interrupt condition.

The four flag conditions are:

D03 – FIFO Full
D02 – FIFO Almost Full
D01 – FIFO Almost Empty
D00 – FIFO Empty

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6.17 Delay Memory Registers (continued)

6.17.10 Delay Memory FIFO Almost Empty Level Registers

There are two FIFO Almost Empty Level Registers for the Delay Memory, one each for the Delay Memory Read and Delay Memory Write FIFOs. This register sets the programmable boundary flag level of the Almost Empty flag for the associated FIFO.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–81: Delay Memory FIFO Almost Empty Level Registers
Delay Memory Read FIFO: R/W @ BAR2+0x8D78
Delay Memory Write FIFO: R/W @ BAR2+0x8DA8

	D15 – D10	D09 – D00
Bit Name	Reserved	D9 – D0
Function	Write with zeros, Mask when reading	FIFO Almost Empty Level
All bits default to the logic '0' state at power on and reset		

The Almost Empty Level is a 10–bit binary value, with bit D09 the MSB. This value specifies the FIFO Almost Empty flag depth.

NOTE: All 7140 FIFOs are 64 bits wide. Thus, the FIFO level programmed into this register indicates the level of 64–bit words. For example, if you set this register to a level of 12, the FIFO sets a boundary flag when the data transfer reaches 24 32–bit words.

While the FIFO is being read, when the data is at or below the Almost Empty level, the FIFO sets the Almost Empty Flag.

- The Almost Empty Flag is routed to the associated Delay Memory FIFO Status Register, Section 6.17.8.
- If the Almost Empty Flag is enabled by the associated Delay Memory FIFO Interrupt Mask Register, Section 6.17.9, a local bus interrupt will be asserted to the PCI7140.

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6.17 Delay Memory Registers (continued)

6.17.11 Delay Memory FIFO Almost Full Level Registers

There are two FIFO Almost Full Level Registers for the Delay Memory, one each for the Delay Memory Read and Delay Memory Write FIFOs. This register sets the programmable boundary flag level of the Almost Full flag for the associated FIFO.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–82: Delay Memory FIFO Almost Full Level Registers
Delay Memory Read FIFO: R/W @ BAR2+0x8D80
Delay Memory Write FIFO: R/W @ BAR2+0x8DB0

	D15 – D10	D09 – D00
Bit Name	Reserved	D9 – D0
Function	Write with zeros, Mask when reading	FIFO Almost Full Level
All bits default to the logic '0' state at power on and reset		

The Almost Full Level is a 10–bit binary value, with bit D09 the MSB. This value specifies the FIFO Almost Full flag depth.

NOTE: All 7140 FIFOs are 64 bits wide. Thus, the FIFO level programmed into this register indicates the level of 64–bit words. For example, if you set this register to a level of 12, the FIFO sets a boundary flag when the data transfer reaches 24 32–bit words.

While the FIFO is being written to, when the data is at or above the Almost Full level, the FIFO sets the Almost Full Flag.

- The FIFO Almost Full Flag is routed to the associated Delay Memory FIFO Status Register, Section 6.17.8.
- If the Almost Full Flag is enabled by the associated Delay Memory FIFO Interrupt Mask Register, Section 6.17.9, a local bus interrupt will be asserted to the PCI7140.

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6.18 Test FIFO Registers

The following subsections describe the FPGA registers that control the Test FIFO operations.

6.18.1 Test FIFO Control Register

There is one FIFO Control Register for the Test FIFO. This register contains bits that are used to control the FIFO operation.

The following table shows the contents of this register. The subsections following the table provide descriptions of the bits in this register.

Table 6–83: Test FIFO Control Register
R/W @ BAR2+0x8D38

	D15 – D02	D01	D00
Bit Name	Reserved	RESET	ENABLE
Function	Write with zeros, Mask when reading	0 = Run 1 = Reset	0 = Disable 1 = Enable
All bits default to the logic '0' state at power on and reset			

6.18.1.1 RESET Bit D01

This bit resets the Test FIFO. When the bit is cleared to logic '0' (its default state), the FIFO is in run; when the bit is set to logic '1', the FIFO is in reset.

6.18.1.2 ENABLE Bit D00

This bit enables the Test FIFO. When the bit is cleared to logic '0' (its default state), the FIFO is disabled; when the bit is set to logic '1', the FIFO is enabled.

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6.18 Test FIFO Registers (continued)

6.18.2 Test FIFO Status Register

The Test FIFO Status Register contains several flag and status bits associated with the Test FIFO.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–84: Test FIFO Status Register
R/Clr @ BAR2+0x8198

	D15 – D12	D11	D10	D09	D08
Bit Name	Reserved	FULL FLAG	ALMOST FULL FLAG	ALMOST EMPTY FLAG	EMPTY FLAG
Function	Write with zeros, Mask when reading	**Read:** 0 = FIFO flag condition not active 1 = FIFO flag condition latched **Clear:** 1 = Clear latch			
	D07 – D04	**D03 ***	**D02 ***	**D01 ***	**D00 ***
Bit Name	Reserved	FULL	ALMOST FULL	ALMOST EMPTY	EMPTY
Function	Write with zeros, Mask when reading	0 = FIFO flag condition not active 1 = FIFO flag condition active			

* These bits are Read Only
When reset, including power–up, the state of this register is unknown.
You should clear the register flag bits before using it, by writing '1's into bits D11 – D08.

6.18.2.1 FIFO Flag Bits — Bits D11 – D08

Read: Each bit latches a FIFO flag occurrence. Logic '1' in any bit indicates that a FIFO flag has been active. Note that when any status bit in this register (Section 6.18.2.2) changes to logic '1', the corresponding flag bit will also be set to logic '1'. However, when a status bit changes from '1' to '0', the corresponding latched bit in this register does not clear, but remains at the logic '1' state.

Clear: Since these bits latch in response to a FIFO flag occur–rence, to detect subsequent FIFO flags, you must clear the bits in this register. To clear any bit in this register that is set to logic '1' you must write a '1' to that bit.

NOTE: These four FIFO flag bits are present only in boards with an FPGA revision date greater that 10/12/05 (see Section 6.8).

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6.18 Test FIFO Registers (continued)

6.18.2 Test FIFO Status Register (continued)

6.18.2.2 FIFO Status Bits — Bits D03 – D00

Each status bit is a non–latched version of the associated FIFO flag condition. When read as logic '1', the associated FIFO flag condition is active (true). When read as logic '0', the associated FIFO flag condition is inactive.

Note that when any status bit changes to logic '1', the corresponding flag bit in this register (Section 6.18.2.1) will also be set to logic '1'.

The Almost Full and Almost Empty FIFO levels are set using the Test FIFO Almost Full and Test FIFO Almost Empty Level Registers, Sections 6.18.5 and 6.18.4.

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6.18 Test FIFO Registers (continued)

6.18.3 Test FIFO Interrupt Mask Register

There is one Test FIFO Interrupt Mask Register. The FIFO Interrupt Mask Register contains enable bits for each FIFO interrupt condition defined. Each bit enables or disables the generation of a local bus interrupt (LINTix) to the PCI7140.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–85: Test FIFO Interrupt Mask Register
R/W @ BAR2+0x8D40

	D15 – D04	D03	D02	D01	D00
Bit Name	Reserved	FULL	ALMOST FULL	ALMOST EMPTY	EMPTY
Function	Write with zeros, Mask when reading	0 = Disable Interrupt 1 = Enable Interrupt			
All bits default to the logic '0' state at power on and reset					

Each bit of this register enables or disables the generation of a local bus interrupt to the PCI7140, when interrupts are enabled for this register in the Application Interrupt Enable LINTx Registers, Section 6.11.4.

Setting the bit associated with a given interrupt to the logic '1' state enables the generation of a local bus interrupt when that interrupt condition occurs. When a bit is cleared to logic '0' (its default state), the local bus interrupt will not be generated by the associated interrupt condition.

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6.18 Test FIFO Registers (continued)

6.18.4 Test FIFO Almost Empty Level Register

There is one Test FIFO Almost Empty Level Register. This register sets the programmable boundary flag level of the Almost Empty flag for the FIFO.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–86: Test FIFO Almost Empty Level Register
R/W @ BAR2+0x8D48

	D15 – D10	D09 – D00
Bit Name	Reserved	D9 – D0
Function	Write with zeros, Mask when reading	FIFO Almost Empty Level
All bits default to the logic '0' state at power on and reset		

The Almost Empty Level is a 10–bit binary value, with bit D09 the MSB. This value specifies the FIFO Almost Empty flag depth.

NOTE: All 7140 FIFOs are 64 bits wide. Thus, the FIFO level programmed into this register indicates the level of 64–bit words. For example, if you set this register to a level of 12, the FIFO sets a boundary flag when the data transfer reaches 24 32–bit words.

While the FIFO is being read, when the data is at or below the Almost Empty level, the FIFO sets the Almost Empty Flag.

- The Almost Empty Flag is routed to the Test FIFO Status Register, Section 6.18.2.
- If the Almost Empty Flag is enabled by the Test FIFO Interrupt Mask Register, Section 6.18.3, a local bus interrupt will be asserted to the PCI7140.

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6.18 Test FIFO Registers (continued)

6.18.5 Test FIFO Almost Full Level Register

There is one Test FIFO Almost Full Level Register. This register sets the programmable boundary flag level of the Almost Full flag for the associated FIFO.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–87: Test FIFO Almost Full Level Register
R/W @ BAR2+0x8D50

	D15 – D10	D09 – D00
Bit Name	Reserved	D9 – D0
Function	Write with zeros, Mask when reading	FIFO Almost Full Level
All bits default to the logic '0' state at power on and reset		

The Almost Full Level is a 10–bit binary value, with bit D09 the MSB. This value specifies the FIFO Almost Full flag depth.

NOTE: All 7140 FIFOs are 64 bits wide. Thus, the FIFO level programmed into this register indicates the level of 64–bit words. For example, if you set this register to a level of 12, the FIFO sets a boundary flag when the data transfer reaches 24 32–bit words.

While the FIFO is being written to, when the data is at or above the Almost Full level, the FIFO sets the Almost Full Flag.

- The FIFO Almost Full Flag is routed to the Test FIFO Status Register, Section 6.18.2.
- If the Almost Full Flag is enabled by the Test FIFO Interrupt Mask Register, Section 6.18.3, a local bus interrupt will be asserted to the PCI7140.

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Chapter 7: Data Routing and Formatting

7.1 Overview

This chapter describes the data routing and formatting of the Model 7140.

Analog Data Inputs

The Model 7140 has two analog RF input channels from front panel MMCX connectors. Each input channel includes an AD6645 A/D converter that provides data directly to the FPGA. The outputs of both A/D converters are delivered, in parallel, to the FPGA through two 14−bit paths. The FPGA routes the AD6645 14−bit digital output data directly to two ADC FIFOs.

See Section 7.3 for description of the ADC data routing formats.

The Model 7140 also includes one GC4016 quad narrowband digital receiver chip. The GC4016 accepts four 14−bit or three 16−bit inputs. The FPGA provides data paths to the GC4016 and supports both 14−bit and 16−bit input modes. A crossbar switch inside the GC4016 allows each of the four receiver channels to independently select any of the inputs. The GC4016 delivers a real or complex parallel data stream to the FPGA, which routes the data to the DDC FIFOs.

See Section 7.4 for description of the DDC data routing formats.

Analog Data Outputs

The Model 7140 is designed with a maximum output sample rate of 320 MHz in upconverter mode and 500 MHz in D/A only mode. One Texas Instruments 16−bit DAC5686 is used to produce a pair of analog outputs capable of operating in D/A only, quadrature modulation, and single−sideband upconversion modes. The D/A has built−in interpolation filters settable to 2x, 4x, 8x, and 16x. The FPGA delivers 32−bit data to the DAC5686 where the analog outputs are sent to a pair of 1−to−1 transformers and then passed to front panel MMCX connectors.

See Section 7.5 for description of the DAC data routing formats.

NOTE: All FIFOs on the Model 7140 are 64 bits wide. Thus, the data formats presented in this chapter are shown as 64−bit formats.

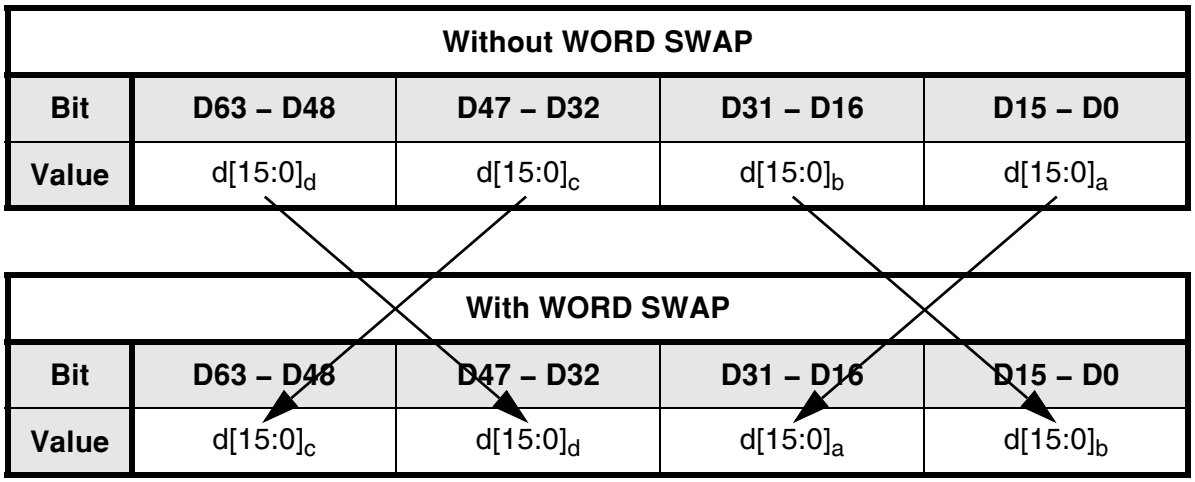
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7.2 FIFO Word Swap Formats

The data formats for the ADC, DDC, and DAC FIFOS allow you to use a WORD SWAP feature with the FIFO data. When the WORD SWAP control bit is set to logic '1' in the associated FIFO Control Register (ADC FIFO Control Register, Section 6.12.1, DDC FIFO Control Register, Section 6.13.1, or DAC FIFO Control Register, Section 6.15.1), word swapping is enabled and each pair of 16–bit samples are swapped in the 64–bit FIFO word, as follows:

Bits D00:15 are swapped with bits D16:31,
Bits D32:47 are swapped with bits D48:63.

The data is swapped as illustrated below.



This data WORD SWAP can be applied to any of the FIFO formats in the following sec–tions: Section 7.3 ADC data routing formats, Section 7.4 DDC data routing formats, and Section 7.5 DAC output data routing formats.

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7.3 ADC Data Routing and Formats

Each input AD6645 A/D converter channel provides 14–bit digital data directly to the ADC FIFOs (A/D 1 to ADC 1 FIFO, A/D 2 to ADC 2 FIFO). The ADC output can be written to a FIFO at a programmed decimation rate, and may be unpacked or packed by time of arrival as set by the associated ADC FIFO Control Register, Section 6.12.1.4. The following subsections describe these data formats. WORD SWAP, Section 7.2, can be applied to any of these ADC FIFO formats.

7.3.1 Unpacked

Each ADC FIFO receives the raw 14–bit data directly from its associated AD6645 A/D (A/D 1 data to ADC 1 FIFO, A/D 2 data to ADC 2 FIFO). Writing to the FIFO is controlled by the selected gate. The data is written to the FIFO at a programmed decimation rate N, where N is 1 to 4096, only when the gate is enabled.

When PACK MODE (bit D08 in the ADC FIFO Control Register) is cleared to 0, data is unpacked with two consecutive A/D samples duplicated in each 64–bit FIFO word. Each A/D sample is left justified in the 14 most signifi–cant bits out of 16 in each 16–bit segment of the 64–bit FIFO data word.

- The first sample, received at time 't', is placed into bits D15 to D2. The same sample is duplicated in bits D31 to D18.
- The next sample, received at time 't+1', is placed into bits D47 to D34. The same sample is duplicated in bits D63 to D50.

The ADC FIFO data is in the following format:

Table 7–1: Data Format – ADC FIFO, Unpacked

Bit	D63 – D50	D49 D48	D47 – D34	D33 D32	D31 – D18	D17 D16	D15 – D2	D1 D0
Value	14–bit A/D sample[13:0] at time (t+1)	00	14–bit A/D sample[13:0] at time (t+1)	00	14–bit A/D sample[13:0] at time (t)	00	14–bit A/D sample[13:0] at time (t)	00

With WORD SWAP enabled the data format is the same.

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7.3 ADC Data Routing and Formats (continued)

7.3.2 Time–Packed

Each ADC FIFO receives the raw 14–bit data directly from its associated AD6645 A/D (A/D 1 data to ADC 1 FIFO, A/D 2 data to ADC 2 FIFO). The data is written to the FIFO at a programmed decimation rate N (1 to 4096), only when the selected gate is enabled.

When PACK MODE (bit D08 in the ADC FIFO Control Register) is set to 1, data is packed with four A/D samples in each 64–bit FIFO word.

Without WORD SWAP (disabled), data is packed with four consecutive A/D samples in each 64–bit FIFO word. Each A/D sample is left justified in the 14 most significant bits out of 16 in each of the 16–bit segments of the 64–bit FIFO data word.

- The first sample, received at time 't', is placed into bits D15 to D2.
- The next sample, received at time 't+1', is placed into bits D31 to D18.
- The next sample, received at time 't+2', is placed into bits D47 to D34.
- The next sample, received at time 't+3', is placed into bits D63 to D50.

The ADC FIFO data is in the following format:

Table 7–2: Data Format – ADC FIFO, Time Packed

Bit	D63 – D50	D49 D48	D47 – D34	D33 D32	D31 – D18	D17 D16	D15 – D2	D1 D0
Value	14–bit A/D sample[13:0] at time (t+3)	00	14–bit A/D sample[13:0] at time (t+2)	00	14–bit A/D sample[13:0] at time (t+1)	00	14–bit A/D sample[13:0] at time (t)	00

With WORD SWAP enabled, each consecutive pair of samples (e.g., t and t+1) are swapped as follows:

Table 7–3: Data Format – ADC FIFO, Time Packed, Word Swap

Bit	D63 – D50	D49 D48	D47 – D34	D33 D32	D31 – D18	D17 D16	D15 – D2	D1 D0
Value	14–bit A/D sample[13:0] at time (t+2)	00	14–bit A/D sample[13:0] at time (t+3)	00	14–bit A/D sample[13:0] at time (t)	00	14–bit A/D sample[13:0] at time (t+1)	00

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7.4 DDC Data Routing and Formats

The FPGA provides 14−bit ADC digital data to the GC4016; A/D 1 data is routed to DDC Channel A input, A/D 2 data to DDC Channel B input. DDC Channels C and D can be setup to receive digital data from the Delay Memory (Bank 1 to Channel C, Bank 2 to Channel D), or from A/D 1 and 2 (A/D 1 to Channel C, A/D 2 to Channel D).

The GC4016 must be set up for parallel output mode, **SFS_MODE**=2, at the full clock rate (see GC4016 Registers, Section 6.14, and GC4016 Data Sheet, Section 1.16, for GC4016 programming). The GC4016 **RDY** signal indicates the start of a data frame and the **SFS** signal denotes valid data samples. The data is collected from the GC4016 as 24−bit parallel words, regardless of whether the GC4016 is set for 16− or 24−bit mode.

DDC Data Routing

The FPGA multiplexes data from the GC4016 four channels and writes the formatted data to the DDC FIFOs. The four channels of DDC data are routed to the DDC FIFOs as follows:

- When the GC4016 is set up for tagging, each DDC output data word contains a tag indicating the DDC channel (A, B, C, or D). The GC4016 can be set up for 2 or 4−bit tagging (see Section 1.16 for GC4016 Data Sheet), as follows. If you set GC4016 control bit **TAG_EN**=1, four tag bits replace the four LSBs of the 24−bit output word. If you set GC4016 control bit **TAG_22**=1, two tag bits replace the two LSBs of the 24−bit output word. The FPGA uses this tag to route the 24−bit data word (including the tag) to the applicable DDC FIFO.

  For this mode, you must enable Tag Mode in the associated DDC FIFO Control Register, Section 6.13.1.3.

- When the GC4016 is **not** set up for tagging, the DDC output data is written to any of the four DDC FIFOs that are enabled. The FPGA routes each consecutive 24−bit DDC output data word to each enabled FIFO.

  For this mode, you must disable Tag Mode in the associated DDC FIFO Control Register, Section 6.13.1.3.

DDC Data Formatting

DDC outputs written to the FIFOs may be unpacked or packed by the FPGA, as set by the associated DDC FIFO Control Register, Section 6.13.1.3. The following subsections describe these data formats. WORD SWAP, Section 7.2, can be applied to any of these DDC FIFO formats.

NOTE: The following descriptions assume that the GC4016 is set up for COMPLEX output (the default output), providing both I and Q values. If you configure the GC4016 for REAL output, real samples are output from the GC4016 as one word per frame and the FPGA identifies the REAL data sample as I values.

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7.4 DDC Data Routing and Formats (continued)

7.4.1 Unpacked I/Q

The DDC FIFO takes 24–bit I and Q samples from the parallel output of the GC4016. If Tag Mode is enabled, the tag bits in each data sample determine the DDC FIFO that the data is written to. See DDC Data Routing, page 217. Writing to the FIFO is controlled by the selected gate. FIFO writes are disabled except when the gate is enabled.

Without WORD SWAP, two consecutive DDC data samples are left justified in the 24 most significant bits in each 32–bit half of the 64–bit FIFO data word. If Tag Mode is enabled, the least significant 2 or 4 bits of each data sample contain the GC4016 tag. The FPGA also sets an I/Q code for this sample in the least significant bit of each 32–bit half.

- The first sample, received at time 't', is placed into bits D31 to D8. Bits D7 to D1 are zeros, and bit D0 is the I/Q code.
- The next sample, received at time 't+1', is placed into bits D63 to D40. Bits D39 to D33 are zeros, and bit D32 is the I/Q code.

The DDC FIFO data is in the following format:

Table 7–4: Data Format – DDC FIFO, Unpacked I/Q

Bit	D63 – D40	D39–D33	D32	D31 – D8	D7–D1	D0
Value	24–bit DDC sample[23:0] at time (t+1)	0	I/Q code	24–bit DDC sample[23:0] at time (t)	0	I/Q code
I/Q code: I = 0, Q = 1						

With WORD SWAP enabled the DDC FIFO data is in the following format:

Table 7–5: Data Format – DDC FIFO, Unpacked I/Q, Word Swap

Bit	D63–D56	D55–D49	D48	D47 – D32	D31–D24	D23–D17	D16	D15 – D0
Value	DDC sample bits[7:0] at time (t+1)	0	I/Q code	DDC sample bits[23:8] at time (t+1)	DDC sample bits[7:0] at time (t)	0	I/Q code	DDC sample bits[23:8] at time (t)
I/Q code: I = 0, Q = 1								

NOTE: If you configure the GC4016 for REAL output, real samples are output from the GC4016 as one word per frame and the FPGA identifies the REAL data sample as I values (I/Q code =0).

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7.4 DDC Data Routing and Formats (continued)

7.4.2 Packed I/Q

The DDC FIFO takes 24–bit I and Q samples from the parallel output of the GC4016. If Tag Mode is enabled, the tag bits in each data sample determine the DDC FIFO that the data is written to. See DDC Data Routing, page 217. Writing to the FIFO is controlled by the selected gate. FIFO writes are disabled except when the gate is enabled.

Without WORD SWAP, in packed mode DDC data samples are packed with the most significant 16 bits of two consecutive 24–bit I and Q samples packed into the 64–bit FIFO data word. If Tag Mode is enabled, the tag bits will not appear in each sample.

- The first sample, received at time 't', is placed into the lowest 32 bits of the 64–bit word with the 16–bit Q value in bits D15 to D0 and the 16–bit I value in bits D31 to D16.

- The next sample, received at time 't+1', is placed into the highest 32 bits of the 64–bit word with the 16–bit Q value in bits D47 to D32 and the 16–bit I value in bits D63 to D48.

The DDC FIFO data is in the following format:

Table 7–6: Data Format – DDC FIFO, Packed I/Q

Bit	D63 – D48	D47 – D32	D31 – D16	D15 – D0
Value	I data sample bits[23:8] at time (t+1)	Q data sample bits[23:8] at time (t+1)	I data sample bits[23:8] at time (t)	Q data sample bits[23:8] at time (t)

With WORD SWAP enabled the I and Q samples are swapped as follows:

Table 7–7: Data Format – DDC FIFO, Packed I/Q, Word Swap

Bit	D63 – D48	D47 – D32	D31 – D16	D15 – D0
Value	Q data sample bits[23:8] at time (t+1)	I data sample bits[23:8] at time (t+1)	Q data sample bits[23:8] at time (t)	I data sample bits[23:8] at time (t)

NOTE: The above description assumes that the GC4016 is set up for COMPLEX output (the default output), providing both I and Q values. If you configure the GC4016 for REAL output, real samples are output from the GC4016 as one word per frame.

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7.5 DAC Data Routing and Formats

The FPGA receives digital data from the DAC FIFOs, and then presents the digital data to the DAC5686's dual 16−bit interfaces (DAC channels A and B). There are four packing modes of DAC FIFO data: Unpacked, 16−bit Time Packed, 16−bit Channel Packed, and 8−bit Channel/Time Packed. To select a packing mode, set the Pack Mode bits in the associated DAC FIFO Control Register, Section 6.15.1. WORD SWAP, Section 7.2, can be applied to any of these DAC FIFO formats, except Unpacked.

The following subsections describe these data formats.

7.5.1 Unpacked

In Unpacked mode, the FPGA presents the DAC5686 with 16−bit digital samples from each DAC FIFO to the associated DAC channel (DAC A FIFO to DAC channel A, DAC B FIFO to DAC channel B) (see page 221 for illustration of the routing of the data samples to each DAC5686 channel).

Each 64−bit FIFO data word contains two consecutive data samples for the associated DAC channel. Data is unpacked with data for the DAC channel in the upper 16 bits of each 32−bit half of the 64−bit word, and zeros in the lower 16 bits of each 32−bit half.

- The first sample, for time 't', is placed into the lowest 32 bits of the 64−bit word with the 16−bit sample in bits D31 to D16.
- The next sample, for time 't+1', is placed into the highest 32 bits of the 64−bit word with the 16−bit sample in bits D63 to D48.

The DAC FIFO data is in the following format:

Table 7−8: Data Format − DAC X FIFO, Unpacked

Bit	D63 − D48	D47 − D32	D31 − D16	D15 − D0
Value	data[15:0] for DAC channel X at time (t+1)	0	data[15:0] for DAC channel X at time (t)	0
X = A or B, depending on the FIFO accessed				

NOTE: WORD SWAP should not be used with this mode since the data bits for the DAC5686 (D63:48 and D31:16) would contains zeros.

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7.5 DAC Data Routing and Formats (continued)

7.5.1 Unpacked (continued)

The data routing is illustrated below.

DAC5686 Input Channels		
Bit	**DA[15 :0]**	**DB[15:0]**
Word 1	$d[15:0]_{A(t)}$	$d[15:0]_{B(t)}$
Word 2	$d[15:0]_{A(t+1)}$	$d[15:0]_{B(t+1)}$
Word 3	$d[15:0]_{A(t+2)}$	$d[15:0]_{B(t+2)}$
Word 4	$d[15:0]_{A(t+3)}$	$d[15:0]_{B(t+3)}$
Word n	...	...

Bit	**D63:48**	**D47:32**	**D31:D16**	**D15:D0**	**D63:48**	**D47:32**	**D31:D16**	**D15:D0**
Word 1	$d[15:0]_{A(t+1)}$	0	$d[15:0]_{A(t)}$	0	$d[15:0]_{B(t+1)}$	0	$d[15:0]_{B(t)}$	0
Word 2	$d[15:0]_{A(t+3)}$	0	$d[15:0]_{A(t+2)}$	0	$d[15:0]_{B(t+3)}$	0	$d[15:0]_{B(t+2)}$	0
Word n	...	0	...	0	...	0	...	0
	DAC A FIFO				**DAC B FIFO**			

NOTE: WORD SWAP should not be used with this mode since the data bits sent to the DAC5686 (D63:48 and D31:16) would contains zeros and the actual data would not be transferred.

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7.5 DAC Data Routing and Formats (continued)

7.5.2 Channel Packed, 16–bit

In Channel Packed mode, the FPGA presents the DAC5686 with 16–bit digital samples for both DAC channels from DAC A FIFO only. DAC B FIFO is not used in this mode (see page 223 for illustration of the routing of the data samples to each DAC5686 channel).

Each 64–bit FIFO data word presents the DAC with two consecutive 16–bit data samples for each DAC channel.

Without WORD SWAP (disabled), data is packed with data for DAC channel B in the upper 16 bits of each 32–bit half, and data for DAC channel A in the lower 16 bits of each 32–bit half of the 64–bit word.

- The first sample, for time 't', is placed into the lowest 32 bits of the 64–bit word, with the channel B sample in bits D31 to D16 and the channel A sample in bits D15 to D0.
- The next sample, for time 't+1', is placed into the highest 32 bits of the 64–bit word, with the channel B sample in bits D63 to D48 and the channel A sample in bits D47 to D32.

The DAC A FIFO data is in the following format:

Table 7–9: Data Format – DAC A FIFO, Channel Packed

Bit	D63 – D48	D47 – D32	D31 – D16	D15 – D0
Value	data[15:0] for DAC channel B at time (t+1)	data[15:0] for DAC channel A at time (t+1)	data[15:0] for DAC channel B at time (t)	data[15:0] for DAC channel A at time (t)

With WORD SWAP enabled channel A and B data are swapped as follows:

Table 7–10: Data Format – DAC A FIFO, Channel Packed, Word Swap

Bit	D63 – D48	D47 – D32	D31 – D16	D15 – D0
Value	data[15:0] for DAC channel A at time (t+1)	data[15:0] for DAC channel B at time (t+1)	data[15:0] for DAC channel A at time (t)	data[15:0] for DAC channel B at time (t)

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7.5 DAC Data Routing and Formats (continued)

7.5.2 Channel Packed, 16–bit (continued)

The data routing ***without*** WORD SWAP is illustrated below.

DAC5686 Input Channels		
Bit	**DA[15 :0]**	**DB[15:0]**
Word 1	$d[15:0]_{A(t)}$	$d[15:0]_{B(t)}$
Word 2	$d[15:0]_{A(t+1)}$	$d[15:0]_{B(t+1)}$
Word 3	$d[15:0]_{A(t+2)}$	$d[15:0]_{B(t+2)}$
Word 4	$d[15:0]_{A(t+3)}$	$d[15:0]_{B(t+3)}$
Word n	...	...

Bit	**D63:48**	**D47:32**	**D31:D16**	**D15:D0**	**D63:48**	**D47:32**	**D31:D16**	**D15:D0**
Word 1	$d[15:0]_{B(t+1)}$	$d[15:0]_{A(t+1)}$	$d[15:0]_{B(t)}$	$d[15:0]_{A(t)}$	Not Used in this mode			
Word 2	$d[15:0]_{B(t+3)}$	$d[15:0]_{A(t+3)}$	$d[15:0]_{B(t+2)}$	$d[15:0]_{A(t+2)}$				
Word n	...	...	...	...				
	DAC A FIFO				**DAC B FIFO**			

The data routing ***with*** WORD SWAP is illustrated below.

DAC5686 Input Channels		
Bit	**DA[15 :0]**	**DB[15:0]**
Word 1	$d[15:0]_{B(t)}$	$d[15:0]_{A(t)}$
Word 2	$d[15:0]_{B(t+1)}$	$d[15:0]_{A(t+1)}$
Word 3	$d[15:0]_{B(t+2)}$	$d[15:0]_{A(t+2)}$
Word 4	$d[15:0]_{B(t+3)}$	$d[15:0]_{A(t+3)}$
Word n	...	...

Bit	**D63:48**	**D47:32**	**D31:D16**	**D15:D0**	**D63:48**	**D47:32**	**D31:D16**	**D15:D0**
Word 1	$d[15:0]_{A(t+1)}$	$d[15:0]_{B(t+1)}$	$d[15:0]_{A(t)}$	$d[15:0]_{B(t)}$	Not Used in this mode			
Word 2	$d[15:0]_{A(t+3)}$	$d[15:0]_{B(t+3)}$	$d[15:0]_{A(t+2)}$	$d[15:0]_{B(t+2)}$				
Word n	...	...	...	...				
	DAC A FIFO				**DAC B FIFO**			

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7.5 DAC Data Routing and Formats (continued)

7.5.3 Time Packed, 16–bit

In Time Packed mode, the FPGA presents the DAC5686 with 16–bit digital samples from each DAC FIFO for the associated DAC channel (DAC A FIFO to DAC channel A, DAC B FIFO to DAC channel B) (see page 225 for illustration of the routing of the data samples to each DAC5686 channel).

Without WORD SWAP (disabled), each 64–bit FIFO data word contains four consecutive 16–bit samples for the associated DAC channel. The samples are time–ordered with the least 16 significant bits of the FIFO word containing the first sample.

- The first sample, for time 't', is placed into bits D15 to D0.
- The next sample, for time 't+1', is placed into bits D31 to D16.
- The next sample, for time 't+2', is placed into bits D47 to D32.
- The next sample, for time 't+3', is placed into bits D63 to D48.

The data is packed into the DAC FIFO in the following format:

Table 7–11: Data Format – DAC X FIFO, Time Packed

Bit	D63 – D48	D47 – D32	D31 – D16	D15 – D0
Value	data[15:0] for DAC channel X at time (t+3)	data[15:0] for DAC channel X at time (t+2)	data[15:0] for DAC channel X at time (t+1)	data[15:0] for DAC channel X at time (t)
X = A or B, depending on the FIFO accessed				

With WORD SWAP enabled, each consecutive pair of data (e.g., t and t+1) is swapped as follows:

Table 7–12: Data Format – DAC X FIFO, Time Packed, Word Swap

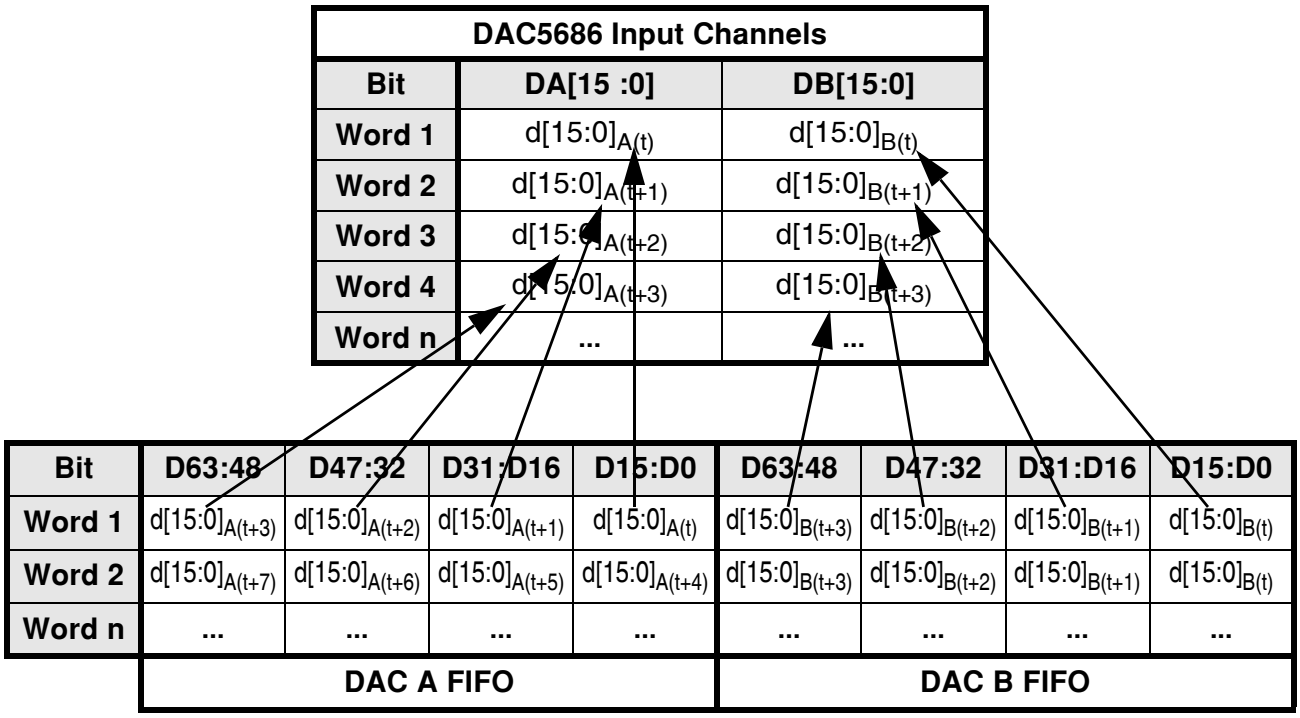
Bit	D63 – D48	D47 – D32	D31 – D16	D15 – D0
Value	data[15:0] for DAC channel X at time (t+2)	data[15:0] for DAC channel X at time (t+3)	data[15:0] for DAC channel X at time (t)	data[15:0] for DAC channel X at time (t+1)
X = A or B, depending on the FIFO accessed				

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7.5 DAC Data Routing and Formats (continued)

7.5.3 Time Packed, 16–bit (continued)

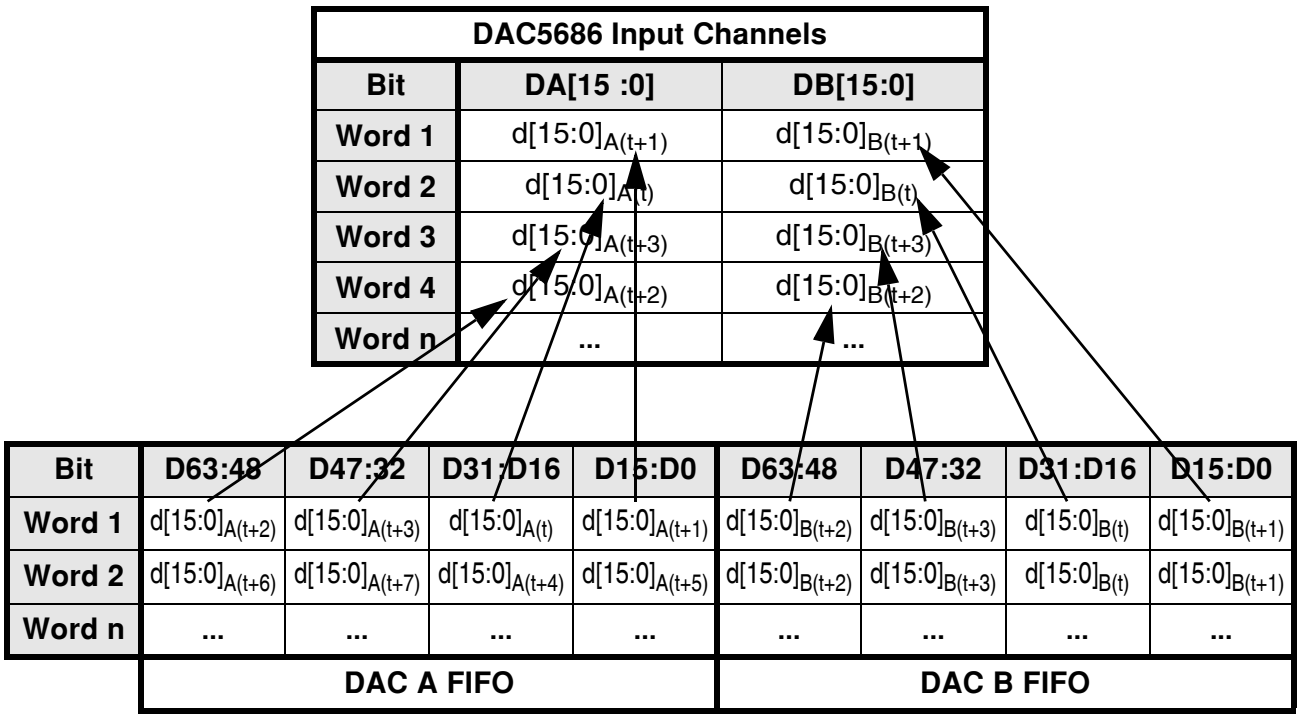
The data routing ***without*** WORD SWAP is illustrated below.



DAC5686 Input Channels		
Bit	**DA[15 :0]**	**DB[15:0]**
Word 1	$d[15:0]_{A(t)}$	$d[15:0]_{B(t)}$
Word 2	$d[15:0]_{A(t+1)}$	$d[15:0]_{B(t+1)}$
Word 3	$d[15:0]_{A(t+2)}$	$d[15:0]_{B(t+2)}$
Word 4	$d[15:0]_{A(t+3)}$	$d[15:0]_{B(t+3)}$
Word n	...	...

Bit	D63:48	D47:32	D31:D16	D15:D0	D63:48	D47:32	D31:D16	D15:D0
Word 1	$d[15:0]_{A(t+3)}$	$d[15:0]_{A(t+2)}$	$d[15:0]_{A(t+1)}$	$d[15:0]_{A(t)}$	$d[15:0]_{B(t+3)}$	$d[15:0]_{B(t+2)}$	$d[15:0]_{B(t+1)}$	$d[15:0]_{B(t)}$
Word 2	$d[15:0]_{A(t+7)}$	$d[15:0]_{A(t+6)}$	$d[15:0]_{A(t+5)}$	$d[15:0]_{A(t+4)}$	$d[15:0]_{B(t+3)}$	$d[15:0]_{B(t+2)}$	$d[15:0]_{B(t+1)}$	$d[15:0]_{B(t)}$
Word n	...	...	...	...	...	...	...	...
	DAC A FIFO				**DAC B FIFO**			

The data routing ***with*** WORD SWAP is illustrated below.



DAC5686 Input Channels		
Bit	**DA[15 :0]**	**DB[15:0]**
Word 1	$d[15:0]_{A(t+1)}$	$d[15:0]_{B(t+1)}$
Word 2	$d[15:0]_{A(t)}$	$d[15:0]_{B(t)}$
Word 3	$d[15:0]_{A(t+3)}$	$d[15:0]_{B(t+3)}$
Word 4	$d[15:0]_{A(t+2)}$	$d[15:0]_{B(t+2)}$
Word n	...	...

Bit	D63:48	D47:32	D31:D16	D15:D0	D63:48	D47:32	D31:D16	D15:D0
Word 1	$d[15:0]_{A(t+2)}$	$d[15:0]_{A(t+3)}$	$d[15:0]_{A(t)}$	$d[15:0]_{A(t+1)}$	$d[15:0]_{B(t+2)}$	$d[15:0]_{B(t+3)}$	$d[15:0]_{B(t)}$	$d[15:0]_{B(t+1)}$
Word 2	$d[15:0]_{A(t+6)}$	$d[15:0]_{A(t+7)}$	$d[15:0]_{A(t+4)}$	$d[15:0]_{A(t+5)}$	$d[15:0]_{B(t+2)}$	$d[15:0]_{B(t+3)}$	$d[15:0]_{B(t)}$	$d[15:0]_{B(t+1)}$
Word n	...	...	...	...	...	...	...	...
	DAC A FIFO				**DAC B FIFO**			

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7.5 DAC Data Routing and Formats (continued)

7.5.4 Channel/Time Packed, 8–bit

In Channel/Time Packed mode, the FPGA presents the DAC5686 with 8–bit digital samples for both DAC output channels from DAC A FIFO only (see page 227 and page 228 for illustration of the routing of the data samples to each DAC5686 channel).

Without WORD SWAP (disabled), each 64–bit FIFO data word contains eight 8–bit digital samples, four consecutive samples for each DAC channel. The samples are time–ordered with the least significant eight bits of the FIFO word containing the first sample.

- The first two samples, for time 't', are placed into the lowest 16 bits of the 64–bit word, Ch A in bits D15 to D8, Ch B in bits D9 to D0.
- The next samples, for time 't+1', are placed into the next lower 16 bits, Ch A in D31 to D24, Ch B in bits D23 to D16.
- The next samples, for time 't+2', are placed into the next lower 16 bits, Ch A in D47 to D40, Ch B in bits D39 to D32.
- The next samples, for time 't+3', are placed into the lowest 16 bits of the 64–bit word, Ch A in bits D63 to D56, Ch B in bits D55 to D48.

The data is packed into the DAC FIFO in the following format:

Table 7–13: Data Format – DAC A FIFO, 8–bit Packed

Bit	D63:56	D55:48	D47:D40	D39:D32	D31:24	D2316	D15:D8	D7:D0
Value	data[7:0] for DAC channel A at time (t+3)	data[7:0] for DAC channel B at time (t+3)	data[7:0] for DAC channel A at time (t+2)	data[7:0] for DAC channel B at time (t+2)	data[7:0] for DAC channel A at time (t+1)	data[7:0] for DAC channel B at time (t+1)	data[7:0] for DAC channel A at time (t)	data[7:0] for DAC channel B at time (t)

With WORD SWAP enabled, each consecutive set of samples (e.g., t and t+1) are swapped as follows:

Table 7–14: Data Format – DAC A FIFO, 8–bit Packed, Word Swap

Bit	D63:56	D55:48	D47:D40	D39:D32	D31:24	D2316	D15:D8	D7:D0
Value	data[7:0] for DAC channel A at time (t+2)	data[7:0] for DAC channel B at time (t+2)	data[7:0] for DAC channel A at time (t+3)	data[7:0] for DAC channel B at time (t+3)	data[7:0] for DAC channel A at time (t)	data[7:0] for DAC channel B at time (t)	data[7:0] for DAC channel A at time (t+1)	data[7:0] for DAC channel B at time (t+1)

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7.5 DAC Data Routing and Formats (continued)

7.5.4 Channel/Time Packed, 8–bit (continued)

The data routing ***without*** WORD SWAP is illustrated below.

DAC5686 Input Channels				
Bit	**DA[15:8]**	**DA[7:0]**	**DB[15:8]**	**DB[7:0]**
Word 1	$d[7:0]_{A(t)}$	$d[7:0]_{B(t)}$	$d[7:0]_{B(t)}$	0
Word 2	$d[7:0]_{A(t+1)}$	$d[7:0]_{B(t+1)}$	$d[7:0]_{B(t+1)}$	0
Word 3	$d[7:0]_{A(t+2)}$	$d[7:0]_{B(t+2)}$	$d[7:0]_{B(t+2)}$	0
Word 4	$d[7:0]_{A(t+3)}$	$d[7:0]_{B(t+3)}$	$d[7:0]_{B(t+3)}$	0
Word n	...		...	0

Bit	**D63:56**	**D55:48**	**D47:D40**	**D39:D32**	**D31:24**	**D2316**	**D15:D8**	**D7:D0**
Word 1	$d[7:0]_{A(t+3)}$	$d[7:0]_{B(t+3)}$	$d[7:0]_{A(t+2)}$	$d[7:0]_{B(t+2)}$	$d[7:0]_{A(t+1)}$	$d[7:0]_{B(t+1)}$	$d[7:0]_{A(t)}$	$d[7:0]_{B(t)}$
Word 2	$d[7:0]_{A(t+7)}$	$d[7:0]_{B(t+7)}$	$d[7:0]_{A(t+6)}$	$d[7:0]_{B(t+6)}$	$d[7:0]_{A(t+5)}$	$d[7:0]_{B(t+5)}$	$d[7:0]_{A(t+4)}$	$d[7:0]_{B(t+4)}$
Word n	...	...	...	...	...	...	...	...
DAC A FIFO (**DAC B FIFO** not used)								

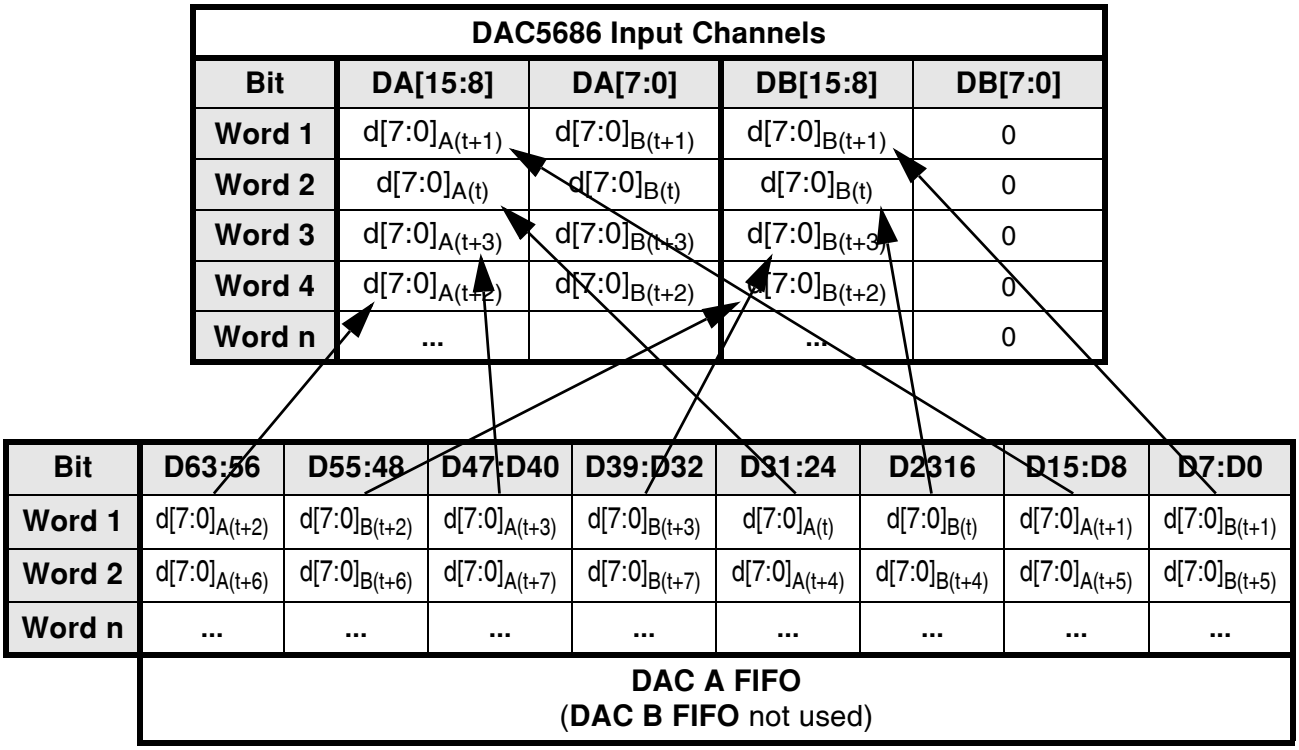
NOTE: Note that the channel B data is included in the data sent to channel A, however the resolution of this 8–bit data is insignificant to the output signal on A.

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7.5 DAC Data Routing and Formats (continued)

7.5.4 Channel/Time Packed, 8–bit (continued)

The data routing ***with*** WORD SWAP is illustrated below.



NOTE: Note that the channel B data is included in the data sent to channel A, however the resolution of this 8–bit data is insignificant to the output signal on A.

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Appendix A: PCI Configuration Space Registers

A.1 Introduction

This Appendix shows the pre–defined header region of PCI Configuration Space.

A.2 PCI Configuration Space Registers

The PCI Configuration Space consists of fields that uniquely identify the device and allow the device to be generically controlled. The first 16 Bytes (four words) are defined the same for all types of PCI devices. The remaining words can have different layouts depending on the base function that the device supports. The PCI interface on the Model 7140 uses Header Type 00h, which has the layout shown in the table below. This table lists the PCI Configuration Space registers, their functions, and their base address in Configuration Space.

Table A–1: PCI Configuration Space Header (Type 00h)

Address	Register Function			
0x00	Device ID		Vendor ID	
0x04	Status		Command	
0x08	Class Code			Revision ID
0x0C	BIST	Header Type	Latency Timer	Cache Line Size
0x10	Base Address Register 0 (BAR0)			
0x14	Base Address Register 1 (BAR1)			
0x18	Base Address Register 2 (BAR2)			
0x1C	Base Address Register 3 (BAR3)			
0x20	Base Address Register 4 (BAR4)			
0x24	Base Address Register 5 (BAR5)			
0x28	Cardbus CIS Pointer			
0x2C	Subsystem ID		Subsystem Vendor ID	
0x30	Expansion ROM Base Address			
0x34	Reserved			
0x38	Reserved			
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line

The Base Address Registers defined for the Model 7140 are shown on the next page.

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A.2 PCI Configuration Space Registers (continued)

In the Model 7140, the first four Base Address Registers of PCI Configuration Space are used to configure the memory maps of board resources and registers. The following table shows the use of these registers in the 7140.

Table A–2: PCI Base Address Registers

Address	Register	Model 7140 Use
0x10	Base Address Register 0 (BAR0)	Memory accesses to PCI7140 Local, Runtime, and DMA registers
0x14	Base Address Register 1 (BAR1)	Memory accesses to 7140 FIFOs
0x18	Base Address Register 2 (BAR2)	Memory accesses to 7140 FPGA Global, Clock/Sync/ Gate, Interrupt,D/A, A/D, Registers
0x1C	Base Address Register 3 (BAR3)	not used on 7140

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