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OPERATING MANUAL

MODEL 71620

3–Channel 200 MHz A/D, 2–Channel 800 MHz D/A
Cobalt Family XMC Module



PENTEK

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Manual Revision History

Date	Revision	Comments
6/10 – 5/11	Preliminary	Contact Factory for manual revision history.
6/21/11	A	Sect 5.14, corrected description of BUSY bit in CDC Control/Status Register, per KBCase 1382. Release manual Revision A.
7/21/11	A.1	Sect 5.33, added note to NUM BYTES, bits 3–0, for accessing board ID EEPROM.
8/18/11	A.2	Sect 2.7.1, corrected external CLK maximum input to +12 dBm.
10/25/11	A.3	Sect 7.17, corrected RAM Capture Count Register address to 0x30044 in Table 7–17.
11/4/11	A.4	Sect 3.5.3, Sect 5.14, & Sect 5.21, corrected description of CDC reset per KBCase 1391.
12/13/11	A.5	Sect 2.2.2, updated switch SW2 descriptions. Sect 2.7.2, removed incorrect reference to Option 002.
12/22/11	A.6	Sect 5.34.1, added new EEPROM format for boards shipped in November 2011 or later. Sect 2.5 & Sect 2.7.4, added Note of input limits for PMC P14 and front panel Sync Bus connectors.
1/16/12	2.0	Version number change only. (Starting January 2012 Pentek upgraded document Version numbering.)
4/20/12	2.1	Sect 1.14 & Sect 2.7.1, corrected external clock input voltage limit to +10 dBm.
5/10/12	2.2	Sect 1.14, deleted Output IF specification for Digital to Analog Upconverter.
11/20/12	2.3	Sect 2.5.1, add XMC P16 connector pin definition table.
4/22/13	2.4	Updated several graphics' fonts.
5/28/13	2.5	Sect 1.14 & Sect 2.7.1, corrected external clock input frequency maximum to 800 MHz.
8/2/13	2.6	Table 3–20, corrected Min VCCINT address to 0x08094.
9/6/13	2.7	Verified & updated cross–reference links in manual.
2/19/14	2.8	Sect 3.2.2, increased minimum number of clock cycles to 5 for DELAY in ADC Input Linked List.
3/21/14	2.9	Sect 2.2.2, changed switch SW2–5 to OFF, factory use only.
4/21/14	2.10	Sect 1.14, spec update: removed environmental Option 700 – Option 701 is now default.
6/12/14	2.11	Sect 1.14 & Sect 3.5, changed external Sync unit needed to Pentek Model 7893.
9/18/14	2.12	Sect 5.30, changed Timestamp Start Time Register to Write Only.
6/25/15	2.13	Sect 2.7.4, provided Pentek Model numbers for available mating connectors.
12/27/17	2.14	Sect 2.5.2 & Table 2–8, removed references to VMEbus from P14 connector.

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Chapter 1: Introduction

1.1 General Description

Pentek's Cobalt® Family Model 71620 is a multichannel, high−speed data converter suitable for connection to HF or IF ports of a communications or radar system. It includes three 200−MHz, 16−bit A/D converters and two 800−MHz D/A upconverters. The 71620 is compatible with the VITA 42.0 XMC format and supports PCI Express® (PCIe®) Gen 1 or 2 as a native interface.

The 71620 XMC module can be attached directly to any digital signal processing (DSP) baseboard equipped with an XMC expansion site, or to an XMC carrier/adaptor, such as the Pentek Model 7806 XMC PCI Express carrier.

NOTE: This 71620 Operating Manual applies to all Pentek Cobalt products that include Pentek's Model 71620 XMC, including the Model 78620 PCIe board and the Model 53620 VPX board.

1.2 Features

- Three 200−MHz 16−bit A/D converters
- Two 800−MSPS 16−bit D/A converters
- Xilinx® Virtex®−6 FPGA
- Up to 32 MB of QDRII+ SRAM or 2 GB of DDR3 SDRAM
- Clock synthesizer can create different clock rates for A/D and D/A processing
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen 1 or 2) interface up to x8 wide
- VITA 42.0 XMC compatible with switched fabric interfaces
- LVDS connections to the Virtex−6 FPGA for custom I/O

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1.3 Block Diagram

The following is a simplified block diagram of the Model 71620 module.

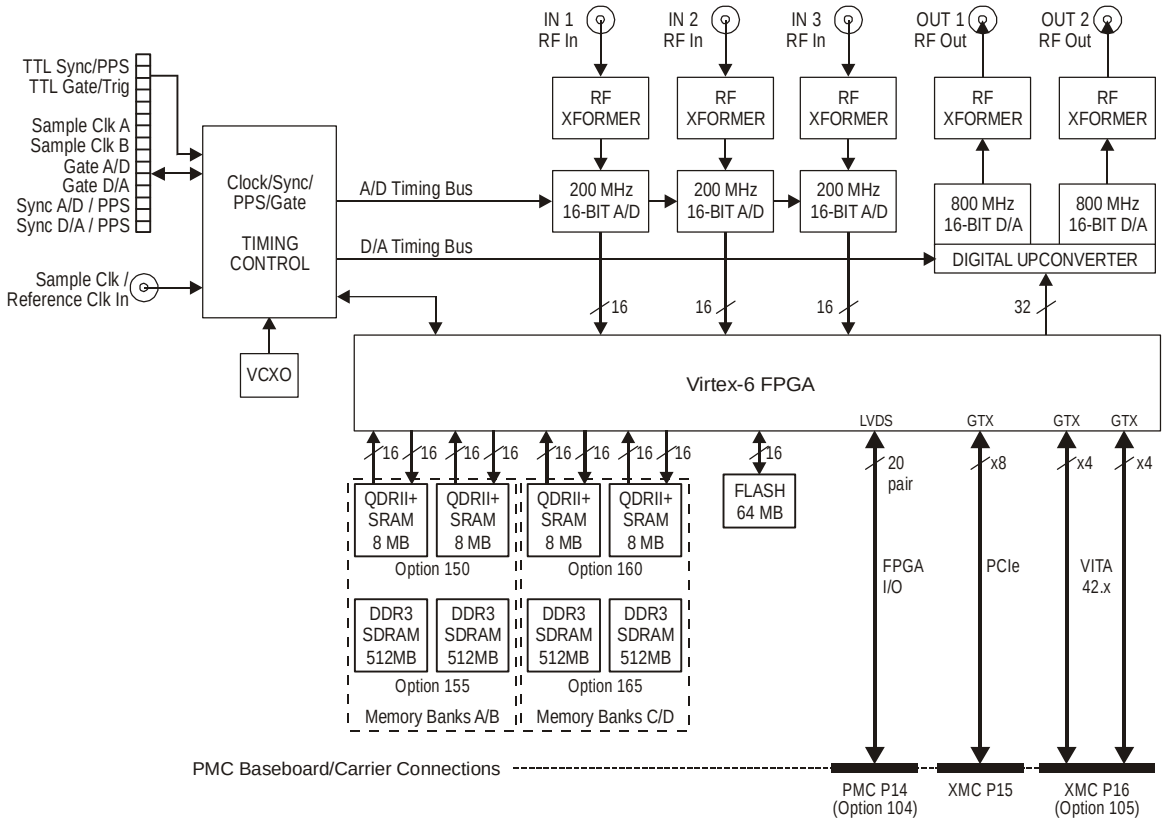


Figure 1–1: Model 71620 Block Diagram

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1.4 Principle of Operation

The Model 71620 is an A/D module suitable for direct connection to HF or IF ports of a communications or radar system. Using the popular XMC module format, it includes three A/D converters and two D/A converters.

The 71620 is compatible with VITA 42 XMC carrier boards. This emerging standard provides separate serial data links between the XMC and the carrier. These links support Serial RapidIO, PCI Express, and Aurora protocols and provide a dedicated high–speed streaming data path.

The 71620 features a Xilinx Virtex–6 FPGA for signal interfaces and processing. The FPGA is pre–configured to provide signal acquisition buffering functions. This FPGA also provides board interfaces including PCIe and XMC. Custom I/O connections are provided to the FPGA through the optional PMC P14 connector (Option 104). Custom gigabit serial interfaces may be implemented through the optional XMC P16 connector (Option 105).

Three 16–bit A/D converters provide data to the FPGA, where the data can be formatted, processed, or routed to board resources. Two D/A converters include both interpolation filters and an upconverter stage capable of producing baseband I & Q and quadrature modulation analog output.

The 71620 includes up to 32 MBytes of QDRII+ SRAM, or 2 GBytes of DDR3 SDRAM. This memory is controlled by the FPGA and is organized as two or four banks, depending on the 71620 options ordered. Separate banks (separate address and data per bank) allow simultaneous access to all banks. This memory can be used as data capture, as buffer memory when transferring data between board resources or to off–board resources, or as a memory resource for custom FPGA applications.

The 71620 includes an onboard VCXO and a programmable clock synthesizer for clocking, but can also accept external clocks through front panel connectors. The 71620 is equipped with an LVPECL front panel sync bus that allows synchronizing A/D and D/A processing on multiple modules.

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1.5 Analog to Digital Input Conversion

The Model 71620 is designed for a maximum input sampling frequency of 200 MHz. The front end accepts three full scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200−MHz, 16−bit A/D converters (ADCs). The ADC digital outputs are delivered into the FPGA for signal processing or for routing to other module resources.

1.6 Digital to Analog Output Conversion

A Texas Instruments DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate, and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16−bit D/A converter. Analog output is through a pair of front panel SSMC connectors. If translation is disabled, the DAC5688 acts as a dual interpolating 16−bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x, and 8x.

1.7 FPGA Digital Interfaces

The Model 71620 includes a Xilinx Virtex−6 FPGA. The FPGA serves as a control and status engine with data and programming interfaces to each of the onboard resources including the A/D converters and RAM memory. The FPGA is factory programmed by Pentek to implement the standard signal processing and control functions specified in this document. Pentek GateFlow® FPGA Design Kits facilitate integration of user−created IP with the factory shipped functions.

Option 104 adds PMC P14 LVDS connections to the FPGA for custom I/O. Option 105 adds XMC P16 gigabit serial connections to the FPGA for custom high−speed I/O.

1.8 FPGA Configurations

The Model 71620 includes a Xilinx Virtex−6 FPGA. Option 061 FPGA is a Xilinx XC6VLX130T, Option 062 is XC6VLX240T, Option 063 is XC6VLX365T, Option 064 is XC6VSX315T, and Option 065 is XC6VSX475T.

The 71620 is shipped with a default set of logic functions for the FPGA, on FLASH memory. The 71620 loads the FPGA configuration from FLASH memory at power−up. Up to four FPGA configurations can be stored in FLASH, identified as Version 0, Version 1, Version 2, and Version 3. Versions 0 and 1 are the Pentek−supplied default boot configuration (0 is the Gen 1 x4 PCIe code, 1 is the Gen 2 x4 PCIe code) and Versions 2 and 3 are reserved for user−defined configurations.

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1.9 Memory

Two or four independent banks of QDRII+ (Quad Data Rate II+) SRAM or DDR3 (Dou−ble Data Rate 3) SDRAM are available to the FPGA, depending on the Memory Option ordered. Built−in memory functions include ADC data buffering with post−triggering, and DAC waveform storage. Custom user−installed functions within the FPGA can take advantage of the memory for many other purposes. A 64−MByte FLASH memory supports booting and FPGA configuration.

1.10 Timing and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths. Each timing bus includes a clock, a sync, and a gate or trigger signal. An on−board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built−in clock synthesizer circuit to provide different A/D and D/A clocks. Alternatively, the sample clock can be sourced from an on−board programmable VCXO (Voltage−Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for syn−chronizing the internal oscillator.

A front panel 26−pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules. Multiple 71620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

1.11 XMC Baseboard Interfaces

The FPGA is connected to the XMC baseboard through an x8 Gen 1 PCI Express inter−face or x4 Gen 2 PCI Express interface. (x8 Gen 2 is possible with fast speed−grade FPGAs and custom design—call Pentek for details.) This interface includes multiple DMA controllers for efficient transfers to and from the module. Through this PCIe interface, any processor on the XMC baseboard can transfer data to or from any A/D converter or the D/A converter. Any PCIe Bus Master can control all programmable features on the board, including the A/D converters, the D/A converter, RAM memo−ries, and all FPGA memory map registers.

Interrupts can be asserted through this PCIe interface by A/D conversion, D/A con−version, A/D and D/A FIFO flags, Sync Bus gate, sync, or PPS signal transitions, clock loss, hardware over−temperature, or power supply over−voltage.

Option 105 provides two x4 or one x8 3.125 GHz secondary interface between the XMC and the baseboard/carrier. This link supports switched interconnect protocols includ−ing Serial RapidIO, PCI Express, and Aurora. The interface provides a dedicated high−speed streaming data path independent of the PCIe interface.

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1.12 Board Support Software

The FPGA is supported with a Pentek GateFlow® FPGA Design Kit. The GateFlow Design Kit (Model 4953 Option 162) facilitates user−installed FPGA functions using the Xilinx ISE Foundation tool suite. The FPGA Design Kit assists the user in configuring FPGA for implementing preprocessing functions such as convolution, framing, pattern recognition, or decompression.

Several Pentek software packages are available to speed development tasks for the Model 71620. Pentek's ReadyFlow® Board Support Libraries contain a set of C−language data structures and routines for accessing the Model 71620 programmable resources. Refer to the ReadyFlow documentation for the Model 71620, Pentek part #801.71620.

Pentek's ReadyFlow® Board Support Packages (BSP) contain software support for the Model 71620 XMC. This includes a device driver for the 71620, plus the ReadyFlow Board Support Library data structures and routines. The following available BSPs allow high−level programming for various workstation platforms. Refer to the software documentation indicated for each.

- Model 4994A Option 162 ReadyFlow BSP for Linux®, Pentek document #816.71620.
- Model 4995A Option 162 ReadyFlow BSP for Windows®, Pentek document #815.71620.
- Model 4996A Option 162 ReadyFlow BSP for VxWorks® (contact Pentek for availability)

1.13 Supporting Documentation

In addition to the operating instructions provided in this manual, copies of the following datasheets for the programmable devices on the Model 71620 are provided in the Pentek Model 7x620 Series Supplemental Manual, part number 809.7x620. This document is available on the CD provided by Pentek, in file **`8097x620.pdf`** (PDF format).

- ❑ Texas Instruments, Inc., ADS5485 Analog−to−Digital Converter Data Sheet
- ❑ Texas Instruments, Inc., DAC5688 D/A Upconverter Data Sheet
- ❑ National Semiconductor Corporation, LM83 Temperature Sensor Data Sheet
- ❑ National Semiconductor Corporation, LM73 Temperature Sensor Data Sheet
- ❑ Silicon Labs, Inc., Si571 Any−Rate VCXO Data Sheet
- ❑ Texas Instruments, Inc., CDC7005 Clock Synthesizer Data Sheet
- ❑ Xilinx Inc., Virtex−6 FPGA System Monitor Users Guide

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1.14 Specifications

Analog Signal Inputs

Quantity:	Three signal inputs
Connector Type:	Front panel SSMC connectors, **IN 1**, **IN 2**, & **IN 3**
Input Type:	Single–ended, non–inverting
Full Scale Input:	+8 dBm
Coupling:	Transformer coupled
Input Impedance:	50Ω
Analog Input Transformers:	
3dB Passband:	300 kHz to 700 MHz
Insertion Loss:	0.58 dB max.

Analog to Digital Converters

Quantity:	Three Texas Instruments ADS5485 A/D converters
Sampling Rate:	10–200 MHz
Resolution:	16 bits
Clock Source:	Sample clock source can be selected from onboard VCXO, front panel external clock, or LVPECL clock
A/D Data Reduction:	Data from the A/Ds can be written directly into the FPGA at a rate equal to the A/D clock decimated by any integer value between 1 and 65536

CAUTION: **Take care that the ADC clock never exceeds the ADS5485 rated clock speed (see Section 2.7.1).**

Analog Signal Output

Quantity:	Two signal outputs
Connector Type:	Front panel SSMC connectors, **OUT 1** & **OUT 2**
Output Type:	Single–ended, non–inverting
Coupling:	Transformer coupled
Output Impedance:	50Ω
Output Power:	+4 dBm
Analog Output Transformers:	
3dB Passband:	300 kHz to 700 MHz
Insertion Loss:	0.58 dB max.

Digital to Analog Upconverter

Quantity:	One Texas Instruments DAC5688 D/A converter
Sampling Rate:	500 MSPS in upconvert mode, 800 MSPS in D/A only mode
DAC Resolution:	16 bits
Input Data Rate:	0–250 MHz
Output Signal:	Analog, real or quadrature
Interpolation filters:	2x, 4x, 8x
Clock Source:	Sample clock source can selected be from onboard VCXO, front panel external clock, or LVPECL clock

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1.14 Specifications (continued)

Sync Bus Inputs/Outputs

Connector Type:	Front panel 26−pin connector, **SYNC/GATE**
Signals:	Clk A In/Out: 2 pins (LVPECL pair) Clk B In/Out: 2 pins (LVPECL pair) Gate A In/Out: 2 pins (LVPECL pair) Gate B In/Out: 2 pins (LVPECL pair) Sync A In/Out: 2 pins (LVPECL pair) Sync B In/Out: 2 pins (LVPECL pair) TTL Gate/Trig In: 1 pin (single−ended) TTL Sync/PPS In: 1 pin (single−ended) Grounds: 12 pins
Bus Master/Slave:	Bus master or bus slave mode selectable via software
Bus Termination:	Bus termination provided by in−line cable end terminator
Nr Boards Supported:	Up to four boards can be synchronized with a ribbon cable. Pentek's Model 7893 Synchronizer PCIe board allows synchronization of up to eight boards.

External Clock Input

Connector Type:	Front panel SSMC connector, **CLK**
Signal Type:	Sine wave or Square wave
Frequency Range:	10 to 800MHz (Must be divided down by CDC7005 for ADC when greater than 200MHz)
Voltage Range:	+0 to +10 dBm
Coupling:	AC coupled
Input Impedance:	50Ω

Clocks

Quantity:	Two separate input Clocks, Clk A & Clk B
Clock Source:	Selectable from external or internal clock
External:	Front panel Sync Bus LVPECL Clk A/B or EXT CLK IN
Internal:	Generated from programmable VCXO

Internal Sample Clock

Device:	Silicon Labs Si571 Any−Rate VCXO
Type:	Programmable VCXO
Frequency Range:	10−810 MHz
Start−Up Freq:	200 MHz
Freq Resolution:	0.09 ppb
Interface:	FPGA TWSI (I^2C) Bus 1

Clock Synthesizer

Type:	Texas Instruments CDC7005
Frequency Dividers:	1, 2, 4, 8, and 16
Output Clocks:	Five LVPECL output clocks
Interface:	FPGA registers

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1.14 Specifications (continued)

Gates

Quantity:	Two separately controllable gates, Gate A (for ADCs) & Gate B (for DAC)
Gate Sources:	Each gate selectable from external or internal gates
External:	Front panel Sync Bus LVPECL Gate A/B or TTL Gate
Internal:	Generated from programmable registers (A & B)
Gate Polarity:	Programmable polarity for external gates
Triggering:	Each gate can be programmed as a trigger with a programmable trigger length

Syncs

Quantity:	Two separately controllable syncs, Sync A (for ADCs) & Sync B (for DAC)
Sync Source:	Selectable from external or internal syncs
External:	Front panel Sync Bus LVPECL Sync A/B or TTL Sync
Internal:	Generated from programmable registers (A & B)
Sync Pulse Width:	2 clock cycles, minimum

Sync can also be used as a PPS input

Field–Programmable Gate Array

Device:	
Option 061:	Xilinx Virtex–6 XC6VLX130T
Option 062:	Xilinx Virtex–6 XC6VLX240T
Option 063:	Xilinx Virtex–6 XC6VLX365T
Option 064:	Xilinx Virtex–6 XC6VSX315T
Option 065:	Xilinx Virtex–6 XC6VSX475T
Configuration:	Factory programmed by Pentek: A/D, D/A, RAM Memory, FIFOs

RAM memory

Memory Module 1	
Option 150:	16 MB QDRII+ SRAM, 2 banks of 4M x 16
Option 155:	1 GB DDR3 SDRAM, 2 banks of 128M x 32
Memory Module 2	
Option 160:	16 MB QDRII+ SRAM, 2 banks of 4M x 16
Option 165:	1 GB DDR3 SDRAM, 2 banks of 128M x 32
Speed & Bus Width:	
QDRII+:	400 MHz clock rate 16 bits read, 16 bits write
DDR3:	400 MHz clock rate 32–bit bus
Interface:	FPGA

Configuration FLASH memory

Size:	64 MBytes
Bus Width:	16 bits
Interface:	FPGA memory map

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1.14 Specifications (continued)

XMC Interfaces

PCI Express Interface

XMC Connector:	114–pin (XMC standard Pn5 connector), **P15**
Compliance:	VITA 42.3 XMC PCI Express Protocol Standard
Lanes/Speed:	Gen1 x8 – 2 GB/sec Gen2 x4 – 2 GB/sec Gen2 x8 – 4 GB/sec * * Gen 2 x8 is possible with some select FPGA types and speed grades. Factory–default configuration for this speed is not currently available.

Secondary XMC Interface (Option 105)

XMC Connector:	114–pin (XMC standard Pn6 connector), **P16**
Compliance:	VITA 42.0 XMC Standard
Protocol:	VITA 42.2 XMC Serial RapidIO Protocol Standard * VITA 42.3 XMC PCI Express Protocol Standard * VITA 42.5 Aurora Pin Assignments *

* User must implement these protocols with user FPGA code

PMC Interface (Option 104)

PMC Connector:	64–pin PMC standard Pn4 connector, **P14**
Compliance:	40 I/O lines routed as 20 LVDS pairs to the FPGA

Temperature and Voltage Sensors

Main PCB Temperature

Quantity:	Three temperature sensors
Controller:	National Semiconductor LM83
Interface:	FPGA TWSI (I^2C) Bus 1

Front Panel Interface Module Temperature

Quantity:	Three temperature sensors
Controller:	National Semiconductor LM83
Interface:	FPGA TWSI (I^2C) Bus 1

Memory Module Temperature

Quantity:	One sensor per module
Controller:	National Semiconductor LM73
Interface:	FPGA TWSI (I^2C) Bus 1

Voltage

Quantity:	Six voltage sensors
Controller:	Virtex–6 System Monitor
Interface:	FPGA registers

Estimated Power Consumption

Current Draw:	**+3.3V**	**VPWR (12V or 5V)**	**Total Power**
XC6VLX130T	2A	1.95A@12V or 4.7A@5V	30W
XC6VLX240T	2.3A	2A@12V or 4.8A@5V	32W
XC6VLX365T	TBD		
XC6VSX315T	TBD		

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1.14 Specifications (continued)

Physical

Dimensions: Single PMC/XMC board dimensions as defined by IEEE P1386 Common Mezzanine Card Specification

Depth: 149.0 mm (5.87 in)

Height: 74 mm (2.91 in)

Weight: Approximately 14 oz (400 grams), with 2−slot heatsink

Environmental

Pentek Ruggedization Level L1

Pentek Option Number:	−701 (default)
Cooling Method (operational):	Forced Air
Operating Temperature:	0° to 50° C
Storage Temperature:	−40° C to +100° C
Sine Vibration:	2g, 20−500 Hz
Random Vibration:	$0.01g^2$/Hz, 20−2000 Hz
Shock:	10g, 11ms
Relative Humidity:	0 to 95% non−condensing

Pentek Ruggedization Level L2

Option Number:	−702
Cooling Method (operational):	Forced Air
Operating Temperature:	−20° to 65° C
Storage Temperature:	−40° C to +100° C
Sine Vibration:	2g, 20−500 Hz
Random Vibration:	$0.04g^2$/Hz, 20−2000 Hz
Shock:	20g, 11ms
Relative Humidity:	
No conformal coating:	0% to 95% non−condensing
Conformal coating (Option 720):	0% to 100% non−condensing

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Chapter 2: Installation and Connections

2.1 Inspection

After unpacking, inspect the unit carefully for possible damage to connectors or components. If any damage is discovered, contact Pentek immediately at (201) 818–5900. Please save the shipping container and packing material in case reshipment is required.

An assembly drawing of the Model 71620 is provided below, showing the complete 71620 PCB assembly as shipped, with the front panel I/O interface and two optional memory modules mounted onto to the main PCB.

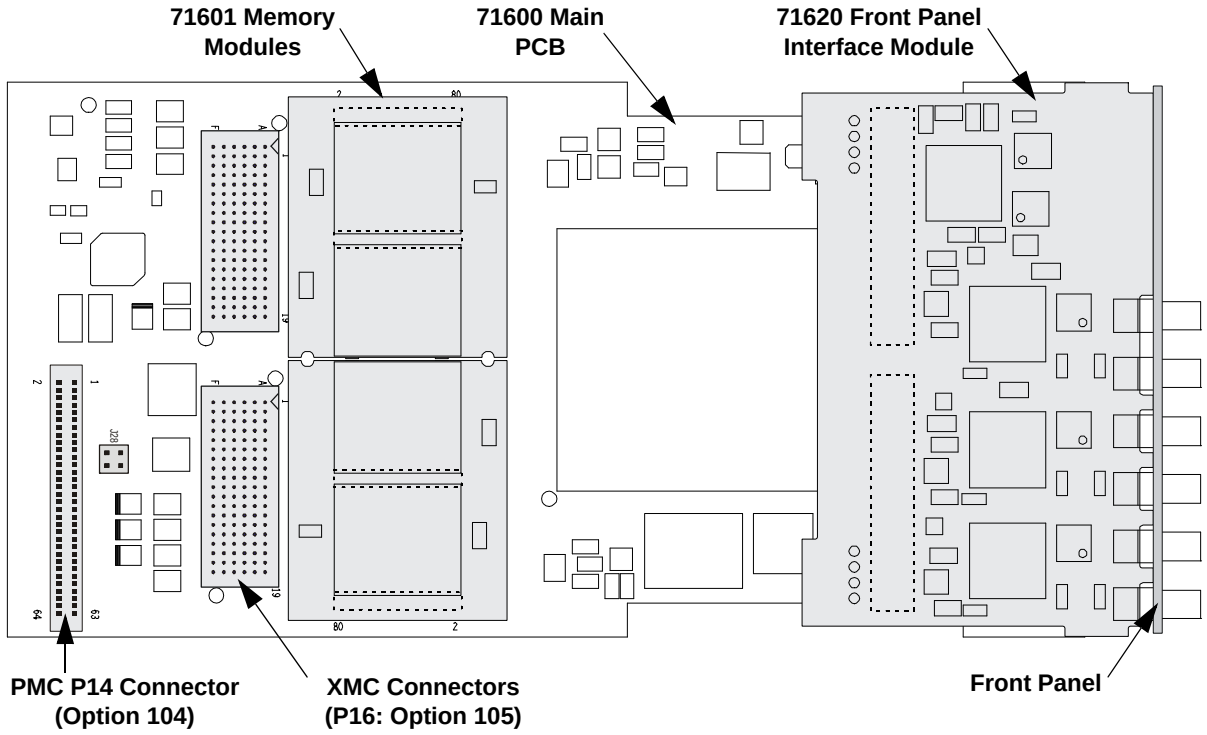


Figure 2–1: Model 71620 PCB Assembly Drawing, Connector Side

Note that a heat sink may be mounted on the 71620 PCB assembly as shipped.



The Model 71620 is shipped to boot with the Gen 1 x8 PCIe default FPGA code. If you want a different default, see Section 2.2.2.

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2.2 DIP Switch Settings

The following subsections describe user operating parameters that are set by two DIP switches, identified as **SW1** and **SW2**, on the Model 71620 PCB.

As shipped from the factory, all switches are set in default positions on your board. The default operating parameters they select may or may not meet your requirements. Before installing your Model 71620 onto an XMC baseboard, please review the following subsections to determine whether you need to change any of these settings.

The user should not change any switches that are not described in the following sections—those are reserved for factory test and setup purposes only.

All user switches are located on the solder side of the Model 71620 main PCB (Pentek part number 320–71600), and are accessible while the heat sink is mounted on the PCB. An assembly drawing of the solder side of the main PCB is provided below, showing the location of switches **SW1** and **SW2** on the PCB.

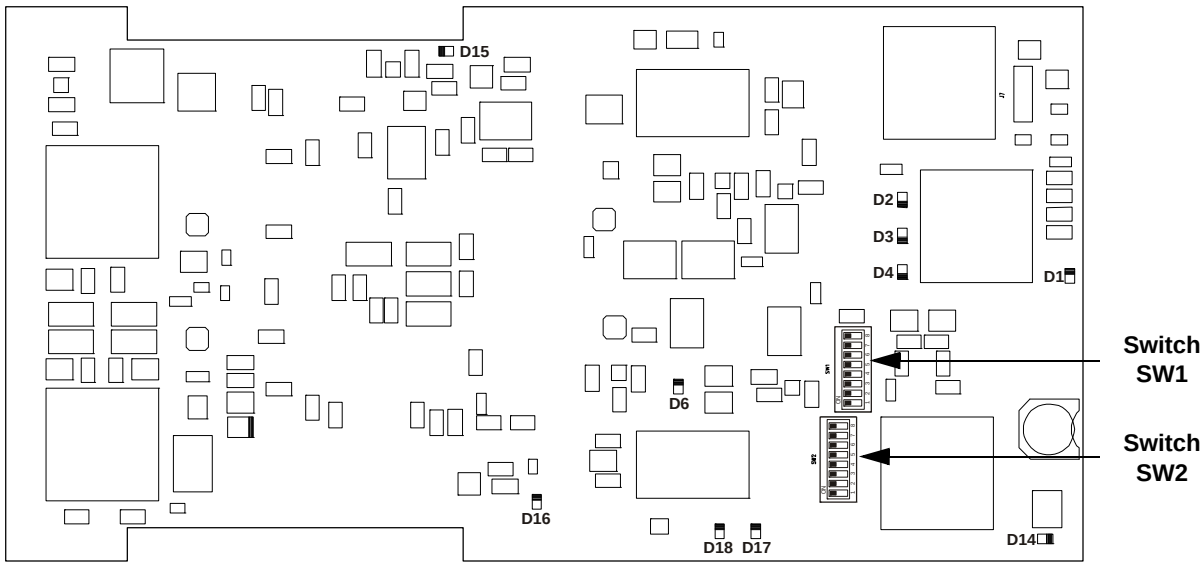


Figure 2–2: Model 71620 Main PCB Assembly Drawing, Solder Side

Note that several user LEDs are located on the solder side of the 71620 PCB. Refer to Section 2.4, on page 35 for description of these LEDs.

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2.2 DIP Switch Settings (continued)

2.2.1 Switch SW1 – FPGA MGT Clock Operation

Switch **SW1** provides user control over the FPGA MGT clocks used for the XMC interface. The following table shows the settings for this switch. Refer to Figure 2–3 on the next page for a block diagram of FPGA MGT clock logic.

CAUTION

Use ballpoint tip only for setting DIP switches.

DO NOT USE paper clips, tweezers, or any other sharp objects, as they may damage the switch.

Table 2–1: SW1 – FPGA MGT Clock Operation

Switch	Function	ON	OFF
SW1–1	Primary PCIe Clock Frequency **	100 MHz	250 MHz *
SW1–2	Secondary PCIe Clock Frequency	100 MHz	250 MHz *
SW1–3	Auxiliary MGT Clocks (A/B/C) Frequency	See Table 2–2 below	
SW1–4			
SW1–5	Secondary PCIe Clock Disable	Disabled *	Enabled
SW1–6	Auxiliary MGT Clocks (A/B/C) Disable	Disabled *	Enabled
SW1–7	Primary PCIe Clock Source	XMC CLK0 *	250 MHz Crystal
SW1–8	Secondary PCIe Clock Source ***	XMC CLK1 *	AUX_MGT_CLK_A

* Factory Default Settings

Note: Primary and Secondary PCIe Clock Frequencies – 100 MHz XMC clock source is converted to 250 MHz in the default position.

** Switch **SW1–1** must be in the **OFF** (250 MHz) position for Pentek factory FPGA code and for any x8 or Gen 2 design.

*** Switch **SW1–8**, when in the **ON** position clock source is the Option 105 XMC P16 connector – if option 105 is not installed switch must be in the **OFF** position.

Table 2–2: Aux MGT Clock Frequency – Switches SW1–3:4

SW1–3	SW1–4	Aux MGT Clk A/B	Aux MGT Clk C
OFF *	OFF *	312.5 MHZ	125 MHz
ON	OFF	156.25 MHz	125 MHz
OFF	ON	125 MHz	156.25 MHz
ON	ON	156.25 MHz	156.25 MHz

* Factory Default Setting

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2.2 DIP Switch Settings (continued)

2.2.1 Switch SW1 – FPGA MGT Clock Operation (continued)

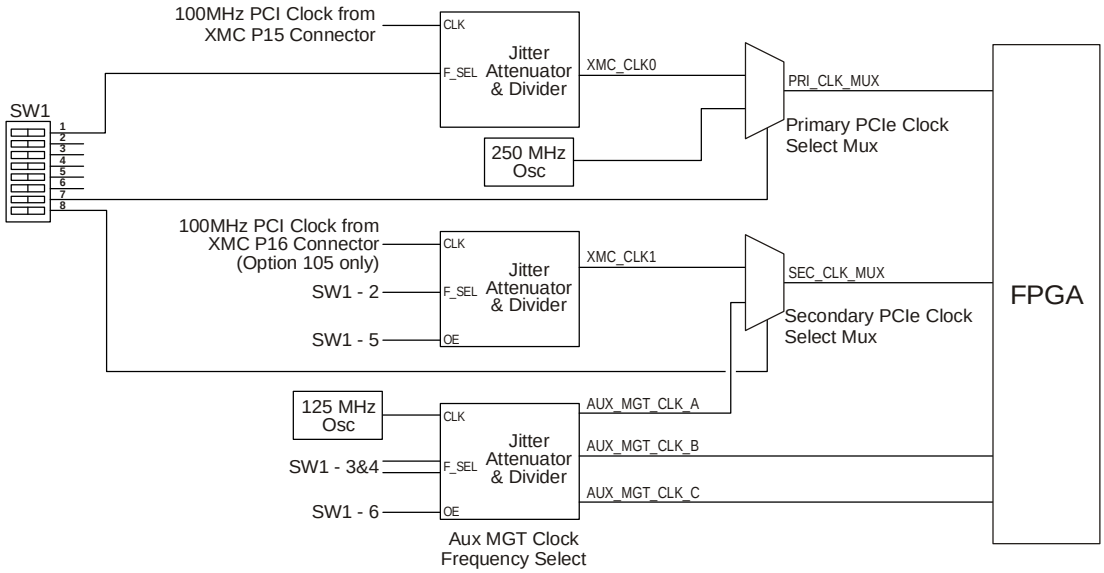


Figure 2–3: Model 71620 FPGA MGT Clock Logic

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2.2 DIP Switch Settings (continued)

2.2.2 Switch SW2 – FPGA Configuration

Switch **SW2** controls access to the FPGA configuration functions. The following table shows the settings for this switch.

CAUTION

Use ballpoint tip only for setting DIP switches.

DO NOT USE paper clips, tweezers, or any other sharp objects, as they may damage the switch.

Table 2–3: SW2 – FPGA Configuration

Switch	Function	ON	OFF
SW2–1	FLASH Memory Write Protect/Write Enable	Write Protected *	Write Enabled
SW2–2	Factory use only – should always be set to **ON**		
SW2–3	Select Boot Configuration at power on	See Table 2–4 below	
SW2–4			
SW2–5	Factory use only – should always be set to **OFF**		
SW2–6	no function	–	–
SW2–7	XMC JTAG Enable	XMC JTAG	Board JTAG *
SW2–8	Select whether JTAG chain includes Memory	FPGA & Memory	FPGA Only *
	Note: Factory use only – should always be set to **OFF**, FPGA only.		

* Factory Default Settings

Table 2–4: FPGA Configuration Select – Switches SW2–3:4

SW2–3	SW2–4	Configuration Select (FLASH)
ON *	ON *	Version 0 Boot Code – Gen 1 x8 PCIe
OFF	ON	Version 1 Boot Code – Gen 2 x4 PCIe
ON	OFF	Version 2 Boot Code
OFF	OFF	Version 3 Boot Code

* Factory Default Setting
See Section 3.8 for description of FLASH Memory use.

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2.3 PCB Jumpers

The following describes user operating parameters that are set by jumper block **J28** on the Model 71620 PCB. This jumper block is located on the connector side of the Model 71620 main PCB (Pentek part number 320–71600). An assembly drawing of the connector side of the PCB is provided below, showing the location of jumper block **J28**.

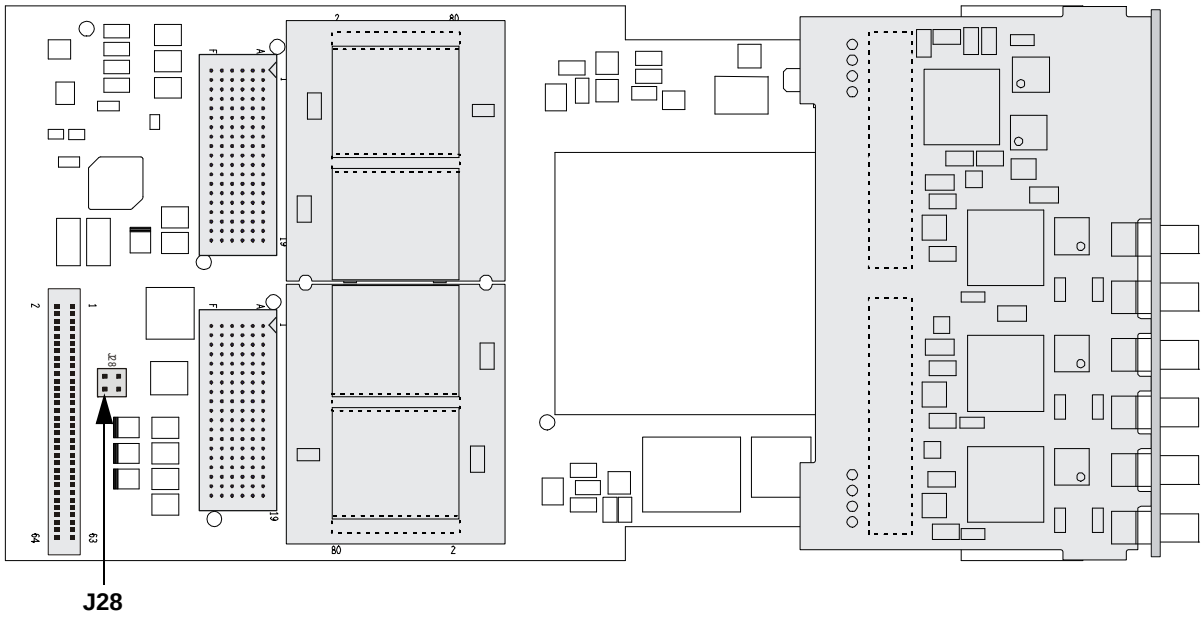


Figure 2–4: Model 71620 PCB Jumpers, Connector Side

NOTE: You must set **J28** before the XMC module is mounted on a PCIe carrier.

Table 2–5: Virtex–6 Program eFUSE Enable – Jumper Block J28

Jumper Pins	Function	Installed	Removed
Pins 1 – 3	Virtex–6 Program eFUSE	Enabled	Disabled *
Pins 2 – 4	no function	–	–
* Factory Default Setting			

Jumper **J28**, pins 1–3, are used to program eFUSE in the Virtex–6 FPGA. Refer to the Xilinx Virtex–6 FPGA Configuration Guide (Xilinx document UG360) for further information about using this capability.

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2.4 PCB LEDs

The following describes the Model 71620 PCB LEDs, labeled **Dnn**, that provide general operating status for the board. These LEDs are positioned on the solder side of the Model 71620 main PCB, as illustrated below, and are visible through the heat sink mounted on the PCB. The use of each LED is indicted in Table 2–6 below.

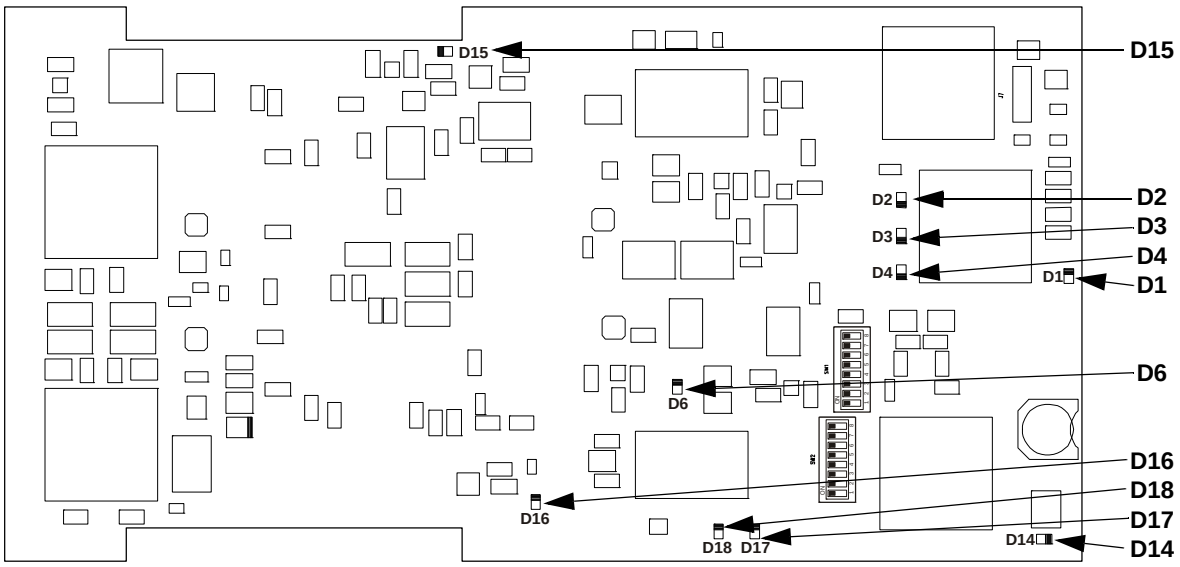


Figure 2–5: Model 71620 PCB LEDs, Solder Side

Table 2–6: PCB LED Use

LED	USE
D1	Yellow LED indicates PCI Express Gen 2 operation
D2 & D3	Yellow LEDs indicate PCI Express Active Lanes:
D4	Green LED indicates PCI Express link has been established
D6	Green LED for user applications – see LED Control Register, Section 5.22
D14	Red LED indicates temperature fault from the main PCB LM83, Section 5.32.1
D15	Red LED indicates temp/volt fault from the FPGA System Monitor, Section 3.7.1
D16	Green LED indicates FPGA configuration done
D17	Red LED indicates FPGA configuration error
D18	Yellow LED indicates FPGA configuration active

	x1	x2	x4	x8
D2	Off	On	Off	On
D3	Off	Off	On	On

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2.5 Baseboard Connectors

The following subsections describe the baseboard PMC/XMC connectors on the 71620 PCB. Refer to Figure 2–1 on page 29 for the location of these connectors on the PCB.

2.5.1 XMC Connectors

The Model 71620 provides an XMC high–speed serial connector, identified as **P15**, that complies with the VITA 42.3 XMC Standard. This primary interface is configured as either an x4 or x8 PCI Express Gen 1 or Gen 2.

Option 105 for the 71620 provides high–speed serial connections from FPGA spare pins using XMC connector **P16**. This connector complies with the VITA 42.0 XMC Standard and can support various interfaces including VITA 42.2 Serial RapidIO, VITA 42.3 PCI Express, or VITA 42.5 Aurora.

The FPGA to XMC **P16** pin connections are identified below.

Table 2–7: Option 105 XMC P16 FPGA Pin Connections

Pin	A	B	C	D	E	F
01	S2_TD_P0	S2_TD_N0	n/c	S2_TD_P1	S2_TD_N1	n/c
02	GND	GND	n/c	GND	GND	n/c
03	S2_TD_P2	S2_TD_N2	n/c	S2_TD_P3	S2_TD_N3	n/c
04	GND	GND	n/c	GND	GND	n/c
05	S3_TD_P0	S3_TD_N0	n/c	S3_TD_P1	S3_TD_N1	n/c
06	GND	GND	n/c	GND	GND	n/c
07	S3_TD_P2	S3_TD_N2	n/c	S3_TD_P3	S3_TD_N3	n/c
08	GND	GND	n/c	GND	GND	n/c
09	n/c	n/c	n/c	n/c	n/c	n/c
10	GND	GND	n/c	GND	GND	n/c
11	S2_RD_P0	S2_RD_N0	n/c	S2_RD_P1	S2_RD_N1	n/c
12	GND	GND	n/c	GND	GND	n/c
13	S2_RD_P2	S2_RD_N2	n/c	S2_RD_P3	S2_RD_N3	n/c
14	GND	GND	n/c	GND	GND	n/c
15	S3_RD_P0	S3_RD_N0	n/c	S3_RD_P1	S3_RD_N1	n/c
16	GND	GND	n/c	GND	GND	n/c
17	S3_RD_P2	S3_RD_N2	n/c	S3_RD_P3	S3_RD_N3	n/c
18	GND	GND	n/c	GND	GND	n/c
19	XMC_REFCLK1_P	XMC_REFCLK1_N	n/c	n/c	n/c	n/c

Sn_TD_Pm, Sn_TD_Nm = Serial Transmit, FPGA Auxiliary Port n, lane m
Sn_RD_Pm, Sn_RD_Nm = Serial Receive, FPGA Auxiliary Port n, lane m

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2.5 Baseboard Connectors (continued)

2.5.2 PMC FPGA Connections (Option 104)

Option 104 for the Model 71620 provides connections from FPGA spare pins to the baseboard or carrier using PMC connector **P14**. These connections are programmed for low–voltage differential signals (LVDS) in the default FPGA configuration; the user can reconfigure these pins with custom FPGA programming (refer to Section 1.8, FPGA Configuration).



The P14 signals can be configured in the FPGA as either LVDS or LVTTL but in either case are limited to 2.5V, and also cannot be driven with a negative voltage.

The following table identifies the LVDS signals that are connected from the FPGA to the PMC **P14** connector pins. Pins 41 through 63 are not connected.

Table 2–8: Option 104 PMC P14 FPGA Pin Connections

FPGA Signal	PMC P14 Pin	FPGA Signal	PMC P14 Pin
P4_LVDS_IN_N0	2	P4_LVDS_OUT_N0	1
P4_LVDS_IN_P0	4	P4_LVDS_OUT_P0	3
P4_LVDS_IN_N1	6	P4_LVDS_OUT_N1	5
P4_LVDS_IN_P1	8	P4_LVDS_OUT_P1	7
P4_LVDS_IN_N2	10	P4_LVDS_OUT_N2	9
P4_LVDS_IN_P2	12	P4_LVDS_OUT_P2	11
P4_LVDS_IN_N3	14	P4_LVDS_OUT_N3	13
P4_LVDS_IN_P3	16	P4_LVDS_OUT_P3	15
P4_LVDS_IN_N4	18	P4_LVDS_OUT_N4	17
P4_LVDS_IN_P4	20	P4_LVDS_OUT_P4	19
P4_LVDS_IN_N5	22	P4_LVDS_OUT_N5	21
P4_LVDS_IN_P5	24	P4_LVDS_OUT_P5	23
P4_LVDS_IN_N6	26	P4_LVDS_OUT_N6	25
P4_LVDS_IN_P6	28	P4_LVDS_OUT_P6	27
P4_LVDS_IN_N7	30	P4_LVDS_OUT_N7	29
P4_LVDS_IN_P7	32	P4_LVDS_OUT_P7	31
P4_LVDS_IN_N8	34	P4_LVDS_OUT_N8	33
P4_LVDS_IN_P8	36	P4_LVDS_OUT_P8	35
P4_LVDS_IN_CLK_N11	38	P4_LVDS_OUT_CLK_N11	37
P4_LVDS_IN_CLK_P11	40	P4_LVDS_OUT_CLK_P11	39

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2.6 Installing the Model 71620 on an XMC Baseboard

The Model 71620 mounts on the connector side of an XMC baseboard or carrier. Refer to the operating manual supplied with your baseboard for any specific mounting instructions. A typical XMC baseboard is illustrated in Figure 2–6 below.

CAUTION

REMOVE POWER to the XMC baseboard before installation!

Note

The Model 71620 requires both a 3.3V and a 5V or 12V power supply (12V is recommended).

Ensure that the XMC baseboard or carrier you are using has both a 3.3V and a 5V or 12V power supply.

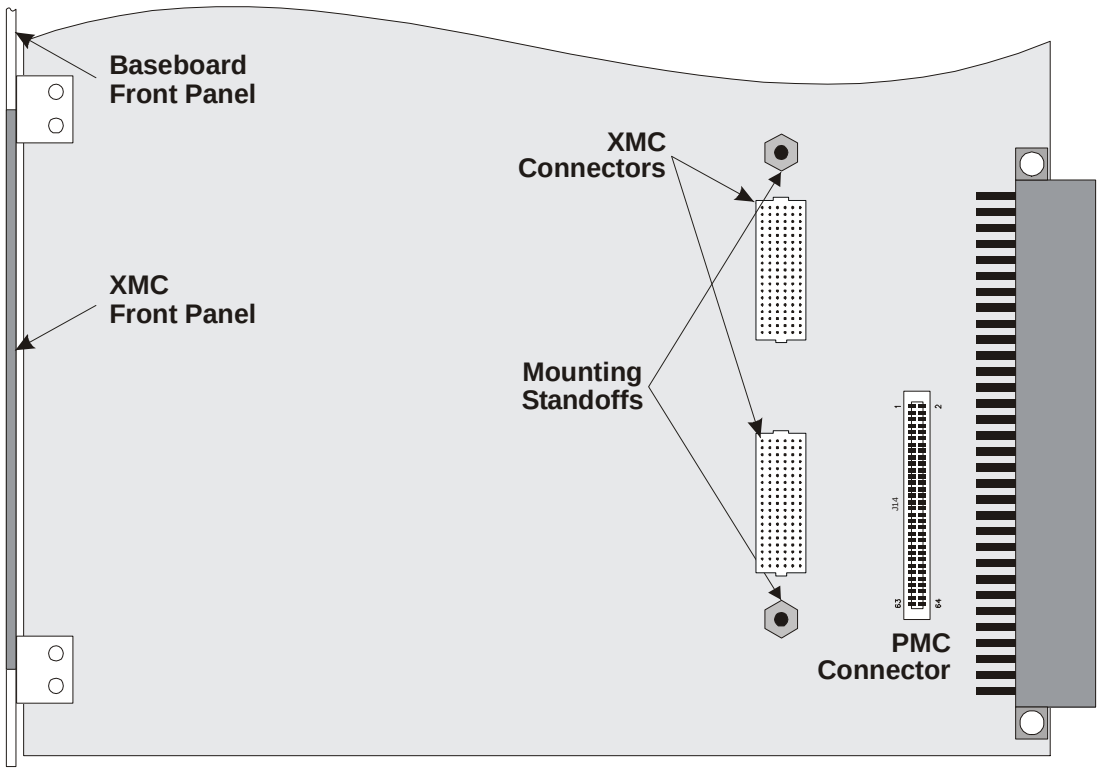


Figure 2–6: Typical XMC Baseboard – Connectors & Mounting Hardware

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2.6 Installing the Model 71620 on an XMC Baseboard (continued)

Installation instructions:

1) Attach an ESD strap to your wrist—attach the other end to a ground source. The ESD strap must be secured both to your wrist and to ground throughout the procedure.

2) Pentek XMC baseboards are supplied with module standoffs and mounting screws installed. Ensure that the standoffs on your baseboard are installed at the locations shown in Figure 2–7 below and Figure 2–6 on the prior page.

3) Remove the blank module front panel from the front panel of the XMC baseboard (see Figure 2–6 on the prior page).

4) Position the Model 71620 front panel into the opening from behind the baseboard front panel, and position the module so that the 71620 XMC connectors are over the XMC connectors on the baseboard (see illustration below).

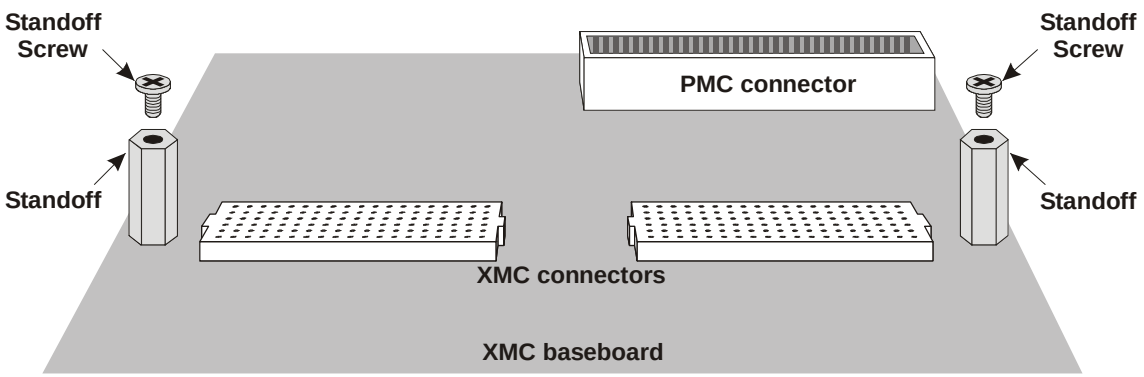


Figure 2–7: Baseboard PMC/XMC Connections

5) **GENTLY but firmly**, press down on the 71620 module opposite the connectors to fully seat the module's connectors into the baseboard. The connectors on the underside of the 71620 PCB should connect smoothly with the corresponding connectors on the baseboard.

6) Using two flat–head Phillips standoff screws (supplied with the 71620), secure the Model 71620 PCB, through the PCB's standoff holes, to the baseboard's standoffs (see Figure 2–7 above).

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2.7 Front Panel Connections

The Model 71620 XMC front panel, illustrated in the figure at the right, includes six SSMC coaxial connectors for input/output of clock and analog signals, and a 26–pin Sync Bus input/output connector. These connectors are described in the following subsections.

The front panel also includes ten LED indicators, which are described in Section 2.8, on page 43.

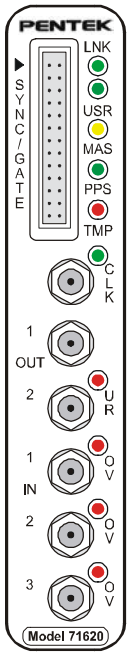


Figure 2–8: Model 71620 Front Panel

2.7.1 Clock Input Connector CLK

The front panel has one SSMC coaxial connector, labeled **CLK**, for input of an external sample clock. The external clock signal must be a sine wave or square wave of +0 dBm to +10 dBm, with a frequency range from 10 to 800 MHz.

The external clock input can be used as the sample clock signal for the A/D and D/A converters. This input is enabled using the Sync Bus Control Register 1 CLK SEL bits (see Section 5.17.9). The selected clock source is input to a CDC7005 Clock Synthesizer (see Sections 5.14 and 5.15) that generates separate output clocks, each programmable as submultiples of the input frequency. One CDC7005 output clock (Y0) provides ADC timing, one clock (Y1) provides DAC timing.

CAUTION

Take care that the ADC clock never exceeds the ADS5485 rated clock speed during any change of frequency with the input clock signal.

– If you are increasing the external input frequency, first reprogram the appropriate CDC7005 divider so that the ADS5485 clock does not exceed 200 MHz.

– If you are decreasing the input frequency, do not reprogram the CDC7005 divider until the input has been reprogrammed so that the ADS5485 clock does not exceed 200 MHz.

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2.7 Front Panel Connections (continued)

2.7.2 Analog Output Connectors **OUT 1, 2**

The front panel has two SSMC coaxial connectors for analog signal outputs, labeled **OUT 1** and **2**, one for each DAC5688 output.

The analog output signal is within the range of +4 dBm. This output is driven by an RF transformer into 50Ω output impedance.

2.7.3 Analog Input Connectors **IN 1, 2, 3**

The front panel has three SSMC coaxial connectors for analog signal inputs, labeled **IN 1, 2**, and **3**, one for each ADC input channel.

The analog input signal has a full−scale level of +8 dBm. Each input drives an RF transformer, with 50Ω input impedance.

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2.7 Front Panel Connections (continued)

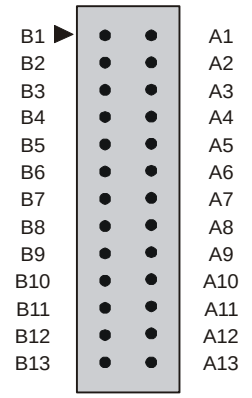
2.7.4 Sync Bus Connector SYNC/GATE

The 26–pin Sync Bus front panel connector, labeled **SYNC/GATE**, provides clock, sync, and gate input/output pins for the Low–Voltage Positive Emitter–Coupled Logic (LVPECL) Sync Bus. When the Model 71620 is a bus Master, these pins output LVPECL Sync Bus signals to other slave units. When the 71620 is a bus Slave, these pins input LVPECL signals from a bus Master. This connector also accepts two Low–Voltage TTL (LVTTL) Gate/Sync inputs.

The following table shows the **SYNC/GATE** connector pin configuration. The mating 26–pin connector is Pentek Model 2140–998.

Table 2–9: SYNC/GATE Connector Pins

Signal	Pin		Pin	Signal
LVTTL GATE/TRIG	B1		A1	GND
LVTTL SYNC/PPS	B2		A2	GND
LVPECL GATE A–	B3		A3	LVPECL GATE A+
GND	B4		A4	GND
LVPECL SYNC A–	B5		A5	LVPECL SYNC A+
GND	B6		A6	GND
LVPECL CLK A–	B7		A7	LVPECL CLK A+
GND	B8		A8	GND
LVPECL GATE B–	B9		A9	LVPECL GATE B+
GND	B10		A10	GND
LVPECL SYNC B–	B11		A11	LVPECL SYNC B+
GND	B12		A12	GND
LVPECL CLK B–	B13		A13	LVPECL CLK B+





When connecting LVPECL Sync Bus pins to additional Model 71620 modules, the LVPECL pins on the LAST unit must be terminated. Pentek includes a terminating board with your shipment for this purpose, Pentek Model 2140–999.



The LVTTL Gate/Trig and Sync/PPS signals are 5V tolerant but they must NOT have any negative voltage applied. They are terminated with a 392–Ohm resistor to 3.3V and a 392–Ohm resistor to ground.

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2.8 Front Panel LEDs

The Model 71620 front panel has ten LED indicators, as illustrated in Figure 2–8.

2.8.1 Link LED **LNK**

The green **LNK** LED illuminates when a valid link has been established over the PCIe interface.

2.8.2 User LED **USR**

The green **USR** LED is for user applications. Use the LED Control Register USER LED SRC bits (see Section 5.22) to select the signal source for this LED.

2.8.3 Master LED **MAS**

The yellow **MAS** LED illuminates when this Model 71620 is the Sync Bus Master (see Sync Bus Control Register 1, Section 5.17). When only a single 71620 is used, it must be a Master.

2.8.4 PPS LED **PPS**

The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal. Use the LED Control Register PPS LED SRC and DISABLE bits (see Section 5.22) to control this LED.

2.8.5 Over Temperature LED **TMP**

The red **TMP** LED illuminates when an over–temperature or over–voltage condition is indicated by any of the temperature/voltage sensors on the Model 71620 PCB.

2.8.6 Clock LED **CLK**

The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed. Use the LED Control Register CLK DET LED CTRL bits (see Section 5.22) to select the source for this LED.

2.8.7 DAC Underrun LED **UR**

There is one red underrun **UR** LED for the D/A output. This LED illuminates when the DAC5688 FIFO is out of data.

2.8.8 ADC Overload LEDs **OV**

There are three red **OV** LEDs, one for each A/D input. Use the ADC Data Control Register (see Section 6.4) to select the signal source for each LED, either an overload in the associated ADS5485, or an ADC FIFO overrun.

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Chapter 3: Model 71620 Resource Operation

3.1 Overview

This chapter describes operation of the Model 71620 resources from an XMC baseboard processor. An overall data flow of the 71620 data flow is provided below.

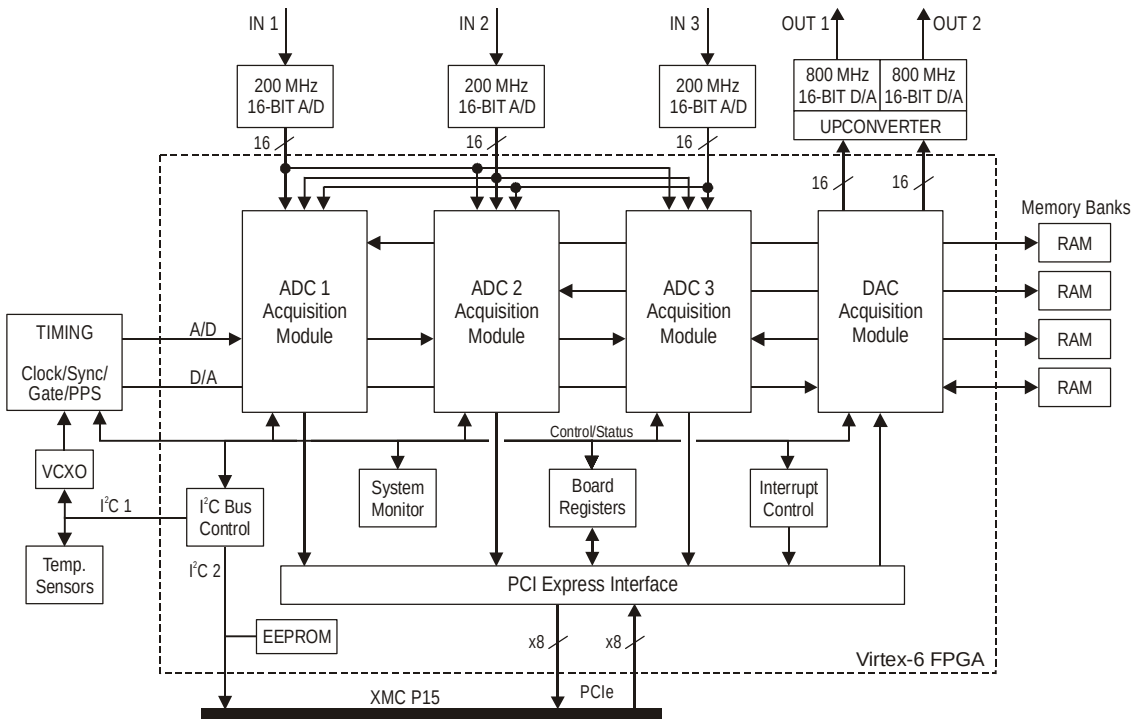


Figure 3–1: Model 71620 Data Flow

Several of these functional blocks are described in the following sections.

- See Section 3.2 for description of the Analog to Digital Input Operation.
- See Section 3.3 for description of the Digital to Analog Output Operation.
- See Section 3.4 for description of RAM Memory Operation.
- See Section 3.5 for description of Timing and Synchronization Operation.
- See Section 3.6 for description of Interrupt Operation.
- See Section 3.7 for description of FPGA Resources (System Monitor, I^2C).

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3.2 Analog to Digital Input

The Model 71620 accepts three analog RF inputs at +8 dBm full scale into 50 ohms on front panel connectors, labeled **IN 1**, **2**, and **3**. Each of the three inputs is transformer coupled, digitized by a Texas Instruments ADS5485 200−MHz, 16−bit A/D converter (ADC), and then routed to one of the three ADC channel acquisition modules. Refer to the TI ADS5485 data sheet (see Section 1.13) for description of ADS5485 operation.

Each of the three ADC acquisition modules has several inputs that can be selected: any of the three ADS5485 digital inputs, a loopback of the DAC output digital data, and a digital test signal provided by an onboard sinewave generator. Each ADC acquisition module is referred to as an ADC Channel in this manual.

Using an Input Linked List Engine, each ADC Channel routes the selected 16−bit digital data to a data packing function and then to an ADC PACK FIFO. Alternately, the raw 16−bit data can be sent to a User Block for processing by user−defined or pre−installed FPGA IP code, then to the packing function and FIFO. See Section 3.2.1 for description of the data packing formats, and Section 3.2.2 for description of the Input Linked List operation. Data from the ADC FIFO can be routed to the optional RAM memory. The packed data can be read from the PACK FIFO or RAM memory through the PCIe interface using an Input DMA Engine. See Section 3.2.3 for description of the Input DMA operation.

The following is a simplified block diagram of the analog to digital input data flow for one of the three A/D input channels. Examples of A/D signal processing applications are provided in Appendix B.

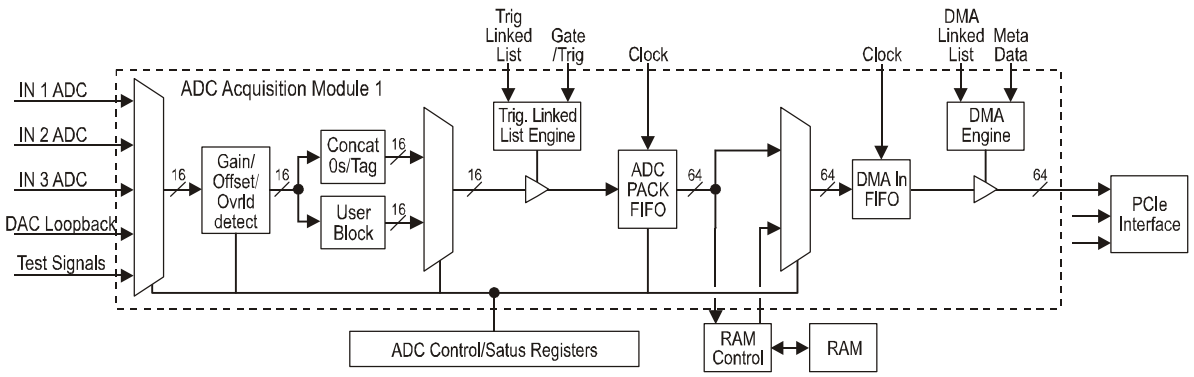


Figure 3−2: Analog to Digital Input Channel Data Flow

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3.2 Analog to Digital Input (continued)

3.2.1 ADC Data Packing Formats

Each ADS5485 ADC provides 16–bit digital data to a packing function for an ADC PACK FIFO. Alternately, the 16–bit ADS5485 data can be sent to a User Block for processing by user–defined or pre–installed FPGA IP code, and then routed to data packing for the PACK FIFO. (The User Block can be configured with one of a variety of IP cores for custom signal processing, such as Digital Down–Converters; contact Pentek for further information on these IP cores.) Use the associated ADC Data Control Register, Section 6.4, USR DATA SEL bit, to select the data source for the packing function.

Note that if you select ADS5485 ADC as the data source, the ADS5485 raw data samples are handled as Real–only data by the packing function. The User Block data is assumed to be I and Q output pairs from an FPGA IP core.

The selected digital data can be written to the PACK FIFO at a programmed decimation rate, and may be packed or unpacked as set by the associated ADC Data Control Register, Section 6.4. The four packing formats (Real–only Packed, Real–only Unpacked, I/Q Packed, and I/Q Unpacked) are described in the following pages.

NOTE: Since all FIFO data transfers are 64–bits wide, the packing formats in the following subsections are illustrated in 64–bit format.

Writing to the PACK FIFO is controlled by the selected gate or by a Linked List of acquisition gates. See Section 3.2.2 for description of ADC Linked List operation.

ADS5485 data can be written to the FIFO at a programmed decimation rate N (where N is 1 to 65,536) set by the associated ADC Rate Divider Register, Section 6.5.

NOTE: When the Timestamp marker is enabled (from the ADC Data Control Register, Section 6.4), bit 0 of each sample is replaced with a timestamp marker.

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3.2 Analog to Digital Input (continued)

3.2.1 ADC Data Packing Formats (continued)

3.2.1.1 Real–only Packed

When PACK MODE is cleared to 00, data is packed with four consecutive real (I) data samples in each 64–bit FIFO word.

- The first sample, at time 't', is placed into bits 15 to 0.
- The next sample, at time 't+1', is placed into bits 31 to 16.
- The next sample, at time 't+2', is placed into bits 47 to 32.
- The next sample, at time 't+3', is placed into bits 63 to 48.

The ADC PACK FIFO data is packed in the following format:

Table 3–1: ADC PACK FIFO – Real–only Packed Format

Bit	63 – 48	47 – 32	31 – 16	15 – 0
Value	16–bit I sample[15:0] at time (t+3)	16–bit I sample[15:0] at time (t+2)	16–bit I sample[15:0] at time (t+1)	16–bit I sample[15:0] at time (t)

Note: When Timestamp marker is enabled, bit 0 of each sample is replaced with a timestamp marker. If you select the ADS5485 as data source the I data is the raw ADS5485 input.

3.2.1.2 Real–only Unpacked

When PACK MODE is set to 01, data is unpacked with two consecutive real (I) data samples stored in each 64–bit FIFO word.

- The first sample, at time 't', is placed into bits 31 to 16 and the ADC channel number is put into bits 7–4.
- The next sample, at time 't+1', is placed into bits 63 to 48 and the ADC channel number is put into bits 39–36.

The ADC PACK FIFO data is in the following format:

Table 3–2: ADC PACK FIFO – Real–only Unpacked Format

Bit	63 – 48	47 – 40	39–36	35–32	31 – 16	15 – 8	7–4	3–0
Value	16–bit I sample[15:0] at time (t+1)	00000000	ADC Chan	000T	16–bit I sample[15:0] at time (t)	00000000	ADC Chan	000T

Note: When Timestamp marker is enabled, bit T for each sample is replaced with a timestamp marker. If you select the ADS5485 as data source the I data is the raw ADS5485 input.

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3.2 Analog to Digital Input (continued)

3.2.1 ADC Data Packing Formats (continued)

3.2.1.3 I/Q Packed

When PACK MODE is set to 10, data is packed with two consec–utive I/Q data samples in each 64–bit FIFO word.

- The first sample Q value, at time 't', is placed into bits 15 to 0.
- The first sample I value, at time 't', is placed into bits 31 to 16.
- The next sample Q value, at time 't+1', is put into bits 47 to 32.
- The next sample I value, at time 't+1', is put into bits 63 to 48.

The ADC PACK FIFO data is packed in the following format:

Table 3–3: ADC PACK FIFO – I/Q Packed Data Format

Bit	63 – 48	47 – 32	31 – 16	15 – 0
Value	16–bit I sample[15:0] at time (t+1)	16–bit Q sample[15:0] at time (t+1)	16–bit I sample[15:0] at time (t)	16–bit Q sample[15:0] at time (t)

Note: When Timestamp marker is enabled, bit 0 of each sample is replaced with a timestamp marker. If you select the ADS5485 as data source the Q data is zero.

3.2.1.4 I/Q Unpacked

When PACK MODE is set to 11, data is unpacked with one I/Q data samples stored in each 64–bit FIFO word.

- The first sample Q value, at time 't', is placed into bits 31 to 0.
- The first sample I value, at time 't', is placed into bits 63 to 32.

The ADC PACK FIFO data is in the following format:

Table 3–4: ADC PACK FIFO – I/Q Unpacked Data Format

Bit	63 – 48	47 – 32	31 – 16	15 – 0
Value	32–bit I sample[31:0] at time (t)		32–bit Q sample[31:0] at time (t)	

Note: When Timestamp marker is enabled, bit 0 of each sample is replaced with a timestamp marker. If you select the ADS5485 as data source the Q data is zero.

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3.2 Analog to Digital Input (continued)

3.2.2 ADC Input Linked List Operation

Each ADC channel has a flexible ADC Trigger Controller Linked List Engine that is capable of generating complex gating to control acquisition of ADC data in response to input triggers. This is useful in applications like radar systems where it makes it possible to create complex chains of acquisition periods and delays in response to a single trigger, as well as allowing the ability to increment through different acquisition period lengths and delays at each trigger event. Numerous other possibilities exist. Each link definition defines the delay before acquisition begins, the length of acquisition, how many times to repeat it before going to the next link definition, as well as the ability to execute multiple link definitions from a single trigger event.

Note that this ADC Trigger Controller Linked List Engine functions only in trigger mode, not Gate mode. When Gate mode is selected, ADC data is written to the PACK FIFO while the selected gate is active and the Linked List Engine is not used.

Table 3–5: ADC Trigger Controller Linked List RAM

Address Offset *	Link Definition	Link Descriptor Register
+0x00000	Link Definition 0	DELAY[31:0]
+0x00004		LENGTH[31:0]
+0x00008		REPEAT[15:0]
+0x0000C		Bit 8 = CONTINUE NEXT_LINK_DEF[5:0]
+0x00010	Link Definition 1	DELAY[31:0]
+0x00014		LENGTH[31:0]
+0x00018		REPEAT[15:0]
+0x0001C		Bit 8 = CONTINUE NEXT_LINK_DEF[5:0]
	. . .	
+0x003E0	Link Definition 63	DELAY[31:0]
+0x003E4		LENGTH[31:0]
+0x003E8		REPEAT[15:0]
+0x003EC		Bit 8 = CONTINUE NEXT_LINK_DEF[5:0]

* Offset from applicable ADC channel Trigger Controller Linked List RAM address (see Table 4–2, Section 4.2)

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3.2 Analog to Digital Input (continued)

3.2.2 ADC Input Linked List Operation (continued)

DELAY[31:0] – This value sets the delay in number of ADC CLOCK cycles that the ADC Trigger Controller Linked List waits before opening the acquisition gate. The minimum valid setting for this register is **0x00000001**. A value of zero is not valid. The actual delay period is equal to the setting DELAY[31:0] +3. This implies that the delay may be any number of clock cycles between 5 and 4,294,967,298. The delay may not be less than 5 because the state machine needs a few clock cycles to set up for the settings in the link definition.

LENGTH[31:0] – This value sets the acquisition gate period in terms of the number of desired data samples. It is not in terms of ADC CLOCK rate, as the data rate may be at a sub−multiple of this. An output sample is defined as one 16−bit sample. The minimum valid setting for this register is **0x00000004**. A value of zero is not valid. The actual acquisition gate length is equal to the setting LENGTH[31:0] +1. This implies that it may be any number of output samples between 5 and 4,294,967,296.

REPEAT[15:0] – This value sets the number of times to repeat the delay and acquisition gate period. This may have a value of 0 to 65535. Once the number of repeats has executed, the Linked List moves on to the next link definition. A value of 1 will execute the delay and acquisition gate period once. A value of 0 will repeat forever until a TRIGGER CLEAR is issued or the linked list is reset.

CONTINUE (bit 8) – The continue bit controls whether, when the link definition has completed execution, the next link definition in the chain executes immediately, or whether it waits for the next trigger event to occur before executing.

- Clearing bit 8 to '0' causes the next link to wait for another trigger before executing.
- Setting bit 8 to '1' causes the next link to execute immediately without waiting for another trigger event.

This feature makes this output controller very flexible to create complex strings of delays and acquisition gate periods off of a single trigger event, or to step through a sequence different acquisition gate length on sequential trigger events.

NEXT_LINK_DEF[5:0] – This value specifies the next link definition in the chain. Valid values are 0 through 63.

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3.2 Analog to Digital Input (continued)

3.2.2 ADC Input Linked List Operation (continued)

The ADC Trigger Gen Linked List Start Pointer Register (Section 6.7) controls the pointer for which link definition to start at when the TRIG LINKED LIST RST bit (ADC Gate/Trigger Control Register, Section 6.6, bit 8) is toggled to a '1'. This resets the linked list and the next trigger event will execute the specified link definition. The linked list must be reset prior to operation or whenever it is desired to change to a new start address.

Note that using the ADC Linked List Start Pointer Register, several chains can be set up within the 64 link definitions, and different start addresses can be used to index to them.

Example #1:

Requirement:

1) The 71620 receives a trigger from an external source.

2) After the trigger, 71620 must acquire data for 23,000 samples then stop.

3) Repeat at each trigger event.

Solution: Set up the linked List RAM table as follows:

ADC1 Linked List Start Pointer Register (Section 6.7) = **0x00**

Table 3–6: ADC1 Trigger Controller Linked List RAM

BAR0+0x10800	Link Definition 0	DELAY[31:0] = **0x00000001** (minimum)
BAR0+0x10804		LENGTH[31:0] = **0x000059D7**
BAR0+0x10808		REPEAT[15:0] = **0x00000001**
BAR0+0x1080C		CONTINUE (8) + NEXT_LINK_DEF[5:0] = **0x00000000**

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3.2 Analog to Digital Input (continued)

3.2.2 ADC Input Linked List Operation (continued)

Example #2:

Requirement:

1) The 71620 receives a trigger from an external source.

2) After the trigger, 71620 acquires 2048 data samples.

3) Then after waiting 512 clocks of delay 71620 must acquire another 2048 data samples.

4) Waiting another 512 clocks of delay and acquire another 2048 data samples.

5) After a delay of 1011 clock cycles, 71620 must acquire 4000 more samples and then stop.

6) Repeat at each trigger event.

Solution: Set up the linked List RAM table as follows:

ADC1 Linked List Start Pointer Register (Section 6.7) = **0x00**

Table 3–7: ADC1 Trigger Controller Linked List RAM

BAR0+0x10800	Link Definition 0	DELAY[31:0] = **0x00000001** (minimum)
BAR0+0x10804		LENGTH[31:0] = **0x000007FF**
BAR0+0x10808		REPEAT[15:0]= **0x00000001**
BAR0+0x1080C		CONTINUE(8) + NEXT_LINK_DEF[5:0] = **0x00000101**
BAR0+0x10800	Link Definition 1	DELAY[31:0] = **0x000001FD**
BAR0+0x10814		LENGTH[31:0] = **0x000007FF**
BAR0+0x10818		REPEAT[15:0]= **0x00000002**
BAR0+0x1081C		CONTINUE(8) + NEXT_LINK_DEF[5:0] = **0x00000102**
BAR0+0x10800	Link Definition 2	DELAY[31:0] = **0x000003F0**
BAR0+0x10824		LENGTH[31:0] = **0x00000F9F**
BAR0+0x10828		REPEAT[15:0]= **0x00000001**
BAR0+0x1082C		CONTINUE(8) + NEXT_LINK_DEF[5:0] = **0x00000000**

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3.2 Analog to Digital Input (continued)

3.2.3 ADC DMA Operation

Each ADC channel has its own DMA engine that transfers ADC data packets directly to a PCIe memory address (i.e., XMC baseboard memory). Each ADC DMA engine has a linked list RAM capable of storing up to 512 link descriptors. See Section 3.2.4 for the format of this Linked List RAM. The DMA engine is capable of reading ADC data packets directly from the ADC PACK FIFO or RAM memory, and meta data from an internal FIFO.

The DMA engine has the ability to end a DMA early if an END OF GATE marker is reached. This is useful for radar applications where the actual gate length may vary. The DMA length can be set up to a maximum length and then configured to end and jump to the next link descriptor when the END OF GATE marker is reached.

Meta data can be generated at the execution of each link descriptor. Meta Data is transmitted in 32 bytes containing the following information (the following two pages provide definitions of each Meta Data field):

Table 3–8: ADC DMA Meta Data Format

Offset	31:28	27:24	23:20	19:17	16	15:12	11:8	7:5	4	3:0
+0x00000	Time Stamp Sample Clock Offset Count									
+0x00004	Time Stamp PPS Count									
+0x00008	Reserved					Gate Number				
+0x0000C	Reserved					Trigger Number				
+0x00010	Valid Sample Count									
+0x00014	Packet Count			000		Link Number		000	F/O	ADC Channel Number
+0x00018	Destination Address [31:0]									
+0x0001C	Destination Address [63:32]									

A link definition can be configured to transmit this meta data to any destination address. In this way the linked list may be set up to alternately send ADC data packets followed by meta data packets that describe the ADC data.

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3.2 Analog to Digital Input (continued)

3.2.3 ADC DMA Operation (continued)

The Meta Data includes the following data values:

Time Stamp Sample Clock Offset Count * – This is a 32–bit Time Stamp Sample Clock Offset Counter. This value increments every clock cycle and is reset at each PPS input event. It measures the number of clock cycles that have passed since the last PPS event. When no PPS input is used it is a free–running counter.

Time Stamp PPS Count * – This is a 32–bit Time Stamp PPS Counter value of the first sample of Gate. This value increments every PPS input. The value indicates the PPS timestamp counter value at the clock cycle of the first data sample of the DMA transfer if it also was the first sample of an active gate.

Gate Number * – This is a 16–bit counter of Gate periods. Since a trigger event can result in multiple gate periods, it is not necessarily the same number as the trigger number.

Trigger Number * – This is a 16–bit counter of Trigger events. When the first sample of the DMA transfer is also the first sample of a gate period, the number of the trigger that triggered the gate is supplied in the meta data.

Valid Sample Count – This is a 32–bit count of the number of valid 16–bit samples transmitted in the execution of the link descriptor.

Dummy words for non–multiple gate lengths are transmitted at the end of a packet payload but not counted in this meta data value. Only valid data samples are counted. Worst case is three dummy samples.

Packet Count – This is a 12–bit free–running count corresponding to the packet count of the first packet of the DMA transfer.

Link Number – This number corresponds to the Link Definition number (0 through 511) that was responsible for the first packet of the DMA transfer.

---

* Only if start of gate tag was found at beginning of this link descriptor execution, as would occur if it was the first data sample of a gate interval. Otherwise values are zeroed. Time Stamp values are not included in ADC data packet payloads, only meta data payloads.

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3.2 Analog to Digital Input (continued)

3.2.3 ADC DMA Operation (continued)

FIFO Overflow Flag (F/O) – When this bit is equal to '1' this indicates that a FIFO overflow has occurred in the data of this DMA transfer. This flags that data was lost and may not be contiguous samples.

ADC Channel Number – This is the ADC channel number (1, 2, or 3) of the samples in the current DMA transfer.

Destination Address – This is the start address (32–bit or 64–bit depending on PCIe addressing mode) that the data was written to.

A link definition can be configured to transmit this meta data to any destination address. In this way the linked list may be set up to alternately send ADC data packets followed by meta data packets that describe the ADC data.

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3.2 Analog to Digital Input (continued)

3.2.4 ADC DMA Linked Lists

ADC DMA Linked List RAM memory map:

Table 3–9: ADC DMA Linked List RAM

Address Offset *	Link Descriptor	Link Descriptor Register
+0x00000	Link Descriptor 0	Link Control Word
+0x00004		Length [31:0] (number of Bytes)
+0x00008		Destination Address [31:0]
+0x0000C		Destination Address [63:32]
+0x00010	Link Descriptor 1	Link Control Word
+0x00014		Length [31:0]
+0x00018		Destination Address [31:0]
+0x0001C		Destination Address [63:32]
	. . .	
+0x01FE0	Link Descriptor 510	Link Control Word
+0x01FE4		Length [31:0]
+0x01FE8		Destination Address [31:0]
+0x01FEC		Destination Address [63:32]
+0x01FF0	Link Descriptor 511	Link Control Word
+0x01FF4		Length [31:0]
+0x01FF8		Destination Address [31:0]
+0x01FFC		Destination Address [63:32]

* Offset from applicable ADC channel DMA Linked List RAM address (see Table 4–2, Section 4.2)

Link Control Word – See Table 3–10 on the next page.

Length– Number of Bytes, 8 to 4,294,967,288 (0 = 4,294,967,296) to be written. Length must be a multiple of 8 (Length[2:0] must be 000). Length and Payload Size (Link Control Word) have no effect on Meta Data size.

Destination Address – 64–bit PCIe start address that the data is to be written to. This must be a multiple of 8 (Address[2:0] must be 000).

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3.2 Analog to Digital Input (continued)

3.2.4 ADC DMA Linked Lists (continued)

The following table shows the format of the ADC DMA Link Control Word. The paragraphs following the table describe the bits in this word.

Table 3–10: ADC Link Control Word Format

Bit	31	30	29	28	27	26	25	24
Bit Name	End Chain	Reserved	End Chain Interrupt Enable	End Link Interrupt Enable	Reserved	Chain End Mode	Link End Mode	Reserved
Function	0 - Not end 1 - End	Write zero	0 - Disable 1 - Enable	0 - Disable 1 - Enable	Write zero	0 - Normal 1 - Gate	0 - Normal 1 - Gate	Write zero
Bit	**23**	**22**	**21**	**20 – 12**				**11 – 8**
Bit Name	Start Mode	Meta Data Link	Meta Data Mode	Next Link Address				Reserved
Function	0 - Manual 1 - Auto	0 - ADC Data 1 - Meta Data	0 - Don't store 1 - Store	Determines next link to execute when the present one is complete. Values from 0 to 511				Write zeros
Bit	**7 – 4**				**3**	**2**	**1 – 0**	
Bit Name	Reserved				Payload Size Mode	Reserved	PCIe Packet Manual Payload Size	
Function	Write zeros				0 - Auto 1 - Manual	Write zero	0 - 128 Bytes 1 - 256 Bytes 2 - 512 Bytes 3 - Reserved	

End Chain Bit 31

0 – This Link is not the end of the chain
1 – This Link is the end of the chain

End Chain Interrupt Enable Bit 29

0 – No interrupt is generated
1 – The completed execution of the chain generates an interrupt

End Link Interrupt Enable Bit 28

0 – No interrupt is generated
1 – The completed execution of this Link generates an interrupt

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3.2 Analog to Digital Input (continued)

3.2.4 ADC DMA Linked Lists (continued)

Chain End Mode Bit 26

0 – Normal – Chain ends at Link with END CHAIN bit (31) set
1 – Gate End – Chain ends when end of Gate is reached regard–less of whether this Link is the last in the chain

Link End Mode Bit 25

0 – Normal – Current DMA Link ends when specified Length is reached
1 – Gate End – Current DMA Link ends at the earlier of:
1) end of Gate is reached; or
2) specified Length is reached

Start Mode Bit 23

0 – Manual Start – Register Write starts execution
1 – Auto – Start execution immediately

NOTE: The first link in a chain requires a register write to start regardless of the setting of this bit.

Meta Data Link Bit 22

0 – Normal Data – Data source for this Link is the ADC data
1 – Meta Data – Data source for this Link is the Meta Data FIFO (Payload Size and Link Length have no effect on Meta Data size, Meta Data is always 32 Bytes)

Meta Data Mode Bit 21

0 – Don't store Meta Data for this Link
1 – Store Meta Data for this Link

Next Link Address Bits 20:12

Determines the next Link to execute when the present one is complete. Values from 0 to 511 (Link Descriptor number).

Payload Size Mode Bit 3

0 – Auto Mode – Payload Size = **Max_Payload_Size** from PCI Express Device Control Register, Offset **08h**
1 – Manual Mode – Payload Size is controlled by bits 1:0 below

PCIe Packet Manual Payload Size Bits 1:0

0 – Payload Size = 128 Bytes 1 – Payload Size = 256 Bytes
2 – Payload Size = 512 Bytes 3 – Reserved

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3.3 Digital To Analog Output

The Model 71620 is designed with a maximum output sample rate of 500 MHz in upconverter mode and 800 MSPS in D/A only mode. One Texas Instruments 16–bit DAC5688 is used to produce an analog output.

The DAC5688 is a dual–output 16–bit 800 MSPS digital–to–analog converter with dual CMOS digital data bus, integrated 2x–8x interpolation filters, a fine frequency mixer with 32–bit complex numerically controlled oscillator (NCO), on–board clock multiplier, IQ compensation, and internal voltage reference. Different modes of operation enable or bypass various signal processing blocks. The DAC5688 dual CMOS data bus provides 250 MSPS input data transfer per DAC output. Several input data options are available for the DAC5688: dual bus mode, interleaved (single) bus mode, and half rate bus mode. Refer to the Texas Instruments DAC5688 data sheet (see Section 1.13) for description of DAC operation.

The 71620 FPGA has a single DAC data acquisition module that accepts data from the PCIe interface, and routes the data, using a DMA linked list engine and DMA FIFO, to an output linked list engine and to the optional RAM memory. The PCIe interface data, or memory data, can be transferred, using the output linked list engine, through a DAC FIFO and unpacked to the DAC5688 A and B inputs. See Section 3.3.1 for description of the DAC DMA operation, Section 3.3.2 for description of the DAC Output Linked List operation, and Section 3.3.3 for description of the DAC routing and data formats.

The DAC5688 output A signal is sent to the front panel **OUT 1** connector and the DAC5688 output B signal is sent to the front panel **OUT 2** connector. The FPGA also loops the DAC5688 A and B signals back to the ADC input modules.

The following is a simplified block diagram of the digital to analog output data flow. Examples of D/A signal processing applications are provided in Appendix B.

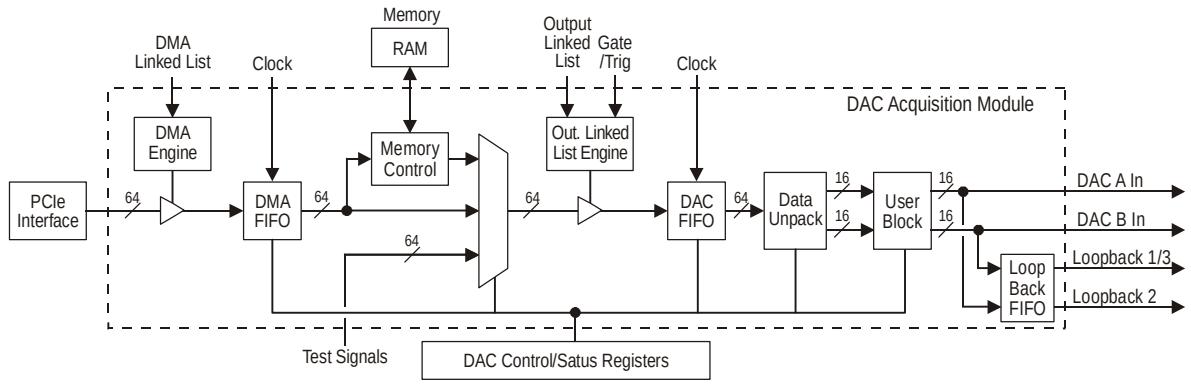


Figure 3–3: Digital to Analog Output Data Flow

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3.3 Digital To Analog Output (continued)

3.3.1 DAC DMA Linked Lists

The DAC DMA engine has a linked list RAM capable of storing up to 512 link descriptors. The DMA engine reads data from the PCIe interface and writes it directly to the DAC DMA FIFO, for transfer to the DAC output linked list engine (Section 3.3.2) and to the optional RAM memory.

Table 3–11: DAC DMA Linked List RAM

Address Offset *	Link Descriptor	Link Descriptor Register
+0x00000	Link Descriptor 0	Link Control Word
+0x00004		Length [31:0] (number of Bytes)
+0x00008		Source Address [31:0]
+0x0000C		Source Address [63:32]
+0x00010	Link Descriptor 1	Link Control Word
+0x00014		Length [31:0]
+0x00018		Source Address [31:0]
+0x0001C		Source Address [63:32]
	. . .	
+0x01FF0	Link Descriptor 511	Link Control Word
+0x01FF4		Length [31:0]
+0x01FF8		Source Address [31:0]
+0x01FFC		Source Address [63:32]

* Offset from DAC DMA Linked List RAM address (see Table 4–2, Section 4.2)

Link Control Word – See Table 3–12 on the next page.

Length– Number of Bytes, 4 to 4,294,967,292 (0 = 4,294,967,296) to be read. Length must be a multiple of 4 (Length[1:0] must be 00).

NOTE: If you start with a link that pre–fills the DAC DMA FIFO prior to starting the output transfer gate, the maximum pre–fill transfer size is 8192 bytes.

Source Address – 64–bit PCIe start address that the data is to be read from. This must be a multiple of 4 (Address[1:0] must be 00).

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3.3 Digital To Analog Output (continued)

3.3.1 DAC DMA Linked Lists (continued)

The following table shows the format of the DAC DMA Link Control Word. The paragraphs following the table describe the bits in this word.

Table 3–12: DAC Link Control Word Format

Bit	31	30	29	28	27 – 24		
Bit Name	End Chain	Reserved	End Chain Interrupt Enable	End Link Interrupt Enable	Reserved		
Function	0 - Not end 1 - End	Write zero	0 - Disable 1 - Enable	0 - Disable 1 - Enable	Write zero		
Bit	**23**	**22 – 21**		**20 – 12**			**11 – 8**
Bit Name	Start Mode	Reserved		Next Link Address			Reserved
Function	0 - Manual 1 - Auto	Write zeros		Determines next link to execute when the present one is complete. Values from 0 to 511			Write zeros
Bit	**7 – 4**			**3**	**2 – 0**		
Bit Name	Reserved			Read Request Size Mode	PCIe Packet Manual Read Request Size		
Function	Write zeros			0 - Auto 1 - Manual	0 - 128 Bytes 1 - 256 Bytes 2 - 512 Bytes 3 - 1024 Bytes	4 - 2048 Bytes 5 - 4096 Bytes 6 - Reserved 7 - Reserved	

End Chain Bit 31

0 – This Link is not the end of the chain
1 – This Link is the end of the chain

End Chain Interrupt Enable Bit 29

0 – No interrupt is generated
1 – The completed execution of the chain generates an interrupt

End Link Interrupt Enable Bit 28

0 – No interrupt is generated
1 – The completed execution of this Link generates an interrupt

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3.3 Digital To Analog Output (continued)

3.3.1 DAC DMA Linked Lists (continued)

Start Mode Bit 23

0 – Manual Start – Register Write starts execution
1 – Auto – Start execution immediately

NOTE: The first link in a chain requires a register write to start regardless of the setting of this bit.

Next Link Address Bits 20:12

Determines the next Link to execute when the present one is complete. Values from 0 to 511 (Link Descriptor number).

Read Request Size Mode Bit 3

0 – Auto Mode – Read Request Size = **Max_Read_Request_Size** from PCI Express Device Control Register, Offset **08h**
1 – Manual Mode – Payload Size is controlled by bits 2:0 below

PCIe Packet Manual Read Request Size Bits 2:0

Payload Size:
0 – 128 Bytes
1 – 256 Bytes
2 – 512 Bytes
3 – 1024 Bytes
4 – 2048 Bytes
5 – 4096 Bytes
6, 7 – Reserved

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3.3 Digital To Analog Output (continued)

3.3.2 DAC Output Linked List Operation

The 71620 DAC Output Controller Linked List Engine can generate complex output gates in response to input triggers as well as allowing for flexible access to multiple waveforms stored in its waveform storage RAM. This is useful in applications like radar systems where it makes it possible to output complex chains of waveforms and delays in response to a single trigger, as well as making it possible to increment through different waveforms at each trigger event. Each link definition defines the delay before waveform output, the length of the waveform output, how many times to repeat it before going to the next link definition, an address pointer for the RAM that indexes to the desired waveform, as well as the ability to execute multiple link definitions from a single trigger event.

Table 3–13: DAC Output Controller Linked List RAM

Address Offset *	Link Definition	Link Descriptor Register
+0x00000	Link Definition 0	DELAY[31:0] **
+0x00004		LENGTH[31:0] **
+0x00008		REPEAT[15:0] **
+0x0000C		RAM OFFSET[31:0]
+0x00010		RAM LENGTH[31:0]
+0x00014		Bit 0 = CONTINUE
+0x00018		NEXT_LINK_DEF[5:0]
+0x0001C		Reserved
+0x00020	Link Definition 1	DELAY[31:0]
+0x00024		LENGTH[31:0]
+0x00028		REPEAT[15:0]
+0x0002C		RAM OFFSET[31:0]
+0x00030		RAM LENGTH[31:0]
+0x00034		Bit 0 = CONTINUE
+0x00038		NEXT_LINK_DEF[5:0]
+0x0003C		Reserved
	. .	
+0x003E0	Link Definition 63	DELAY[31:0]
+0x003E4		LENGTH[31:0]
+0x003E8		REPEAT[15:0]
+0x003EC		RAM OFFSET[31:0]
+0x003F0		RAM LENGTH[31:0]
+0x003F4		Bit 0 = CONTINUE
+0x003F8		NEXT_LINK_DEF[5:0]
+0x003FC		Reserved

* Offset from DAC Output Controller Linked List RAM address (see Table 4–2, Section 4.2)
** DELAY, LENGTH, and REPEAT are not functional in Gate mode – See Note on next page

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3.3 Digital To Analog Output (continued)

3.3.2 DAC Output Linked List Operation (continued)

DELAY[31:0] – This value sets the delay in number of DAC CLOCK cycles that the DAC Output Controller Linked List waits before opening the output gate. The minimum valid setting for this register is **0x00000001**. A value of zero is not valid. The actual delay period is equal to the setting DELAY[31:0] +3. This implies that the delay may be any number of clock cycles between 4 and 4,294,967,298. The delay may not be less than 4 since the state machine needs a few clock cycles to set up for the settings in the link definition.

LENGTH[31:0] – This value sets the active gate period in terms of the number of desired output samples. It is not in terms of DAC CLOCK rate, as the output data rate may be at a sub−multiple of this. An output sample is defined as one 32−bit output. If the DAC5688 is set up for normal input format, this yields one sample for each DAC output, or one IQ pair. If the DAC5688 is set up for time packed (half data rate) format, it yields two output samples for DAC output A only, and the length must be calculated to take this into consideration. The minimum valid setting for this register is **0x00000001**. A value of zero is not valid. The actual OUTPUT GATE length is equal to the setting LENGTH[31:0] +1. This implies that the OUTPUT GATE may be any number of output samples between 2 and 4,294,967,296.

REPEAT[15:0] – This value sets the number of times to repeat the delay and active gate period. This may have a value of 0 to 65535. Once the number of repeats has executed, the Linked List moves on to the next link definition. A value of 1 will execute the delay and active gate period once. A value of 0 will repeat forever until a TRIGGER CLEAR is issued or the Linked list is reset.

RAM_OFFSET[31:0] – This value sets the start address in the waveform storage RAM to begin reading from for this output gate period. Note that this address is in terms of the address at the memory controller. For QDRII+ SRAM, the controller reads a burst of four 16−bit words per RAM address. For DDR3 SDRAM, the controller reads a burst of eight 32−bit words, one 32−bit word per RAM address – valid offset values must be multiples of eight minus one (7, 15, 23, etc.). See QDRII+ SRAM and DDR3 SDRAM illustrations on the next page for this Link Descriptor.

NOTE: The Output Controller Linked List Engine will also work in gate mode rather than trigger mode. When in gate mode however, the DELAY, LENGTH, and REPEAT parameters are not functional and the active gate output is equal to the input gate signal. The rest of the parameters are functional in gate mode.

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3.3 Digital To Analog Output (continued)

3.3.2 DAC Output Linked List Operation (continued)

RAM_OFFSET (continued)

For QDRII+ SRAM:

RAM_OFFSET	Data	RAM Address
0x0	Data1[15:0]	0
	Data2[15:0]	1
	Data3[15:0]	2
	Data4[15:0]	3
0x1	Data5[15:0]	4
	Data6[15:0]	5
	Data7[15:0]	6
	Data8[15:0]	7
0x2	Data9[15:0]	8
. . .	. . .	. . .

For DDR3 SDRAM:

RAM_OFFSET	Data	RAM Address
0x00	Data1[31:0]	0
0x01	Data2[31:0]	1
0x02	Data3[31:0]	2
0x03	Data4[31:0]	3
0x04	Data5[31:0]	4
0x05	Data6[31:0]	5
0x06	Data7[31:0]	6
0x07	Data8[31:0]	7
0x08	Data9[31:0]	8
0x09	Data10[31:0]	9
0x0A	Data11[31:0]	10
0x0B	Data12[31:0]	11
0x0C	Data13[31:0]	12
0x0D	Data14[31:0]	13
0x0E	Data15[31:0]	14
0x0F	Data16[31:0]	15
0x10	Data17[31:0]	16
. . .	. . .	. . .

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3.3 Digital To Analog Output (continued)

3.3.2 DAC Output Linked List Operation (continued)

RAM_LENGTH[31:0] – This value sets the span of RAM addresses that are read from the RAM_OFFSET start address before starting over again at the RAM_OFFSET start address again. This allows looping in the memory until the active gate period is done. This is useful if a repetitive waveform is required. Only one cycle of the waveform would be needed to be store in the RAM. The actual repeat span is equal to RAM_LENGTH + 1. Therefore, a value of 0 will repeat a read of the start address over and over. A value of 255 would read from RAM_OFFSET to RAM offset + 255 and then repeat. This value does not have to be a sub−multiple of the active gate period created by LENGTH[31:0].

For QDRII+ SRAM, RAM_LENGTH is in terms of RAM controller addressing – for every four 16−bit samples there is one RAM controller address. For DDR3 SDRAM, RAM_LENGTH is in terms of number of 32−bit words – valid values must be multiples of eight minus one (7, 15, 23, etc.).

CONTINUE – The continue bit controls whether, when the link definition has completed execution, the next link definition in the chain executes immediately, or whether it waits for the next trigger event to occur before executing.

- Clearing this bit to '0' causes the next link to wait for another trigger before executing.
- Setting this bit to '1' causes the next link to execute immediately without waiting for another trigger event.

This feature makes this output controller very flexible to create complex strings of delays and active DAC output off of a single trigger event, or to step through a sequence of different DAC waveforms on sequential trigger events.

NEXT_LINK_DEF[5:0] – This value specifies the next link definition in the chain. Valid values are 0 through 63.

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3.3 Digital To Analog Output (continued)

3.3.2 DAC Output Linked List Operation (continued)

The DAC Linked List Start Pointer Register (Section 7.7) controls the pointer for which link definition to start at when the OUT CNTRL LINKED LIST RST bit (DAC Gate/Trigger Control Register, Section 7.6, bit 8) is toggled to a '1'. This resets the linked list and the next trigger event will execute the specified link definition. The linked list must be reset prior to operation or whenever it is desired to change to a new start address.

Note that using DAC Linked List Start Pointer Register, several chains can be set up within the 64 link definitions, and different start addresses can be used to index to them.

Example #1:

Requirement:

1) The 71620 receives a trigger from an external source.

2) The 71620 has QDRII+ waveform storage RAM installed.

3) After the trigger, 71620 outputs waveform #1.
Waveform #1 is 135000 I/Q samples long.

4) Waveform #1 is at RAM offset **0x40000**.

5) Repeat at each trigger event.

Solution: Set up the linked List RAM table as follows:

DAC Linked List Start Pointer Register (Section 7.7) = **0x00**

Table 3–14: DAC Output Controller Linked List RAM

BAR0+0x30800	Link Definition 0 Waveform #1	DELAY[31:0] = **0x00000001** (minimum)
BAR0+0x30804		LENGTH[31:0] = **0x00020F57**
BAR0+0x30808		REPEAT[15:0]= **0x00000001**
BAR0+0x3080C		RAM OFFSET[31:0] = **0x00040000**
BAR0+0x30810		RAM LENGTH[31:0] =**0x000107AB**
BAR0+0x30814		CONTINUE = **0x00000000**
BAR0+0x30818		NEXT_LINK_DEF[5:0] = **0x00000000**
BAR0+0x3081C		Reserved

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3.3 Digital To Analog Output (continued)

3.3.2 DAC Output Linked List Operation (continued)

Example #2:

Requirement:

1) The 71620 receives a trigger from an external source.

2) The 71620 has QDRII+ waveform storage RAM installed.

3) After the trigger, 71620 outputs waveform #1.
Waveform #1 is 2048 I/Q samples long.

4) 71620 must output waveform #1 for a total three times with a delay of 512 clocks in between each waveform.

5) After a delay of 1011 clock cycles, 71620 must output waveform #2 and wait for the next trigger event. Waveform # 2 is 4000 I/Q samples long.

6) Repeat at each trigger event.

Solution: Set up the linked List RAM table as follows:

DAC Linked List Start Pointer Register (Section 7.7) = **0x00**

Table 3–15: DAC Output Controller Linked List RAM

BAR0+0x30800	Link Definition 0 First Waveform #1	DELAY[31:0] = **0x00000001** (minimum)
BAR0+0x30804		LENGTH[31:0] = **0x000007FF**
BAR0+0x30808		REPEAT[15:0]= **0x00000001**
BAR0+0x3080C		RAM OFFSET[31:0] = **0x00000000**
BAR0+0x30810		RAM LENGTH[31:0] =**0x000003FF**
BAR0+0x30814		CONTINUE = **0x00000001**
BAR0+0x30818		NEXT_LINK_DEF[5:0] = **0x00000001**
BAR0+0x3081C		Reserved
BAR0+0x30820	Link Definition 1 Two Additional Waveform #1	DELAY[31:0] = **0x000001FD** (minimum)
BAR0+0x30824		LENGTH[31:0] = **0x000007FF**
BAR0+0x30828		REPEAT[15:0]= **0x00000002**
BAR0+0x3082C		RAM OFFSET[31:0] = **0x00000000**
BAR0+0x30830		RAM LENGTH[31:0] =**0x000003FF**
BAR0+0x30834		CONTINUE = **0x00000001**
BAR0+0x30838		NEXT_LINK_DEF[5:0] = **0x00000002**
BAR0+0x3083C		Reserved

(continued on next page)

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3.3 Digital To Analog Output (continued)

3.3.2 DAC Output Linked List Operation (continued)

Example #2 (continued):

Table 3–15: DAC Output Controller Linked List RAM (continued)		
BAR0+0x30840	Link Definition 2 Waveform #2	DELAY[31:0] = **0x000003F0**
BAR0+0x30844		LENGTH[31:0] = **0x00000F9F**
BAR0+0x30848		REPEAT[15:0]= **0x00000001**
BAR0+0x3084C		RAM OFFSET[31:0] = **0x00000400**
BAR0+0x30850		RAM LENGTH[31:0] =**0x000007CF**
BAR0+0x30854		CONTINUE = **0x00000000**
BAR0+0x30858		NEXT_LINK_DEF[5:0] = **0x00000000**
BAR0+0x3085C		Reserved

The waveforms are stored in QDRII+ SRAM as illustrated below.

Table 3–16: QDRII+ Waveform Storage RAM	
. . . . . **0x000BD0**	
0x000BCF **0x000400**	WAVEFORM #2
0x0003FF **0x000000**	WAVEFORM #1

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3.3 Digital To Analog Output (continued)

3.3.3 DAC Data Routing and Formats

The FPGA routes digital data from the DAC FIFO to the DAC5688's dual 16–bit interfaces (DAC inputs A and B). The DAC5688 can be set up for Dual Bus, Interleaved Bus, or Half Rate Bus mode for these inputs using the DAC Serial Registers, Sections 7.19 and 7.20. Refer to the Texas Instruments DAC5688 data sheet (see Section 1.13) for description of these input bus modes. The following subsections describe the DAC FIFO data formats used for the Dual Bus and Half Rate Bus modes (Interleaved Bus mode is not recommended on the 71620).

3.3.3.1 Dual Bus Mode – Channel–Packed FIFO

When the DAC5688 is set up for Dual Bus mode, each 32–bit FIFO data word contains a single 16–bit data sample for each DAC5688 channel, with data for DAC channel B in the upper 16 bits, and data for DAC channel A in the lower 16 bits of each 32–bit word. The DAC FIFO data is in the following format:

Table 3–17: DAC FIFO, Channel–Packed Data Format

Bit	31 – 16	15 – 0
Value	data[15:0] for DAC channel B	data[15:0] for DAC channel A

The DAC FIFO routing is illustrated below.

	DAC FIFO	
Bit	31:16	15:0
Word 1	$d[15:0]B_{(t)}$	$d[15:0]A_{(t)}$
Word 2	$d[15:0]B_{(t+1)}$	$d[15:0]A_{(t+1)}$
Word 3	$d[15:0]B_{(t+2)}$	$d[15:0]A_{(t+2)}$
Word n	...	...

DAC5688 Inputs		
input	DB[15:0]	DA[15 :0]
Word 1	$d[15:0]B_{(t)}$	$d[15:0]A_{(t)}$
Word 2	$d[15:0]B_{(t+1)}$	$d[15:0]A_{(t+1)}$
Word 3	$d[15:0]B_{(t+2)}$	$d[15:0]A_{(t+2)}$
Word n	...	...

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3.3 Digital To Analog Output (continued)

3.3.3 DAC Data Routing and Formats (continued)

3.3.3.2 Half Rate Bus Mode – Time–Packed FIFO

When the DAC5688 is set up for Half Rate Bus mode, each 32–bit FIFO data word contains two consecutive 16–bit samples for DAC5688 channel A. The first sample, for time 't', is placed into bits 15 to 0, and next sample, for time 't+1', is placed into bits 31 to 16. The DAC FIFO data is in the following format:

Table 3–18: DAC FIFO, Time Packed Data Format

Bit	31 – 16	15 – 0
Value	data[15:0] for DAC channel A, time (t+1)	data[15:0] for DAC channel A, time (t)

The DAC FIFO routing is illustrated below.

	DAC FIFO	
Bit	31:16	15:0
Word 1	$d[15:0]A_{(t+1)}$	$d[15:0A_{(t)}$
Word 2	$d[15:0]A_{(t+3)}$	$d[15:0]A_{(t+2)}$
Word 3	$d[15:0]A_{(t+5)}$	$d[15:0A_{(t+4)}$
Word n	...	...

DAC5688 Inputs		
Input	DB[15:0]	DA[15 :0]
Word 1	$d[15:0]A_{(t+1)}$	$d[15:0]A_{(t)}$
Word 2	$d[15:0]A_{(t+3)}$	$d[15:0]A_{(t+2)}$
Word 3	$d[15:0]A_{(t+5)}$	$d[15:0A_{(t+4)}$
Word n	...	...

Both DA and DB inputs are merged into a single data stream for channel A within the DAC5688 device.

Note that there is no signal output from DAC5688 channel B in this mode (front panel **OUT 2** connector).

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3.4 RAM Memory Operation

Two or four independent banks of QDRII+ (Quad Data Rate II+) SRAM or DDR3 (Dou–ble Data Rate 3) SDRAM are available to the Model 71620 FPGA, depending on the Memory Option ordered. The following memory options are available:

Memory Module 1 – Banks A and B
Option 150: 16 MB QDRII+ SRAM, 2 banks of 4M x 16
Option 155: 1 GB DDR3 SDRAM, 2 banks of 128M x 32
Memory Module 2 – Banks C and D
Option 160: 16 MB QDRII+ SRAM, 2 banks of 4M x 16
Option 165: 1 GB DDR3 SDRAM, 2 banks of 128M x 32

Each Memory Module includes two separate banks of memory. The default FPGA fac–tory code uses the memory as FIFO buffers for the three ADC channels and waveform storage for the DAC channel. In the default FPGA code, each of these four channels has one bank of memory assigned for these purposes, as illustrated in Figure 3–4 below. These memory functions are controlled through the default set of FPGA registers. Refer to Chapter 4 for the memory map of these FPGA registers.

Custom user–installed functions within the FPGA can take advantage of the memory for many other purposes.

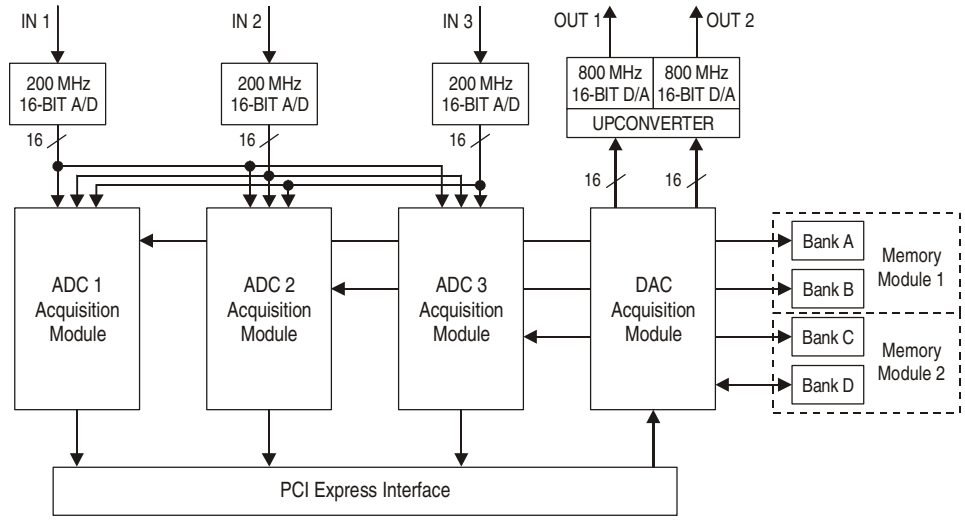


Figure 3–4: RAM Memory Module Interfaces

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3.5 Timing and Synchronization

The Model 71620 front panel LVPECL Sync Bus connector (Section 2.7.4) provides clock, sync, PPS, and gate input/output signals. This connector also provides two TTL Gate/Sync inputs. The front panel has a coaxial SSMC receptacle for input of an external sample clock signal.

The front panel interface allows one Model 71620 to act as a Master, driving the clock, sync, and/or gate signals to the Sync Bus using LVPECL (Low−Voltage Positive Emitter−Coupled Logic). Up to three Slave 7162x's can be driven by the LVPECL Sync Bus, supporting synchronous sampling and sync functions across all connected boards. If more than four boards need to be synchronized, Pentek's Model 7893 Synchronizer allows synchronization of up eight boards. Note that the 7893 is a PCIe board.

3.5.1 Gates

The Model 71620 provides two gate signals, GATE A and GATE B, which are used to enable writes to the ADC and DAC FIFOs, respectively. The Sync Bus Control Registers 1 and 2, Sections 5.17 and 5.18, and the ADC and DAC Gate/Trigger Control Registers, Sections 6.6 and 7.6, control gate source selection and characteristics. Gates may be individually disabled, in which case FIFO writes are always enabled.

Each gate can be driven directly from the associated front panel Sync Bus LVPECL GATE A or B input (Section 2.7.4), from a Gate Generate Register write (Section 5.23 or 5.24), or from the front panel Sync Bus TTL GATE/TRIG input (Section 2.7.4). The polarity of each TTL GATE/TRIG signal is programmable.

In addition, each ADC channel has a local gate, generated by a Local Gate Generate Register (Section 6.8), that can be used for the ADC PACK FIFO.

When the Model 71620 is a Sync/Gate Master, the applicable Gate Generate Register write or the Sync Bus TTL GATE/TRIG input signal is output to the GATE pins of the Sync Bus.

Each FIFO gate may be programmed as a trigger (Trigger mode) using the ADC or DAC Gate/Trigger Control Registers, Section 6.6 or 7.6. In Trigger mode, the gate is generated after a desired polarity logic transition on the gate source, and the resulting gate continues either indefinitely (Hold mode) or for a programmed number of ADC samples (Linked List). At any time the triggered gate may be asynchronously disabled by a control register write.

When Trigger mode is selected for an ADC or DAC Gate signal, a linked list of delays is defined, as described in Section 3.2.2 or 3.3.2. Each link definition defines the delay before acquisition begins, the length of acquisition, how many times to repeat it before going to the next link definition, as well as the ability to execute multiple link definitions from a single trigger event.

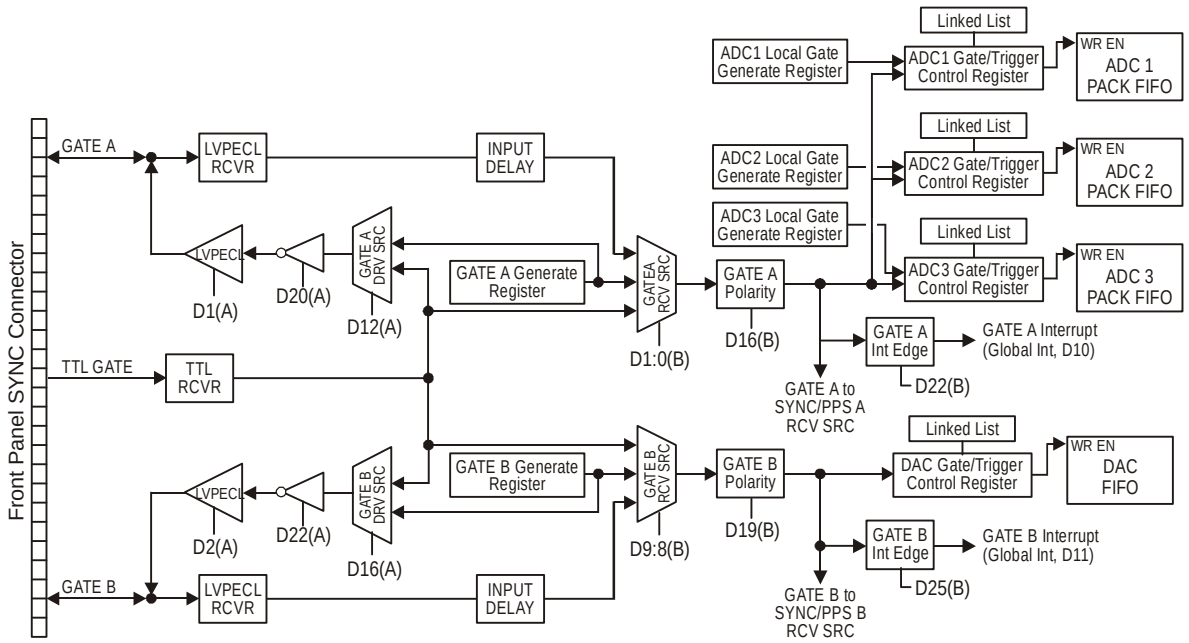
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3.5 Timing and Synchronization (continued)

3.5.1 Gates (continued)

The following diagram illustrates the gate/trigger logic and the controlling FPGA registers. Refer to the following sections for descriptions of the registers and linked lists identified in this diagram.

- Sections 5.17 and 5.18 – Sync Bus Control Registers 1 and 2
- Sections 5.23 and 5.24 – Gate A and B Generate Registers
- Sections 6.6 and 7.6 – ADC and DAC Gate/Trigger Control Registers
- Section 6.8 – ADC Local Gate Generate Registers
- Sections 3.2.2 and 3.3.2 – ADC and DAC FIFO Linked List operation



(A) SYNC BUS Control Register 1 - BAR0+0x0402C

Bit:	D16 GATE B DRV SRC	D12 GATE A DRV SRC	D2 GATE/SYNC B MASTER	D1 GATE/SYNC A MASTER
Values:	0 = Register 1 = TTL GATE	0 = Register 1 = TTL GATE	0 = Slave 1 = Master	0 = Slave 1 = Master

	D22 GATE B DRV INV	D20 GATE A DRV INV
	0 = Normal 1 = Invert	0 = Normal 1 = Invert

(B) SYNC BUS Control Register 2 - BAR2+0x04030

Bit:	D25 GATE B INT EDGE	D22 GATE A INT EDGE	D19 GATE B POL	D16 GATE A POL	D9:8 GATE B RCV SRC	D1:0 GATE A RCV SRC
Values:	0 = Start 1 = End	0 = Start 1 = End	0 = High 1 = Low	0 = High 1 = Low	00 = None 01 = Register 10 = TTL GATE 11 = GATE B	00 = None 01 = Register 10 = TTL GATE 11 = GATE A

Figure 3–5: Gate Logic Diagram

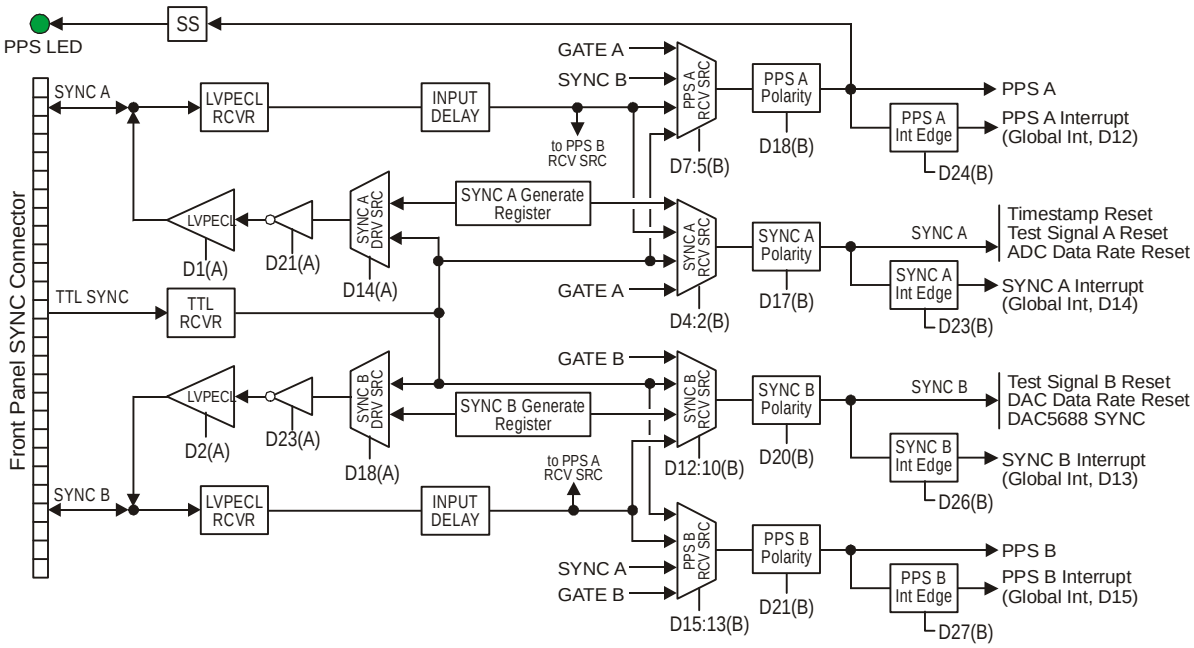
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3.5 Timing and Synchronization (continued)

3.5.2 Syncs

The 71620 provides SYNC A, SYNC B, PPS A, and PPS B signals for ADC (Sync A), DAC (Sync B), and user applications. These signals can be driven from the front panel Sync Bus LVPECL SYNC input (Section 2.7.4), a Sync Generate Register write (Section 5.25 or 5.26), the front panel Sync Bus TTL SYNC input (Section 2.7.4), or a GATE signal (Section 3.5.1). When the Model 71620 is a Sync/Gate Master, the applicable register write or the input Sync Bus TTL SYNC signal is output to the Sync Bus SYNC pins.

The following diagram illustrates the sync logic and the Sync Bus Control Registers that control this logic. Refer to Section 5.17, 5.18, 5.25, and 5.26 for description of the registers referenced in this diagram.



(A) SYNC BUS Control Register 1 - BAR0+0x0402C				
Bit:	D23 SYNC B DRV INV	D21 SYNC A DRV INV	D18 SYNC B DRV SRC	D14 SYNC A DRV SRC
Values:	0 = Normal 1 = Invert	0 = Normal 1 = Invert	0 = Register 1 = TTL SYNC	0 = Register 1 = TTL SYNC
	D2 GATE/SYNC B MASTER	D1 GATE/SYNC A MASTER		
	0 = Slave 1 = Master	0 = Slave 1 = Master		

(B) SYNC BUS Control Register 2 - BAR2+0x04030							
D27 PPS B INT EDGE	D26 SYNC B INT EDGE	D24 PPS A INT EDGE	D23 SYNC A INT EDGE	D21 PPS B POL	D20 SYNC B POL	D18 PPS A POL	D17 SYNC A POL
0 = Start 1 = End	0 = Start 1 = End	0 = Start 1 = End	0 = Start 1 = End	0 = High 1 = Low	0 = High 1 = Low	0 = High 1 = Low	0 = High 1 = Low
D15:13 PPS B RCV SRC		D12:10 SYNC B RCV SRC		D7:5 PPS A RCV SRC		D4:2 SYNC A RCV SRC	
000 = None 001 = TTL SYNC 010 = SYNC B 011 = SYNC A 100 = GATE B Rise		000 = None 001 = Register 010 = TTL SYNC 011 = SYNC B 100 = GATE B Rise 101 = GATE B Fall		000 = None 001 = TTL SYNC 010 = SYNC A 011 = SYNC B 100 = GATE A Rise		000 = None 001 = Register 010 = TTL SYNC 011 = SYNC A 100 = GATE A Rise 101 = GATE A Fall	

Figure 3–6: Sync Logic Diagram

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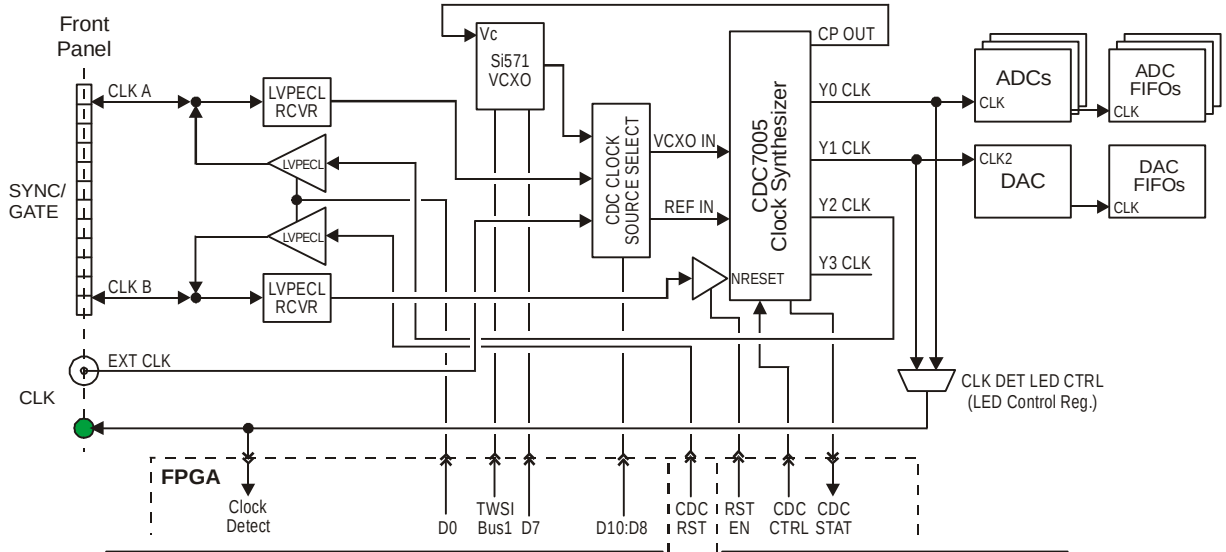
3.5 Timing and Synchronization (continued)

3.5.3 Clocks

71620 clocks can be selected from the front panel Sync Bus LVPECL CLK A input (Section 2.7.4), the front panel CLK input (Section 2.7.1), or the onboard Si571 VCXO. The selected clock source is input to a CDC7005 Clock Synthesizer that generates four output clocks, each independently programmable as sub−multiples of the input frequency using divisors of 1, 2, 4, 8, or 16. CDC7005 clock Y0 provides ADC timing, and clock Y1 pro−vides DAC timing. When the Model 71620 is a Clock Master, CDC7005 clock Y2 is output to the CLK A pins of the LVPECL Sync Bus, and CDC RST from the User LED Register is output to the Sync Bus CLK B pins. CLK B is used for CDC7005 reset.

CAUTION: Take care that the ADC clock never exceeds the ADS5485 rated clock speed.

The following diagram illustrates the clock logic and the Control Registers that control this logic. Refer to Sections 5.17, 5.14, 5.15, and 5.21 for descrip−tion of the registers referenced in this diagram.



Sync Bus Control Register 1 - BAR0+0x0402C

Bit:	D10:D8 CDC CLK SEL			D7 VCXO DIS	D0 CLK MASTER
Values:		VCXO IN	REF IN	0 = Enable 1 = Disable	0 = Slave 1 = Master
	000	VCXO	EXT CLK		
	001	VCXO	LVPECL CLK A		
	010	VCXO	none		
	011	VCXO	none		
	100	EXT CLK	EXT CLK		
	101	LVPECL CLK A	LVPECL CLK A		

CDC7005 Control Registers

CDC Control/Status - BAR0+0x04020
CDC Data - BAR0+0x04024

User LED Register - BAR0+0x0403C

Figure 3–7: Clock Logic Diagram

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3.6 Interrupt Operation

The 71620 XMC module can generate INTA interrupts in legacy mode or MSI interrupts. Refer to the Operating Manual supplied with your XMC baseboard for description of the board's interrupt response operation.

The following figure illustrates the interrupt signal routing on the Model 71620.

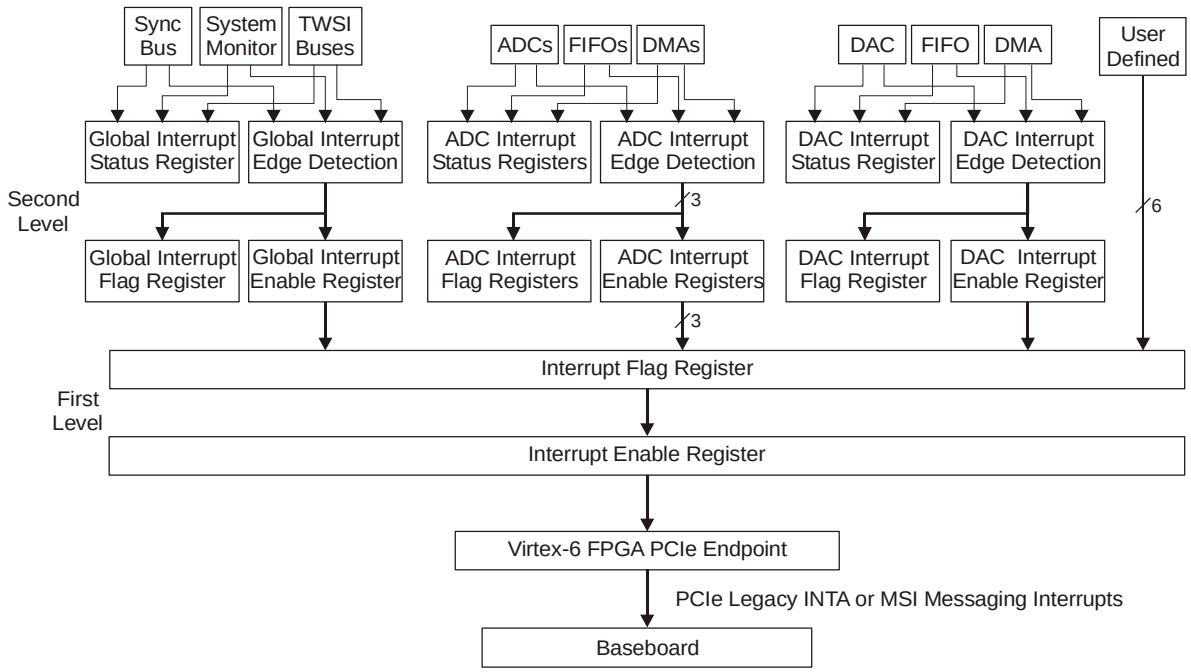


Figure 3–8: Interrupt Signal Logic Diagram

Interrupt events are edge–detected and latched in second–level interrupt flag registers. In addition, the interrupt sources are also routed to dynamic interrupt status registers. The interrupt edges from various sources can be individually enabled by interrupt enable registers and then OR'ed per system module to form sources to the first–level interrupt flag register where the event is latched. Enable bits in the first–level interrupt enable register can individually enable each module's flag, which are then OR'ed together for a single level interrupt input to the PCIe interface.

Clearing an interrupt in the first–level interrupt flag register will turn off the interrupt. The sources are still latched in the second–level flag register but a new interrupt will not be asserted even if the source is still present until the second–level flag is cleared and the logic subsequently detects a new edge.

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3.6 Interrupt Operation (continued)

3.6.1 PCIe Interrupts

The Interrupt Flag and Enable Registers (Sections 5.3 and 5.4) contain interrupt bits for the board. These Interrupts include the following:

- GLBL – This interrupt is associated with an interrupt from the Global Interrupt Enable Register, Section 3.6.2. Use the Global Interrupt Status or Flag Register to determine the source of the interrupt.
- ADC ACQ Module 1, ADC ACQ Module 2, ADC ACQ Module 3 – Each of these interrupts is associated with an interrupt from one of the ADC Interrupt Registers, Section 3.6.3. Use the applicable ADC Interrupt Status or Flag Register to determine the source of the interrupt.
- DAC ACQ Module 1 – This interrupt is associated with an interrupt from the DAC Interrupt Registers, Section 3.6.4. Use the applicable DAC Interrupt Status or Flag Register to determine the source of the interrupt.
- USER 1 to 6 – There are six user–defined interrupts that can be programmed for custom FPGA core applications.

In response to any of these interrupt signals, the Interrupt Enable Register, Section 5.4, can be enabled to pass an interrupt to the FPGA PCIe core. The PCIe core is capable of generating a legacy INTA interrupt or MSI interrupts.

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3.6 Interrupt Operation (continued)

3.6.2 Global Interrupts

The set of Global Interrupt Registers (Sections 5.35 to 5.37) contain interrupt status, flag, and enable bits for the FIFO Flags and the System Interrupt conditions. The Global Interrupts include the following:

- TWSI Port 2, TWSI Port 1 – Each of these interrupts is associated with an interrupt from TWSI Port 2 or Port 1. Use the associated TWSI Port Data Register, Sections 5.34 or 5.32, to determine the source of this interrupt.
- PPS B, PPS A – Each of these interrupts is associated with Sync Bus PPS B or PPS A interrupt. Use the Sync Bus Control Register 2, Section 5.18, to specify the signal edge that triggers this interrupt.
- SYNC B, SYNC A – Each of these interrupts is associated with a Sync Bus SYNC B or SYNC A interrupt. Use the Sync Bus Control Register 2, Section 5.18, to specify the signal edge that triggers this interrupt.
- GATE B, GATE A – Each of these interrupts is associated with a Sync Bus GATE B or GATE A interrupt. Use the Sync Bus Control Register 2, Section 5.18, to specify the signal edge that triggers this interrupt.
- BRD TMP – This interrupt is associated with a temperature limit interrupt from the LM83 sensors. Use the TWSI Port 1 Data Register, Section 5.32, to determine the sensor causing the interrupt.
- SYS MON ALM2, SYS MON ALM1, SYS MON ALM0, SYS MON OT – Each of these interrupts is associated with a System Monitor interrupt from the FPGA sensors. Use the memory–mapped System Monitor registers, Section 3.7.1, to determine the sensor causing the interrupt.
- CLK A NOT LOCKED, CLK B NOT LOCKED – Each of these interrupts is associated with a PLL not locked interrupt from one of the Sync Bus Clocks.
- CLK A STOPPED, CLK B STOPPED – Each of these interrupts is associated with a Clock stopped interrupt from one of the Sync Bus Clocks.
- CDC NOT LOCKED – This interrupt is associated with a PLL not locked interrupt from the CDC7005.

In response to these interrupt signals, the Global Interrupt Enable Register, Section 5.35, can be enabled to assert an interrupt to the Interrupt Flag Register, Section 3.6.1.

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3.6 Interrupt Operation (continued)

3.6.3 ADC Interrupts

The ADC Interrupt Registers (Sections 6.13 to 6.15) contain interrupt status and control bits for each ADC data acquisition module. The ADC Interrupts include the following for each ADC channel:

- ADC OVLD – This interrupt signals an ADS5485 overload detected.
- ADC CLK NOT LOCK – This interrupt signals a clock PLL not locked condition.
- ADC CLK NOT DET – This interrupt signals a clock not detected.
- TRIG CMPLT – This interrupt signals a trigger complete, which occurs at the end of the active linked list gates/trigger occurrences.
- GATE START, GATE END – Each of these interrupts signals the start or end, respectively, of a programmed Gate period.
- LINK END, CHAIN END – Each of these interrupts signals the end of a link or end of the full chain of links, respectively, of a DMA transfer linked list.
- XXXX FIFO EMP, XXXX FIFO FULL – Each of these interrupts signals a FIFO Empty or Full condition, respectively, from the respective FIFO:
    - ADC PACK FIFO
    - DMA IN FIFO
    - RAM FIFO
    - TRIG NUM FIFO
    - TIMESTAMP FIFO
- MEM MMCM NOT LOCK – This interrupt signals a memory MMCM clock PLL not locked condition.
- MEM CLK IN STOPPED – This interrupt signals a memory clock stopped condition.
- BAD TRIGGER – This interrupt signals a trigger occurrence before the end of the active linked list gates/triggers.

In response to these interrupt signals, the ADC Interrupt Enable Register, Section 6.13, can be enabled to assert an interrupt to the Interrupt Flag Reg–ister, Section 3.6.1.

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3.6 Interrupt Operation (continued)

3.6.4 DAC Interrupts

The DAC Interrupt Registers (Sections 7.12 to 7.14) contain interrupt status and control bits for the DAC data processing modules. The DAC Interrupts include the following for the DAC channel:

- DAC NOT LOCK – This interrupt signals a DAC5688 PLL not locked condition.
- DAC CLK NOT LOCK – This interrupt signals a clock PLL not locked condition.
- DAC CLK NOT DET – This interrupt signals a clock not detected.
- TRIG CMPLT – This interrupt signals a trigger complete, which occurs at the end of the active linked list gates/trigger occurrences.
- GATE START, GATE END – Each of these interrupts signals the start or end, respectively, of a programmed Gate period.
- LINK END, CHAIN END – Each of these signals the end of a link or end of the full chain of links, respectively, of a DMA transfer linked list.
- DAC FIFO EMP, DAC FIFO FULL – Each of these interrupts signals a FIFO Empty or Full condition, respectively, from the DAC output FIFO:
- MEM MMCM NOT LOCK – This interrupt signals a memory MMCM clock PLL not locked condition.
- MEM CLK STOPPED – This interrupt signals a memory clock stopped condition.
- BAD TRIGGER – This interrupt signals a trigger occurrence before the end of the active linked list gates/triggers.
- REAL TIME LOST – This interrupt signals that the DAC output FIFO went empty (ran out of data).
- POISONED TLP – This interrupt signals that the PCI Express receiver has received a poisoned Transaction Layer Protocol error.
- ALL DATA RCVD – This interrupt signals that all requested DAC DMA data has been received.

In response to these interrupt signals, the DAC Interrupt Enable Registers, Section 7.12, can be enabled to assert an interrupt to the Interrupt Flag Reg–ister, Sections 3.6.1.

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3.7 FPGA Resources Operation

The following subsections describe the operation of several functional components of the Virtex–6 FPGA, including the System Monitor and the I^2C bus controller.

3.7.1 FPGA System Monitor

The Virtex–6 FPGA System Monitor measures several board power supplies and FPGA on–chip voltages and temperatures. The following lists the parameters measured by the System Monitor measurement ports.

Table 3–19: System Monitor Measurement Ports

Port	Parameter Measured	Alarm Out
Internal Temperature	FPGA on–chip temperature	**ALM0, OT**
Internal V_{CCINT}	FPGA on–chip voltage, 1.0 V	**ALM1**
Internal V_{CCAUX}	FPGA on–chip voltage, 2.5 V	**ALM2**
V_{AUX9}	Primary XMC 5V or 12V supply	–
V_{AUX10}	3.3 V supply	–
V_{AUX11}	1.8V supply	–
V_{AUX12}	1.5V supply	–

On–board registers provide access to the measured data and the System Monitor control registers. All registers are mapped to 71620 memory space starting at PCI Base Address Register BAR0 +**0x08000** to BAR0 +**0x0815C**. See Table 3–20 and Table 3–21 on the following pages for memory maps of these registers. Refer to the Xilinx Virtex–6 FPGA System Monitor Users Guide provided with the 71620 supporting documentation (see Section 1.13) for further description and use of these registers.

The System Monitor provides several alarm outputs (identified Table 3–19 above) that are routed to the Global Interrupt Status Register, Section 5.36, and can illuminate front panel LEDs, Section 5.22. System Monitor also provides user–programmable alarm thresholds for the associated on–chip sensors. If an on–chip monitored parameter moves outside the user–specified operating range, an alarm output (**ALM0** – **ALM2**) becomes active. System Monitor issues a special alarm called Over–Temperature (**OT**) if the FPGA temperature exceeds a user–specified upper limit. By default the over–temperature limit is set to 125°C. The **OT** signal is deactivated when the device temperature falls below a user–specified lower limit. If the FPGA power down feature is enabled, the FPGA enters power down when the **OT** signal becomes active. The FPGA powers up again when the alarm is deactivated. A separate system monitor output illuminates a red LED on the 71620 PCB, Section 2.4, when any parameter is outside the user limits.

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3.7 FPGA Resources Operation (continued)

3.7.1 FPGA System Monitor (continued)

The following is the memory map of the System Monitor Status registers (read only), including the BAR0 address offset of the register. All registers are 16 bits wide, and the register addresses are in increments of 32 bits.

Table 3–20: System Monitor Status Register Addresses

Register	Address BAR0+	Description
Temperature	**0x08000**	The result of the on–chip temperature sensor measurement.
V_{CCINT}	**0x08004**	The result of the on–chip V_{CCINT} 1.0V supply monitor measurement.
V_{CCAUX}	**0x08008**	The result of the on–chip V_{CCAUX} 2.5V supply monitor measurement.
V_P – V_{AUX8}	**0x0800C** – **0x0807C**	These locations are unused in the 71620
V_{AUX9}	**0x08064**	The result of the V_{AUX9} XMC VPWR (5V or 12V) supply measurement.
V_{AUX10}	**0x08068**	The result of the V_{AUX10} XMC 3.3V supply measurement.
V_{AUX11}	**0x0806C**	The result of the V_{AUX11} 1.8V supply measurement.
V_{AUX12}	**0x08070**	The result of the V_{AUX12} 1.5V supply measurement.
V_{AUX13} – V_{AUX15}	**0x08074** – **0x0807C**	These locations are unused in the 71620
Max Temp	**0x08080**	Maximum temperature measurement recorded since power–up or reset.
Max V_{CCINT}	**0x08084**	Maximum V_{CCINT} measurement recorded since power–up or reset.
Max V_{CCAUX}	**0x08088**	Maximum V_{CCAUX} measurement recorded since power–up or reset.
Undefined	**0x0808C**	This location is unused in the 71620
Min Temp	**0x08090**	Minimum temperature measurement recorded since power–up or reset.
Min V_{CCINT}	**0x08094**	Minimum V_{CCINT} measurement recorded since power–up or reset.
Min V_{CCAUX}	**0x08098**	Minimum V_{CCAUX} measurement recorded since power–up or reset.
Undefined	**0x0809C** – **0x080F8**	These locations are unused in the 71620
Flag	**0x080FC**	This register contains general status information

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3.7 FPGA Resources Operation (continued)

3.7.1 FPGA System Monitor (continued)

The following is the memory map of the System Monitor Control Registers (read and write) including the BAR0 address offset of the register. All registers are 16 bits wide, and the register addresses are in increments of 32 bits.

Table 3–21: System Monitor Control Register Addresses

Register	Address BAR0+	Description
Configuration registers 0 to 2	**0x08100 – 0x08108**	System Monitor configuration registers.
Test registers 0 to 4	**0x0810C – 0x0811C**	System Monitor Test registers. These registers are used for factory test and should be left at the default initialization.
Sequence registers	**0x08120 – 0x0813C**	Program the Channel Sequencer function in System Monitor.
Temperature Upper	**0x08140**	Program the **ALM0** Temperature Upper threshold.
V_{CCINT} Upper	**0x08144**	Program the **ALM1** Voltage Upper threshold.
V_{CCAUX} Upper	**0x08148**	Program the **ALM2** Voltage Upper threshold.
OT Upper	**0x0814C**	Program the **OT** Temperature Upper threshold.
Temperature Lower	**0x08150**	Program the **ALM0** Temperature Lower threshold.
V_{CCINT} Lower	**0x08154**	Program the **ALM1** Voltage Lower threshold.
V_{CCAUX} Lower	**0x08158**	Program the **ALM2** Voltage Lower threshold.
OT Lower	**0x0815C**	Program the **OT** Temperature Lower threshold.

System Monitor generates an alarm signal on the outputs **ALM0** – **ALM2** when an internal sensor measurement (Temperature, V_{CCINT}, or V_{CCAUX}) exceeds the user–defined thresholds programmed by these control registers. The alarms are reset when a subsequently measured value falls inside the threshold.

System Monitor issues the **OT** alarm if the FPGA temperature exceeds the OT Upper threshold. The **OT** alarm is deactivated when the device temperature falls below the OT Lower threshold.

The default alarm thresholds programmed at system power on are shown on the next page.

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3.7 FPGA Resources Operation (continued)

3.7.1 FPGA System Monitor (continued)

The System Monitor alarm threshold registers are programmed for the following defaults at power on or System Monitor reset.

System Monitor Port	Alarm	Default Threshold
Internal Temperature	**OT**	Upper – 125.0 °C
		Lower – 70.0 °C
	ALM0	Upper – 100.0 °C
		Lower – 90.0 °C
Internal V_{CCINT}	**ALM1**	Upper – 1.05 Volts
		Lower – 0.96 Volts
Internal V_{CCAUX}	**ALM2**	Upper – 2.625 Volts
		Lower – 2.375 Volts

3.7.2 I^2C Bus Controllers

The Virtex–6 FPGA provides two I^2C serial buses. Both I^2C buses are controlled using 71620 registers.

- I^2C bus #1 is used internally on the 71620 for several temperature sensors and for control of the Si571 VCXO. Refer to Section 5.31 for the FPGA registers that control this bus.

- I^2C bus #2 is connected to the XMC **P15** connector **MSDA** (I^2C serial data) and **MSCL** (I^2C serial clock) pins, and provides access to the on–board serial EEPROM. Refer to Section 5.33 for the FPGA registers that control this bus.

  The serial EEPROM is used for Cobalt board identification, as described in Section 5.34.

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3.8 FLASH Memory Operation

A 64–MByte bank of FLASH memory is provided for FPGA boot code. Up to four Processing FPGA boot configurations can be stored in FLASH, identified as Version 0, Version 1, Version 2, and Version 3. Versions 0 and 1 are the Pentek–supplied default boot configuration (0 is the Gen 1 x4 PCIe code, 1 is the Gen 2 x4 PCIe code) and Versions 2 and 3 are reserved for user–defined configurations.

At power–up, PCB switches **SW2–3:4** designate which one of the FPGA configurations to boot from FLASH, as indicated in Section 2.2.2.

FLASH memory is write–protected using PCB switch **SW2–1**. See Section 2.2.2 for these switch settings.

The following table shows the memory map of FLASH.

Table 3–22: FLASH Memory Map

FLASH Memory Address	FLASH Memory Storage
BAR4 + **0x000 0000** – **0x1FF FFFF**	Version 0 Boot Code – Gen 1 x8 PCIe (Pentek–supplied)
BAR4 + **0x200 0000** – **0x3FF FFFF**	Version 1 Boot Code – Gen 2 x4 PCIe (Pentek–supplied)
BAR4 + **0x400 0000** – **0x5FF FFFF**	Version 2 Boot Code
BAR4 + **0x600 0000** – **0x7FF FFFF**	Version 3 Boot Code
The Versions 2 and 3 Boot Code storage areas are blank as shipped from the factory.	

3.9 User Register Address Space

The FPGA provides a block of addresses reserved for user registers for custom processing of data from or to the Model 71620 resources. Access these registers using PCI Base Address Register 2 at addresses BAR2 + **0x000000** to **0x3FFFFF**.

In the default FPGA configurations, these register addresses perform no functions, but are available as read/write temporary storage. You can read and write any type of data to each register address.

NOTE: If you have ordered a Pentek–defined custom FPGA Option, the user space may be programmed for that option's processing. Any such use of these User FPGA Address Space registers is defined in the applicable Pentek documentation for that option.

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Chapter 4: Model 71620 Memory Maps

4.1 Overview

This chapter describes access to the Model 71620 resources and control registers from an external (off–board) PCIe Bus Master, such as an XMC baseboard processor. Mem–ory maps to these resources are given from the baseboard processor's viewpoint.

The Model 71620 is controlled from the XMC baseboard through a PCIe Bus interface. All 71620 resources are configured to be available in PCI Address Space, relative to PCI Base Address Registers as listed in the following table. See Appendix A for a summary of the PCI Configuration Space Registers.

Table 4–1: Model 71620 PCI Memory Map

PCI Bus Address *	Resource	Information
BAR0 + **0x00000** – **0x3FFFF**	FPGA Registers	Section 4.2
BAR1	Reserved	–
BAR2 + **0x000000** – **0x3FFFFF**	User Register Space	Section 3.9
BAR3	Reserved	–
BAR4 + **0x0000000** – **0x7FFFFFF**	FLASH Memory	Section 3.8

* Refer to the operating manual supplied with your baseboard or carrier for the PCI Base Address settings.

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4.2 Default FPGA Memory Map

The following is the memory map of the default FPGA registers accessible from an XMC baseboard processor, including the PCI BAR0 address offset of the register and a reference to the description for each register. All registers are 32–bits wide, and the register addresses are in increments of 32 bits (four bytes).

Table 4–2: Default FPGA Memory Map

Address Offset BAR0+	Register	Access	Description
PCIe Control and Status Registers			
0x00000	Link Status	RO	Section 5.2
0x00004	Interrupt Flag	R/Clr	Section 5.3
0x00008	Interrupt Enable	R/W	Section 5.4
0x0000C	Byte Swap	R/W	Section 5.5
0x00010	Interrupt Control	R/W	Section 5.6
0x00014	Global Register Reset	R/W	Section 5.7
0x00018 - 0x03FFC	Reserved	–	–
Board and Code Identification Registers			
0x04000	Board Identification	RO	Section 5.8
0x04004	Daughter Board Identification	RO	Section 5.9
0x04008	Reserved	–	–
0x0400C	Reserved	–	–
0x04010	FPGA Code Type	RO	Section 5.10
0x04014	FPGA Code Revision	RO	Section 5.11
0x04018	FPGA Date Code	RO	Section 5.12
All addresses are offset from PCI Base Address Register 0 (**BAR0**)			

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4.2 Default FPGA Memory Map (continued)

Table 4–2: Default FPGA Memory Map (continued)

Address Offset BAR0+	Register	Access	Description
Global Control Registers			
0x0401C	ICAP	R/W	Section 5.13
0x04020	CDC Control/Status	R/W	Section 5.14
0x04024	CDC Data	R/W	Section 5.15
0x04028	Clock Control/Status	R/W	Section 5.16
0x0402C	Sync Bus Control 1	R/W	Section 5.17
0x04030	Sync Bus Control 2	R/W	Section 5.18
0x04034	Sync Bus Input Delay Tap Control	R/W	Section 5.19
0x04038	Sync Bus Input Delay Control	R/W	Section 5.20
0x0403C	User LED	R/W	Section 5.21
0x04040	LED Control	R/W	Section 5.22
0x04044	Gate A Generate	R/W	Section 5.23
0x04048	Gate B Generate	R/W	Section 5.24
0x0404C	Sync A Generate	R/W	Section 5.25
0x04050	Sync B Generate	R/W	Section 5.26
0x04054	Test Signal and Timestamp Control	R/W	Section 5.27
0x04058	Test Sine A Frequency Control	R/W	Section 5.28
0x0405C	Test Sine B Frequency Control	R/W	Section 5.29
0x04060	Timestamp Start Time	WO	Section 5.30
0x04064	TWSI Port 1 Control/Status	R/W	Section 5.31
0x04068	TWSI Port 1 Data	R/W	Section 5.32
0x0406C	TWSI Port 2 Control/Status	R/W	Section 5.33
0x04070	TWSI Port 2 Data	R/W	Section 5.34
0x04074	Global Interrupt Source Enable	R/W	Section 5.35
0x04078	Global Interrupt Status	RO	Section 5.36
0x0407C	Global Interrupt Flag	R/Clr	Section 5.37
FPGA System Monitor Registers			
0x08000 - 0x080FC	System Monitor Status Registers	RO	Section 3.7.1
0x08100 - 0x0815C	System Monitor Control Registers	R/W	
All addresses are offset from PCI Base Address Register 0 (**BAR0**)			

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4.2 Default FPGA Memory Map (continued)

Table 4–2: Default FPGA Memory Map (continued)

Address Offset BAR0+	Register	Access	Description
A/D Channel 1 Registers			
0x10000	Channel Status/Power Management	R/W	Section 6.2
0x10004	ADC Input Delay Tap Control	R/W	Section 6.3
0x10008	ADC Data Control	R/W	Section 6.4
0x1000C	ADC Rate Divider	R/W	Section 6.5
0x10010	ADC Gate/Trigger Control	R/W	Section 6.6
0x10014	ADC Trigger Gen Linked List Start Pointer	R/W	Section 6.7
0x10018	Local Gate Generate	R/W	Section 6.8
0x1001C	RAM Control	R/W	Section 6.9
0x10020	Input DC Offset	R/W	Section 6.10
0x10024	Input Gain Trim	R/W	Section 6.11
0x10028	ADC DMA Control	R/W	Section 6.12
0x1002C	ADC Interrupt Enable	R/W	Section 6.13
0x10030	ADC Interrupt Flag	R/Clr	Section 6.14
0x10034	ADC Interrupt Status	RO	Section 6.15
0x10038	IDelay and Clock Status	RO	Section 6.16
0x1003C	RAM Controller Status	RO	Section 6.17
0x10040	RAM FIFO Count	RO	Section 6.18
0x10044	Reserved	–	–
0x10048	Reserved	–	–
0x1004C	ADC DMA Status	RO	Section 6.19
0x10050 - 0x10058	Reserved	–	–
0x1005C	Data Rate Detection Control	R/W	Section 6.20
0x10060	Data Rate Detect Value	RO	Section 6.21
0x10064	Peak Data Rate Detect Value	RO	Section 6.22
0x10068 - 0x107FC	Reserved	–	–
0x10800 - 0x10BFC	ADC Trigger Controller Linked List RAM	R/W	Section 3.2.2
0x14000 - 0x15FFC	ADC DMA Linked List RAM	R/W	Section 3.2.4

All addresses are offset from PCI Base Address Register 0 (**BAR0**)

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4.2 Default FPGA Memory Map (continued)

Table 4–2: Default FPGA Memory Map (continued)

Address Offset BAR0+	Register	Access	Description
A/D Channel 2 Registers			
0x18000	Channel Status/Power Management	R/W	Section 6.2
0x18004	ADC Input Delay Tap Control	R/W	Section 6.3
0x18008	ADC Data Control	R/W	Section 6.4
0x1800C	ADC Rate Divider	R/W	Section 6.5
0x18010	ADC Gate/Trigger Control	R/W	Section 6.6
0x18014	ADC Trigger Gen Linked List Start Pointer	R/W	Section 6.7
0x18018	Local Gate Generate	R/W	Section 6.8
0x1801C	RAM Control	R/W	Section 6.9
0x18020	Input DC Offset	R/W	Section 6.10
0x18024	Input Gain Trim	R/W	Section 6.11
0x18028	ADC DMA Control	R/W	Section 6.12
0x1802C	ADC Interrupt Enable	R/W	Section 6.13
0x18030	ADC Interrupt Flag	R/Clr	Section 6.14
0x18034	ADC Interrupt Status	RO	Section 6.15
0x18038	IDelay and Clock Status	RO	Section 6.16
0x1803C	RAM Controller Status	RO	Section 6.17
0x18040	RAM FIFO Count	RO	Section 6.18
0x18044	Reserved	–	–
0x18048	Reserved	–	–
0x1804C	ADC DMA Status	RO	Section 6.19
0x18050 - 0x18058	Reserved	–	–
0x1805C	Data Rate Detection Control	R/W	Section 6.20
0x18060	Data Rate Detect Value	RO	Section 6.21
0x18064	Peak Data Rate Detect Value	RO	Section 6.22
0x18068 - 0x187FC	Reserved	–	–
0x18800 - 0x18BFC	ADC Trigger Controller Linked List RAM	R/W	Section 3.2.2
0x1C000 - 0x1DFFC	ADC DMA Linked List RAM	R/W	Section 3.2.4
All addresses are offset from PCI Base Address Register 0 (**BAR0**)			

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4.2 Default FPGA Memory Map (continued)

Table 4–2: Default FPGA Memory Map (continued)

Address Offset BAR0+	Register	Access	Description
A/D Channel 3 Registers			
0x20000	Channel Status/Power Management	R/W	Section 6.2
0x20004	ADC Input Delay Tap Control	R/W	Section 6.3
0x20008	ADC Data Control	R/W	Section 6.4
0x2000C	ADC Rate Divider	R/W	Section 6.5
0x20010	ADC Gate/Trigger Control	R/W	Section 6.6
0x20014	ADC Trigger Gen Linked List Start Pointer	R/W	Section 6.7
0x20018	Local Gate Generate	R/W	Section 6.8
0x2001C	RAM Control	R/W	Section 6.9
0x20020	Input DC Offset	R/W	Section 6.10
0x20024	Input Gain Trim	R/W	Section 6.11
0x20028	ADC DMA Control	R/W	Section 6.12
0x2002C	ADC Interrupt Enable	R/W	Section 6.13
0x20030	ADC Interrupt Flag	R/Clr	Section 6.14
0x20034	ADC Interrupt Status	RO	Section 6.15
0x20038	IDelay and Clock Status	RO	Section 6.16
0x2003C	RAM Controller Status	RO	Section 6.17
0x20040	RAM FIFO Count	RO	Section 6.18
0x20044	Reserved	–	–
0x20048	Reserved	–	–
0x2004C	ADC DMA Status	RO	Section 6.19
0x20050 - 0x20058	Reserved	–	–
0x2005C	Data Rate Detection Control	R/W	Section 6.20
0x20060	Data Rate Detect Value	RO	Section 6.21
0x20064	Peak Data Rate Detect Value	RO	Section 6.22
0x20068 - 0x207FC	Reserved	–	–
0x20800 - 0x20BFC	ADC Trigger Controller Linked List RAM	R/W	Section 3.2.2
0x24000 - 0x25FFC	ADC DMA Linked List RAM	R/W	Section 3.2.4

All addresses are offset from PCI Base Address Register 0 (**BAR0**)

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4.2 Default FPGA Memory Map (continued)

Table 4–2: Default FPGA Memory Map (continued)

Address Offset BAR0+	Register	Access	Description
DAC Channel Registers			
0x30000	Channel Status/Power Management	R/W	Section 7.2
0x30004	Output Delay Tap Control	R/W	Section 7.3
0x30008	DAC Data Control	R/W	Section 7.4
0x3000C	DAC Rate Divider	R/W	Section 7.5
0x30010	DAC Gate/Trigger Control	R/W	Section 7.6
0x30014	Output Controller Linked List Start Pointer	R/W	Section 7.7
0x30018	RAM Capture Start Address	R/W	Section 7.8
0x3001C	RAM Control	R/W	Section 7.9
0x30020	Output Gate Delay	R/W	Section 7.10
0x30024	Reserved	–	–
0x30028	DAC DMA Control	R/W	Section 7.11
0x3002C	DAC Interrupt Enable	R/W	Section 7.12
0x30030	DAC Interrupt Flag	R/Clr	Section 7.13
0x30034	DAC Interrupt Status	RO	Section 7.14
0x30038	ODelay and Clock Status	RO	Section 7.15
0x3003C	RAM Controller Status	RO	Section 7.16
0x30040	Reserved	–	–
0x30044	RAM Capture Count	RO	Section 7.17
0x30048	Reserved	–	–
0x3004C	DAC DMA Status	RO	Section 7.18
0x30050	Reserved	–	–
0x30054	DAC Serial Address	R/W	Section 7.19
0x30058	DAC Serial Data	R/W	Section 7.20
0x3005C	Data Rate Detection Control	R/W	Section 7.21
0x30060	Data Rate Detect Value	RO	Section 7.22
0x30064	Peak Data Rate Detect Value	RO	Section 7.23
0x30068 - 0x307FC	Reserved	–	–
0x30800 - 0x30FFC	DAC Output Controller Linked List RAM	R/W	Section 3.3.2
0x34000 - 0x35FFC	DAC DMA Linked List RAM	R/W	Section 3.3.1
All addresses are offset from PCI Base Address Register 0 (**BAR0**)			

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Chapter 5: Global Registers

5.1 Overview

This chapter describes access to the common registers from an external (off–board) PCIe Bus Master. These registers and memory regions are common to all FPGA code configurations.

Refer to Chapter 4 for the memory maps of all 71620 registers.

All register descriptions are given from an XMC baseboard processor's viewpoint. All registers are 32–bits wide, and the register addresses are in increments of 32 bits (four bytes).

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5.2 Link Status Register

The read–only Link Status Register reports the current status of the 71620 PCIe interface link.

The following table shows the contents of this register. The subsections following the table provide descriptions of the bits in this register.

Table 5–1: Link Status Register
RO @ BAR0+0x00000

Bit	31 – 23							24
Bit Name	Reserved							MSI ENABLED
Function	Write zeros, Mask read							0 = Disabled 1 = Enabled
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Bit Name	Reserved	MAX RD RQST			Reserved	MAX PAYLOAD		
Function	Mask read	000 = 128 Bytes 001 = 256 Bytes 010 = 512 Bytes 011 = 1024 Bytes 100 = 2048 Bytes 101 = 4096 Bytes			Mask read	000 = 128 Bytes 001 = 256 Bytes 010 = 512 Bytes 011 = 1024 Bytes 100 = 2048 Bytes 101 = 4096 Bytes		
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Bit Name	SEL LINK WIDTH		CORE NOM WIDTH		SEL LINK RATE	CORE NOM SPEED	Reserved	LINK UPCFG CAP
Function	00 = x1 link 01 = x2 link 10 = x4 link 11 = x8 link		00 = x1 link 01 = x2 link 10 = x4 link 11 = x8 link		0 = 2.5 GT/s 1 = 5.0 GT/s	0 = Gen 1 x8 1 = Gen 2 x4	Mask read	0 = Not cap. 1 = Up Config capable
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	PARTNER GEN2 SPRT	LINK GEN2 CAP	LANE RVRSL MODE		Reserved	INITIAL LINK WIDTH		
Function	0 = Not cap. 1 = Gen2 capable	0 = Not cap. 1 = Gen2 capable	00 = No reversal 01 = Lanes 1:0 reversed 10 = Lanes 3:0 reversed 11 = Lanes 7:0 reversed		Mask read	000 = Link not Trained 001 = 1 lane link 010 = 2 lane link 011 = 4 lane link 100 = 8 lane link		
When reset, including power on, the state of this register is unknown.								

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5.2 Link Status Register (continued)

5.2.1 MSI ENABLED Bit 24

This read–only bit indicates the status of MSI interrupts. When read as logic '0' MSI interrupts are not enabled. When read as logic '1' MSI interrupts are being used instead of INTA.

5.2.2 MAX RD RQST Bits 22 – 20

These read–only bits indicate the maximum read request size suggested by the system, as follows.

000 128 Bytes
001 256 Bytes
010 512 Bytes
011 1024 Bytes
100 2048 Bytes
101 4096 Bytes

NOTE: When setting up DAC DMA link definitions with manual read request size control, depending on the system, you may find that exceeding this amount may be required to maintain real–time at high DAC output rates. Selecting automatic read request size mode will use this value automatically as the default request size.

5.2.3 MAX PAYLOAD Bits 18 – 16

These read–only bits indicate the maximum payload size allowed by the system, as follows.

000 128 Bytes
001 256 Bytes
010 512 Bytes
011 1024 Bytes
100 2048 Bytes
101 4096 Bytes

NOTE: Depending on the system it may be less than or equal to the maximum that the 71620 can handle (512 bytes). When setting up ADC DMA link definitions with manual payload size control, it is important that you do not exceed the value read here. Selecting automatic payload size mode will use this value automatically as the default payload size.

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5.2 Link Status Register (continued)

5.2.4 SEL LINK WIDTH Bits 15 – 14

These read–only bits indicate the current link width, as follows:

00 x1 link
01 x2 link
10 x4 link
11 x8 link

5.2.5 CORE NOM WIDTH Bits 13 – 12

These read–only bits indicate the PCIe core default link width, as follows:

00 x1 link
01 x2 link
10 x4 link
11 x8 link

5.2.6 SEL LINK RATE Bit 11

This read–only bit indicates the current PCIe interface link rate. When read as logic '0' the current link rate is 2.5 GT/s (gigatransfers per second). When read as logic '1' the current link rate is 5.0 GT/s.

5.2.7 CORE NOM SPEED Bit 10

This read–only bit indicates the current PCIe core nominal speed. When read as logic '0' the PCIe core is a Gen 1 x8 core by default. When read as logic '1' the PCIe core is a Gen 2 x4 core by default.

5.2.8 LINK UPCFG CAP Bit 8

This read–only bit indicates the current PCIe interface link upconfigure capability. When read as logic '0' the link is not upconfigure capable. When read as logic '1' the link is upconfigure capable.

5.2.9 PARTNER GEN2 SPRT Bit 7

This read–only bit indicates if the PCIe link partner supports Gen 2 PCIe. When read as logic '0' the link partner is not Gen 2 capable. When read as logic '1' the link partner supports a Gen 2, 5.0 GT/s (gigatransfers per sec–ond) data rate.

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5.2 **Link Status Register** (continued)

5.2.10 LINK GEN2 CAP Bit 6

This read−only bit indicates if the PCIe link is Gen 2 capable (both the Link Partner and the Device are Gen 2 capable). When read as logic '0' the link is not Gen 2 capable. When read as logic '1' the link supports Gen 2, 5.0 GT/s data rate.

5.2.11 LANE RVRSL MODE Bits 5 – 4

These read−only bits indicate the current lane reversal mode, as follows:

00 No reversal
01 Lanes 1:0 reversed
10 Lanes 3:0 reversed
11 Lanes 7:0 reversed

5.2.12 INITIAL LINK WIDTH Bits 2 – 0

These read−only bits indicate the initial negotiated link width after the PCIe port has achieved the first successful link training, as follows:

000 Link not trained
001 x1 link
010 x2 link
011 x4 link
100 x8 link

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5.3 Interrupt Flag Register

The Interrupt Flag Register contains one latched bit associated with each 71620 system interrupt condition.

The following table shows the contents of this register. Table 5–3, on the next page, describes the interrupt condition associated with each bit.

Table 5–2: Interrupt Flag Register
R/Clr@ BAR0+0x00004

Bit	**31 – 16**							
Bit Name	Reserved							
Function	Mask when reading							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Bit Name	USER 6	USER 5	USER 4	USER 3	USER 2	USER 1	Reserved	
Function	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Reserved	DAC ACQ MODULE 1	Reserved	ADC ACQ MODULE 3	ADC ACQ MODULE 2	ADC ACQ MODULE 1	Reserved	GLBL
Function	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch							

IMPORTANT! When reset, including power–up, the state of this register is unknown. You should clear this register before using it, by writing '1's into all bits.

Each bit in this register latches the edge interrupt events from various modules. Logic '1' in any bit in this register indicates that an interrupt has occurred. To clear any bit in this register that is set to '1' you must write a '1' to that bit.

If the corresponding bit in the Interrupt Enable Register (Section 5.4) has been set to logic '1', then any Interrupt Flag Register bit transition from logic '0' to logic '1' will also generate an interrupt to the PCIe interface. If you do not want an interrupt to occur and have set the corresponding interrupt enable bit to '0', you may poll any Interrupt Flag Register bit to determine if an event has occurred.

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5.3 Interrupt Flag Register (continued)

The following table describes the interrupt source and condition associated with each bit of the Interrupt Flag and Interrupt Enable registers.

Table 5–3: Interrupt Register Bits

Bit Name	Bit Position	Interrupt Function
USER 1 – 6	15 – 10	These bits are reserved for user–defined interrupt functions. These are also used by Pentek–installed FPGA IP cores.
DAC ACQ MODULE 1	6	This bit is associated with an interrupt from any of the enabled interrupts in the DAC Interrupt Enable Register (Section 7.12).
ADC ACQ MODULE 1 – 3	4, 3, 2	Each of these bits is associated with an interrupt from any of the enabled interrupts in each of the ADC Interrupt Enable Registers (Section 6.13).
GLBL	0	This bit is associated with an interrupt from any of the enabled interrupts in the Global Interrupt Enable Register (Section 5.35).
These bit assignments and definitions apply to the Interrupt Enable Register, Section 5.4, and the Interrupt Flag Register, Section 5.3		

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5.4 Interrupt Enable Register

The Interrupt Enable Register contains one enable bit associated with each 71620 system interrupt condition.

The following table shows the contents of this register. Table 5–3, on the prior page, describes the interrupt condition associated with each bit.

Table 5–4: Interrupt Enable Register
R/W@ BAR0+0x00008

Bit	31 – 16							
Bit Name	Reserved							
Function	Write zeros, Mask when reading							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Bit Name	USER 6	USER 5	USER 4	USER 3	USER 2	USER 1	Reserved	
Function	0 = Disable Interrupt 1 = Enable Interrupt							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Reserved	DAC ACQ MODULE 1	Reserved	ADC ACQ MODULE 3	ADC ACQ MODULE 2	ADC ACQ MODULE 1	Reserved	GLBL
Function	0 = Disable Interrupt 1 = Enable Interrupt							
All bits default to the logic '0' state at power on and reset								

Each bit of this register enables or disables the generation of an interrupt for an interrupt condition. Setting the bit associated with a given interrupt to logic '1' enables the generation of an interrupt to the PCIe interface when that interrupt condition occurs from the associated Interrupt Flag Register, Section 5.3. When a bit is cleared to logic '0' (its default state) the interrupt will not be generated by the defined interrupt condition.

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5.5 Byte Swap Register

The Byte Swap Register enables or disables byte swap for all 64–bit PCIe transactions.

The following table shows the contents of this register.

Table 5–5: Byte Swap Register
R/W @ BAR0+0x0000C

Bit	31 – 25	24	23 – 1	0
Bit Name	Reserved	BYTE SWAP	Reserved	BYTE SWAP
Function	Write zeros, Mask read	0 = No swap 1 = Swap	Write zeros, Mask read	0 = No swap 1 = Swap
All bits default to the logic '0' state at power on and reset				

NOTE: You must set both bits 0 and 24 to the same value so that the command is seen regardless of the present BYTE SWAP setting.

When the Byte Swap bit is cleared (No Swap) the byte order of a 64–bit word is as indicated in the top line below; when Byte Swap is enabled the order of bytes in the 64-bit PCIe interface is reversed as indicated in the bottom line below.

No Swap (BYTE SWAP = 0)								
Bits	63 – 56	55 – 48	47 – 40	39 – 32	31 – 24	23 – 16	15 – 8	7 – 0
Byte	Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0

Swap Enabled (BYTE SWAP = 1)								
Bits	63 – 56	55 – 48	47 – 40	39 – 32	31 – 24	23 – 16	15 – 8	7 – 0
Byte	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7

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5.6 Interrupt Control Register

The Interrupt Control Register controls the 71620 PCIe interrupt.

The following table shows the contents of this register. The subsections following the register describe the contents of this register.

Table 5–6: Interrupt Control Register
R/W @ BAR0+0x00010

Bit	31 – 1	0
Bit Name	Reserved	FORCE INT DEASSERT
Function	Write zeros, Mask read	0 = Normal 1 = Force clear
All bits default to the logic '0' state at power on and reset		

The FORCE INT DEASSERT bit forcibly clears the PCIe interrupt by making the PCIe interface send an INT OFF message. When this bit is cleared to logic '0' (its default state) the interrupt operates normally. When the bit is set to logic '1' the interrupt is forcibly cleared.

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5.7 Global Register Reset Register

The Global Register Reset Register resets all control registers in the 71620.

The following table shows the contents of this register. The subsections following the register describe the contents of this register.

Table 5–7: Global Register Reset Register
R/W @ BAR0+0x00014

Bit	31 – 1	0
Bit Name	Reserved	GLOBAL RESET
Function	Write zeros, Mask read	0 = Run 1 = Reset
All bits default to the logic '0' state at power on and reset		

The GLOBAL RESET bit forcibly resets all registers in the 71620. When set to '1', all control registers will be set to their power–up default values. Note that this bit does not clear linked lists as they are stored in RAM.

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5.8 Board Identification Register

The read–only Board Identification Register provides the Pentek Model 71620 board identification.

Table 5–8: Board Identification Register
RO @ BAR0+0x04000

Bit	31 – 20	19 – 16	15 – 12	11 – 8	7 – 4	3 – 0
Bit Name	Reserved	Board Identification				
Function	Mask read	0111	0001	0110	0010	0000
When reset, including power on, this register should always read as indicated above.						

These read–only bits indicate the board identification. When read, this register always returns a value of **0x00071620**.

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5.9 Daughter Board ID Register

The read–only Daughter Board ID Register identifies the types of RAM Memory boards and Front Panel I/O board that are installed on this 71620.

The following table shows the contents of this register. The subsections following the register describe the contents of this register.

Table 5–9: Daughter Board ID Register
RO @ BAR0+0x04004

Bit	**31 – 16**							
Bit Name	Reserved							
Function	Mask when reading							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Bit Name	Reserved	FPGA TYPE			Reserved	FPIO TYPE		
Function	Mask read	See Section 5.9.1			Mask read	010		
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Reserved		MEM CD TYPE		Reserved		MEM AB TYPE	
Function	Mask read		00 = 16MB QDRII+ 01 = Reserved 10 = 1 GB DDR3 11 = No Memory		Mask read		00 = 16MB QDRII+ 01 = Reserved 10 = 1 GB DDR3 11 = No Memory	
All bits default to the installed configuration at power on and reset								

5.9.1 FPGA TYPE Bits 14 – 12

These three read–only bits indicate the type of FPGA on the board. This depends on the FPGA option, and reads as follows:

000 Xilinx Virtex–6 XC6VLX130T – Option 061
001 Reserved
010 Xilinx Virtex–6 XC6VLX240T – Option 062
011 Xilinx Virtex–6 XC6VLX365T – Option 063
100 Xilinx Virtex–6 XC6VSX315T – Option 064
101 Xilinx Virtex–6 XC6VSX475T – Option 065
110 – 111 Reserved

5.9.2 FPIO TYPE Bits 10 – 8

These three read–only bits indicate the type of Front Panel I/O module installed on the board. This is fixed as '**010**' for the Model 71620 board.

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5.9 Daughter Board ID Register (continued)

5.9.3 MEM CD TYPE Bits 5 – 4

These read–only bits indicate the type of Memory Module 2 installed on the board. This depends on the memory option, and reads as follows:

00 16MB QDRII+ (Option 150)
01 Reserved
10 1 GB DDR3 (Option 155)
11 No Memory Module detected

5.9.4 MEM AB TYPE Bits 1 – 0

These read–only bits indicate the type of Memory Module 1 installed on the board. This depends on the memory option, and reads as follows:

00 16MB QDRII+ (Option 160)
01 Reserved
10 1 GB DDR3 (Option 165)
11 No Memory Module detected

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5.10 FPGA Code Type Register

The read–only FPGA Code Type Register identifies the type of FPGA code currently installed in the FPGA for the main board and for each memory module.

The following table shows the contents of this register. The subsections following the register describe the contents of this register.

Table 5–10: FPGA Code Type Register
RO @ BAR0+0x04010

Bit	31	30 – 28	27–26	25 – 24	23 – 22	21 – 20	19 – 16
Bit Name	Reserved	FPGA CODE EXPL	Reserved	MEM CD CODE	Reserved	MEM AB CODE	FPGA CODE ID
Function	Mask read	000 = N/A 001 = No Mem 010 = QDRII+ 011 = DDR3 100 = Mixed	Mask read	00 = QDRII 01 = N/A 10 = DDR3 11 = none	Mask read	00 = QDRII+ 01 = N/A 10 = DDR3 11 = none	0111

Bit	15 – 12	11 – 8	7 – 4	3 – 0
Bit Name	FPGA CODE ID			CODE TYPE
Function	0001	0110	0010	0000 = No code 0001 = WB DDC 0010 = NB DDC 0011 - 1111 = TBD

All bits default to the installed FPGA code types at power on and reset

5.10.1 FPGA CODE EXPL Bits 30 – 28

These three read–only bits indicate the type of FPGA example code installed for the board. This reads as follows:

001 No memory example code
010 QDRII+ example code
011 DDR3 example code
100 Mixed example code – QDRII+ for banks A/B; DDR3 for banks C/D

5.10.2 MEM CD CODE Bits 25 – 24

These two read–only bits indicate the memory type for which the FPGA code was compiled for memory banks C & D. This reads as follows:

00 QDRII+ SRAM
10 DDR3 SDRAM
11 no memory

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5.10 FPGA Code Type Register (continued)

5.10.3 MEM AB CODE Bits 21 – 20

These two read–only bits indicate the memory type for which the FPGA code was compiled for memory banks A & B. This reads as follows:

00 QDRII+ SRAM
10 DDR3 SDRAM
11 no memory

5.10.4 FPGA CODE ID Bits 19 – 4

These read–only bits indicate the board type for which the FPGA code was compiled. This must match the first four digits of the Board ID register value (Section 5.8) for proper operation. When read, this field always returns a value of **0x7162**.

5.10.5 CODE TYPE Bits 3 – 0

These read–only bits indicate the type of FPGA IP code compiled into the FPGA core. This reads as follows:

0000	No code
0001	Wideband DDC
0010	Narrowband DDC
0011 – 1111	TBD

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5.11 FPGA Code Revision Register

The read–only FPGA Code Revision Register identifies the Pentek version number of the FPGA code currently installed in the FPGA.

The following table shows the contents of this register. The paragraph below the register describes the contents of this register.

Table 5–11: FPGA Code Revision Register
RO @ BAR0+0x04014

Bit	31 – 8	7 – 0
Bit Name	Reserved	REV
Function	Mask when reading	Code Revision Number
All bits default to the installed FPGA code revision number at power on and reset		

The FPGA Code Revision number is a binary value, starting at revision 0 through 255.

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5.12 FPGA Date Code Register

The read–only FPGA Date Code Register identifies the date of the FPGA code currently installed in the FPGA.

The following table shows the contents of this register. The paragraphs below the reg–ister describe the contents of this register.

Table 5–12: FPGA Date Code Register
RO @ BAR0+0x04018

Bit	31 – 24		23 – 20	19 – 16
Bit Name	Reserved		MONTH	
Function	Mask when reading		1st Digit of Month	2nd Digit of Month
Bit	**15 – 12**	**11 – 8**	**7 – 4**	**3 – 0**
Bit Name	DAY		YEAR	
Function	1st Digit of Day	2nd Digit of Day	3rd Digit of Year	4th Digit of Year
All bits default to the programmed FPGA date coding at power on and reset				

The FPGA code revision date is coded as six BCD characters as follows:

Month: bits 23 – 20, 1st digit of Month
bits 19 – 16, 2nd digit of Month

Day: bits 15 – 12, 1st digit of Day
bits 11 – 8, 2nd digit of Day

Year: bits 7 – 4, 3rd digit of Year
bits 3 – 0, 4th digit of Year

For example, the date of **July 15, 2010** (7/15/10) would read as follows: **0x00071510**

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5.13 ICAP Register

The ICAP Register provides a read/write capability for reconfiguring the FPGA. This is the internal reconfiguration port (ICAP Port) for the FPGA, and is for Pentek use only.

WARNING!!– **Only advanced users who have FPGA reconfiguration experience should use the ICAP port.**

The following table shows the contents of the ICAP Register.

Table 5–13: ICAP Register
R/W @ BAR0+0x0401C

Bit	31 – 16
Bit Name	ICAP
Function	ICAP data
All bits default to the logic '0' state at power on and reset	

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5.14 CDC Control/Status Register

The CDC Control/Status Register controls CDC7005 reprogramming and indicates the status of the CDC7005 clock synthesizer.

The following table shows the contents of this register. The subsections following the table provide descriptions of the bits in this register.

Table 5–14: CDC Control/Status Register
R/W @ BAR0+0x04020

Bit	31 – 16							
Bit Name	Reserved							
Function	Write zeros, Mask when reading							
Bit	**15 ***	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Bit Name	BUSY	PRGM	RESET	RST EN	Reserved			
Function	0 = Busy 1 = Not Busy	0 = Run 1 = Program	0 = Run 1 = Reset	0 = Disable 1 = Enable	Write zeros, Mask when reading			
Bit	**7**	**6**	**5**	**4**	**3**	**2 ***	**1 ***	**0 ***
Bit Name	Reserved					VCXO STAT	REF STAT	LOCK
Function	Write zeros, Mask when reading					0 = Not Valid 1 = Valid	0 = Not Valid 1 = Valid	0 = Not Valid 1 = Valid

* These bits are Read Only
Bits 14 & 13 default to the logic '0' state at power on and reset

5.14.1 BUSY Bit 15

The read–only BUSY bit indicates the status of a data transfer to the CDC7005 using the CDC Data Registers (Section 5.15). When PRGRM (bit 14 below) is enabled and data is written to the CDC7005 the BUSY bit goes to '0'. When PRGRM (bit 14 below) is cleared BUSY returns to '1'.

Refer to the PRGM bit 14, on the next page, for the CDC7005 writing sequence.

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5.14 CDC Control/Status Register (continued)

5.14.2 PRGM Bit 14

The rising edge of this bit initiates the program sequence for the CDC7005. When cleared to logic '0' (the default setting) the program function does not operate. When set to logic '1' the program sequence initiates, which serially transfers the value written by the CDC Data Register (Section 5.15) to the CDC7005.

NOTE: DO NOT SET PRGM to '1' until CDC_RDY (bit 12 in the Clock Control/Status Register, Section 5.16) is '1'.
DO NOT SET PRGM to '0' until BUSY (bit 15 above) goes low.

CDC7005 programming sequence:

1) Read the CDC_RDY status (bit 12 in the Clock Control/Status Register, Section 5.16). Wait until it is '1' (Ready) before proceeding. If it is not '1', another transfer is still in progress.

2) Write the desired value into CDC Data Register (Section 5.15).

WARNING!!– **Do not write this until CDC_RDY (bit 12 in Clock Control/Status Register) is '1' or the transfer in progress will be corrupted.**

3) Set PRGM to '1' (bit 14 in this register).

4) Poll the BUSY (bit 15 in this register). Wait until it is '0'. Note that the transfer takes approximately 2.5 microseconds, so sleeping for at least that long will reduce the register read traffic of repeated polling.

5) Once the BUSY bit is '0', then set PRGM to '0' (bit 14 in this register). The BUSY bit should return to '1'.

5.14.3 RESET Bit 13

This bit resets the CDC7005 and loads the default values to the CDC (see Section 5.15 for the default values). When the bit is cleared to logic '0' (its default state) the CDC7005 is in run. When the bit is set to logic '1' the CDC7005 is in reset.

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5.14 CDC Control/Status Register (continued)

5.14.4 RST EN Bit 12

This bit enables reset of the CDC7005 using the CLK B signal. Clear the bit to logic '0' (its default state) to disable the reset from this signal. Set the bit to logic '1' to enable CLK B to reset the CDC7005.

After setting RST EN to '1', each slave can generate a local CLK B signal with CDC RST, using the User LED register, Section 5.21. Alternately, the bus clock master could drive CLK B to all boards and that signal used. The CLK B signal is then sent to the CDC7005 to reset the dividers to be in phase with the master.

NOTE: ALWAYS set RST EN back to '0' to disable it. This is important to do; otherwise any other CLK B signal afterward would stop the CDC7005 clocks and put them in reset.

If the CDC7005 dividers (see Section 5.15) are all set to 1, then this special synchronization is not required.

5.14.5 VCXO STAT Bit 2

This read−only bit indicates the status of the Si571 VCXO clock input to the CDC7005. When read as logic '0' the VCXO input is not valid. When read as logic '1' the VCXO input is valid.

5.14.6 REF STAT Bit 1

This read−only bit indicates the status of the reference clock input to the CDC7005. When read as logic '0' the reference clock input is not valid. When read as logic '1' the reference clock input is valid.

5.14.7 LOCK Bit 0

This read−only bit indicates the status of the PLL lock for the CDC7005. When read as logic '0' the PLL lock is not valid (PLL is not locked). When read as logic '1' the PLL lock is valid (PLL is locked).

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5.15 CDC Data Register

The CDC Data Register is used to write to the CDC7005 clock synthesizer. The CDC7005 has four 32−bit addressable registers that configure the clock dividers and internal clock routing (see the CDC7005 Data Sheet in the Model 71620 Supplemental Manual, 809.7x620, for description of each CDC Word register). Each Word register in the CDC7005 is selected by the two least significant bits (bit 0 and bit 1) of the 32−bit CDC Data Register.

The following table shows the contents of this register.

Table 5−15: CDC Data Register
R/W @ BAR0+0x04024

Bit	31 – 2	1	0
Bit Name	CDC WORD DATA	C1	C0
Function	See Table 5−16, on page 120, for CDC Word 0 format, See Table 5−17, on page 121, for CDC Word 1 format, See Table 5−18, on page 122, for CDC Word 2 format, CDC Word 3 reserved for TI factory test purposes only	00 = Word 0 01 = Word 1 10 = Word 2 11 = Word 3	
All bits default to the logic '0' state at power on and reset			

WARNING!!− **Do not write to this register until CDC_RDY (bit 12 in Clock Control/Status Register, Section 5.16) is '1' or the transfer in progress will be corrupted.**

Write: Bits C1 and C0 in this register specify the word address for which one of the four CDC7005 32−bit registers you are writing to. After writing a new Word value to this FPGA register, use the PRGM bit in the CDC Control/ Status Register, Section 5.14, to transfer the Word value serially to the CDC7005.

Read: When this register is read back it returns the value of the last CDC Word written to the CDC7005 by this register.

The following pages show the format of each CDC Word Register, and the default val−ues programmed by the 71620 at power on and reset (see the CDC7005 Data Sheet in the Model 71620 Supplemental Manual, 809.7x620, for description of each CDC Word register).

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5.15 CDC Data Register (continued)

5.15.1 CDC Word 0 Register

Table 5–16: CDC Word 0 Register

Bit	31	30	29	28	27	26	25	24
Bit Name	MUXS2	MUXS1	MUXS0	OP3St	CP3St	Y43St	Y33St	Y23St
Function	MUXSEL Select			OPA 3–state	CP 3–state	Y4 3–state	Y3 3–state	Y2 3–state
Default	1	0	0	0	1	0	1	1
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Bit Name	Y13St	Y03St	CP3	CP2	CP1	CP0	PFD2	PFD1
Function	Y1 3–state	Y0 3–state	CP Current Setting				PFD Pulse Width	
Default	1	1	1	0	0	1	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Bit Name	PFD0	MD2	MD1	MD0	M9	M8	M7	M6
Function	PFD Pulse Width	Reference Delay M			Reference Divider M [bits 9:6]			
Default	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	M5	M4	M3	M2	M1	M0	C1	C0
Function	Reference Divider M [bits 5:0]						0	0
Default	0	0	0	0	1	1	0	0

Word 0 defaults to the value **0x8BE4000C** at power on and reset

The Y0, Y1, Y2, Y3, and Y4 designations refer to each of the five LVPECL outputs of the CDC7005. The five outputs are used as follows in the 71620:

- Y0 – ADC clocks
- Y1 – DAC clocks
- Y2 – Sync Bus Clock A output
- Y3 – Sync Bus Clock B output
- Y4 – not connected

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5.15 CDC Data Register (continued)

5.15.2 CDC Word 1 Register

Table 5–17: CDC Word 1 Register

Bit	31	30	29	28	27	26	25	24
Bit Name	REXT	CP_DIR	MUX42	MUX41	MUX40	MUX32	MUX31	MUX30
Function	Enable external reference resistor	CP regulate direction	MUX4 Select			MUX3 Select		
Default	0	1	0	1	0	0	0	0
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Bit Name	MUX22	MUX21	MIX20	MUX12	MUX11	MUX10	MUX02	MUX01
Function	MUX2 Select			MUX1 Select			MUX0 Select	
Default	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Bit Name	MUX00	ND2	ND1	ND0	N9	N8	N7	N6
Function	MUX0 Select	VCXO Delay M			VCXO Divider N [bits 9:6]			
Default	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	N5	N4	N3	N2	N1	N0	C1	C0
Function	VCXO Divider N [bits 5:0]						0	1
Default	0	0	1	0	0	1	0	1
Word 1 defaults to the value **0x50000025** at power on and reset								

The MUXn Select bits of the Word 1 register selects the clock frequency divisors (1, 2, 4, 8, or 16) for each of the five CDC LVPECL outputs. The default divisors of the five outputs are set as follows at power on or reset:

- MUX0 (Y0 – ADC clocks) = 1:1 (200 MHz) *
- MUX1 (Y1 – DAC clocks) = 1:1 (200 MHz)
- MUX2 (Y2 – Sync Bus Clock A output) = 1:1 (200 MHz)
- MUX3 (Y3 – Sync Bus Clock B output) = 1:1 (200 MHz)
- MUX4 (Y4 – not connected)

* **Take care that the ADC clock never exceeds the ADS5485 rated clock speed (200 MHz) during any change of frequency with the CDC7005 and/or the VCXO. Refer to VCXO Caution, Section 5.32.4.**

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5.15 CDC Data Register (continued)

5.15.3 CDC Word 2 Register

Table 5–18: CDC Word 2 Register

Bit	31 – 8							
Bit Name	Reserved							
Function	Write zeros, Mask when reading							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	LOCKW1	LOCKW0	ENBG	NRESET	NPD	HOLD	C1	C0
Function	Lock Detect WIndow		Enable Bandgap	Reset All Dividers	PD Current Sources	Enable Hold	1	0
Default	0	0	1	1	1	0	1	0
Word 2 defaults to the value **0x0000003A** at power on and reset								

NOTE: CDC Word 3 is reserved for Texas Instruments CDC7005 factory test purposes only and should not be accessed by the user.

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5.16 Clock Control/Status Register

The Clock Control/Status Register manages the CDC7005 output clocks, CDC CLKA (CDC7005 Y0 output) and CDC CLKB (CDC7005 Y1 output) and the FPGA internal clocks, FPGA CLKA and FPGA CLKB, and indicates the status of these clocks.

The following table shows the contents of this register. The subsections following the table provide descriptions of the bits in this register.

Table 5–19: Clock Control/Status Register
R/W @ BAR0+0x04028

Bit	31 – 16							
Bit Name	Reserved							
Function	Write zeros, Mask when reading							
Bit	**15**	**14**	**13**	**12 ***	**11 ***	**10 ***	**9 ***	**8 ***
Bit Name	Reserved			CDC RDY	CDC CLKB LOCKED	CDC CLKB DET	CDC CLKA LOCKED	CDC CLKA DET
Function	Write zeros, Mask when reading			0 =Not Ready 1 = Ready	0 =Not locked 1 = Locked	0 =Not valid 1 = Detected	0 =Not locked 1 = Locked	0 =Not valid 1 = Detected
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Reserved	FPGA CLKB SRC SEL	FPGA CLKB PWR DWN	Reserved		FPGA CLKA SRC SEL	FPGA CLKA PWR DWN	Reserved
Function	Write zero, Mask read	0 = CDC CLKB 1 = DAC Clk	0 = Operate 1 = Pwr dwn	Write zeros, Mask when reading		0 = CDC CLKA 1 = ADC1 Clk	0 = Operate 1 = Pwr dwn	Write zero, Mask read

* These bits are Read Only
Bits 0 – 7 default to the logic '0' state at power on and reset

5.16.1 CDC RDY

Bit 12

This read–only bit indicates the status of the CDC7005 interface. When read as logic '0' the CDC interface is not ready – do not access the CDC interface when it is not ready. When read as logic '1' the CDC is ready for a new request.

5.16.2 CDC CLKB/CLKA LOCKED

Bits 11, 9

Each of these read–only bits indicates the locked status of one of the CDC output clocks, either CDC CLKA or CDC CLKB depending on the bit selected. When read as logic '0' the clock is not locked. When read as logic '1' the clock is locked.

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5.16 Clock Control/Status Register (continued)

5.16.3 CDC CLKB/CLKA DET Bits 10, 8

Each of these read−only bits indicates the status of one of the CDC output clocks, either CDC CLKA or CLKB depending on the bit selected. When the bit is read as logic '0' a valid clock is not detected. When the bit is read as '1' a valid clock is detected.

5.16.4 FPGA CLKB/CLKA SRC SEL Bits 6, 2

Each of these bits selects the input source of one of the FPGA internal clocks, FPGA CLKA or CLKB depending on the bit selected. When the bit is cleared to logic '0' (its default state) the clock source is the associated CDC clock output, CDC CLKA or CDC CLKB. When the bit is set to logic '1' the clock source is the ADC1 clock output (DRY) for FPGA CLKA, or the DAC clock output (CLKO) for FPGA CLKB. (See illustration below.)

NOTE: Set FPGA CLKB to DAC clock output for DAC modes that involve interpolation or for time−packed modes.

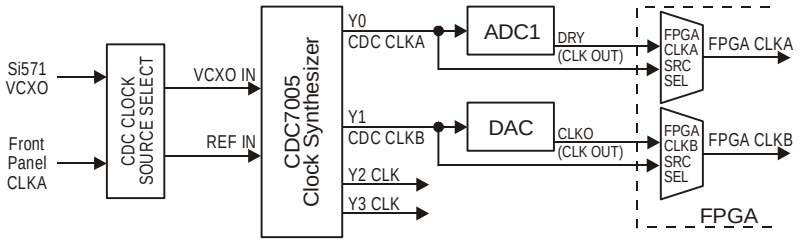


Figure 5–1: CDC/FPGA Clock Logic

5.16.5 FPGA CLKB/CLKA PWR DWN Bits 5, 1

Each of these bits allows the user to power down one of the FPGA clocks, either FPGA CLKA or CLKB depending on the bit. When this bit is cleared to logic '0' (its default state) the clock is operating. When the bit is set to logic '1' the clock output is powered down.

NOTE: Use this clock power down with caution to save power if the clock is not being used.

FPGA CLKA is used for all ADC channels data processing in the FPGA. If FPGA CLKA is powered down, all logic involved with ADC data movement will stop operating.
FPGA CLKB is used for DAC acquisition module data processing. If FPGA CLKB is powered down, all logic involved with DAC data movement will stop operating.

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5.17 Sync Bus Control Register 1

The Sync Bus Control Register 1 allows you to configure the Model 71620 as a Clock/Sync/Gate Master or Slave on the front panel Sync Bus, to select the sources of the Clock, Gate, and Sync output signals, and to control the CDC7005 Clock Generator inputs.

The following table shows the contents of this register. The subsections following the table provide descriptions of each register bit.

Table 5–20: Sync Bus Control Register 1
R/W @ BAR0+0x0402C

Bit	31 – 24							
Bit Name	Reserved							
Function	Write zeros, Mask when reading							
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Bit Name	SBUS SYNCB DRV INV	SBUS GATEB DRV INV	SBUS SYNCA DRV INV	SBUS GATEA DRV INV	Reserved	SBUS SYNCB DRV SRC	Reserved	SBUS GATEB DRV SRC
Function	0 = Normal 1 = Invert	0 = Normal 1 = Invert	0 = Normal 1 = Invert	0 = Normal 1 = Invert	Write zero, Mask read	0 = Sync B Register 1 = Sync Bus LVTTL Sync	Write zero, Mask read	0 = Gate B Register 1 = Sync Bus LVTTL Gate
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Bit Name	Reserved	SBUS SYNCA DRV SRC	Reserved	SBUS GATEA DRV SRC	Reserved	CLK SEL		
Function	Write zero, Mask read	0 = Sync A Register 1 = Sync Bus LVTTL Sync	Write zero, Mask read	0 = Gate A Register 1 = Sync Bus LVTTL Gate	Write zero, Mask read	See Section 5.17.9		
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	VCXO OUT DISABLE	Reserved				GATEB/ SYNCB MSTR	GATEA/ SYNCA MSTR	CLK MASTER EN
Function	0 = Enable 1 = Disable	Write zeros, Mask when reading				0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Disable 1 = Enable
All bits default to the logic '0' state at power on and reset								

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5.17 Sync Bus Control Register 1 (continued)

5.17.1 SBUS SYNCB DRV INV Bit 23

This bit inverts the LVPECL Sync B signal output to the Front Panel Sync Bus. When cleared to logic '0' (the default setting) the signal is not inverted. When set to logic '1' the signal is inverted.

5.17.2 SBUS GATEB DRV INV Bit 22

This bit inverts the LVPECL Gate B signal output to the Front Panel Sync Bus. When cleared to logic '0' (the default setting) the signal is not inverted. When set to logic '1' the signal is inverted.

5.17.3 SBUS SYNCA DRV INV Bit 21

This bit inverts the LVPECL Sync A signal output to the Front Panel Sync Bus. When cleared to logic '0' (the default setting) the signal is not inverted. When set to logic '1' the signal is inverted.

5.17.4 SBUS GATEA DRV INV Bit 20

This bit inverts the LVPECL Gate A signal output to the Front Panel Sync Bus. When cleared to logic '0' (the default setting) the signal is not inverted. When set to logic '1' the signal is inverted.

5.17.5 SBUS SYNCB DRV SRC Bit 18

This bit selects the source of the LVPECL Sync B signal output to the Front Panel Sync bus. When cleared to logic '0' (the default setting) the signal is from the Sync B Generate Register, Section 5.26. When set to logic '1' the signal is from the Sync Bus LVTTL Sync/PPS input, Section 2.7.4.

5.17.6 SBUS GATEB DRV SRC Bit 16

This bit selects the source of the LVPECL Gate B signal output to the Front Panel Sync bus. When cleared to logic '0' (the default setting) the signal is from the Gate B Generate Register, Section 5.24. When set to logic '1' the signal is from the Sync Bus LVTTL Gate/Trig input, Section 2.7.4.

5.17.7 SBUS SYNCA DRV SRC Bit 14

This bit selects the source of the LVPECL Sync A signal output to the Front Panel Sync bus. When cleared to logic '0' (the default setting) the signal is from the Sync A Generate Register, Section 5.25. When set to logic '1' the signal is from the Sync Bus LVTTL Sync/PPS input, Section 2.7.4.

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5.17 Sync Bus Control Register 1 (continued)

5.17.8 SBUS GATEA DRV SRC Bit 12

This bit selects the source of the LVPECL Gate A signal output to the Front Panel Sync bus. When cleared to logic '0' (the default setting) the signal is from the Gate A Generate Register, Section 5.23. When set to logic '1' the signal is from the Sync Bus LVTTL Gate/Trig input, Section 2.7.4.

5.17.9 CLK SEL Bits 10 – 8

These three bits select the source of the input signal for the CDC7005 clock and reference inputs (VCXO_IN and REF_IN, respectively). The settings for these three bits are:

Bits	Clocking Mode	CDC VCXO_IN Input	CDC REF_IN Input
000	VCXO genlocked to External Clock	VCXO	External Clock
001	VCXO genlocked to Sync Bus CLKA	VCXO	Front Panel Sync Bus CLKA
010	VCXO with no reference	VCXO	None
011	VCXO with no reference	VCXO	None
100	External Clock	External Clock	External Clock
101	Sync Bus CLKA	Front Panel Sync Bus CLKA	Front Panel Sync Bus CLKA
110	not used	None	None
111	not used	None	None

5.17.10 VCXO OUT DISABLE Bit 7

This bit enables or disables the frequency output of the Si571 VCXO. When cleared to logic '0' (the default setting) the VCXO output is enabled. When set to logic '1' the VCXO output is disabled.

NOTE: For best performance, the VCXO output should be disabled in Clocking Modes **100** and **101** (bits 10–8 above).

5.17.11 GATEB/SYNCB MSTR Bit 2

This bit sets the 71620 as the GateB/SyncB Master for the Front Panel Sync Bus. When this bit is cleared to logic '0' (its default state) the 71620 does not drive the GATEB and SYNCB signals out onto the front panel Sync Bus. When the bit is set to logic '1' this 71620 is the Bus Master and the board drives the GATEB and SYNCB signals out onto the front panel Sync Bus. When only one 71620 is used it must be set as the GateB/SyncB Master.

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5.17 Sync Bus Control Register 1 (continued)

5.17.12 GATEA/SYNCA MSTR Bit 1

This bit sets the 71620 as the GateA/SyncA Master for the Front Panel Sync Bus. When this bit is cleared to logic '0' (its default state) the 71620 does not drive the GATEA and SYNCA signals out onto the front panel Sync Bus. When the bit is set to logic '1' this 71620 is the Bus Master and the board drives the GATEA and SYNCA signals out onto the front panel Sync Bus. When only one 71620 is used it must be set as the GateA/SyncA Master.

5.17.13 CLK MASTER EN Bit 0

This bit sets the 71620 as the Clock Master for the Front Panel Sync Bus. When this bit is cleared to logic '0' (its default state) the 71620 does not drive the CLKA and CLKB signals out onto the front panel Sync Bus. When the bit is set to logic '1' this 71620 is the Clock Master and the board drives the CLKA and CLKB signals out onto the front panel Sync Bus. When only one 71620 is used it must be set as the Clock Master.

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5.18 Sync Bus Control Register 2

The Sync Bus Control Register 2 allows you to select the source and polarity of the Gate, Sync, and PPS input signals, and select the edge of these signals that will assert an interrupt.

The following table shows the contents of this register. The subsections following the table provide descriptions of each control bit in this register.

Table 5–21: Sync Bus Control Register 2
R/W @ BAR0+0x04030

Bit	31 – 28				27	26	25	24
Bit Name	Reserved				PPS B INT EDGE	SYNC B INT EDGE	GATE B INT EDGE	PPS A INT EDGE
Function	Write zeros, Mask when reading				0 = Start of pulse 1 = End of pulse			
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Bit Name	SYNC A INT EDGE	GATE A INT EDGE	PPS B RCV POL	SYNC B RCV POL	GATE B RCV POL	PPS A RCV POL	SYNC A RCV POL	GATE A RCV POL
Function	0 = Start of pulse 1 = End of pulse		0 = Active High 1 = Active Low					
Bit	**15 – 13**			**12 – 10**			**9 – 8**	
Bit Name	PPS B RCV SRC			SYNC B RCV SRC			GATE B RCV SRC	
Function	See Section 5.18.3			See Section 5.18.4			See Section 5.18.5	
Bit	**7 – 5**			**4 – 2**			**1 – 0**	
Bit Name	PPS A RCV SRC			SYNC A RCV SRC			GATE A RCV SRC	
Function	See Section 5.18.6			See Section 5.18.7			See Section 5.18.8	
All bits default to the logic '0' state at power on and reset								

5.18.1 PPS/SYNC/GATE A/B EDGE

Bits 27 to 22

Each of these bits selects the interrupting edge for one of the Sync Bus signals, either PPS B, SYNC B, GATE B, PPS A, SYNC A, or GATE A, depending on the bit selected. When the bit is cleared to logic '0' (its default state) the start of the signal asserts an interrupt to the Global Interrupt Status Register, Section 5.36. When the bit is set to logic '1' the end of the signal asserts this interrupt.

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5.18 Sync Bus Control Register 2 (continued)

5.18.2 PPS/SYNC/GATE A/B POL Bits 21 to 16

Each of these bits selects the polarity of one of the Sync Bus signals, either PPS B, SYNC B, GATE B, PPS A, SYNC A, or GATE A, depending on the bit selected. When the bit is cleared to logic '0' (its default state) the polarity is active high. When the bit is set to logic '1' the polarity is active low.

5.18.3 PPS B RCV SRC Bits 15 – 13

These three bits select the input source for the Sync Bus PPS B signal. The settings for these three bits are:

000	None (Off)
001	Front Panel LVTTL Sync/PPS input, Section 2.7.4
010	Front Panel LVPECL Sync B input, Section 2.7.4
011	Front Panel LVPECL Sync A input, Section 2.7.4
100	Rising edge of selected Gate B
101-111	None (Off)

5.18.4 SYNC B RCV SRC Bits 12 – 10

These three bits select the input source for the Sync Bus SYNC B signal. The settings for these three bits are:

000	None (Off)
001	Sync B Register, Section 5.26
010	Front Panel LVTTL Sync/PPS input, Section 2.7.4
011	Front Panel LVPECL Sync B input, Section 2.7.4
100	Rising edge of selected Gate B
101	Falling edge of selected Gate B
110-111	None (Off)

5.18.5 GATE B RCV SRC Bits 9 – 8

These two bits select the input source for the Sync Bus GATE B signal. The settings for these bits are:

00	None (Off)
01	Gate B Register, Section 5.24
10	Front Panel LVTTL Gate/Trig input, Section 2.7.4
11	Front Panel LVPECL Gate B input, Section 2.7.4

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5.18 Sync Bus Control Register 2 (continued)

5.18.6 PPS A RCV SRC Bits 7 – 5

These three bits select the input source for the Sync Bus PPS A signal. The settings for these three bits are:

000	None (Off)
001	Front Panel LVTTL Sync/PPS input, Section 2.7.4
010	Front Panel LVPECL Sync A input, Section 2.7.4
011	Front Panel LVPECL Sync B input, Section 2.7.4
100	Rising edge of selected Gate A
101-111	None (Off)

5.18.7 SYNC A RCV SRC Bits 4 – 2

These three bits select the input source for the Sync Bus SYNC A signal. The settings for these three bits are:

000	None (Off)
001	Sync A Register, Section 5.25
010	Front Panel LVTTL Sync/PPS input, Section 2.7.4
011	Front Panel LVPECL Sync A input, Section 2.7.4
100	Rising edge of selected Gate A
101	Falling edge of selected Gate A
110-111	None (Off)

5.18.8 GATE A RCV SRC Bits 1 – 0

These two bits select the input source for the Sync Bus GATE A signal. The settings for these bits are:

00	None (Off)
01	Gate A Register, Section 5.23
10	Front Panel LVTTL Gate/Trig input, Section 2.7.4
11	Front Panel LVPECL Gate A input, Section 2.7.4

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5.19 Sync Bus Input Delay Tap Control Register

The Sync Bus Input Delay Tap Control Register allows you to program a time delay up to 2.325 nanoseconds, in increments of 75 picoseconds, for the front panel Gate A, Sync A, Gate B, and Sync B input signals. This allows fine adjustment to timing to compensate for time losses in signal wiring connections.

The following table shows the contents of this register. The subsections following the table provide descriptions of each bit in this register.

Table 5–22: Sync Bus Input Delay Tap Control Register
R/W @ BAR0+0x04034

Bit	31 *	30 – 29	28 – 24
Bit Name	IODELAY CNTRL RDY	Reserved	SBUS SYNC B IN DLY [4:0]
Function	0 = Not Ready 1 = Ready	Write zeros, Mask read	Delay = N x 75 ps
Bit	**23 – 21**		**20 – 16**
Bit Name	Reserved		SBUS GATE B IN DLY [4:0]
Function	Write zeros, Mask read		Delay = N x 75 ps
Bit	**15 – 13**		**12 – 8**
Bit Name	Reserved		SBUS SYNC A IN DLY [4:0]
Function	Write zeros, Mask read		Delay = N x 75 ps
Bit	**7 – 5**		**4 – 0**
Bit Name	Reserved		SBUS GATE A IN DLY [4:0]
Function	Write zeros, Mask read		Delay = N x 75 ps

* Bit 31 is Read Only
Bits 30 – 0 default to the logic '0' state at power on and reset

5.19.1 IODELAY CNTRL RDY Bit 31

This read–only bit indicates the status of the delay controller. When read as logic '1' the delay controller for the front panel Sync Bus input is ready. When read as logic '0' the delay controller is not ready. This is a failure condition.

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5.19 Sync Bus Input Delay Tap Control Register (continued)

5.19.2 SBUS SYNC B/A IN DLY Bits 28–24/12–8

These bits specify the delay period for the applicable front panel input signal (Sync A or B, depending on the bits selected). The delay period is a 5–bit integer, with the least significant bit equal to 75 picoseconds.

To calculate the 5–bit register setting the formula is:

IN DLY = Desired Delay/75 where Desired Delay is in picoseconds

5.19.3 SBUS GATE B/A IN DLY Bits 20–16/4–0

These bits specify the delay period for the applicable front panel input signal (Gate A or B, depending on the bits selected). The delay period is a 5–bit integer, with the least significant bit equal to 75 picoseconds.

To calculate the 5–bit register setting the formula is:

IN DLY = Desired Delay/75 where Desired Delay is in picoseconds

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5.20 Sync Bus Input Delay Control Register

The Sync Bus Input Delay Control Register allows you to program a time delay of 1 to 3 clock cycles for the front panel Gate A, Sync A, Gate B, and Sync B input signals. This allows adjustment to timing to compensate for time losses in signal wiring connections.

The following table shows the contents of this register. The subsections following the table provide descriptions of each bit in this register.

Table 5–23: Sync Bus Input Delay Control Register
R/W @ BAR0+0x04038

Bit	31 – 8			
Bit Name	Reserved			
Function	Write zeros, Mask when reading			
Bit	**7 – 6**	**5 – 4**	**3 – 2**	**1 – 0**
Bit Name	SBUS SYNC B IN DLY	SBUS GATE B IN DLY	SBUS SYNC A IN DLY	SBUS GATE A IN DLY
Function	Delay = N x Clock Cycles	Delay = N x Clock Cycles	Delay = N x Clock Cycles	Delay = N x Clock Cycles
All bits default to the logic '0' state at power on and reset				

5.20.1 SBUS SYNC B/A IN DLY

Bits 7–6/3–2

These bits specify the delay period for the applicable front panel input signal (Sync A or B, depending on the bits selected). The delay period is a 2–bit integer, which indicates the number of clock cycles for the delay.

5.20.2 SBUS GATE B/A IN DLY

Bits 5–4/1–0

These bits specify the delay period for the applicable front panel input signal (Gate A or B, depending on the bits selected). The delay period is a 2–bit integer, which indicates the number of clock cycles for the delay.

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5.21 User LED Register

The User LED Register controls the Model 71620 front panel **USR** LED (and the PCB **D6** LED) when this register is selected by the USER LED SRC bits in the LED Control Register, and can generate a CDC7005 reset on a Model 71620 that is configured as a Clock Master, or on a 71620 that is not connected to an external Sync Bus.

The following table shows the contents of this register.

Table 5–24: User LED Register
R/W @ BAR0+0x0403C

Bit	31 – 1	0
Bit Name	Reserved	USER LED/ CDC RST
Function	Write zeros, Mask when reading	0 = Off 1 = On
Bit 0 defaults to the logic '1' state at power on and reset		

This register has two functions. It controls the user LEDs, and it generates a reset signal for the CDC7005.

- If the USER LED SRC bits in the LED Control Register, Section 5.22, are set to 00, the USER LED bit in this register turns on or off the **USR** LED on the 71620 front panel, Section 2.8.2, and the PCB **D6** LED, Section 2.4. If the USER LED SRC bits are set to any other value, this register has no affect on the **USR** LED.

- The CDC RST bit in this register generates the CLK B signal on a Model 71620 that is configured as a Clock Master, or on a 71620 that is not connected to an external Sync Bus. On a Model 71620 that is configured as a Clock Slave, the CLK B signal is input from an external Master. If the RST EN bit in the CDC Control/Status Register, Section 5.14, is set to enable, the CLK B signal resets the CDC7005.

  Toggle the CDC RST bit to 1, then back to 0 to perform the CDC7005 reset.

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5.22 LED Control Register

The LED Control Register controls several LEDs on the Model 71620 front panel.

The following table shows the contents of this register. The subsections following the table provide descriptions of each bit in this register.

Table 5–25: LED Control Register
R/W @ BAR0+0x04040

Bit	31 – 16							
Bit Name	Reserved							
Function	Write zeros, Mask when reading							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Bit Name	Reserved		CLK DET LED CTRL		ALM2 LED DISABLE	ALM1 LED DISABLE	ALM0 LED DISABLE	OT LED DISABLE
Function	Write zeros, Mask read		00 = CLKA or CLKB 01 = CLKA 10 = CLKB 11 = CLKA and CLKB		0 = TMP LED Active 1 = TMP LED Disabled for this alarm			
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	PPS LED SRC	PPS LED DISABLE	USER LED SRC		Reserved	SBUS B MSTR LED DISABLE	SBUS A MSTR LED DISABLE	CLK MSTR LED DISABLE
Function	0 = PPS A 1 = PPS B	0 = Active 1 = Disabled	00 = User LED Register 01 = PCIe activity 10 = User application 11 = PCIe interrupt		Write zero, Mask read	0 = MAS LED Active 1 = MAS LED Disabled for this condition		
All bits default to the logic '0' state at power on and reset								

5.22.1 CLK DET LED CTRL Bits 13 – 12

These two bits select the source condition for the front panel **CLK** LED, Section 2.8.6. This LED illuminates when:

00 Either CLKA or CLKB are locked and detected
01 CLKA is locked and detected
10 CLKB is locked and detected
11 Both CLKA and CLKB are locked and detected

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5.22 LED Control Register (continued)

5.22.2 ALMn/OT LED DISABLE Bits 11 to 8

Each of these bits enables or disables the front panel **TMP** LED, Section 2.8.5, in response to the associated FPGA System Monitor alarm signal, either ALM2, ALM1, ALM0, or OT, depending on the bit selected. Note that each alarm signal also can assert an interrupt to the Global Interrupt Status Register, Section 5.36.

When a bit is cleared to logic '0' (its default state) the **TMP** LED will illuminate when the associated FPGA System Monitor alarm signal is active. When a bit is set to logic '1' the **TMP** LED is disabled for that FPGA alarm signal.

See Section 3.7.1 for System Monitor operation.

5.22.3 PPS LED SRC Bit 7

This bit specifies the signal source for the **PPS** LED, Section 2.8.4. When this bit is cleared to logic '0' (its default state) the **PPS** LED is driven by an event on PPS A. When the bit is set to logic '1' the **PPS** LED is driven by an event on PPS B.

5.22.4 PPS LED DISABLE Bit 6

This bit enables or disables the front panel **PPS** LED, Section 2.8.4. When this bit is cleared to logic '0' (its default state) the **PPS** LED is active and is driven by an event on PPS A or B, depending on the setting of Bit 9, PPS LED SRC, above. When the bit is set to logic '1' the **PPS** LED is disabled.

5.22.5 USER LED SRC Bits 5 – 4

These two bits select the signal source for the front panel **USR** LED on the 71620 front panel, Section 2.8.2, and the PCB **D6** LED, Section 2.4. The **USR** LED is driven by:

- **00** User LED Register, Section 5.21
- **01** PCIe activity
- **10** User application input signal
- **11** PCIe interrupt

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5.22 LED Control Register (continued)

5.22.6 xxx MSTR LED DISABLE Bits 2 – 0

Each of these bits enables or disables the front panel **MAS** LED, Section 2.8.3, in response to the associated Sync Bus signal enabled as Master in the Sync Bus Control Register 1, either SBUS B, SBUS A, or CLK, depending on the bit selected. Note that each of these six bits is in the same bit position as the associated Master enable bits in Sync Bus Control Register 1, Section 5.17.

When a bit is cleared to logic '0' (its default state) the **MAS** LED is active and will illuminate when any one of the associated Sync Bus signals is set to Master. When a bit is set to logic '1' the **MAS** LED is disabled for that Sync Bus signal setting.

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5.23 Gate A Generate Register

The Gate A Generate Register generates the GATE A signal on a Model 71620 that is configured as a SyncA/GateA Master, or on a 71620 that is not connected to an external Sync Bus. Refer to Section 3.5.1 for additional information about operation of the GATE signals. The following table shows the contents of this register.

Table 5–26: Gate A Generate Register
R/W @ BAR0+0x04044

Bit	31 – 1	0
Bit Name	Reserved	GATE A
Function	Write zeros, Mask when reading	0 = Inactive 1 = Active
Bit 0 defaults to the logic '1' state at power on and reset		

When the gate source is set to the onboard register (SBUS GATEA DRV SRC = 00, Sync Bus Control Register 1, Section 5.17), the GATE bit in this register creates the gate signal (GATE A) for the board, and for output to the Front Panel Sync Bus. GATE A is used to control writing to the ADC PACK FIFOs.

5.24 Gate B Generate Register

The Gate B Generate Register generates the GATE B signal on a Model 71620 that is configured as a Sync B/Gate B Master, or on a 71620 that is not connected to an external Sync Bus. Refer to Section 3.5.1 for additional information about operation of the GATE signals. The following table shows the contents of this register.

Table 5–27: Gate B Generate Register
R/W @ BAR0+0x04048

Bit	31 – 1	0
Bit Name	Reserved	GATE B
Function	Write zeros, Mask when reading	0 = Inactive 1 = Active
Bit 0 defaults to the logic '1' state at power on and reset		

When the gate source is set to the onboard register (SBUS GATEB DRV SRC = 00, Sync Bus Control Register 1, Section 5.17), the GATE bit in this register creates the gate signal (GATE B) for the board, and for output to the Front Panel Sync Bus. GATE B is used to control writing to the DAC FIFO.

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5.25 Sync A Generate Register

The Sync A Generate Register generates the SYNC A signal on a Model 71620 that is configured as a SyncA/GateA Master, or on a 71620 that is not connected to an external Sync Bus. Refer to Section 3.5.2 for additional information about operation of the SYNC signals. The following table shows the contents of this register.

Table 5–28: Sync A Generate Register
R/W @ BAR0+0x0404C

Bit	31 – 1	0
Bit Name	Reserved	SYNC A
Function	Write zeros, Mask when reading	0 = Inactive 1 = Active
Bit 0 defaults to the logic '1' state at power on and reset		

When the sync source is set to the onboard register (SBUS SYNCA DRV SRC = 00, Sync Bus Control Register 1, Section 5.17), the SYNC bit in this register creates the sync signal (SYNC A) for the board, and for output to the Front Panel Sync Bus.

SYNC A signal is used for the following functions on the 71620:

- Timestamp Counters Reset, Section 5.27
- Test Signal A Reset, Section 5.27
- ADC Data Rate Monitor Reset, Section 6.20

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5.26 Sync B Generate Register

The Sync B Generate Register generates the SYNC B signal on a Model 71620 that is configured as a Sync B/Gate B Master, or on a 71620 that is not connected to an external Sync Bus. Refer to Section 3.5.2 for additional information about operation of the SYNC signals. The following table shows the contents of this register.

Table 5–29: Sync B Generate Register
R/W @ BAR0+0x04050

Bit	31 – 1	0
Bit Name	Reserved	SYNC B
Function	Write zeros, Mask when reading	0 = Inactive 1 = Active
Bit 0 defaults to the logic '1' state at power on and reset		

When the sync source is set to the onboard register (SBUS SYNCB DRV SRC = 00, Sync Bus Control Register 1, Section 5.17), the SYNC bit in this register creates the sync signal (SYNC B) for the board, and for output to the Front Panel Sync Bus.

SYNC B signal is used for the following functions on the 71620:

- Test Signal B Reset, Section 5.27
- DAC5688 SYNC input, Section 7.4
- DAC Data Rate Monitor Reset, Section 7.21

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5.27 Test Signal and Timestamp Control Register

The Test Signal and Timestamp Control Register controls the reset of several devices in the FPGA.

The following table shows the contents of this register. The subsections following the table describe each bit in this register.

Table 5–30: Test Signal and Timestamp Control Register
R/W @ BAR0+0x04054

Bit	31 – 12					11 – 8		
Bit Name	Reserved					Factory Use Only		
Function	Write zeros, Mask when reading					DO NOT CHANGE *		
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	TS STRT TIME LOAD	TS PPS SIG EN	TS SYNC A RST EN	TS MODULE RST	SYS MON RST	TEST SIG SYNCB RST EN	TEST SIG SYNCA RST EN	TEST SIG RST
Function	0 = Inactive 1 = Load	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Run 1 = Reset	0 = Run 1 = Reset	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Run 1 = Reset

All bits default to the logic '0' state at power on and reset.
* Bits 11–8 are reserved for Pentek factory use only and should not be changed.

5.27.1 TS START TIME LOAD Bit 7

This bit is the Timestamp Time load control bit. When the bit is toggled to logic '1', the value in the Timestamp Start Time Register, Section 5.30, is loaded into the timestamp PPS counter. The time stamp counter will not operate until it is again deasserted.

This may be used to initialize the timestamp counter to a time standard such as the number of seconds since 00:00:00 on January 1, 1970.

5.27.2 TS PPS SIG EN Bit 6

This bit enables the PPS counter in the Timestamp module. Clear the bit to logic '0' (its default state) to disable the reset; the PPS signal is ignored and only the clock cycle counter is active. Set the bit to logic '1' to enable the PPS counter; the PPS signal is enabled to increment the PPS counter and reset the clock cycle counter.

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5.27 Test Signal and Timestamp Control Register (continued)

5.27.3 TS SYNCA RST EN Bit 5

This bit enables the reset of the Timestamp module counters using the SYNC A signal. Clear the bit to logic '0' (its default state) to disable the reset from SYNC A. Set the bit to logic '1' to enable SYNC A to reset the Timestamp module counters.

5.27.4 TS MODULE RST Bit 4

This bit resets the Timestamp module and flushes all four Timestamp FIFOs. Set the bit to logic '1' to reset the Timestamp module. Clear the bit to logic '0' (its default state) to return the Timestamp module to normal operation.

5.27.5 SYS MON RST Bit 3

This bit resets the FPGA System Monitor. Set the bit to logic '1' to reset the System Monitor. Clear the bit to logic '0' (its default state) to return the Sys–tem Monitor to normal operation.

5.27.6 TEST SIG SYNCB RST EN Bit 2

This bit enables the reset of the test signal associated with FPGA CLKB (Test Sine B, Section 5.29) using the SYNC B signal. Clear the bit to logic '0' (its default state) to disable the reset from SYNC B. Set the bit to logic '1' to enable SYNC B to reset the test signal associated with FPGA CLKB.

5.27.7 TEST SIG SYNCA RST EN Bit 1

This bit enables the reset of the test signal associated with FPGA CLKA (Test Sine A, Section 5.28) using the SYNC A signal. Clear the bit to logic '0' (its default state) to disable the reset from SYNC A. Set the bit to logic '1' to enable SYNC A to reset the test signal associated with FPGA CLKA.

5.27.8 TEST SIG RST Bit 0

This bit resets the Test Signal module (resets both A and B). Set the bit to logic '1' to reset the Test Signal module. Clear the bit to logic '0' (its default state) to return the Test Signal module to normal operation.

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5.28 Test Sine A Frequency Control Register

The Test Sine A Frequency Control Register determines the frequency of the Test Signal for the ADC input acquisition modules (see Section 3.2). The following table shows the contents of this register.

Table 5–31: Test Sine A Frequency Control Register
R/W @ BAR0+0x04058

Bit	31 – 0
Bit Name	PHS INC
Function	Test Signal Phase Increment
All bits default to the logic '0' state at power on and reset	

The Test Signal Phase Increment is a 32–bit binary value. It is used to increment the Test Signal according to the following formula:

$$\text{Frequency} = \text{CLKA_FREQ} \times (\text{PHS INC} / 2^{32})$$

Where CLKA is the FPGA CLKA (selected by FPGA CLKA SRC SEL, Section 5.16.4).

5.29 Test Sine B Frequency Control Register

The Test Sine B Frequency Control Register determines the frequency of the Test Signal for the DAC output module (see Section 3.3). The following table shows the contents of this register.

Table 5–32: Test Sine B Frequency Control Register
R/W @ BAR0+0x0405C

Bit	31 – 0
Bit Name	PHS INC
Function	Test Signal Phase Increment
All bits default to the logic '0' state at power on and reset	

The Test Signal Phase Increment is a 32–bit binary value. It is used to increment the Test Signal according to the following formula:

$$\text{Frequency} = \text{CLKB_FREQ} \times (\text{PHS INC} / 2^{32})$$

Where CLKB is the FPGA CLKB (selected by FPGA CLKB SRC SEL, Section 5.16.4).

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5.30 Timestamp Start Time Register

The write–only Timestamp Start Time Register determines the start time for the Time–stamp Module.

The following table shows the contents of this register.

Table 5–33: Timestamp Start Time Register
WO @ BAR0+0x04060

Bit	31 – 0
Bit Name	SECONDS
Function	Initial Number of Seconds
All bits default to the logic '0' state at power on and reset	

SECONDS is a 32–bit binary value that specifies the number of seconds to initialize the timestamp PPS counter to. Use the TS STRT TIME LOAD control bit in the Test Signal and Timestamp Control Register, Section 5.27, to load this value into the counter.

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5.31 TWSI Port 1 Control/Status Register

The TWSI Port 1 Control/Status Register and the associated TWSI Port 1 Data Register, Section 5.32, allow you to program the 71620 voltage/temperature sensor thresholds and the internal Si571 VCXO clock frequency over the board's serial TWSI (Two–Wire Serial Interface) Port 1. The Control/Status Register, below, contains control and status bits for TWSI Port 1, and the Data Register, Section 5.32, provides the data bits.

NOTE: This interface is identified as I^2C, SMBus, or TWSI bus in different vendors' literature. Pentek refers to this as the TWSI bus in this manual.

The following table shows the contents of this register. The subsections following the table provide descriptions of each bit in this register.

Table 5–34: TWSI Port 1 Control/Status Register
R/W @ BAR0+0x04064

Bit	31 – 29			28 – 24 *				
Bit Name	Reserved			RX FIFO CNT[4:0]				
Function	Write zeros, Mask when reading			Number of Bytes Received				
Bit	**23**	**22 ***	**21 ***	**20**	**19**	**18 ***	**17 ***	**16 ***
Bit Name	Reserved	RX FIFO FULL	RX FIFO EMPTY	Reserved		TX FIFO FULL	TX FIFO EMPTY	TRNSFR BUSY
Function	Write zero, Mask read	0 = Not Full 1 = Full	0 = Not Empt 1 = Empty	Write zero, Mask read		0 = Not Full 1 = Full	0 = Not Empt 1 = Empty	0 = Complete 1 = Busy
Bit	**15**	**14 – 8**						
Bit Name	Reserved	TWSI ADDR[6:0]						
Function	Write zero, Mask read	TWSI Bus Device Address						
Bit	**7**	**6**	**5**	**4**	**3 – 0**			
Bit Name	START TRNSFR	Reserved	DATA DIR	PORT ENABLE	NUM BYTES[3:0]			
Function	0 = Run 1 = Start	Write zero, Mask read	0 = Write 1 = Read	0 = Disable 1 = Enable	Number of Bytes to Transfer - 1			

* These bits are read–only
Bits 14 – 0 default to the logic '0' state at power on and reset.

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5.31 TWSI Port 1 Control/Status Register (continued)

5.31.1 RX FIFO CNT[4:0] Bits 28 – 24

These read–only bits indicate the number of bytes received for a TWSI Port 1 read operation.

5.31.2 RX FIFO FULL Bit 22

This read–only bit indicates the status of the TWSI Port 1 Receive FIFO. The Receive FIFO buffers data bytes from the device after you start a transfer until you are ready to read them using the TWSI Port 1 Data Register, Section 5.32. When read as logic '1' the FIFO FULL flag is active (true). When read as logic '0' the FIFO FULL flag is inactive.

5.31.3 RX FIFO EMPTY Bit 21

This read–only bit indicates the status of the TWSI Port 1 Receive FIFO. When read as logic '1' the FIFO EMPTY flag is active (true). When read as logic '0' the FIFO EMPTY flag is inactive.

5.31.4 TX FIFO FULL Bit 18

This read–only bit indicates the status of the TWSI Port 1 Transmit FIFO. The Transmit FIFO buffers data bytes that you have written using the TWSI Port 1 Data Register, Section 5.32, until you start the transfer. When read as logic '1' the FIFO FULL flag is active (true). When read as logic '0' the FIFO FULL flag is inactive.

5.31.5 TX FIFO EMPTY Bit 17

This read–only bit indicates the status of the TWSI Port 1 Transmit FIFO. When read as logic '1' the FIFO EMPTY flag is active (true). When read as logic '0' the FIFO EMPTY flag is inactive.

5.31.6 TRNSFR BUSY Bit 16

This read–only bit indicates the status of the TWSI Port 1 transfer. When read as logic '0' the transfer is complete. When read as logic '1' the transfer is still in progress (busy).

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5.31 TWSI Port 1 Control/Status Register (continued)

5.31.7 TWSI ADDR[6:0] Bits 14 – 8

These seven bits specify the bus address of the device on TWSI Bus 1. Each device on the TWSI bus has a separate bus address, as listed in the following table. Refer to the subsections identified in this table for device programming information.

Table 5–35: TWSI Port 1 Bus Addresses

Device	Address *	Information
Main PCB LM83 Temperature Sensor	**0011000h**	Section 5.32.1
Front Panel Module LM83 Temperature Sensor	**0011001h**	Section 5.32.2
Memory Module A/B LM73 Temperature Sensor	**1001000h**	Section 5.32.3
Memory Module C/D LM73 Temperature Sensor	**1001001h**	
Si571 Programmable VCXO	**1100000h**	Section 5.32.4

* The TWSI bus addresses are 7–bit serial bus address, followed by the bus R/W bit **h**: 0 = Write, 1 = Read

5.31.8 START TRNSFR Bit 7

This bit initiates a TWSI bus 1 transfer. When you change this bit from '0' to '1', the TWSI controller generates a START. See next page for the read/write sequence description.

5.31.9 DATA DIR Bit 5

This bit specifies the direction of a TWSI bus 1 transfer. Clear the bit to logic '0' (its default state) to set the transfer to Write (to the addressed device). Set the bit to logic '1' to set the transfer to Read (from the addressed device).

5.31.10 PORT ENABLE Bit 4

This bit enables or disables TWSI Port 1. When this bit is cleared to logic '0' (its default state) the Port is disabled, the output is tri–state, and the logic is reset. When the bit is set to logic '1' the Port is enabled for a transfer.

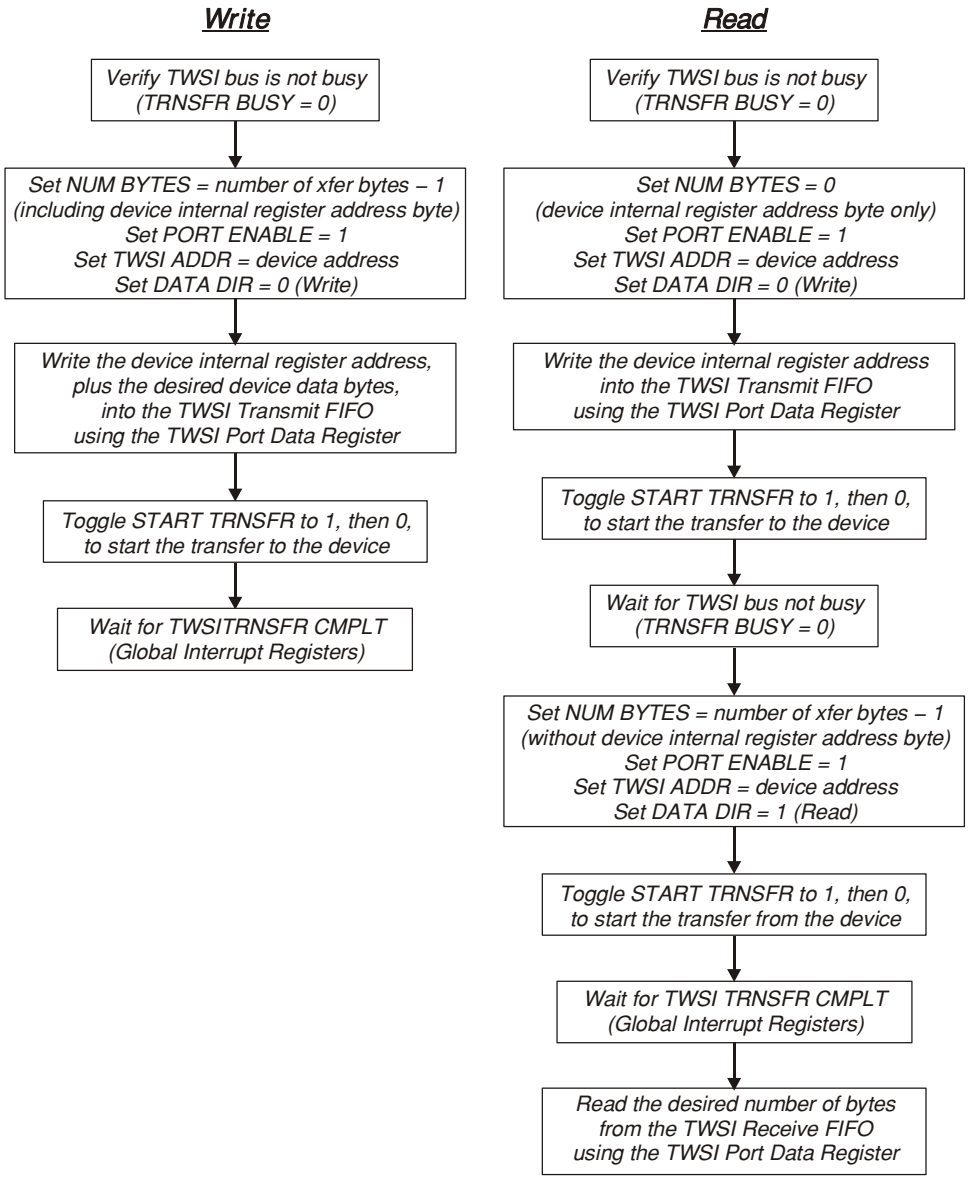
5.31.11 NUM BYTES[3:0] Bits 3 – 0

These bits specify the number of bytes to transfer. This must be set to the number of bytes desired minus 1.

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5.31 TWSI Port 1 Control/Status Register (continued)

The following steps illustrate the sequences required for writing to or reading from any device on the TWSI Port 1 bus. Note that each device on TSWI Port 1 has subaddresses that access internal register on each device. Thus, the read/write sequence requires writing this subaddress first, before the read/write of the data bytes.



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5.32 TWSI Port 1 Data Register

The TWSI Port 1 Data Register provides the data bits to program the 71620 voltage/ temperature sensor thresholds and the internal Si571 VCXO clock frequency over the board's serial TWSI Port 1.

NOTE: This interface is identified as I^2C, SMBus, or TWSI bus in different vendors' literature. Pentek refers to this as the TWSI bus in this manual.

The following table shows this register's bit layout. The paragraphs following this table describe these bits.

Table 5–36: TWSI Port 1 Data Register
R/W @ BAR0+0x04068

Bit	31 – 16							
Bit Name	Reserved							
Function	Write zeros, Mask when reading							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
Function	When DATA DIRECTION = 0, data to write to TWSI Port 1. When DATA DIRECTION = 1, data read from TWSI Port 1.							
All bits default to the logic '0' state at power on and reset								

NOTE: You must set up the TWSI bus devices following power on of the Model 71620. The following paragraphs describe the setup of these devices. Routines for programming these devices are provided in the ReadyFlow board support software for the Model 71620 (Pentek part #801.71620).

The devices on the TWSI bus 1 include a National Semiconductor LM83 Temperature Sensor located on the main 71600 PCB, a National Semiconductor LM83 Temperature Sensor located on the front panel PCB, a National Semiconductor LM73 Temperature Sensor located on each (optional) memory module PCB, and a Silicon Labs Si571 VCXO. You can program these devices from the TWSI Port 1 Register, using internal registers in each device, as described in the following paragraphs.

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5.32 TWSI Port 1 Data Register (continued)

When any of the following sensor inputs exceeds the high setpoint limit, the front panel red **TMP** LED (Section 2.8.5) is illuminated, and an interrupt is asserted to bit 9 in the Global Interrupt Status Register, Section 5.36.

5.32.1 Main PCB LM83 Temperature Sensor

There are several temperature sensors in the LM83 that can be programmed on the serial TWSI bus, using LM83 internal registers (refer to the National Semiconductor LM83 datasheet (see Section 1.13) for description of these registers). The following table lists the programmable sensors on the LM83:

Table 5–37: Main PCB LM83 Programmable Sensors

Monitored Condition	LM83 Input	ReadyFlow Limits *
FPGA Temperature	1	100° C
PCB Rear Power Supplies	2	60° C
PCB Front Power Supplies	3	60° C
LM83 Local	(internal)	50° C

* These limits are programmed if you run the Pentek ReadyFlow 71620 Hardware Monitor routines for the LM83 using the default values.

When any of the four inputs exceeds the HIGH setpoint limit, a red LED on the main 71620 PCB (Section 2.4) is illuminated.

5.32.2 Front Panel Module LM83 Temperature Sensor

There are several temperature sensors in the LM83 that can be programmed on the serial TWSI bus, using LM83 internal registers (refer to the National Semiconductor LM83 datasheet (see Section 1.13) for description of these registers). The following table lists the programmable sensors on the LM83:

Table 5–38: Front Panel PCB LM83 Programmable Sensors

Monitored Condition	LM83 Input	ReadyFlow Limits *
Near ADC 1 and ADC 2	1	85° C
Near ADC3	2	85° C
Near DAC	3	85° C
LM83 Local	(internal)	85° C

* These limits are programmed if you run the Pentek ReadyFlow 71620 Hardware Monitor routines for the LM83 using the default values.

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5.32 TWSI Port 1 Data Register (continued)

5.32.3 Memory Module LM73 Temperature Sensors

Each optional memory module has a single LM73 temperature sensor that can be programmed on the serial TWSI bus, using LM73 internal registers (refer to the National Semiconductor LM73 datasheet (see Section 1.13) for description of these registers).

5.32.4 Si571 Programmable VCXO

The Silicon Labs Si571 programmable Any−Rate VCXO generates the on−board clock for the CDC7005 Clock Synthesizer. The Si571 output frequency is determined by programming the oscillator frequency and the output dividers using onboard registers. Refer to the Silicon Labs Si571 datasheet (see Section 1.13) for Si571 programming information.

CAUTION

Take care that the ADC clock output from the CDC7005 never exceeds the ADS5485's rated clock speed during any change of frequency with the VCXO and/or the CDC7005.

– If you are increasing the VCXO frequency, first reprogram the appropriate CDC divider so that the ADS5485 clock does not exceed 200 MHz.

– If you are decreasing the VCXO frequency, do not reprogram the CDC divider until the VCXO has been reprogrammed so that the ADS5485 clock does not exceed 200 MHz.

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5.33 TWSI Port 2 Control/Status Register

The TWSI Port 2 Control/Status Register and the associated TWSI Port 2 Data Register, Section 5.34, allow you to program the XMC interface I^2C port and the on–board serial EEPROM using the 71620's serial TWSI (Two–Wire Serial Interface) Port 2. The Con–trol/Status Register, below, contains control and status bits for TWSI bus 2, and the Data Register, Section 5.34, provides the data bits.

NOTE: This interface is identified as I^2C, SMBus, or TWSI bus in vendors' literature. Pentek refers to this as the TWSI bus in this manual.

The following table shows the contents of this register. The subsections following the table provide descriptions of each bit in this register.

Table 5–39: TWSI Port 2 Control/Status Register
R/W @ BAR0+0x0406C

Bit	31 *	30 *	29 *	28 – 24 *				
Bit Name	MGA[2:0]			RX FIFO CNT[4:0]				
Function	Geographical Address			Number of Bytes Received				
Bit	23	22 *	21 *	20	19	18 *	17 *	16 *
Bit Name	Reserved	RX FIFO FULL	RX FIFO EMPTY	Reserved		TX FIFO FULL	TX FIFO EMPTY	TRNSFR BUSY
Function	Write zero, Mask read	0 = Not Full 1 = Full	0 = Not Empt 1 = Empty	Write zero, Mask read		0 = Not Full 1 = Full	0 = Not Empt 1 = Empty	0 = Complete 1 = Busy
Bit	15	14 – 8						
Bit Name	Reserved	TWSI ADDR[6:0]						
Function	Write zero, Mask read	TWSI Bus Device Address						
Bit	7	6	5	4	3 – 0			
Bit Name	START TRNSFR	Reserved	DATA DIR	PORT ENABLE	NUM BYTES[3:0]			
Function	0 = Run 1 = Start	Write zero, Mask read	0 = Write 1 = Read	0 = Disable 1 = Enable	Number of Bytes to Transfer - 1			

* These bits are Read Only.
Bits 14 – 0 default to the logic '0' state at power on and reset.

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5.33 TWSI Port 2 Control/Status Register (continued)

5.33.1 MGA[2:0] Bits 31 – 29

These read–only bits indicate the geographical address for the EEPROM on the XMC interface connected to TWSI Port 2. The EEPROM A2, A1, and A0 address bits are tied to the XMC connector geographical address MGA[2:0] bits.

5.33.2 RX FIFO CNT[4:0] Bits 28 – 24

These read–only bits indicate the number of bytes received for a TWSI Port 2 read operation.

5.33.3 RX FIFO FULL Bit 22

This read–only bit indicates the status of the TWSI Port 2 Receive FIFO. The Receive FIFO buffers data bytes from the device after you start a transfer until you are ready to read them using the TWSI Port 2 Data Register, Section 5.34. When read as logic '1' the FIFO FULL flag is active (true). When read as logic '0' the FIFO FULL flag is inactive.

5.33.4 RX FIFO EMPTY Bit 21

This read–only bit indicates the status of the TWSI Port 2 Receive FIFO. When read as logic '1' the FIFO EMPTY flag is active (true). When read as logic '0' the FIFO EMPTY flag is inactive.

5.33.5 TX FIFO FULL Bit 18

This read–only bit indicates the status of the TWSI Port 2 Transmit FIFO. The Transmit FIFO buffers data bytes that you have written using the TWSI Port 2 Data Register, Section 5.34, until you start the transfer. When read as logic '1' the FIFO FULL flag is active (true). When read as logic '0' the FIFO FULL flag is inactive.

5.33.6 TX FIFO EMPTY Bit 17

This read–only bit indicates the status of the TWSI Port 2 Transmit FIFO. When read as logic '1' the FIFO EMPTY flag is active (true). When read as logic '0' the FIFO EMPTY flag is inactive.

5.33.7 TRNSFR BUSY Bit 16

This read–only bit indicates the status of the TWSI Port 2 transfer. When read as logic '0' the transfer is complete. When read as logic '1' the transfer is still in progress (busy).

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5.33 TWSI Port 2 Control/Status Register (continued)

5.33.8 TWSI ADDR[6:0] Bits 14 – 8

These seven bits specify the bus address of the device on TWSI Bus 2. The 71620 TWSI Port 2 lines are connected to the XMC connector I^2C serial data and I^2C serial clock pins. This allows the user to address any I^2C devices on or connected to the XMC baseboard or carrier that have access to these pins.

A Serial EEPROM is connected to this XMC I^2C interface at TWSI address **0xAn** (binary address **0b1010nnn**), where the last three digits '**nnn**' are determined by the XMC module's GA[0:2} inputs, which are connected from the XMC connector **MGAn** pins (reported in bits 31–29, Section 5.33.1). Refer to Section 5.34.1 for description of this EEPROM.

5.33.9 START TRNSFR Bit 7

This bit initiates a TWSI bus 2 transfer. When you change this bit from '0' to '1', the TWSI controller generates a START. See next page for the read/write sequence description.

5.33.10 DATA DIR Bit 5

This bit specifies the direction of a TWSI bus 2 transfer. Clear the bit to logic '0' (its default state) to set the transfer to Write (to the specified device). Set the bit to logic '1' to set the transfer to Read (from the specified device).

5.33.11 PORT ENABLE Bit 4

This bit enables or disables TWSI Port 2. When this bit is cleared to logic '0' (its default state) the Port is disabled, the output is tri–state, and the logic is reset. When the bit is set to logic '1' the Port is enabled for a transfer.

5.33.12 NUM BYTES[3:0] Bits 3 – 0

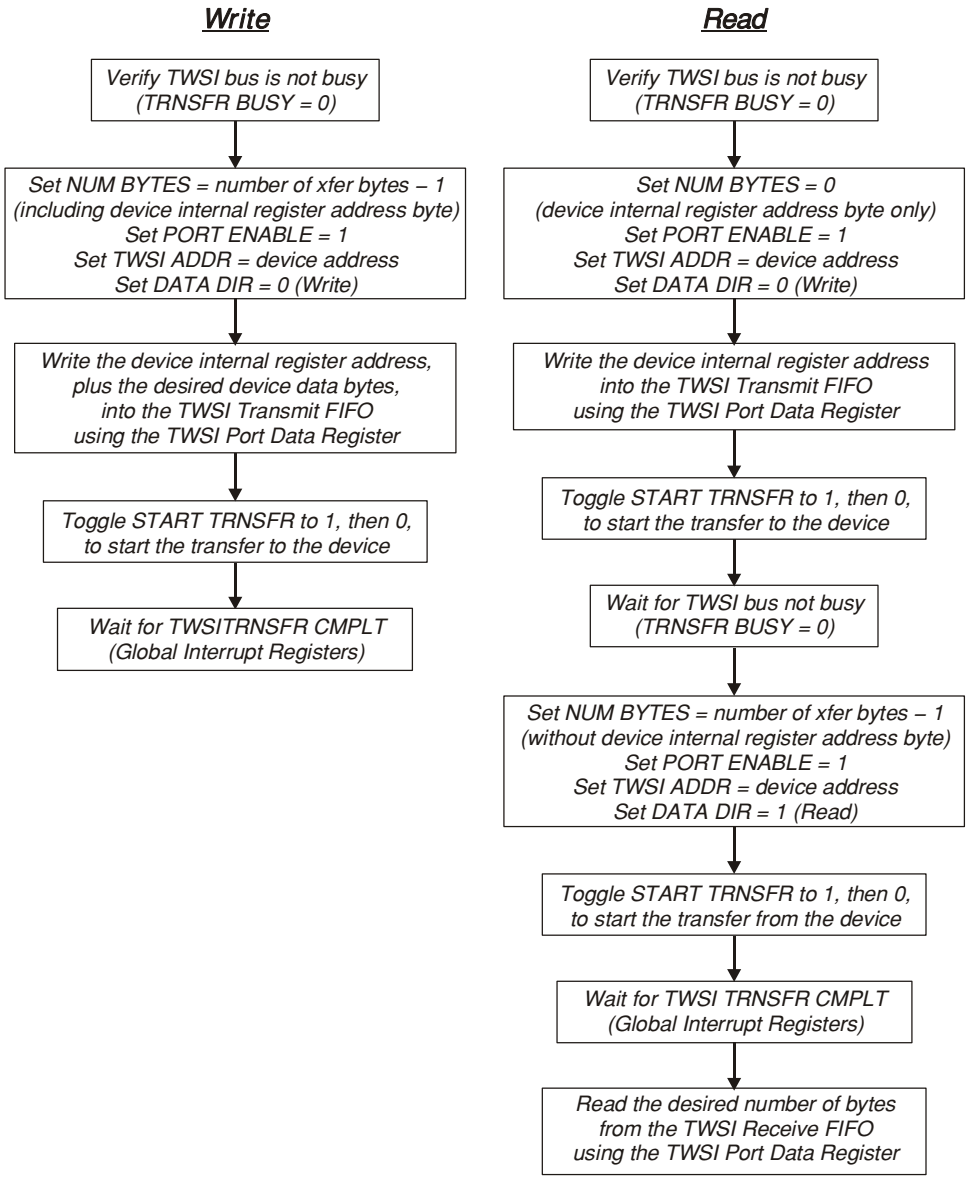
These bits specify the number of bytes to transfer. This must be set to the number of bytes desired minus 1.

NOTE: When accessing the Serial EEPROM, the number of bytes must be set to one more, or to the actual number of bytes desired to be transferred.

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5.33 TWSI Port 2 Control/Status Register (continued)

The following steps illustrate the sequences required for writing to or reading from any device on the TWSI Port 2 bus. Note that each device on TSWI Port 2 has subaddresses that access internal register on each device. Thus, the read/write sequence requires writing this subaddress first, before the read/write of the data bytes.



NOTE: When accessing the Serial EEPROM, NUM BYTES must be set to the actual number of bytes to be transferred (do not subtract 1).

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5.34 TWSI Port 2 Data Register

The TWSI Port 2 Data Register provides the data bits to program the XMC interface I^2C port using the board's serial TWSI Port 2.

The following table shows this register's bit layout. The paragraphs following this table describe these bits.

Table 5–40: TWSI Port 2 Data Register
R/W @ BAR0+0x04070

Bit	31 – 16							
Bit Name	Reserved							
Function	Write zeros, Mask when reading							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
Function	When DATA DIRECTION = 0, data to write to TWSI Port 2. When DATA DIRECTION = 1, data read from TWSI Port 2.							
All bits default to the logic '0' state at power on and reset								

The 71620 TWSI Port 2 lines are connected to the XMC connector **MSDA** (I^2C serial data) and **MSCL** (I^2C serial clock) pins. This allows the user to communicate with any I^2C devices on or connected to the XMC baseboard or carrier that have access to these pins. (Refer to the VITA XMC standard 42.0 for further description of this interface.)

A Serial EEPROM is connected to this XMC interface at TWSI address **`0xAn`** (binary address **`0b1010nnn`**). The last three bits of the EEPROM TWSI address (**`nnn`**) are determined by the XMC GA[0:2} inputs, from the **MGAn** pins, Section 5.33.1. The serial EEPROM is used for the Cobalt board identification, as described in Section 5.34.1 on the next page, and it's MGA address is set to binary 000.

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5.34 TWSI Port 2 Data Register (continued)

5.34.1 Cobalt Serial EEPROM

The serial EEPROM is programmed at the factory to identify the Cobalt Model number of the board and all Options installed by Pentek. To read this EEPROM, use binary **1010000** as the TWSI address, Section 5.33.8, in the TWSI Port 2 Control/Status Register.

NOTE: This Cobalt Model identification feature is available only on 71620 boards shipped in June 2011 or later.

The contents of the EEPROM are shown in the following two tables, organized as 32−bit words. Table 5−41 on page 159 shows the contents in the original format; Table 5−42 on page 160 shows the contents in the new format used in boards shipped in November 2011 and later. ReadyFlow board support software for the Model 71620 supports both formats.

- In the New Format (Table 5−42), the first 32 32−bit words (addresses **0x0000** to **0x00FF**) contain XMC and PCIe information as defined by the ANSI/VITA 42.0−2008 and ANSI/VITA 42.3−2006 standards.
- The next word in the New Format (Table 5−42), and the first word in the Old Format (Table 5−41), is a valid data flag (**0x00EECODE**).
- Following the valid data word is the Cobalt board model number (71620 illustrated in table).
- Next are words containing the PCB number, revision, and options for the main PCB module, for the front end I/O module, and for each memory module installed on your product. Where options are not installed, the 16−bit Option field is set to **0xFFFF**.
- If you have ordered a Cobalt assembly on a Pentek−supplied PCIe or VPX carrier (such as a Model 78620 PCIe board or Model 53620 VPX board) the next three 32−bit words identify the carrier PCB number, revision, and options for the carrier.
- The last word is a checksum of all 32−bit words, calculated by Pentek.

CAUTION

Do Not write to this EEPROM.

The contents of the serial EEPROM are programmed by Pentek to identify the model of the board and all options installed by Pentek.

If you write to the EEPROM you risk destroying this information.

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5.34 TWSI Port 2 Data Register (continued)

5.34.1 Cobalt Serial EEPROM (continued)

The following table shows the contents of the serial EEPROM in the old for–mat used in boards shipped prior to November 2011.

Table 5–41: EEPROM Contents (Old Format)

EEPROM Byte Address	Contents	Comments
0x0000	0x00EEC0DE	Valid data word
0x0004	0x71620000	Model Number
0x0008	0x01234567	Main PCB Number
0x000C	(unsigned int) 'A'	Main Assembly Revision
0x0010	0x00020001	Option 2, Option 1
0x0014	0x00040003	Option 4, Option 3
0x0018	0x00060005	Option 6, Option 5
0x001C	0x00080007	Option 8, Option 7
0x0020	0x000A0009	Option 10, Option 9
0x0024	0x01234567	Front End PCB Number
0x0028	(unsigned int) 'A'	Front End Assembly Revision
0x002C	0x00020001	Option 2, Option 1
0x0030	0x00004567	Memory Module 1 PCB Number
0x0034	(unsigned int) 'A'	Memory Module 1 Assembly Revision
0x0038	0x00020001	Option 2, Option 1
0x003C	0x00004567	Memory Module 2 PCB Number
0x0040	(unsigned int) 'A'	Memory Module 2 Assembly Revision
0x0044	0x00040003	Option 2, Option 1
0x0048	0x03456789	Pentek Carrier PCB Number
0x004C	(unsigned int) 'A'	Pentek Carrier Assembly Revision
0x0050	0x00020001	Option 2, Option 1
0x0054 - 0x0078	0xFFFFFFFF	Reserved
0x007C	0x--------	Checksum

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5.34 TWSI Port 2 Data Register (continued)

5.34.1 Cobalt Serial EEPROM (continued)

The following table shows the contents of the serial EEPROM in the new format used in boards shipped in November 2011 and later.

Table 5–42: EEPROM Contents (New Format)

EEPROM Byte Address	Contents	Comments
0x0000	0x00000300	Base Definition Subtype, Version ANSI/VITA 42.3, Module Size: Single Wide[a]
0x0004	0x00002000	VITA 42.1, 5W @ 3.3V, 0W @ 12V, 0W @ –12W[a]
0x0008	0x000C5C00	20W @ 5V (VPWR), 20W @12V (VPWR), LINK 0 Protocol, LINK 0 Protocol[a]
0x000C	0x0000000C	LINK 1 Protocol, LINK 1 Protocol[a]
0x0010 - 0x00FC	0xFFFFFFFF	Reserved
0x0100	0x00EEC0DE	Valid data word
0x0104	0x71620000	Model Number
0x0108	0x01234567	Main PCB Number
0x010C	(unsigned int) 'A'	Main Assembly Revision
0x0110	0x00020001	Option 2, Option 1
0x0114	0x00040003	Option 4, Option 3
0x0118	0x00060005	Option 6, Option 5
0x011C	0x00080007	Option 8, Option 7
0x0120	0x000A0009	Option 10, Option 9
0x0124	0x01234567	Front End PCB Number
0x0128	(unsigned int) 'A'	Front End Assembly Revision
0x012C	0x00020001	Option 2, Option 1
0x0130	0x00004567	Memory Module 1 PCB Number
0x0134	(unsigned int) 'A'	Memory Module 1 Assembly Revision
0x0138	0x00020001	Option 2, Option 1
0x013C	0x00004567	Memory Module 2 PCB Number
0x0140	(unsigned int) 'A'	Memory Module 2 Assembly Revision
0x0144	0x00040003	Option 2, Option 1
0x0148	0x03456789	Pentek Carrier PCB Number
0x014C	(unsigned int) 'A'	Pentek Carrier Assembly Revision
0x0150	0x00020001	Option 2, Option 1
0x0154 - 0x01F8	0xFFFFFFFF	Reserved
0x01FC	0x--------	Checksum

a. Refer to the following publications for more information: *Standard for VITA 42.0 XMC* (ANSI/VITA 42.0 - 2008) and *American National Standard for XMC PCI Express Protocol Layer Standard* (ANSI/VITA 42.3-2006).

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5.35 Global Interrupt Enable Register

The Global Interrupt Enable Register contains enable bits for each interrupt condition defined. Each bit enables or disables the generation of an interrupt input to the Interrupt Flag Register, Section 5.3.

The following table shows this register's bit layout. Table 5–44, on page 162, describes the interrupt condition associated with each bit.

Table 5–43: Global Interrupt Enable Register
R/W @ BAR0+0x04074

Bit	31 – 20	19	18	17	16
Bit Name	Reserved	TWSI2 NO ACK	TWSI2 TRNSFR CMPLT	TWSI1 NO ACK	TWSI1 TRNSFR CMPLT
Function	Write zeros, Mask when reading	0 = Disable Interrupt 1 = Enable Interrupt			

Bit	15	14	13	12	11	10	9	8
Bit Name	PPS B	PPS A	SYNC B	SYNC A	GATE B	GATE A	BRD TMP	SYS MON OT
Function	0 = Disable Interrupt 1 = Enable Interrupt							

Bit	7	6	5	4	3	2	1	0
Bit Name	SYS MON ALM2	SYS MON ALM1	SYS MON ALM0	CLK B NOT LOCKED	CLK B NOT DET	CLK A NOT LOCKED	CLK A NOT DET	CDC NOT LOCKED
Function	0 = Disable Interrupt 1 = Enable Interrupt							

All bits default to the logic '0' state at power on and reset

Each bit of this register enables or disables the generation of an interrupt for an interrupt condition. Setting the bit associated with a given interrupt to logic '1' enables the generation of an interrupt to the Interrupt Flag Register, Section 5.3, when that interrupt condition occurs from the Global Interrupt Status Register, Section 5.36. When an enable bit is cleared to '0' (its default state) the interrupt will not be generated by the defined interrupt condition.

Table 5–44, on the next page, provides descriptions of the interrupt condition associated with each of these bits.

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5.35 Global Interrupt Enable Register (continued)

The following table describes the interrupt condition associated with each bit of the Global Interrupt Enable register.

Table 5–44: Global Interrupt Register Bits

Bit Name	Bit	Interrupt Function
TWSI2 NO ACK TWSI1 NO ACK	19 17	Each of these bits is associated with a lack of an acknowledge from the TWSI Port 1 or 2 controller (Section 5.31 or 5.33).
TWSI2 TRNSFR CMPLT TWSI1 TRNSFR CMPLT	18 16	Each of these bits is associated with a transfer completion signal from the TWSI Port 1 or 2 controller (Section 5.31 or 5.33).
PPS B PPS A	15 14	Each of these bits is associated with a Sync Bus PPS A or B interrupt. The interrupt occurs at the start or end edge of the respective signal, depending on the setting in Sync Bus Control Register 2 (Section 5.18).
SYNC B SYNC A	13 12	Each of these bits is associated with a Sync Bus SYNC A or B interrupt. The interrupt occurs at the start or end edge of the respective signal, depending on the setting in Sync Bus Control Register 2 (Section 5.18).
GATE B GATE A	11 10	Each of these bits is associated with an Sync Bus GATE A or B interrupt. The interrupt occurs at the start or end edge of the respective signal, depending on the setting in Sync Bus Control Register 2 (Section 5.18).
BRD TMP	9	This bit is associated with an interrupt from the LM83 and LM73 Temperature Sensors on the 71620 Main PCB, Front Panel Module, and Memory Module (Sections 5.32.1, 5.32.2, and 5.32.3).
SYS MON OT SYS MON ALM2 SYS MON ALM1 SYS MON ALM0	8 7 6 5	Each of these bits is associated with an alarm signal from the FPGA System Monitor. See Section 3.7.1 for System Monitor operation. OT – Over–Temperature alarm ALM2 – V_{CCAUX} sensor alarm ALM1 – V_{CCINT} sensor alarm ALM0 – Temperature sensor alarm
CLK B NOT LOCKED	4	This bit is associated with PLL Lock for Sync Bus Clock B.
CLK B NOT DET	3	This bit is associated with a clock loss from Sync Bus Clock B.
CLK A NOT LOCKED	2	This bit is associated with PLL Lock for Sync Bus Clock A.
CLK A NOT DET	1	This bit is associated with a clock loss from Sync Bus Clock A.
CDC NOT LOCKED	0	This bit is associated with PLL lock for the CDC7005.
These bit assignments and definitions apply to Global Interrupt Enable Register, Section 5.35, Global Interrupt Status Register, Section 5.36, and Global Interrupt Flag Register, Section 5.37		

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5.36 Global Interrupt Status Register

The Global Interrupt Status Register has one read–only status bit associated with each Global interrupt condition (the same bit associations as the Global Interrupt Enable Register, Section 5.35). The following table shows this register's bit layout. Table 5–44, on page 162, describes the interrupt condition associated with each bit.

Table 5–45: Global Interrupt Status Register
RO @ BAR0+0x04078

Bit	31 – 20	19	18	17	16
Bit Name	Reserved	TWSI2 NO ACK	TWSI2 TRNSFR CMPLT	TWSI1 NO ACK	TWSI1 TRNSFR CMPLT
Function	Write zeros, Mask when reading	0 = No Interrupt 1 = Interrupt condition asserted			

Bit	15	14	13	12	11	10	9	8
Bit Name	PPS B	PPS A	SYNC B	SYNC A	GATE B	GATE A	BRD TMP	SYS MON OT
Function	0 = No Interrupt 1 = Interrupt condition asserted							

Bit	7	6	5	4	3	2	1	0
Bit Name	SYS MON ALM2	SYS MON ALM1	SYS MON ALM0	CLK B NOT LOCKED	CLK B NOT DET	CLK A NOT LOCKED	CLK A NOT DET	CDC NOT LOCKED
Function	0 = No Interrupt 1 = Interrupt condition asserted							

When reset, including power on, the state of this register is unknown.

A status bit changes to logic '1' when the source interrupt occurs. When a status bit in this register changes to '1' the corresponding flag bit in the Global Interrupt Flag Register, Section 5.37, is set to '1'. A status bit in this register clears to logic '0' when that interrupt condition clears, whereas the associated flag bit in the Global Interrupt Flag Register, Section 5.37, remains latched at '1' until it is cleared by that register's clear action.

If the corresponding enable bit in the Global Interrupt Enable Register, Section 5.35, has been set to '1', then a status bit transition from '0' to '1' will also generate an interrupt to the Interrupt Flag Register, Section 5.3. If you do not want an interrupt to occur and have set the corresponding interrupt enable bit to '0', you may poll the status bit in this register to determine if such an event has occurred.

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5.37 Global Interrupt Flag Register

The Global Interrupt Flag Register has one read/clear flag bit associated with each Global interrupt condition (the same bit associations as the Global Interrupt Enable Register, Section 5.35). The following table shows this register's bit layout. Table 5–44, on page 162, describes the interrupt condition associated with each bit.

Table 5–46: Global Interrupt Flag Register
R/Clr @ BAR0+0x0407C

Bit	31 – 20	19	18	17	16
Bit Name	Reserved	TWSI2 NO ACK	TWSI2 TRNSFR CMPLT	TWSI1 NO ACK	TWSI1 TRNSFR CMPLT
Function	Write zeros, Mask when reading	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch			

Bit	15	14	13	12	11	10	9	8
Bit Name	PPS B	PPS A	SYNC B	SYNC A	GATE B	GATE A	BRD TMP	SYS MON OT
Function	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch							

Bit	7	6	5	4	3	2	1	0
Bit Name	SYS MON ALM2	SYS MON ALM1	SYS MON ALM0	CLK B NOT LOCKED	CLK B NOT DET	CLK A NOT LOCKED	CLK A NOT DET	CDC NOT LOCKED
Function	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch							

IMPORTANT! When reset, including power on, the state of this register is unknown. You should clear this register before using it, by writing '1's into all bits.

Read: Each flag bit in this register latches an interrupt occurrence. A '1' in any flag bit in this register indicates that an interrupt has occurred. Note that when any status bit in the Global Interrupt Status Register (Section 5.36) changes to '1' the corresponding flag bit in this register will also be set to '1'. However, when a status bit in the Global Interrupt Status Register clears from '1' to '0', the corresponding latched flag bit in this register does not clear, but remains at '1'.

Clear: Since these flag bits latch in response to an interrupt, to detect subsequent interrupts, you must clear the flag bits in this register. To clear any flag bit in this register that is set to '1' you must write a '1' to that bit.

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Chapter 6: Analog to Digital Channel Registers

6.1 Overview

This chapter describes the default FPGA registers provided for analog to digital pro–cessing. All descriptions are given from an XMC baseboard processor's viewpoint. All registers are 32–bits wide, and the register addresses are in increments of 32 bits.

The Model 71620 accepts three analog RF inputs at +8 dBm full scale into 50 ohms on front panel connectors, labeled **IN 1**, **2**, and **3**. Each of the three inputs is transformer coupled, digitized by a Texas Instruments ADS5485 200–MHz, 16–bit A/D converter (ADC), and then routed to one of the three ADC channel acquisition modules.

Each ADC channel acquisition module has several inputs that can be selected: the three ADS5485 digital outputs, a loopback of the DAC output digital data, and a digital test signal provided by an onboard sinewave generator. The FPGA routes the selected 16–bit digital data to a data packing function and then to an ADC PACK FIFO. Alter–nately, the raw 16–bit ADS5485 output can be sent to a User Block for processing by user–defined or pre–installed FPGA IP code, then to the packing function and FIFO. Data from the ADC FIFO can be routed to the optional RAM memory. The packed data can be read from the PACK FIFO or RAM memory through the PCIe interface by an Input DMA Engine.

The following is a block diagram of the analog to digital input data flow for one A/D input channel. The 71620 has three of these A/D input channels.

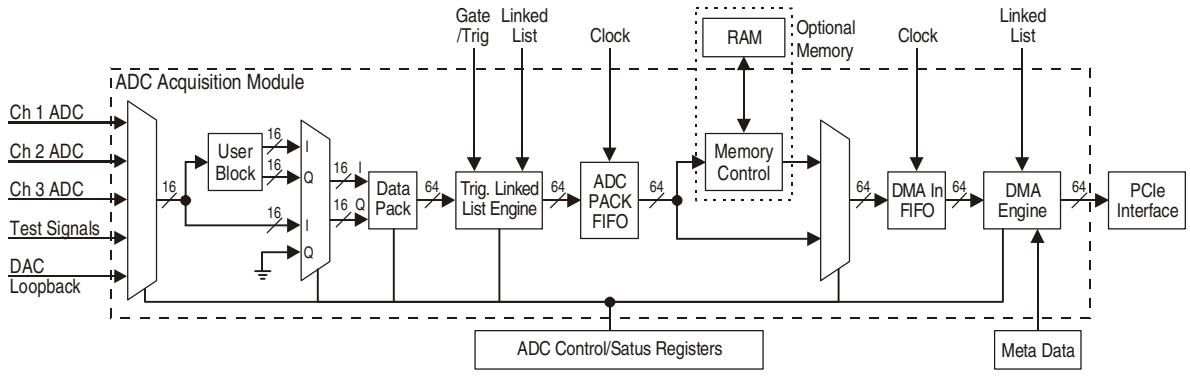


Figure 6–1: Analog to Digital Input Channel Data Flow

Refer to Chapter 4 for the memory map of all 71620 registers.

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6.2 Channel Status/Power Management Registers

There are three Channel Status/Power Management Registers, one for each ADC channel, 1, 2, and 3. Each register contains bits that provide power saving functions for elements of that ADC channel.

The following table shows the contents of these registers. The subsections following the table provide descriptions of the bits in this register.

Table 6–1: Channel Status/Power Management Registers
ADC 1: R/W @ BAR0+0x10000
ADC 2: R/W @ BAR0+0x18000
ADC 3: R/W @ BAR0+0x20000

Bit	31 – 9					8
Bit Name	Reserved					DMA DSBL
Function	Write zeros, Mask when reading					0 = Active 1 = Pwr dwn
Bit	**7**	**6**	**5**	**4**	**3 – 1 ***	**0 ***
Bit Name	MMCM PWR DWN	MEM CTRL DSBL	Reserved	ADC PWR DN	ACQ TYPE	CHAN PRESENT
Function	0 = Active 1 = Pwr dwn	0 = Active 1 = Pwr dwn	Write zero, Mask read	0 = Active 1 = Pwr dwn	000 = No RAM 001 = QDRII+ SRAM 010 = DDR3 SDRAM 011 - 111 = User defined	0 = Not present 1 = Present

* These bits are Read Only.
Bits 4 to 8 default to the logic '0' state at power on and reset

6.2.1 DMA DSBL Bit 8

This bit selects the power saving mode for DMA access to the selected ADC channel (1, 2, or 3). When the bit is cleared to logic '0' (its default state) this channel's DMA is active. When the bit is set to logic '1' this channel's DMA is shut down.

6.2.2 MMCM PWR DWN Bit 7

This bit selects the power saving mode for the ADC channel's (1, 2, or 3) memory clock PLL. When the bit is cleared to logic '0' (its default state) this channel's clock PLL is operational. When the bit is set to logic '1' this chan–nel's clock PLL is in power saving mode and the clock PLL for this channel's memory and memory controller is powered down. When the memory clock PLL is in power saving mode, the entire clock network in the FPGA is dis–abled rendering this channel inoperable. Both the DMA and the memory controller must be disabled prior to shutting down the clock.

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6.2 Channel Status/Power Management Registers (continued)

6.2.3 MEM CTRL DSBL Bit 6

This bit selects the power saving mode for the ADC channel's (1, 2, or 3) memory controller. When the bit is cleared to logic '0' (its default state) this channel's memory controller and the associated memory (if present) are operational. When the bit is set to logic '1' this channel's memory controller is held in reset and the associated memory is held in power down.

When the controller is in power saving mode, the flow of data to the DMA for this channel is still possible through the internal bypass FIFO. Maximum data rate may be impacted due to the limited depth of this FIFO.

6.2.4 ADC PWR DN Bit 4

This bit selects the power saving mode for the ADC (1, 2, or 3). When the bit is cleared to logic '0' (its default state) this channel's ADC is active. When the bit is set to logic '1' this channel's ADC is powered down to sleep mode.

6.2.5 ACQ TYPE Bits 3 – 1

These three read–only bits indicate the type of data acquisition available for this ADC channel (1, 2, or 3). The types of data acquisition are:

000	Data acquisition uses no external RAM
001	Data acquisition uses QDRII+ SRAM
010	Data acquisition uses DDR3 SDRAM
011-111	User defined

6.2.6 CHAN PRESENT Bit 0

This read–only bit indicates the FPGA code availability for this ADC data processing channel (1, 2, or 3). When the bit is cleared to logic '0' (its default state) this channel is not present in the FPGA code. When the bit is set to logic '1' this channel is present in the FPGA code.

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6.3 ADC Input Delay Tap Control Registers

There are three ADC Input Delay Tap Control Registers, one for each ADC channel (1, 2, and 3). Each register determines the input delay of the digital data from the associated ADS5485.

The following table shows the contents of this register.

Table 6–2: ADC Input Delay Tap Control Registers
ADC 1: R/W @ BAR0+0x10004
ADC 2: R/W @ BAR0+0x18004
ADC 3: R/W @ BAR0+0x20004

Bit	31 – 5	4 – 0
Bit Name	Reserved	IN TAP DLY[4:0]
Function	Write zeros, Mask when reading	N
All bits default to the logic '0' state at power on and reset		

IN TAP DLY is a 5–bit binary value. It is used to specify an input delay according to the following formula:

IN TAP DLY = **N** x 75 picoseconds

Depending on the setting of the CLKA SRC SEL bit in the Clock Control/Status Register, Section 5.16, this register should be set to the following value for proper operation:

- For ‘CDC clock’ – set IN TAP DLY to 0 (zero)
- For ‘ADC1 clock’ – set IN TAP DLY to 0

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6.4 ADC Data Control Registers

There are three ADC Data Control Registers, one for each ADC channel, 1, 2, and 3. Each register contains bits that select the data packing modes and the characteristics of the data samples from the ADS5485 to the ADC PACK FIFOs.

The following table shows the contents of these registers. The subsections following the table provide descriptions of the bits in this register.

Table 6–3: ADC Data Control Registers
ADC 1: R/W @ BAR0+0x10008
ADC 2: R/W @ BAR0+0x18008
ADC 3: R/W @ BAR0+0x20008

Bit	31 – 14	13	12	11–10	9	8
Bit Name	Reserved	SYNC SEL	OV LED SEL	Reserved	TS SUB EN	ADC DITHER
Function	Write zeros, Mask when reading	0 = Sync A 1 = Pulse	0 = ADC ovld 1 = FIFO ovrn	Write zeros, Mask when reading	0 = Disable 1 = Enable	0 = Disable 1 = Enable

Bit	7	6	5	4	3	2 – 0
Bit Name	PACK FIFO RST	USR DAT SEL	PACK MODE		Reserved	DATA SRC
Function	0 = Run 1 = Reset	0 = ADS5485 1 = User Block	00 = I Packed 01 = I Unpacked 10 = I/Q Packed 11 = I/Q Unpacked		Write zero, Mask read	000 = This ADC 001 = ADC1 010 = ADC2 011 = ADC3 100 = Not used on 71620 101 = Test Sig Gen Ramp 110 = Test Sig Gen Sinewave 111 = DAC Loopback

All bits default to the logic '0' state at power on and reset

6.4.1 SYNC SEL Bit 13

This bit specifies the sync source for the user block sync signal. When this bit is cleared to logic '0' (its default state) the user block sync is the Sync A RCV signal selected by the Sync Bus Control Register 2, Section 5.18. When the bit is set to logic '1' the user block sync is a 1 clock–cycle pulse that is generated on the rising edge of each active gate, either from the selected input gate or the linked list gates, depending on the source of the gate selected by the associated ADC Gate/Trigger Control Register Section 6.6.

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6.4 ADC Data Control Registers (continued)

6.4.2 OV LED SEL Bit 12

This bit specifies the error source for the front panel ADC **OV** LED, Section 2.8.8. When this bit is cleared to logic '0' (its default state) the **OV** LED is driven by an overvoltage condition in the associated ADS5485 (1, 2, or 3). When the bit is set to logic '1' the **OV** LED is driven by an ADC FIFO overflow and loss of data.

6.4.3 TS SUB EN Bit 9

This bit enables the Time Stamp marker for the selected ADC (1, 2, or 3). When the bit is cleared to logic '0' (its default state) Time Stamp is disabled. When the bit is set to logic '1' Time Stamp is enabled and the marker bit substitutes for the data LSB (see ADC Data Formats, Section 3.2.1).

6.4.4 ADC DITHER Bit 8

This bit enables dither mode in the associated ADS5485 (1, 2, or 3). When the bit is cleared to logic '0' (its default state) ADS5485 dither is disabled. When the bit is set to logic '1' ADS5485 dither is enabled.

6.4.5 PACK FIFO RST Bit 7

This bit resets the ADC PACK FIFO (1, 2, or 3). When the bit is cleared to logic '0' (its default state) the FIFO is in run. When the bit is set to logic '1' the FIFO is in reset.

6.4.6 USR DAT SEL Bit 6

This bit selects the data source for writes to the ADC PACK FIFO (1, 2, or 3). When the bit is cleared to logic '0' (its default state) the raw ADS5485 data is the source; when the bit is set to logic '1' the User Block data is the source.

6.4.7 PACK MODE Bits 5 – 4

These two bits select the data packing mode for the ADC PACK FIFO (1, 2, or 3). The types of data packing are:

00 Real data is packed with four samples per 64–bit FIFO word
01 Real data is unpacked with two samples per 64–bit FIFO word
10 I/Q data is packed with two I/Q values per 64–bit FIFO word
11 I/Q data is unpacked with one I/Q value per 64–bit FIFO word

See Section 3.2.1 for illustration of the ADC data packing formats. Note that when you select ADS5485 as the data source (Bit 6 above), the ADS5485 data is the Real data, and the Q data is zero.

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6.4 ADC Data Control Registers (continued)

6.4.8 DATA SRC Bits 2 – 0

These three bits select the data source for the ADC PACK FIFO (1, 2, or 3). The data sources are:

000 This channel's ADS5485
001 ADS5485 #1
010 ADS5485 #2
011 ADS5485 #3
100 not used on 71620
101 Test Signal Gen Ramp
110 Test Signal Gen Sinewave
111 DAC output loopback

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6.5 ADC Rate Divider Registers

There are three ADC Rate Divider Registers, one for each ADC channel, 1, 2, and 3. This register sets the decimation rate of data samples written to the applicable ADC PACK FIFO.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–4: ADC Rate Divider Register
ADC 1: R/W @ BAR0+0x1000C
ADC 2: R/W @ BAR0+0x1800C
ADC 3: R/W @ BAR0+0x2000C

Bit	31 – 16	15 – 0
Bit Name	Reserved	DEC[15:0]
Function	Write zeros, Mask when reading	16–bit rate divider 'N–1'
All bits default to the logic '0' state at power on and reset		

DEC is a 16–bit binary value, with bit 15 the MSB. To take every Nth sample, where N is any value between 1 and 65536, set this value to N–1.

This rate divider is applied pre–packing. It does not affect User Block data, only raw ADC data.

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6.6 ADC Gate/Trigger Control Registers

There are three ADC Gate/Trigger Control Registers, one for each ADC channel, 1, 2, and 3. Each register contains bits that select the source and characteristics of the gate/trigger used to control writing data samples from the ADS5485 to the associated ADC PACK FIFO.

The following table shows the contents of these registers. The subsections following the table provide descriptions of the bits in this register.

Table 6–5: ADC Gate/Trigger Control Registers
ADC 1: R/W @ BAR0+0x10010
ADC 2: R/W @ BAR0+0x18010
ADC 3: R/W @ BAR0+0x20010

	31 – 10	9	8
Bit Name	Reserved	LOC GATE SEL	TRIG LINKED LIST RST
Function	Write zeros, Mask when reading	0 = Global 1 = Local	0 = Run 1 = Reset

	7	6	5	4	3	2	1	0
Bit Name	TIMESTAMP FIFO RST	TRIG NUM RST	PPS LATCH EN	USR DVAL EN	TRIG CLR	TRIG HOLD	GATE TRIG IN EN	TRIG MODE
Function	0 = Run 1 = Reset	0 = Run 1 = Reset	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Run 1 = Clear	0 = None 1 = Hold	0 = Disable 1 = Enable	0 = Gate 1 = Trigger

All bits default to the logic '0' state at power on and reset

6.6.1 LOC GATE SEL Bit 9

This bit selects the gate signal for the associated ADC PACK FIFO (1, 2, or 3) from either the global gate or the local gate. When the bit is cleared to logic '0' (its default state) the global gate (GATE A) is used to enable writing to the PACK FIFO. When the bit is set to logic '1' this ADC channel's local gate, generated by the associated Local Gate Generate Register Section 6.8, is used to enable writing to the PACK FIFO.

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6.6 ADC Gate/Trigger Control Registers (continued)

6.6.2 TRIG LINKED LIST RST Bit 8

This bit resets the Trigger Gen Linked List for this channel's ADC PACK FIFO (1, 2, or 3). When the bit is cleared to logic '0' (its default state) the Linked List is in run. When the bit is set to logic '1' the Linked List is reset to the starting Link Definition index number specified in the associated ADC Trigger Gen Linked List Start Pointer Register, Section 6.7.

NOTE: A reset must be performed prior to starting a new linked list sequence, and a reset must be performed after programming the linked list definitions in the Linked List RAM.

Refer to Section 3.2.4 for description of the ADC DMA Linked Lists.

6.6.3 TIMESTAMP FIFO RST Bit 7

This bit resets the Timestamp FIFO for this channel's ADC PACK FIFO. When the bit is cleared to logic '0' (its default state) the FIFO is in run. When the bit is set to logic '1' the FIFO is in reset.

6.6.4 TRIG NUM RST Bit 6

This bit resets the Trigger Number Counter and the Gate Number Counter for this ADC channel (1, 2, or 3). When the bit is cleared to logic '0' (its default state) the counters are in run. When the bit is set to '1' the counters are in reset.

6.6.5 PPS LATCH EN Bit 5

This bit enables the PPS latch for this channel's ADC PACK FIFO. When the bit is cleared to logic '0' (its default state) the FIFO is disabled. When the bit is set to logic '1' the FIFO is enabled.

When enabled, at the first active data sample period of a gate or trigger gen−erated gate, the timestamp value is latched and stored in a holding FIFO for use by this channel's DMA in Meta−Data packets. See timestamp module info for more details.

6.6.6 USR DVAL EN Bit 4

This bit enables the data valid signal for this channel's ADC PACK FIFO. When the bit is cleared to logic '0' (its default state), the rate divider DEC[15:0] (Section 6.5) controls the data valid rate to the data packing mod−ule and increment rate of the trigger counter. When the bit is set to logic '1' the USER_DVAL signal from the User Block is used to control the data rate and increment rate of the trigger counter. Set to 1 when User Block data is selected unless user block data is not decimated.

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6.6 ADC Gate/Trigger Control Registers (continued)

6.6.7 TRIG CLR Bit 3

When in Trigger mode (TRIG MODE bit 0 = 1, below), this bit clears any active triggered gate for the channel's ADC PACK FIFO. When this bit is cleared to logic '0' (its default state) the trigger is in run. When this bit is set to logic '1', the system asynchronously clears any active trigger for this FIFO.

6.6.8 TRIG HOLD Bit 2

This bit enables a gate Hold after the trigger is received in Trigger mode (TRIG MODE bit 0 = 1, below) for the channel's ADC PACK FIFO. When the bit is cleared to logic '0' (its default state) the selected gate is active (FIFO writes enabled) for the specified trigger length after the trigger (specified using the Trigger Gen Linked List), and then goes inactive (FIFO writes disabled). When the bit is set to logic '1' HOLD is enabled and the gate remains active (FIFO writes enabled) after the trigger is received until the Trigger is cleared using the TRIG CLR bit 3, above.

Note that when HOLD is enabled, you must set the Trigger Length to any number greater than zero.

6.6.9 GATE TRIG IN EN Bit 1

This bit enables the gate/trigger signal for the channel's ADC PACK FIFO. When this bit is cleared to logic '0' (its default state), this bit inhibits the Gate signal (GATE A) from affecting an individual channel. Use this to disable the gate or trigger to channels that are not being used. This saves power and also keeps data from flowing into FIFOs on unused channels. When this bit is set to logic '1', the Gate signal is enabled.

6.6.10 TRIG MODE Bit 0

This bit selects Gate or Trigger mode for enabling ADC PACK FIFO writes. When this bit is cleared to logic '0' (its default state) Gate mode is selected. When this bit is set to logic '1', Trigger mode is selected and you must set the trigger length using the Trigger Gen Linked List (Section 3.2.2), and optionally enable trigger Hold (TRIG HOLD bit 2, above).

The active edge of trigger must be separated by a minimum of three clock cycles. Triggers occurring before the present trigger period is completed are ignored.

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6.7 ADC Trigger Gen Linked List Start Pointer Registers

There are three ADC Trigger Gen Linked List Start Pointer Registers, one for each ADC data channel, 1, 2, and 3. These registers specify the starting Link Number in the linked list for the applicable ADC PACK FIFO trigger sequences.

The following tables show the format of these registers.

Table 6–6: ADC Trigger Gen Linked List Start Pointer Registers
ADC 1: R/W @ BAR0+0x10014
ADC 2: R/W @ BAR0+0x18014
ADC 3: R/W @ BAR0+0x20014

Bit	31 – 6	5 – 0
Bit Name	Reserved	TRIG LL STRT ADDR[5:0]
Function	Write zeros, Mask when reading	Trigger Gen Linked List Start Index (N)
All bits default to the logic '0' state at power on and reset		

TRIG LL STRT ADDR is a 6–bit binary value, with the most significant bit in bit 5 of the register. This value specifies the starting Link Definition index number, within the Trigger Gen Linked List (Section 3.2.2), to be used for the next ADC FIFO transfer. The linked list in this memory area contains all the trigger sequences required for this transfer.

When starting a new linked list sequence at this Link Definition number, you must reset the linked list using TRIG LINKED LIST RST (bit 8) in the associated ADC Gate/ Trigger Control Register, Section 6.6.

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6.8 Local Gate Generate Registers

There are three Local Gate Generate Registers, one for each ADC data channel, 1, 2, and 3. Each register generates a local GATE signal for the associated ADC channel, which can be used to enable writing to the channel's ADC PACK FIFO.

The following table shows the contents of this register.

Table 6–7: Local Gate Generate Registers
ADC 1: R/W @ BAR0+0x10018
ADC 2: R/W @ BAR0+0x18018
ADC 3: R/W @ BAR0+0x20018

Bit	31 – 1	0
Bit Name	Reserved	LOC GATE
Function	Write zeros, Mask when reading	0 = Inactive 1 = Active
Bit 0 defaults to the logic '1' state at power on and reset		

When the local gate is selected for the associated ADC channel (LOC GATE SEL = 1, ADC Gate/Trigger Control Register, Section 6.6), the GATE bit in this register creates the gate signal to enable writing to the ADC channel's PACK FIFO.

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6.9 RAM Control Registers

There are three RAM Control Registers, one for each ADC data channel, 1, 2, and 3. These registers contain control bits for operation of QDRII+ SRAM or DDR3 SDRAM for the associated ADC channel.

The following table shows the contents of this register. The subsections following the table provide descriptions of each bit in this register.

Table 6–8: RAM Control Registers
ADC 1: R/W @ BAR0+0x1001C
ADC 2: R/W @ BAR0+0x1801C
ADC 3: R/W @ BAR0+0x2001C

Bit	31 – 8							
Bit Name	Reserved							
Function	Write zeros, Mask when reading							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	RAM READ EN	Reserved	RAM PATH EN	RAM RST	Reserved			MEM CTLR RST
Function	0 = Disable 1 = Enable	Write zero, Mask read	0 = Disable 1 = Enable	0 = Run 1 = Reset	Write zeros, Mask when reading			0 = Run 1 = Reset
All bits default to the logic '0' state at power on and reset.								

6.9.1 RAM READ EN Bit 7

This bit enables the data flow of the data output from QDRII+ or DDR3 RAM to the DMA IN FIFO for the selected ADC channel (1, 2, or 3). When the bit is cleared to logic '0' (its default state) data flow out of the RAM is disabled from starting. When the bit is set to '1' data flow out of the RAM is allowed to start to the DMA IN FIFO.

6.9.2 RAM PATH EN Bit 5

This bit enables data flow from the ADC PACK FIFO to QDRII+ or DDR3 RAM for the selected ADC channel (1, 2, or 3). When this bit is cleared to logic '0' (its default state) SRAM is bypassed and data flows directly to the DMA IN FIFO. When this bit is set to '1' data flow to the RAM is enabled. Data from the PACK FIFO flows into the RAM, which is used as a deep FIFO, and the DMA engine can simultaneously read data from it.

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6.9 RAM Control Registers (continued)

6.9.3 RAM RST Bit 4

This bit resets the QDRII+ or DDR3 RAM for the selected ADC channel (1, 2, or 3). When the bit is cleared to logic '0' (its default state) the RAM is in run. When the bit is set to '1' the RAM is in reset and the RAM FIFO is flushed.

Reset before a capture to clear the previous capture data, data pointers, and data count.

6.9.4 MEM CTLR RST Bit 0

This bit resets the memory controller for the selected ADC channel (1, 2, or 3). When the bit is cleared to logic '0' (its default state) the memory controller is in run. When the bit is set to '1' the memory controller is in reset. After being reset, the memory controller will reinitialize and recalibrate. Note: The memory controller is also reset by LRST_N from the PCIe core and power−on reset.

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6.10 Input DC Offset Registers

There are three Input DC Offset Registers, one for each ADC channel, 1, 2, and 3. The registers define the DC offset for each ADC channel.

The following table shows the bit layout of this register. The paragraphs following the table describe these bits.

Table 6–9: Input DC Offset Registers
ADC 1: R/W @ BAR0+0x10020
ADC 2: R/W @ BAR0+0x18020
ADC 3: R/W @ BAR0+0x20020

Bit	31 – 16
Bit Name	Reserved
Function	Write zeros, Mask when reading
Bit	**15 – 0**
Bit Name	DC OFFSET[15:0]
Function	DC Offset Trim
All bits default to the logic '0' state at power on and reset	

DC OFFSET is the DC Offset trim for this ADC channel. This value is a two's comple–ment, signed 16–bit number.

0x7FFF = +full scale
0x8000 = –full scale

This value is added to the input stream for this acquisition module and can be used to null out or minimize ADC DC offset errors. Note that is will affect all input sources selected for input, including the test signal.

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6.11 Input Gain Trim Registers

There are three Input Gain Trim Registers, one for each ADC channel, 1, 2, and 3. The registers define the gain trim for each ADC channel.

The following table shows the bit layout of this register. The paragraphs following the table describe these bits.

Table 6–10: Input Gain Trim Registers
ADC 1: R/W @ BAR0+0x10024
ADC 2: R/W @ BAR0+0x18024
ADC 3: R/W @ BAR0+0x20024

Bit	31 – 16
Bit Name	Reserved
Function	Write zeros, Mask when reading
Bit	**15 – 0**
Bit Name	GAIN[15:0]
Function	Gain Trim
All bits default to the logic '0' state at power on and reset	

GAIN is the gain trim for this ADC channel. This value is an unsigned 16–bit number.

0x0000 = zero gain
0x8000 = unity gain
0x8FFF = almost gain of 2

The following shows unity gain with the decimal place after bit 15.

Bit number:	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Decimal place:	1.	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This value multiplies the input stream for this acquisition module and can be used to trim the gain of the input ADC signal. Note that is will affect all input sources selected for input, including the test signal. Therefore it can also be used to create a test signal with an amplitude less than full scale.

The result of the multiplication is rounded and is also saturated to a 16–bit value if it exceeds full scale.

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6.12 ADC DMA Control Registers

There are three ADC DMA Control Registers, one for each ADC channel, 1, 2, and 3. The registers provide control bits for DMA data transfers from each ADC channel to the PCIe interface.

The following table shows the bit layout of this register. The subsections following the table describe these bits.

Table 6–11: ADC DMA Control Registers
ADC 1: R/W @ BAR0+0x10028
ADC 2: R/W @ BAR0+0x18028
ADC 3: R/W @ BAR0+0x20028

Bit	31 – 16							
Bit Name	Reserved							
Function	Write zeros, Mask when reading							
Bit	**15**	**14 – 13**		**12 – 10**			**9**	**8**
Bit Name	BYTE SWAP	DMA AT		DMA TC			DMA ATTR1	DMA ATTR0
Function	0 = No swap 1 = Swap	00 = Default/Untranslated 01 = Translation request 10 = Translated 11 = Reserved		000 = Best effort service class 001 - 111 = Differentiated service class			0 = Default 1 = Relaxed	0 = Default 1 = No Snoop
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Reserved	DMA ABORT	DMA IN FIFO RST	DMA RST	Reserved			DMA ADV
Function	Write 0, Mask read	0 = Run 1 = Abort	0 = Run 1 = Reset	0 = Run 1 = Reset	Write zeros, Mask when reading			0 = No action 1 = Advance
All bits default to the logic '0' state at power on and reset								

6.12.1 BYTE SWAP Bit 15

This bit sets byte swap mode of the DMA transfer for the selected ADC channel (1, 2, or 3). When the bit is cleared to logic '0' (its default state) byte swapping is disabled. When the bit is set to '1' byte swapping is enabled for DMA transfers to the PCIe interface.

Bytes are swapped within each 64–bit word, as follows.

No swap: 0, 1, 2, 3, 4, 5, 6, 7
Swap: 7, 6, 5, 4, 3, 2, 1, 0

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6.12 ADC DMA Control Registers (continued)

6.12.2 DMA AT Bits 14 – 13

These two bits select the Address Type of the PCI Express Packet transferred by DMA for this ADC channel (1, 2, or 3). These address types are defined by the PCI Express Base Specification:

00 Default/Untranslated
01 Translation Request
10 Translated
11 Reserved

6.12.3 DMA TC Bits 12 – 10

These three bits select the Traffic Class of the PCI Express Packet transferred by DMA for this ADC channel (1, 2, or 3). These traffic classes are defined by the PCI Express Base Specification:

000 TC0: Best Effort service class (General Purpose I/O)
001 – 111 TC1–TC7: Differentiated service classes

6.12.4 DMA ATTR1 Bit 9

This bit selects the Relaxed Ordering Attribute of the PCI Express Packet transferred by DMA for this ADC channel (1, 2, or 3). These attributes are defined by the PCI Express Base Specification. When the bit is cleared to logic '0' (its default state) the packet is in Default Ordering (PCI Strongly Ordered Model). When the bit is set to '1' the packet is in Relaxed Ordering (PCI–X Relaxed Ordering Model).

6.12.5 DMA ATTR0 Bit 8

This bit selects the No Snoop Attribute of the PCI Express Packet transferred by DMA for this ADC channel (1, 2, or 3). These attributes are defined by the PCI Express Base Specification. When the bit is cleared to logic '0' (its default state) the packet is in default (Hardware enforced cache coherency expected). When the bit is set to '1' the packet is in No Snoop (Hardware enforced cache coherency not expected).

6.12.6 DMA ABORT Bit 6

This bit aborts the DMA engine for the selected ADC channel (1, 2, or 3). When toggled to a '1' then '0' a DMA abort sequence will commence. Any DMA packets that have already been constructed will be allowed to be transmitted. All new DMA activity will be inhibited. When all packets have been transmitted, a DMA reset will automatically be generated.

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6.12 ADC DMA Control Registers (continued)

6.12.7 DMA IN FIFO RST Bit 5

This bit resets the DMA IN FIFO for the selected ADC channel (1, 2, or 3). When the bit is cleared to logic '0' (its default state) the FIFO is in run. When the bit is set to '1' the FIFO is in reset.

- For QDRII+ SRAM, this bit will reset the input FIFO to the DMA engine. It also resets and flushes the FIFO implemented using the QDRII+ SRAM.
- For DDR3 SDRAM, this bit will reset the input FIFO to the DMA engine. It also resets and flushes the FIFO implemented using the DDR3 SDRAM.

Note that the FIFO is also reset by DMA RST (bit 4) = 1, as described below.

6.12.8 DMA RST Bit 4

This bit resets the DMA engine for the selected ADC channel (1, 2, or 3). When the bit is cleared to logic '0' (its default state) the DMA is in run. When the bit is set to '1' the DMA engine is in reset and the DMA IN FIFO is reset.

6.12.9 DMA ADV Bit 0

This bit advances the DMA linked list for the selected ADC channel (1, 2, or 3). When the bit is cleared to logic '0' (its default state) the DMA linked list does not advance. When the bit is toggled to '1' the DMA linked list Advances. At the rising edge of this bit the linked list will advance if it is waiting. The first link must be kicked off by this bit and any other link that is programmed to not execute automatically also will be kicked off by tog−gling this bit.

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6.13 ADC Interrupt Enable Registers

There are three ADC Interrupt Enable Registers, one for each ADC channel, 1, 2, and 3. Each register contains enable bits for each ADC acquisition module interrupt. Each bit enables or disables the generation of an interrupt input to the ADC Interrupt Status Register, Section 6.15.

The following table shows the enable bit layout of this register. Table 6–13, on the next page, describes the interrupt condition associated with each bit.

Table 6–12: ADC Interrupt Enable Registers
ADC 1: R/W @ BAR0+0x1002C
ADC 2: R/W @ BAR0+0x1802C
ADC 3: R/W @ BAR0+0x2002C

Bit	31 – 23	22	21	20	19	18	17	16
Bit Name	Reserved	TIMESTAMP FIFO FULL	TIMESTAMP FIFO EMP	BAD TRIGGER	TRIG NUM FIFO FULL	TRIG NUM FIFO EMP	MEM CLK IN STOPPED	MEM MMCM NOT LOCK
Function	0 = Disable Interrupt 1 = Enable Interrupt							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Bit Name	Reserved		RAM FIFO ALM FULL	RAM FIFO EMP	DMA IN FIFO ALM FULL	DMA IN FIFO EMP	ADC PACK FIFO FULL	ADC PACK FIFO EMP
Function	0 = Disable Interrupt 1 = Enable Interrupt							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	CHAIN END	LINK END	GATE END	GATE START	TRIG CMPLT	FPGA CLKA NOT DET	CDC CLKA NOT LOCK	ADC OVLD
Function	0 = Disable Interrupt 1 = Enable Interrupt							

All bits default to the logic '0' state at power on and reset

Each bit of this register enables or disables the generation of an interrupt for an interrupt condition. Setting the bit associated with a given interrupt to logic '1' enables passing the interrupt to the Interrupt Flag Register, Section 5.3, when that interrupt condition occurs from the associated ADC Interrupt Status Register, Section 6.15. When an enable bit is cleared to logic '0' (its default state) the interrupt will not be passed to the Interrupt Flag Register, Section 5.3, but will be latched in the ADC Interrupt Flag Register, Section 6.14.

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6.13 ADC Interrupt Enable Registers (continued)

The following table describes the interrupt condition associated with each bit of the ADC Interrupt registers.

Table 6–13: ADC Interrupt Register Bits

Bit Name	Bit Position	Interrupt Function
TIMESTAMP FIFO FULL, TIMESTAMP FIFO EMP	22, 21	Each of these interrupts signals a FIFO Empty or Full condition, respectively, from the TIMESTAMP FIFO.
BAD TRIGGER	20	This interrupt signals a trigger occurrence before the end of the active linked list gates/triggers.
TRIG NUM FIFO FULL, TRIG NUM FIFO EMP	19, 18	Each of these interrupts signals a FIFO Empty or Full condition, respectively, from the TRIG NUM FIFO.
MEM CLK IN STOPPED	17	This interrupt signals a memory clock stopped condition.
MEM MMCM NOT LOCK	16	This interrupt signals a memory MMCM clock PLL not locked condition.
RAM FIFO ALM FULL, RAM FIFO EMP	13, 12	Each of these interrupts signals a FIFO Empty or FIFO Almost Full condition, respectively, from the RAM FIFO. See RAM Controller Status Registers, Section 6.17,
DMA IN FIFO ALM FULL, DMA IN FIFO EMP	11, 10	Each of these interrupts signals a FIFO Empty or FIFO Almost Full condition, respectively, from the ADC DMA IN FIFO.
ADC PACK FIFO FULL, ADC PACK FIFO EMP	9, 8	Each of these interrupts signals a FIFO Empty or Full condition, respectively, from the ADC PACK FIFO.
CHAIN END, LINK END	7, 6	Each of these interrupts is the end of a link or end of the full chain of links, respectively, of a DMA transfer linked list.
GATE END, GATE START	5, 4	Each of these interrupts is the start or end, respectively, of a programmed Gate period.
TRIG CMPLT	3	This interrupt signals a trigger complete, which occurs at the end of the active linked list gate/trigger occurrences. Note that this does not necessarily mean that the data transfer that was started by the trigger/gate has completed, only that the trigger/gate is complete.
FPGA CLKA NOT DET	2	This interrupt signals the FPGA CLKA clock not detected. See IDelay and Clock Status Register, Section 6.16.
CDC CLKA NOT LOCK	1	This interrupt signals CDC7005 CLKA clock PLL not locked. See IDelay and Clock Status Register, Section 6.16.
ADC OVLD	0	This interrupt is from the ADS5485 overload detection circuitry.
These bit assignments and definitions apply to ADC Interrupt Enable Register, Section 6.13, ADC Interrupt Status Register, Section 6.15, and ADC Interrupt Flag Register, Section 6.14		

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6.14 ADC Interrupt Flag Registers

There are three ADC Interrupt Flag Registers, one for each ADC channel, 1, 2, and 3. Each register contains one read/clear flag bit associated with each ADC interrupt condition (the same bit associations as the ADC Interrupt Enable Register, Section 6.13.

The following table shows the flag bit layout of this register. Table 6–13, on page 186, describes the interrupt condition associated with each bit.

Table 6–14: ADC Interrupt Flag Registers

ADC 1: R/Clr @ BAR0+0x10030
ADC 2: R/Clr @ BAR0+0x18030
ADC 3: R/Clr @ BAR0+0x20030

Bit	31 – 23	22	21	20	19	18	17	16
Bit Name	Reserved	TIMESTAMP FIFO FULL	TIMESTAMP FIFO EMP	BAD TRIGGER	TRIG NUM FIFO FULL	TRIG NUM FIFO EMP	MEM CLK IN STOPPED	MEM MMCM NOT LOCK
Function	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Bit Name	Reserved		RAM FIFO ALM FULL	RAM FIFO EMP	DMA IN FIFO ALM FULL	DMA IN FIFO EMP	ADC PACK FIFO FULL	ADC PACK FIFO EMP
Function	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	CHAIN END	LINK END	GATE END	GATE START	TRIG CMPLT	FPGA CLKA NOT DET	CDC CLKA NOT LOCK	ADC OVLD
Function	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch							

IMPORTANT! When reset, including power–up, the state of this register is unknown. You should clear this register before using it, by writing '1's into all bits.

Read: Each flag bit of this register latches an interrupt occurrence. Logic '1' in any bit in this register indicates that an interrupt has occurred. Note that when any status bit in the ADC Interrupt Status Register (Section 6.15) changes to logic '1' the corresponding flag bit in this register will also be set to logic '1'. However, when a status bit in the ADC Interrupt Status Register clears from logic '1' to logic '0', the corresponding latched flag bit in this register does not clear, but remains at logic '1'.

Clear: Since these bits latch in response to an interrupt, to detect subsequent interrupts, you must clear the flag bits in this register. To clear any flag bit in this register that is set to '1' you must write a '1' to that bit.

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6.15 ADC Interrupt Status Registers

There are three ADC Interrupt Status Registers, one for each ADC channel, 1, 2, and 3. Each register contains one read–only status bit associated with each ADC interrupt condition (the same bit associations as the ADC Interrupt Enable Register, Section 6.13.

The following table shows the status bit layout of this register. Table 6–13, on page 186, describes the interrupt condition associated with each bit.

Table 6–15: ADC Interrupt Status Registers

ADC 1: RO @ BAR0+0x10034
ADC 2: RO @ BAR0+0x18034
ADC 3: RO @ BAR0+0x20034

Bit	31 – 23	22	21	20	19	18	17	16
Bit Name	Reserved	TIMESTAMP FIFO FULL	TIMESTAMP FIFO EMP	BAD TRIGGER	TRIG NUM FIFO FULL	TRIG NUM FIFO EMP	MEM CLK IN STOPPED	MEM MMCM NOT LOCK
Function	0 = No Interrupt 1 = Interrupt condition asserted							
Bit	15	14	13	12	11	10	9	8
Bit Name	Reserved		RAM FIFO ALM FULL	RAM FIFO EMP	DMA IN FIFO ALM FULL	DMA IN FIFO EMP	ADC PACK FIFO FULL	ADC PACK FIFO EMP
Function	0 = No Interrupt 1 = Interrupt condition asserted							
Bit	7	6	5	4	3	2	1	0
Bit Name	CHAIN END	LINK END	GATE END	GATE START	TRIG CMPLT	FPGA CLKA NOT DET	CDC CLKA NOT LOCK	ADC OVLD
Function	0 = No Interrupt 1 = Interrupt condition asserted							

When reset, including power–up, the state of this register is unknown.

A status bit changes to logic '1' when the source interrupt occurs. When a status bit in this register changes to '1' the corresponding flag bit in the ADC Interrupt Flag Register, Section 6.14, is set to '1'. A status bit in this register clears to logic '0' when that interrupt condition clears, whereas the associated flag bit in the ADC Interrupt Flag Register, Section 6.14, remains latched at '1' until it is cleared by that register's clear action.

If the corresponding enable bit in the ADC Interrupt Enable Register, Section 6.13, has been set to logic '1', then a status bit transition from logic '0' to logic '1' will also generate an interrupt to the Interrupt Flag Register, Section 5.3. If you do not want an interrupt to occur and have set the corresponding interrupt enable bit to '0', you may poll the ADC Interrupt Flag Register flag bit, Section 6.14, to determine if such an event has occurred. The ADC Interrupt Flag Register will latch the event regardless of the setting of the interrupt enable bit.

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6.16 IDelay and Clock Status Registers

There are three read–only IDelay and Clock Status Registers, one for each ADC channel, 1, 2, and 3. The registers provide status bits for the clocks and input delays for the selected ADC channel.

The following table shows the bit layout of this register. The subsections following the table describe these bits.

Table 6–16: IDelay and Clock Status Registers
ADC 1: RO @ BAR0+0x10038
ADC 2: RO @ BAR0+0x18038
ADC 3: RO @ BAR0+0x20038

Bit	31 – 8							
Bit Name	Reserved							
Function	Mask when reading							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	MEM CLK FB STOPPED	MEM CLK IN STOPPED	MEM MMCM LOCK	MEM IODLY CTRL RDY	Reserved	FPGA CLKA NOT DET	CDC CLKA LOCK	ADC IODLY CTRL RDY
Function	0 = Not stop 1 = Stopped	0 = Not stop 1 = Stopped	0 = Not lock 1 = Locked	0 = Not rdy 1 = Ready	Mask read	0 = Normal 1 = Not det.	0 = Not lock 1 = Locked	0 = Not rdy 1 = Ready
When reset, including power–up, the state of this register is unknown.								

6.16.1 MEM CLK FB STOPPED Bit 7

This bit indicates the operating state of the memory clock output for the selected ADC channel (1, 2, or 3). When the bit is read as logic '0' the Memory Clock is not stopped. When the bit is read as '1' Memory Clock output is stopped. This indicates a problem with the PLL or the Memory clock oscillator.

6.16.2 MEM CLK IN STOPPED Bit 6

This bit indicates the operating state of the memory clock input for the ADC channel (1, 2, or 3). When the bit is read as logic '0' the Memory Clock is not stopped. When the bit is read as '1' Memory Clock is stopped. This indicates a problem with the PLL or the Memory clock oscillator.

6.16.3 MEM MMCM LOCK Bit 5

This bit indicates the locked state of the memory clock PLL for the ADC channel (1, 2, or 3). When the bit is read as logic '0' the Memory Clock PLL is not locked. When the bit is read as '1' Memory Clock PLL is locked.

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6.16 IDelay and Clock Status Registers (continued)

6.16.4 MEM IODLY CTRL RDY Bit 4

This bit indicates the ready state of the memory IODELAY control for the ADC channel (1, 2, or 3) RAM interface. When the bit is read as logic '0' IODELAY control is not ready – it is either held in reset or the 200–MHz Reference clock is missing. When the bit is read as '1' IODELAY control is ready.

6.16.5 FPGA CLKA NOT DET Bit 2

This bit indicates the operating state of the FPGA CLKA clock (either CDC7005 CLKA or ADC1 CLK OUT, depending on setting of FPGA CLKA SRC SEL, Section 5.16.4, see Figure 6–2 below). When the bit is read as logic '0' FPGA CLKA is in normal operation. When the bit is read as '1' FPGA CLKA is not detected. (Note that in this condition, the CDC7005 PLL may still run at some unknown frequency.) This bit also is present as bit 2 in the ADC Interrupt Status Register, Section 6.15.

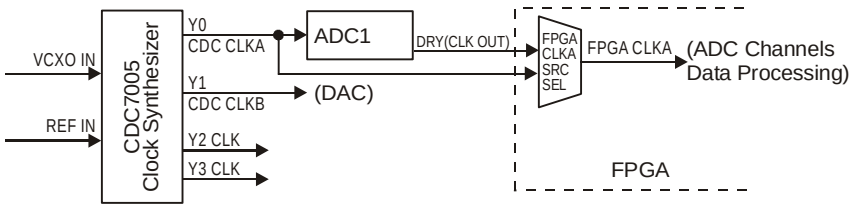


Figure 6–2: CDC/FPGA ADC Clock Logic

6.16.6 CDC CLKA LOCK Bit 1

This bit indicates the locked state of the CDC CLKA clock PLL (CDC7005 Y0 output, see Figure 6–2 above). When the bit is read as logic '0' the clock PLL is not locked. When the bit is read as '1' clock PLL is locked. This bit also is present, inverted, as bit 1 in the ADC Interrupt Status Register, Section 6.15.

6.16.7 ADC IODLY CTRL RDY Bit 0

This bit indicates the ready state of the memory IODELAY control for the ADC channel (1, 2, or 3) data input. When the bit is read as logic '0' IODE–LAY control is not ready – it is either held in reset or the 200–MHz Refer–ence clock is missing. When the bit is read as '1' IODELAY control is ready.

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6.17 RAM Controller Status Registers

There are three read–only RAM Controller Status Registers, one for each ADC data channel, 1, 2, and 3. These registers contain status bits indicating operating status of QDRII+ or DDR3 RAM FIFO for the associated ADC channel.

The following table shows the contents of this register. The subsections following the table provide descriptions of each bit in this register.

Table 6–17: RAM Controller Status Registers
ADC 1: RO @ BAR0+0x1003C
ADC 2: RO @ BAR0+0x1803C
ADC 3: RO @ BAR0+0x2003C

Bit	31 – 8							
Bit Name	Reserved							
Function	Write zeros, Mask when reading							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	RAM FIFO FULL	RAM FIFO AFL	RAM FIFO AEM	RAM FIFO EMP	DDR DET	DDR PHY INIT DONE	QDR DET	QDR CAL CMPLT
Function	0 = Not Full 1 = Full	0 = Not AFL 1 = Almost F	0 = Not AEM 1 = Almost E	0 = Not Empt 1 = Empty	0 = Not Det 1 = Detected	0 = Not done 1 = Complete	0 = Not det 1 = Detected	0 = Not done 1 = Complete
When reset, including power–up, the state of this register is unknown.								

6.17.1 RAM FIFO FULL Bit 7

This bit indicates the Full state of the QDRII+ or DDR3 RAM FIFO for the selected ADC channel (1, 2, or 3). When the bit is read as logic '0' the FIFO is not Full. When the bit is read as '1' the FIFO is Full.

6.17.2 RAM FIFO AFL Bit 6

This bit indicates the Almost Full state of the QDRII+ or DDR3 RAM FIFO for the selected ADC channel (1, 2, or 3). When the bit is read as logic '0' the FIFO is not Almost Full. When the bit is read as '1' the FIFO is Almost Full, indicating that there is one 64–bit word space left in the RAM FIFO.

This status bit also is present as bit 13 in the ADC Interrupt Status Register, Section 6.15.

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6.17 RAM Controller Status Registers (continued)

6.17.3 RAM FIFO AEM Bit 5

This bit indicates the Almost Empty state of the QDRII+ or DDR3 RAM FIFO for the selected ADC channel (1, 2, or 3). When the bit is read as logic '0' the FIFO is not Almost Empty. When the bit is read as '1' the FIFO is Almost Empty, indicating that there is only one 64−bit word in the RAM FIFO.

6.17.4 RAM FIFO EMP Bit 4

This bit indicates the Empty state of the QDRII+ or DDR3 RAM FIFO for the selected ADC channel (1, 2, or 3). When the bit is read as logic '0' the FIFO is not Empty. When the bit is read as '1' the FIFO is Empty.

This status bit also is present as bit 12 in the ADC Interrupt Status Register, Section 6.15.

6.17.5 DDR DET Bit 3

This bit indicates the presence of DDR3 SDRAM memory for the selected ADC channel (1, 2, or 3). When the bit is read as logic '0' the DDR3 memory board is not detected. When the bit is read as '1' the DDR3 memory board is detected.

6.17.6 DDR PHY INIT DONE Bit 2

This bit indicates the initialization state of the DDR3 SDRAM memory for the selected ADC channel (1, 2, or 3). When the bit is read as logic '0' initial−ization is in progress or did not successfully complete − access to the SDRAM is not yet possible. When the bit is read as '1' the SDRAM PHY ini−tialization is complete.

6.17.7 QDR DET Bit 1

This bit indicates the presence of QDRII+ SRAM for the selected ADC chan−nel (1, 2, or 3). When the bit is read as logic '0' the QDRII+ memory board is not detected. When the bit is read as '1' the QDRII+ memory board is detected.

6.17.8 QDR CAL CMPLT Bit 0

This bit indicates the initialization state of the QDRII+ SRAM for the selected ADC channel (1, 2, or 3). When the bit is read as logic '0' calibration is in progress or did not successfully complete − access to the RAM is not yet possible. When the bit is read as '1' the QDRII+ SRAM calibration is com−plete.

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6.18 RAM FIFO Count Registers

There are three ADC RAM FIFO Count Registers, one for each ADC channel, 1, 2, and 3. This read−only register returns the count of 16−bit data samples accessed in the QDRII+ or DDR3 RAM FIFO.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 6–18: RAM FIFO Count Registers
ADC 1: RO @ BAR0+0x10040
ADC 2: RO @ BAR0+0x18040
ADC 3: RO @ BAR0+0x20040

Bit	31	30 – 0
Bit Name	Reserved	CNT[30:0]
Function	Mask read	31−bit sample count
When reset, including power−up, the state of this register is unknown.		

CNT is the number of 16−bit data samples accessed in the QDRII+ or DDR3 RAM FIFO.

- For QDRII+ SRAM, this will always be a multiple of four 16−bit words as the memory burst is 4. If the number of 16−bit samples is not a multiple of 4, this number will include any pad words added at the end of an active gate period.
- For DDR3 SDRAM, this will always be a multiple of 16 16−bit words as the memory burst is 16 and the SDRAM is 32 bits wide. If the number of 16−bit samples is not a multiple of 16, this number will include any pad words added at the end of an active gate period.

NOTE: With DDR3 SDRAM, the FPGA adds a set of tag information to each acquisition gate period (for each Input Linked List definition, Section 3.2.2) equivalent to 32 samples. The count of data samples (CNT) present in the DDR3 RAM FIFO will include these added data sets.

When transferring the input samples from DDR3 RAM FIFO to PCIe, do not include the size of these additional data sets in the ADC DMA Linked List length (Section 3.2.4) as the FPGA automatically strips these data sets during the DMA transfer to PCIe.

For example, if you request an input transfer of 1024 samples in the input linked list, the count in this register would read 1056 (1024 + 32). To transfer this to PCIe you would specify an ADC DMA linked list length of 1024.

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6.19 ADC DMA Status Registers

There are three ADC DMA Status Registers, one for each ADC channel, 1, 2, and 3. The registers provide read–only status bits for DMA data transfers from each ADC channel to the PCIe interface.

The following table shows the bit layout of this register. The subsections following the table describe these bits.

Table 6–19: ADC DMA Status Registers
ADC 1: RO @ BAR0+0x1004C
ADC 2: RO @ BAR0+0x1804C
ADC 3: RO @ BAR0+0x2004C

Bit	31 – 16	15	14	13 – 9	8
Bit Name	Reserved	WAITING FOR ADV	ABORT IN PROGRESS	Reserved	NEXT LINK[8]
Function	Write zeros, Mask when reading	0 = Not wait 1 = Waiting	0 = Normal 1 = Abort	Write zeros, Mask when reading	(see below)
Bit	7 – 0				
Bit Name	NEXT LINK[7:0]				
Function	Link number of next link				
When reset, including power–up, the state of this register is unknown.					

6.19.1 WAITING FOR ADV Bit 15

This bit indicates the state of the DMA for the selected ADC channel (1, 2, or 3). When the bit is read as logic '0' the DMA is not waiting for DMA ADV (bit 0 in the ADC DMA Control Register, Section 6.12) to be toggled. When the bit is read as '1' DMA is waiting for DMA ADV bit to be toggled.

6.19.2 ABORT IN PROGRESS Bit 14

This bit indicates the state of the DMA abort for the selected ADC channel (1, 2, or 3). When the bit is read as logic '0' the DMA is not in an abort cycle (set by DMA ABORT, bit 6 in the ADC DMA Control Register, Section 6.12). When the bit is read as '1' a DMA abort is in progress; the bit will go back to a '0' once the abort is complete.

6.19.3 NEXT LINK Bits 8 – 0

This 9–bit value indicates the Link Definition index number, within the DMA Linked List RAM, of the next Link to be used for the current DMA transfer.

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6.20 Data Rate Detection Control Registers

There are three Data Rate Detection Control Registers, one for each ADC channel, 1, 2, and 3. The registers provide control bits for monitoring the PCI Express data transfer rate of the associated ADC channel.

The following table shows the bit layout of this register. The subsections following the table describe these bits.

Table 6–20: Data Rate Detection Control Registers
ADC 1: R/W @ BAR0+0x1005C
ADC 2: R/W @ BAR0+0x1805C
ADC 3: R/W @ BAR0+0x2005C

Bit	31	30	29	28 – 0
Bit Name	DATA RATE SYNC RST EN	DATA RATE RST	CLR DATA RATE PEAK	MON CLK PERIOD[28:0]
Function	0 = Disable 1 = Enable	0 = Run 1 = Reset	0 = Run 1 = Clear	Period (number of clock cycles)
All bits default to the logic '0' state at power on and reset				

6.20.1 DATA RATE SYNC RST EN Bit 31

This bit enables reset of the data rate monitoring for the selected ADC channel (1, 2, or 3) using the SYNC A signal. Clear the bit to logic '0' (its default state) to disable the reset from SYNC A. Set the bit to logic '1' to enable SYNC A to reset the data rate monitoring for the selected ADC channel.

6.20.2 DATA RATE RST Bit 30

This bit enables a reset of the data rate monitoring for the selected ADC channel (1, 2, or 3). Clear the bit to logic '0' (its default state) to place the data rate monitoring in run state. Set the bit to logic '1' to reset the data rate monitoring for the selected ADC channel.

6.20.3 CLR DATA RATE PEAK Bit 29

This bit clears the peak data rate value stored for the selected ADC channel (1, 2, or 3). Clear the bit to logic '0' (its default state) to enable data rate peak storage. Set the bit to logic '1' to clear the peak data rate value stored for the selected ADC channel (Peak Data Rate Detection Value Registers, Section 6.22).

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6.20 Data Rate Detection Control Registers (continued)

6.20.4 MON CLK PERIOD Bits 28 – 0

These bits specify the data rate monitoring period for the selected ADC channel (1, 2, or 3). This is specified in number of 250 MHz PCIe clock cycles, which determines the time period for counting the number of bytes transferred from the associated ADS5485 for this ADC channel. This value is used in calculating the data transfer rate for this ADC channel (Data Rate Detection Value Registers, Section 6.21).

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6.21 Data Rate Detection Value Registers

There are three Data Rate Detection Value Registers, one for each ADC channel, 1, 2, and 3. These read–only registers return the count of data transferred over PCIe from the associated ADS5485 during the specified period.

The following table shows this register's bit layout. The paragraphs following this table describe these bits.

Table 6–21: Data Rate Detection Value Registers
ADC 1: RO @ BAR0+0x10060
ADC 2: RO @ BAR0+0x18060
ADC 3: RO @ BAR0+0x20060

Bit	31 – 0
Bit Name	DATA RATE[31:0]
Function	Measured Data Rate
When reset, including power–up, the state of this register is unknown.	

DATA RATE is a 32–bit binary value that indicates the number of data bytes transferred over PCIe from the associated ADS5485 during the specified period. It is used to calculate the transfer rate of the associated ADC channel according to the following formula:

ADC transfer rate = (DATA RATE/(AVGR CLK PERIOD+1))*250 MBytes/sec

Where:
DATA RATE = value read from this register
AVGR CLK PERIOD = value set in Data Rate Detection Control register, Section 6.20

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6.22 Peak Data Rate Detection Value Registers

There are three Peak Data Rate Detection Value Registers, one for each ADC channel, 1, 2, and 3. These read–only registers return the maximum DATA RATE value measured since the last time this peak was cleared for the associated ADS5485.

The following table shows this register's bit layout. The paragraphs following this table describe these bits.

Table 6–22: Peak Data Rate Detection Value Registers
ADC 1: RO @ BAR0+0x10064
ADC 2: RO @ BAR0+0x18064
ADC 3: RO @ BAR0+0x20064

Bit	31 – 0
Bit Name	PEAK DATA RATE[31:0]
Function	Peak Data Rate
When reset, including power–up, the state of this register is unknown.	

PEAK DATA RATE is a 32–bit binary value that indicates the maximum DATA RATE value measured since the last time this peak was cleared for the associated ADS5485. The peak data rate value is cleared from this register using the CLR DATA RATE PEAK bit in the Data Rate Detection Control Register, Section 6.20, for this ADC channel.

Calculate the peak transfer rate of the ADC channel using the following formula:

Peak transfer rate = (PEAK DATA RATE/(AVGR CLK PERIOD+1))*250 MBytes/sec

Where:
PEAK DATA RATE = value read from this register
AVGR CLK PERIOD = value set in Data Rate Detection Control register

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Chapter 7: Digital to Analog Channel Registers

7.1 Overview

This chapter describes the default FPGA registers used for the digital to analog processing. All descriptions are given from an XMC baseboard processor's viewpoint. All registers are 32−bits wide, and the register addresses are in increments of 32 bits.

The 71620 has a single DAC data acquisition module that accepts data from the PCIe interface. The FPGA routes digital data from the PCIe interface by a DMA engine, or from the optional RAM memory, through a DAC output FIFO and then unpacked to the DAC5688 A and B inputs. The DAC data processing channel also loops back the DAC5688 A and B inputs to the ADC input modules.

The following is a block diagram of the digital to analog output data flow.

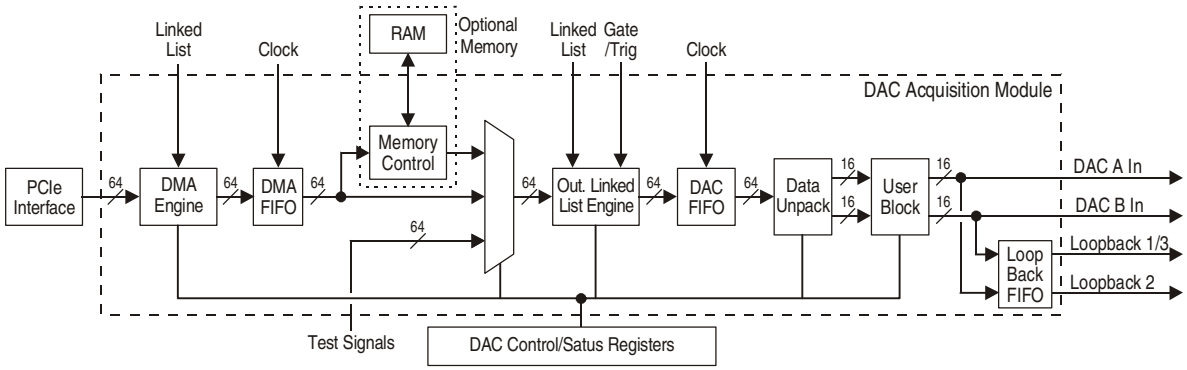


Figure 7–1: Digital to Analog Output Data Flow

Refer to Chapter 4 for the memory map of all 71620 registers.

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7.2 Channel Status/Power Management Register

The Channel Status/Power Management Register contains bits that provide power saving functions for elements of the DAC data processing channel.

The following table shows the contents of these registers. The subsections following the table provide descriptions of the bits in this register.

Table 7–1: Channel Status/Power Management Register
R/W @ BAR0+0x30000

Bit	31 – 9					8
Bit Name	Reserved					DMA DSBL
Function	Write zeros, Mask when reading					0 = Active 1 = Pwr dwn
Bit	**7**	**6**	**5**	**4**	**3 – 1 ***	**0 ***
Bit Name	MMCM PWR DWN	MEM CTRL DSBL	Reserved		ACQ TYPE	CHAN PRESENT
Function	0 = Active 1 = Pwr dwn	0 = Active 1 = Pwr dwn	Write zeros, Mask when reading		000 = No RAM 001 = QDRII+ SRAM 010 = DDR3 SDRAM 011 - 111 = User defined	0 = Not present 1 = Present

* These bits are Read Only.
Bits 5 to 8 default to the logic '0' state at power on and reset

7.2.1 DMA DSBL Bit 8

This bit selects the power saving mode for DMA access to the DAC channel. When the bit is cleared to logic '0' (its default state) this channel's DMA is active. When the bit is set to logic '1' this channel's DMA is shut down.

7.2.2 MMCM PWR DWN Bit 7

This bit selects the power saving mode for the DAC channel's memory clock PLL. When the bit is cleared to logic '0' (its default state) this module's clock PLL is active. When the bit is set to logic '1' this module's clock PLL is in power saving mode and the clock PLL for this module's memory and memory controller is powered down.

When the memory clock PLL is in power saving mode, the entire clock network in the FPGA is disabled rendering this channel inoperable. Both the DMA and the memory controller must be disabled prior to shutting down the clock.

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7.2 Channel Status/Power Management Register (continued)

7.2.3 MEM CTRL DSBL Bit 6

This bit selects the power saving mode for the DAC channel's memory controller. When the bit is cleared to logic '0' (its default state) this channel's memory controller and the associated memory (if present) are operational. When the bit is set to logic '1' this channel's memory controller is held in reset and the associated memory is held in power down.

When the controller is in power saving mode, the flow of data to the DMA for this channel is still possible through the internal bypass FIFO. Maximum data rate may be impacted due to the limited depth of this FIFO.

7.2.4 ACQ TYPE Bits 3 – 1

These three read–only bits indicate the type of data acquisition available for this DAC channel. The types of data acquisition are:

000	Data acquisition uses no external RAM
001	Data acquisition uses QDRII+ SRAM
010	Data acquisition uses DDR3 SDRAM
011 – 111	User defined

7.2.5 CHAN PRESENT Bit 0

This read–only bit indicates the FPGA code availability for this DAC data processing channel. When the bit is cleared to logic '0' (its default state) this channel is not present in the FPGA code. When the bit is set to logic '1' this channel is present in the FPGA code.

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7.3 Output Delay Tap Control Register

The Output Delay Tap Control Register determines the output delay of the digital data sent to the DAC5688.

The following table shows the contents of this register.

Table 7–2: Output Delay Tap Control Register
R/W @ BAR0+0x30004

Bit	31 – 5	4 – 0
Bit Name	Reserved	OUT TAP DLY[4:0]
Function	Write zeros, Mask when reading	N
All bits default to the logic '0' state at power on and reset		

OUT TAP DLY is a 5–bit binary value. It is used to specify an output delay according to the following formula:

Delay = **N** x 75 picoseconds

Depending on the setting of the FPGA CLKB SRC SEL bit in the Clock Control/Status Register, Section 5.16, this register should be set to the following value for proper oper–ation:

- For ‘CDC clock’ – set OUT TAP DLY to 0
- For ‘DAC clock’ – set OUT TAP DLY to 0

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7.4 DAC Data Control Register

The DAC Data Control Register contains bits that select the source and characteristics of the data sent to the DAC5688 from the DAC output FIFO.

The following table shows the contents of these registers. The subsections following the table provide descriptions of the bits in this register.

Table 7–3: DAC Data Control Register
R/W @ BAR0+0x30008

Bit	31 – 14	13	12	11	10	9	8
Bit Name	Reserved	SYNC SEL	UR LED EN	SYNC OUT EN	DAC RST	Reserved	
Function	Write zeros, Mask when reading	0 = Sync B 1 = Pulse	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Run 1 = Reset	Write zeros, Mask when reading	

Bit	7	6	5	4	3	2 – 0
Bit Name	OUT FIFO RST	Reserved				DATA SRC
Function	0 = Run 1 = Reset	Write zeros, Mask when reading				000 = From DMA or RAM 001 = Cos & Sin Test Signal 010 = Cos & Cos Test Signal 011 = Zero output 100 - 111 = Not used on 71620

All bits default to the logic '0' state at power on and reset

7.4.1 SYNC SEL Bit 13

This bit specifies the sync source for the DAC5688 sync signal. When this bit is cleared to logic '0' (its default state) the DAC5688 sync is the Sync B RCV signal selected by the Sync Bus Control Register 2, Section 5.18. When the bit is set to logic '1' the DAC5688 sync is a 1 clock–cycle pulse that is gener–ated on the rising edge of each active gate, either from the selected input gate or the linked list gates, depending on the source of the gate selected by the associated DAC Gate/Trigger Control Register Section 7.6.

7.4.2 UR LED EN Bit 12

This bit enables or disables the front panel DAC FIFO underrun LED (**UR**), Section 2.8.7. When the bit is cleared to logic '0' (its default state) the **UR** LED is disabled. When the bit is set to logic '1' the **UR** LED is enabled.

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7.4 DAC Data Control Register (continued)

7.4.3 SYNC OUT EN Bit 11

This bit enables the use of the onboard Sync B signal for the DAC5688 SYNC input. When the bit is cleared to logic '0' (its default state) the Sync B signal is not routed to the DAC5688. When the bit is set to logic '1' the Sync B signal is routed to the DAC5688 SYNC input.

7.4.4 DAC RST Bit 10

This bit resets the DAC5688. When the bit is cleared to logic '0' (its default state) the DAC5688 is in run. When the bit is set to logic '1' the DAC5688 is in reset.

7.4.5 OUT FIFO RST Bit 7

This bit resets the DAC output FIFO. When the bit is cleared to logic '0' (its default state) the FIFO is in run. When the bit is set to logic '1' the FIFO is in reset.

7.4.6 DATA SRC Bits 2 – 0

These three bits select the data source for the DAC output FIFO. The data sources are:

000 Normal data (from DMA or RAM)
001 Cos & Sin Test Signal
010 Cos & Cos Test Signal
011 Zero output
100 not used on 71620
101 not used on 71620
110 not used on 71620
111 not used on 71620

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7.5 DAC Rate Divider Register

The DAC Rate Divider Register divides the clock to the DAC output FIFO.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 7–4: DAC Rate Divider Register
R/W @ BAR0+0x3000C

Bit	31 – 16	15 – 0
Bit Name	Reserved	DEC[15:0]
Function	Write zeros, Mask when reading	16–bit rate divider 'N–1'
All bits default to the logic '0' state at power on and reset		

DEC is a 16–bit binary value, with bit 15 the MSB. To take every Nth sample, where N is any value between 1 and 4096, set this value to N–1.

This reduces the rate of data output from the DAC Output FIFO and into the DAC User Block. It is useful for user designs that interpolate the data. Otherwise set to zero for data to be sent at the DAC clock rate.

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7.6 DAC Gate/Trigger Control Register

The DAC Gate/Trigger Control Register contains bits that select the source and characteristics of the gate/trigger used to control writing data samples to the DAC5688 from the DAC output FIFO.

The following table shows the contents of these registers. The subsections following the table provide descriptions of the bits in this register.

Table 7–5: DAC Gate/Trigger Control Register
R/W @ BAR0+0x30010

	31 – 9							8
Bit Name	Reserved							OUT CNTRL LINKED LIST RST
Function	Write zeros, Mask when reading							0 = Run 1 = Reset
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Reserved				TRIG CLR	TRIG HOLD	GATE TRIG IN EN	TRIG MODE
Function	Write zeros, Mask when reading				0 = Run 1 = Clear	0 = None 1 = Hold	0 = Disable 1 = Enable	0 = Gate 1 = Trigger
All bits default to the logic '0' state at power on and reset								

7.6.1 OUT CNTRL LINKED LIST RST Bit 8

This bit resets the Output Controller Linked List for the DAC output FIFO. When the bit is cleared to logic '0' (its default state) the Linked List is in normal operation. When the bit is set to logic '1' the DMA Linked List Engine and FIFO are reset, and the Linked List is set to the starting Link Index Number specified in the DAC Output Controller Linked List Start Pointer Register, Section 7.7.

NOTE: A reset must be performed prior to starting a new linked list sequence, and a reset must be performed after programming the linked list definitions in the Linked List RAM.

Refer to Section 3.3.2 for description of the DAC Output Linked Lists.

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7.6 DAC Gate/Trigger Control Register (continued)

7.6.2 TRIG CLR Bit 3

This bit clears any active trigger for enabling DAC output FIFO writes. When this bit is cleared to logic '0' (its default state) the gate/trigger is in run. When this bit is set to logic '1', the system asynchronously clears any active trigger for this FIFO.

7.6.3 TRIG HOLD Bit 2

This bit enables a gate Hold after the trigger is received in Trigger mode (TRIG MODE bit 0 = 1, below) for the DAC output FIFO. When the bit is cleared to logic '0' (its default state) the selected gate is active (FIFO writes enabled) for the specified trigger length after the trigger (specified using the Output Controller Linked List), and then goes inactive (FIFO writes disabled). When the bit is set to logic '1' HOLD is enabled and the gate remains active (FIFO writes enabled) after the trigger is received until the Trigger is cleared using the TRIG CLR bit 3, above.

Note that when HOLD is enabled, you must set the Trigger Length to any number greater than zero.

7.6.4 GATE TRIG IN EN Bit 1

This bit enables the gate/trigger signal for the DAC output FIFO. When this bit is cleared to logic '0' (its default state), this bit inhibits the Gate signal (GATE B) from affecting an individual channel. Use this to disable the gate or trigger to channels that are not being used. This saves power and also keeps data from flowing into FIFOs on unused channels. When this bit is set to logic '1', the Gate signal is enabled.

7.6.5 TRIG MODE Bit 0

This bit selects Gate or Trigger mode for enabling DAC output FIFO writes. When this bit is cleared to logic '0' (its default state) Gate mode is selected. When this bit is set to logic '1', Trigger mode is selected and you must either set the trigger length using the Output Controller Linked List (as described in Section 3.3.2), or enable trigger Hold (TRIG HOLD bit 2, above).

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7.7 Output Controller Linked List Start Pointer Register

The Output Controller Linked List Start Pointer Register specifies the starting Link Number in the linked list for the DAC output FIFO trigger sequences.

The following tables show the format of these registers.

Table 7–6: Output Controller Linked List Start Pointer Register
R/W @ BAR0+0x30014

Bit	31 – 6	5 – 0
Bit Name	Reserved	OUT LL STRT ADDR[5:0]
Function	Write zeros, Mask when reading	Output Controller Linked List Start Index (N)
All bits default to the logic '0' state at power on and reset		

OUT LL STRT ADDR is a 6–bit binary value, with the most significant bit in bit 5 of the register. This value specifies the starting Link Definition Index number, within the Output Controller Linked List (Section 3.3.2), to be used for the next DAC output FIFO transfer. The linked list in this memory area contains all the trigger sequences required for this transfer.

When starting a new linked list sequence at this Link index number, you must reset the linked list using OUT CNTRL LINKED LIST RST (bit 8) in the DAC Gate/Trigger Con–trol Register, Section 7.6.

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7.8 RAM Capture Start Address Register

The RAM Capture Start Address Register specifies the RAM starting address of data to be transferred to QDRII+ SRAM or DDR3 SDRAM by the DAC DMA controller.

NOTE: This register is available only on 71620 boards with FPGA Code Revision 4 or greater, as identified in the FPGA Code Revision Register Section 5.11.

The following table shows this register's bit layout. The paragraphs following this table describe these bits.

Table 7–7: RAM Capture Start Address Register
R/W @ BAR0+0x30018

Bit	31 – 0
Bit Name	START ADDRESS[31:0]
Function	RAM Starting Address
When reset, including power–up, the state of this register is unknown.	

START ADDRESS is a 32–bit binary value that specifies the RAM starting address of data to be transferred to QDRII+ SRAM or DDR3 SDRAM. The RAM start address is specified by the value in this register. This value can be updated at any time while DMAs are not in progress, but can be used to control the start location where data is to be stored in the RAM before a DMA is kicked off.

NOTE: Each count in this start address register is equivalent to:

- One 32–bit RAM address for DDR3
- One 64–bit RAM address for QDRII+

This is useful to replace one stored waveform somewhere in RAM memory without having to DMA everything all over again. You can change this offset address, and kick off a DMA and thereby replace only one section of stored waveform data without affecting any other areas in the RAM.

To make the new start address active bit RAM CAPT ADDR LD (bit 11) in the RAM Control Register, Section 7.9, must be toggled.

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7.9 RAM Control Register

The RAM Control Register contains control bits for operation of QDRII+ SRAM or DDR3 SDRAM for the DAC data processing.

The following table shows the contents of this register. The subsections following the table provide descriptions of each bit in this register.

Table 7–8: RAM Control Register
R/W @ BAR0+0x3001C

Bit	31 – 12				11	10	9	8
Bit Name	Reserved				RAM CAPT ADDR LD	DDR3 DATA DIR	Reserved	
Function	Write zeros, Mask when reading				0 = Run 1 = Load	0 = Write 1 = Read	Write zeros, Mask when reading	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	RAM READ EN	Reserved	RAM PATH EN	RAM RST	DATA REPACK RST	Reserved		MEM CTLR RST
Function	0 = Inhibit 1 = Enable	Write zero, Mask read	0 = Disable 1 = Enable	0 = Run 1 = Reset	0 = Run 1 = Reset	Write zeros, Mask when reading		0 = Run 1 = Reset
All bits default to the logic '0' state at power on and reset.								

7.9.1 RAM CAPT ADDR LD Bit 11

This bit loads the RAM Capture Start Address. When toggled to a '1' then '0' the value specified in the RAM Capture Start Address Register (Section 7.8) is loaded into the RAM address counter. It must be toggled before the RAM address takes effect, and should not be toggled while a DMA is in progress.

NOTE: This bit is available only with FPGA Code Revision 4 or greater.

7.9.2 DDR3 DATA DIR Bit 10

This bit sets the capture data direction of the DDR3 SDRAM. When the bit is cleared to logic '0' (its default state) the direction is input, write to RAM. When the bit is set to '1' the direction is output, read from RAM.

7.9.3 RAM READ EN Bit 7

This bit enables the data flow of the data output from QDRII+ SRAM or DDR3 SDRAM to the DAC output FIFO. When the bit is cleared to logic '0' (its default state) data flow out of the RAM is disabled from starting. When the bit is set to '1' data from the RAM can flow to the DAC Output FIFO.

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7.9 RAM Control Register (continued)

7.9.4 RAM PATH EN Bit 5

This bit enables data flow from the DMA to the QDRII+ SRAM or DDR3 SDRAM. When this bit is cleared to logic '0' (its default state) RAM is bypassed and DMA data flows directly to the DAC output FIFO. When this bit is set to '1' data from the DMA flows into the RAM, and data from the RAM flows to the DAC output FIFO.

7.9.5 RAM RST Bit 4

This bit resets the QDRII+ SRAM or DDR3 SDRAM for the DAC channel and sets the address counters back to zero (0). When the bit is cleared to logic '0' (its default state) the RAM is in run. When the bit is set to '1' the RAM is in reset. Reset before a capture to clear the previous capture data, data pointers, and data count.

7.9.6 DATA REPACK RST Bit 3

This bit resets the Data Re−packer for the DAC channel. When the bit is cleared to logic '0' (its default state) the Data Re−packer is in run. When the bit is set to '1' the Data Re−packer is in reset.

PCIe completion packets will have starting and/or ending data words with only one half (32−bits) of the 64−bit data valid. Therefore data going into the QDRII+ SRAM or DDR3 SDRAM and/or the DAC output FIFO must be repacked to 64−bit values. As a result, if the data written to RAM is not a multiple of the memory controller input width, data can be left over in the re−packer. This bit resets the re−packer to flush the left over data. A status bit is provided in the RAM Controller Status Register (Section 7.16) to indi−cate that data is left over in the re−packer.

7.9.7 MEM CTLR RST Bit 0

This bit resets the QDRII+ SRAM or DDR3 SDRAM memory controller for the DAC channel. When the bit is cleared to logic '0' (its default state) the memory controller is in run. When the bit is set to '1' the memory controller is in reset. After being reset, the memory controller will reinitialize and recalibrate. Note: The memory controller is also reset by LRST_N from the PCIe core and power−on reset.

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7.10 Output Gate Delay Register

The Output Gate Delay Register allows you to program a time delay for the DAC Gate signal. This allows adjustment in output timing to compensate for the latency period in acquiring the data from memory or DMA.

The following table shows the contents of this register. The subsections following the table provide descriptions of each bit in this register.

Table 7–9: Output Gate Delay Register
R/W @ BAR0+0x30020

	31 – 7	6 – 0
Bit Name	Reserved	DAC GATE DLY [6:0]
Function	Write zeros, Mask when reading	DAC Gate Delay (number of clock cycles)
All bits default to the logic '0' state at power on and reset		

DAC GATE DELAY is specified in number of clock cycles. This is a delay in number of DAC CLOCK cycles that the DAC output waits before starting the read gate from the DAC FIFO to the DAC5688.

Depending on the type of memory used for the DAC channel, this register should be set to the following value for proper operation:

- For QDRII+ SRAM – set DAC GATE DLY to 0x30
- For DDR3 SDRAM – set DAC GATE DLY to 0x6F

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7.11 DAC DMA Control Register

The DAC DMA Control Register provides control bits for DMA data transfers to the DAC channel (DAC DMA FIFO) from the PCIe interface.

The following table shows the bit layout of this register. The subsections following the table describe these bits.

Table 7–10: DAC DMA Control Register
R/W @ BAR0+0x30028

Bit	31 – 16							
Bit Name	Reserved							
Function	Write zeros, Mask when reading							
Bit	**15**	**14 – 13**		**12 – 10**			**9**	**8**
Bit Name	BYTE SWAP	DMA AT		DMA TC			DMA ATTR1	DMA ATTR0
Function	0 = No swap 1 = Swap	00 = Default/Untranslated 01 = Translation request 10 = Translated 11 = Reserved		000 = Best effort service class 001-111 = Differentiated service class			0 = Default 1 = Relaxed	0 = Default 1 = No Snoop
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	Reserved	DMA ABORT	Reserved	DMA RST	Reserved			DMA ADV
Function	Write 0, Mask read	0 = Run 1 = Abort	Write 0, Mask read	0 = Run 1 = Reset	Write zeros, Mask when reading			0 = No action 1 = Advance
All bits default to the logic '0' state at power on and reset								

7.11.1 BYTE SWAP Bit 15

This bit sets byte swap mode of the DMA transfer for the DAC channel. When the bit is cleared to logic '0' (its default state) byte swapping is dis–abled. When the bit is set to '1' byte swapping is enabled for DMA transfers from the PCIe interface. Bytes are swapped within each 64–bit word.

No swap: 0, 1, 2, 3, 4, 5, 6, 7
Swap: 7, 6, 5, 4, 3, 2, 1, 0

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7.11 DAC DMA Control Register (continued)

7.11.2 DMA AT Bits 14 – 13

These two bits select the Address Type of the PCI Express Packet transferred by DMA for the DAC channel. These address types are defined by the PCI Express Base Specification:

00 Default/Untranslated
01 Translation Request
10 Translated
11 Reserved

7.11.3 DMA TC Bits 12 – 10

These three bits select the Traffic Class of the PCI Express Packet transferred by DMA for the DAC channel. These traffic classes are defined by the PCI Express Base Specification:

000 TC0: Best Effort service class (General Purpose I/O)
001 – 111 TC1–TC7: Differentiated service classes

7.11.4 DMA ATTR1 Bit 9

This bit selects the Relaxed Ordering Attribute of the PCI Express Packet transferred by DMA for the DAC channel. These attributes are defined by the PCI Express Base Specification. When the bit is cleared to logic '0' (its default state) the packet is in Default Ordering (PCI Strongly Ordered Model). When the bit is set to '1' the packet is in Relaxed Ordering (PCI–X Relaxed Ordering Model).

7.11.5 DMA ATTR0 Bit 8

This bit selects the No Snoop Attribute of the PCI Express Packet transferred by DMA for the DAC channel. These attributes are defined by the PCI Express Base Specification. When the bit is cleared to logic '0' (its default state) the packet is in default (Hardware enforced cache coherency expected). When the bit is set to '1' the packet is in No Snoop (Hardware enforced cache coherency not expected).

7.11.6 DMA ABORT Bit 6

This bit aborts the DMA engine for the DAC channel. When toggled to a '1' then '0' a DMA abort sequence will commence. Any DMA packets that have already been constructed will be allowed to be transmitted. All new DMA activity will be inhibited. When all packets have been transmitted, a DMA reset will automatically be generated.

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7.11 DAC DMA Control Register (continued)

7.11.7 DMA RST Bit 4

This bit resets the DMA engine for the DAC channel. When the bit is cleared to logic '0' (its default state) the DMA is in run. When the bit is set to '1' the DMA engine is in reset.

7.11.8 DMA ADV Bit 0

This bit advances the DMA linked list for the DAC channel DMA linked list. When the bit is cleared to logic '0' (its default state) the DMA linked list does not advance. When the bit is toggled to '1' the DMA linked list is in Advance. At the rising edge of this bit the linked list will advance if it is waiting. The first link must be kicked off by this bit and any other link that is programmed to not execute automatically also will be kicked off by toggling this bit.

Refer to Section 3.3.1 for description of the DAC DMA Linked Lists.

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7.12 DAC Interrupt Enable Register

The DAC Interrupt Enable Register contains enable bits for each DAC channel interrupt. Each bit enables or disables the generation of an interrupt input to the DAC Interrupt Status Register, Section 7.14.

The following table shows the enable bit layout of this register. Table 7–12, on the next page, describes the interrupt condition associated with each bit.

Table 7–11: DAC Interrupt Enable Register
R/W @ BAR0+0x3002C

Bit	31 – 16							
Bit Name	Reserved							
Function	Write zeros, Mask when reading							
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Bit Name	ALL DATA RCVD	POISONED TLP	REAL TIME LOST	BAD TRIGGER	Reserved		MEM CLK IN STOPPED	MEM MMCM NOT LOCK
Function	0 = Disable Interrupt 1 = Enable Interrupt							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Bit Name	Reserved						DAC OUT FIFO FULL	DAC OUT FIFO EMP
Function	0 = Disable Interrupt 1 = Enable Interrupt							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	CHAIN END	LINK END	GATE END	GATE START	TRIG CMPLT	FPGA CLKB NOT DET	CDC CLKB NOT LOCK	DAC5688 NOT LOCK
Function	0 = Disable Interrupt 1 = Enable Interrupt							
All bits default to the logic '0' state at power on and reset								

Each bit of this register enables or disables the generation of an interrupt for an interrupt condition. Setting the bit associated with a given interrupt to logic '1' enables the generation of an interrupt to the Interrupt Flag Register, Section 5.3, when that interrupt condition occurs from the DAC Interrupt Status Register, Section 7.14. When an enable bit is cleared to logic '0' (its default state) the interrupt will not be generated by the defined interrupt condition.

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7.12 DAC Interrupt Enable Register (continued)

The following table describes the interrupt condition associated with each bit of the DAC Interrupt registers.

Table 7–12: DAC Interrupt Register Bits

Bit Name	Bit Position	Interrupt Function
ALL DATA RCVD	23	This interrupt signals that all requested DACDMA data has been received. See DAC DMA Status Register bit 12, Section 7.18.
POISONED TLP	22	This interrupt signals that the PCI Express receiver has received a poisoned Transaction Layer Protocol error.
REAL TIME LOST	21	This interrupt signals that the DAC output FIFO went empty (ran out of data).
BAD TRIGGER	20	This interrupt signals a trigger occurrence before the end of the active linked list gates/triggers.
MEM CLK IN STOPPED	17	This interrupt signals a memory clock stopped condition. See ODelay and Clock Status Register bit 6, Section 7.15.
MEM MMCM NOT LOCK	16	This interrupt signals a memory MMCM clock PLL not locked. See ODelay and Clock Status Register bit 5, Section 7.15.
DAC OUT FIFO FULL, DAC OUT FIFO EMP	9, 8	Each of these interrupts signals a FIFO Empty or Full condition, respectively, from the DAC output FIFO.
CHAIN END, LINK END	7, 6	Each of these interrupts is the end of a link or end of the full chain of links, respectively, of a DMA transfer linked list.
GATE END, GATE START	5, 4	Each of these interrupts is the start or end, respectively, of a programmed Gate period.
TRIG CMPLT	3	This interrupt signals a trigger complete, which occurs at the end of the active linked list gate/trigger occurrences. Note that this does not necessarily mean that the data transfer that was started by the trigger/gate has completed, only that the trigger/gate is complete.
FPGA CLKB NOT DET	2	This interrupt signals an FPGA CLKB clock not detected. See ODelay and Clock Status Register bit 2, Section 7.15.
CDC CLKB NOT LOCK	1	This interrupt signals a CDC7005 CLKB clock PLL not locked. See ODelay and Clock Status Register bit 1, Section 7.15.
DAC5688 NOT LOCK	0	This interrupt signals a DAC5688 clock PLL not locked.

These bit assignments and definitions apply to DAC Interrupt Enable Register, Section 7.12, DAC Interrupt Status Register, Section 7.14, and DAC Interrupt Flag Register, Section 7.13

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7.13 DAC Interrupt Flag Register

The DAC Interrupt Flag Register contains one read/clear flag bit associated with each DAC interrupt condition (the same bit associations as the DAC Interrupt Enable Register, Section 7.12; Table 7–12, on page 217, describes the interrupt condition associated with each bit. The following table shows the flag bit layout of this register.

Table 7–13: DAC Interrupt Flag Register
R/Clr @ BAR0+0x30030

Bit	31 –24							
Bit Name	Reserved							
Function	Write zeros, Mask when reading							
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Bit Name	ALL DATA RCVD	POISONED TLP	REAL TIME LOST	BAD TRIGGER	Reserved		MEM CLK IN STOPPED	MEM MMCM NOT LOCK
Function	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Bit Name	Reserved						DAC OUT FIFO FULL	DAC OUT FIFO EMP
Function	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	CHAIN END	LINK END	GATE END	GATE START	TRIG CMPLT	FPGA CLKB NOT DET	CDC CLKB NOT LOCK	DAC5688 NOT LOCK
Function	**Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch							

IMPORTANT! When reset, including power–up, the state of this register is unknown.
You should clear this register before using it, by writing '1's into all bits.

Read: Each flag bit in this register latches an interrupt occurrence. A logic '1' in any flag bit in this register indicates that an interrupt has occurred. Note that when any status bit in the DAC Interrupt Status Register, Section 7.14, changes to logic '1' the corresponding flag bit in this register will also be set to logic '1'. However, when a status bit in the DAC Interrupt Status Register clears from logic '1' to logic '0', the corresponding latched flag bit in this register does not clear, but remains at logic '1'.

Clear: Since these bits latch in response to an interrupt, to detect subsequent interrupts, you must clear the flag bits in this register. To clear any flag bit in this register that is set to '1' you must write a '1' to that bit.

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7.14 DAC Interrupt Status Register

The DAC Interrupt Status Register contains one read–only status bit associated with each DAC interrupt condition (the same bit associations as the DAC Interrupt Enable Register, Section 7.12); Table 7–12, on page 217, describes the interrupt condition associated with each bit.

The following table shows the status bit layout of this register.

Table 7–14: DAC Interrupt Status Register
RO @ BAR0+0x30034

Bit	31 –24							
Bit Name	Reserved							
Function	Mask when reading							
Bit	23	22	21	20	19	18	17	16
Bit Name	ALL DATA RCVD	POISONED TLP	REAL TIME LOST	BAD TRIGGER	Reserved		MEM CLK IN STOPPED	MEM MMCM NOT LOCK
Function	0 = No Interrupt 1 = Interrupt condition asserted							
Bit	15	14	13	12	11	10	9	8
Bit Name	Reserved						DAC OUT FIFO FULL	DAC OUT FIFO EMP
Function	0 = No Interrupt 1 = Interrupt condition asserted							
Bit	7	6	5	4	3	2	1	0
Bit Name	CHAIN END	LINK END	GATE END	GATE START	TRIG CMPLT	FPGA CLKB NOT DET	CDC CLKB NOT LOCK	DAC5688 NOT LOCK
Function	0 = No Interrupt 1 = Interrupt condition asserted							
When reset, including power–up, the state of this register is unknown.								

When a status bit in this register changes to '1' the corresponding flag bit in the DAC Interrupt Flag Register, Section 7.13, is set to '1'. A status bit in this register clears to logic '0' when that interrupt condition clears, whereas the associated flag bit in the DAC Interrupt Flag Register, Section 7.13, remains latched at '1' until it is cleared.

If the corresponding enable bit in the DAC Interrupt Enable Register, Section 7.12, has been set to logic '1', then a status bit transition from logic '0' to logic '1' will also generate an interrupt to the Interrupt Flag Register, Section 5.3. If you do not want an interrupt to occur and have set the corresponding interrupt enable bit to '0', you may poll DAC Interrupt Flag Register flag bit, Section 7.13, to determine if such an event has occurred. The DAC Interrupt Flag Register will latch the event regardless of the setting of the interrupt enable bit.

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7.15 ODelay and Clock Status Register

The ODelay and Clock Status Register provides status bits for the clocks and input delays associated with the DAC channel.

The following table shows the bit layout of this register. The subsections following the table describe these bits.

Table 7–15: ODelay and Clock Status Register
RO @ BAR0+0x30038

Bit	31 – 8							
Bit Name	Reserved							
Function	Mask when reading							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bit Name	MEM CLK FB STOP	MEM CLK IN STOP	MEM MMCM LOCK	MEM IODLY CTRL RDY	Reserved	FPGA CLKB NOT DET	CDC CLKB LOCK	DAC IODLY CTRL RDY
Function	0 = Not stop 1 = Stopped	0 = Not stop 1 = Stopped	0 = Not lock 1 = Locked	0 = Not rdy 1 = Ready	Mask read	0 = Normal 1 = Not det.	0 = Not lock 1 = Locked	0 = Not rdy 1 = Ready
When reset, including power–up, the state of this register is unknown.								

7.15.1 MEM CLK FB STOP Bit 7

This bit indicates the operating state of the memory clock output for the DAC channel. When the bit is read as logic '0' the Memory Clock is not stopped. When the bit is read as '1' Memory Clock output is stopped. This indicates a problem with the PLL or the Memory clock oscillator.

7.15.2 MEM CLK IN STOP Bit 6

This bit indicates the operating state of the memory clock input for the DAC channel. When the bit is read as logic '0' the Memory Clock is not stopped. When the bit is read as '1' Memory Clock is stopped. This indicates a prob–lem with the PLL or the Memory clock oscillator. This status bit also occurs as bit 17 in the DAC Interrupt Status Register, Section 7.14.

7.15.3 MEM MMCM LOCK Bit 5

This bit indicates the locked state of the memory clock PLL for the DAC channel. When the bit is read as logic '0' the Memory Clock PLL is not locked. When the bit is read as '1' Memory Clock PLL is locked. This status bit also occurs, inverted, as bit 16 in the DAC Interrupt Status Register, Sec–tion 7.14.

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7.15 ODelay and Clock Status Register (continued)

7.15.4 MEM IODLY CTRL RDY Bit 4

This bit indicates the ready state of the memory IODELAY control for the DAC channel. When the bit is read as logic '0' IODELAY control is not ready – it is either held in reset or the 200–MHz Reference clock is missing. When the bit is read as '1' IODELAY control is ready.

7.15.5 FPGA CLKB NOT DET Bit 2

This bit indicates the operating state of the FPGA CLKB clock for the DAC channel (either CDC7005 CLKB or DAC5688 CLK OUT, depending on FPGA CLKB SRC SEL, Section 5.16.4, see Figure 7–2 below). When the bit is read as logic '0' the FPGA CLKB is in normal operation. When the bit is read as '1' FPGA CLKB is not detected. (Note that in this condition, the CDC7005 PLL may still run at some unknown frequency.) This bit also occurs as bit 2 in the DAC Interrupt Status Register, Section 7.14.

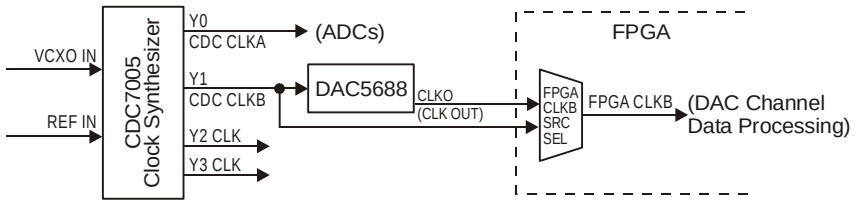


Figure 7–2: CDC/FPGA DAC Clock Logic

7.15.6 CDC CLKB LOCK Bit 1

This bit indicates the locked state of the CDC CLKB clock PLL (CDC7005 Y1 output, see Figure 7–2 above). When the bit is read as logic '0' the clock PLL is not locked. When the bit is read as '1' the clock PLL is locked. This bit also occurs, inverted, as bit 1 in the DAC Interrupt Status Register, Section 7.14.

7.15.7 DAC IODLY CTRL RDY Bit 0

This bit indicates the ready state of the IODELAY control for the DAC channel. When the bit is read as logic '0' IODELAY control is not ready – it is either held in reset or the 200–MHz Reference clock is missing. When the bit is read as '1' IODELAY control is ready.

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7.16 RAM Controller Status Register

The read–only RAM Controller Status Register contains status bits indicating operating status of QDRII+ SRAM or DDR3 SDRAM memory for the DAC channel.

The following table shows the contents of this register. The subsections following the table provide descriptions of each bit in this register.

Table 7–16: RAM Controller Status Register
RO @ BAR0+0x3003C

Bit	31 – 13	12	11	10	9	8
Bit Name	Reserved	REPACK NOT EMP	Reserved			
Function	Write zeros, Mask when reading	0 = Empty 1 = Not Empt	Write zeros, Mask when reading			
Bit	**7 – 4**		**3**	**2**	**1**	**0**
Bit Name	Reserved		DDR DET	DDR PHY INIT DONE	QDR DET	QDR CAL CMPLT
Function	Write zeros, Mask when reading		0 = Not det 1 = Detected	0 = Not done 1 = Complete	0 = Not det 1 = Detected	0 = Not done 1 = Complete
When reset, including power–up, the state of this register is unknown.						

7.16.1 REPACK NOT EMP Bit 12

This bit indicates the state of the Data Re–packer for the DAC channel. When the bit is read as logic '0' the re–packer is empty. When the bit is read as '1' the re–packer is not empty.

PCIe completion packets will have starting and/or ending data words with only one half (32–bits) of the 64–bit data valid. Therefore data going into the RAM and/or the DAC output FIFO must be repacked to 64–bit values. As a result, if the data written to RAM is not a multiple of the memory con–troller input width, data can be left over in the re–packer. This bit is pro–vided to indicate that data is left over in the re–packer.

7.16.2 DDR DET Bit 3

This bit indicates the presence of DDR3 SDRAM memory for the DAC chan–nel. When the bit is read as logic '0' a DDR3 memory board is not detected. When the bit is read as '1' a DDR3 memory board is detected.

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7.16 RAM Controller Status Register (continued)

7.16.3 DDR PHY INIT DONE Bit 2

This bit indicates the initialization state of the DDR3 SDRAM memory for the DAC channel. When the bit is read as logic '0' initialization is in prog− ress or did not successfully complete − access to the SDRAM is not yet pos− sible. When the bit is read as '1' the SDRAM PHY initialization is complete.

7.16.4 QDR DET Bit 1

This bit indicates the presence of QDRII+ SRAM for the DAC channel. When the bit is read as logic '0' a QDRII+ memory board is not detected. When the bit is read as '1' a QDRII+ memory board is detected.

7.16.5 QDR CAL CMPLT Bit 0

This bit indicates the initialization state of the QDRII+ SRAM for the DAC channel. When the bit is read as logic '0' calibration is in progress or did not successfully complete − access to the RAM is not yet possible. When the bit is read as '1' the RAM calibration is complete.

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7.17 RAM Capture Count Register

There read–only RAM Capture Count Register returns the count of 32–bit data samples present in the QDRII+ SRAM or DDR3 SDRAM.

The following table shows the bit layout of this register. The paragraphs following the table provide descriptions of these bits.

Table 7–17: RAM Capture Count Register
RO @ BAR0+0x30044

Bit	31 – 28	27 – 0
Bit Name	Reserved	CAPTURE CNT[27:0]
Function	Mask when reading	28–bit sample count
When reset, including power–up, the state of this register is unknown.		

CAPTURE CNT is the number of 32–bit data samples present in the RAM.

- For QDRII+ SRAM, this will always be a multiple of two 32–bit words as the memory burst is four 16–bit words.
- For DDR3 SDRAM, this will always be a multiple of eight 32–bit words as the memory burst is eight 16–bit words.

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7.18 DAC DMA Status Register

The DAC DMA Status Register provides read–only status bits for DMA data transfers to the DAC channel (DAC DMA FIFO) from the PCIe interface.

The following table shows the bit layout of this register. The subsections following the table describe these bits.

Table 7–18: DAC DMA Status Register
RO @ BAR0+0x3004C

Bit	31 – 16	15	14	13	12	11 – 9	8
Bit Name	Reserved	WAITING FOR ADV	ABORT IN PROGRESS	Reserved	ALL DATA RCVD	Reserved	NEXT LINK[8]
Function	Write zeros, Mask when reading	0 = Not wait 1 = Waiting	0 = Normal 1 = Abort	Write 0, Mask read	0 = Not rcvd 1 = Received	Write zeros, Mask read	(see below)
Bit	7 – 0						
Bit Name	NEXT LINK[7:0]						
Function	Link number of next link						
When reset, including power–up, the state of this register is unknown.							

7.18.1 WAITING FOR ADV Bit 15

This bit indicates the state of the DMA for the DAC channel. When the bit is read as logic '0' the DMA is not waiting for DMA ADV (bit 0 in the DAC DMA Control Register, Section 7.11) to be toggled. When the bit is read as '1' DMA is waiting for DMA ADV bit to be toggled.

7.18.2 ABORT IN PROGRESS Bit 14

This bit indicates the state of the DMA abort for the DAC channel. When the bit is read as logic '0' the DMA is not in an abort cycle (set by DMA ABORT, bit 6 in the DAC DMA Control Register, Section 7.11). When the bit is read as '1' a DMA abort is in progress; the bit will go back to a '0' once the abort is complete.

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7.18 DAC DMA Status Register (continued)

7.18.3 ALL DATA RCVD Bit 12

This bit indicates the state of the DMA data for the DAC channel. When the bit is read as logic '0' the DMA is waiting for the transfer completion. When the bit is read as '1' all requested DMA data has been received by the DAC DMA FIFO.

NOTE: This status bit will read 0 (not received) only momentarily when you start a new DMA transfer using the DMA ADV bit (DAC DMA Control Register, Section 7.11), then change back to 1 signalling the end of DMA transfer. It stays at 1 after a reset (DMA RST) until the next DMA ADV starts a new transfer.

NOTE: If you start a DMA linked list sequence (see Section 3.3.1) with a DMA link that pre−fills the DAC DMA FIFO prior to starting the output transfer gate, the maximum pre−fill transfer size is 8192 bytes. If it is greater, this ALL DATA RVCD flag may not be set.

This status bit also occurs as bit 23 in the DAC Interrupt Status Register, Section 7.14.

7.18.4 NEXT LINK Bits 8 – 0

This 9−bit value indicates the Link Definition index number, within the DMA Linked List RAM, of the next Link to be used for the current DMA transfer.

Refer to Section 3.3.1 for description of the DAC DMA Linked Lists.

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7.19 DAC Serial Address Register

The DAC Serial Address Register specifies the address of the DAC5688 internal register to read from or write to using the DAC Serial Data Register, Section 7.20.

NOTE: Set the DAC5688 register address first before reading or writing to the DAC Serial Data Register.

The following table shows the contents of the register. The paragraph following the table provide descriptions of the bits in this register

Table 7–19: DAC Serial Address Register
R/W @ BAR0+0x30054

	31 – 6	5 *	4	3	2	1	0
Bit Name	Reserved	SERIAL BUSY	SER ADDR [4:0]				
Function	Write zeros, Mask when reading	0 = Not busy 1 = Busy	Offset of DAC register to write to				

* These bits are Read Only
All bits default to the logic '0' state at power on and reset.

7.19.1 SERIAL BUSY Bit 5

This read–only bit indicates the status of the DAC serial data transfer. When read as logic '0' the last transfer is complete. When read as logic '1' the transfer is still in progress (busy).

NOTE: Do not write to the DAC Serial Data Register, Section 7.20, while the SERIAL BUSY bit is '1'.

7.19.2 SER ADDR[4:0] Bits 4 – 0

SER ADDR is the DAC5688 control register address. Set these bits to the (address) offset of the DAC5688 internal control register to write to. Refer to the Texas Instruments DAC5688 data sheet (see Section 1.13) for the content of these registers. See Table 7–20 on the next page for a list of the DAC5688 internal control register addresses.

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7.19 DAC Serial Address Register (continued)

The following table lists all internal control registers in the DAC5688 and their address offset.

Table 7–20: DAC5688 Register Addresses

Register Name	Address
STATUS0	**0x00**
CONFIG1	**0x01**
CONFIG2	**0x02**
CONFIG3	**0x03**
CONFIG4	**0x04**
CONFIG5	**0x05**
CONFIG6	**0x06**
CONFIG7	**0x07**
CONFIG8	**0x08**
CONFIG9	**0x09**
CONFIG10	**0x0A**
CONFIG11	**0x0B**
CONFIG12	**0x0C**
CONFIG13	**0x0D**
CONFIG14	**0x0E**
CONFIG15	**0x0F**
CONFIG16	**0x10**
CONFIG17	**0x11**
CONFIG18	**0x12**
CONFIG19	**0x13**
CONFIG20	**0x14**
CONFIG21	**0x15**
CONFIG22	**0x16**
CONFIG23	**0x17**
CONFIG24	**0x18**
CONFIG25	**0x19**
CONFIG26	**0x1A**
CONFIG27	**0x1B**
CONFIG28	**0x1C**
CONFIG29	**0x1D**
CONFIG30	**0x1E**

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7.20 DAC Serial Data Register

The DAC Serial Address Register reads from or writes to a selected DAC5688 internal control register. Use the DAC Serial Address Register, Section 7.19, to specify the DAC register address that you wish to write to/read from.

NOTE: Set the DAC Serial Address Register, Section 7.19, first before reading or writing to the DAC Serial Data Register.

NOTE: Do not write to this register while the SERIAL BUSY bit in the DAC Serial Address Register, Section 7.19, is '1'.

The following table shows the contents of the register. The paragraph following the table provide descriptions of the bits in this register

Table 7–21: DAC Serial Data Register
R/W @ BAR0+0x30058

Bit	31 – 8							
Bit Name	Reserved							
Function	Write zeros, Mask when reading							
	7	6	5	4	3	2	1	0
Bit Name	SER DATA[7:0]							
Function	Data read from/write to the DAC register							
All bits default to the logic '0' state at power on and reset.								

Use this register to write or read the value of the DAC internal control register pointed to by SER ADDR[4:0], Section 7.19.

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7.21 Data Rate Detection Control Register

The Data Rate Detection Control Register provides control bits for monitoring the input data transfer rate over PCIe of the DAC channel. The following table shows the bit lay–out of this register. The subsections following the table describe these bits.

Table 7–22: Data Rate Detection Control Register
R/W @ BAR0+0x3005C

Bit	31	30	29	28 – 0
Bit Name	DATA RATE SYNC RST EN	DATA RATE RST	CLR DATA RATE PEAK	MON CLK PERIOD[28:0]
Function	0 = Disable 1 = Enable	0 = Run 1 = Reset	0 = Run 1 = Clear	Period (number of clock cycles)
All bits default to the logic '0' state at power on and reset				

7.21.1 DATA RATE SYNC RST EN Bit 31

This bit enables a reset of the data rate monitoring for the DAC channel using the SYNC B signal. Clear the bit to logic '0' (its default state) to disable the reset from SYNC B. Set the bit to logic '1' to enable SYNC B to reset the data rate monitoring for the DAC channel.

7.21.2 DATA RATE RST Bit 30

This bit enables a reset of the data rate monitoring for the DAC channel. Clear the bit to logic '0' (its default state) to place the data rate monitoring in run state. Set the bit to logic '1' to reset the data rate monitoring for the DAC channel.

7.21.3 CLR DATA RATE PEAK Bit 29

This bit clears the peak data rate value stored for the DAC channel. Clear the bit to logic '0' (its default state) to enable data rate peak storage. Set the bit to logic '1' to clear the peak data rate value stored for the DAC channel (Peak Data Rate Detection Value Registers, Section 7.23).

7.21.4 MON CLK PERIOD Bits 28 – 0

These bits specify the data rate monitoring period for the DAC channel. This is specified in number of clock cycles, which determines the time period for counting the number of bytes transferred to the DAC5688. This value is used in calculating the data transfer rate for the DAC channel (Data Rate Detection Value Registers, Section 7.22).

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7.22 Data Rate Detection Value Register

The Data Rate Detection Value Register returns the count of data transferred to the DAC5688 during the specified period.

The following table shows this register's bit layout. The paragraphs following this table describe these bits.

Table 7–23: Data Rate Detection Value Register
RO @ BAR0+0x30060

Bit	31 – 0
Bit Name	DATA RATE[31:0]
Function	Measured Data Rate
When reset, including power–up, the state of this register is unknown.	

DATA RATE is a 32–bit binary value that indicates the number of data bytes transferred from the DAC5688 during the specified period. It is used to calculate the transfer rate of the DAC channel according to the following formula:

DAC transfer rate = (DATA RATE/(AVGR CLK PERIOD+1))*250

Where:
DATA RATE = value read from this register
AVGR CLK PERIOD = value set in Data Rate Detection Control register, Section 7.21

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7.23 Peak Data Rate Detection Value Register

The Peak Data Rate Detection Value Register returns the maximum DATA RATE value measured since the last time this peak was cleared for the DAC channel.

The following table shows this register's bit layout. The paragraphs following this table describe these bits.

Table 7–24: Peak Data Rate Detection Value Register
RO @ BAR0+0x30064

Bit	31 – 0
Bit Name	PEAK DATA RATE[31:0]
Function	Peak Data Rate
When reset, including power–up, the state of this register is unknown.	

PEAK DATA RATE is a 32–bit binary value that indicates the maximum DATA RATE value measured since the last time this peak was cleared for the DAC channel. The peak data rate value is cleared from this register using the CLR DATA RATE PEAK bit in the DAC Data Rate Detection Control Register, Section 7.21.

Calculate the peak transfer rate of the DAC channel using the following formula:

Peak transfer rate = (PEAK DATA RATE/(AVGR CLK PERIOD+1))*250 MBytes/sec

Where:

PEAK DATA RATE = value read from this register

AVGR CLK PERIOD = value set in Data Rate Detection Control register, Section 7.21

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Appendix A: PCI Configuration Space Registers

A.1 Introduction

This Appendix shows the pre–defined header region of PCI Configuration Space.

A.2 PCI Configuration Space Registers

The PCI Configuration Space consists of fields that uniquely identify the device and allow the device to be generically controlled. The first 16 Bytes (four words) are defined the same for all types of PCI devices. The remaining words can have different layouts depending on the base function that the device supports. The PCI interface on the Model 71620 uses Header Type 00h, which has the layout shown in the table below. This table lists the PCI Configuration Space registers, their functions, and their base address in Configuration Space.

Table A–1: PCI Configuration Space Header (Type 00h)

Address	Register Function			
0x00	Device ID		Vendor ID	
0x04	Status		Command	
0x08	Class Code			Revision ID
0x0C	BIST	Header Type	Latency Timer	Cache Line Size
0x10	Base Address Register 0 (BAR0)			
0x14	Base Address Register 1 (BAR1)			
0x18	Base Address Register 2 (BAR2)			
0x1C	Base Address Register 3 (BAR3)			
0x20	Base Address Register 4 (BAR4)			
0x24	Base Address Register 5 (BAR5)			
0x28	Cardbus CIS Pointer			
0x2C	Subsystem ID		Subsystem Vendor ID	
0x30	Expansion ROM Base Address			
0x34	Reserved			
0x38	Reserved			
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line

The Base Address Registers defined for the Model 71620 are shown on the next page.

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A.2 PCI Configuration Space Registers (continued)

In the Model 71620, the first five Base Address Registers of PCI Configuration Space are used to configure the memory maps of board resources and registers. The following table shows the use of these registers in the 71620.

Table A–2: PCI Base Address Registers

Address	Register	Model 71620 Use
0x10	Base Address Register 0 (BAR0)	Memory access to 71620 FPGA Registers
0x14	Base Address Register 1 (BAR1)	reserved
0x18	Base Address Register 2 (BAR2)	Memory access to User–defined Registers
0x1C	Base Address Register 3 (BAR3)	reserved
0x20	Base Address Register 4 (BAR4)	Memory access to FLASH Memory

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Appendix B: Sample 71620 Applications

B.1 Introduction

This Appendix provides several Cobalt 71620 XMC module sample signal processing applications, showing the proper setup sequences for these typical applications. The following sample applications are provided:

- Using Triggered Acquisition of ADC Data – Section B.2
- Using the ADC DMA Engine – Section B.3
- Using the DAC DMA Engine and Linked List Output Controller – Section B.4

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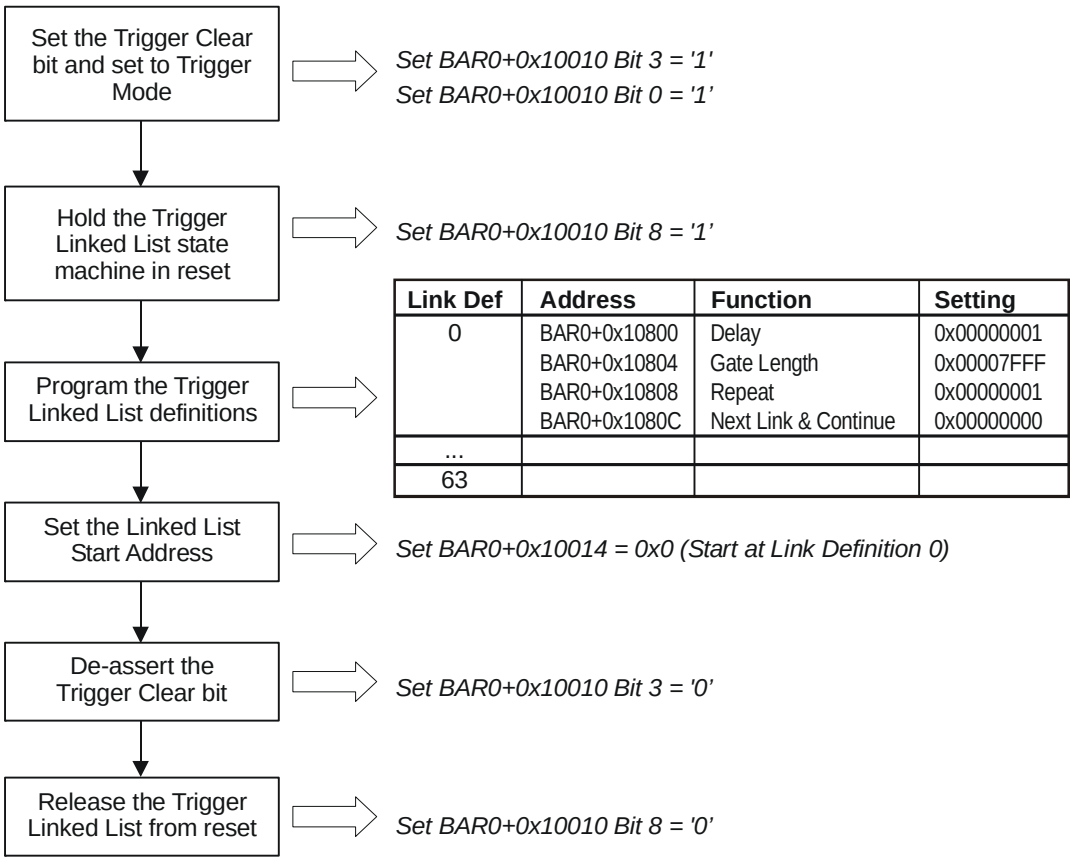
B.2 Using Triggered Acquisition of ADC Data

All data acquisition in the Cobalt 71620 XMC module is controlled by a gate signal that allows data to be written to the FIFO. This gate signal can be applied directly in "GATE MODE" or triggered in "TRIGGER MODE." Further, the Cobalt 71620 XMC module is capable of generating complex gate patterns following a single trigger event. Examples of several trigger scenarios and how to program the triggering circuitry to create them are illustrated below

B.2.1 Scenario 1

Requirement: After a trigger event, acquire 32768 data samples on ADC channel 1 and then stop. Repeat at each trigger event.

Solution:



Link Def	Address	Function	Setting
0	BAR0+0x10800	Delay	0x00000001
	BAR0+0x10804	Gate Length	0x00007FFF
	BAR0+0x10808	Repeat	0x00000001
	BAR0+0x1080C	Next Link & Continue	0x00000000
...			
63			

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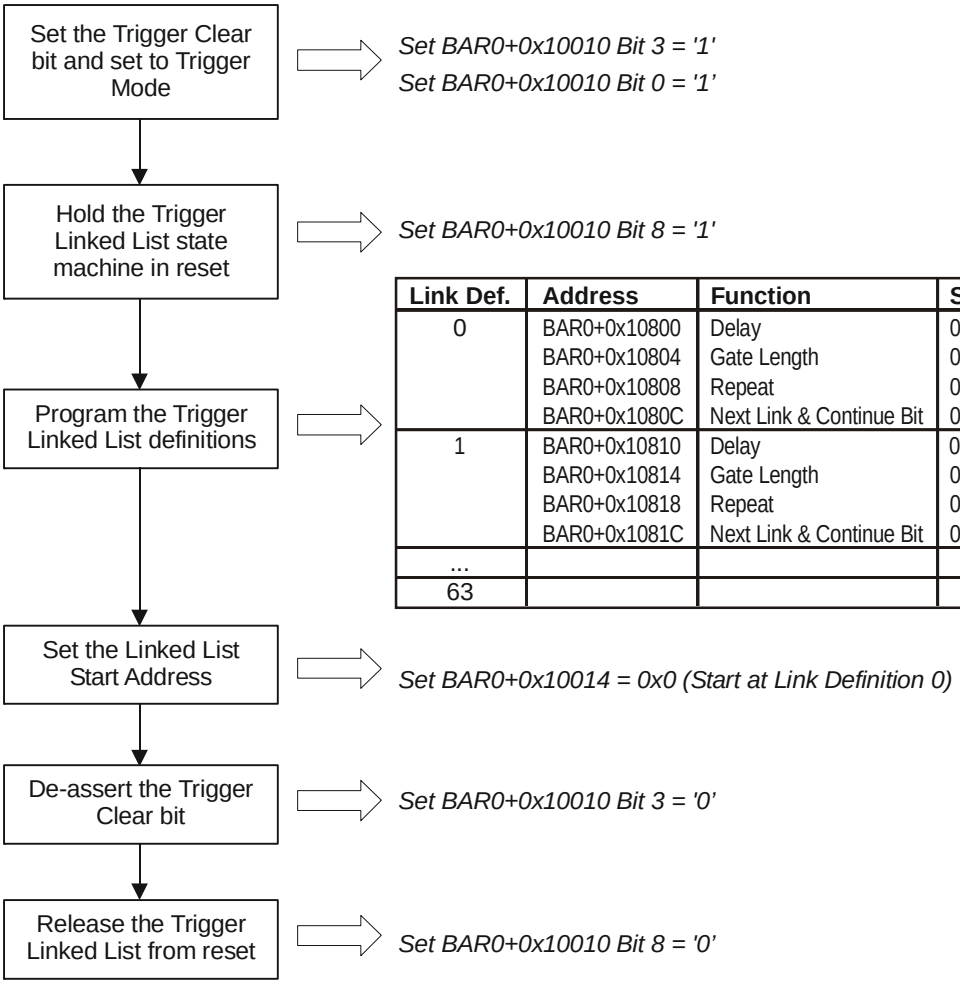
B.2 Using Triggered Acquisition of ADC Data (continued)

B.2.2 Scenario 2

Requirement: After a trigger event –

1) Wait 4000 clock cycles.
2) Acquire 16384 data samples on ADC channel 1.
3) Wait 10,000 clock cycles.
4) Acquire 16384 data samples on ADC channel 1.
5) Wait 10,000 clock cycles.
6) Acquire 16384 data samples on ADC channel 1.
7) Wait 10,000 clock cycles.
8) Acquire 16384 data samples on ADC channel 1.
9) Stop, wait for the next trigger and repeat.

Solution:



Link Def.	Address	Function	Setting
0	BAR0+0x10800	Delay	0x00000F9D
	BAR0+0x10804	Gate Length	0x00003FFF
	BAR0+0x10808	Repeat	0x00000001
	BAR0+0x1080C	Next Link & Continue Bit	0x00000101
1	BAR0+0x10810	Delay	0x0000270D
	BAR0+0x10814	Gate Length	0x00003FFF
	BAR0+0x10818	Repeat	0x00000003
	BAR0+0x1081C	Next Link & Continue Bit	0x00000000
...			
63			

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B.3 Using the ADC DMA Engine

The Cobalt 71620 XMC module includes an independent DMA engine for each of the three channels of ADC data. The DMA engine includes many special features that can minimize actions required by the host processor while at the same time providing it with useful information about the DMA transfer in side channel packets of meta data.

GATE CONTROLLED DMA MODE

The optional Gate Controlled DMA mode of operation is a useful mode when the length of acquisition is not known ahead of time. Examples of applications that can benefit from this are applications like radar systems using gate mode and an external gate source of unknown or varying length. Using this mode, only the amount of data acquired during the active gate period is transferred via DMA and no data remains stuck in the FIFO that the host would normally need to flush. The DMA link definition will halt execution at the earlier of the number of bytes to transfer specified in the link definition or at the last data sample of the active gate period. It then advances to the next link definition, requiring no cleanup operations from the host processor.

META DATA

The DMA engine can optionally collect useful information about the ADC data transferred during the last DMA and automatically DMA this information to the host processor. The interrupt that normally is generated at the end of the ADC data DMA can be delayed to occur after the transfer of the meta data packet. Information included in the meta data packet such as the number of ADC samples transferred as well as the destination buffer location can aid the host processor in processing the received data.

At a minimum, the meta data packet supplies the following information:

1) ADC Channel Number
2) The number of data samples transferred in the last completed DMA.
3) The Destination address where the data is located.
4) The link definition number that was responsible for the DMA.
5) A running 12–bit counter that identifies the number of the first packet of the DMA.
6) Notification of whether the FIFO overflowed and data was lost during this DMA.

When the first sample of the DMA is also the first sample of data of a gate period, the following information is also provided in the meta data packet:

1) A 32–bit PPS (Pulse per second) timestamp count for the first data sample.
2) A 32–bit Clock Cycle Offset timestamp count (number of clock cycles since the PPS pulse event) for the first data sample.
3) A running 16–bit trigger number, identifying what trigger event this data belongs to.
4) A running 16–bit gate number, identifying what gate period this data belongs to (Multiple gate periods may be generated by a trigger event).

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B.3 Using the ADC DMA Engine (continued)

Examples of several data acquisition scenarios and how to program the DMA engine to accomplish them are illustrated below.

B.3.1 Scenario 1

Requirement: The 71620 XMC module uses a software–generated trigger to acquire 32K 16–bit ADC data samples. It is desired that the data from each consecutive triggered gate period be sent to two buffers set up in the host processor's memory in an alternating ping–pong fashion. Upon the comple–tion of data transfer, the 71620 must interrupt the host processor. It is further desired that meta data be sent to the host notifying it of the timestamp of the first data sample. Meta data can also be used to determine which buffer data went to. It is desired that no cleanup operations be necessary between trig–gers, such as FIFO flushes and resets, and that host processor interaction be limited to reading and clearing the interrupt flag. After each interrupt is received, the host processor generates another software trigger with a length of 32K data samples.

Solution:

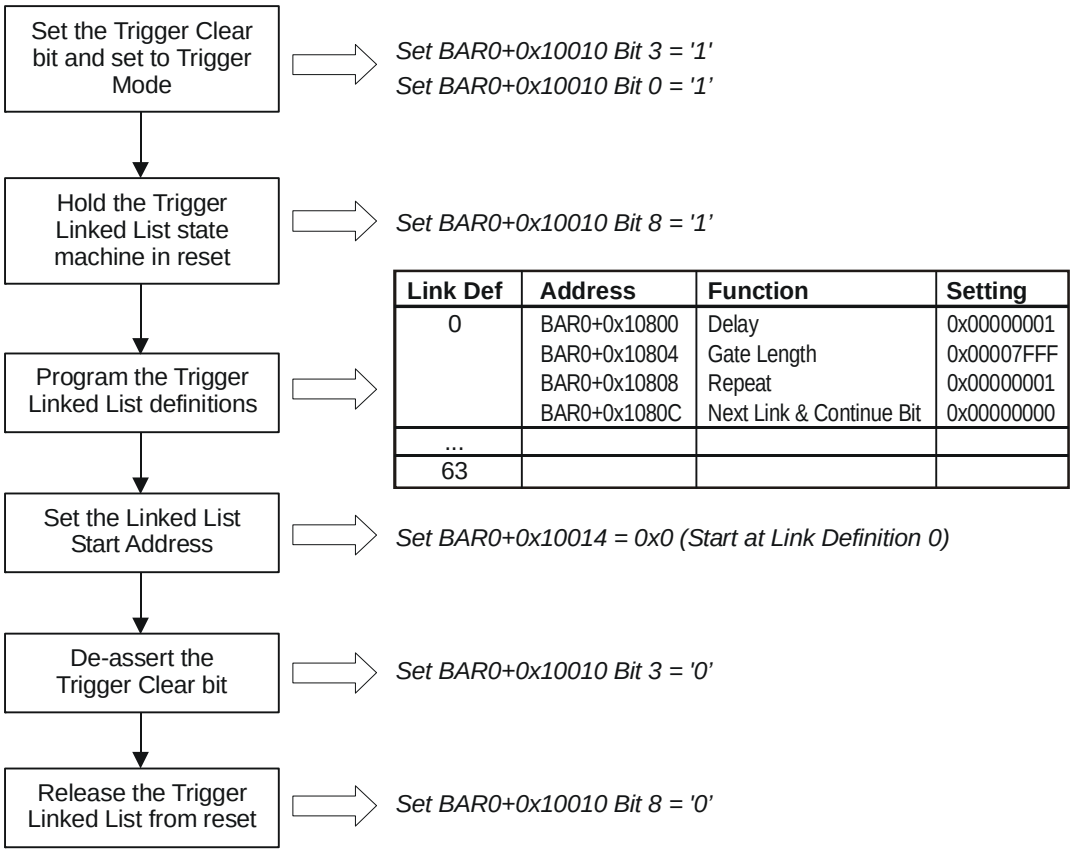
1) Set the acquisition mode to Trigger Mode and set the trigger length to (32768–1).
2) Since the data length is known, Gate Controlled DMA mode is optional but will not adversely affect operation.
3) Set the DMA transfer length to 64K bytes (32K data samples).
4) Set the DMA link definition to collect meta data.
5) Set up four link definitions:
   a) Data transfer to buffer #1
   b) Meta data transfer to buffer #3 with interrupt enabled.
   c) Data transfer to buffer #2
   d) Meta data transfer to buffer #3 with interrupt enabled.

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B.3 Using the ADC DMA Engine (continued)

B.3.1 Scenario 1 (continued)

❑ Scenario 1 Trigger Setup



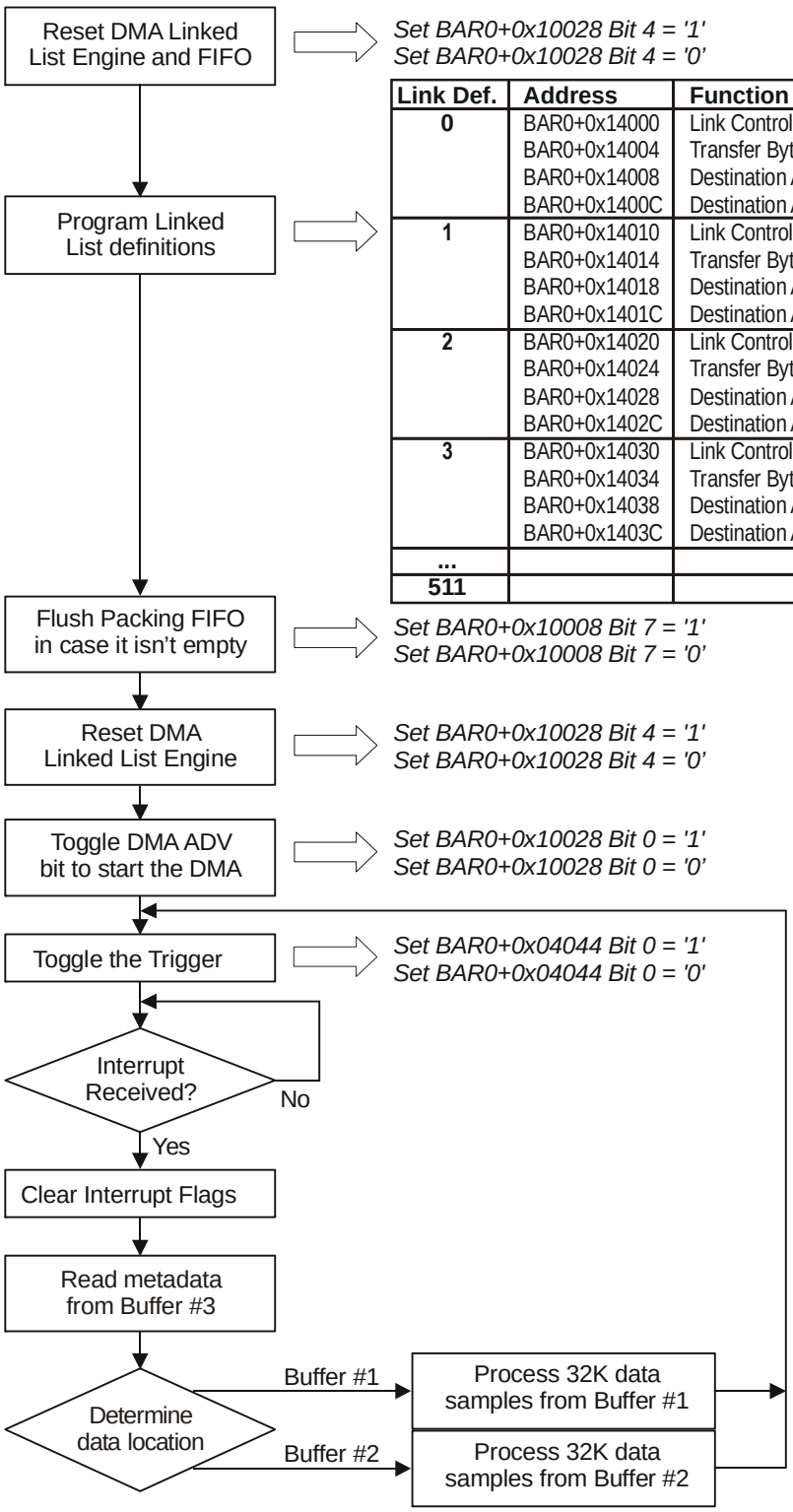
Link Def	Address	Function	Setting
0	BAR0+0x10800	Delay	0x00000001
	BAR0+0x10804	Gate Length	0x00007FFF
	BAR0+0x10808	Repeat	0x00000001
	BAR0+0x1080C	Next Link & Continue Bit	0x00000000
...			
63			

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B.3 Using the ADC DMA Engine (continued)

B.3.1 Scenario 1 (continued)

❑ Scenario 1 DMA Setup



Link Def.	Address	Function	Setting
0	BAR0+0x14000	Link Control Word	0x02A01000
	BAR0+0x14004	Transfer Byte Length	0x00010000
	BAR0+0x14008	Destination Addr[31:0]	Buffer1 Addr
	BAR0+0x1400C	Destination Addr[63:32]	0x00000000
1	BAR0+0x14010	Link Control Word	0x02C02000
	BAR0+0x14014	Transfer Byte Length	0x00000020
	BAR0+0x14018	Destination Addr[31:0]	Buffer3 Addr
	BAR0+0x1401C	Destination Addr[63:32]	0x00000000
2	BAR0+0x14020	Link Control Word	0x02A03000
	BAR0+0x14024	Transfer Byte Length	0x00010000
	BAR0+0x14028	Destination Addr[31:0]	Buffer2 Addr
	BAR0+0x1402C	Destination Addr[63:32]	0x00000000
3	BAR0+0x14030	Link Control Word	0x02C00000
	BAR0+0x14034	Transfer Byte Length	0x00000020
	BAR0+0x14038	Destination Addr[31:0]	Buffer3 Addr
	BAR0+0x1403C	Destination Addr[63:32]	0x00000000
...			
511			

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B.3 Using the ADC DMA Engine (continued)

B.3.2 Scenario 2

Requirement: The 71620 XMC module receives an external gate signal and must transfer ADC data from ADC channel 1 to the host processor only during the active period of that gate. The length of the gate will vary but it is known that it will never be more than 512K sample clocks in length. It is desired that the data from each consecutive gate period be sent to two buffers set up in the host processor's memory in an alternating ping–pong fashion. Upon the completion of data transfer, the 71620 must interrupt the host processor. It is further desired that meta data be sent to the host notifying it of the amount of data transferred during the gate period, which buffer it went to, and the timestamp of the first data sample. It is desired that no cleanup operations be necessary between gates, such as FIFO flushes and resets, and that host processor interaction be limited to reading and clearing the interrupt flag.

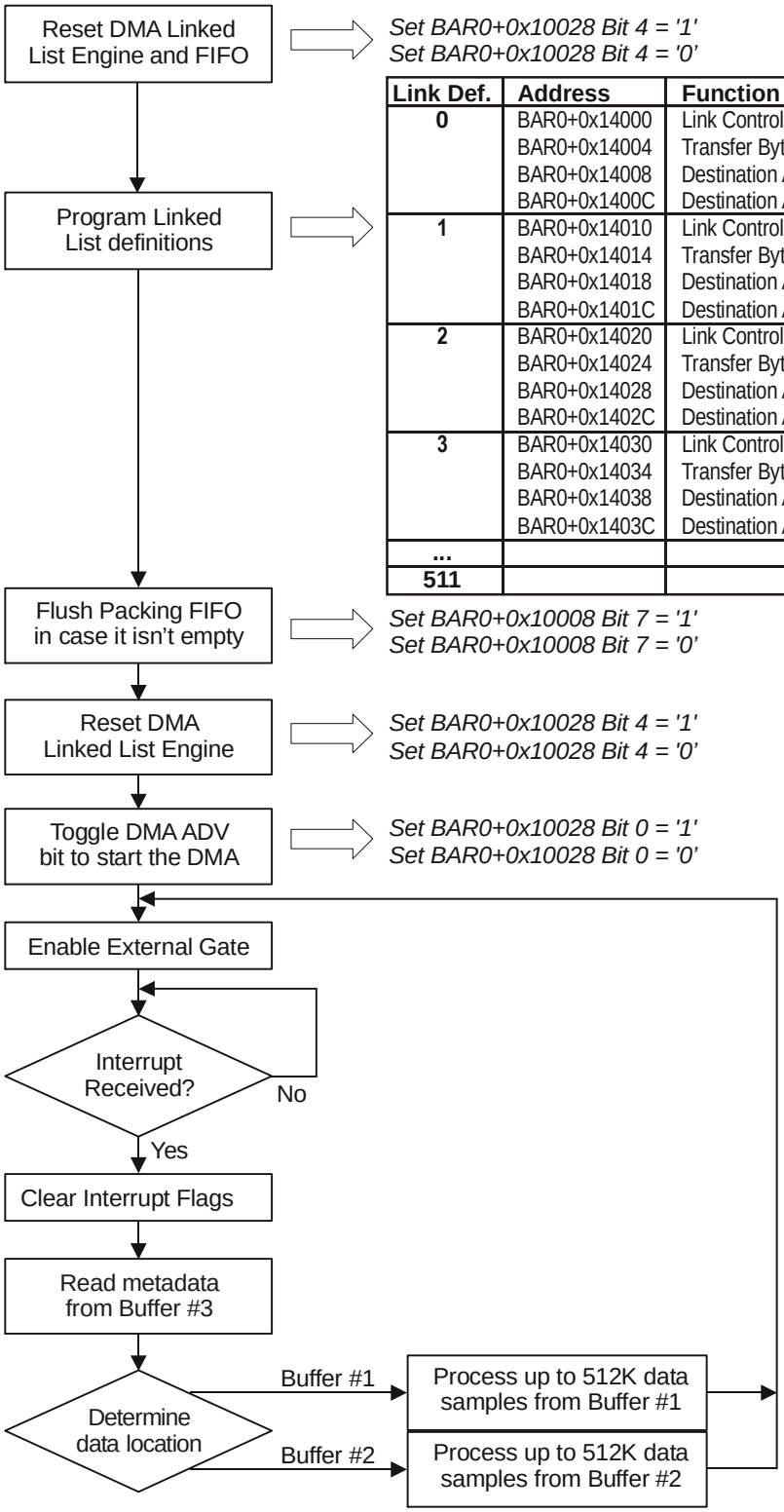
Solution:

1) Use Gate Controlled DMA mode. This will terminate the DMA transfer at the last data sample of the active gate period.
2) Set the DMA transfer length to 512K data samples. The transfer will terminate at the last sample of the active gate period or at 512K samples, whichever comes first.
3) Set the DMA link definition to collect meta data.
4) Set up four link definitions:
    a) Data transfer to buffer #1
    b) Meta data transfer to buffer #3 with interrupt enabled.
    c) Data transfer to buffer #2
    d) Meta data transfer to buffer #3 with interrupt enabled.

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B.3 Using the ADC DMA Engine (continued)

B.3.2 Scenario 2 (continued)



Link Def.	Address	Function	Setting
0	BAR0+0x14000	Link Control Word	0x02A01000
	BAR0+0x14004	Transfer Byte Length	0x00080000
	BAR0+0x14008	Destination Addr[31:0]	Buffer1 Addr
	BAR0+0x1400C	Destination Addr[63:32]	0x00000000
1	BAR0+0x14010	Link Control Word	0x02C02000
	BAR0+0x14014	Transfer Byte Length	0x00000020
	BAR0+0x14018	Destination Addr[31:0]	Buffer3 Addr
	BAR0+0x1401C	Destination Addr[63:32]	0x00000000
2	BAR0+0x14020	Link Control Word	0x02A03000
	BAR0+0x14024	Transfer Byte Length	0x00080000
	BAR0+0x14028	Destination Addr[31:0]	Buffer2 Addr
	BAR0+0x1402C	Destination Addr[63:32]	0x00000000
3	BAR0+0x14030	Link Control Word	0x02C00000
	BAR0+0x14034	Transfer Byte Length	0x00000020
	BAR0+0x14038	Destination Addr[31:0]	Buffer3 Addr
	BAR0+0x1403C	Destination Addr[63:32]	0x00000000
...			
511			

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B.3 Using the ADC DMA Engine (continued)

B.3.3 Scenario 3

Requirement: The 71620 XMC module uses an external trigger to start a long acquisition of ADC data from ADC channel 1. Acquisition continues and the triggered gate is held on until software clears the trigger. This is a common mode for data recorders. It is desired that the data be transferred to a series of four 16–megabyte data buffers in a circular fashion (Buffer#1–Buffer#4). Upon filling up a buffer, the 71620 must interrupt the host processor. The host processor needs the timestamp information for the beginning of the recording. Because it is a continuous acquisition, it can infer the timestamp of later samples. The host processor is also interested in maintaining real time and not dropping samples due to FIFO overflow. Therefore it is also interested in receiving notification of this event via the meta data. When the host processor ends acquisition with a software clear of the triggered gate, it is interested in knowing how much of the last buffer is good data, because the last buffer will only be partially filled. It is desired that no cleanup operations be necessary between DMAs, and that host processor interaction be limited to reading and clearing the interrupt flag. It is also desirable that the last DMA not hang due to the gate going away before it transfers a full 16–megabyte buffer of data.

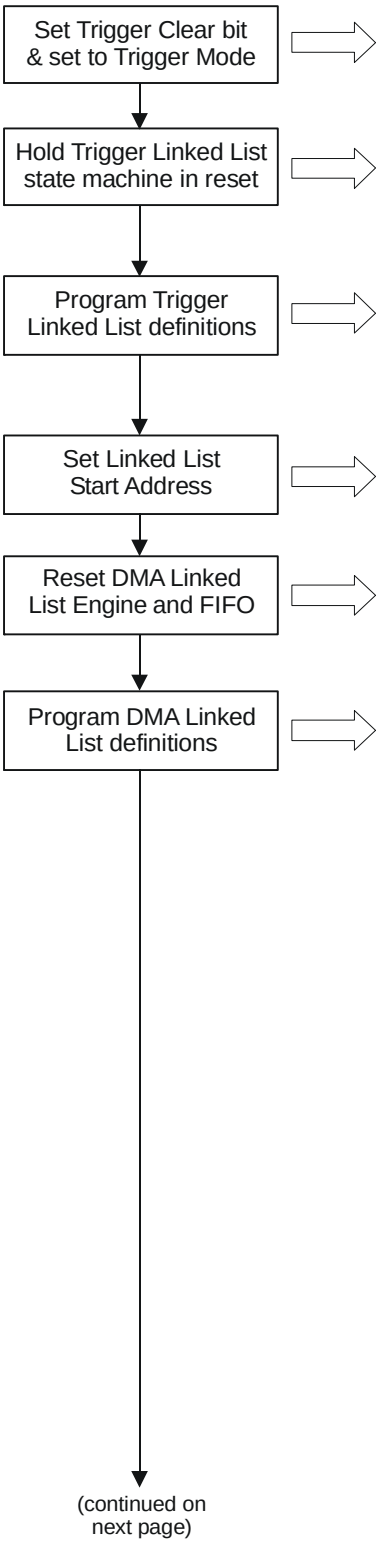
Solution:

1) Set the acquisition mode to Trigger Mode and Hold Mode.
2) Use Gate Controlled DMA mode.
3) Set the DMA transfer length to 16 Megabytes (8 Mega–samples).
4) Set the DMA link definition to collect meta data.
5) Set up eight link definitions:
    a) Data transfer to buffer #1
    b) Meta data transfer to Table Address #1 with interrupt enabled.
    c) Data transfer to buffer #2
    d) Meta data transfer to Table Address #2 with interrupt enabled.
    e) Data transfer to buffer #3
    f) Meta data transfer to Table Address #3 with interrupt enabled.
    g) Data transfer to buffer #4
    h) Meta data transfer to Table Address #4 with interrupt enabled.

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B.3 Using the ADC DMA Engine (continued)

B.3.3 Scenario 3 (continued)



Set BAR0+0x10010 Bit 3 = '1'
Set BAR0+0x10010 Bit 0 = '1'

Set BAR0+0x10010 Bit 8 = '1'

Link Def	Address	Function	Setting
0	BAR0+0x10800	Delay	0x00000001
	BAR0+0x10804	Gate Length	0x00000001
	BAR0+0x10808	Repeat	0x00000001
	BAR0+0x1080C	Next Link & Continue Bit	0x00000000
...			
63			

Set BAR0+0x10014 = 0x0 (Start at Link Definition 0)

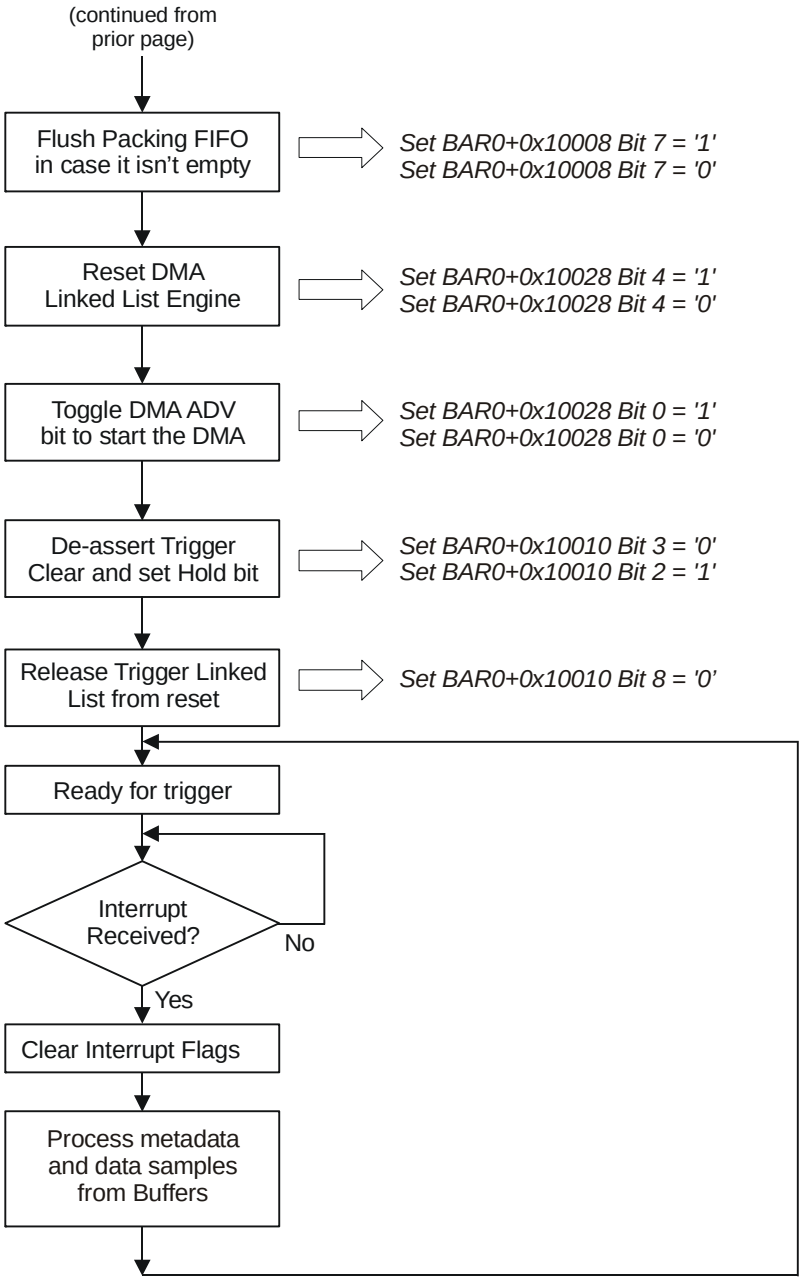
Set BAR0+0x10028 Bit 4 = '1'
Set BAR0+0x10028 Bit 4 = '0'

Link Def	Address	Function	Setting
0	BAR0+0x14000	Link Control Word	0x02A01000
	BAR0+0x14004	Transfer Byte Length	0x01000000
	BAR0+0x14008	Destination Addr[31:0]	Buffer1 Addr
	BAR0+0x1400C	Destination Addr[63:32]	0x00000000
1	BAR0+0x14010	Link Control Word	0x02C02000
	BAR0+0x14014	Transfer Byte Length	0x00000020
	BAR0+0x14018	Destination Addr[31:0]	Table1 Addr
	BAR0+0x1401C	Destination Addr[63:32]	0x00000000
2	BAR0+0x14020	Link Control Word	0x02A03000
	BAR0+0x14024	Transfer Byte Length	0x01000000
	BAR0+0x14028	Destination Addr[31:0]	Buffer2 Addr
	BAR0+0x1402C	Destination Addr[63:32]	0x00000000
3	BAR0+0x14030	Link Control Word	0x02C04000
	BAR0+0x14034	Transfer Byte Length	0x00000020
	BAR0+0x14038	Destination Addr[31:0]	Table2 Addr
	BAR0+0x1403C	Destination Addr[63:32]	0x00000000
4	BAR0+0x14000	Link Control Word	0x02A05000
	BAR0+0x14004	Transfer Byte Length	0x01000000
	BAR0+0x14008	Destination Addr[31:0]	Buffer3 Addr
	BAR0+0x1400C	Destination Addr[63:32]	0x00000000
5	BAR0+0x14010	Link Control Word	0x02C06000
	BAR0+0x14014	Transfer Byte Length	0x00000020
	BAR0+0x14018	Destination Addr[31:0]	Table3 Addr
	BAR0+0x1401C	Destination Addr[63:32]	0x00000000
6	BAR0+0x14020	Link Control Word	0x02A07000
	BAR0+0x14024	Transfer Byte Length	0x01000000
	BAR0+0x14028	Destination Addr[31:0]	Buffer4 Addr
	BAR0+0x1402C	Destination Addr[63:32]	0x00000000
7	BAR0+0x14030	Link Control Word	0x02C00000
	BAR0+0x14034	Transfer Byte Length	0x00000020
	BAR0+0x14038	Destination Addr[31:0]	Table4 Addr
	BAR0+0x1403C	Destination Addr[63:32]	0x00000000

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B.3 Using the ADC DMA Engine (continued)

B.3.3 Scenario 3 (continued)



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B.4 Using the DAC DMA Engine and Linked List Output Controller

All DAC data output from the Cobalt 71620 XMC module is controlled by a gate signal that allows data to be read from the DAC output FIFO. The source of data into this FIFO can either be directly from the DMA engine or from QDRII+ or DDR3 RAM waveform storage. This gate signal can be applied directly in "GATE MODE" or triggered in "TRIGGER MODE." Further, the Cobalt 71620 XMC module is capable of generating complex output gate patterns following a single trigger event. Examples of several scenarios and how to program the triggering circuitry and DMA to create them are illustrated below.

B.4.1 Scenario 1

Requirement: It is required that 32K I/Q samples of a waveform be stored in QDRII+ RAM and after an external trigger event, the waveform is output to the DAC. Repeat output of the same waveform at each trigger event.

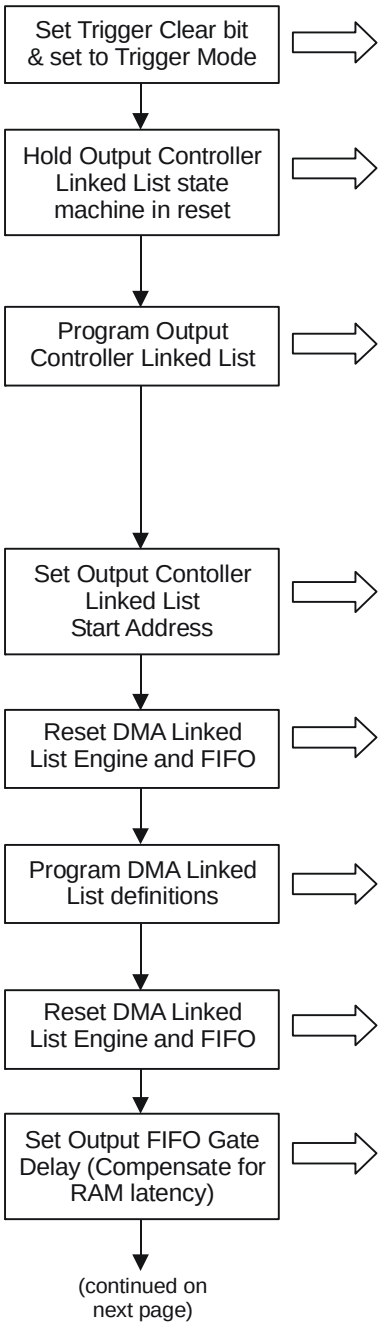
Solution:

1) Set up the DAC channel for external trigger mode.
2) Set up the DAC Output Linked List Controller to acquire 32K I/Q samples from QDRII+ RAM at each trigger event.
3) Set up the DAC DMA to read 32K I/Q samples from the host processor's memory at address Buffer #1.

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B.4 Using the DAC DMA Engine and Linked List Output Controller (cont'd)

B.4.1 Scenario 1 (continued)



Set BAR0+0x30010 Bit 3 = '1'
Set BAR0+0x30010 Bit 0 = '1'

Set BAR0+0x30010 Bit 8 = '1'

Link Def	Address	Function	Setting
0	BAR0+0x30800	Delay	0x00000001
	BAR0+0x30804	Gate Length	0x00007FFF
	BAR0+0x30808	Repeat	0x00000001
	BAR0+0x3080C	RAM Offset Address	0x00000000
	BAR0+0x30810	RAM Repeat Length	0x00003FFF
	BAR0+0x30814	Continue Bit	0x00000000
	BAR0+0x30818	Next Link	0x00000000
	BAR0+0x3081C	No Function	0x00000000
...			
63			

Set BAR0+0x30014 = 0x0 (Start at Link Definition 0)

Set BAR0+0x30028 Bit 4 = '1'
Set BAR0+0x30028 Bit 4 = '0'

Link Def	Address	Function	Setting
0	BAR0+0x34000	Link Control Word	0x90800000
	BAR0+0x34004	Transfer Byte Length	0x00020000
	BAR0+0x34008	Source Addr[31:0]	Buffer1 Addr
	BAR0+0x3400C	Source Addr[63:32]	0x00000000
...			
511			

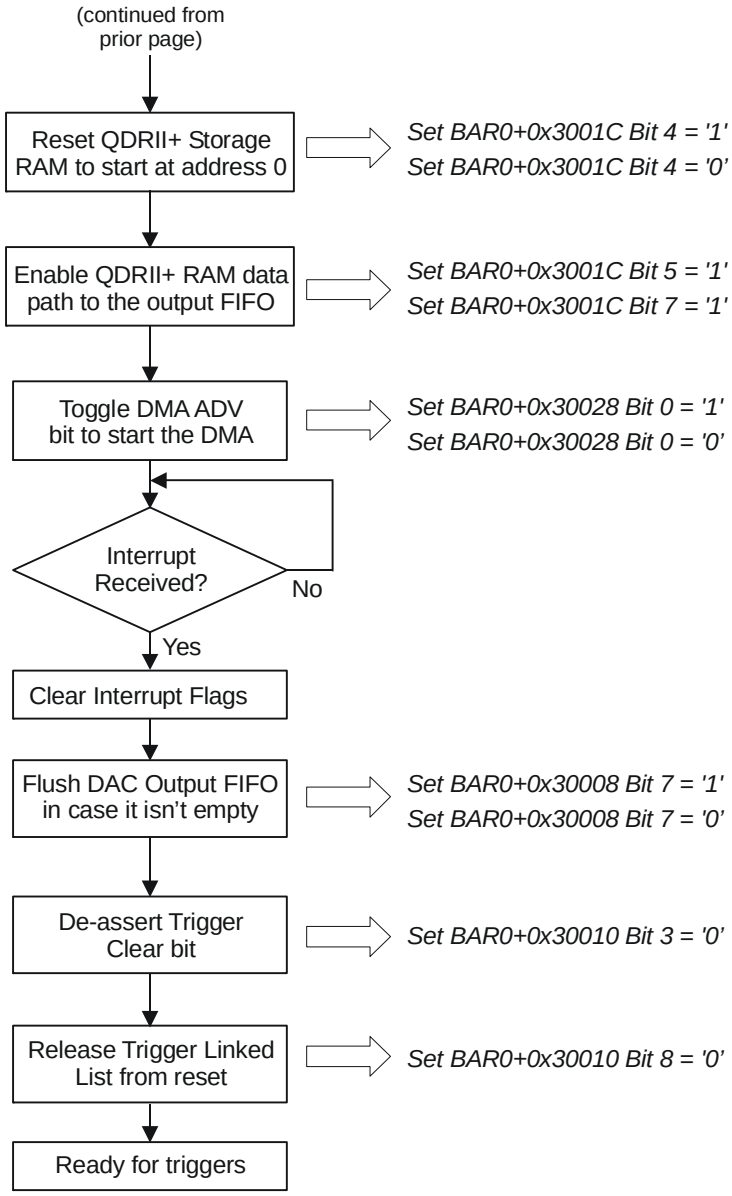
Set BAR0+0x30028 Bit 4 = '1'
Set BAR0+0x30028 Bit 4 = '0'

Set BAR0+0x30020 Bit 4 = 0x00000020

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B.4 Using the DAC DMA Engine and Linked List Output Controller (cont'd)

B.4.1 Scenario 1 (continued)



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B.4 Using the DAC DMA Engine and Linked List Output Controller (cont'd)

B.4.2 Scenario 2

Requirement: It is required that the 71620 XMC output a continuous stream of I/Q data to the DAC. Data must be transferred from the host processor's memory and fed directly to the DAC output FIFO. Data in the host processor's memory is set up as a ping–pong buffer. Whenever the 71620 DMA is finished reading one buffer it must interrupt the host processor so that the host processor may begin writing new data into the last used buffer while the next buffer is being read by the 71620.

Solution:

1) Set up the DAC channel for Gate Mode.

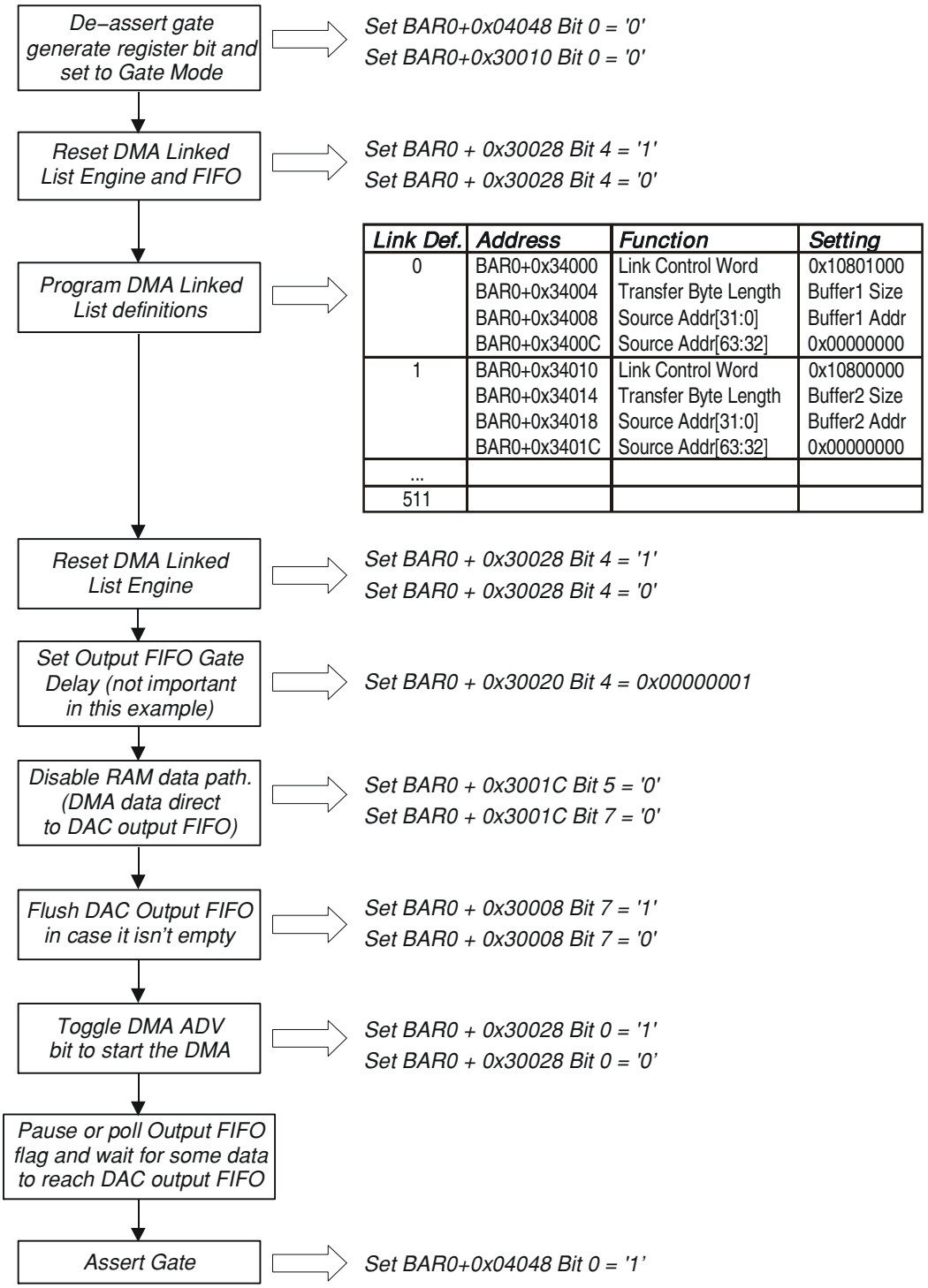
2) Set up two link definitions in DAC DMA to alternately read Buffer #1 and Buffer #2 from the host processor's memory and output it directly to the DAC output FIFO.

NOTE: Maintaining real time is highly dependent on the host PCIe bus speed, the speed of the host processor's RAM, motherboard architecture, as well as PCIe Read Request Size. PCIe Read Request sizes of 1024 bytes or greater may be required.

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B.4 Using the DAC DMA Engine and Linked List Output Controller (cont'd)

B.4.2 Scenario 2 (continued)



Link Def.	Address	Function	Setting
0	BAR0+0x34000	Link Control Word	0x10801000
	BAR0+0x34004	Transfer Byte Length	Buffer1 Size
	BAR0+0x34008	Source Addr[31:0]	Buffer1 Addr
	BAR0+0x3400C	Source Addr[63:32]	0x00000000
1	BAR0+0x34010	Link Control Word	0x10800000
	BAR0+0x34014	Transfer Byte Length	Buffer2 Size
	BAR0+0x34018	Source Addr[31:0]	Buffer2 Addr
	BAR0+0x3401C	Source Addr[63:32]	0x00000000
...			
511			

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B.4 Using the DAC DMA Engine and Linked List Output Controller (cont'd)

B.4.3 Scenario 3

Requirement: It is required that four unique waveforms of different lengths be stored in QDRII+ RAM.

- Waveform #1: 32768 I/Q data samples in length (Resides at host processor memory address Buffer #1)
- Waveform #2: 60,000 I/Q data samples in length (Resides at host processor memory address Buffer #2)
- Waveform #3: 100,000 I/Q data samples in length (Resides at host processor memory address Buffer #3)
- Waveform #4: 128,000 I/Q data samples in length (Resides at host processor memory address Buffer #4)

After an external trigger event the following sequence occurs:

1) Delay 10 clock cycles
2) Output Waveform #1
3) Delay 10,000 clock cycles
4) Output Waveform #2
5) Delay 20,000 clock cycles
6) Output Waveform #3
7) Delay 40,000 clock cycles
8) Output Waveform #4

Repeat at each trigger event.

Solution:

1) Set up the DAC channel for external trigger mode.
2) Set up four link definitions in the DAC Output Linked List Controller to acquire the four waveforms from QDRII+ RAM at each trigger event.
3) Set up four link definitions in the DAC DMA to read the four waveforms from the host processor's memory.

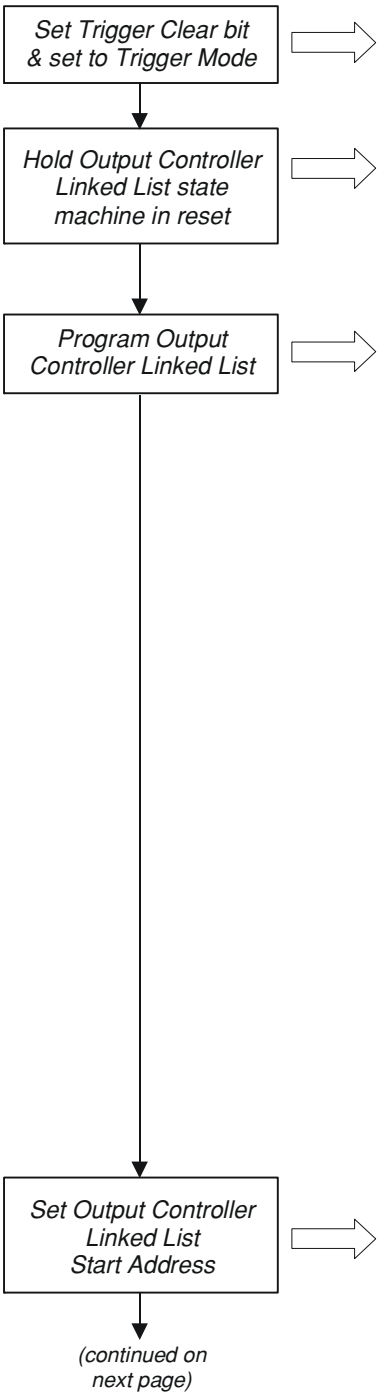
   The packed I/Q pair is a 32–bit word. The QDRII+ addressing is in terms of 64–bit words. Therefore, after the four DMAs complete the start address in QDRII+ memory will be as follows for the four waveforms:

   Waveform #1: Start Address = 0x00000
   Waveform #2: Start Address = 0x04000
   Waveform #3: Start Address = 0x0B530
   Waveform #4: Start Address = 0x17880

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B.4 Using the DAC DMA Engine and Linked List Output Controller (cont'd)

B.4.3 Scenario 3 (continued)

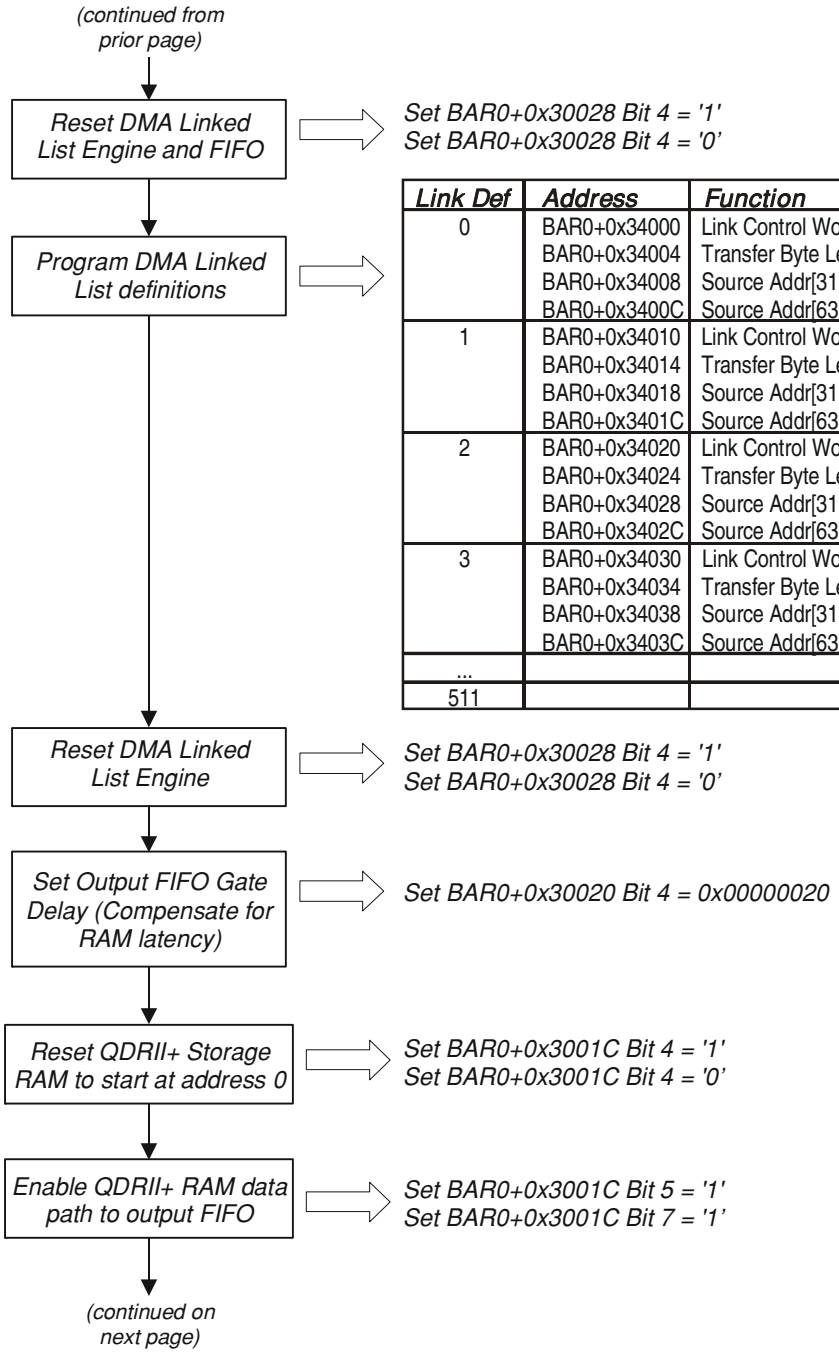


Link Def	Address	Function	Setting
0	BAR0+0x30800	Delay	0x00000007
	BAR0+0x30804	Gate Length	0x00007FFF
	BAR0+0x30808	Repeat	0x00000001
	BAR0+0x3080C	RAM Offset Address	0x00000000
	BAR0+0x30810	RAM Repeat Length	0x00003FFF
	BAR0+0x30814	Continue Bit	0x00000001
	BAR0+0x30818	Next Link	0x00000001
	BAR0+0x3081C	No Function	0x00000000
1	BAR0+0x30820	Delay	0x0000270D
	BAR0+0x30824	Gate Length	0x0000EA5F
	BAR0+0x30828	Repeat	0x00000001
	BAR0+0x3082C	RAM Offset Address	0x00004000
	BAR0+0x30830	RAM Repeat Length	0x0000752F
	BAR0+0x30834	Continue Bit	0x00000001
	BAR0+0x30838	Next Link	0x00000002
	BAR0+0x3083C	No Function	0x00000000
2	BAR0+0x30840	Delay	0x00004E1E
	BAR0+0x30844	Gate Length	0x0001869F
	BAR0+0x30848	Repeat	0x00000001
	BAR0+0x3084C	RAM Offset Address	0x0000B530
	BAR0+0x30850	RAM Repeat Length	0x0000C34F
	BAR0+0x30854	Continue Bit	0x00000001
	BAR0+0x30858	Next Link	0x00000003
	BAR0+0x3085C	No Function	0x00000000
3	BAR0+0x30860	Delay	0x00009C3E
	BAR0+0x30864	Gate Length	0x0001F3FF
	BAR0+0x30868	Repeat	0x00000001
	BAR0+0x3086C	RAM Offset Address	0x00017880
	BAR0+0x30870	RAM Repeat Length	0x0000F9FF
	BAR0+0x30874	Continue Bit	0x00000000
	BAR0+0x30878	Next Link	0x00000000
	BAR0+0x3087C	No Function	0x00000000
...			
63			

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B.4 Using the DAC DMA Engine and Linked List Output Controller (cont'd)

B.4.3 Scenario 3 (continued)

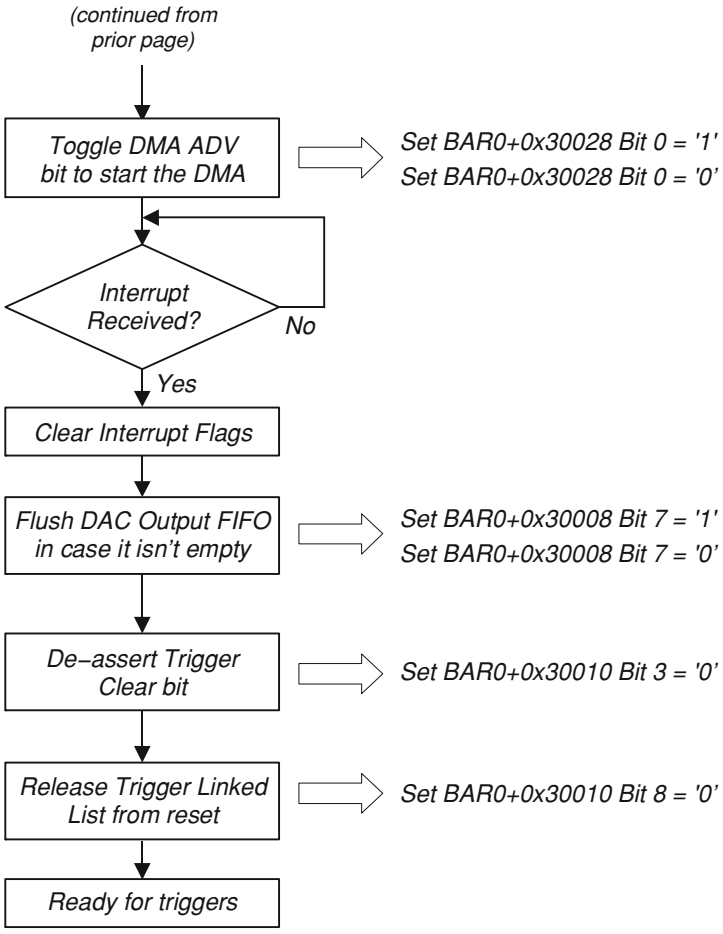


Link Def	Address	Function	Setting
0	BAR0+0x34000	Link Control Word	0x00801000
	BAR0+0x34004	Transfer Byte Length	0x00020000
	BAR0+0x34008	Source Addr[31:0]	Buffer1 Addr
	BAR0+0x3400C	Source Addr[63:32]	0x00000000
1	BAR0+0x34010	Link Control Word	0x00802000
	BAR0+0x34014	Transfer Byte Length	0x0003A980
	BAR0+0x34018	Source Addr[31:0]	Buffer2 Addr
	BAR0+0x3401C	Source Addr[63:32]	0x00000000
2	BAR0+0x34020	Link Control Word	0x00803000
	BAR0+0x34024	Transfer Byte Length	0x00061A80
	BAR0+0x34028	Source Addr[31:0]	Buffer3 Addr
	BAR0+0x3402C	Source Addr[63:32]	0x00000000
3	BAR0+0x34030	Link Control Word	0x90800000
	BAR0+0x34034	Transfer Byte Length	0x0007D000
	BAR0+0x34038	Source Addr[31:0]	Buffer4 Addr
	BAR0+0x3403C	Source Addr[63:32]	0x00000000
...			
511			

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B.4 Using the DAC DMA Engine and Linked List Output Controller (cont'd)

B.4.3 Scenario 3 (continued)



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