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OPERATING MANUAL

MODEL 6509

Octal Digital Receiver with TMS320C40-
Compatible Comm Port I/O
for VMEbus Systems

Pentek, Inc.
One Park Way
Upper Saddle River, NJ 07458
(201) 818-5900
http://www.pentek.com/

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Pentek Model 6509 Operating Manual - Revision History

Date	Rev	Applicable Serial #ís	Comments
12/20/96 - 8/29/97	Preliminary	9650001 - 9739000	Six revisions in this period - contact factory for details
09/18/97	Preliminary	9718056 - 9739000	Update Block Diagram (Fig. 1-1) to show the ëC40 & its connections. Add setup (2 ns) & hold (8 ns) times, and max clk. rate (70 MHz) to Specs in Sec. 1-6. Change note following Sec. 3.5.7 to indicate that direct FIFO readout is disabled if Comm Port readout is enabled - reword Sec. 3.5.7.4 and add an additional note under that sec. to drive home this point. Clock Not Ready status/interrupts are actually arranged by channel rather than by receiver, and use only 2 bits in Int. Mask Reg. 1 & Stat. Reg. 1 - this affects Secs. 3.5.2.2 & 3.5.4.4, and Tables 3-8 & 3-10. New Comm Port readout mode - Packed, Time Ordered, Real Only - delivers 2 real samples from selected receiver in each longword. This affects Secs.3.5.7 & 3.5.7.2 and Table 3-13. Add Packed, I/Q Ordered, Complex port readout mode to Table 3-21 (Tagged format table). Odd-numbered FIFO reset bits are used to reset the Comm Port controller for the port pair (Sec. 3.5.6)
10/30/97	Preliminary	9739000 - Forward	Sec. 2.4.1 & Fig. 2-6 - Std. Comm Port Cable is Model 2104, not 2014, and 4285 Cable is Model 2115, not 2015. Comm Port Initialization bit added to FIFO Reset Register (changes to Secs. 2.4.1 & 3.5.6, and Table 3-12, add Secs. 3.5.6.1 & 3.5.6.2).
02/11/98, 3/05/98, 3/16/98	Preliminary	9739000 - Forward	Corrections to Figure 2-7: True and Complemented data pins for ECL input stage swapped - improved resolution of figure. In pinout table, Channel Bís pins should be the lower-numbered half of the connector. Corrected ëC40 to VME Interrupt Status Bit (D31), interrupt bit was flipped.
04/02/98	A	9739000 - Forward	Added Chapter 4 and Appendix A. Both derived from 6510 Manual.
04/15/98	A.1	9739000 - Forward	Completed Firmware programming examples. Made minor corrections to existing Firmware examples.
08/28/98	B	9739000 - Forward	Added ECL Mezz. board diagram (Fig. 2-4). Added Sec.2.5 on using multiple ECL 6509 cards from a single source. Added Sec. 4.2 on disabling the 6509ís firmware.
10/06/98	C	9739000 - Forward	Added Jumper Setting table to Secs. 3.5.8 and 2.3. Also included new information about jumpers to Sec. 2.3. Added Input Signal Cable Changes for Single Master Sync (Sec. 2.4.3).
6/10/99	C.1	9739000 - Forward	Remove all references to a TTL input option. Sec. 1.6 - Input connector is 68 pins, not 80. Sec. 2.2 - Set address switches before installing in card cage. Fig. 2-3 - Correct reversal of callouts on JB1 & JB2, flip figure to match orientation of Fig. 2-2, and show RN locations so that the next figure can be deleted (formerly Fig. 2-4). Sec. 2.3 - Renamed & completely rewritten, including Table 2-1. Add new Section (2.4) on terminating ressitors, containing 2 new Figs. (2-4 & 2-5) - this replaces the former Secs. 2.5.3 & 2.6. Sec. 2.5.2 & Fig. 2-8 - Recommended cable changed to 3M # 3756/68. Minor formatting changes to FW chapter.

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Chapter 1: Overview

1.1 General Description

Pentek's Model 6509 is a general purpose multiband digital receiver VMEbus board that accepts digitized data at rates up to 70 MHz. It can be configured with up to eight receiver channels to perform frequency down conversion, low-pass filtering and decimation of the sampled input signal.

The receiver output signals are delivered through front panel 'C40 Comm Ports to facilitate the implementation of DSP functions on Pentek's 'C40 Digital Signal Processor boards. Another set of front panel 'C40 Comm Ports can be used to allow the DSP to tune and control the receiver. Receiver tuning, filter and FIFO control are also available over the VMEbus.

1.2 Operating Principle

The Model 6509 uses the highly integrated GC1011A, from Graychip, which contains a tunable local oscillator, a mixer and a tunable low-pass output filter. The local oscillator frequency and the output filter cutoff frequency for each receiver are independently programmable over either the VMEbus or the channel's comm port interface, providing extremely flexible and agile operation.

1.3 Applications

This device provides an effective way to create multichannel Digital Signal Processing and analysis systems for selected frequency bands. Since the selected bands are down-converted, they make it economically feasible to perform DSP functions, such as FFT spectrum analysis, on RF signals. Typical applications include frequency-division multiplexed communications systems, modem modulation schemes, and analysis of many forms of radar signals.

1.4 Flexible Input Connections

All input data is accepted on front panel digital connectors with differential ECL logic level compliance. An input multiplexer allows the same digital data stream to feed all eight receivers, in order to simultaneously extract up to eight different frequency bands. Operating modes and receiver frequencies are programmable from either the VMEbus or the Comm Port interface.

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1.5 Block Diagram.

Figure 1-1, below, shows the block diagram of Pentek's Model 6509 Octal Digital Receiver VMEbus Board with 'C40 Comm Port I/O.

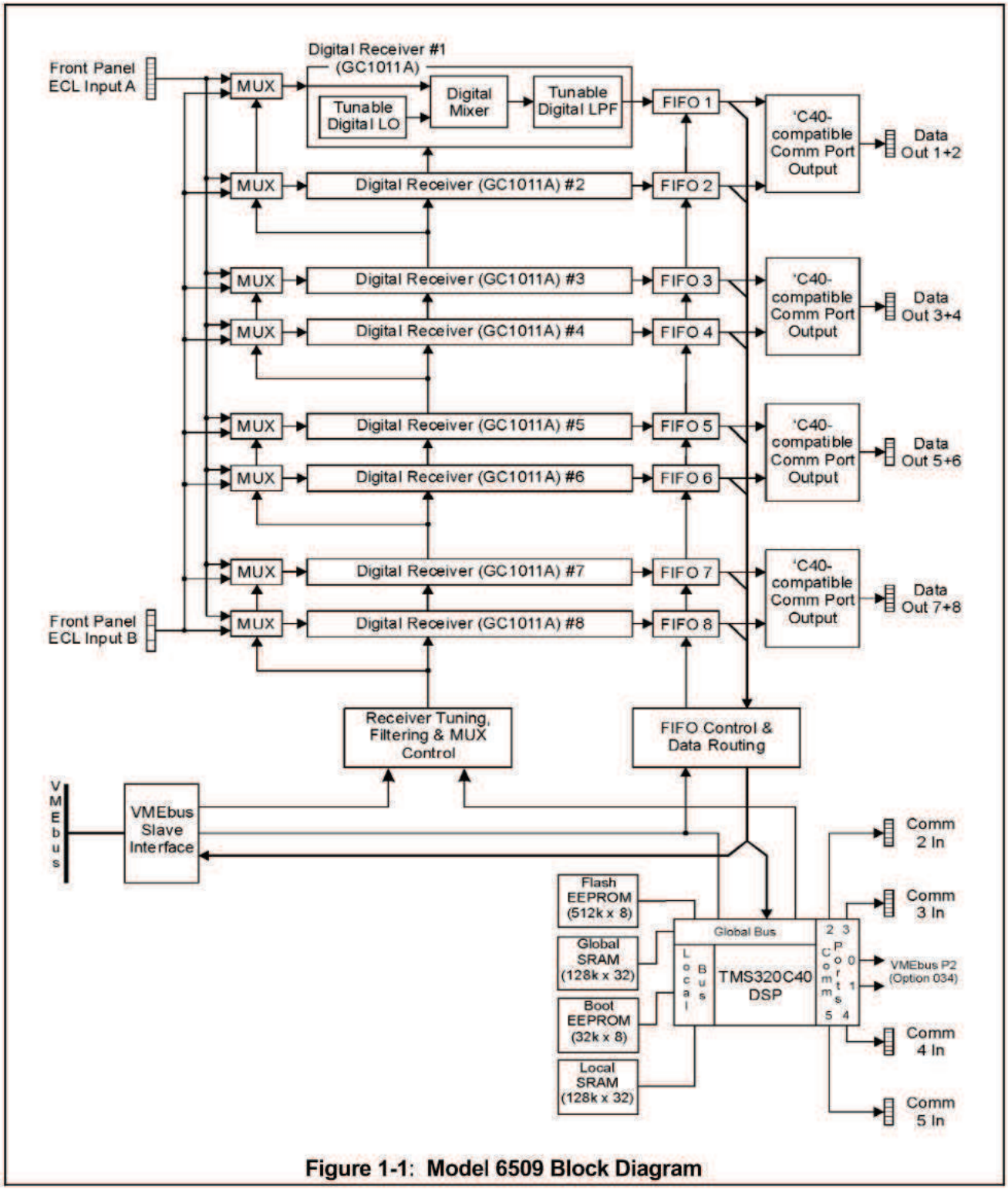


Figure 1-1: Model 6509 Block Diagram

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1.6 Specifications

Receiver Chips: Up to 8 (eight) Graychip GC1011A - 12-bit input data; (Option 004 - 4 (four) receiver chips); See Appendix B for chip specifications.

Digital Inputs

Option 012: Differential ECL inputs compatible with Pentek Models 6402-002, 6410-002 and 6441-002 A/D Converters (using Pentekís Model 2119 cable assembly), and Pentek Models 6470 and 6472 A/D Converters (using Pentekís Model 2106 cable assembly). These A/D Converters can provide data rates up to 70 MHz.

Input Connectors: Front panel 68-pin 3M connector (#82068-6006) for .025-in. pitch cable. Accepts up to 12 bits of data using 68-conductor cable & 68-pin connector.

Input Signals:

Data:	12 (twelve) input lines/channel.
Clock:	1 (one) input line/channel. Clock Rate 70 MHz max.
External Sync:	2 (two) input lines/channel (filter & accumulator syncs).
Data Setup Time:	2 nsec before rising edge of clock.
Data Hold Time:	8 nsec after rising edge of clock .

Input Multiplexers: Each receiver can independently select Input Channel A or Input Channel B.

Input Comm Ports: Four, connected via buffers to ëC40 processor. (excluded in Option 040).

Buffers: Active.

Functions: Receiver control & tuning, Multiplexer & Synchronization control. Any port can control any or all channels.

Output Comm Ports: Four, one for each pair of receivers; byte serial with 4 bytes per 32-bit longword; data may be packed (two 16-bit data words per longword) or unpacked (one 16-bit data word per longword).

Buffers: Active.

Functions: Each port delivers data from two receivers.

Maximum Data Rate: 10 MBytes/sec.

FIFO Memory:

Standard: 1k x 16 FIFO for each receiver channel.

Option 020: 8k x 16 FIFO for each receiver channel.

Option 021: 16k x 16 FIFO for each receiver channel.

Option 022: 4k x 16 FIFO for each receiver channel.

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1.6 Specifications (continued)

VMEbus Interface: Slave; A32/D32; I1-7; Powers up with no A24/A32 address mapping; Bus Grant daisy chain bussed through; Interrupt daisy chain supported.

- **A16 Memory Map:** A16 Base Address set with Rotary Switch; 256 byte address space max; A24/A32 base address configuration registers; Interrupt Vector Register; 'C40 Test Bus Controller for 'C40 J-TAG; Status/Control Registers ('C40 Reset, 'C40 Interrupt, IRQ level select, A24 enable, word swap, etc.).
- **A24/32 Memory:** Mapping disabled on power up, configured with A16 registers; 1 MB address space in A24; 4 MB address space in A32; All Data FIFO's (no data packing in VME memory - 16 bits only); Receiver, Multiplexer & Synchronization Control functions; Interrupt Mask Registers; Threshold Detectors; Clock Timeout; Threshold Select Registers - one of four thresholds per Input channel; 'C40 Status/ Control Registers; 128k x 32 'C40 Shared Global SRAM; 256k x 8 Flash memory (A32 only).
- **VMEbus Data Rate:** 200 nsec DS to DTACK delay max (with no contention for global bus by 'C40); 280 nsec bus cycle time max (with 80 nsec master response overhead).

Processor: One Texas Instruments TMS320C40 - 50 MHz; On-board XDS-510 14-pin J-TAG emulator connector; Texas Instruments Test Bus Controller mapped into A16 VMEbus space; four active buffered Comm Ports to front panel; Comm Ports 0 and 1 may optionally be made available over VMEbus P2 connector (Option 034).

- **'C40 Global Bus:** 128k x 32 Global SRAM, 1 wait state, Shared with VMEbus; 256k x 8 Flash User EEPROM; Receiver, Multiplexer & Synchronization Control registers; all data FIFOs.
- **'C40 Local Bus:** 128k x 32 Local SRAM - 0 wait state; 32k x 8 Boot PROM (factory code).

Power: 3.0 A @ + $5V_{DC}$ max.

Dimensions: 6U (160 mm x 233.35 mm), Single (4HP) 0.8" slot width.

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Chapter 2: Installation and Connections

2.1 Inspection

After unpacking the unit, inspect it carefully for possible damage to connectors or components. If any damage is discovered, please contact Pentek immediately, at the phone number shown on this manual's title page. Please save the original shipping container and packing material, in case re-shipment is required.

The Model 6509 contains two printed circuit (PC) assemblies. The board with the VMEbus P1 and P2 connectors (the VME board, Pentek part # 004.65080) contains the VME interface, the 'C40 DSP its associated memory resources, the Comm Ports and the FIFOs. The other board (the Mezzanine board, Pentek part # 004.65091), houses the input connectors and the Digital Receiver circuitry. Drawings of the component sides of both PC assemblies are shown in Figure 2-2 and Figure 2-3, on the next two pages.

2.2 VMEbus A16 Base Address Switches

Three separate address spaces are defined for the VMEbus environment. These three regions are known as A16, A24 and A32. Each device in your VMEbus card cage must have a unique address in any address space in which it must be accessible. On the Model 6509 the A16_base address (i. e., the lowest address in the A16 region occupied by this device) is set by means of two rotary switches. These switches, SW1 and SW2, are located at the top rear of the VME board, with SW1 adjacent to the VME P1 connector, and SW2 directly to the left of SW1. These switches should be set for the desired A16_base address before installing the Model 6509 in the VMEbus card cage. Figure 2-1, below, shows what these switches look like and Figure 2-2, on the next page, shows the location of this pair of switches.

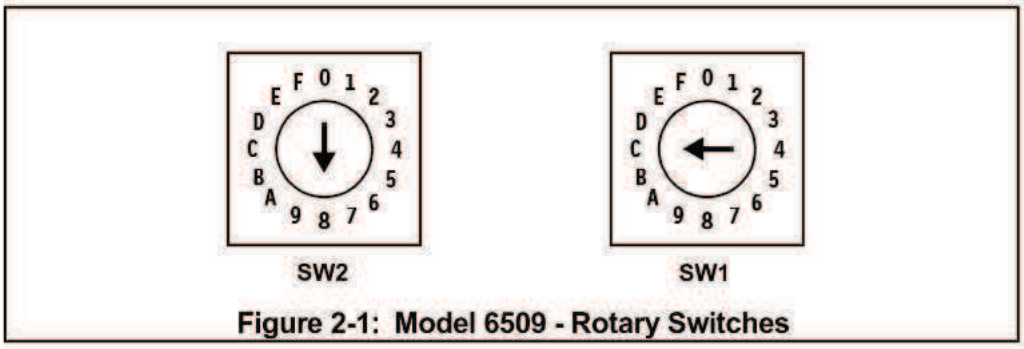


Figure 2-1: Model 6509 - Rotary Switches

The settings of these 16-position rotary switches each define four bits of the 6509's A16_base address. Each of the 16 positions on the switches is denoted with a hex digit (0 - F), whose four-bit binary value will be used as part of the device's base address. SW2 defines the four most significant bits (MSBs) of the address (A15 - A12) and SW1 defines the next four address bits (A11 - A8). Thus, with 16 settings available on each of two switches, one of 256 different base addresses may be selected for any 6509. Figure 2-1, above, shows the switches set for an A16_base address of 0x8C00.

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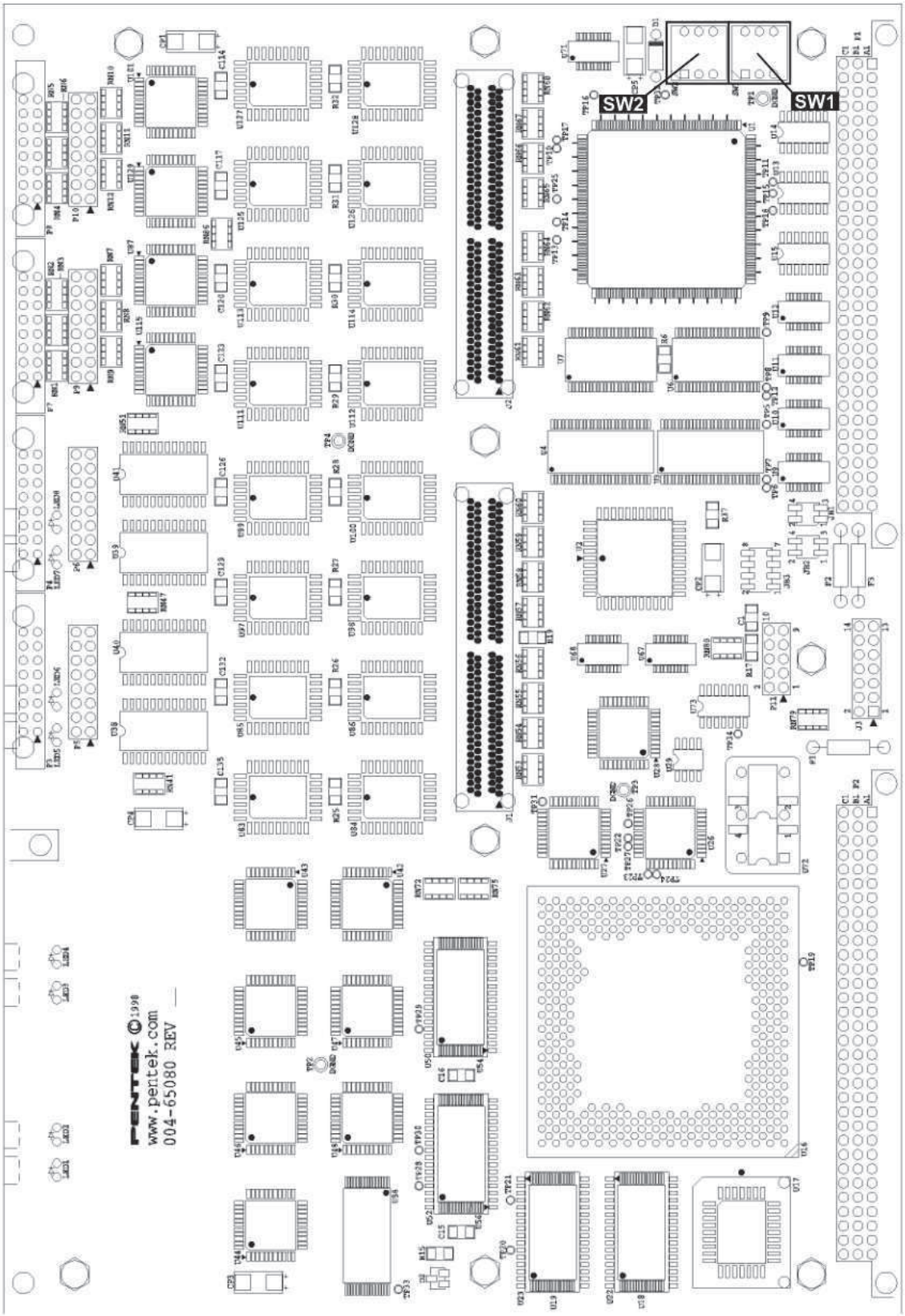


Figure 2-2: Model 6509 - Main Board (Pentek Part # 004.65080), Component Side

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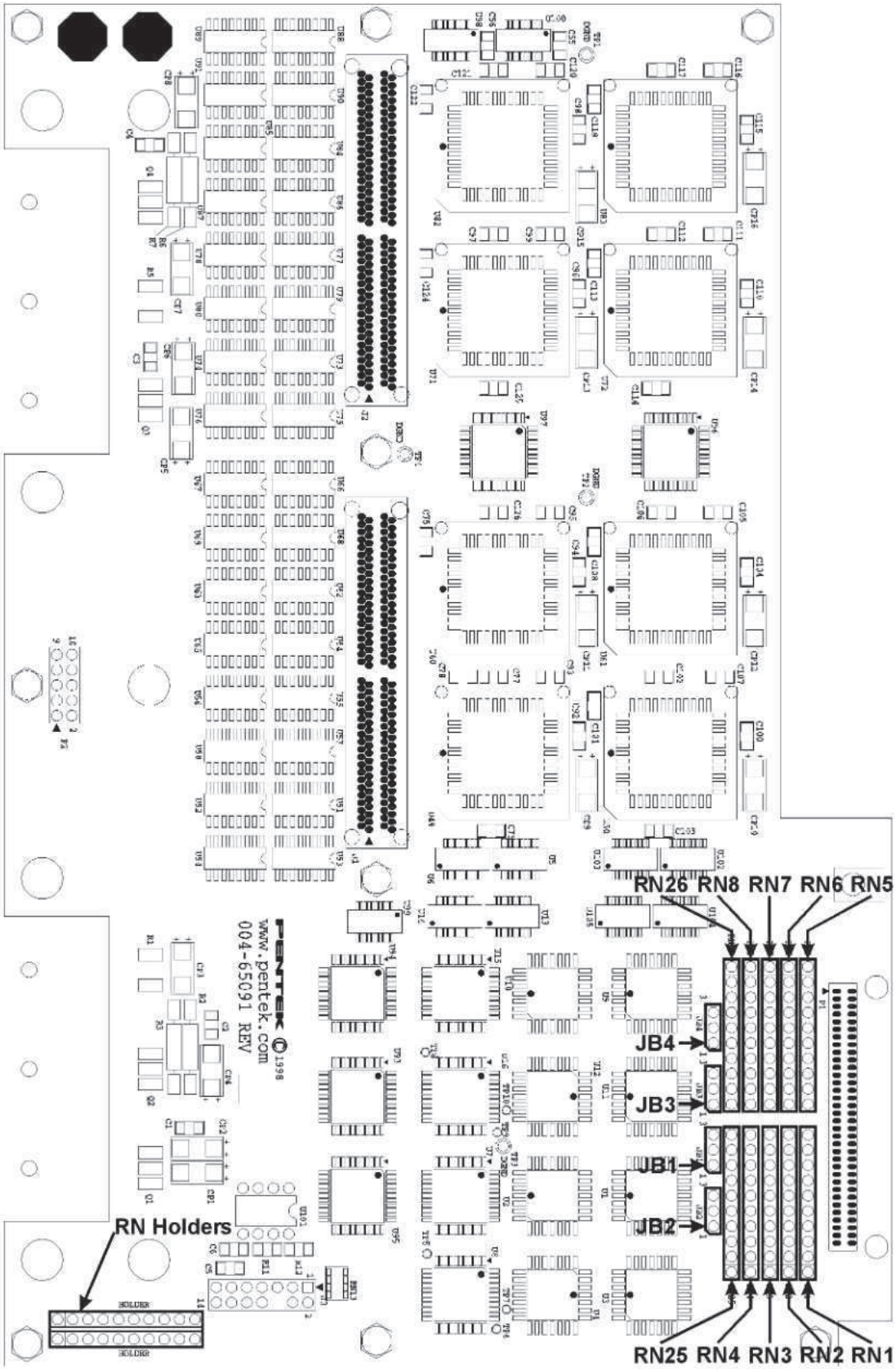


Figure 2-3: Model 6509 - ECL Mezzanine Board (Pentek Part # 004.65091) Showing JB1 - JB4, RN1 - RN8 and RN25 - RN26

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2.2 VMEbus A16 Base Address Switches (continued)

Throughout this manual, all VMEbus addresses will be given as offsets from the assigned base address. For example, the A24 and A32 base addresses for the 6509 are defined by writing to a register at address A16_base+0x04.

2.3 Sync Select Jumper Settings - JB1 thru JB4

In addition to input signal data, pins are provided on each of the Model 6509ís input channel connectors on for two synchronizing signals, the System Sync (SS), and the Accumulator Sync (AS). Each of the input channels can be configured as either a master or a slave. A master channel can drive the sync lines on its input connector (i. e., the syncs lines are outputs for a master), while slave channels accept the sync signals as inputs. (Note that, on master channels, the sync signals are generated in software, see Sections 3.5.8.2 and 3.5.8.3.)

Jumper blocks JB1 - JB4, on the Mezzanine board (004.65091 - see Figure 2-3, on the previous page) are involved in the selection of the sync mode for the input channels on the Model 6509. JB1 & JB2 are associated with Channel A, and JB3 & JB4 are associated with Channel B. JB1 and JB4 are involved with selecting the mode for the Accumulator Sync for the associated channel, and JB2 and JB3 are involved with the selection for the System Sync. A jumper should be placed between pins 1 and 2 of both associated jumper blocks if the channel is a master. If the channel in question will be a slave, jumpers should be placed between pins 2 and 3 of the associated jumper blocks (or may be removed) before the Model 6509 is installed in the VMEbus card cage. Additional information on Sync signals and Master/Slave operation is given in Section 3.5.8, on page 52. Table 2-1, below, summarizes these jumper settings.

Table 2-1: Model 6509 Sync Select Jumper Settings - JB1 thru JB4, 6509 Mezz Board

Channel	Signal	Block	Jumper	Mode
A	AS	JB1	1 - 2*	Master
			2 - 3	Slave
	SS	JB2	1 - 2*	Master
			2 - 3	Slave
B	AS	JB4	1 - 2*	Master
			2 - 3	Slave
	SS	JB3	1 - 2*	Master
			2 - 3	Slave

* - Factory default jumper placement

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2.4 Input Terminating Resistors and Cable Routing

Because of the fast rise and fall times generated by ECL devices, it is important that the cables carrying data to the Model 6509 are treated as high frequency transmission lines (even at lower data rates) and that these lines are terminated properly. Proper transmission line practice dictates that the device driving the signal is placed at one end of the line, and that all the receiving devices are aligned along a single path, without branching. A single terminating resistor for the signal should be placed at the end of the signal path opposite the driver.

The input terminating resistor networks for the Model 6509 (RN1 - RN8 and RN25 - RN26) are socketed, to allow for easy installation and removal. At the factory, 150Ω resistor packages are installed at all of the above locations on the Mezzanine board (004.65091, see Figure 2-3, on the page before the previous). RN1 - RN4 are the terminations for Input Channel Aís data, and RN5 - RN8 terminate the data for Input Channel B. In systems where the same digital input signal will drive multiple channels, the terminating resistors must be removed from all channels except for the last channel on the cable. In such systems, the cabling should be arranged such that the data source drives one end of the cable (i. e., do not place the source device in the center of the card cage and fan out to receivers on both sides). Figure 2-4, below, shows an example of a system involving several 6509s, and illustrates proper routing and termination of the data cables.

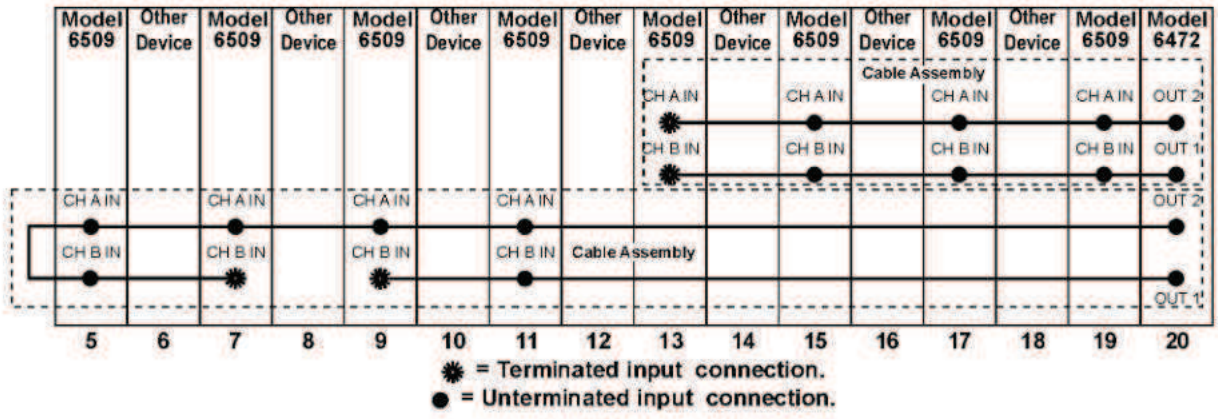


Figure 2-4: Model 6509 - Data Cable Routing and Terminating Example

Figure 2-4 shows the connections that should be made, but does not represent the physical implementation of the ribbon cable. The scheme shown above using the ì topî outputs of the 6472 would involve a simple, 68-wire ribbon cable, with five connectors crimped on in the standard fashion. The arrangement using the ì bottomî outputs of the 6472 would be much more physically complex. For this scheme, you would need to cut the 68-wire cable with a fair amount of extra length. After the output connector and the first two input connectors are crimped across all 68 pins, the cable must be split into two 34-wire sections. The 34 wires coming from OUT 1 on the 6472 can be cut after the second 6509 connector. The remaining 34 lines would need to pass through the A In side of the other two connectors, then folded over itself appropriately so it can pick up the B In side of the same two connectors in the proper orientation.

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2.4 Input Terminating Resistors and Cable Routing (continued)

Special attention should be paid to the resistor packages at locations RN25 and RN26. RN25 is the terminator package for the two sync signals for Channel A and RN26 contains the terminators for Channel Bís sync signals. No other data signals are terminated in these two packages. This allows the sync signals to be routed and terminated differently from the data signals, which may be necessary in systems using master/slave synchronization. As stated above, the sync cable should be routed such that the source of the signals (i. e., the master) drives one end of the cable. Only one terminator should be installed, in the channel at the other end of the signal path.

In situations where both channels in one or more 6509ís are slaves to the same master, some more creativity may be needed in the cabling. Consider the example presented in Figure 2-5, below. This shows a system with four 6509ís where one channel (Channel B in the left-hand unit) is the master, and the other 7 are slaves. The data portion of the cables has been omitted for clarity, but let us also assume that all eight channels receive the same input data from the same A/D, and that the unit on the left (the one with the master channel) is the first in the data chain. In this case, the wires on the ribbon cable that carry the Sync signals (pins 25 - 28 and 60 - 62) should be removed from the ribbon cable in the region between the A/D and the 6509 on the left. Shorting wires should be soldered onto the PC-board pattern for the input connector of the 6509 on the right, between the SS, $\overline{SS}$, AS and $\overline{AS}$ pins for Channels A and B (the pin numbers are shown in the figure). This will arrange the wiring such that the sync signals are driven by the master, travel down the ribbon cable to the other three B Channels, pick up Channel A in the last unit via the shorting wires, then travel back up the ribbon cable to hit the other two A Channels and back into the master unit (where Channel A is a slave) to be terminated.

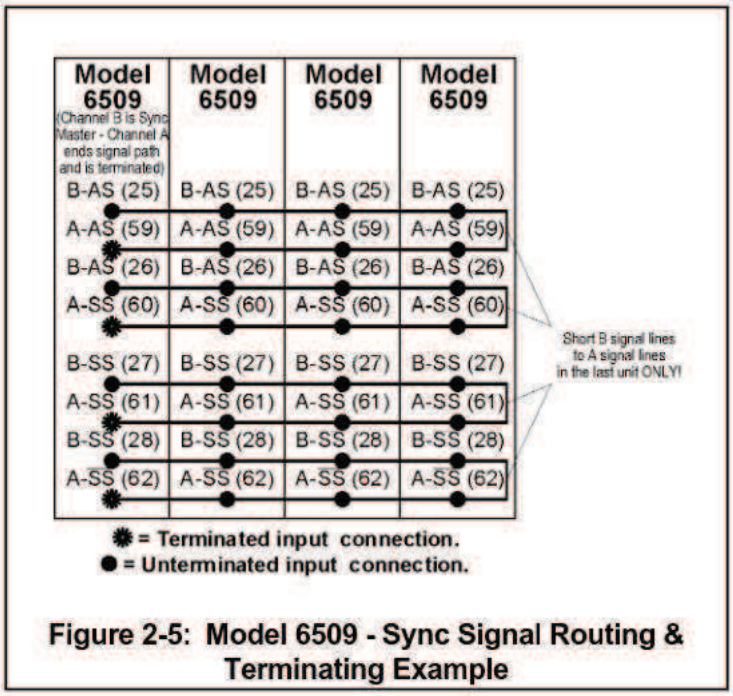


Figure 2-5: Model 6509 - Sync Signal Routing & Terminating Example

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2.5 Model 6509 Front Panel

The front panel of Pentek's Model 6509 Octal Digital Receiver VME-bus Board contains a 68-pin flat cable connector, which can carry two 12-bit input data streams. The panel also has eight Comm Port connectors (four for the receiver data outputs, four for receiver control inputs), two red Overload indicator LEDs, and two green Clock Ready indicator LEDs. The subsections below will discuss the connectors on the front panel, what kinds of connectors can be used to mate with them, and the types of signals that should be applied to them. We will also discuss the LEDs, and describe the conditions they are used to indicate. Figure 2-6, at the right, depicts the front panel of the Model 6509.

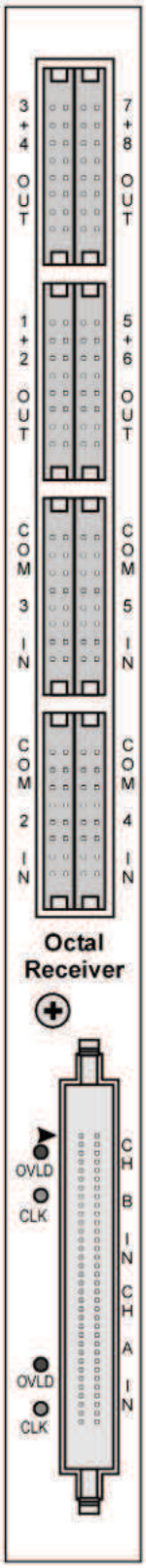


Figure 2-6: Model 6509 Front Panel

2.5.1 Comm Port Connectors

The four connectors at the top of the Model 6509's front panel are 16-pin, dual in-line ribbon cable connectors for the TMS320C40-compatible Comm Port outputs. These ports provide an alternative to the VMEbus for reading data from the Model 6509, in applications where a 'C40 processor will handle the data. **These ports are NOT driven by the on-board 'C40 processor, but are PAL-controlled, and can be connected to a 'C40 input or output Comm Ports. These ports have built-in token forcing.**

Each connector carries data from two receivers. The connector on the top left carries data from receivers 3 & 4, and the connector below it (left, above center) carries data from receivers 1 & 2. The connectors on the right side of the panel carry data from receivers 7 & 8 (top right), and receivers 5 & 6 (right, above center) For details about programming the 6509 to use these ports, please refer to Section 3.5.7 of this manual.

Below the four connectors discussed above are four more physically identical connectors, which are used on the 6509 as input ports for receiver tuning and control information. Unlike the ports described above, however, these ports are connected, through buffers, to four of the Comm Ports on the on-board 'C40 processor. (The input Comm Ports are excluded from Option 040).

These connectors carry signals that eventually find their way to Comm Ports 2, 3, 4 and 5 of the 'C40. As all experienced 'C40 users know, the 'C40's default power up configuration has Comm Ports 0, 1 and 2 configured as outputs, and Comm Ports 3, 4 and 5 configured as inputs. Circuitry is provided to force the token on Comm Port 2, making it an input Port.

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2.5 Model 6509 Front Panel (continued)

2.5.1 Comm Port Connectors (continued)

Figure 2-7, below left, shows the Comm Port pin assignments. The connectors are keyed to prevent improper insertion.

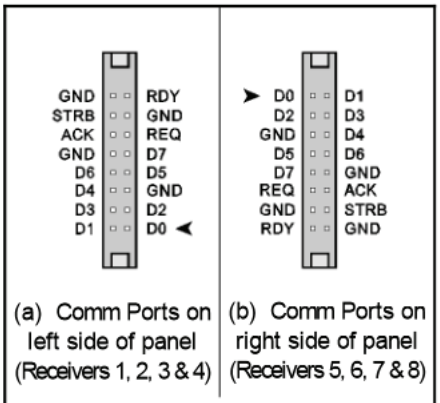


Figure 2-7: Model 6509 - Comm Port Pinouts

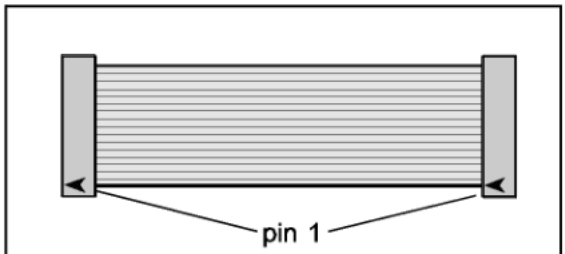


Figure 2-8: Comm Port Cable - Model 2104

Comm Port cables can be easily assembled by using a 3M hand press with locator plate #3443-110 and standard 16-conductor, 0.050 pitch flat ribbon cable such as 3M #3365/16. Every Model 6509 is shipped with four mating connectors (3M #50116-B000) and the optional strain reliefs (3M #3448-50116). The use of these standard components allows the user to easily configure the Comm Port cables to minimize excess cable length for any given interconnect pattern.

As an aid to consistent assembly techniques, make sure that pin 1 of each socket at the end of the cable is connected to pin 1 of the ribbon cable. Pin 1 of the cable is identified by the colored stripe. A typical Comm Port cable is shown in Figure 2-8, at the bottom right of the previous page. Comm Port cables are available preassembled from Pentek as Model 2104 (to mate with the connectors on the Models 4284, 4270, 4269, 4257 and 4254) and Model 2115 (to mate with the connectors on the Model 4285). Cable lengths of up to 18" can be accommodated.

Each of the twelve signal lines on each Comm Port is back-terminated with a series 24Ω resistor to properly match the characteristic impedance of the flat ribbon wiring used in the Comm Port cables.

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2.5 Model 6509 Front Panel (continued)

2.5.2 Digitized Signal Input Connectors

The Model 6509 Option 012 accommodates differential ECL-level input signals from Pentek A/D Converter Models 6402-002, 6410-002, 6441-002, 6470, and 6472. The input circuitry is contained on a daughter card inside the module, called the Mezzanine board.

The input connector is a 68-pin flat ribbon cable header manufactured by 3M. The part number for the header is 3M #81068-620203.

The flat cable socket connector is 3M #82068-6006, and the strain relief is 3M #3858-068. Pentek's Part number for the connector, with the strain relief, is 353.06805. One of each of these items is supplied with the Model 6509. The recommended .025-in. pitch flat ribbon cable is 3M #3756/68.

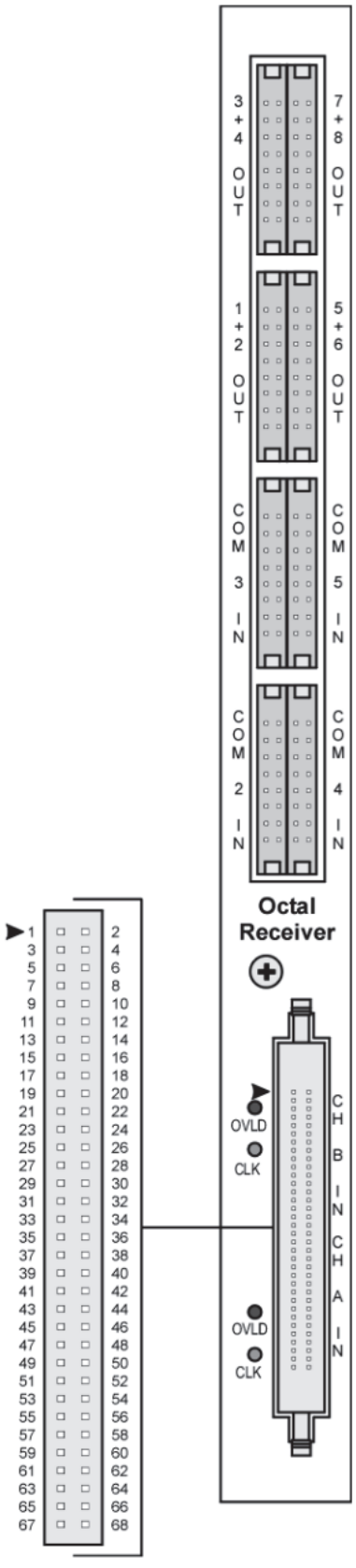
The 68-pin connector is composed of two identical 34-pin groups, one for each input channel. The 68-conductor ribbon cable can be split in half, forming two identical 34-pin cables. The pin assignment for the connector is shown on the next page in Figure 2-9.

For each of the input channels, the input signal consists of 12 differential data lines (D0 - D11), a data strobe (CK), and two sync control lines (SS and AS). Note that each input line has its associated complement opposite it in the charts in Figure 2-9. This creates the optimal signal line sequence in the flat ribbon cable, very desirable in controlling crosstalk and impedance. It is recommended that the driving end of the cable have all of the GND lines connected to signal ground to help maintain signal integrity.

The nominal impedance of the 3M flat cable mentioned above is 85Ω. All input lines are terminated with 150Ω pulldown resistors to -2V. The input circuitry for the 12 data lines and the clock is shown schematically in Figure 2-10, at the top of the next page. The level translator is a type F100325. The 100K ECL family is noted for fast rise and fall times and excellent high-frequency performance. The data register is a type 74FCT574, an edge-sensitive D-type flip-flop. FCT is a high-performance, TTL compatible CMOS logic family manufactured by Integrated Device Technology (IDT), among others. The other lines (SS and AS) may be received as inputs or driven as outputs, depending upon how the device is programmed. The driver is type F100324, also of the 100K ECL family. These lines are terminated by the same type of termination resistor arrangement as the data lines.

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Differential ECL (Option 012) Input Connector - Channel A and B			
Pin #	**Signal**	**Pin #**	**Signal**
1	CHB-D0 (LSB)	2	CHB-$\overline{D0}$ (LSB)
3	CHB-D1	4	CHB-$\overline{D1}$
5	CHB-D2	6	CHB-$\overline{D2}$
7	CHB-D3	8	CHB-$\overline{D3}$
9	CHB-D4	10	CHB-$\overline{D4}$
11	CHB-D5	12	CHB-$\overline{D5}$
13	CHB-D6	14	CHB-$\overline{D6}$
15	CHB-D7	16	CHB-$\overline{D7}$
17	CHB-D8	18	CHB-$\overline{D8}$
19	CHB-D9	20	CHB-$\overline{D9}$
21	CHB-D10	22	CHB-$\overline{D10}$
23	CHB-D11 (MSB)	24	CHB-$\overline{D11}$ (MSB)
25	CHB-AS	26	CHB-$\overline{AS}$
27	CHB-SS	28	CHB-$\overline{SS}$
29	CHB-CKIN	30	CHB-$\overline{CKIN}$
31	GND	32	GND
33	GND	34	GND
35	CHA-D0 (LSB)	36	CHA-$\overline{D0}$ (LSB)
37	CHA-D1	38	CHA-$\overline{D1}$
39	CHA-D2	40	CHA-$\overline{D2}$
41	CHA-D3	42	CHA-$\overline{D3}$
43	CHA-D4	44	CHA-$\overline{D4}$
45	CHA-D5	46	CHA-$\overline{D5}$
47	CHA-D6	48	CHA-$\overline{D6}$
49	CHA-D7	50	CHA-$\overline{D7}$
51	CHA-D8	52	CHA-$\overline{D8}$
53	CHA-D9	54	CHA-$\overline{D9}$
55	CHA-D10	56	CHA-$\overline{D10}$
57	CHA-D11 (MSB)	58	CHA-$\overline{D11}$ (MSB)
59	CHA-AS	60	CHA-$\overline{AS}$
61	CHA-SS	62	CHA-$\overline{SS}$
63	CHA-CKIN	64	CHA-$\overline{CKIN}$
65	GND	66	GND
67	GND	68	GND



The mating flat cable socket connector is 3M #82068-6006, and the strain relief is 3M #3858-068.

One each of these items is supplied with the Model 6509.

The recommended 0.025" pitch flat cable is 3M # 3756/68.

Figure 2-9: Model 6509 - Front Panel Digitized Signal Input Connector - Pin Assignments

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2.5 Model 6509 Front Panel (continued)

2.5.2 Digitized Signal Input Connectors (continued)

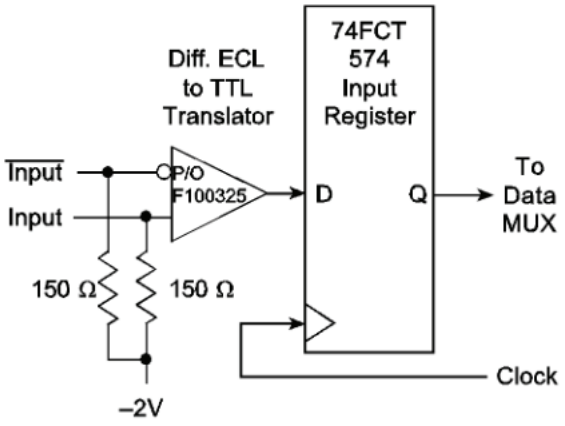


Figure 2-10: Model 6509 - Typical Data Line Input Circuitry

2.5.3 LED Indicators

Two LED indicators are provided for each input channel. These will be discussed in the subsections below.

2.5.3.1 Clock (CLK) LED (Green)

The green LED for a given input channel will be lit when a clock signal for that channel is detected. If this LED is not lit, then no clock signal has been detected and no data from this stream can be processed.

2.5.3.2 Overload (OVLD) LED (Red)

The red LED for a given input channel was initially intended as an indicator for the threshold detection function (hence the name), and may still be used as such if desired. The states of these LEDs are controlled by two user-addressable bits in the Input Control Registers. See Section 3.5.8.1 for further details.

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2.6 Inserting and Removing the Model 6509 in the VMEbus Card Cage

CAUTION!!

Never INSERT or REMOVE the Model 6509 while card cage power is turned on!

2.6.1 Inserting the Unit

Align the Model 6509 card edge with the cage card guides and push evenly on both ejector handles until the front panel seats against the upper and lower rails. Secure the unit in the cage by tightening the upper and lower retaining screws in the front panel.

2.6.2 Removing the Unit

Loosen the upper and lower retaining screws; they are captive screws and will remain part of the panel assembly. Gently push both ejector handles apart (away from the center of the panel) until the unit unseats itself from the cage connectors. Then pull outward to remove the unit.

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Chapter 3: Memory Maps and Register Descriptions

3.1 Programming Overview

The Model 6509 is controlled by commands sent over the VMEbus to memory-mapped control registers. Each of these registers will be described in detail in this chapter. The 6509 acts as a VMEbus slave device.

Six control registers (five associated with VMEbus operations and the other with the Test Bus Controller) are mapped into the Model 6509's VMEbus A16 memory space. Access to this address space is determined by the A16 Base Address Switches, which are described in Section 2.2. All control register addresses are given as offsets from the base address defined by the settings of these switches. The form used is A16_base+0xYZ, where YZ is the hexadecimal offset from the Base Address. A VMEbus memory map to all the Model 6509's registers is included in this chapter.

The data FIFO memories and the control registers associated with Digital Receiver operations are mapped into A24 and/or A32 VMEbus memory space(s). These resources can also be accessed by the 'C40 processor, on its global bus. This chapter also includes complete memory maps for the 'C40 (both the local and global busses) and for VMEbus A24/A32 space.

3.2 VMEbus Address Modifier Codes

There are three addressing modes defined for VMEbus transfers: 32-bit, 24-bit and 16-bit modes. These modes are provided to support a variety of bus devices ranging from simple I/O functions with only a few memory locations to large RAM arrays with hundreds of Megabytes of storage. The addressing mode used for a given transaction is determined by a special 6-bit code that is placed on six dedicated VMEbus lines by the current bus master. This code is known as the Address Modifier, or AM, code.

The VMEbus specification defines the usage of certain AM codes as shown in Table 3-1, at the top of the next page. The Model 6509 responds only to those codes shown in the table.

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3.2 VMEbus Address Modifier Codes (continued)

Table 3-1: VMEbus Address Modifiers	
AM Code	**Access**
0x3F	A24 - Standard Supervisory Block Transfer
0x3D	A24 - Standard Supervisory Data Access
0x3B	A24 - Standard Nonprivileged Block Transfer
0x39	A24 - Standard Nonprivileged Data Access
0x2D	A16 - Short Supervisory Access
0x29	A16 - Short Non-Privileged Access
0x0F	A32 - Extended Supervisory Block Transfer
0x0D	A32 - Extended Supervisory Data Access
0x0B	A32 - Extended Nonprivileged Block Transfer
0x09	A32 - Extended Nonprivileged Data Access
NOTE: The model 6509 will **ONLY** respond to the address modifier codes shown in this table.	

3.3 VMEbus Access

The Model 6509 presents two distinct memory maps to VMEbus masters, one in A16 space and another in A32 and/or A24 space. When power is initially applied to this device, only A16 access is enabled. The 6509 occupies 256 bytes of VME A16 memory. A32 access is enabled by the first write to the VMEbus Address Register. Once enabled, A32 access cannot be disabled without cycling power or resetting the device. Block access is permitted in A32 space only (A24 block accesses (AM codes 0x3F and 0x3B) will be DTACKed by the 6509, but no block transfers can be conducted with those modifiers). The 6509 occupies 4 MBytes of A32 VMEbus memory. A bit is provided in the VME Address register to enable A24 access. When A24 Access is enabled, the 6509 will occupy 1 MByte of A24 memory AND 4 MBytes of A32 memory. The resources available in A16 space are accessible exclusively to the VMEbus. Those in the A24 and A32 memory maps can also be accessed by the on-board 'C40 processor.

The sections that follow will present the memory maps for all the resources available on the Model 6509. A16-accessible resources will be discussed first. Each section will provide a table giving the memory map for the address space in question, and then describe the registers and other available resources.

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3.4 VMEbus A16 Slave Memory Map

The memory address map for the six resources available in VMEbus A16 space on the Model 6509 is given in Table 3-2, below. Note that most of these resources are accessible for both read and write operations. The exceptions are the VME-to-'C40 interrupt address, which is accessible only for write operations, and the VMEbus Status Register, which is accessible only for read operations. To access these registers, the bus master that conducts the read or write cycle must select A16 address space by using AM code 2D or 29 (see Table 3-1, previous page). All resources on the Model 6509 are mapped on 4-byte boundaries (i. e., the least significant hex address digit is either 0, 4, 8 or C), to simplify master access to the board by DSP-based devices that use 32-bit addressing, such as Pentek's Models 4283, 4284 and 4285.

Table 3-2: Model 6509 - VMEbus A16 Slave Memory Map

Address	Access	Resource	Symbolic Name
A16_base+0x00	R/W	VMEbus Control Register	Ctrl_Reg
A16_base+0x04	R/W	VMEbus Address Register	Addr_Reg
A16_base+0x08	W. O.	VMEbus Interrupt to 'C40	C40_Int
A16_base+0x0C	R/W	Global Bus Address Page Register	Page _Reg
A16_base+0x10	R. O.	VMEbus Status Register	VME_Stat
A16_base+0x80 - A16_base+0xFF	R/W	Test Bus Controller Registers	TBC

All VMEbus A16 space addresses are expressed in hexadecimal notation, as offsets from the A16_base address. This address is determined by the settings of the two 16-position rotary switches, SW1 and SW2 (see Section 2.2). The A16 memory space occupied by this device is a 256-byte block starting at the A16_base address. All accesses within this region will cause the 6509 to handshake with the VMEbus, **and no other VMEbus device may be mapped within this same 256-byte region of A16 address space**. If more than one 6509 will be used in the same card cage, the A16 Base Address switches must be set to give each board a unique address.

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3.4 VMEbus A16 Slave Memory Map (continued)

3.4.1 VMEbus Control Register - R/W @ A16_base+0x00

The VMEbus Control Register contains an 8-bit IACK Vector field and a 3-bit IRQ Level field. It also has individual bits that can reset the entire board or just the 'C40 processor, a bit that determines the source of the code that will be used to boot the 'C40 and a bit to enable VME access to the Test Bus Controller. Table 3-3, below, shows the bit arrangement within the Model 6509's VMEbus Control Register. The subsections that follow the table give detailed descriptions of these bits and bit fields.

Table 3-3: Model 6509 - VMEbus Control Register - R/W @ A16_base+0x00

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	Not Used	C40_Boot_Source	TBC_Enable	C40_Reset	Board_Reset	IRQ_Level_Select_2	IRQ_Level_Select_1	IRQ_Level_Select_0
Bit Function	Write 0, Mask on Reads	1=CommPort 0 = EEPROM	1 = Enabled 0 = Disabled	1 = Reset 0 = Run	1 = Reset 0 = Run	1,1,1=IRQ7 1,1,0=IRQ6 1,0,1=IRQ5 1,0,0=IRQ4 0,1,1=IRQ3 0,1,0=IRQ2 0,0,1=IRQ1 0,0,0=None		
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Field	VMEbus IACK Vector Address							
Destination	VME_D07	VME_D06	VME_D05	VME_D04	VME_D03	VME_D02	VME_D01	VME_D00

3.4.1.1 C40 Boot Source Select - D14

When this bit is cleared to the logic '0' state, the 'C40 processor on the Model 6509 will boot from the code contained in the unit's EEPROM, at 'C40 address 0x0030 0000. This is the default case. Setting this bit to the logic '1' state, and toggling (i. e., writing a '1', then a '0') the 'C40 Reset bit (D12 in this register, see Section 3.4.1.3) will cause the 'C40 to look to its Comm Ports for boot code.

Remember, however, that on the Model 6509, half of the Front Panel Comm Ports (the four at the top of the panel) are PAL based, output-only devices, and are unconnected to the 'C40. Only the four Comm Ports in the middle of the panel are usable as inputs, for boot code or other purposes. This feature is also very useful in units equipped with Option 034, in which the 'C40's Comm Ports are wired out to the VMEbus P2 connector. When instructed to boot from the Comm Ports, the 'C40 polls the ports and attempts to boot from the first port at which data is found.

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3.4 VMEbus A16 Slave Memory Map (continued)

3.4.1 VMEbus Control Register (continued)

3.4.1.2 Test Bus Controller Enable - D13

The 74ACT8990 is used as a JTAG-compliant Test Bus Controller on the Model 6509. To enable access to the ëC40 JTAG Interface from the VMEbus, set this bit to the logic '1' state. When this bit is cleared to the logic '0' state (the default state after power-up or reset), JTAG access to the ëC40 is disabled. For more information about the 74ACT8990, please refer to Texas Instruments' **Advanced Logic and Bus Interface Logic Data Book**.

3.4.1.3 ëC40 Reset - D12

The Model 6509's 'C40 Processor will be held in its Reset state whenever this bit is set to the logic '1' state. To release the 'C40 and allow it to operate normally, this bit must be cleared to the logic '0' state. The 'C40 Reset function should be implemented as a toggle, i. e., this bit should be set to logic '1', then cleared back to '0'.

Note that this bit affects the processor only, not the Digital Receiver chips or the data FIFOs.

3.4.1.4 Board Reset - D11

All circuits and devices on the Model 6509 (including the 'C40 processor, the Digital Receiver Chips, and the data FIFOs) will be held in the Reset state while this bit is in the logic '1' state. For normal operation of the digital receiver board, this bit must be cleared to the logic '0' state. The software reset function should be implemented as a toggle, i. e., this bit should be set to logic '1', then cleared back to '0'.

3.4.1.5 VMEbus IRQ Level Select - D10 through D8

This bit field should be written with the binary code for the desired VMEbus Interrupt Requester level for the Model 6509 (see Table 3-3, on the previous page). Clearing all three of these bits to the logic '0' state will disable the 6509's Interrupter interface.

3.4.1.6 VMEbus IACK Vector Address - D7 through D0

This 8-bit field is used to store the IACK Vector Address, which will be placed on the VME Data bus when the Model 6509 issues an interrupt to VME. Table 3-3, on the previous page, shows the correspondence between the bits in this register and the VME Data Bus lines that are their destinations.

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3.4 VMEbus A16 Slave Memory Map (continued)

3.4.2 VMEbus Address Register - R/W @ A16_base+0x04

This 16-bit register contains a 10-bit field used for the VME A32 base address, a 4-bit field used for the VME A24 base address, a bit to enable A24 space VME slave access, and a Word Swap bit. A32 VME slave access is enabled by the first write operation to this register. Table 3-4, below, shows the arrangement of bits in the 6509's VMEbus Address Register. The subsections that follow the table will provide more details about the register's bit fields and bits.

Table 3-4: Model 6509 - VMEbus Address Register - R/W @ A16_base+0x04

Bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6
Bit Field	A32 Base Address									
Match	VME_A31	VME_A30	VME_A29	VME_A28	VME_A27	VME_A26	VME_A25	VME_A24	VME_A23	VME_A22

Bit #	D5	D4	D3	D2	D1	D0
Bit Name	A24_Enable	A24 Base Address				Word_Swap
Bit Function	1 = Enable 0 = Disable	VME_A23	VME_A22	VME_A21	VME_A20	1 = Swap 0 = No Swap

3.4.2.1 A32_Base Address - D15 through D6

When power is initially applied to the Model 6509 (or after a reset), the only enabled VMEbus interface is the A16 space slave. A32 slave access is enabled by the first write to this register, at the address written to the register's ten most significant bits. The bits in D15 - D6 in this register will be compared to the VMEbus A31 - A22 address lines, respectively, to determine if the 6509 is being addressed during a VME transaction. Once this register has been written, the only way to disable A32 slave access to the 6509 is to reset it (see Section 3.4.1.4), or to cycle power.

3.4.2.2 A24 Enable - D5

When this bit is cleared to the logic '0' state (the power-up default condition), A24 slave access to the 6509 is disabled. To enable A24 access, set this bit to the logic '1' state and write the desired base address to bits D4 - D1 in this register (see Section 3.4.2.3, next page). Note that, because the first write to this register enables A32 slave access, it is not possible to enable A24 access to the 6509 without also enabling A32 access.

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3.4 VMEbus A16 Slave Memory Map (continued)

3.4.2 VMEbus Address Register (continued)

3.4.2.3 A24_Base Address - D4 through D1

When A24 slave access to the 6509 is enabled (see Section 3.4.2.2, previous page) the 6509 will respond to VME data cycles in A24 space when VME address bits A23 - A20 match the contents of bits D4 - D1 in this register, respectively.

3.4.2.4 Word Swap - D0

Word Swap Mode is used to allow Intel type processors to access the 6509's memory, by setting D0 in this register to a ë1í. Leave this bit in the ë0í state if you are working with a Motorola host.

This is a very common function in VME cards. Remember that Intel and Motorola processors address words differently; with an Intel host, the upper 16 bits of the 32 bit longword are stored at locations with the VME address line A1 = '1'. A Motorola host stores those same bits at locations with A1 = '0'.

3.4.3 VMEbus Interrupt to ëC40 - W. O. @ A16_base+0x08

Any VMEbus write operation to this address will cause an interrupt to be asserted on the 6509's 'C40 processor. This interrupt will drive the IIOF1 input of the 'C40. Since this device is not a VMEbus interrupt handler, the assertion of this interrupt will not result in a VMEbus IACK cycle. The data written during this operation is neither used nor stored and is therefore trivial.

3.4.4 Global Bus Address Page Register - R/W @ A 16_base+0x0C

This register allows the VMEbus to access resources on the 'C40's Global bus, when Global bus address bits above A19 are required (this corresponds to VME address bit A21; remember that the A32_base address uses VME address bits A31 - A22). The bits in this register are mapped to 'C40 Global address bits A27 - A20, which correspond to VME address bits A29 - A22, as shown in Table 3-5, below.

Table 3-5: Model 6509 - Global Bus Address Page Register - R/W @ A16_base+0x0C

Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Field	Global Bus Address Page							
Global Bits	Gbus_A27	Gbus_A26	Gbus_A25	Gbus_A24	Gbus_A23	Gbus_A22	Gbus_A21	Gbus_A20
VME Bits	VME_A29	VME_A28	VME_A27	VME_A26	VME_A25	VME_A24	VME_A23	VME_A22

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3.4 VMEbus A16 Slave Memory Map (continued)

3.4.5 VME Status Register - R. O. @ A16_base+0x10

Only two of the 16 bits in this register are used. One indicates whether an interrupt to the ëC40 processor is pending, and the other gives the status of the Test Bus Controller. Table 3-6, below, shows the registerís bit arrangement. The subsections below the table describe the status bits.

Table 3-6: Model 6509 - VMEbus Status Register - R. O. @ A16_base+0x10

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	Pending_C40 _Interrupt	Not Used	TBC_ Ready	Not Used				
Bit Function	1 = True 0 = False	Mask when Reading	1=Not Ready 0=Ready	Mask when Reading.				
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	Not used							
Bit Function	Mask when Reading.							

3.4.5.1 Pending ëC40 Interrupt - D15

This bit will read back on the logic '1' state when the VMEbus has issued an interrupt to the 'C40 Processor that has not yet been acknowledged. Write operations to this bit have no effect. VME interrupts are issued by writing to the A16 VME address A16_base+0x08. The 'C40 acknowledges this interrupt by writing to address 0x8004 0000 in its Global memory map.

3.4.5.2 TBC_Ready - D13

If this bit reads back in the logic ë0í state, the JTAG Interface to the Model 6509ís ëC40 processor is ready for use. When the JTAG interface is busy, this bit will read back in the logic ë0í state. For further information on the use of this interface, please refer to the 74ACT8990 Data Sheet in Texas Instruments' **Advanced Logic and Bus Interface Logic Data Book**.

3.4.6 Test Bus Controller Registers - R/W from A16_base+0x80 to A16_base+0xFF

A JTAG-compliant interface to the Model 6509ís on-board TMS320C40 processor is provided by the Texas Instruments 74ACT8990. The register set of this device can be accessed from the VMEbus in the address range beginning at 0x80 and ending at 0xFF. for further information on these registers and their functions, please refer to the 74ACT8990 Data Sheet in Texas Instruments' **Advanced Logic and Bus Interface Logic Data Book**.

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3.5 ëC40 Global and VMEbus A32/A24 Slave Memory Map

Table 3-7, below, shows the memory map for the resources shared by the VMEbus and the 'C40 processor on the 6509. The term VME_base is used for the A32 or A24 base address, depending upon the address modifier in use. The table gives both VME and 'C40 addresses for each resource. The subsections that begin on the next page describe these resources in detail.

Table 3-7: Model 6509 - Dual-Mapped Resources - ëC40 Global and VMEbus A32/A24 Slave Address Spaces

Symbolic Name	Resource	Size	Access	VME Address	ëC40 Address
SRAM	Global SRAM	128k x 32	R / W	VME_base+0x0000 0000 - VME_base+0x0007 FFFF	0x8000 0000 - 0x8001FFFF
C40_Int_Mask_1	ëC40 Interrupt Mask Register #1	1 x 32	R / W	VME_base+0x0008 0000	0x8002 0000
C40_Int_Mask_2	ëC40 Interrupt Mask Register #2	1 x 16	R / W	VME_base+0x0008 8000	0x8002 2000
Rec_Stat_Reg_1	Receiver Status Register #1	1 x 32	R. O.	VME_base+0x0009 0000	0x8002 4000
Rec_Stat_Reg_2	Receiver Status Register #2	1 x 16	R. O.	VME_base+0x0009 8000	0x8002 6000
F_Rst_Reg	FIFO Reset Register	1 x 16	R / W	VME_base+0x000A 0000	0x8002 8000
Out_Comm_Ctl	Output Comm Port Control Register	1 x 16	R / W	VME_base+0x000A 8000	0x8002 A000
Gray_1_Regs	Graychip #1 Registers	16 x 8	R / W	VME_base+0x000B 8000 - VME_base+0x000B 803F	0x8002 E000 - 0x8002 E00F
Gray_2_Regs	Graychip #2 Registers	16 x 8	R / W	VME_base+0x000B 8040 - VME_base+0x000B 807F	0x8002 E010 - 0x8002 E01F
Gray_3_Regs	Graychip #3 Registers	16 x 8	R / W	VME_base+0x000B 8080 - VME_base+0x000B 80BF	0x8002 E020 - 0x8002 E02F
Gray_4_Regs	Graychip #4 Registers	16 x 8	R / W	VME_base+0x000B 80C0 - VME_base+0x000B 80FF	0x8002 E030 - 0x8002 E03F
Gray_5_Regs	Graychip #5 Registers	16 x 8	R / W	VME_base+0x000B 8100 - VME_base+0x000B 813F	0x8002 E040 - 0x8002 E04F
Gray_6_Regs	Graychip #6 Registers	16 x 8	R / W	VME_base+0x000B 8140 - VME_base+0x000B 817F	0x8002 E050 - 0x8002 E05F
Gray_7_Regs	Graychip #7 Registers	16 x 8	R / W	VME_base+0x000B 8180 - VME_base+0x000B 81BF	0x8002 E060 - 0x8002 E60F
Gray_8_Regs	Graychip #8 Registers	16 x 8	R / W	VME_base+0x000B 81C0 - VME_base+0x000B 81FF	0x8002 E070 - 0x8002 E07F
Gray_W_All	Write All Graychip Registers	16 x 8	W. O.	VME_base+0x000B 8200 - VME_base+0x000B 823F	0x8002 E080 - 0x8002 E08F
Mode Ch_A_Ctl	Mode Select / Channel A Control Register	1 x 16	R / W	VME_base+0x000B 8240	0x8002 E090
Tag_En_Ch_B_Ctl	Tag Enable / Channel B Control Register	1 x 16	R / W	VME_base+0x000B 8280	0x8002 E0A0
In_Mux_Reg	Input Multiplex Register	1 x 16	R / W	VME_base+0x000B 8300	0x8002 E0C0
Thr_Det_A	Chan. A Threshold Detection Register	1 x 16	R / W	VME_base+0x000B 8340	0x8002 E0D0
Thr_Det_B	Chan. B Threshold Detection Register	1 x 16	R / W	VME_base+0x000B 8380	0x8002 E0E0
FIFO_1	Receiver 1 FIFO	8k x 16	R. O.	VME_base+0x000C 0000 - VME_base+0x000C 7FFF	0x8003 0000 0x8003 1FFF
FIFO_2	Receiver 2 FIFO	8k x 16	R. O.	VME_base+0x000C 8000 - VME_base+0x000C FFFF	0x8003 2000 - 0x8003 3FFF
FIFO_3	Receiver 3 FIFO	8k x 16	R. O.	VME_base+0x000D 0000 - VME_base+0x000D 7FFF	0x8003 4000 - 0x8003 5FFF
FIFO_4	Receiver 4 FIFO	8k x 16	R. O.	VME_base+0x000D 8000 - VME_base+0x000D FFFF	0x8003 6000 - 0x8003 7FFF
FIFO_5	Receiver 5 FIFO	8k x 16	R. O.	VME_base+0x000E 0000 - VME_base+0x000E 7FFF	0x8003 8000 - 0x8003 9FFF
FIFO_6	Receiver 6 FIFO	8k x 16	R. O.	VME_base+0x000E 8000 - VME_base+0x000E FFFF	0x8003 A000 - 0x8003 BFFF
FIFO_7	Receiver 7 FIFO	8k x 16	R. O.	VME_base+0x000F 0000 - VME_base+0x000F 7FFF	0x8003 C000 - 0x8003 DFFF
FIFO_8	Receiver 8 FIFO	8k x 16	R. O.	VME_base+0x000F 8000 - VME_base+0x000F FFFF	0x8003 E000 - 0x8003 FFFF
C40_IACK	ëC40 Interrupt Acknowledge Address	1 x 16	W. O.*	VME_base+0x0010 0000	0x8004 0000
VME_Int	ëC40 Interrupt to VMEbus	1 x 16	W. O.*	VME_base+0x0014 0000	0x8005 0000
Flash	Global Flash EEPROM	512k x 8	R / W*	VME_base+0x0020 0000 - VME_base+0x003F FFFF	0x8008 0000 - 0x800F FFFF

* - C40_IACK, VME_Int and Flash are accessible to the ëC40 and in A32 VME space only (i. e., these resources cannot be accessed in VME A24 space.)

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3.5 ëC40 Global and VMEbus A32/A24 Slave Memory Map (continued)

3.5.1 Global SRAM - R/W @ SRAM

A 512 kByte (128 kLongword) bank of shared SRAM is provided for data to be shared by VMEbus masters and the 6509's 'C40 processor. This bank occupies VME memory space from the VME_base address to VME_base+0x0007 FFFF, and 'C40 memory space from address 0x8000 0000 to address 0x8001 FFFF. Remember that each 'C40 longword address is equivalent to four VMEbus byte addresses.

3.5.2 ëC40 Interrupt Mask Register #1 - R/W @ C40_Int_Mask_1

This 32-bit register can be accessed by the 'C40 processor and by the VMEbus. The upper 8 bits are unused, and should be written with zeros and masked when read. Two bits (one associated with each input channel) in the next lower byte field are used enable or disable (i. e., mask) generation of a 'C40 interrput when the Threshold Detector flags go true. The next lower byte field also contains only two active bits (one for each channel), used for 'C40 interrupts based on the state of the Clock Not Ready flags. The lowest byte field contains one bit associated with each digital receiver, and is used for FIFO Full interrupts to the 'C40 processor. All of the interrupts under this register's control will be asserted on the IIOF0 input of the 'C40 processor. Table 3-8, below, shows the bit arrangement within 'C40 Interrupt Mask Register #1. The subsections beginning on the next page give detailed descriptions of the register's bit fields.

Table 3-8: Model 6509 - ëC40 Interrupt Mask Register #1 - R/W @ C40_Int_Mask_1

Bit #	D31	D30	D29	D28	D27	D26	D25	D24
Bit Field	Not Used (Write as 0, mask when reading)							
Bit #	D23	D22	D21	D20	D19	D18	D17	D16
Bit Field	Threshold Detector interrupts							
I/P Channel	Reserved			Channel B	Reserved			Channel A
Bit Function	Write as 0, Mask when reading			1 = Enabled 0 = Masked	Write as 0, Mask when reading			1 = Enabled 0 = Masked
Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Field	Clock Not Ready Flag Interrupts							
I/P Channel	Reserved			Channel B	Reserved			Channel A
Bit Function	Write as 0, Mask when reading			1 = Enabled 0 = Masked	Write as 0, Mask when reading			1 = Enabled 0 = Masked
Bit #	D7	D6	D5	D4	D3	D2	D1	D0
Bit Field	FIFO Full Flag Interrupts							
Receiver #	Receiver 8	Receiver 7	Receiver 6	Receiver 5	Receiver 4	Receiver 3	Receiver 2	Receiver 1
Bit Function	1 = Interrupt Enabled 0 = Interrupt Masked							

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3.5 ëC40 Global and VMEbus A32/A24 Slave Memory Map (continued)

3.5.2 ëC40 Interrupt Mask Register #1 (continued)

3.5.2.1 Threshold Detector Interrupts - D20 & D16

Setting either of these two bits to the logic '1' state will cause a 'C40 interrupt to be generated when the Threshold Detector Flag becomes true for the input channel associated with the given bit. Threshold interrupts will be asserted on the 'C40's IIOF0 input. These interrupts are disabled for those channels whose associated bits in this field are cleared to the logic '0' state.

The threshold conditions for a given input channel are determined by that channel's Threshold Detection Register. See Section 3.5.12 for information about these registers.

NOTE: The other six bits in this 8-bit field (D23, D22, D21, D19, D18 & D17) are reserved. They should **ALWAYS** be written with logic '0's and masked when read.

3.5.2.2 Clock Not Ready Flag Interrupts - D12 & D8

Setting either of these two bits to the logic '1' state will cause a 'C40 interrupt to be generated when the clock signal is not detected on the input channel associated with a given bit. Clock interrupts will be asserted on the 'C40's IIOF0 input. These interrupts are disabled for those channels whose associated bits in this field are cleared to the logic '0' state.

NOTE: The other six bits in this 8-bit field (D15, D14, D13, D11, D10 & D9) are reserved. They should **ALWAYS** be written with logic '0's and masked when read.

3.5.2.3 FIFO Full Flag Interrupts - D7 through D0

Setting any of these eight bits to the logic '1' state will cause a 'C40 interrupt to be generated when the data FIFO for the associated receiver becomes full. FIFO Full interrupts will be asserted on the 'C40's IIOF0 input. These interrupts are disabled for receivers whose associated bits in this field are cleared to the logic '0' state. The FIFO Full interrupt is often used to indicate that data has been lost in a real-time system.

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3.5 ëC40 Global and VMEbus A32/A24 Slave Memory Map (continued)

3.5.3 ëC40 Interrupt Mask Register #2 - R/W @ ëC40_Int_Mask_2

This 16-bit register, which can be accessed by the 'C40 processor and by the VMEbus, contains two 8-bit fields. Each field contains one bit associated with each digital receiver. One field will enable or disable (i. e., mask) generation of 'C40 interrupts when the FIFO Half-Full flags go true. The other is used for FIFO Not Empty interrupts to the 'C40. Table 3-9, below, shows the bit arrangement within Interrupt Mask Register #2. The subsections beginning below the table give detailed descriptions of the register's bit fields.

Table 3-9: Model 6509 - ëC40 Interrupt Mask Register #2 - R/W @ C40_Int_Mask_2

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Field	FIFO Half-Full Flag Interrupts							
Receiver #	Receiver 8	Receiver 7	Receiver 6	Receiver 5	Receiver 4	Receiver 3	Receiver 2	Receiver 1
Bit Function	1 = Interrupt Enabled 0 = Interrupt Masked							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Field	FIFO Not Empty Flag Interrupts							
Receiver #	Receiver 8	Receiver 7	Receiver 6	Receiver 5	Receiver 4	Receiver 3	Receiver 2	Receiver 1
Bit Function	1 = Interrupt Enabled 0 = Interrupt Masked							

3.5.3.1 FIFO Half Full Flag Interrupts - D15 through D8

Setting any of these eight bits to the logic '1' state will cause a 'C40 interrupt to be generated when the data FIFO for the associated receiver has reached the half-full point. FIFO Half-Full interrupts will be asserted on the 'C40's IIOF3 input. These interrupts are disabled for receivers whose associated bits in this field are cleared to the logic '0' state.

The FIFO Half-full condition is often used in real-time systems to trigger the FIFO readout routine. This prevents the data loss that can occur if one waits until the FIFO is full, and reduces the one-sample-at-a-time processing overhead associated with the use of the FIFO Not Empty condition.

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3.5 ëC40 Global and VMEbus A32/A24 Slave Memory Map (continued)

3.5.3 ëC40 Interrupt Mask Register #2 (continued)

3.5.3.2 FIFO Not Empty Flag Interrupts - D7 through D0

Setting any of these eight bits to the logic '1' state will cause a ëC40 interrupt to be generated when the data FIFO for the associated receiver contains at least one sample. FIFO Empty interrupts will be asserted on the 'C40's IIOF2 input. These interrupts are disabled for receivers whose associated bits in this field are cleared to the logic '0' state. The FIFO Not Empty condition is usually used in systems where the data rate is low and the processor is relatively unburdened.

3.5.4 Receiver Status Register #1 - R. O. @ Rec_Stat_Reg_1

This 32-bit, read-only register, which can be accessed by the 'C40 processor and by the VMEbus, contains a bit associated with VMEbus interrupt status and a 2-bit field associated with the Front Panel Clock LEDs in its most significant byte field. The next two lower byte fields each use two bits to show the status of the Overload and Clock Not ready flags for each input channel. The least significant byte field uses all eight bits to give the Full Flag status for each receiverís FIFO. Write operations to this register will have no effect. Table 3-10, at the top of the next page, shows the bit arrangement within Receiver Status Register #1. The subsections beginning at the top of the next page give detailed descriptions of the register's bit fields.

3.5.4.1 ëC40 Interrupt to VMEbus Status Bit - D31

When this bit reads back on the logic '1' state, it indicates that a VMEbus interrupt issued by the 6509's 'C40 processor has not yet been acknowledged. It is set to the logic '1' (true) state when the 'C40 writes to address 0x8005 0000 in its Global Bus memory map (the VME_Int address, see Table 3-7 and Section 3.5.15). The bit is cleared to the logic '0' state during the VMEbus IACK cycle. A '0' in this bit means that there is no longer a pending VMEbus interrupt from the 'C40.

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3.5 ëC40 Global and VMEbus A32/A24 Slave Memory Map (continued)

3.5.4 Receiver Status Register #1 (continued)

Table 3-10: Model 6509 - Receiver Status Register #1 - R. O. @ Rec_Stat_Reg_1

Bit #	D31	D30	D29	D28	D27	D26	D25	D24
Bit Name	C40_to_VME _Int_Stat	Reserved					Input_B_Clk _LED_Status	Input_A_Clk _LED_Status
Bit Function	1=Int. Pending 0=No Int.	Indeterminate					1 = LED Off 0 = LED On	
Bit #	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
Bit Field	Threshold Detector Status							
I/P Channel	Reserved			Channel B	Reserved			Channel A
Bit Function	Indeterminate			1 = False 0 = True	Indeterminate			1 = False 0 = True
Bit #	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Bit Field	Clock Not Ready Flag Status							
I/P Channel	Reserved			Channel B	Reserved			Channel A
Bit Function	Indeterminate			1 = False 0 = True	Indeterminate			1 = False 0 = True
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Field	FIFO Full Flag Status							
Receiver #	Receiver 8	Receiver 7	Receiver 6	Receiver 5	Receiver 4	Receiver 3	Receiver 2	Receiver 1
Bit Function	1 = FIFO Full Flag False 0 = FIFO Full Flag True							

3.5.4.2 Clock LED Status Bits - D25 and D24

This two-bit field contains one bit associated with each input channel. D25 is associated with Input Channel B and D24 with Channel A. The bit associated with a given channel will read back in the logic '1' state if the Clock LED for that input channel is OFF, i. e., if a clock signal has **not been detected** on that channel. These bits are not latched, and always indicate the current state of the associated LEDs. Under normal operating conditions, one would expect to read a '0' back in a bit associated with a used input channel, and a '1' in a bit associated with an unused input channel.

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3.5 ëC40 Global and VMEbus A32/A24 Slave Memory Map (continued)

3.5.4 Receiver Status Register #1 (continued)

3.5.4.3 Detector Flag Status Bits - D20 and D16

If either of these two bits reads back in the logic '0' state, the data on the associated input channel has exceeded the programmed threshold value at least the programmed number of times. A '1' in either of these bits indicates that the threshold detection conditions have not been met in associated channel. These bits are not latched, and always indicate the current state of the associated channel's threshold detector.

The threshold data value and count for a given input channel are determined by that channel's Threshold Detection Register. See Section 3.5.12 for information about these registers.

NOTE: The data returned in the other six bits in this 8-bit field (D23, D22, D21, D19, D18 & D17) is both indeterminate and meaningless.

3.5.4.4 Clock Not Ready Flag Status Bits - D12 & D8

If either of these 2 bits reads back in the logic '0' state, the input channel associated with that bit has lost its clock signal. Under normal operating conditions, the bits in this field associated with an active channel should read back in the logic '1' state. Those bits associated with an unused channel will read back in the logic '0' state. These bits are not latched, and always indicate the current state of the associated input channel's clock signal.

NOTE: The data returned in the other six bits in this 8-bit field (D15, D14, D13, D11, D10 & D9) is both indeterminate and meaningless.

3.5.4.5 FIFO Full Flag Status Bits - D7 through D0

If any of these 8 bits reads back in the logic '0' state, the data FIFO for the associated receiver has become full, indicating that data may have been lost. A logic '1' in any of these bits indicates that the associated receiver's FIFO is not yet full. These bits are not latched, and always indicate the current state of the associated receiver's FIFO.

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3.5 ëC40 Global and VMEbus A32/A24 Slave Memory Map (continued)

3.5.5 Receiver Status Register #2 - R. O. @ Rec_Stat_Reg_2

This 16-bit, read-only register, which can be accessed by the 'C40 processor and by the VMEbus, contains two 8-bit fields. Each field contains a bit associated with each digital receiver. One field gives the current status of the FIFO Full Flags, and the other gives the FIFO Empty Status. Write operations to this register will have no effect. Table 3-11, below, shows the bit arrangement within Status Register #2. The subsections beginning below the table give detailed descriptions of the register's bit fields.

Table 3-11: Model 6509 - Receiver Status Register #2 - R. O. @ Rec_Stat_Reg_2

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Field	FIFO Half-Full Flag Status							
Receiver #	Receiver 8	Receiver 7	Receiver 6	Receiver 5	Receiver 4	Receiver 3	Receiver 2	Receiver 1
Bit Function	1 = FIFO Half-Full Flag False 0 = FIFO Half-Full Flag True							
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Field	FIFO Empty Flag Status							
Receiver #	Receiver 8	Receiver 7	Receiver 6	Receiver 5	Receiver 4	Receiver 3	Receiver 2	Receiver 1
Bit Function	1 = FIFO Emptyl Flag False 0 = FIFO Empty Flag True							

3.5.5.1 FIFO Half-Full Flag Status Bits - D15 through D8

If any of these 8 bits reads back in the logic '0' state, the data FIFO for the associated receiver has become half-full. A logic '1' in any of these bits indicates that the associated receiver's FIFO is not yet half-full. These bits are not latched, and always indicate the current state of the associated receiver's FIFO. If polling is being used as an alternative to interrupts to determine when to read data from the 6509's FIFO's in a real-time system, these are the flags that we suggest you poll.

3.5.5.2 FIFO Empty Flag Status Bits - D7 through D0

If any of these 8 bits reads back in the logic '0' state, the data FIFO for the associated receiver has become empty. A logic '1' in any of these bits indicates that the associated receiver's FIFO contains data. These bits are not latched, and always indicate the current state of the associated receiver's FIFO.

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3.5 ëC40 Global and VMEbus A32/A24 Slave Memory Map (continued)

3.5.6 FIFO Reset Register - R/W @ F_Rst_Reg

This 16-bit register, which can be accessed by the 'C40 processor and by the VMEbus, contains one bit to reset the data FIFO associated with each of the 6509's digital receivers. A ninth bit is used to initialize the ëC40 Comm Ports after the board is reset. Table 3-12, below, shows which of these bits is associated with which receiver's FIFO.

Table 3-12: Model 6509 - FIFO Reset Register - R/W @ F_Rst_Reg

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Bit Name	Not Used							Comm_Port_Init
Bit Function	Not Applicable							1 = Run 0 = Initialize
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	FIFO_8_Reset	FIFO_7_Reset	FIFO_6_Reset	FIFO_5_Reset	FIFO_4_Reset	FIFO_3_Reset	FIFO_2_Reset	FIFO_1_Reset
Bit Function	1 = Release & Run 0 = Reset FIFO							

NOTE: When reading the contents of the FIFOs via the Comm Port interface, the ports are read in pairs. The FIFO reset bit associated with the odd-numbered receiver in the pair (i. e., the Reset bit for the lower-numbered FIFO) also resets the Comm Port Control circuit. The implication of this fact is that, if one wishes to use the Comm Port interface to read all the data from one FIFO in the pair before reading the other FIFOs data, the lower-numbered FIFO in the pair **MUST** be read first.

3.5.6.1 FIFO Reset Bits - D7 through D0

FIFOs on the Model 6509 will be held in the reset state for as long as the associated Reset bit remains in the logic '0' state. The reset function should therefore be written as a toggle (i. e., clear the bit of interest to the logic '0' state, then set it back to logic '1'). When a FIFO is reset, any data it may contain is erased, the Full and Half-full flags become false, and the Empty flag goes true. Note that these bits also reset the circuitry that controls FIFO write operations, which guarantees that the correct I/Q ordering within the FIFO will be maintained.

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3.5 ëC40 Global and VMEbus A32/A24 Slave Memory Map (continued)

3.5.6 FIFO Reset Register (continued)

3.5.6.2 Comm Port Initialization Bit - D8

This bit is used to reset the ëC40 Comm Ports, which are brought, through buffers, to the Model 6509ís Front Panel. The Comm Ports are held in the reset state for as long as this bit remains in the logic ë0í state. When this bit is set to the logic ë1í state, the ports are released and Comm Ports 2, 3, 4 and 5 are configured as inputs. The function that implements this reset should be written as a toggle (i. e., this bit should be cleared to the logic ë0í state, then set to the logic ë1í state). The firmware for this device toggles this bit as a part of the reset and boot routines. However, this initialization can only be performed once for each ëC40 reset.

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3.5 ëC40 Global and VMEbus A32/A24 Slave Memory Map (continued)

3.5.7 Output Comm Port Control Register - R/W @ Out_Comm_Ctl

Each of the four Output Comm Port connectors on the 6509's Front Panel carries the data from a pair of digital receivers. This 16-bit register, which can be accessed by the 'C40 processor and by the VMEbus, contains four bit fields, each of which is associated with one receiver pair's Output Comm Port. One bit in each field enables the data packing feature (two data samples contained in each 32-bit word). Another selects the order in which the samples are packed. A third selects which receiver's data will be carried by the port (if packed mode is not enabled or if Time ordering is selected), and the last bit enables the pair's Comm Port. Table 3-13, below, shows the bit arrangement within the Output Comm Port Control Register. The subsections beginning at the top of the next page give detailed descriptions of the register's bit fields.

NOTE: The settings of this register affect the presentation of data at the Model 6508's Front Panel Output Comm Ports **ONLY**. Except for the Port Enable bits (which disable direct FIFO readout), they do not affect data read from the FIFOs, by the on-board 'C40 or over the VMEbus, which can **only** be read in Non-Packed Mode.

Table 3-13: Model 6509 - Output Comm Port Control Register - R/W @ Out_Comm_Ctl

Bit #	D15	D14	D13	D12	D11	D10	D9	D8
Port	Comm 7 & 8				Comm 5 & 6			
Bit Name	Pack_ Mode	Data_ Order	Receiver _Select	Port_ Enable	Pack_ Mode	Data_ Order	Receiver _Select	Port_ Enable
Bit Function	1 = Packed 0=NonPacked	1=I/Q(Time) 0 = Receiver	1 = Receiver 7 0 = Receiver 8	1 = Disabled 0 = Enabled	1 = Packed 0=NonPacked	1=I/Q(Time) 0 = Receiver	1 = Receiver 5 0 = Receiver 6	1 = Disabled 0 = Enabled
Bit #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Port	Comm 3 & 4				Comm 2 & 1			
Bit Name	Pack_ Mode	Data_ Order	Receiver _Select	Port_ Enable	Pack_ Mode	Data_ Order	Receiver _Select	Port_ Enable
Bit Function	1 = Packed 0=NonPacked	1=I/Q(Time) 0 = Receiver	1=Receiver 3 0=Receiver 4	1 = Disabled 0 = Enabled	1 = Packed 0=NonPacked	1=I/Q(Time) 0 = Receiver	1=Receiver 1 0=Receiver 2	1 = Disabled 0 = Enabled

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3.5 ëC40 Global and VMEbus A32/A24 Slave Memory Map (continued)

3.5.7 Output Comm Port Control Register (continued)

3.5.7.1 Pack Mode Bits - D15, D11, D7 & D3

In Packed Mode, each 32-bit word delivered by a Comm Port contains two 16-bit samples. In Non-Packed Mode, only one 16-bit sample is contained in each 32-bit Comm Port word, justified in the upper 16 bits. Packed mode is enabled for a given Comm Port pair by setting that pair's Pack_Mode bit to the logic '1' state. Clearing the Pack_Mode bit to the logic '0' state will cause Non-Packed samples to be delivered. When data is Non-Packed, the lower 16 bits of the Comm Port longword will be indeterminate. Table 3-14, on the next page, shows examples of Packed and Non-Packed data formats. **In order to read data from both of the receivers associated with a given Comm Port, Packed Mode MUST be enabled.**

3.5.7.2 Data Ordering Bits - D14, D10, D6 & D2

When Packed Mode is enabled, the data in a given longword may be ordered by Receiver, by I/Q status (for complex data) or by time (for real-only data). When the data is ordered by Receiver, a 16-bit sample from the even (i. e., higher) numbered receiver in the pair will occupy bits D31 - D16 in the longword, and a 16-bit sample from the odd (i. e., lower) numbered receiver in the pair will be placed in bits D15 - D0. Packed data will be ordered by Receiver over a given Comm Port when the Data_Order bit associated with that port is cleared to the logic '0' state. Note that for Option 004 (four receivers), the installed receiver chips are #ís 1, 3, 5 and 7. The impact of this statement is that ordering Packed data by Receiver in these units offers no real advantage.

When the Data_Order bit associated with a given port is set to the logic '1' state, and that portís selected receiver is programmed for complex operation (by clearing the associated Receiver Mode bit in the Mode Select/Channel A Control Register to the logic ë0í state (see Section 3.5.9), and appropriately programming the Graychips (see Appendix B)), I/Q ordering is selected for that port. When I/Q ordering is enabled, only the selected receiver in the pair will send data to the Comm Port (see Receiver Select Bits, below). When data is ordered by I/Q status, the 16-bit In-Phase (I) sample is located in bits D31 - D16 and the 16-bit Quadrature (Q) sample is contained in bits D15 - D0 of the Comm Port's longword.

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3.5 ëC40 Global and VMEbus A32/A24 Slave Memory Map (continued)

3.5.7 Output Comm Port Control Register (continued)

Table 3-14: Model 6509 - Comm Port Data Packing and Ordering Formats (Tagging Disabled)

Sample #	D31		D16	D15		D0
Packed, Receiver Ordered Mode, Complex Data (see NOTE below)						
1	(MSB)	Even Receiver, Q Sample 1	(LSB)	(MSB)	Odd Receiver, Q Sample 1	(LSB)
2	(MSB)	Even Receiver, I Sample 1	(LSB)	(MSB)	Odd Receiver, I Sample 1	(LSB)
3	(MSB)	Even Receiver, Q Sample 2	(LSB)	(MSB)	Odd Receiver, Q Sample 2	(LSB)
4	(MSB)	Even Receiver, I Sample 2	(LSB)	(MSB)	Odd Receiver, I Sample 2	(LSB)
Packed, Receiver Ordered Mode, Real Data Only (see NOTE below)						
1	(MSB)	Even Receiver, Sample 1	(LSB)	(MSB)	Odd Receiver, Sample 1	(LSB)
2	(MSB)	Even Receiver, Sample 2	(LSB)	(MSB)	Odd Receiver, Sample 1	(LSB)
3	(MSB)	Even Receiver, Sample 3	(LSB)	(MSB)	Odd Receiver, Sample 1	(LSB)
4	(MSB)	Even Receiver, Sample 4	(LSB)	(MSB)	Odd Receiver, Sample 1	(LSB)
Non-Packed, Receiver Ordered Mode, Complex Data						
1	(MSB)	Selected Receiver, Q Sample 1	(LSB)	I n d e t e r m i n a t e		
2	(MSB)	Selected Receiver, I Sample 1	(LSB)	I n d e t e r m i n a t e		
3	(MSB)	Selected Receiver, Q Sample 2	(LSB)	I n d e t e r m i n a t e		
4	(MSB)	Selected Receiver, I Sample 2	(LSB)	I n d e t e r m i n a t e		
Non-Packed, Receiver Ordered Mode, Real Data Only						
1	(MSB)	Selected Receiver, Sample 1	(LSB)	I n d e t e r m i n a t e		
2	(MSB)	Selected Receiver, Sample 2	(LSB)	I n d e t e r m i n a t e		
3	(MSB)	Selected Receiver, Sample 3	(LSB)	I n d e t e r m i n a t e		
4	(MSB)	Selected Receiver, Sample 4	(LSB)	I n d e t e r m i n a t e		
Packed, I/Q Ordered Mode, Complex Data						
1	(MSB)	Selected Receiver, I Sample 1	(LSB)	(MSB)	Selected Receiver, Q Sample 1	(LSB)
2	(MSB)	Selected Receiver, I Sample 2	(LSB)	(MSB)	Selected Receiver, Q Sample 2	(LSB)
3	(MSB)	Selected Receiver, I Sample 3	(LSB)	(MSB)	Selected Receiver, Q Sample 3	(LSB)
4	(MSB)	Selected Receiver, I Sample 4	(LSB)	(MSB)	Selected Receiver, Q Sample 4	(LSB)
Packed, Time Ordered Mode, Real Data Only						
1	(MSB)	Selected Receiver, Sample 1	(LSB)	(MSB)	Selected Receiver, Sample 2	(LSB)
2	(MSB)	Selected Receiver, Sample 3	(LSB)	(MSB)	Selected Receiver, Sample 4	(LSB)
3	(MSB)	Selected Receiver, Sample 5	(LSB)	(MSB)	Selected Receiver, Sample 6	(LSB)
4	(MSB)	Selected Receiver, Sample 7	(LSB)	(MSB)	Selected Receiver, Sample 8	(LSB)

NOTE: In Option 004, only the odd numbered receivers are installed. In these units, the Packed, Receiver ordered format offers no advantage.

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3.5 ëC40 Global and VMEbus A32/A24 Slave Memory Map (continued)

3.5.7 Output Comm Port Control Register (continued)

3.5.7.2 Data Ordering Bits (continued)

If a given receiver is programmed for the real-only operating mode (see Section 3.5.9 and Appendix B), and the Data_Order bit associated with that receiverís port is set to the logic ëlí state, Time ordering is selected for that port. Time ordering is used in combination with Packed mode (see Section 3.5.7.1, on page 46), to allow each longword delivered by the Comm Port to carry two real samples from the same receiver (see Receiver Select Bits, below). In Packed, Time Ordered, Real readout mode, the earlier sample will be placed in the upper 16 bits of the Comm Port longword (D31 - D16), and the later sample will be in the lower word (D15 - D0).

Table 3-14, on the previous page, shows examples of Receiver Ordered data in Packed and Non-Packed modes, and of I/Q and Time ordered data in Packed mode.

NOTE: **(1) The only format in which data from both of the receivers in a given pair can be delivered over the Comm Port interface is the Packed, Receiver Ordered format.**

(2) When I/Q or Time Ordering is enabled, Packed Mode MUST also be enabled.

3.5.7.3 Receiver Select Bits - D13, D9, D5 & D1

When the other bits in these bit fields are configured such that the associated Comm Port will deliver data from only one of the receivers in the associated pair (i. e., if the data is either to be Non-Packed or Packed and not Receiver ordered) these bits select which receiver's data will be output. When one of these bits is set to the logic '1' state, the odd (i. e., lower) numbered receiver's data will be delivered to the Comm Port interface. When one of these bits is cleared to the logic '0' state, the even (i. e., higher) numbered receiver's data will be output.

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3.5 ëC40 Global and VMEbus A32/A24 Slave Memory Map (continued)

3.5.7 Output Comm Port Control Register (continued)

3.5.7.4 Comm Port Enable Bits - D12, D8, D4 & D0

These bits are used to enable or disable their associated Comm Port interfaces. When one of these bits is held in the logic '1' state, the Port is disabled. To enable the Comm Port interface for a given receiver pair, clear the associated bit to the logic '0' state.

NOTE: When Comm Port readout of a given receiverís FIFO is enabled, direct readout of that FIFO (by either the ëC40 or VME) is disabled. To enable direct FIFO readout, the Comm Port must be disabled.

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3.5 ëC40 Global and VMEbus A32/A24 Slave Memory Map (continued)

3.5.7 Graychip Control Registers - R/W @ Gray_1_Regs through Gray_8_Regs and W. O. @ Gray_W_All

Each of the Graychip GC1011A receivers on the Model 6509 has 16 internal registers for control and status of these devices. Since there are 8 GC1011As, there are a total of 128 registers. Each register is mapped into a separate VMEbus (or 'C40) address, at longword address intervals (i. e., 4-byte intervals from the VME point of view) from the base address of the Graychip of interest. A ninth 16-longword, write-only region has been set aside to allow a given register (or group of registers) in all eight Graychip receivers to be programmed identically. Table 3-15, below, gives the function, the internal address offset and a mnemonic for each of the Graychip registers. The mnemonics are used in Table 3-16 and Table 3-17, on the next page. Table 3-16 gives the VME addresses of each Graychip register, and Table 3-17 gives the 'C40 addresses. A complete description of each register and its functions is given in Appendix B of this manual, which is a reprint of the GC1011A Manual.

Table 3-15: Model 6509 - GC1011A Internal Memory Map

Register Description	Mnemonic	ëC40 Address Offset (Gray_N_base+)	VME Address Offset (Gray_N_base+)
Frequency Byte 0 (Least Sig. Byte)	FB0	0x00	0x00
Frequency Byte 1	FB1	0x01	0x04
Frequency Byte 2	FB2	0x02	0x08
Frequency Byte 2 (Most Sig. Byte)	FB3	0x03	0x0C
Sync Mode Register	SMR	0x04	0x10
Output Mode Register	OMR	0x05	0x14
Filter Mode Register	FMR	0x06	0x18
Gain Control Register	GCR	0x07	0x1C
Decimation Control 0	DC0	0x08	0x20
Decimation Control 1	DC1	0x09	0x24
Output Status Register	OSR	0x0A	0x28
Checksum Register	CSR	0x0B	0x2C
I-Output Byte 0	IO0	0x0C	0x30
I-Output Byte 1	IO1	0x0D	0x34
Q-Output Byte 0	QO0	0x0E	0x38
Q-Output Byte 1	QO1	0x0F	0x3C

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