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Find the *Pentek 6504* at our website: ***Click HERE***

Model 6504

4-Channel 2-Input Wideband Digital Receiver VME Board



Features

- Sampling rates to 70 MHz
- Two TTL or ECL inputs
- Four 'C40 comm port data outputs
- Tuning control via VMEbus interface or four input 'C40 comm ports
- Dynamic range greater than 70 dB
- 0.26 Hz tuning resolution
- FIFO buffering
- Compatible A/D's available, Series 64xx

Ordering Information

Model	Description
6504	4-Channel 2-Input Digital Receiver VME board

Options:

-012	ECL diff. inputs

General Information

Model 6504 is a wideband digital receiver VME board which accepts digitized data at sampling rates up to 70 MHz. It provides four channels of wideband receivers to perform frequency down conversion, lowpass filtering, and decimation of the sampled output. Parallel digital input data samples from two sources are accepted on a front panel multipin connector.

The receiver output signals are delivered through front panel 'C40 comm ports for implementing DSP functions on Pentek's 'C40 DSP processor boards. Another set of front panel 'C40 comm ports can be used for receiver tuning control from the DSP processor. Receiver tuning, filter and FIFO control is available from the VMEbus.

Operating Principle

These units utilize highly integrated digital receiver chips containing a tunable digital oscillator, a mixer and a tunable low pass output filter. The oscillator frequency and the output filter cutoff frequency in each section are independently programmable over the VMEbus providing extremely flexible and agile operation.

Specifications

Wideband Receivers (4)

Receiver type: Graychip GC1012

Digital input format: 12-bit words, 2's complement; one sample clock line

Input level: TTL single-ended; optionally ECL differential (option -012)

Sampling rate: DC to 70 MHz max

Local oscillator: direct digital synthesizer; frequency = F*$f_s/2^{28}$, where F is a 28-bit binary integer and f_s is input sample rate

Low pass filter: decimating FIR with a decimation range M of 2, 4, 8, 16, 32 or 64; nominal output Nyquist bandwidth $f_N = f_s/M$; output sampling rate is f_s/M for complex outputs and $2f_s/M$ for real outputs

Filter response: in band ripple = ±0.1 dB; -2 dB bandwidth = $0.8f_N$; out of band rejection >75 dB

Real mode: 16-bit real output samples at sampling rate $2f_s/M$

Complex mode: 16-bit I and Q output samples at sampling rate f_s/M per complex pair

Output signal: gain adjustable from 0.0 dB to 90.0 dB with 0.03 dB resolution

FIFO's: 16k x 16 bits; 25 MHz max. input rate; I and Q delivered in parallel to both FIFO's for complex mode; real samples delivered to one FIFO for real mode

Comm port outputs: four total, one per channel; byte serial with four bytes per 32-bit longword described below

Real mode packing: unpacked only (one 16-bit sample in each 32-bit longword)

Complex mode packing: packed (16-bit I sample and 16-bit Q sample packed in 32-bit longword); unpacked (16-bit I sample in 32-bit longword, followed by 16-bit Q sample in 32-bit longword)

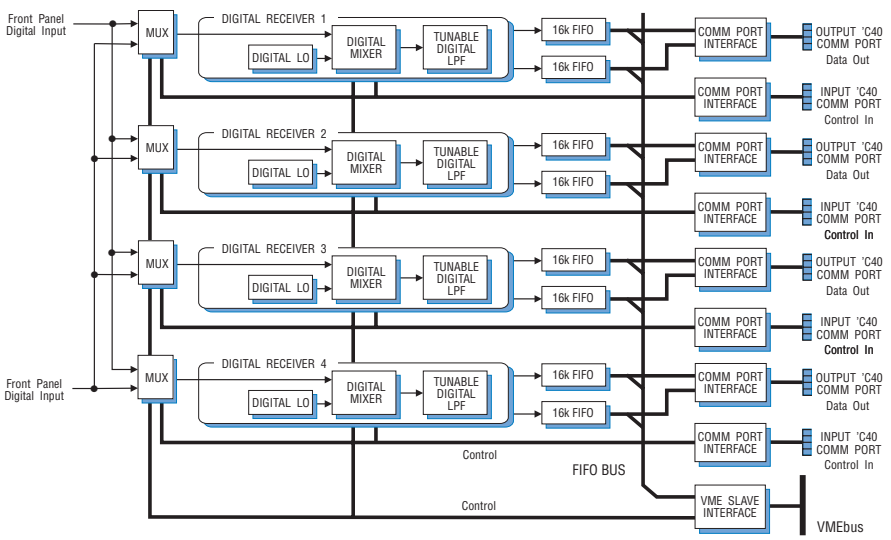
VME interface: slave A32, D32, I(1-7)

VME data outputs: unpacked only (one 16-bit sample in each 32-bit longword)

Power: 4.3 A at +5 V; 0.5 A at –12 V

Size: 6U board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 0.8 in. wide

Block Diagram, Model 6504



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