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PENTLAND SYSTEMS LIMITED

OPERATING MANUAL

MPV901

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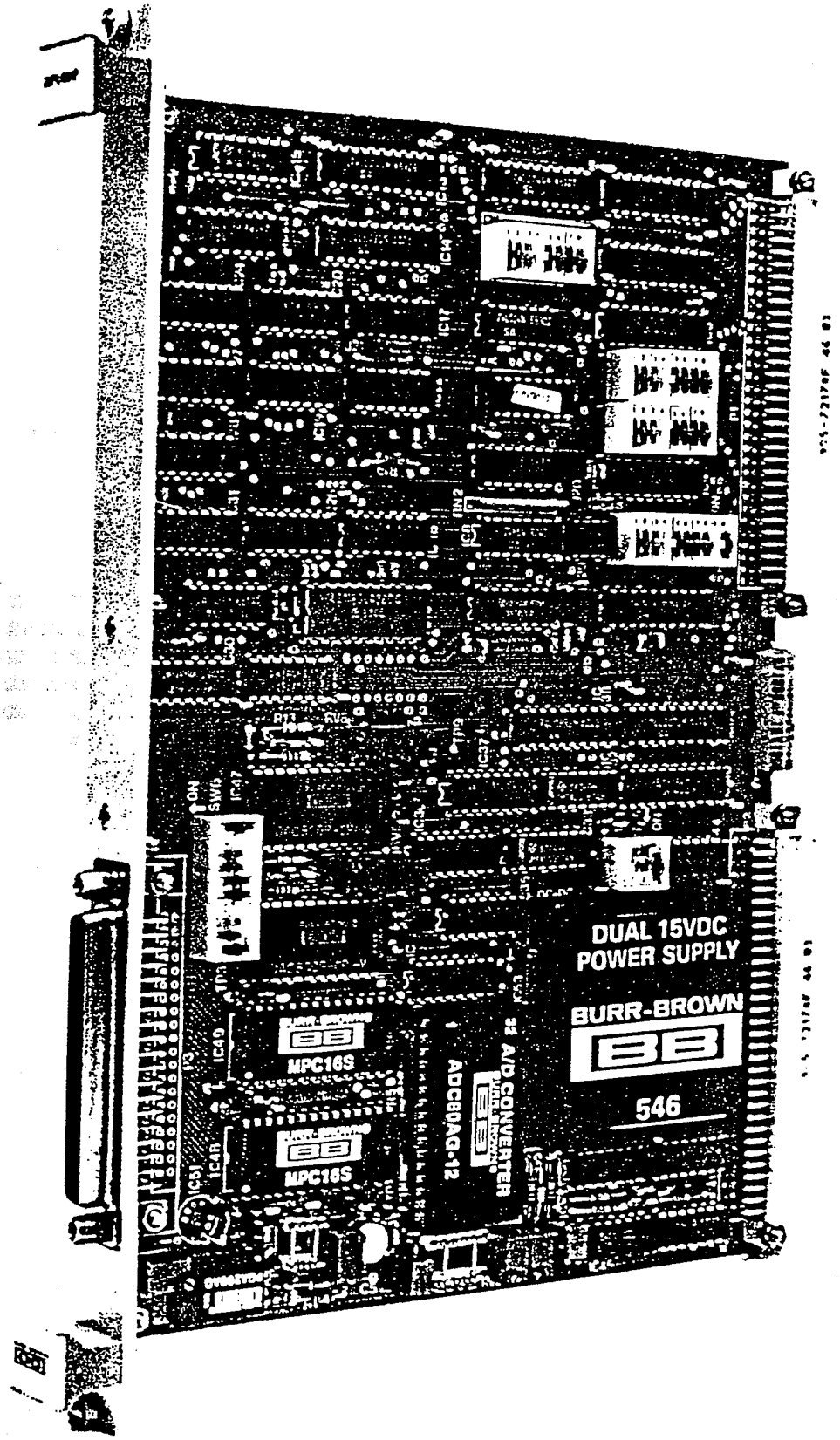
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** THIS MANUAL APPLIES TO THE MPV901 - Rev 9 ONLY **

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Chapter 1 - GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, installation instructions, operating instructions, functional description and applications software examples for the MPV901 series analog input/output data acquisition boards.

1.2 GENERAL DESCRIPTION

The MPV901 series of analog I/O boards are electrically and mechanically compatible with, and interface directly to the VMEbus.

Three versions of the MPV901 series are available:

MPV901 - Analog input only
MPV901A - Analog input and output
MPV901P - Analog input and output with software Programmable Gain Amplifier (P.G.A.)

The analog input section of the MPV901 includes:

- analog multiplexer suitable for 32 single-ended or 16 differential channels.
- resistor programmed instrumentation amplifier (MPV901, MPV901A) or a software programmable amplifier (MPV901P).
- sample/hold amplifier.
- 12 bit A/D converter.

An optional analog output system is included on the MPV901A and MPV901P, consisting of two 12 bit D/A converters and associated control logic.

MPV901P gain setting and channel selection are dynamically monitored and the settling time of the PGA calculated to allow maximum data throughput rates.

Gains of 1 to 1000 are software selectable for the PGA and the gain for each channel may be stored in an on-board RAM if desired. The proper gain for each channel is then selected automatically by the MPV901.

MPV901 series VMEbus interface capability includes standard or short addressing modes with or without address modifier codes. Address modifier response is user selectable by appropriate programming of the on board PROM.

Any one of the seven levels of interrupt available on the VMEbus can be user selected and generated by the MPV901. During the interrupt mode of operation the MPV901 supplies the user defined interrupt vector to the CPU when requested.

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1.3 SPECIFICATION

ELECTRICAL
Typical at +25°C and rated power supplies unless otherwise stated.

ANALOG INPUT SECTION

INPUT CHARACTERISTICS	
Number of Channels	32 single-ended/16 differential
ADC Gain Ranges (Jumper Selectable)[1]	0 to +5V,0 to +10V,±2.5V,±5V,±10V
Amplifier Gain Ranges	
Resistor-Programmable[2](MPV901, MPV901A)	1 to 1000
Software Programmable (MPV901P)	1 to 1000 (values of 1,10,100,1000)
Maximum Input Voltage Without Damage	±25V (Power Off)
	±35V (Power On)
Input Impedance	>100 MOhm, 5pF OFF Channel
	>100 MOhm, 50pF ON Channel
Bias Current (+25°C)max	±35nA
(0°C to + 70°C) max	±60nA
Differential Bias Current	±35nA
Amplifier Input Offset Voltage[3]MPV901P	±320µV
MPV901, MPV901A	±160µV
Amplifier Input Offset Voltage Drift	±10µV/°C
TRANSFER CHARACTERISTICS	
Resolution	12 bits
Throughput Time G = 1	70µs, (100µs, max)
Throughput Time G = 1000	720µs, max
ACCURACY	
System Errors at +25°C, max[4]	
MPV901P G = 1, G = 1000	±0.05%, ±0.075% FSR[5]
MPV901, MPV901A G = 1, G = 1000	±0.05%, ±0.08% FSR
System Linearity	±0.025% FSR
A/D Converter:	
Linearity	+1/2LSB
Differential Linearity	±1/2LSB
Quantizing Error	±1/2LSB
Gain Error	Adjustable to Zero
Offset Error	Adjustable to Zero
Monotonicity[6]	Guaranteed 0°C to + 70°C
ACCURACY OVER TEMPERATURE	
System Accuracy Drift	
MPV901P G = 1, G = 1000	50ppm, 50ppm of FSR/°C
MPV901, MPV901A G = 1, G = 1000	40ppm, 100ppm of FSR/°C
DYNAMIC ACCURACY	
Sample/Hold Aperture Time	125ns
Aperture Time Uncertainty	±5ns
Differential Amplifier CMRR, G = 1	
MPV901P	90dB (DC to 60Hz)
MPV901, MPV901A	80dB (DC to 60Hz)
Channel Crosstalk	75dB down at 1kHz for OFF Channel to ON Channel

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ANALOG OUTPUT SECTION (MPV901A, MPV901P)

OUTPUT CHARACTERISTICS	
Number of Channels	2
Output Voltage Ranges (Switch Selectable)	0 to +5V, 0 to +10V ±2.5V, ±5V, ±10V, at 5mA
Output Impedance (at DC)	0.05 Ohm
Short Circuit Protection, Duration	Indefinite to Common
TRANSFER CHARACTERISTICS	
Resolution	12 bits
Output Settling Time, max	5µs
ACCURACY	
Output Error, typical	±0.025% FSR
max [7]	±0.05%FSR
Temperature Coefficient of Accuracy	±25 ppm of FSR/°C
POWER REQUIREMENTS	
MPV901	+5V ±5% at 1.5A max
MPV901A	+5V ±5% at 2.0A max
MPV901P	+5V ±5% at 2.0A max
ENVIRONMENTAL	
Operating Temperature	0°C to + 70°C
Storage Temperature	-25°C to +85°C
Relative Humidity	90% noncondensing

NOTES:
[1] Factory set for ±10V operation.
[2] Factory set for Gain = 1.
[3] Adjustable to zero.
[4] Includes linearity errors with gain and offset errors adjustable to zero.
[5] FSR mean Full Scale Range.
[6] No missing codes guaranteed.
[7] Maximum error with gain and offset errors adjusted to zero.

MECHANICAL

Compatible with double-height VMEbus card-racking systems.

Minimum card spacing 20.34mm (0.8") (VMEbus specification compatible).

One 37-pin 'D' type connector on board for analog inputs/outputs.

Use Cannon 'D' type connector part number DC37P/1A1N or equivalent.

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Chapter 2 - INSTALLATION INSTRUCTIONS

2.1 INTRODUCTION

This chapter provides installation instructions and an overview of the user selectable options on the MPV901 series.

2.2 PREPARING THE BOARD

This section describes the hardware preparation of the MPV901 series prior to installation in a VMEbus system. Following the instructions described in this section will ensure that the board is configured as desired and will function as expected when installed.

MPV901 series boards are factory calibrated and tested prior to shipment with jumpers and switches in pre-determined positions.

Figure 2.1 indicates the physical position of the jumpers and switches.

NOTE: jumper and switch positions are identical on all versions of the board.

Table 2.1 lists each jumper/switch, its function and the factory set position.

A detailed description of each jumper/switch is given in sections 2.2.1 through 2.2.9.

To alter the address modifier code response from the factory set values, the user must program the decoding PROM as described in section 2.2.10.

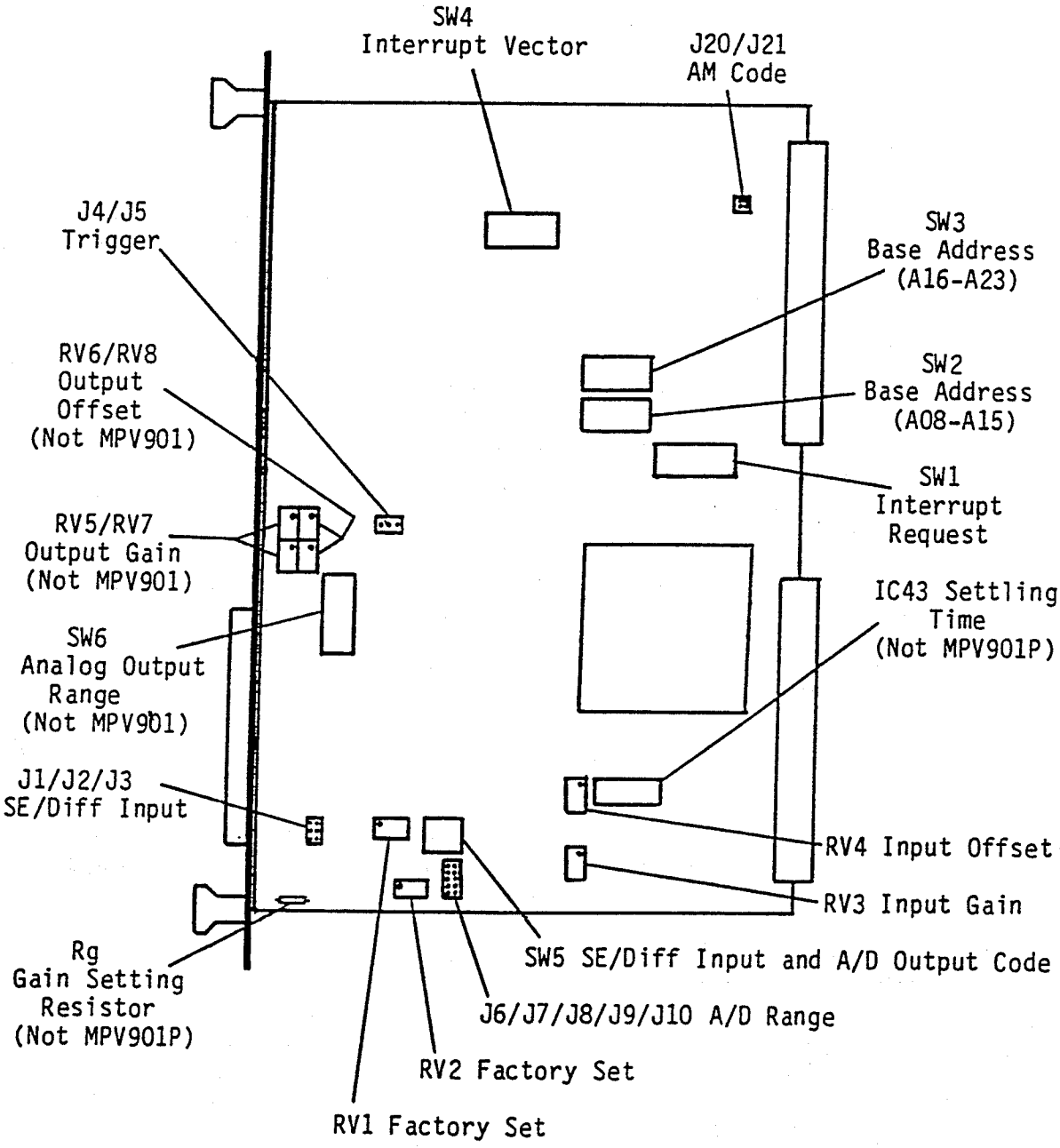
Before installation, the user should verify the configuration of the jumpers/switches and, if necessary, alter the configuration to suit particular system requirements.

The board should not be installed or removed while power is applied to the VMEbus system.

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Figure 2.1

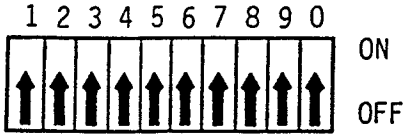
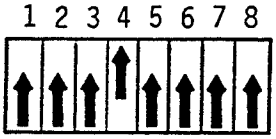
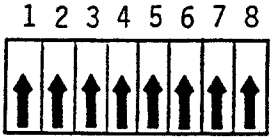
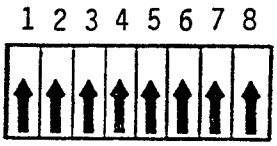
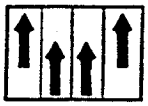
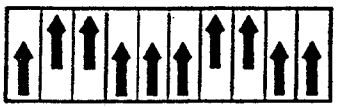
Position of Jumpers/Switches/Pots



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TABLE 2.1

JUMPER/SWITCH FUNCTIONS & FACTORY SETTINGS

SWITCH/JUMPER DESIGNATION	FUNCTION	FACTORY SET CONDITION
SW1	Interrupt Request Line Selection	
SW2	Base Address Selection (A08-A15)	
SW3	Base Address Selection (A16-A23)	
SW4	Interrupt Vector Selection	
SW5 position 1) 2) 3) 4)	Single-Ended/Differential Mode Selection. A/D Output Code Selection	
SW6#	Analog Output Range Selection	
J1, J2, J3	Single Ended/Differential	J1, J3 INSERTED
J4, J5	Internal/External Trigger	J5 INSERTED
J6, J7, J8, J9, J10	A/D Converter Range Selection	J7, J9 INSERTED
J20, J21	AM Code Response	J20, J21 INSERTED
IC43*: 2-3 , 6-7 10-11,14-15	Mux, Amp, S/H Settling Time Selection	2-3 , 6-7 ALL 10-11,14-15 INSERTED

Not used on MPV901
* Not used on MPV901P

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2.2.1 Base Address Selection

The base address of the MPV901 can be set to any value by selecting the appropriate combination of positions on switches SW2 and SW3. The factory set configuration is FFF780H. To change the sense of a bit simply change the switch setting for that bit.

The MPV901 occupies 64 successive memory locations (word locations) within the system memory map.

Table 2.2 lists the switch positions that determine which base address is selected.

Figure 2.2
Base Address Selection Switches

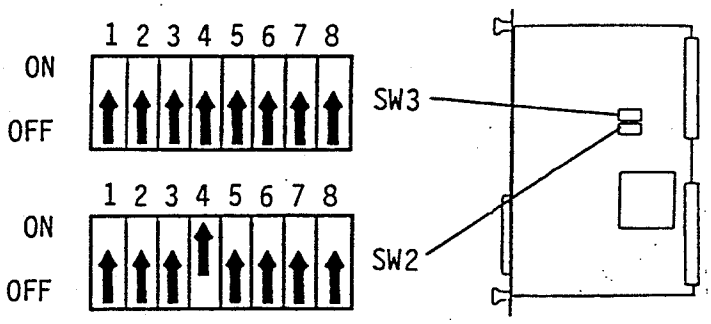


Table 2.2
Base Address Switch Selection

ADDRESS LINE	FACTORY SET	SWTICH POSITION FOR "0"	SWTICH POSITION FOR "1"
A07	1	-	-
A08	1	SW2 psn 1 ON	SW2 psn 1 OFF
A09	1	2 ON	2 OFF
A10	1	3 ON	3 OFF
A11	0	4 ON	4 OFF
A12	1	5 ON	5 OFF
A13	1	6 ON	6 OFF
A14	1	7 ON	7 OFF
A15	1	8 ON	8 OFF
A16	1	SW3 psn 8 ON	SW3 psn 8 OFF
A17	1	7 ON	7 OFF
A18	1	6 ON	6 OFF
A19	1	5 ON	5 OFF
A20	1	4 ON	4 OFF
A21	1	3 ON	3 OFF
A22	1	2 ON	2 OFF
A23	1	1 ON	1 OFF

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Figure 2.4
Interrupt Vector Selection Switch

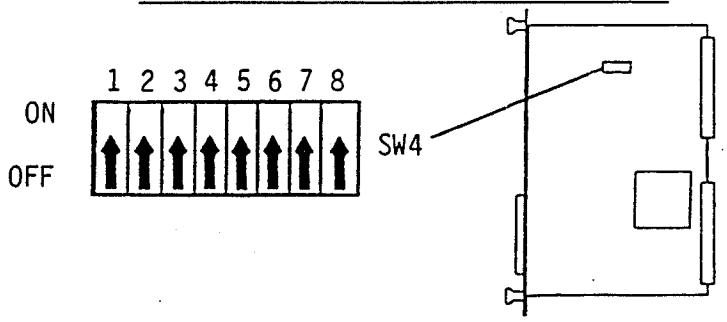


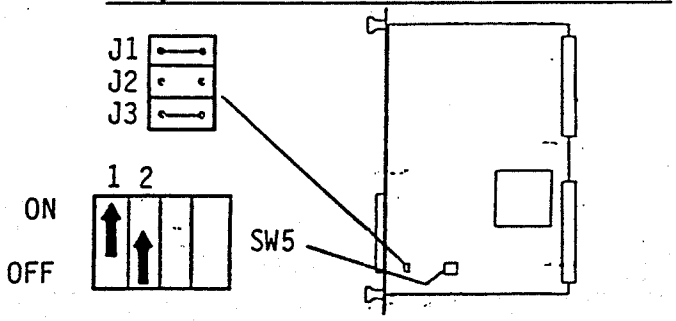
Table 2.4
Interrupt Vector Selection

DATA LINE	SWITCH POSITION FOR "0"	SWITCH POSITION FOR "1"	FACTORY SET
D00	SW4 psn 1 ON	SW4 psn 1 OFF	1
D01	2 ON	2 OFF	1
D02	3 ON	3 OFF	1
D03	4 ON	4 OFF	1
D04	5 ON	5 OFF	1
D05	6 ON	6 OFF	1
D06	7 ON	7 OFF	1
D07	8 ON	8 OFF	1

2.2.4 Analog Input Single Ended/Differential Operation

Jumpers J1, J2, J3 and switch SW5 are used to select between 32 single ended channels or 16 differential channels of operation. Figure 2.5 illustrates the factory set configuration of the jumpers and switch. The factory set condition is 32 channels single-ended mode. Table 2.5 lists the two allowable configurations of the jumpers and switch positions.

Figure 2.5
Single-Ended/Differential Operation



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2.2.2 Interrupt Request Line Selection

Figure 2.3 illustrates the location and configuration of switch SW1. The MPV901 series can be selected to interrupt on any one of seven interrupt request lines as shown in Table 2.3.

Figure 2.3
Interrupt Request Line Selection

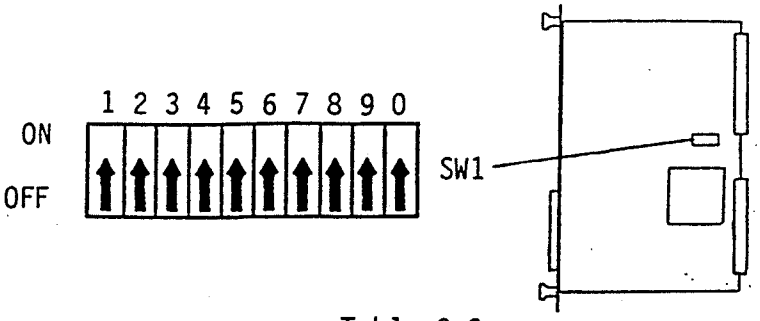


Table 2.3
Interrupt Switch Configurations

REQUEST INTERRUPT ON LINE	SW1 SWITCH POSITION(S) SELECTED
$\overline{IRQ1}$	10,3,2 ON
$\overline{IRQ2}$	9,3,1 ON
$\overline{IRQ3}$	8,3 ON
$\overline{IRQ4}$	7,2,1 ON
$\overline{IRQ5}$	6,2 ON
$\overline{IRQ6}$	5,1 ON
$\overline{IRQ7}$	4 ON

NOTES: 1. Factory set with all positions OFF on SW1.
2. An interrupt should be requested on ONE line only

2.2.3 Interrupt Vector Selection

During the interrupt mode of operation, the MPV901 supplies the interrupt vector on data lines D00 - D07 when requested by the CPU. The factory set configuration for the interrupt vector is shown in Figure 2.4 The interrupt vector is factory set to FFH and is user definable by switch SW4 as shown in Table 2.4

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Table 2.5
Single-Ended/Differential
Allowable Configurations

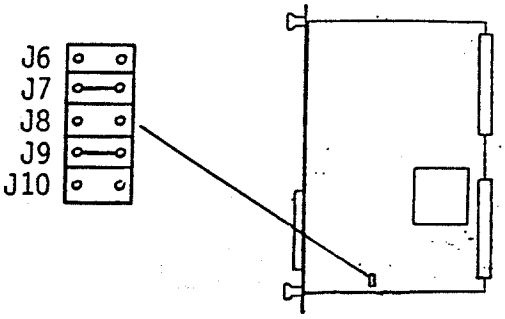
JUMPER/SWITCH POSITION	MODE OF OPERATION
J1,J3 IN and J2 OUT SW5 psn 1 ON and psn 2 OFF	Single-Ended (FACTORY SET)
J2 IN and J1, J3 OUT SW5 psn 2 ON and psn 1 OFF	Differential

NOTE: Positions 3 and 4 on SW5 select A/D converter output code. (Section 2.2.6)

2.2.5 Analog to Digital Converter (A/D) Range Selection

There are two gain determining elements within the MPV901 - the A/D converter and the instrumentation amplifier. For lowest system noise, the A/D range should be set at +10V or 0 to +10V with the amplifier providing all the system gain. The A/D range is factory set for ±10V. The A/D range can be set to various values, these being shown in Table 2.8 with their corresponding jumper configurations. Before adding new jumpers to change range, remove those inserted for the present range.

Figure 2.6
A/D Range Selection



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Table 2.6
A/D Converter Range Setting Jumpers

RANGE	INSERT JUMPER
±10V	J7, J9
±5V	J6, J9
±2.5V	J6, J8, J9
0 to +5V	J6, J8, J10
0 to +10V	J6, J10

2.2.6 Analog to Digital Converter Code Selection

SW5 positions 3 and 4 determine the coding arrangement of the output data from the A/D converter. Three coding schemes are possible - complementary straight binary for unipolar ranges and either complementary offset binary or complementary two's complement for bipolar ranges.

Figure 2.7 shows the factory set configuration which is complementary offset binary coding while Table 2.7 indicates the two allowable configurations for SW5.

Figure 2.7

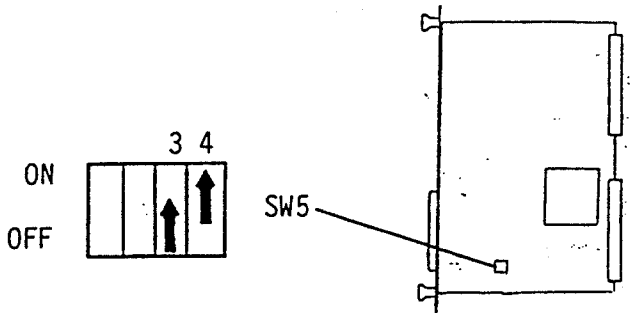


Table 2.7
Code Configuration

SWITCH POSITION SW5	OUTPUT CODING
3 ON 4 OFF	Complementary Two's Complement
3 OFF 4 ON	Complementary Straight Binary (Unipolar ranges only) (FACTORY SET)

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2.2.7 Multiplexer, Amplifier and Sample/Hold Settling Time (MPV901, MPV901A)

On MPV901 and MPV901A versions (which have the resistor programmable amplifier option) position IC43 contains four jumper headers. When a new channel is selected and a conversion initiated, the system (multiplexer, amplifier and sample/hold) requires time to settle before the A/D can begin to convert. The settling time depends upon the gain of the amplifer and is smallest for lowest gain values. The four jumpers allow the optimum settling time to be set for three different gain ranges thus enabling maximum system throughput for a given gain setting.

Table 2.8 shows the factory set position of the jumpers at location IC43. This configuration allows a settling time of 650µs and is suitable for amplifer gains up to 1000. The appropriate delay for values of gain can be set by inserting the jumper links at position IC43 as shown in Table 2.8.

Figure 2.8
IC43 Jumpers

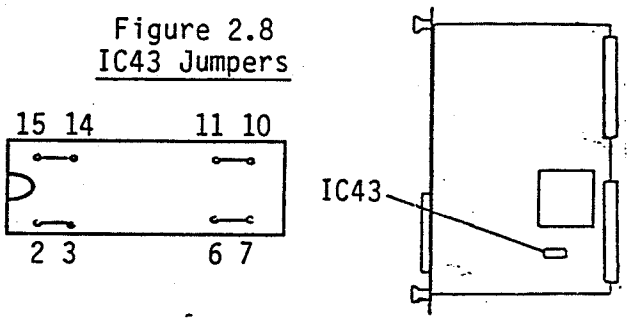


Table 2.8
Settling Time Selection

GAIN RANGE	SETTLING TIME REQUIRED	PINS CONNECTED AT POSITION IC43
1-10	45 µs max	6-7,
11-100	70 µs max	2-3,6-7,14-15
* 100-1000	650 µs max	2-3,6-7,10-11,14-15

* NOTE:- Factory set condition

2.2.8 Analog Output Range Selection (MPV901A,MPV901P)

Switch SW6 is used to set the output voltage range of the analog outputs (each output range being individually selectable).

Each output is set at the factory for ±10V operation (complementary offset binary coding).

When making a change, first set all switch positions on SW6 to the OFF position and then set to the ON position those switches required for the desired range. Table 2.9 lists the available analog output ranges and the switch settings that determine which range is selected.

NOTE:- The analog outputs default on power up to the most positive value in the selected range.

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Figure 2.9
Analog Output Range Selection Switch

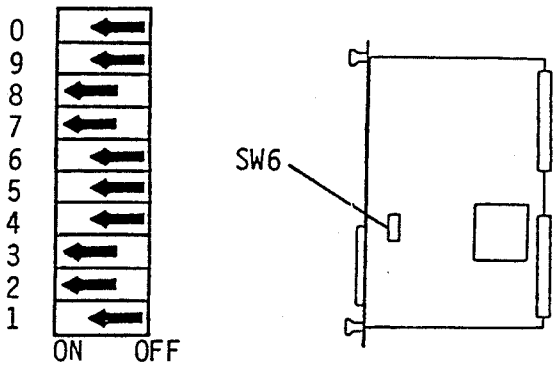


Table 2.9
Analog Output Range Selection

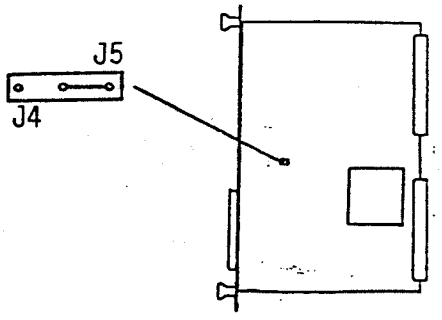
RANGE	OUTØ	OUT1
* ±10V	SW6 psn 2,3 ON	SW6 psn 7,8 ON
±5V	1,3 ON	6,8 ON
±2.5V	1,3,5 ON	6,8,10 ON
0 to +5V	1,4,5 ON	6,9,10 ON
0 to +10V	1,4 ON	6,9 ON

* NOTE:- Factory Set Condition

2.2.9 Internal/External Trigger Selection

Jumpers J4 and J5 are used to select between internal and external triggering. Before external triggering can be used, bit D0 of the control register has to be set to a '1'. Table 2.10 shows the two configurations available.

Figure 2.10
Internal/External Trigger Selection



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Table 2.10
J4, J5 Configurations

JUMPER INSERTED	OPTION SELECTED
#J4	External Trigger
*J5	Internal trigger

* Factory set condition
\# Bit D10 of the control register has also to be set to a '1' before External triggering can be used.

2.2.10 Address Modifier Code Response

IC11 is a PROM, which in conjunction with jumpers J20 and J21, allows the response to address modifier codes to be varied to suit user requirements. The PROM/jumper combination offers the options illustrated in Table 2.11. The PROM program which enables this response is shown in the programming chart of Figure 2.12, at the end of this chapter.

Figure 2.11

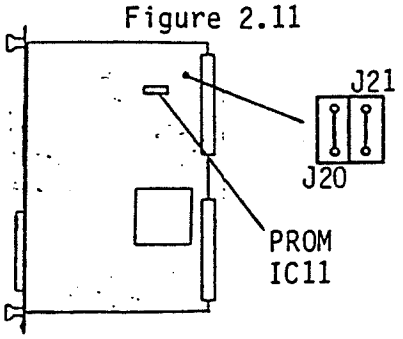


Table 2.11
Address/Address Modifier (AM) Response

	J20	J21	AM CODES	ADDRESS DECODING
* 1	Insert	Insert	N/A	A01-A15
2	Insert	Remove	N/A	A01-A23
3	Remove	Remove	3D, 39	A01-A23

* Factory set condition

A new PROM can be programmed to provide an alternative AM code response. The PROM is a 256 x 4 bit open-collector 82S126 type. The following section explains the interaction between J20, J21 and the codes stored in the PROM. An understanding of this section should allow the user to select the correct jumper/PROM code combination for a given response.

A list of VMEbus address modifier codes is given in section 6.2.

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2.2.10.1 Programming the PROM

There are three allowable combinations of jumper links J20 and J21. These combinations are given in Table 2.11 and are referred to as (1), (2), (3). It is intended that combinations (1) and (2) be reserved for the responses detailed in Table 2.11, ie, short addressing with no AM codes and standard addressing with no AM codes respectively.

Combination (3) however, (Jumper J20 and J21 removed), in conjunction with the information stored in the PROM, is designed to allow the response to address/AM codes to be modified, to suit system requirements, as shown in Table 2.12. Setting the two most significant data bits (D3 and D2) to a low level allows responses (1) and (2) as shown in Table 2.11. With both J20 and J21 removed it is the setting of data bits D0 and D1 which determines the response.

The following section (2.2.10.2) illustrates the method to be used when programming the PROM to produce a given response.

Table 2.12
Address/AM Response Options with J20 & J21 Removed

AM CODE NOTE (1)	DATA BIT D3 D2 D1 D0	RESPONSE
XY	0 0 0 0	Short addressing with AM
XY	0 0 0 1	Short addressing with AM
XY	0 0 1 0	Standard addressing with AM
XY	0 0 1 1	No response to address/AM

NOTE :- The AM code indicated as XY in Table 2.12 can take any of the possible values defined in the VMEbus specification Rev B. (See Section C).

2.2.10.2 Programming Examples

The Factory Response

Referring to Table 2.12 the programming of the PROM to give the factory set response is as follows.

1. Decide upon STANDARD or SHORT addressing - STANDARD (ie, A01-A23 decoded)

2. Decide upon AM codes to which the board will respond - 3D, 39.

3. Refer to Table 2.12 and under "response" heading look for "Standard addressing with AM". The data to be stored at the relevant memory addresses can then be read from the table (in this case 0010 (02H)).

4. Place the code obtained in (3), (ie 02H), at memory locations 3D and 39.

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5. Refer to Table 2.12 and under "response" heading look for "No response to address/AM". The data to be stored at the relevant memory addresses, (in this case all locations other than 3D and 39), can then be read from the table, (in this case 0011 (03H)).

6. Place the code obtained in (5), (ie 03H), at all memory locations other than 3D and 39.

Short Addressing With AM

Assume that the following response is desired - Short Address decoding, (ie, A01 -A15 decoded) and AM codes 2D and 29* to be responded to. The following steps would yield the data to be placed in the PROM.

1. Addressing mode - SHORT.

2. Code response - 2D and 29.

3. Refer to Table 2.12 and under "response" heading look for "Short addressing with AM" (Note - there are two entries under this heading). The data to be stored at the relevant memory address can then be read from the table, (in this there is a choice of two codes - 0000 (00H) or 0001 (01H)).

4. Place either of the codes obtained in (3), (ie, 00H or 01H), at memory locations 2D and 29.

5. Refer to table 2.12 and under "response" heading look for "No response to address/AM". The data to be stored at the relevant memory addresses (in this case all locations other than 2D and 29), can then be read from the table, (in this case 03H).

6. Place the code obtained in (5), (ie, 03H) at all memory locations other than 2D and 29.

Similar reasoning applies to any other combination of address/AM response.

*Any number and combination of AM codes may be catered for.

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Chapter 3 - OPERATING INSTRUCTIONS

3.1 INTRODUCTION

This chapter provides the necessary information to allow the use of the MPV901 series in a VMEbus system.

3.1.1 Switch/Jumper Setting Checklist

Before plugging the board into a VMEsystem and applying power, check, to ensure proper system operation, that the following options have been correctly set.

1. Base Address.
   Has the Base Address of the board been set to suit system requirements? (Section 2.2.1.)

2. Address Modifier Response.
   Has Address Modifier Response been correctly set? (Section 2.2.10)

3. Interrupt Request and Vector.
   Have the Interrupt Request Line and Interrupt Vector been set to the appropriate value? (Section 2.2.2., 2.2.3)

4. Single-Ended/Differential Operation.
   Has correct input mode been selected (ie, 32 single-ended or 16 differential channels)? (Section 2.2.4)

5. A/D Range and Code.
   Has correct A/D input range been selected? (Section 2.2.5)
   Has appropriate output coding been selected? (Section 2.2.6)

6. Settling Time (MPV901, MPV901A).
   Has correct settling time been selected to suit the gain of the amplifier? (Section 2.2.7)

   NOTE:- Factory condition is all jumpers inserted ie. maximum delay. Remove appropriate jumpers for use with gain of 1.

7. Output Range (MPV901A, MPV901P).
   Has the correct output range been selected for each analog output? (Section 2.2.8.)

3.2 OPERATING PROCEDURE

The board is shipped from the factory in a calibrated condition and ready for use. Installation only requires plugging the card into an empty slot in the VMEbus card cage and wiring the analog connector. However, the board can be adapted to suit user requirements therefore, some features of the board are switch or jumper selectable. These features are covered in chapter 2 which should be referred to before using the board or if a configuration other than the factory set condition is desired.

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3.2.1 Programming

The board is programmed as 64 successive memory locations (word locations), switch selectable within the 16 Mbyte address range, in 64 word blocks, commencing at address 000080H. The analog to digital converter output has a resolution of 12-bits and therefore word accesses are required for each channel. The digital to analog converter inputs are 12 bits and therefore also require data word accesses.

The board can be programmed to operate in either the polling or interrupt mode.

For MPV901P, the gain is software programmable and may be stored in the on-board RAM if desired.

3.2.1.1 Address Map (Memory Map)

The address map (memory map) for the MPV901 series boards is shown in Figure 3.1. The base address is switch selectable. (Section 2.2.1)

Measurement data (converted data) and status information is transferred to and from the board and CPU with MOVE instructions, with the appropriate addresses. Gain selection data, control and analog output data are sent to the board by the CPU also using MOVE instructions.

For single-ended operation, 32 consecutive addresses are used, starting from the base address XXXX80, (the X-states are selected as previously described). As each operation is a word access, word addressing must be used (even addresses only).

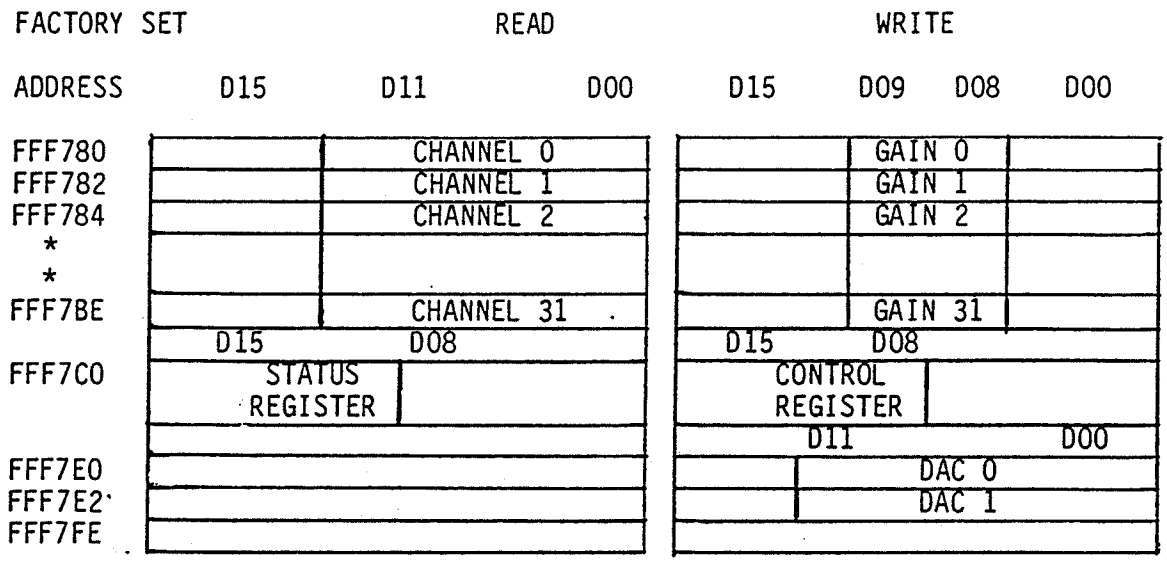
For differential operation, 16 consecutive addresses are used, starting from address XXXXA0.

The control and status registers are selected with address XXXXC0 while the two analog output channels occupy addresses XXXXE0 (OUTØ) and XXXXE2 (OUT1).

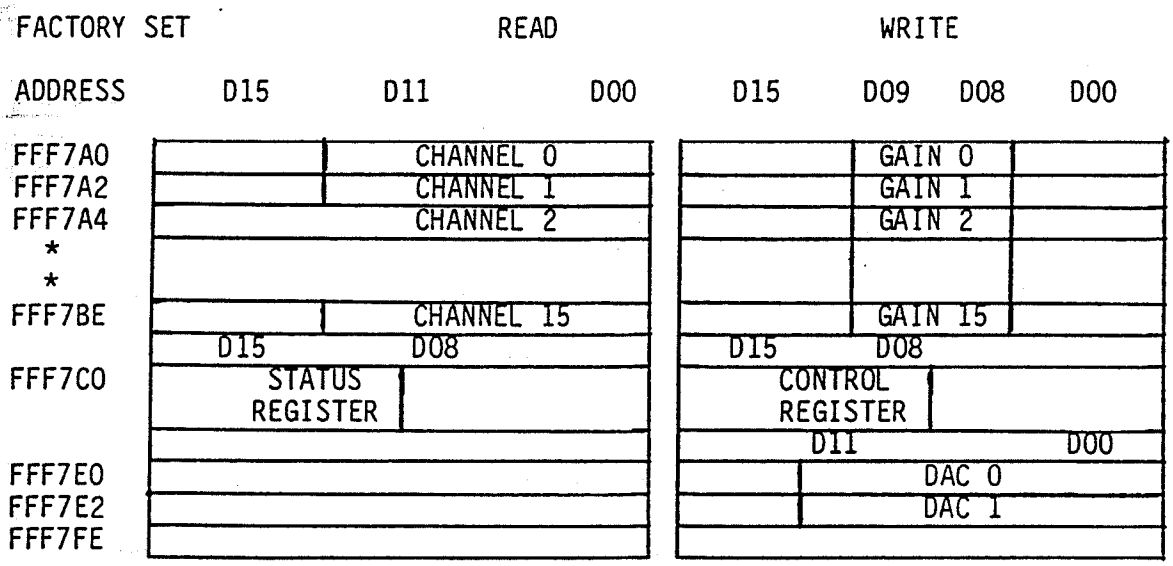
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Figure 3.1
MPV901 Address (Memory Map)

SINGLE ENDED OPERATION



DIFFERENTIAL OPERATION



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3.2.1.2 Control Register

Certain board functions can be selected, under software control, by setting or resetting the data bits in a control register. The function of each bit in this register is as shown in Figure 3.2 and is defined below.

Data is written into the control register via data lines D08 - D15 at address XXXXC0.

Figure 3.2
Control Register

D15	D14	D13	D12	D11	D10	D09	D08
NOT USED	INT EN	R/W EN	RAM EN	SHORT CYCLE	EXT TRIG	G1*	G0*

* Used only on MPV901P

D08/D09 - The amplifier gain must be written to these two bits when the RAM on the MPV901P is not used to store this information. The gain value remains as written until a new value overwrites the old value. The selection codes are shown in Table 3.4. (Section 3.2.4.3)

D10 - A '0' plus J5 inserted and J4 removed disables the external a triggering, a '1' plus J4 inserted and J5 removed enables external triggering.

D11 - A 'Ø' enables 10-bit conversion to take place (for increased speed but reduced accuracy operation). A '1' disables short-cycle to allow full 12-bit conversion.

D12 - A 'Ø' disables the RAM on the MPV901P and the CPU must write the gain into the control register. A '1' enables the RAM to supply the gains as stored for each channel.

D13 - A 'Ø' enables the CPU to write the gain for each channel to the RAM on-board the MPV901P. A '1' prevents the CPU from writing the gain to the RAM. In the latter case the gain must be written to data bits D08/D09 of the control register.

NOTE: When no more gain information is to be written into the RAM, bit D13 of the control register should be set to a high level. Failure to do this may result in spurious write signals to the RAM followed by loss of data.

D14 - A '1' enables interrupts, a 'Ø' disables interrupts.

D15 - Not used.

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3.2.1.3 Status Register

The status of the condition bits in the control register can be monitored by reading the contents of the status register. The status register is read via data lines D08 - D15 and is located at address XXXXC0. The function of each bit within this register is as shown in Figure 3.3 and is defined below.

Figure 3.3
Status Register

D15	D14	D13	D12	D11	D10	D09	D08
CONV COMP	INT EN	R/W EN	RAM EN	SHORT CYCLE	EXT TRIG	G1*	G0*

* Used only on MPV901P

D08/D09 - This bits show the current value of the gain stored in the control register. The selection codes are shown in Table 3.4. (Section 3.2.4.3)

D10 - External trigger enable/disable. This bit is high when external triggering is enabled and is low when internal triggering is enabled.

NOTE: For external triggering J4 should be inserted and J 5 removed. For internal triggering J5 should be inserted and J4 removed.

D11 - This bit is high for full 12-bit operation and is low when the analog input data is converted into a 10-bit value. (ie, short cycle).

D12 - This bit is high when the RAM on the MPV901P is enabled to be used as the gain control for the amplifier and is low when the RAM output is disabled and gain must be supplied via the control register.

D13 - This bit is low when the RAM has been enabled to allow the gain values to be written into it (MPV901P only). It is high when writing to the RAM is disabled (ie, the RAM is write protected).

D14 - This bit is high when interrupts are enabled and low when interrupts are disabled.

D15 - This bit is low during conversion. It goes high upon completion of conversion.

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The power-up condition of the control/status register is shown in Figure 3.4:-

Figure 3.4
Control/Status Register Power-on Condition

D15	D14	D13	D12	D11	D10	D09	D08
X	0	0	0	0	0	0	0

Gain (MPV901P only)	-	1
Short cycle	-	Yes (10 bit conversion enabled)
Ram Enable (MPV901P only)	-	Disabled
R/W Enable (MPV901P only)	-	Write Enabled
Interrupt Enable	-	Interrupts Disabled
Conversion Complete	-	Indeterminate

NOTE: 1: Input signal power-up setting is Channel 0 selected.
2: To set the conversion complete bit (D15) to a known condition at power-up, a read operation should be performed on the board.

3.2.2 Operating Modes

MPV901 series operates in one of two modes, either polling or interrupt mode. Both modes of operation are discussed in the sections, 3.2.2.1 and 3.2.2.2.

3.2.2.1 Polling Mode

To allow this mode of operation, the interrupts must first be disabled by setting data bit D14 low.

A MOVE instruction to the board reads the converted data from the previously addressed channel and starts the conversion process for the next channel at the address just placed on the bus. The CPU determines the end of conversion by monitoring data bit D15 of the status register. When conversion is complete, the CPU reads the data using a MOVE instruction addressed to the next channel to be converted. The data of the last channel is thus transferred to the CPU and conversion is started for the next channel (at the address just placed on the bus).

The status register is read using a MOVE instruction at address XXXXC0. Data bit D15 is low during conversion and goes high upon completion of conversion.

NOTE: The first read to the board, after power-up is a dummy read (ie, the data should be discarded). This read instruction should be addressed to the first channel to be converted.

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3.2.4 Analog Input Section

3.2.4.1 Analog Input and Converter Output Codes

The analog input value of a selected channel is amplified and then converted to a hexadecimal value. The analog to digital converter offers three output coding schemes - complementary straight binary (for unipolar ranges) and complementary offset binary or complementary two's complement (for bipolar ranges).

Tables 3.1, 3.2 and 3.3 illustrate the full scale negative, midscale and full scale positive codes for the five input ranges with the corresponding input voltage of the analog to digital converter and the value of the least significant bit (LSB).

Figures 3.5, 3.6 and 3.7 show, in graphical form, the relationship between analog input voltage and A/D converter output codes.

e.g. In table 3.2 a value of (F)FFFH corresponds to an A/D input voltage of -10V in the range $\pm$10V. In the same range a value of (F)000H will be read if the input voltage of the A/D is 9.9951 (10V - 4.88mV).

If complementary two's complement mode is selected (Table 3.3) a value of (F)FFFH will be read if the input voltage is 0V in the range $\pm$10V. With the same range and code selection, a value of (F)000H corresponds to an A/D input voltage of -4.88mV.

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3.2.2.2 Interrupt Mode

To allow this mode of operation, the interrupts must first be enabled by setting control register data bit D14 high.

A MOVE instruction to the board reads the converted data from the previously addressed channel and starts the conversion process for the next channel at the address just placed on the bus. An interrupt is generated at the end of the conversion. The interrupt can be connected to any one of seven interrupt request lines ($\overline{IRQ1}$-$\overline{IRQ7}$). To allow an interrupt, the interrupts must be enabled both by software, (control register bit D14 high) and by hardware (appropriate selection of switch positions on SW1 and SW3). Refer to sections 2.2.2 and 2.2.3 for selection of switch positions.

After receiving the interrupt request, the main system program can input the converted value with a MOVE instruction thus starting a conversion for the next channel.

3.2.3 CPU Instructions

The CPU exchanges data and control information with the MPV901 series by using MOVE instructions, using the addresses and data lines shown in the address (memory) map of Figure 3.1. These instructions are described in the following list. The selected base address of the board is XXXX80 (factory set to FFF780H). The CPU register Dn is used as the data register (and may be any of the allowable registers within the CPU).

MOVE.W XXXXC0,Dn - This instruction moves the contents of the status register into data bits D08 - D15 of the CPU register Dn.

MOVE.W Dn,XXXXC0 - This instruction moves control data from data bits D08 - D15 of the CPU register, Dn, into the control register of the MPV901.

MOVE.W Dn,XXXXE0 - This instruction moves data bits D00 - D11 of the CPU register, Dn, into analog output OUTØ (MPV901A, MPV901P only).

MOVE.W XXXX80,Dn - These three instructions perform the following actions
MOVE.W XXXXA0,Dn (discussion commencing at the instruction MOVE.W
MOVE.W XXXXBE,Dn XXXXA0,Dn) :- Move the converted input data of channel 0 (address XXXX80 in the single-ended mode) into data bits D00 - D11 of the CPU register and then initiate a conversion at channel 16 (address XXXXA0 in single-ended mode). Then move the converted input data of channel 16 into the CPU data register and initiate a conversion at channel 32 (address XXXXBE in single-ended mode).

This illustrates the procedure for transferring converted data and initiating a conversion at a new channel address.

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Table 3.1
Complementary Straight Binary

	SELECTED RANGE	NEGATIVE FULL SCALE	MIDSCALE	POSITIVE FULL SCALE	RESOLUTION
OUTPUT CODE		(F)FFFH	(F)7FFH	(F)000H	
	0 to +5V	0V	+2.5V	4.9988V	1.22mV
	0 to +10V	0V	+5.0V	9.9976V	2.44mV

Table 3.2
Complementary Offset Binary

	SELECTED RANGE	NEGATIVE FULL SCALE	MIDSCALE	POSITIVE FULL SCALE	RESOLUTION
OUTPUT CODE		(F)FFFH	(F)7FFH	(F)000H	
	±2.5V	-2.5V	0V	2.4988V	1.22mV
	±5.0V	-5.0V	0V	4.9976V	2.44mV
	±10.0V	-10.0V	0V	9.9951V	4.88mV

Table 3.3
Complementary Two's Complement

	SELECTED RANGE	NEGATIVE FULL SCALE	MIDSCALE	POSITIVE FULL SCALE	RESOLUTION
OUTPUT CODE		(F)7FFH	(F)FFFH	(F)800H	
	±2.5V	-2.5V	0V	2.4988V	1.22mV
	±5.0V	-5.0V	0V	4.9976V	2.44mV
	±10.0V	-10.0V	0V	9.9951V	4.88mV

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Figure 3.5
Complementary Straight Binary

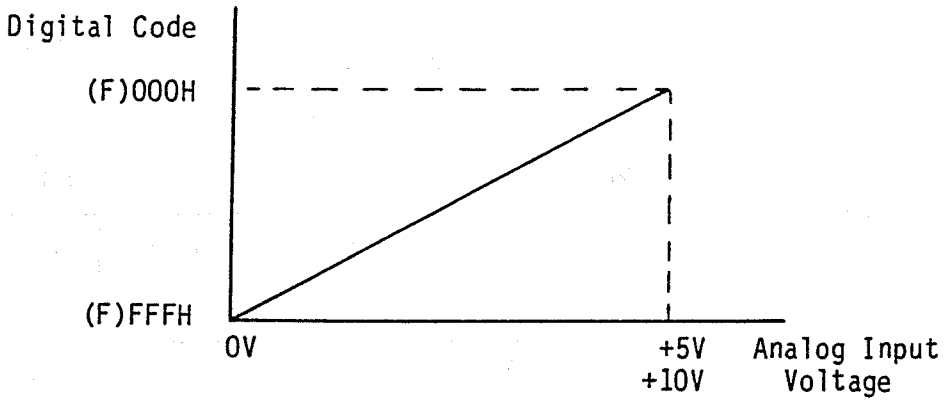


Figure 3.6
Complementary Offset Binary

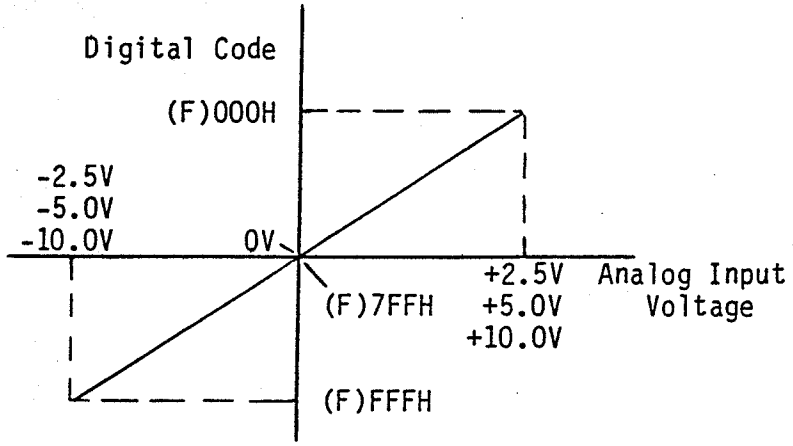
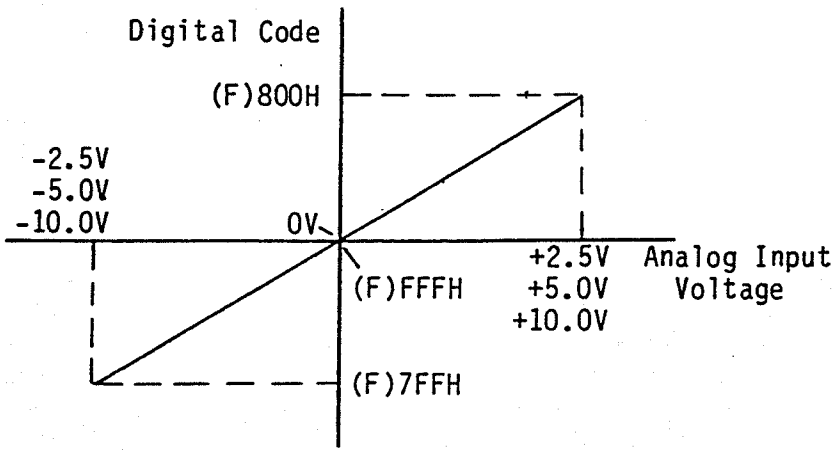


Figure 3.7
Complementary Two's Complement



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3.2.4.2 Calculating Input Voltage from Output Codes

The analog to digital converter input voltage may be calculated from the output code read by the CPU as shown below.

NOTE: The output code consists of 12 significant bits; bits D00-D11. In the CPU register bits D12 to D15 are set when a converted value is read. Before using the following formulae, bits D12 to D15 must be set to Zero for all output codes.

i) Complementary Straight Binary and Complementary Offset Binary

$$\text{A/D Input voltage} = \text{positive full scale} - \frac{\text{code}}{4096} \times \text{range}$$

where,

range = range of input values
code = DECIMAL value of code found in CPU register after conversion (with four MSB's set to zero).

e.g. assume that the code in the CPU register is (F)7FFH and that the range is 0 to +5V for complementary straight binary coding and ±5V for complementary offset binary coding. Then,

$$\text{A/D Input Voltage} = +4.9988 - \frac{2047}{4096} \times 5$$

$$= \underline{2.5V}$$

Referring to Table 3.1 it can be seen for the given conditions that 2.5V is the expected voltage.

In the second case,

$$\text{A/D Input Voltage} = +4.9976 - \frac{2047}{4096} \times 10$$

$$= \underline{0V}$$

Referring to Table 3.2 it can be seen for the given condition that 0V is the expected voltage.

ii) Complementary Two's Complement

$$\text{A/D Input Voltage} = \text{positive full scale} - \frac{\text{code}}{4096} \times \text{range}$$

where,

range = range of input values
code = DECIMAL value of code found in CPU register after conversion (with four MSB's set to zero) AND with data bit D11 inverted.

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e.g. assume that the code in the CPU register is (F)FFFH and that the range is ±10V. Then,

Register code = (F)FFFH

Code (in formula) = Register code with MSB inverted.

= 7FFH

$$\text{A/D Input Voltage} = +9.9951 - \frac{07FF}{4096} \times \text{range}$$

$$= +9.9951 - \frac{2048}{4096} \times 20$$

= 0V

Referring to Table 3.3 it can be seen for an A/D converter code of (F)FFFH that the expected input voltge is 0V.

The A/D covnerter input voltage should be divided by the amplifier gain to calculate the analog input voltage to the board i.e.,

$$\text{Analog Input Voltage} = \frac{\text{A/D Input Voltage}}{\text{Amplifier Gain}}$$

3.2.4.3 Analog Input Range Selection

MPV901P

The analog system as shipped from factory can be software set for input ranges of ±10V to ±10mV. Four amplifier gains are programmable, corresponding with four input ranges as shown in Table 3.4. Note that amplifier gain and input range are closely related.

Table 3.4
Software Programmable Amplifier Input Ranges

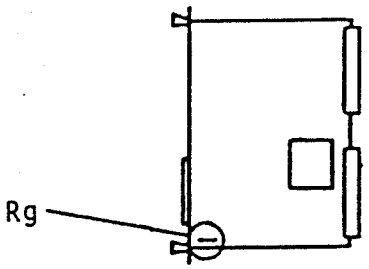
GAIN SETTING D09	GAIN SETTING D08	AMPLIFIER GAIN	*INPUT RANGE	L.S.B. VALUE
0	0	1	±10V	4.88mV
0	1	10	±1V	0.488mV
1	0	100	±100mV	48.8µV
1	1	1000	±10mV	4.88µV

* Assumes A/D converter range of ±10V

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The analog input system can be set for input ranges of ±10V to ±10mV. Binding posts for the external gain setting resistor are provided in order that the instrumentation amplifier can be set for gains between 1 and 1000. The position of the gain setting resistor, Rg, is shown in Figure 3.8:

Figure 3.8



Use the following formula to calculate the value of resistor Rg in kOhm.

$$\text{Gain} = 1 + \frac{40}{Rg} \text{ or } Rg = \frac{40}{\text{Gain}-1} \quad \text{kOhm}$$

A stable resistor (with temperature co-efficient of resistance 5ppm/°C or better) should be used in this application. As shipped from the factory, gain is set to a 1 (no resistor Rg).

The settling time of the amplifier increases as gain increases. To select the correct settling time for a particular gain value. (Section 2.2.7)

Note that the A/D input range and amplifier gain should be selected as a function of each other and as a function of the expected input signal.

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3.2.5 Analog Input Calibration

If the input range of the resistor-programmable amplifier is to be changed, gain and offset should be adjusted. The gain and offset errors of the board may be optimized for any one range by calibrating the unit on that range. The board is factory calibrated on the ±10V range. Before making the adjustments allow the board to reach thermal equilibrium (about 15 minutes under power).

Calibration is performed by connecting a voltage source capable of 0.002% accuracy to any input channel. This could also be a DC voltage source of less absolute accuracy whose output is monitored by a DVM capable of 0.002% accuracy. Offset and gain adjustments are made while applying the voltages listed in Table 3.5.

The positions of the offset and gain adjustment potentiometers RV4 and RV3 are shown in Figure 3.9.

Table 3.5
Input Calibration Values

RANGE	OFFSET	GAIN
0 to +5V	+0.610mV	+4.9982V
0 to +10V	+1.221mV	+9.9963V
±2.5V	-2.4994V	+2.4982V
±5V	-4.9988V	+4.9963V
±10V	-9.9976V	+9.9927V

For other ranges, offset voltage adjustment is made at the most negative value of the range, plus 1/2 x LSB. An LSB is equal to the full scale range divided by 4096 (for 12-bit resolution). Gain adjustment is made at the most positive value of the range less 3/2 x LSB.

Thus for a range of ±10V, 1 x LSB is 20V/4096 = 4.88 mV. The offset adjustment is made at -10V +2.44mV = -9.9976V and the gain adjustment at +10V - 7.32mV = 9.9927V.

The offset calibration is made first by using the offset calibration voltage and the following procedure:

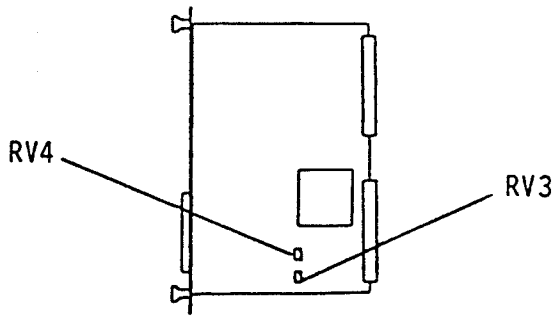
- Set input voltage to appropriate value.
- Adjust the on-board offset potentiometer (RV4) until the output code reads FFFEH.
- Adjust the offset potentiometer until the position where the output code makes the transition from FFFEH to FFFFH.

To perform the gain adjustment, perform the following procedure:

- Set input voltage to appropriate value.
- Adjust the on-board gain potentiometer (RV3) until the output code reads F001H.
- Adjust the gain potentiometer until the position where the output code makes the transition from F001H to F000H.

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Figure 3.9



3.2.6 Analog Output Section

3.2.6.1 Analog Output Voltage and Converter Input Codes

The digital input value of a selected output is converted to a voltage. The digital to analog converter offers two output coding schemes - complementary straight binary (for unipolar ranges) and complementary offset binary (for bipolar ranges).

Tables 3.6 and 3.7 illustrate the full-scale negative, mid-scale and full-scale positive output voltages for the five output ranges with the corresponding digital input codes of the digital to analog converter and the value of the least significant bit (LSB).

Figures 3.10 and 3.11 show in graphical form, the relationship between the digital input codes and the output voltages.

e.g. In Table 3.7 a digital input code of (X)FFFH corresponds to an output voltage of -10V in the range +10V. In the same range a value of (X)000H will produce an output voltage of +9.9951V.

Table 3.6
Complementary Straight Binary

	SELECTED RANGE	NEGATIVE FULL SCALE	MIDSCALE	POSITIVE FULL SCALE	RESOLUTION
OUTPUT CODE		(X)FFFH	(X)7FFH	(X)000H	
	0 to +5V	0.000V	+2.500V	+4.9988V	1.22mV
	0 to +10V	0.000V	+5.000V	+9.9976V	2.44mV

NOTE:- X indicates don't care states

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Figure 3.10
Complementary Straight Binary

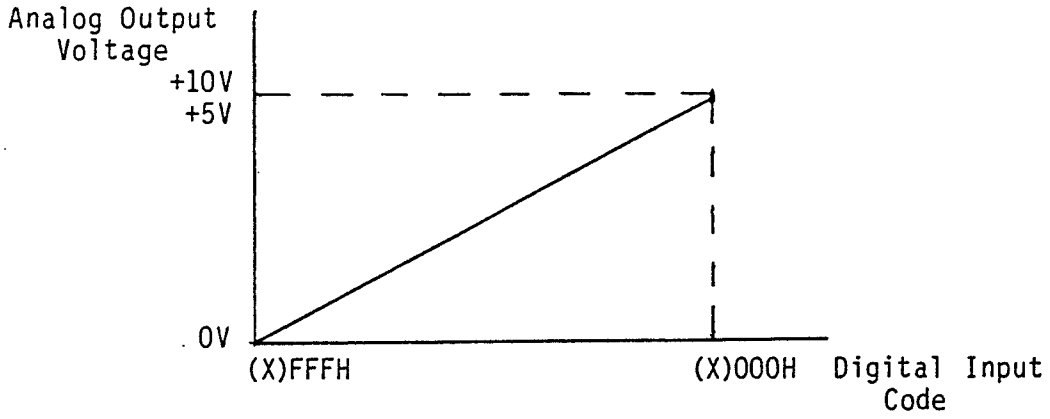
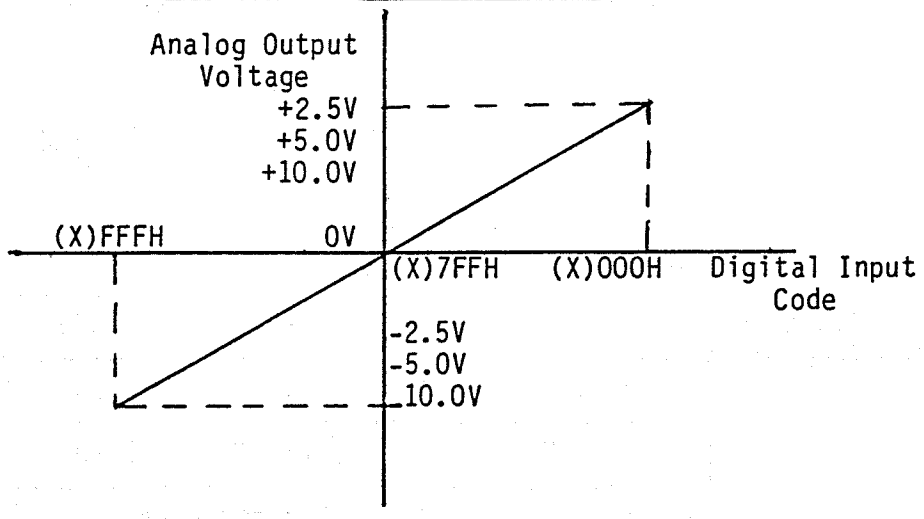


Table 3.7
Complementary Offset Binary

	SELECTED RANGE	NEGATIVE FULL SCALE	MIDSCALE	POSITIVE FULL SCALE	RESOLUTION
OUTPUT CODE		(X)FFFH	(X)7FFH	(X)000H	
	±2.5V	-2.5V	0.000V	+2.4988V	1.22mV
	±5.0V	-5.000V	0.000V	+4.9976V	2.44mV
	±10.0V	-10.000V	0.000V	+9.9951V	4.88mV

NOTE:- X indicates don't care states

Figure 3.11
Complementary Offset Binary



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3.2.6.2 Calculating Output Voltage From Input Code

The digital to analog converter output voltage may be calculated from the input code, written by the CPU, as shown below.

$$\text{Output Voltage} = \text{Negative Full Scale} + (4095\text{-code}) \times \frac{\text{range}}{4096}$$

where,

range = theoretical range of values in the selected output range.
code = DECIMAL value of code placed in CPU register and written to output (with four MSB's set to zero).

NOTE: The input code consists of 12 significant bits; bits D00-D11. In the CPU register bits D12 to D15 can be set to any value before data is written to the output. However, before using the following formula, bits D12 to D15 must be set to 0 for all input codes.

e.g. consider an output range of ±10V and an output code of 7FFH. Then,

range = +10V - (-10V)
= 20V

code = Decimal value of 7FFH
= 2047

$$\text{Output voltage} = -10V + (4095 - 2047) \times \frac{20}{4096}$$

$$= 0V$$

Referring to Table 3.7 it can be seen that for an input code of 7FFH, the expected voltage is 0V.

3.2.6.3 Output Range Selection

The digital to analog converters are factory set for a range of ±10V with complementary offset binary coding. Other output ranges can be selected as described in section 2.2.8.

The analog outputs default, on power-up, to the most positive value in the selected range. The maximum output current is 5mA per output on all ranges.

3.2.6.4 Output Check

Static checks of the two analog outputs can be performed by loading the DAC locations with an output data word. Their base addresses XXXXE0 and XXXXE2 are factory set to FFF7E0H and FFF7E2H (refer to address map Figure 3.1). The ideal values for positive and negative full scale are shown in Tables 3.6 and 3.7. The most significant four bits of the data word (D11-D15) are don't care states.

A program which performs a simple dynamic check of the two analog outputs is listed in section 5.8.

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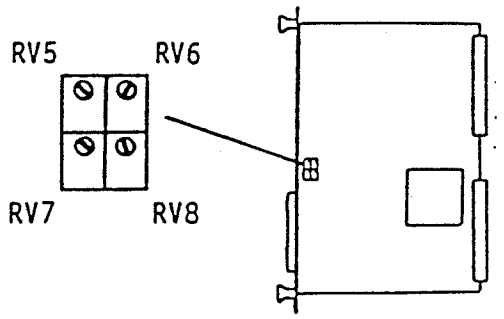
3.2.7 Output Calibration

To calibrate the analog outputs, install the board in a VMEbus racking system and allow it to reach thermal equilibrium (about 15 minutes under power) before commencing the procedure. The positions of the calibration potentiometers are shown in Figure 3.12.

1. Load both DACS with data that will produce the most negative output (code FFFH).

2. Set the DACS by their offset control (RV6 for OUTØ and RV8 for OUT1) to the appropriate LOW voltage value shown in Table 3.7 for the different ranges.

Figure 3.12



3. Load both DACS with data that will produce the most positve output (code 000H).

4. Set the DACS by their gain control (RV5 for OUTØ and RV7 for OUT1) tc the appropriate HIGH voltage value shown in Table 3.5 for the different ranges.

Table 3.8
DAC Calibration Values

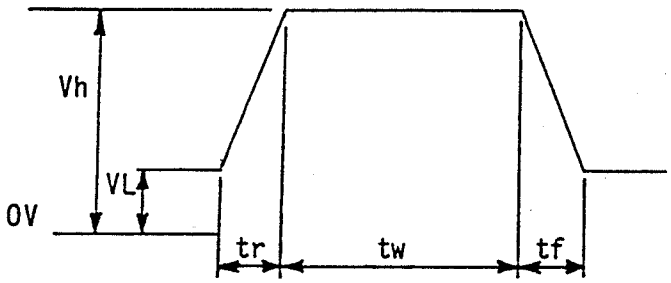
RANGE	LOW	HIGH	1 LSB
±10V	-10.000V	+9.9951V	4.88mV
±5V	-5.000V	+4.9976V	2.44mV
±2.5V	-2.500V	+2.4988V	1.22mV
0 to +5V	0.000V	+4.9988V	1.22mV
0 to +10V	0.000V	+9.9976V	2.44mV

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3.3 External Trigger

A TTL compatible input signal can be used to externally trigger the board (synchronize conversions with external or off-board events). Details of the trigger signal are shown in Figure 3.13 below.

Figure 3.13



	Max	Min
V_L	+0.8V	0V
V_h	+5V	+2V
tr	1µs	-
tw	-	300nS
tf	1µs	-

The data acquisition and conversion process is initiated on the rising edge of the trigger signal.

The maximum trigger signal repetition rate must not exceed the rate at which an input can be acquired and converted since each application of the trigger signal causes the conversion process to re-start.

The following sequence of operations should be performed when using external trigger:-

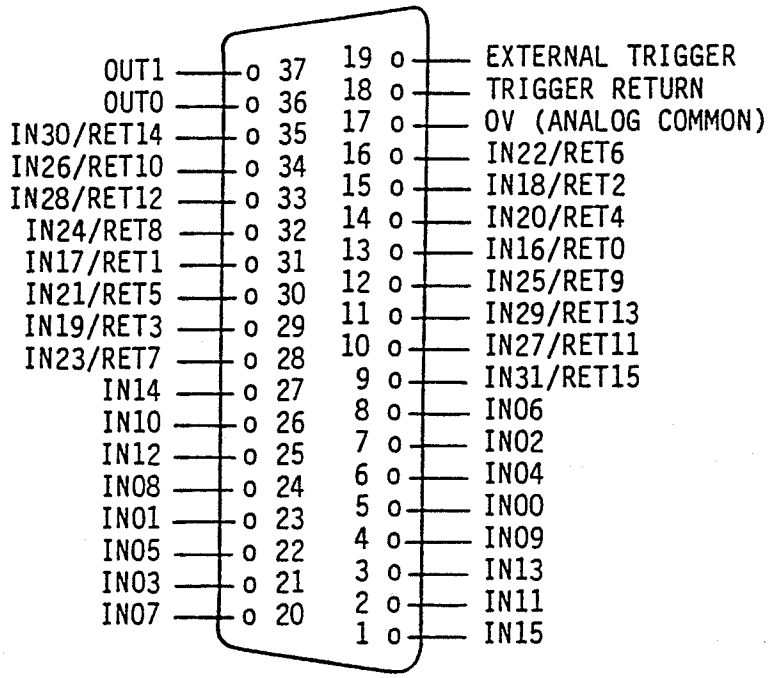
1. Change the jumper link from J5 to J4.
2. Set control register to enable external trigger instruction.
3. Select channel to be converted (perform a READ operation using a MOVE instruction).
4. Apply external trigger.
5. Monitor STATUS or INTERRUPT to determine end of conversion.
6. READ converted data (using MOVE instruction at next channel to be converted).
7. Return to 4 and repeat.

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3.4 Analog Connector

The analog front panel connector, P3, is a 37 way 'D' type socket (female). The mating connector should be a 37 way 'D' type plug (male). Use Cannon type DC37P/1A1N or equivalent.

Connector Pinout 'D' Type



NOTE: Unused inputs should be connected to 0V (ANALOG COMMON).

3.5 Factory Set Configuration

All boards are shipped from the factory ready for immediate use, however, they do have a number of user selectable options. These options and their factory set conditions, which have already been described, are summarized below:

BASE ADDRESS	FFF780H
ADDRESS/AM RESPONSE	SHORT ADDRESSING, ALL AM CODES
INTERRUPT REQUEST	NONE
INTERRUPTS	DISABLED
INTERRUPT VECTOR	FFH
CHANNEL ARRANGEMENT	32 SINGLE-ENDED
AMPLIFIER GAIN	1
A/D INPUT RANGE	+10V
A/D OUTPUT CODING	COMPLEMENTARY OFFSET BINARY
ANALOG OUTPUT RANGE (MPV901A, MPV901P)	±10V (BOTH OUTPUTS)
EXTERNAL/INTERNAL TRIGGERING	INTERNAL

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Chapter 4 - FUNCTIONAL DESCRIPTION

4.1 INTRODUCTION

This chapter is intended to provide a background to the theory of operation for the MPV901 series. It should be read while referring to the schematics, major component data sheets (Chapter 6), and where appropriate, other chapters in this manual.

4.2 GENERAL INFORMATION

The MPV901 is a data acquisition board that interfaces directly to the VMEbus. Figure 4.1, 4.2 and 4.3 are block diagrams of the different versions available, ie, MPV901, MPV901A, MPV901P.

4.3 THEORY OF OPERATION

4.3.1 Decoder

The address decoding section consists of two eight bit magnitude comparators (IC20,IC24). These devices monitor address bits A08 to A23 inclusive. The address bit supplies one input to a two input comparator within IC20 and IC24 while the other input is switched to either +5V or ground through switch SW2 or SW3. When the monitored level of address bit on the bus matches the corresponding level set by the switches, the output of the appropriate comparator goes HIGH. This process occurs for all eight inputs within each of the IC's. When the result of the eight comparisons is true (ie, monitored levels are the same as set levels), the output ($\overline{P = Q}$) goes LOW.

The address modifier (AM) decoding section consists of PROM IC11. The PROM is mounted on a socket and can be user programmed to give the desired response to AM codes. The factory set prom codes are 3D and 39.

The response to AM codes can be controlled by using jumpers J20 and J21. With both jumpers removed, Address Lines A08 to A23 are decoded along with the AM lines AM0 to AM5.

With jumper J20 inserted and J21 removed only Address Lines A08 to A23 are decoded with AM lines AM0 to AM5 being ignored.

With both jumpers inserted only Address Lines A08 to A15 are decoded (short addressing) with AM lines AM0 to AM5 being ignored.

The operation of the AM decoding would be as follows. The CPU places an address and address modifier code on the appropriate bus lines. (The address lines are decoded as previously described). Upon receipt of $\overline{AS}$, the address modifier code is decoded by the PROM, an acceptable code resulting in the appropriate PROM output pin in goin LOW. An unrecognisable AM code would result in the PROM outputs remaining HIGH.

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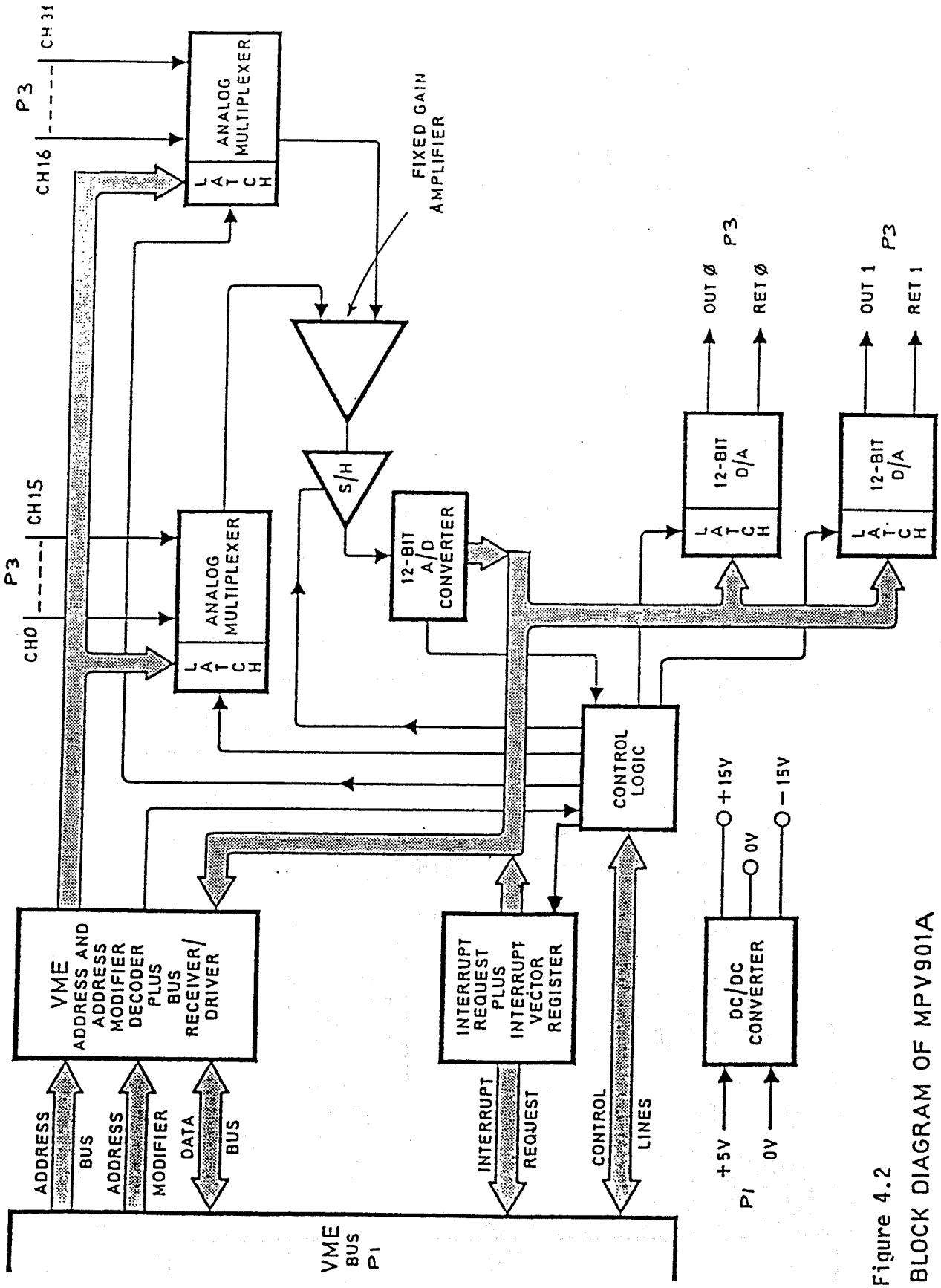


Figure 4.2
BLOCK DIAGRAM OF MPV901A

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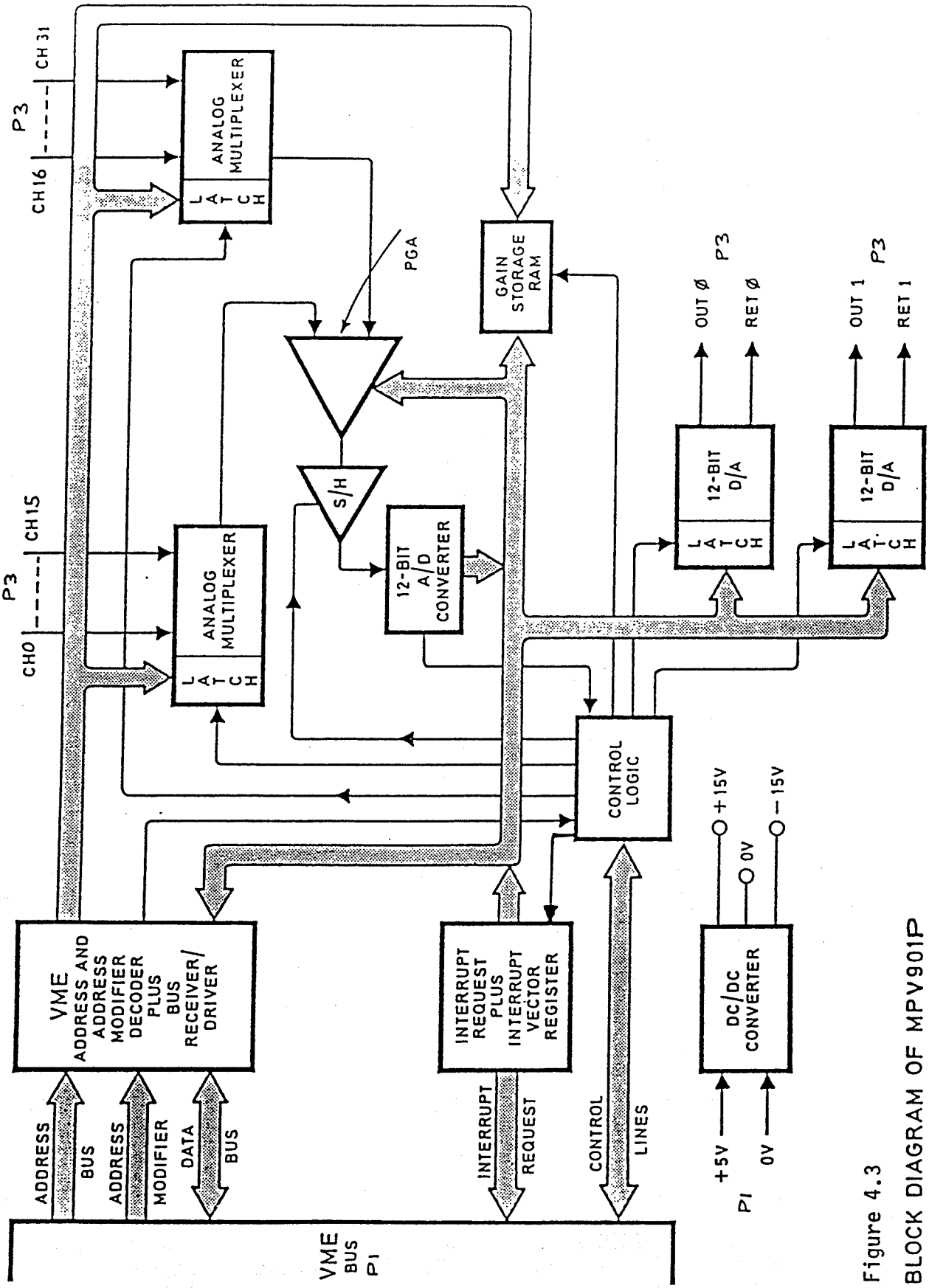


Figure 4.3
BLOCK DIAGRAM OF MPV901P

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4.3.5 Analog To Digital Converter

The A/D used in the MPV901 is the ADC80AG. The analog input is held steady during conversion by the S/H. The A/D can be jumpered for 0 to 5V, 0 to 10V, +2.5V, +5V or +10V operation by the proper arrangement of J6, J7, J8, J9 and J10. Gain and offset of the A/D are controlled (adjustable) by RV3 and RV4. The 12 bit output of the A/D is placed on the data bus as a single word on data lines D00 - D11 with the remaining lines D12 - D15 being in the high state.

The MPV901 is factory set for complementary offset binary output code.

4.3.6 Analog Timing And Control

The multiplexer, amplifier and sample/hold have settling times associated with them. The multiplexer settling time is essentially fixed. The S/H acquisition time must be designed for worst case conditions and is therefore also fixed. The amplifier settling time however, is a function of gain and also depends upon whether or not the input signal is switched between channels. The settling time of the amplifiers (both INA101 and PGA200), can be considerable at high gain values (eg, 700µs). IC41, IC43, IC49 and IC51 "calculate" the optimum settling time required for a given set of conditions (channel and gain) by comparing past and present parameters and then allowing sufficient amplifier settling time before applying a convert pulse to the A/D.

This has the effect of allowing the MPV901 to operate at maximum throughput regardless of the gain settings on individual channels, eg, without this facility and one channel set at a gain of 1000, the settling delay for all 32 channels would have to be set at the delay for a gain of 1000. This would result in considerably reduced throughput over the system described which would only insert maximum delay at the required condition.

The circuit operates by storing the previous conditions (channel selected and gain) in IC49 and comparing this information with the present conditions (stored in IC45). IC51 compares the information and sets the delay by selecting the appropriate switch combination(s) on IC43 which connects the counter/timer outputs on IC41 to the S/H control pin, and A/D converter pin.

4.3.7 DAC Output (MPV901A, MPV901P)

Two independent analog output channels with 12 bit resolution are provided on MPV901A and MPV901P versions. The analog outputs are switch selectable for the ranges 0 to +5V, 0 to +10V, ±2.5V, ±5V, or ±10V, with an output current of 5mA, by proper selection of switch SW6. Gain and offset adjustment of each output is performed by RV5, RV6, RV7 and RV8.

IC37 and IC38 store the data for output OUTØ whilst IC34 and IC35 store the data for output OUT1. Data should be presented on the VMEbus data lines D00 - D11 during a write operation to the appropriate location (FFF7E0H for OUTØ, and FFF7E2H for OUT1, as factory set). The data will then be stored in the appropriate IC pair until over written by a new value.

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4.3.8 Control/Status Register

An octal latch IC7 is used as the control register.

A write to memory location FFF7C0H (factory set), will cause the data bits D08 - D15 to be captured by the latch. The use of each of the bits within the control register is as described in section 3.2.1.2.

The output of the control register is passed back to the data bus to allow the CPU to look at the content. This is called the status of the board and includes a conversion complete flag in the data bit 15 position. Data is read by a MOVE instruction from memory location FFF7C0H (factory set).

4.3.9 Random Access Memory(MPV901P)

The RAM (IC33), is a 256 x 4 bit read/write memory with independent inputs and outputs. Channel gains can be stored in the RAM for all 32 channels. The data outputs are enabled when bit D12 of the control register is set high by the CPU. This puts a low level on pin 18 of the RAM to enable the outputs and high level on pin 15 of the buffer IC3 to put the two gain bit buffers in the tri-state mode. The RAM output now drives the PGA gain inputs through IC45.

To write new gain values into the RAM, bit D13 of the control register should first be set to a zero. This allows, during a write operation to the RAM, a negative pulse to appear at pin 20 and hence cause the data on lines D08 and D09 to be written into the RAM.

4.3.10 Interrupt Logic

During the interrupt mode of the operation, the MPV901 supplies the interrupt vector on data lines D00 - D07 when requested by the CPU, by enabling pins 1 and 19 of IC12 which causes the 8 bit vector to be output to the VMEbus through IC6.

The interrupt mode of operation must first be enabled by setting the control register bit D14 to a '1'. This places a high level on IC26 pin 9 and IC28 pin 4. Upon completion of a conversion IC16 pin 5, goes high causing IC28 pin 5 to go low thereby causing an interrupt request (IC28 pin 6 low) on the line selected by SW1.

During the interrupt acknowledge cycle, IC30 decodes address lines A01, A02, A03 to determine the level of the interrupt being serviced. If the request and service levels match, IC30 pin 6 (A = B) goes high, eventually causing IC12 pins 1 and 19 to go low and hence the vector to be placed on the bus.

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5.4 Analog Input and Output in Polling Mode (MPV901A, MPV901P)

This program reads the converted data for channel 2 (in single-ended mode) using the polling mode of operation and writes the converted data value to analog output OUTØ.

NOTE:- For input and output signals to be identical, the A/D converter and D/A converter should be set to the same range.

```
            ORG       @$1000;          Start address of program storage.
BASEADD:    EQU       @$FFF780;        Factory set board base address.
CH2ADD:     EQU       BASEADD+$4;      Channel 2 address in single-ended
                                       mode.
REGADD:     EQU       BASEADD+$40;     Status and control register address.
OUTADD:     EQU       BASEADD+$60;     Address of analog output OUTØ.
REGVAL:     EQU       #$0000A8FF;      Disables board interrupt. Disables
                                       RAM on MPV901P and selects amplifier
                                       gain 1.
                                       Use #$0000A9FF for a gain of 10.
                                       Use #$0000AAFF for a gain of 100.
                                       Use #$0000ABFF for a gain of 1000.

            MOVE.L    #0,D3;           Clears D3 so that existing data
                                       does not interfere with comparison in
                                       polling loop.
            MOVE.L    REGVAL,REGADD;   Loads the control register of the
                                       analog board with A8, A9, AA, or AB,
                                       which disables both the interrupts
                                       and the gain RAM and sets up a gain
                                       of 1, 10, 100 or 1000 on MPV901P.

NEXT:       MOVE.W    CH2ADD,D0;       Stores data of the input channel in
                                       register D0 and starts the conversion
                                       for the addressed channel.

POLL:       MOVE.W    REGADD,D3;       Keep polling bit 15 of the status
                                       register until conversion is
                                       complete.
            CMPI      REGVAL,D3;
            BNE       POLL;

            MOVE.W    D0,OUTADD;       Sends the converted data from D0 to
                                       the analog output OUTØ.
            JMP       NEXT;            Repeat.
```


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5.5 Analog Input and Output in Interrrupt Mode (MPV901A, MPV901P)

This program reads the converted data for channel 3 (in single-ended mode), using the interrupt mode of operation and writes the converted data value to analog output OUT1.

The interrupt request line used is IRQ3 and the interrupt vector 40H. The location of the interrupt pointer is 100H.

NOTE:- For input and output signals to be identical, the A/D converter and the D/A converter should be set to the same range.

```
            ORG       @$1000;          Start address of program storage.
BASEADD:    EQU       @$FFF780;        Factory set board base address.
CH3ADD:     EQU       BASEADD+$6;      Channel 3 address in single-ended
                                       mode.
REGADD:     EQU       BASEADD+$40;     Status and control register address.
OUTADD:     EQU       BASEADD+$62;     Address of analog output OUT1.
REGVAL:     EQU       #$0000E8FF;      Enables board interrupt on conversion
                                       complete. Disables RAM on MPV901P
                                       and selects amplifier gain 1.
                                       Use #$0000E9FF for a gain of 10.
                                       Use #$0000EAFF for a gain of 100.
                                       Use #$0000EBFF for a gain of 1000.
REGRST:     EQU       #$0000A8FF;      Disables board interrupt.
                                       Use #$0000A9FF for a gain of 10.
                                       Use #$0000AAFF for a gain of 100.
                                       Use #$0000ABFF for a gain of 1000.

INTADD:     EQU       #$1F00;          Interrupt routine start address.

            MOVE.W    #$2000,SR;       Enables the CPU to service interrupts
                                       on all 7 lines.
            MOVE.L    REGVAL,REGADD;   Loads the control register of the
                                       analog board with E8, E9, EA, or EB,
                                       which enables interrupts on
                                       completion of conversion, disables
                                       the gain RAM and sets up a gain of 1,
                                       10. 100 or 100 on MPV901P.
            MOVE.L    INTADD,@$100;    Load interrupt location pointer with
                                       interrupt start address.
            MOVE.W    CH3ADD,D0;       Stores a meaningless value in D0 and
                                       starts the conversion for the
                                       addressed channel.
WAIT:       NOP;                       Wait for interrupt.
            JMP       WAIT;
```

Interrupt routine

```
            ORG       @$1F00;          Start address of interrupt routine.
            MOVE.W    D0,OUTADD;       Sends the converted data from D0 to
                                       the analog output.
            MOVE.W    CH3ADD,D0;       Stores converted data in D0 and
                                       starts new conversion for the same
                                       channel.
            RTE;                       Return from interrupt.
```


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5.6 Storing Different Gain Values In RAM (MPV901P)

This program stores a different value of gain for each of four selected input channels.

```
            ORG     @$1000;              Start address of program storage.
BASEADD:    EQU     @$FFF780;            Factory set board base address.

            MOVE.L  #$000088FF,BASEADD+$40; Set up control register to
                                           write into RAM, disable interrupt.
            MOVE.W  #$0000,BASEADD+$8;   Store gain of 1 for channel 4.
            MOVE.W  #$0100,BASEADD+$16;  Store gain of 10 for channel 11.
            MOVE.W  #$0200,BASEADD+$24;  Store gain of 100 for channel 18.
            MOVE.W  #$0300,BASEADD+$3C;  Store gain of 1000 for channel
                                           30.
            MOVE.L  #$0000B8FF,BASEADD+$40; Set up control register to
                                           enable RAM output.
```

5.7 Storing Identical Gain Values In RAM (MPV901P)

This program stores a gain of 10 for channels Ø through 7.

```
            ORG     @$1000;              Start address of program storage.
BASEADD:    EQU     @$FFF780;            Factory set board base address.

            MOVE.L  #000088FF,BASEADD+$40; Set up control register to
                                           write into RAM, disable interrupt.
            MOVE.W  #$0100,D0;           Store gain of 10 in D0.
            LEA.L   BASEADD,A0;          Load A0 with address of channel Ø
            MOVE.W  #7,D6;
NEXT:       MOVE.W  D0,(A0)+;            Store gain of 10 in RAM and
                                           increment RAM address.
            DBEQ    D6,NEXT;
            MOVE.L  #$0000B8FF,BASEADD+$40; Set up control register to
                                           enable RAM output.
```


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5.8 Analog Output Dynamic Test (MPV901P)

This program performs a simple dynamic check of the two analog outputs. A ramp (sawtooth) waveform with amplitude plus and minus full scale and frequency approximately 1.25kHz will be produced at each output. The constant "STEP" can be altered in the program to give different frequencies and number of steps in the output waveform (eg, changing "STEP" to 63H will give an output frequency of approximately 2.5 kHz).

```
            ORG       @$1000;          Start address of program storage.
BASEADD:    EQU       @$FFF780;        Factory set board base address.
REGADD:     EQU       BASEADD+$40;     Status and control register address.
OUTØADD:    EQU       BASEADD+$60;     Address of analog output OUTØ.
OUT1ADD:    EQU       BASEADD+$62;     Address of analog output OUT1.
STRVAL:     EQU       #$0000;          Positive full scale value.
                                       Use #$0FFF for negative full scale
                                       value.
REGVAL:     EQU       #$0000A8FF;      Disables board interrupt. Disables RAM
                                       on MPV901P and selects amplifier gain
                                       1.
STEP:       EQU       #$0031;          Set frequency and number of steps.


            MOVE.L    REGVAL,REGADD;   Loads the control regiter of the analog
                                       board with hex A8, which disables both
                                       the interrupts and the gain RAM and
                                       sets up a gain of 1 on MPV901P.
            MOVE.W    STRVAL,D0;       Starting value for full scale in D0.
LOOP:       MOVE.W    D0,OUTØADD;      Data to OUTØ.
            MOVE.W    D0,OUT1ADD;      Data to OUT1.
            ADDI      STEP,D0;         Increment value in D0.
            JMP       LOOP;
```


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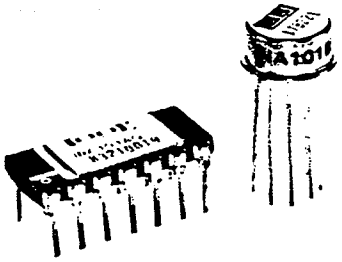
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Chapter 6 - SUPPORT INFORMATION

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BURR-BROWN®



INA101

Very-High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- ULTRA-LOW VOLTAGE DRIFT - 0.25μV/°C
- LOW OFFSET VOLTAGE - 25μV
- LOW NONLINEARITY - 0.002%
- LOW NOISE - 13nV/√Hz at f_0 = 1kHz
- HIGH CMR - 106dB at 60Hz
- HIGH INPUT IMPEDANCE - $10^{10}\Omega$
- LOW COST

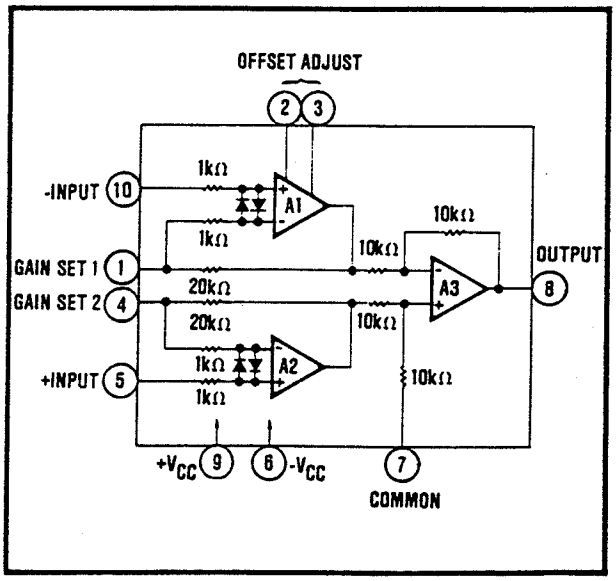
APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gages
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCERS
- LOW LEVEL SIGNALS
- MEDICAL INSTRUMENTATION

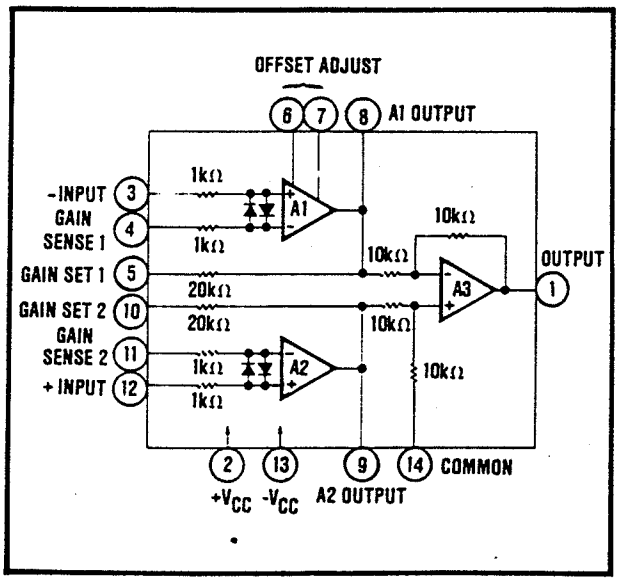
DESCRIPTION

The INA101 is a high accuracy, multistage, integrated-circuit instrumentation amplifier designed for signal conditioning requirements where very-high performance is desired. All circuits, including the interconnected laser-trimmed thin-film resistors, are integrated on a single monolithic substrate.

A multiamplifier design is used to provide the highest performance and maximum versatility with monolithic construction for low cost. The input stage uses Burr-Brown's ultra-low drift, low noise technology to provide exceptional input characteristics.



M Package



G Package

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

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PDS-454D

Printed in U.S.A. July, 1983

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SPECIFICATIONS

ELECTRICAL

At +25°C with ±15VDC power supply and in circuit of Figure 2 unless otherwise noted.

MODEL	INA101AM/AG			INA101SM/SG			INA101CM/CG			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
GAIN										
Range of Gain	1		1000	•		•	•		•	V/V
Gain Equation		G = 1 + (40k/R_G)			•			•		V/V
Error From Equation, DC[1][2]		±(0.04±0.00016G - 0.02/G)	±(0.1±0.003G - 0.05/G)		•	•		•	•	% of FS
Gain Temp. Coefficient[3]										
G = 1		2	5		•	•		2	5	ppm/°C
G = 10		20	100		•	•		10	50	ppm/°C
G = 100		22	110		•	•		11	55	ppm/°C
G = 1000		22	110		•	•		11	55	ppm/°C
Nonlinearity, DC[2]		±(0.002 + 10^{-5}G)	±(0.005 + 2 × 10^{-5}G)		±(0.001 + 10^{-5}G)	±(0.002 + 10^{-5}G)		±(0.001 + 10^{-5}G)	±(0.002 + 10^{-5}G)	% of p-p
RATED OUTPUT										
Voltage	±10	±12.5		•	•		•	•		V
Current	±5	±10		•	•		•	•		mA
Output Impedance		0.2			•			•		Ω
INPUT OFFSET VOLTAGE										
Initial Offset at +25°C[2]		±25 +200/G	±50 ±400/G		±10 ±100/G	±25 ±200/G		±10 ±100/G	±25 ±200/G	µV
vs. Temperature[2]			±2 ±20/G			±0.75 ±10/G			±0.25 ±10/G	µV/°C
vs. Supply		±(1 + 20/G)			•			•		µV/V
vs. Time		±(1 +20/G)			•			•		µV/mo
INPUT BIAS CURRENT										
Initial Bias Current[2] (each input)		±15	±30		±10	±30		±5	±20	nA
vs. Temperature		±0.2			•			•		nA/°C
vs. Supply		±0.1			•			•		nA/V
Initial Offset Current[2]		±15	±30		±10	±30		±5	±20	nA
vs. Temperature		±0.5			•			•		nA/°C
INPUT IMPEDANCE										
Differential		10^{10} ‖ 3			•			•		Ω ‖ pF
Common-mode		10^{10} ‖ 3			•			•		Ω ‖ pF
INPUT VOLTAGE RANGE										
Range, Linear Response	±10			•	•		•	•		V
CMR with 1kΩ Source Imbal.										
DC to 60Hz, G = 1[2]	80	90		•	•		•	•		dB
DC to 60Hz, G = 10	96	106		•	•		•	•		dB
DC to 60Hz, G = 100 to 1000	106	110		•	•		•	•		dB
INPUT NOISE										
Input Voltage Noise										
f_B = 0.01Hz to 10Hz		0.8			•			•		µV, p-p
Density, G = 1000										
f_o = 10Hz		18			•			•		nV/√Hz
f_o = 100Hz		15			•			•		nV/√Hz
f_o = 1kHz		13			•			•		nV/√Hz
Input Current Noise										
f_B = 0.01Hz to 10Hz		50			•			•		pA, p-p
Density										
f_o = 10Hz		0.8			•			•		pA/√Hz
f_o = 100Hz		0.46			•			•		pA/√Hz
f_o = 1kHz		0.35			•			•		pA/√Hz
DYNAMIC RESPONSE										
Small Signal, ±3dB Flatness										
G = 1		300			•			•		kHz
G = 10		140			•			•		kHz
G = 100		25			•			•		kHz
G = 1000		2.5			•			•		kHz
Small Signal, ±1% Flatness										
G = 1		20			•			•		kHz
G = 10		10			•			•		kHz
G = 100		1			•			•		kHz
G = 1000		200			•			•		Hz
Full Power, G = 1 to 100		6.4			•			•		kHz
Slew Rate, G = 1 to 100[2]	0.2	0.4		•	•		•	•		V/µsec
Settling Time (0.1%)										
G = 1		30	40		•	•		•	•	µsec
G = 100		40	55		•	•		•	•	µsec
G = 1000		35	470		•	•		•	•	µsec
Settling Time (0.01%										
G = 1		30	45		•	•		•	•	µsec
G = 100		50	70		•	•		•	•	µsec
G = 1000		500	650		•	•		•	•	µsec

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ELECTRICAL (CONT)

MODEL	INA101AM/AG			INA101SM/SG			INA101CM/CG			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
POWER SUPPLY										
Rated Voltage		±15			•			•		V
Voltage Range	±5		±20	•		•	•		•	V
Current, Quiescent [2]		±6.7	±8.5		•	•		•	•	mA
TEMPERATURE RANGE										
Specification	-25		+85	-55		+125	•		•	°C
Operation	-55		+125	•		•	•		•	°C
Storage	-65		+150	•		•	•		•	°C

*Specifications same as for INA101AM/AG.

NOTES:
1. Typically the tolerance of R_G will be the major source of gain error.
2. Specifically tested for /883.
3. Not including the TCR of R_G.
4. Adjustable to zero at any one gain.

The information in this publication has been carefully checked and is believed to be reliable; however, no responsibility is assumed for possible inaccuracies or omissions. Prices and specifications are subject to change without notice. No patent rights are granted to any of the circuits described herein.

ABSOLUTE MAXIMUM RATINGS

Supply	±20V
Internal Power Dissipation	600mW
Input Voltage Range	±Vcc
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-Circuit Duration	Continuous to ground

SG/SM/883 SCREENING PROCEDURES

SCREEN	METHOD	CONDITION
Internal Visual	Method 2010	Condition B
Interim Electrical Test	Per SM/SG spec (4)	
High Temperature Storage (Stabilization Bake)	Method 1008	Condition C
Temperature Cycling	Method 1010	Condition C
Constant Acceleration	Method 2001	Condition E, Y_1 Plane
Burn-in	Method 1015	Condition B
Seal	Method 1014	
Fine Leak		Condition A1
Gross Leak		Condition C
Final Test including temperature drift of offset and gain	Per SM/SG spec (4)	
External Visual	Method 2009	

ORDERING INFORMATION

INA101 C G

Basic Model Number

Performance Grade Code
- S: -55°C to +125°C
- A, C: -25°C to +85°C

Package Code
- M: TO-100
- G: 14-Pin Hermetic DIP

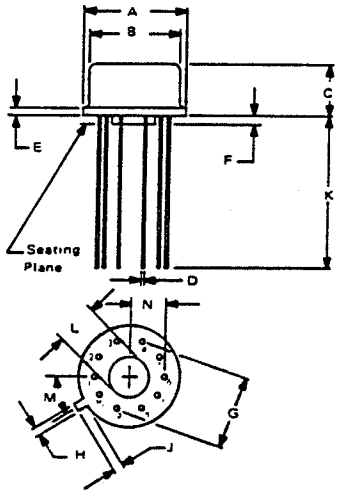
TO-100 (M Suffix)	Hermetic DIP (G Suffix)
INA101AM	INA101AG
INA101CM	INA101CG
INA101SM	INA101SG
INA101SM/883*	INA101SG/883*

*S grade available with MIL-STD-883 screening. To order add /833 as suffix to part number.

MECHANICAL

M Package

TO-100



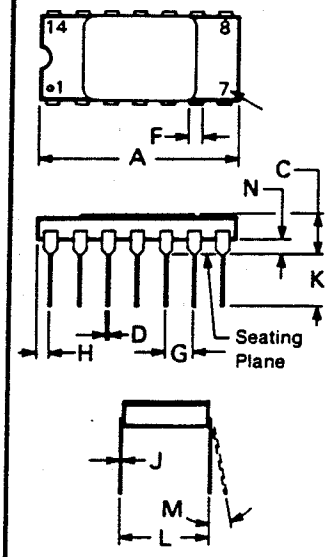
NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.70	--
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

G Package

Hermetic DIP



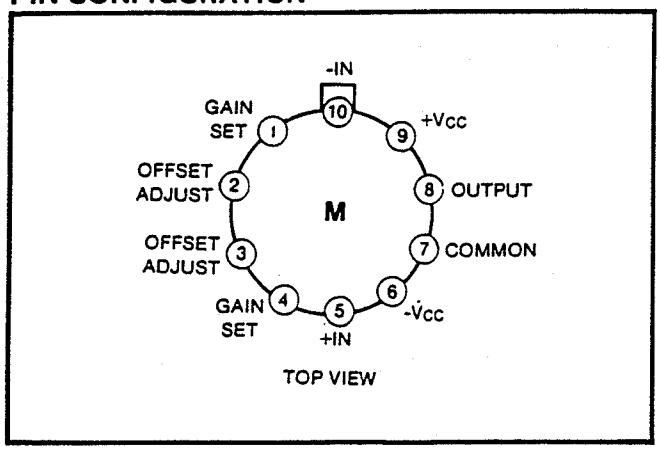
Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

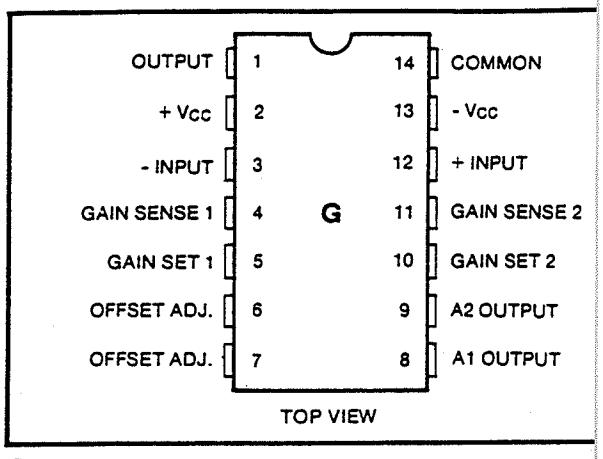
Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.009	.060	0.23	1.52

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PIN CONFIGURATION

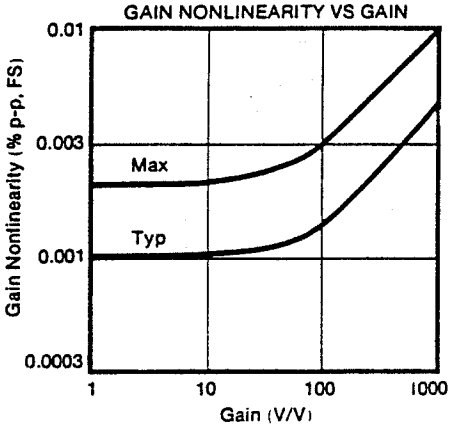




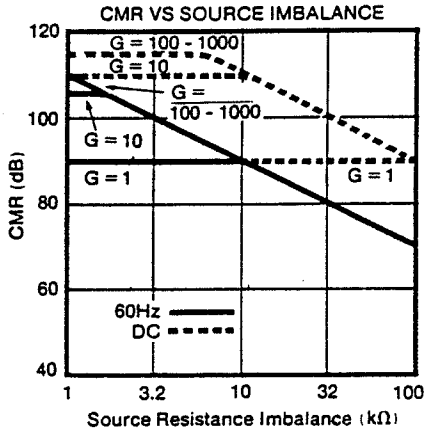
TYPICAL PERFORMANCE CURVES

At +25°C and in circuit of Figure 2 unless otherwise noted.

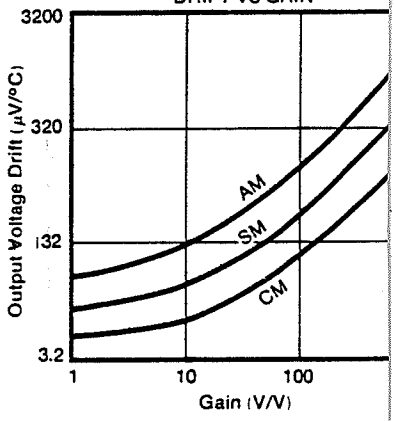
GAIN NONLINEARITY VS GAIN



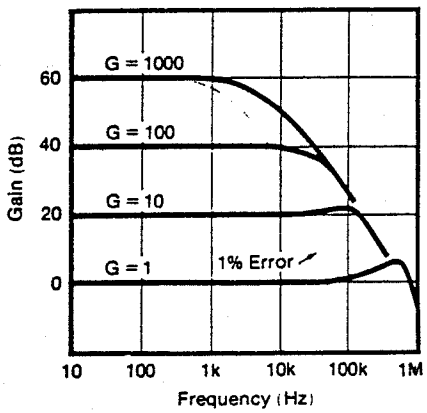
CMR VS SOURCE IMBALANCE



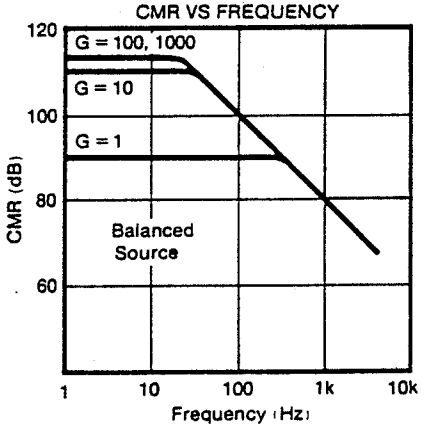
TOTAL OFFSET VOLTAGE DRIFT VS GAIN



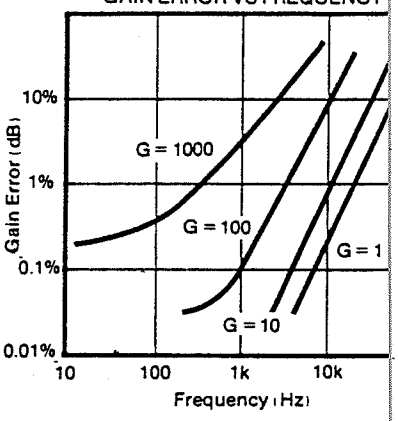
GAIN VS FREQUENCY



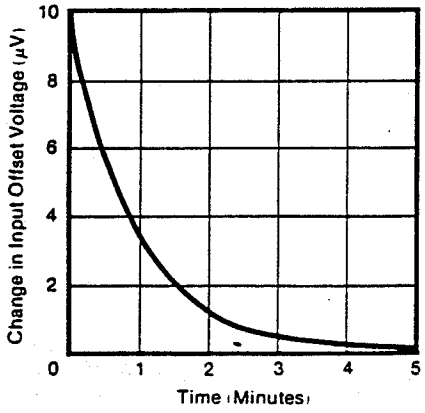
CMR VS FREQUENCY



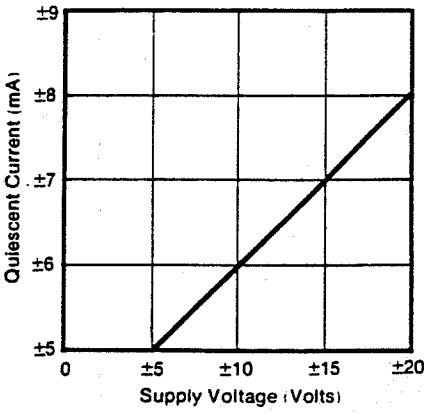
GAIN ERROR VS FREQUENCY



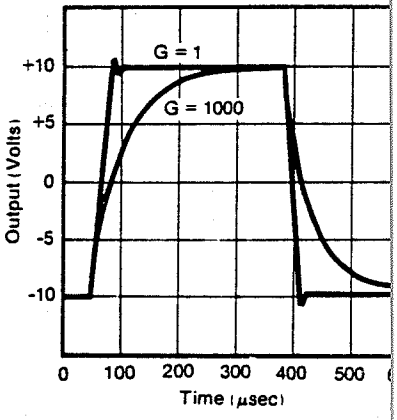
WARM-UP DRIFT VS TIME



QUIESCENT CURRENT VS SUPPLY

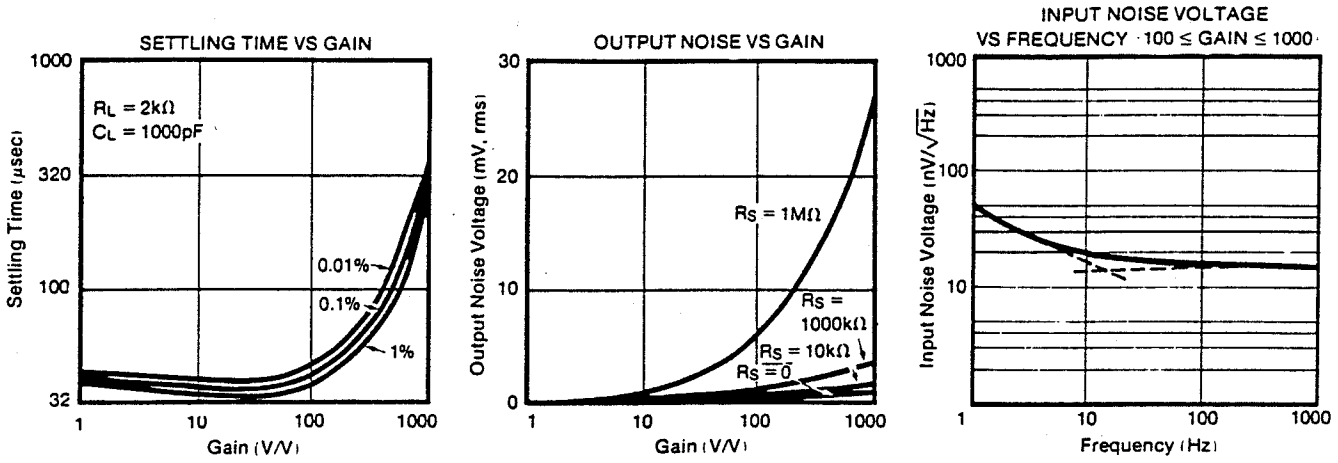


STEP RESPONSE



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TYPICAL PERFORMANCE CURVES (CONT)



DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are differential input closed-loop gain blocks whose committed circuit accurately amplifies the voltage applied to their inputs. They respond only to the difference between the two input signals and exhibit extremely-high input impedance, both differentially and common-mode. Feedback networks are packaged within the amplifier module. Only one external gain setting resistor must be added. An operational amplifier, on the other hand, is an open-loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is very difficult to reach the same level of performance. Using op amps often leads to design trade-offs when it is necessary to amplify low level signals in the presence of common-mode voltages while maintaining high input impedances. Figure 1 shows a simplified model of an instrumentation amplifier that eliminates most of the problems.

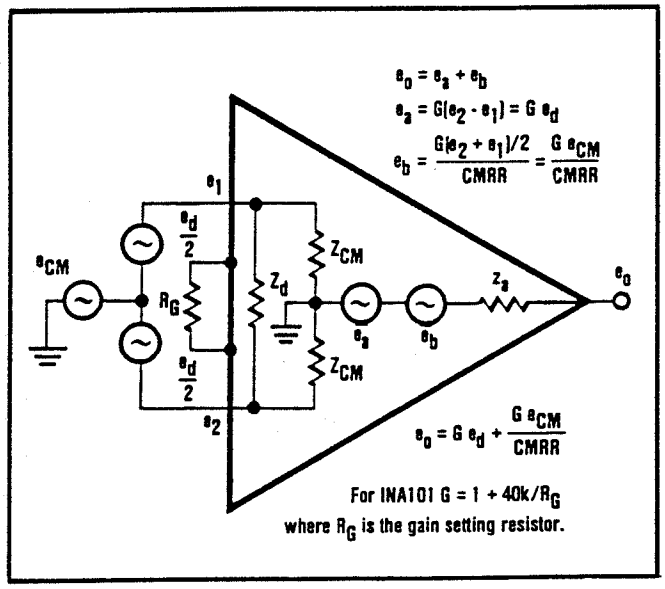


FIGURE 1. Model of an Instrumentation Amplifier.

THE INA101

Simplified schematics of the INA101 are shown on the first page. It is a three-amplifier device which provides all the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found in integrated circuit instrumentation amplifiers.

The input section (A1 and A2) incorporates high performance, low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input impedance ($10^{10}\Omega$) desirable in the instrumentation amplifier function. The offset voltage and offset voltage versus temperature is low due to the monolithic design and improved even further by the state-of-the-art laser-trimming techniques.

The output section (A3) is connected in a unity-gain difference amplifier configuration. A critical part of this stage is the matching of the four 10kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain excellent common-mode rejection. (The 106dB minimum at 60Hz for gains greater than 100V/V is a significant improvement compared to most other integrated circuit instrumentation amplifiers.)

All of the internal resistors are compatible thin-film nichrome formed with the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability of trimmed resistors and simultaneous achievement of excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA101 is operated over wide temperature ranges.

USING THE INA101

Figure 2 shows the simplest configuration of the INA101. The gain is set by the external resistor, R_G, with a gain equation of $G = 1 + (40K/R_G)$. The reference and TCR of R_G contribute directly to the gain accuracy and drift.

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For gains greater than unity, resistor R_G is connected externally between pins 1 and 4. At high gains where the value of R_G becomes small, additional resistance (i.e., relays, sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect.

The optional offset null capability is shown in Figure 2. The adjustment affects only the input stage component of the offset voltage. Thus, the null condition will be disturbed when the gain is changed. Also, the input drift will be affected by approximately $0.3\mu V/°C$ per $100\mu V$ of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset. Output offsetting can be accomplished in Figure 3 by applying a voltage to Common (pin 7) through a buffer amplifier. This limits the resistance in series with pin 7 to minimize CMR error. Resistance above 0.1Ω will cause the common-mode rejection to fall below 106dB. Be certain to keep this resistance low.

It is important to not exceed the input amplifiers' dynamic range. The amplified differential input signal and its associated common-mode voltage should not cause the output of A_1 or A_2 to exceed approximately ±10V or nonlinear operation will result.

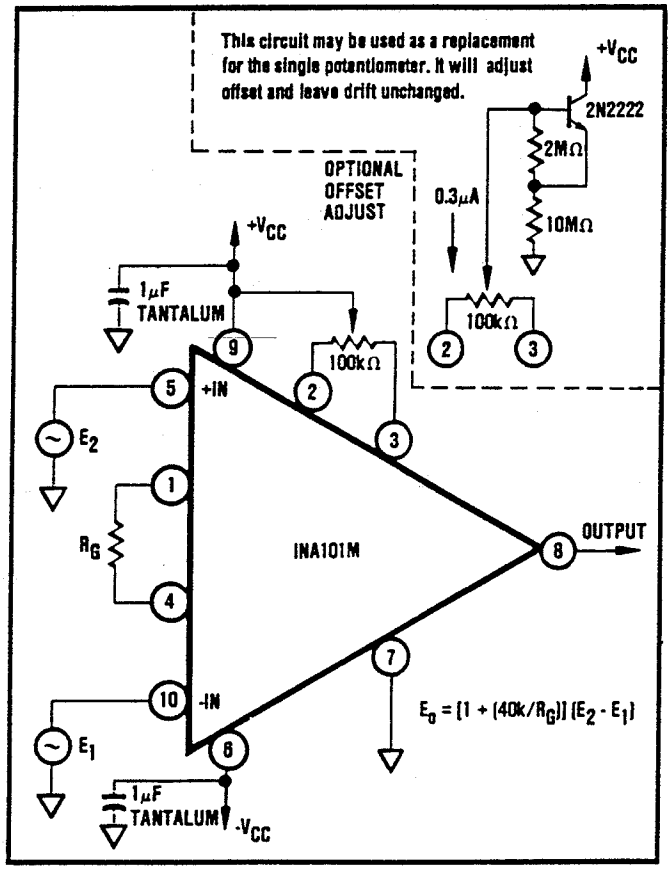


FIGURE 2. Basic Circuit Connection for the INA101 Including Optional Input Offset Null Potentiometer.

BASIC CIRCUIT CONNECTION

The basic circuit connection for the INA101 is shown in Figure 2. The output voltage is a function of the differential input voltage times the gain.

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is frequently desirable to null the input component o offset (Figure 2) and occasionally that of the outpu (Figure 3). The quality of the potentiometer will affect th

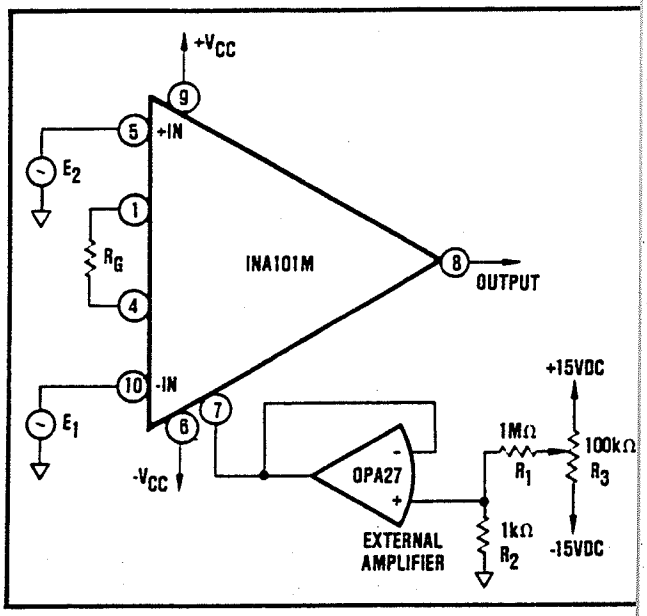


FIGURE 3. Optional Output Offset Nulling or Offsetting Using External Amplifier (Low Impedance to Pin 7).

results, therefore, choose one with good temperature an mechanical-resistance stability. The procedure is a follows:

1. Set $E_1 = E_2 = 0V$ (be sure a good ground return pat exists to the input).
2. Set the gain to the desired value by choosing R_G.
3. Adjust to 100kΩ potentiometer in Figure 2 until th output reads 0V ±1mV or desired setting. Note tha the offset will change when the gain is changed. If th output component of offset is to be removed or if it i desired to establish an intentional offset, adjust th 100kΩ potentiometer in Figure 3 until the outpu reads 0V ±1mV or desired setting. Note that the offse will not change with gain, but be sure to use a stabl external amplifier with good DC characteristics. Th range of adjustment is ±15mV as shown. For large ranges change the ratio of R_1 to R_2.

TYPICAL APPLICATIONS

Many applications of instrumentation amplifiers involv the amplification of low level differential signals fron bridges and transducers such as strain gages, thermo couples, and RTD's. Some of the important parameter include common-mode rejection (differential cancellatio of common-mode offset and noise, see Figure 1), inpu impedance, offset voltage and drift, gain accuracy linearity, and noise. The INA101 accomplishes all o these with high precision.

Figures 4 through 9 show some typical application circuits.

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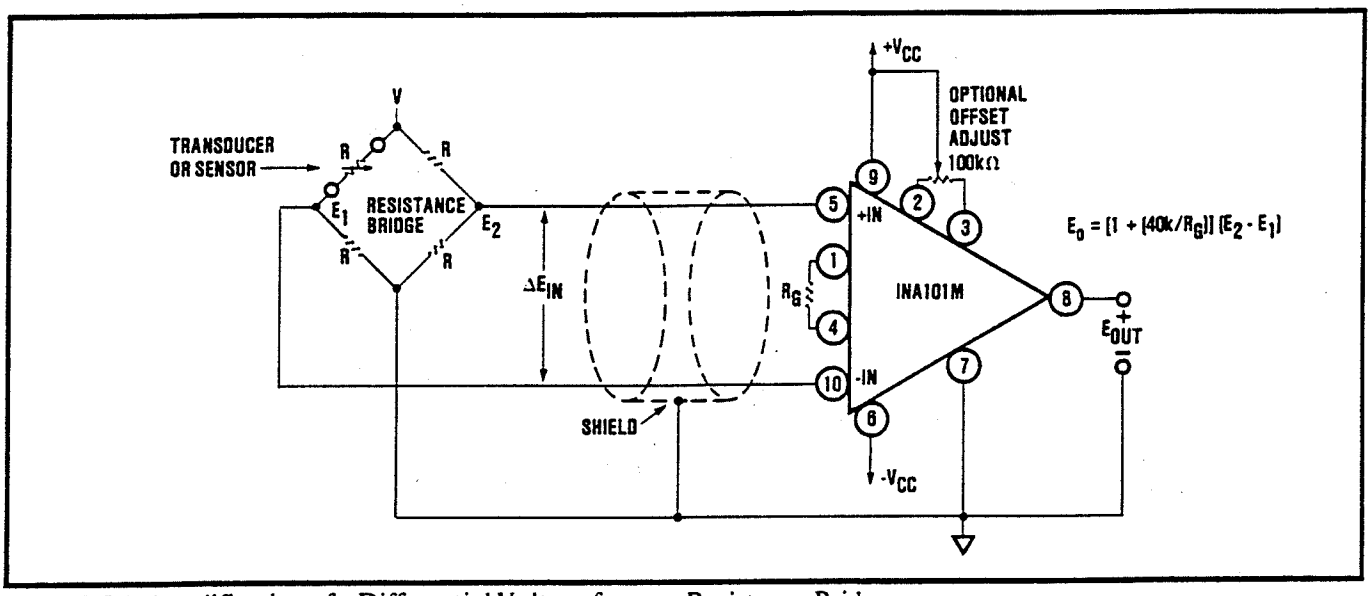


FIGURE 4. Amplification of a Differential Voltage from a Resistance Bridge.

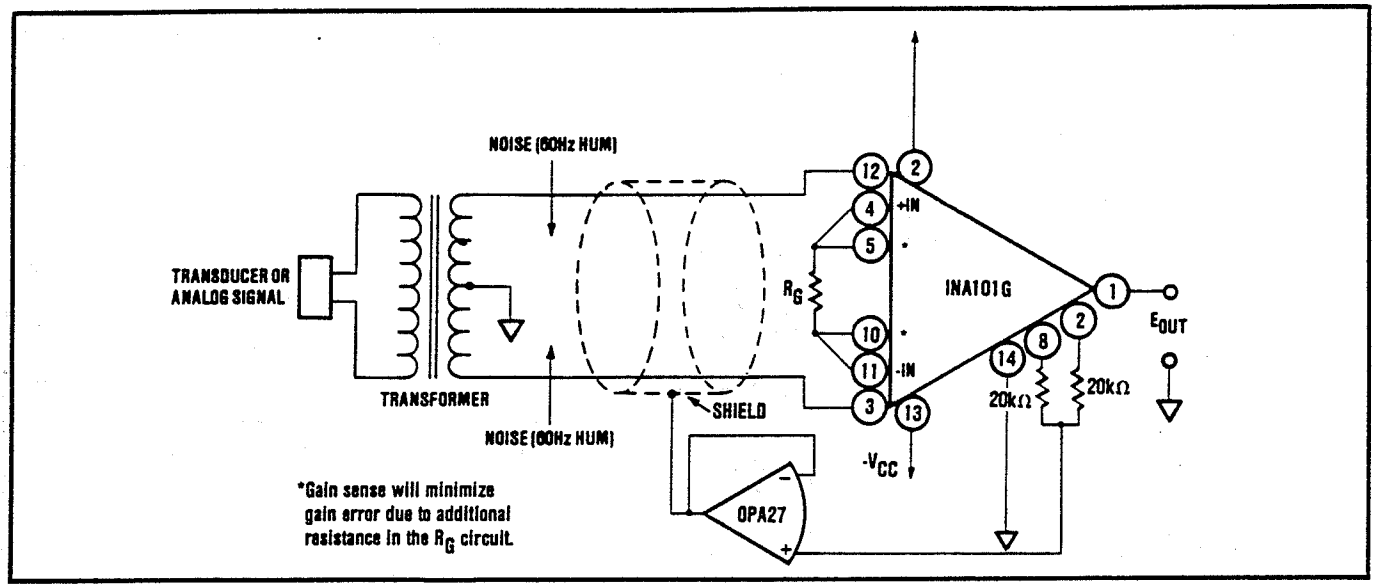


FIGURE 5. Amplification of a Transformer Coupled Analog Signal.

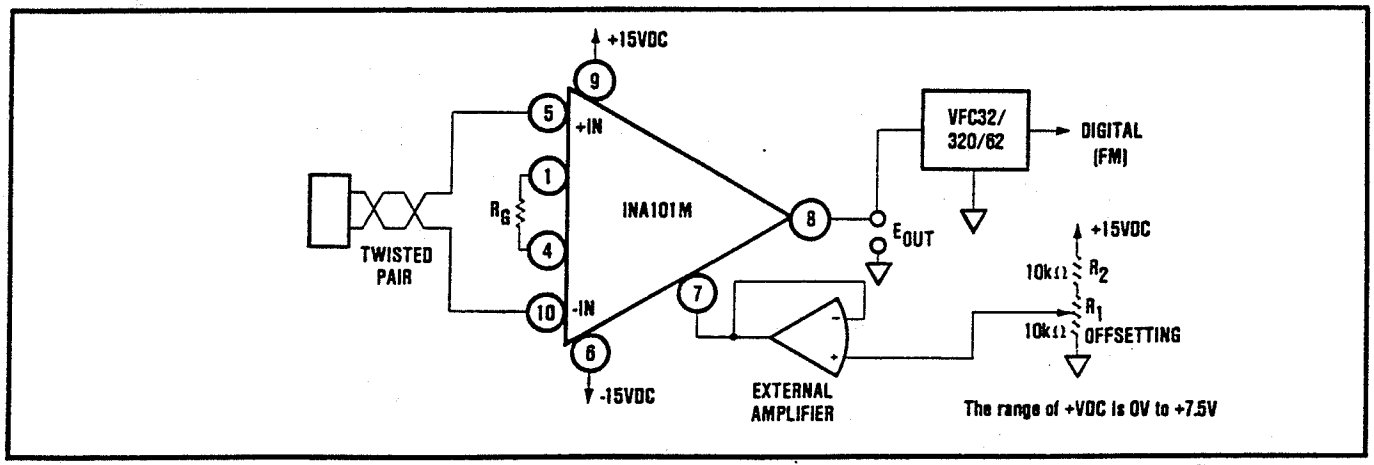


FIGURE 6. Output Offsetting Used to Introduce a DC Voltage for Use with a Voltage-to-Frequency Converter.

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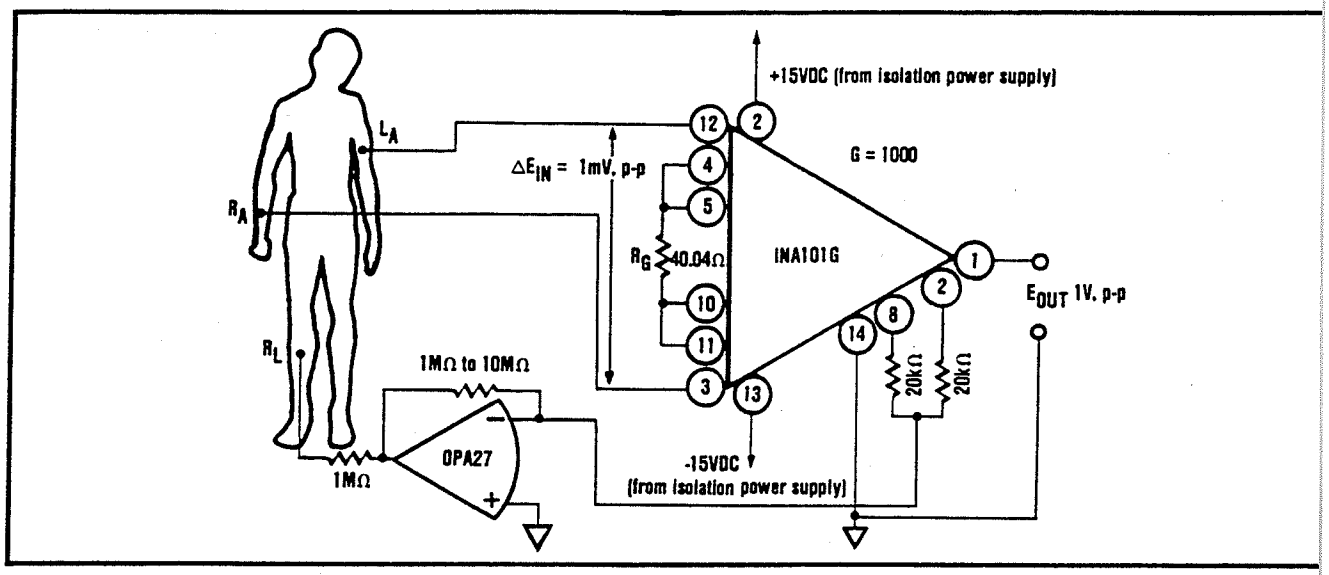


FIGURE 7. ECG Amplifier or Recorder Preamp for Biological Signals.

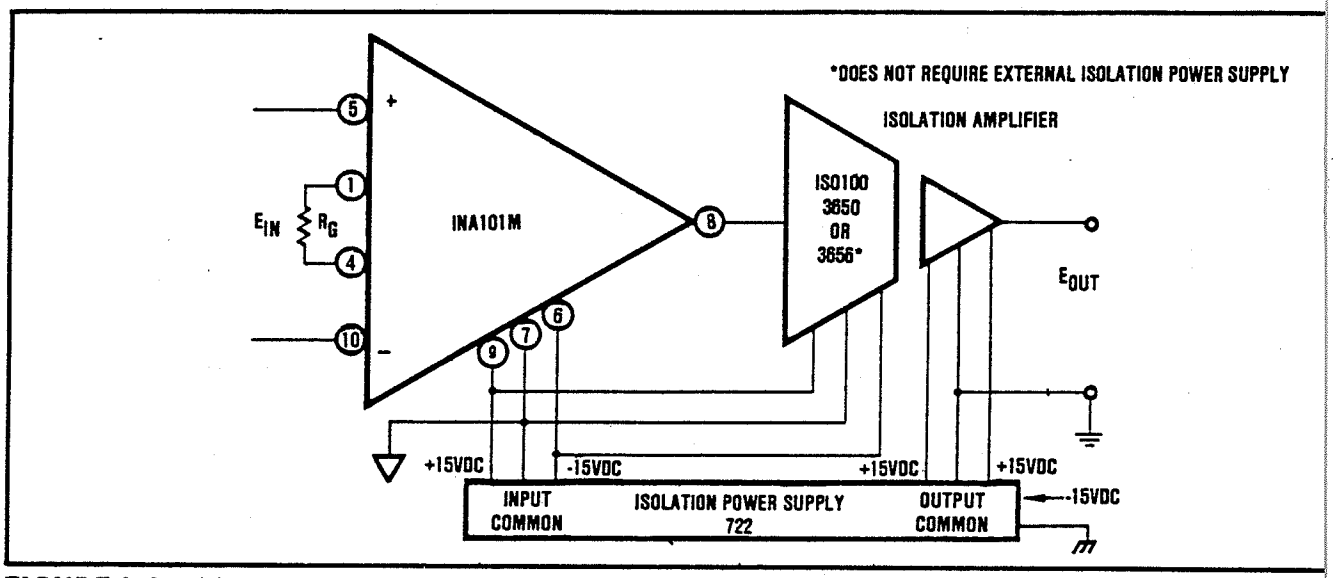


FIGURE 8. Precision Isolated Instrumentation Amplifier.

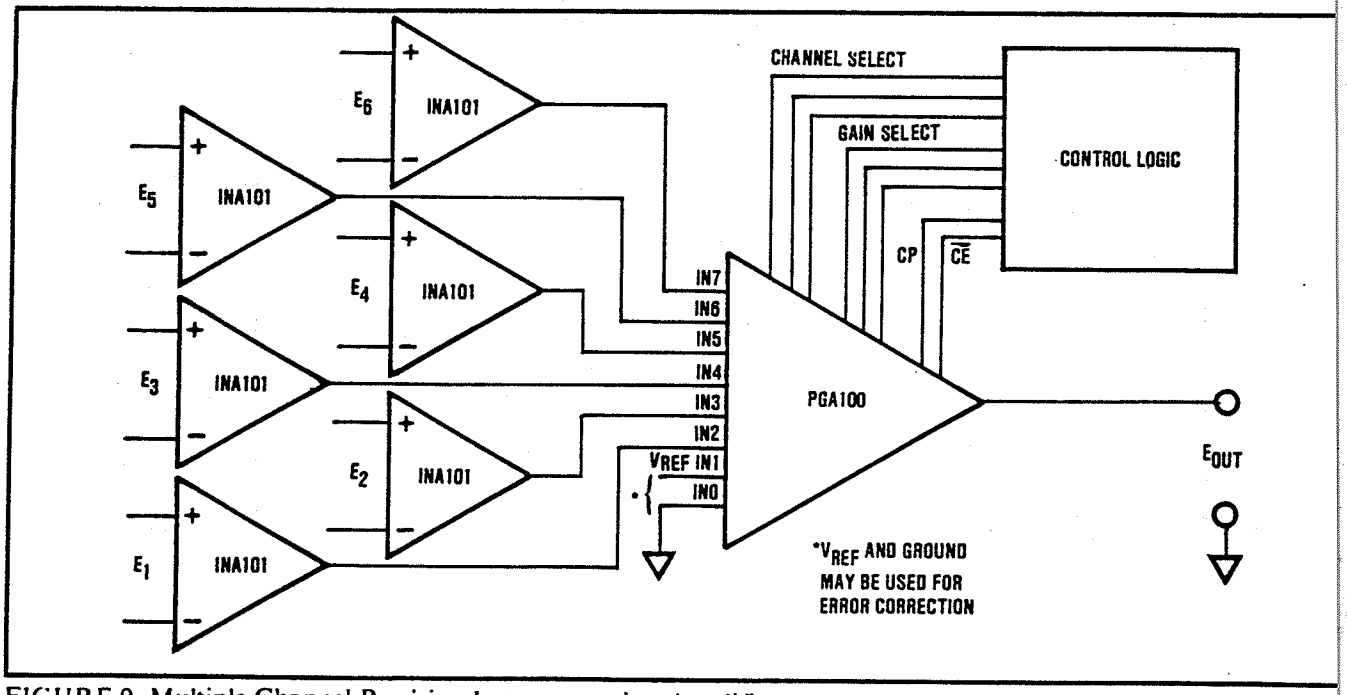


FIGURE 9. Multiple Channel Precision Instrumentation Amplifier.

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APPENDIX A

VMEbus BACKPLANE CONNECTORS AND VME BOARD CONNECTORS

INTRODUCTION

This appendix identifies the VMEbus backplane J1/P1 connector pin assignments, and which ones are used on the MPV901 Series. The following table lists the pin assignments by pin number order. (The connector consists of three rows of pins labeled rows A, B, and C.)

J1/P1 Pin Assignments

PIN NUMBER	ROW A SIGNAL MNEMONIC		ROW B SIGNAL MNEMONIC		ROW C SIGNAL MNEMONIC	
1	D00		BBSY*	(1)	D08	
2	D01		BCLR*	(1)	D09	
3	D02		ACFAIL*	(1)	D10	
4	D03		BGOIN*	(2)	D11	
5	D04		BG0OUT*	(2)	D12	
6	D05		BG1IN*	(3)	D13	
7	D06		BG1OUT*	(3)	D14	
8	D07		BG2IN*	(4)	D15	
9	GND		BG2OUT*	(4)	GND	
10	SYSCLK	(1)	BG3IN*	(5)	SYSFAIL*	(1)
11	GND		BG3OUT*	(5)	BERR*	(1)
12	DS1*		BRO*	(1)	SYSRESET*	
13	DSO*		BR1*	(1)	LWORD*	
14	WRITE*		BR2*	(1)	AM5	
15	GND		BR3*	(1)	A23	
16	DTACK*		AMO		A22	
17	GND		AM1		A21	
18	AS*		AM2		A20	
19	GND		AM3		A19	
20	IACK*		GND		A18	
21	IACKIN*		SERCLK	(1)	A17	
22	IACKOUT*		SERDAT	(1)	A16	
23	AM4		GND		A15	
24	A07		IRQ7*		A14	
25	A06		IRQ6*		A13	
26	A05		IRQ5*		A12	
27	A04		IRQ4*		A11	
28	A03		IRQ3*		A10	
29	A02		IRQ2*		A09	
30	A01		IRQ1*		A08	
31	-12V	(1)	+5V STDBY	(1)	+12V	(1)
32	+5V		+5V		+5V	

NOTE:

(1) Indicates signals used by MPV901 Series and not connected on board.

(2) Signals connected together on Board MPV901 Series

(3) Signals connected together on Board MPV901 Series

(4) Signals connected together on Board MPV901 Series

(5) Signals connected together on Board MPV901 Series

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