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PENTLAND SYSTEMS LIMITED

OPERATING MANUAL

MPV905

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MPV905 OPERATING MANUAL

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CHANGE HISTORY

CN No.	240	120	147	805	10967		
DATE	MAR'85	JUN'86	NOV'86	JUL'87	SEP'90		
REVISION	1.0	1.1	-	1.A	1.B		

**** THIS MANUAL APPLIES TO THE MPV905 - Rev 1 ONLY ****

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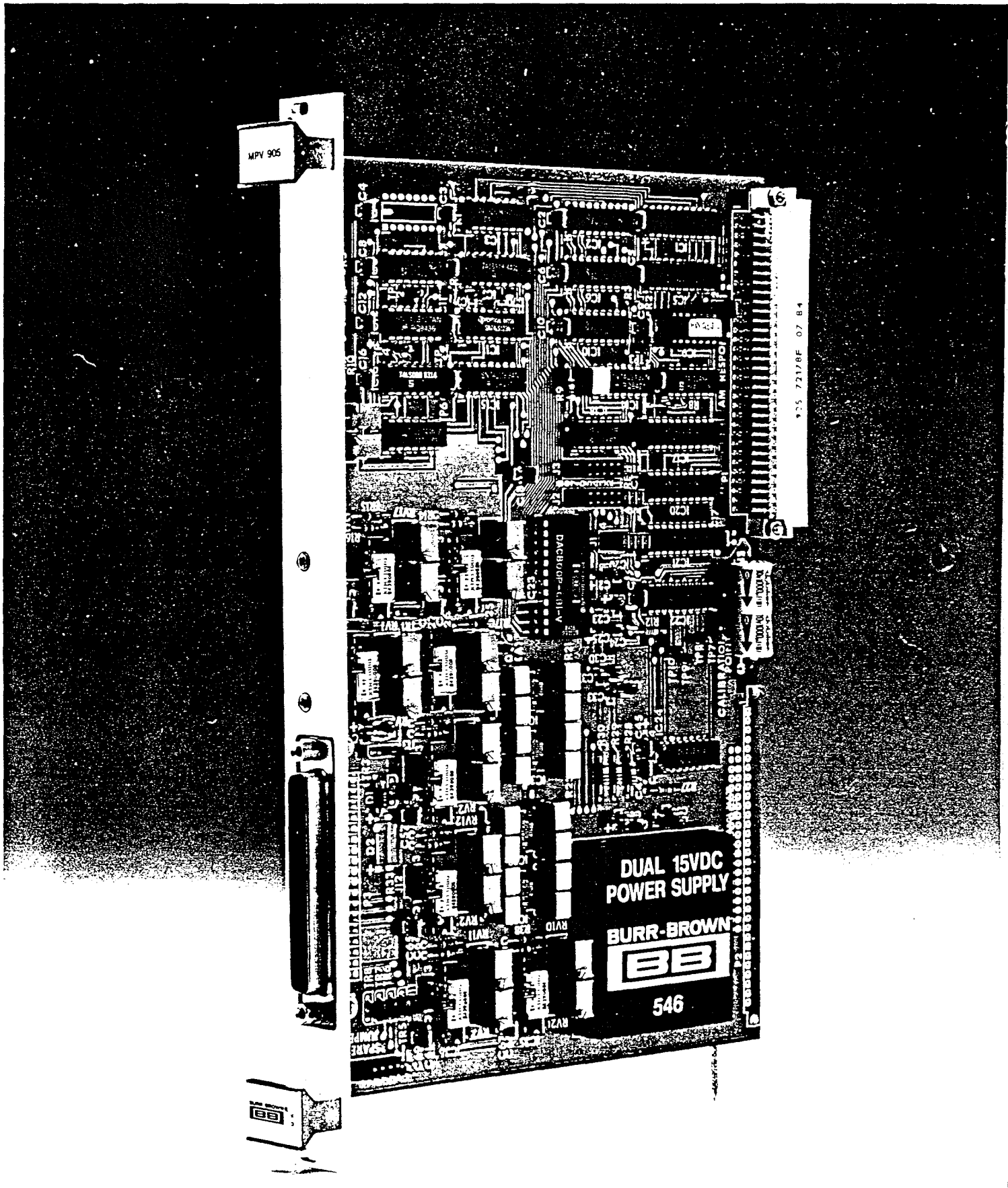
6.5 Circuit Diagram

Appendix A - VMEbus Backplane Connectors and VME Board Connectors

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Figure 1.1 MPV905



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Chapter 1 - GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, installation instructions, operating instructions, functional description and applications software examples for the MPV905 analog output board (current source).

1.2 GENERAL DESCRIPTION

The MPV905 analog output board is electrically and mechanically compatible with, and interfaces directly to the VMEbus.

The features of the MPV905 include:-

- 8 current source output channels.
- 12 bit resolution.
- 3 output ranges covering standard industrial requirements.
- Address block selectable in 16 Mbyte memory space.

Dynamic analog outputs (using a single digital to analog converter to drive all 8 channels) allow the MPV905 to provide high channel density on a single board. This approach frees system space for other peripherals and minimizes per channel power requirement.

Digital output data for each channel is stored in on-board RAM and the corresponding analog output voltage of the DAC is stored in separate sample and hold circuits. These circuits are continually updated by refresh circuitry. A voltage to current converter on each channel then provides the current output.

The host CPU changes data in the on-board RAM, and therefore the output current, by a write operation to the appropriate channel. Glitch free operation is ensured as the refresh circuitry is disabled while new data is being written to the RAM. At power up, all outputs are set to minimum current output for the selected range.

Address and Address Modifier (AM) decoding are jumper programmable in the 16Mbyte memory space.

An on-board DC to DC converter powers the MPV905 from the +5V system supply, the current source outputs being powered from a user supply.

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1.3 SPECIFICATION

ELECTRICAL

Typical at +25°C and rated power supplies unless otherwise stated.

OUTPUT CHARACTERISTICS	
Number of Channels	8
Output Curent Ranges (Jumper Selectable)	0 to 20mA, 4 to 20mA, 5 to 25mA
Short Circuit Protection, Duration	Indefinite to Common
ACCURACY	
Total Error Max [1]	±0.05% FSR [2]
Linearity	±0.03% FSR
Gain Error	±0.6% FSR
Offset Error	±0.4% FSR
ACCURACY OVER TEMPERATURE	
Accuracy Drift	±60ppm of FSR/°C
TRANSFER CHARACTERISTICS	
Resolution	12 bits
Settling Time, max	
To 0.1% of FSR	3.5ms
To 0.01% of FSR	5.0ms
POWER REQUIREMENTS	
From VMEbus	+5V ±5% at 1.5A max
From user supply (Vcc)	13.5V to 40V at 250mA max
ENVIRONMENTAL	
Operating Temperature	0°C to + 60°C
Storage Temperature	-25°C to +85°C
Relative Humidity	5% to 90% noncondensing

[1] Gain and offset adjusted to zero.
[2] FSR means full scale range.

MECHANICAL

Compatible with double-height VMEbus card-racking systems.

Minimum card spacing 20.34mm (0.8") (VMEbus specification compatible).

One 37-pin 'D' type connector on board for analog outputs.

Use Cannon 'D' type connector part number DC37P/1A1N or equivalent.

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Chapter 2 - INSTALLATION INSTRUCTIONS

2.1 INTRODUCTION

This chapter provides installation instructions and an overview of the user selectable options on the MPV905.

2.2 PREPARING THE BOARD

This section describes the hardware preparation of the MPV905 prior to installation in a VMEbus system. Following the instructions described in this section will ensure that the board is configured as desired and will function as expected when installed.

MPV905 boards are factory calibrated and tested prior to shipment with jumpers in pre-determined positions.

Figure 2.1 indicates the physical position of the jumpers on the board.

Table 2.1 lists each jumper, its function and the factory set position.

A detailed description of each jumper is given in sections 2.2.1 through 2.2.3.

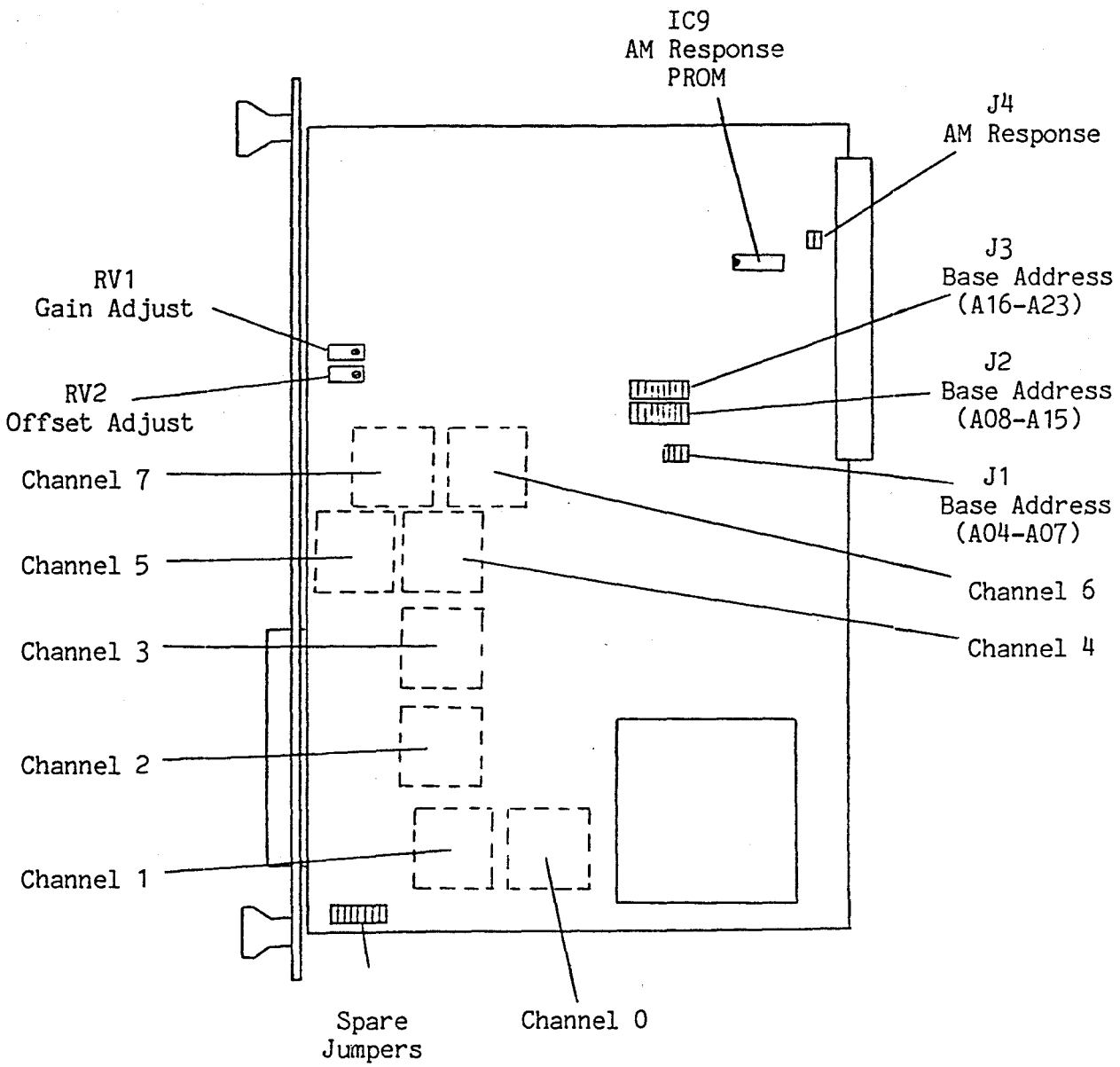
To alter the address modifier code response from the factory set values, the user must program the decoding PROM as described in section 2.2.3.1.

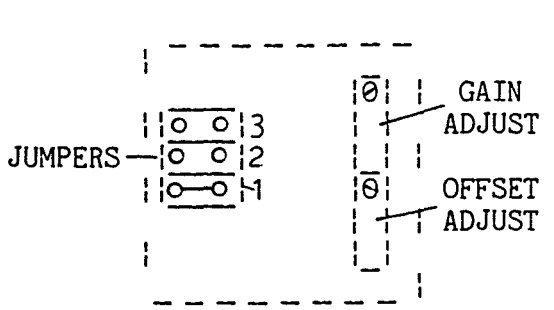
Before installation, the user should verify the configuration of the jumpers and, if necessary, alter the configuration to suit particular system requirements.

The board should not be installed or removed while power is applied to the VMEbus system.

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Figure 2.1
Position of Jumpers and Pots





CHANNEL	JUMPER	GAIN ADJUST	OFFSET ADJUST
0	J10	RV10	RV20
1	J11	RV11	RV21
2	J12	RV12	RV22
3	J13	RV13	RV23
4	J14	RV14	RV24
5	J15	RV15	RV25
6	J16	RV16	RV26
7	J17	RV17	RV27

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Table 2.1
Jumper Functions & Factory Settings

JUMPER DESIGNATION	FUNCTION	FACTORY SET CONDITON
J1	Base Address Selection (A04-A07)	4 3 2 1 
J2	Base Address Selection (A08-A15)	8 7 6 5 4 3 2 1 
J3	Base Address Selection (A16-A23)	8 7 6 5 4 3 2 1 
J4	AM Code Response	2 1 
J10-J17	Output Range Selection	3 2 1 

 Jumper Inserted

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2.2.1 Base Address Selection

The base address of the MPV905 can be set to any value by selecting the appropriate combination of positions on jumpers J1, J2 and J3. The factory set configuration is FFF800H. To change the sense of a bit simply change the jumper setting for that bit.

The MPV905 occupies 8 successive memory locations (word locations) within the system memory map.

Figure 2.2 shows the location and factory set configuration of the jumpers J1, J2 and J3. Table 2.2 lists the jumper positions that determine which base address is selected.

Figure 2.2
Base Address Selection Jumpers

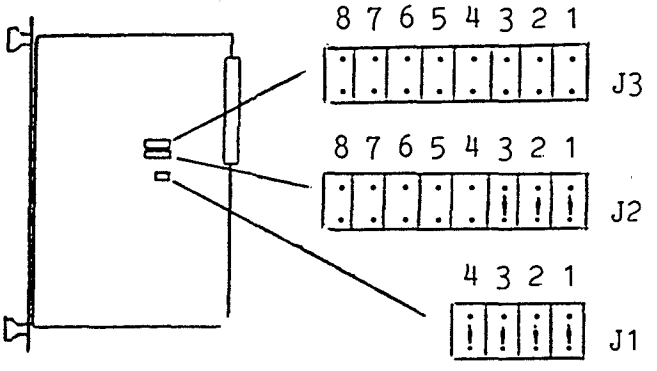


Table 2.2
Base Address Jumper Selection

ADDRESS LINE	FACTORY SET	JUMPER	
A04	0	J1 Position	1
A05	0		2
A06	0		3
A07	0		4
A08	0	J2 Position	1
A09	0		2
A10	0		3
A11	1		4
A12	1		5
A13	1		6
A14	1		7
A15	1		8
A16	1	J3 Position	1
A17	1		2
A18	1		3
A19	1		4
A20	1		5
A21	1		6
A22	1		7
A23	1		8

NOTE: 0 = Jumper Inserted 1 = Jumper Removed

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2.2.2 Output Current Range Selection

Jumpers J10 to J17 are used to set the output current range of the analog outputs.

Each output is set at the factory for 4 to 20mA operation (complementary straight binary coding).

When changing the output current range first remove all the jumper links, then insert those required for the desired range. Table 2.3 lists the available analog output ranges and the appropriate jumper settings.

Figure 2.3 shows the factory set condition for the jumpers of all channels. Refer to Figure 2.1 for the appropriate channel and corresponding jumper number.

Figure 2.3
Analog Output Range Selection Jumper

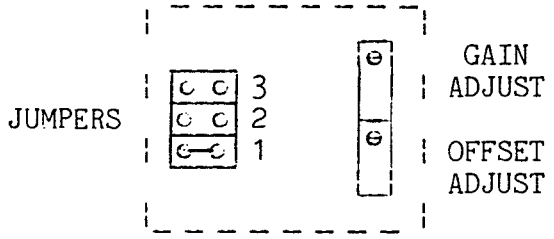


Table 2.3
Analog Output Range Selection

RANGE	JUMPER SELECTION	
	INSERT	REMOVE
0 to 20mA	2,3	1
* 4 to 20mA	1	2,3
5 to 25mA	1,3	2

* NOTE:- Factory Set Condition

2.2.3 Address Modifier Code Response

IC9 is a PROM, which in conjunction with jumper J4, positions 1 and 2, allows the response to address modifier codes to be varied to suit user requirements. The PROM/jumper combination offers the options shown in Table 2.4. The PROM program which enables this response is shown in the programming chart of Figure 2.5, at the end of this chapter.

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The positions of IC9, jumper J4 and its factory set condition are shown in Figure 2.4 below:-

Figure 2.4

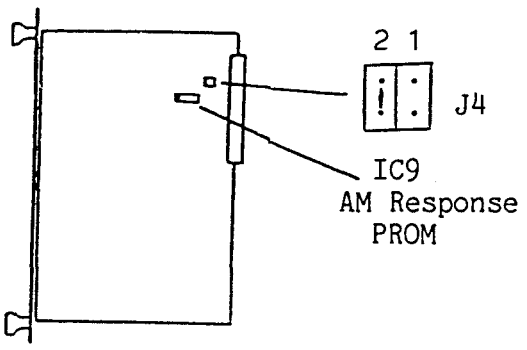


Table 2.4
Address/Address Modifier (AM) Response

	J4 Position 2	J4 Position 1	AM CODES	ADDRESS DECODING
1	Insert	Insert	N/A	A01-A15
* 2	Insert	Remove	N/A	A01-A23
3	Remove	Remove	3D, 39	A01-A23

* NOTE :- Factory set condition

A new PROM can be programmed to provide an alternative AM code response. The PROM is a 256 x 4 bit open-collector 82S126 type. The following section explains the interaction between jumper J4 and the codes stored in the PROM. An understanding of this section should allow the user to select the correct jumper/PROM code combination for a given response.

A list of VMEbus address modifier codes is given in section 6.3.

2.2.3.1 Programming the PROM

There are three allowable combinations of the J4 jumper links. These combinations are given in Table 2.4 and are referred to as (1), (2), (3). It is intended that combinations (1) and (2) be reserved for the responses detailed in Table 2.5, ie, short addressing with no AM codes and standard addressing with no AM codes respectively.

Combination (3) however, (both links removed), in conjunction with the information stored in the PROM, is designed to allow the response to address/AM codes to be modified, to suit system requirements, as shown in Table 2.5. Setting the two most significant data bits (D3 and D2) to a low level allows responses (1) and (2) as shown in Table 2.5. With both jumper links removed it is the setting of data bits D0 and D1 which determines the response.

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The following section (2.2.3.2) illustrates the method to be used when programming the PROM to produce a given response.

Table 2.5
Address/AM Response Options with Jumper Links Removed

AM CODE NOTE (1)	DATA BIT D3 D2 D1 D0	RESPONSE
XY	0 0 0 0	Short addressing with AM
XY	0 0 0 1	Short addressing with AM
XY	0 0 1 0	Standard addressing with AM
XY	0 0 1 1	No response to address/AM

NOTE: The AM code indicated as XY can take any of the possible values defined in the VMEbus specification Revision B. (See Section C).

2.2.3.2 Programming Examples

The Factory Response

Referring to Table 2.4, the programming of the PROM to give the factory set response is as follows.

1. Decide upon STANDARD or SHORT addressing - STANDARD (ie, A01-A23 decoded)

2. Decide upon AM codes to which the board will respond - 3D, 39.

3. Refer to Table 2.5 and under "response" heading look for "Standard addressing with AM". The data to be stored at the relevant memory addresses can then be read from the table (in this case 0010 (02H)).

4. Place the code obtained in (3), (ie 02H), at memory locations 3D and 39.

5. Refer to Table 2.5 and under "response" heading look for "No response to address/AM". The data to be stored at the relevant memory addresses, (in this case all locations other than 3D and 39), can then be read from the table, (in this case 0011 (03H)).

6. Place the code obtained in (5), (ie, 03H), at all memory locations other than 3D and 39.

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Short Addressing With AM

Assume that the following response is desired - Short Address decoding, (ie, A01 -A15 decoded) and AM codes 2D and 29* to be responded to. The following steps would yield the data to be placed in the PROM.

1. Addressing mode - SHORT.

2. Code response - 2D and 29.

3. Refer to Table 2.5 and under "response" heading look for "Short addressing with AM" (Note - there are two entries under this heading). The data to be stored at the relevant memory address can then be read from the table, (in this there is a choice of two codes - 0000 (00H) or 0001 (01H)).

4. Place either of the codes obtained in (3), (ie, 00H or 01H), at memory locations 2D and 29.

5. Refer to table 2.5 and under "response" heading look for "No response to address/AM". The data to be stored at the relevant memory addresses (in this case all locations other than 2D and 29), can then be read from the table, (in this case 03H).

6. Place the code obtained in (5), (ie, 03H) at all memory locations other than 2D and 29.

Similar reasoning applies to any other combination of address/AM response.

*Any number and combination of AM codes may be catered for.

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Chapter 3 - OPERATING INSTRUCTIONS

3.1 INTRODUCTION

This chapter provides the necessary information to allow the use of the MPV905 in a VMEbus system.

3.1.1 Jumper Setting Checklist

Before plugging the board into a VMEsystem and applying power, check, to ensure proper system operation, that the following options have been correctly set.

1. Base Address.
   Has the Base Address of the board been set to suit system requirements? (Section 2.2.1)

2. Address Modifier Response.
   Has Address Modifier Response been correctly set? (Section 2.2.3)

3. Output Range.
   Has the correct current output range been selected? (Section 2.2.2)

3.2 OPERATING PROCEDURE

The board is shipped from the factory in a calibrated condition and ready for use. Installation only requires plugging the card into an empty slot in the VMEbus card cage and wiring the analog connector. However, the board can be adapted to suit user requirements therefore, some features of the board are jumper selectable. These features are covered in chapter 2 which should be referred to before using the board or if a configuration other than the factory set condition is desired.

3.2.1 Programming

The board is programmed as 8 successive memory locations (word locations), jumper selectable within the 16 Mbyte address range, in 8 word blocks, commencing at address 000000H. The analog output has a resolution of 12-bits and therefore word accesses are required for each channel.

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3.2.1.1 Address Map (Memory Map)

The address map (memory map) for the MPV905 board is shown in Figure 3.1. The base address is jumper selectable. (Section 2.2.1)

Output data (i.e. data to set an analog output to a particular value) is transferred to the board from the CPU with MOVE instructions to the appropriate addresses. 8 consecutive addresses are used, starting from the base address XXXXX0, (the X-states are selected as previously described). As each operation is a word access, word addressing must be used (even addresses only).

NOTE : A read operation to a channel results in the channel being reset to the lowest current output in the selected range.

Figure 3.1
MPV905 Address (Memory) Map

Factory Set Address	WRITE D15 ... D11 ... D0	READ D15 ... D11 ... D0
FFF800	OUT0	RESET OUT0
FFF802	OUT1	RESET OUT1
FFF804	OUT2	RESET OUT2
.	.	.
.	.	.
.	.	.
.	.	.
.		
FFF80E	OUT7	RESET OUT7

3.2.2 CPU Instructions

The CPU transfers data to the MPV905 by using MOVE instructions, using the addresses and data lines shown in the address (memory) map of Figure 3.1. These instructions are described in the following list. The selected base address of the board is XXXXX0 (factory set to FFF800H). The CPU register Dn is used as the data register (and may be any of the allowable registers within the CPU).

MOVE.W Dn,FFF800 - This instruction moves the contents of data register Dn, within the CPU, to analog output OUTØ.

MOVE.W Dn,FFF802 - This instruction moves the contents of data register Dn, within the CPU, to analog output OUT1.

MOVE.W Dn,FFF80E - This instruction moves the contents of data register Dn, within the CPU, to analog output OUT7.

This illustrates the procedure for transferring data to the MPV905 to allow each output to be individually set.

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3.2.3 Analog Output Section

3.2.3.1 Analog Output Current and Converter Input Codes

The digital input value of a selected output is converted to a current. The digital to analog converter gives an output coding scheme of complementary straight binary.

Table 3.1 illustrates the full-scale negative, mid-scale and full-scale positive output currents for the three output ranges with the corresponding digital input codes of the digital to analog converter and the value of the least significant bit (LSB).

Figure 3.2 shows, in graphical form, the relationship between the digital input code and the output current.

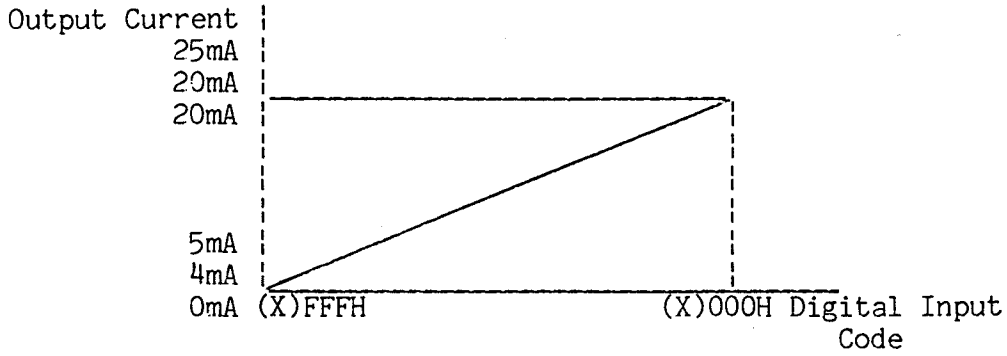
e.g. In Table 3.2 a digital input code of (X)FFFH corresponds to an output current of 4mA in the range 4 to 20mA. In the same range a value of (X)000H will produce an output current of 19.996mA.

Table 3.1
Complementary Straight Binary

OUTPUT CODE	SELECTED RANGE	NEGATIVE FULL SCALE (X)FFFH	MIDSCALE (X)7FFH	POSITIVE FULL SCALE (X)000H	RESOLUTION
	0 to 20mA	0.00mA	+10.0mA	+19.995mA	4.88uA
	4 to 20mA	4.00mA	+12.0mA	+19.996mA	3.91uA
	5 to 25mA	5.00mA	+15.0mA	+24.995mA	4.88uA

NOTE:- X indicates don't care states

Figure 3.2
Complementary Straight Binary



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3.2.3.2 Calculating Output Current From Input Code

The analog output current may be calculated from the input code, written by the CPU, as shown below.

$$\text{Output Current} = \text{Negative Full Scale} + (4095\text{-code}) \times \frac{\text{range}}{4096}$$

where,

range = theoretical range of values in the selected output range.
code = DECIMAL value of code placed in CPU register and written to output (with four MSB's set to zero).

NOTE: The code consists of 12 significant bits; bits D00-D11. In the CPU register bits D12 to D15 can be set to any value before data is written to the output. However, before using the following formula, bits D12 to D15 must be set to 0 for all input codes.

e.g. consider an output range of 0 to 20mA and a code of 7FFH. Then,

range = 20mA

code = Decimal value of 7FFH
= 2047

$$\text{Output Current} = 0\text{mA} + (4095 - 2047) \times \frac{20}{4096}$$

$$= 10\text{mA}$$

Referring to Table 3.1 it can be seen that for a code of 7FFH, the expected voltage is 10mA.

3.2.3.3 Output Range Selection

The analog outputs are factory set for a range of 4 to 20mA. Other output ranges can be selected as described in section 2.2.2.

3.2.3.4 Output Check

Static checks of the analog outputs can be performed by loading the memory locations with output data words. The base address XXXXX0 is factory set to FFF800H (refer to address map Figure 3.1). The ideal values for positive and negative full scale are shown in Tables 3.1 and 3.2. The most significant four bits of the data word (D11-D15) are don't care states.

A program which performs a simple dynamic check of the analog outputs is listed in section 5.3.

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3.2.4 Output Calibration

Each of the analog outputs can be calibrated by means of a gain and offset adjustment as outlined below:-

Install the MPV905 in a VMEbus system and allow it to reach thermal equilibrium (about 20 minutes under power) before commencing the procedure. The positions of the calibration potentiometers are shown in Figure 2.1.

Since multimeters are generally more capable of accurate voltage than current measurement, it is recommended that the scheme shown in Figure 3.3 be adopted during the calibration procedure. This involves the use of a resistive load on each output of the MPV905 and the use of a multimeter to measure the voltage developed across the resistor in response to the current passing through it. The recommended resistance value is 500 Ohm +/-0.01% , 0.25W , T.C. of resistance 10 ppm per degree C or better.

1. Connect a DVM (5 1/2 digit) between the appropriate output being calibrated and a return on the front panel 'D' type connector.

2. Load the appropriate memory location with the code XFFFH. (XFFEH if 0 to 20 mA range).

3. Adjust the appropriate offset control until the DVM reads, for the range of interest, the value indicated in Table 3.3

4. Load the appropriate memory location with the code X000H.

5. Adjust the appropriate gain control until the DVM reads, for the range of interest, the value indicated in Table 3.3

6. Return to step 2 and repeat through 6 until the desired voltages are obtained.

Calibration is now complete.

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Figure 3.3
Recommended Calibration Method

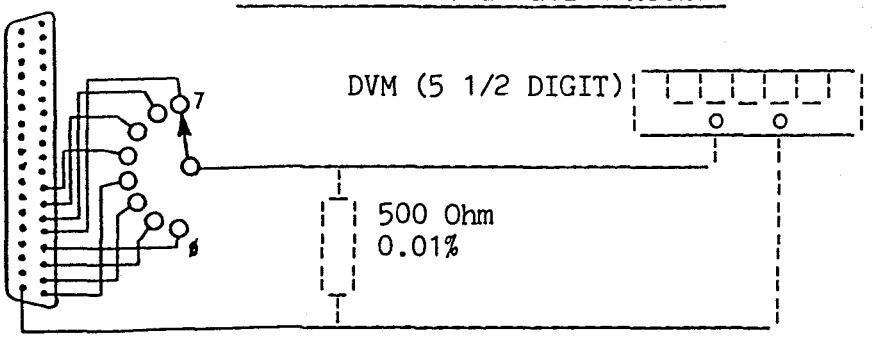


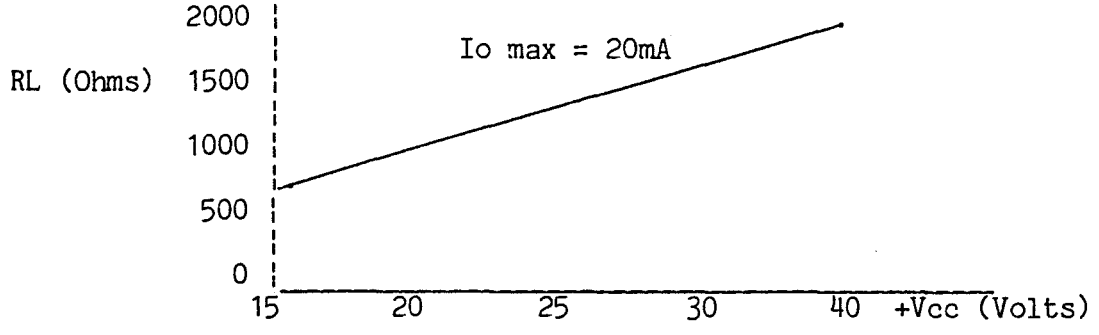
Table 3.3
Calibration Values

RANGE	DATA (X)FFFH	DATA (X)FFEH	DATA (X)000H	1 LSB
0 to 20mA	-	2.44mV ±0.5mV	9.9976V ±1.0mV	4.88uA
4 to 20mA	2V ±1mV	-	9.9980V ±1.0mV	3.91uA
5 to 25mA	2.5V ±1mV	-	12.498V ±1.0mV	4.88uA

3.2.5 Output Loading

The maximum load resistance into which the MPV905 will source current is dependent upon the value of the user defined external power source. Figure 3.4 shows the relationship between load resistance and power supply (Vcc on the front panel 'D' type connector).

Figure 3.4
Maximum RL vs Vcc

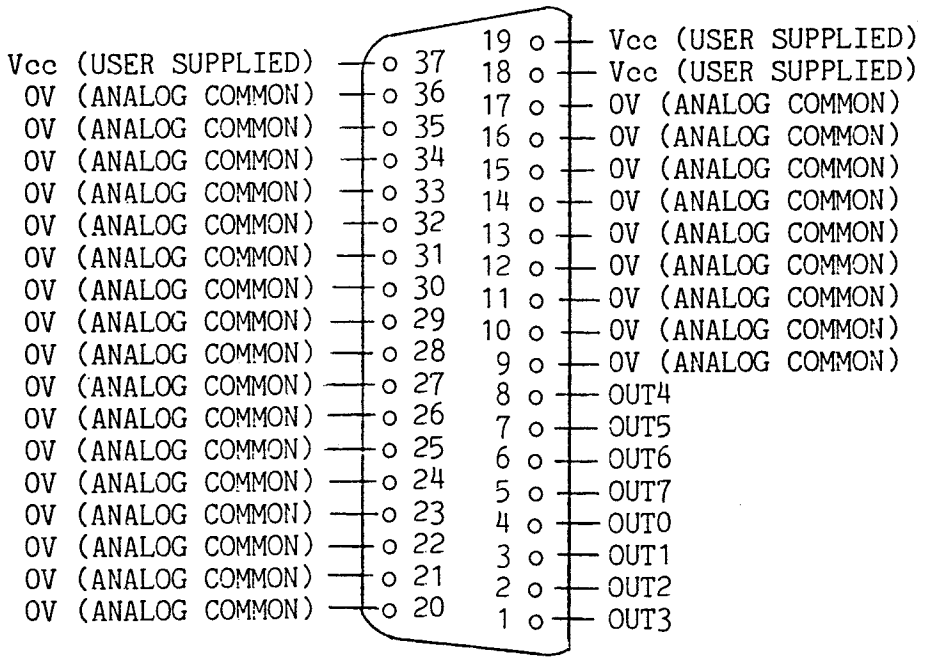


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3.3 Analog Connector

The analog front panel connector, P3, is a 37 way 'D' type socket (female). The mating connector should be a 37 way 'D' type plug (male). Use Cannon type DC37P/1A1N or equivalent.

'D' Type Connector Pinout



3.4 Factory Set Configuration

All boards are shipped from the factory ready for immediate use, however, they do have a number of user selectable options. These options and their factory set conditions, which have already been described, are summarized below:

BASE ADDRESS FFF800H
ADDRESS/AM RESPONSE ..... STANDARD ADDRESSING/ALL AM CODES
OUTPUT RANGE ..... 4 TO 20mA

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4.1 INTRODUCTION

This chapter is intended to provide a background to the theory of operation for the MPV905 8 Channel analog output board. It should be read while referring to the schematics, major component data sheets (Chapter 6), and where appropriate, other chapters in this manual.

4.2 GENERAL INFORMATION

The MPV905 is a 8 channel analog current source output board with 12 bit resolution which interfaces directly to the VMEbus. Figure 4.1 shows a block diagram of the board.

4.3 THEORY OF OPERATION

The design of the MPV905 board is based on a dynamic output approach. This uses a single digital to analog converter (DAC) to drive all 8 outputs. Digital data for each channel is stored in the on-board RAM while analog output data for each channel is stored in separate sample and hold circuits. The control and refresh circuitry contains a channel counter that selects, from RAM, the appropriate DAC input for the channel being updated and multiplexes the DAC output to the appropriate sample and hold circuit. Thus the output data is updated independently of the CPU.

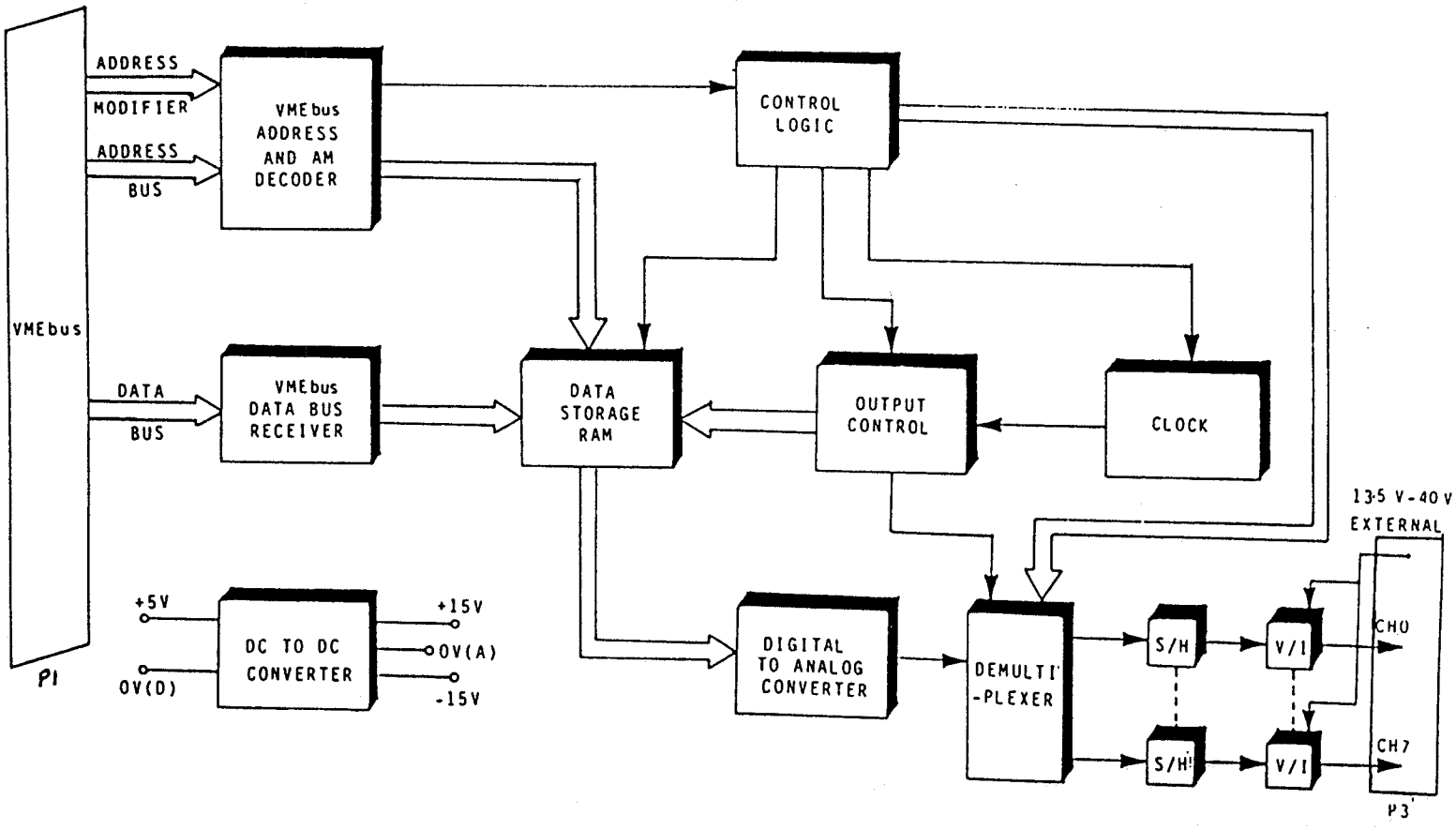
The CPU changes data in the on-board RAM by a write operation on data lines D00-D11, (D00 is the LSB), to the appropriate channel. When this occurs, the control logic disables the refresh circuitry to prevent output glitches and to allow the CPU to change the data stored in the on-board RAM.

4.3.1 Address/AM Decoder

The address decoding section consists of three eight bit magnitude comparators (IC17, IC20, and IC21). These devices monitor address bits A04 through A23 inclusive. The address modifier (AM) decoding is performed by the PROM (IC9). The operation of this section would be as follows:-

The user would insert the appropriate combination of jumper links at positions J1, J2 and J3 thus setting the base address of the board within the memory map. The jumper links at J4 (in combination with the program stored in the PROM IC9) would also be appropriately set to select the desired response to the AM codes.

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MPV 905 Block Diagram

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Upon initiation of a data transfer on the VMEbus, the levels on the address lines A04 through A23 inclusive are compared with the levels set at the jumper positions J1, J2 and J3. Only when every driven level exactly matches the corresponding set level, will the three comparator outputs ($\overline{P=Q}$) be driven to the active LOW level, indicating that the address placed on the bus matches the set address.

Similarly, with AM decoding, a recognisable AM code on bus lines AM0 through AM5 inclusive will result in the PROM outputs being driven to the active LOW level. Assuming that the transfer is neither an interrupt cycle nor a LONGWORD cycle, ($\overline{IACK}$ and $\overline{LWORD}$ are monitored to check this), then a HIGH level will appear at pin 8 of IC7. This HIGH level is an indication to subsequent control circuitry that the MPV905 should respond during the current transfer.

4.3.2 Memory Access

The data to be output is stored in the on-board RAM (IC2, IC6 and IC10) during a write cycle to the board. The memory is enabled to allow write operations to take place when the output of IC7 pin 8 is in the HIGH state. A HIGH level at this point clocks IC19, enabling bus buffers IC1 and IC5, thus allowing the data on the bus to be presented to the inputs of the RAM. Following this, the monostable (IC11 pin 1) is triggered and applies the write enable signal to the RAM thus latching (storing) the data present on the data lines D00 through D11. $\overline{DTACK}$ is then driven, through IC18, to indicate that data has been stored.

4.3.3 Timing and Control Logic

IC14, R9 and C14 form a 50kHz clock, the output of which is fed to a counter (IC15). The counter outputs are fed via IC22 to both the address inputs of the RAM and to the address input of the demultiplexer (IC24). The counter "counts" from 0 to 7 and resets. As it does so, it cycles around the values stored in RAM for each of the outputs. As each location is accessed, the stored data is applied to the input of the digital to analog converter and the output of the converter is switched through the multiplexer to the appropriate output device. This process continues without interruption until a new value is written to the board. During a data write operation the clock is disabled and the counter output is frozen at the current value. The address of the memory location to be updated is fed via IC22 to the RAM address lines allowing the appropriate location to be filled with new data. At the end of the transfer, the clock is restarted and the counter again cycles around the data stored in memory.

4.3.4 Analog Output

Each of the analog outputs is a combined filter and sample-and-hold device followed by a voltage to current converter. The filtering ensures that any glitches which occur during the switching process do not appear at the output.

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5.1 INTRODUCTION

This section is intended to assist the MPV905 user to quickly gain an understanding of the operation of the board using small, easily understood, applications programs.

The following two programs were written assuming that the board is still in its factory set condition and therefore the memory map in chapter 3, Figure 3.1 applies. The programs are written in Motorola MC68000 assembly language on a FORCE SYS68K system, and stored in RAM starting at location 2000H. Depending upon the type of assembler and monitor programs used, the following programs may require modification, further help can be supplied from the factory. Memory locations 2000H to 2F00H are assumed to be RAM locations. If the available user RAM is at some other location the address in line 1 should be modified accordingly.

5.2 Static Analog Output Check

This program provides a simple static check for the 8 analog outputs, by outputting the following currents from each channel as follows:

Channel 0 - 4 mA
Channel 1 - 6 mA
Channel 2 - 8 mA
Channel 3 - 10 mA
Channel 4 - 12 mA
Channel 5 - 14 mA
Channel 6 - 16 mA
Channel 7 - 18 mA

```
            ORG     @$2000;         Start Address of program storage.
BASEADD:    EQU     @$FFF800;       Address of Channel 0.
ENDADD:     EQU     #$FFF810;       Address of last Channel+2.
MINVAL:     EQU     #$0FFF;         Initial output value (4 mA).
STEP:       EQU     #$0200;         Output step size (2 mA).

            MOVE.W  MINVAL,D0;      Start with initial value in D0.
            LEA.L   BASEADD,A1;     CH0 loaded in address pointer A1.
LOOP:       MOVE.W  D0,(A1)+;        Output value and increment A1.
            SUB.W   STEP,D0;        5 mA added to output value in D0.
            CMPA.L  ENDADD,A1;      Have all channels been done?
            BNE.S   LOOP;           No... Then repeat.
            TRAP    #14;            Yes.. Then return to the monitor.
```


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5.3 Dynamic Analog Output Check

This program performs a simple dynamic check of all analog outputs. A ramp (sawtooth) waveform with amplitude plus and minus full scale and frequency approximately 30Hz will be produced at each output.

This program can be used to check correct operation of all channels.

```
            ORG     @$2000;         Start address of program storage.
BASEADD:    EQU     @$FFF800;       Address of channel 0.
ENDADD:     EQU     #$FFF810;       Address of channel 7+2.
MAXVAL:     EQU     #$0000;         Maximum output value.
MINVAL:     EQU     #$0FFF;         Minimum output value.
STEP:       EQU     #$0F;           Output step size.


START:      MOVE.W  MAXVAL,D0;      Start with maximum value in D0 and CH0
RAMPDOWN:   LEA.L   BASEADD,A0;     address in A0.
LOOP1:      MOVE.W  D0,(A0)+;       Output a value then increment the
                                    channel address in A0.
            CMPA.L  ENDADD,A0;      Have all channels been done?
            BNE.S   LOOP1;          No... The repeat.
            ADD.W   STEP,D0;        Yes.. Then next value.
            CMPI    MINVAL,D0;      Check for minimum output value and
            BLT     RAMPDOWN;       repeat if not done...
RAMPUP:     LEA.L   BASEADD,A0;     Else begin to ramp up with min value
LOOP2:      MOVE.W  D0,(A0)+;       in D0 and CH0 address in A0.
            CMPA.L  ENDADD,A0;      Have all channels been done?
            BNE.S   LOOP2;          No... Then repeat.
            SUB.W   STEP,D0;        Yes.. Then next value.
            CMPI    MAXVAL,D0;      Check for max output value and repeat
            BGT     RAMPUP;         if not done...
            JMP     START;          Else begin again.
```


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6.1 COMPONENTS LIST

COMPONENT DESIGNATION	DESCRIPTION
R1	Resistor Metal Oxide 27K 2% 0.25W
R2	Resistor Metal Oxide 2K2 10% 0.25W
R3	Resistor Metal Oxide 2K2 10% 0.25W
R4	Resistor Metal Oxide 4K7 2% 0.25W
R5	Resistor Metal Oxide 2K2 10% 0.25W
R6	Resistor Metal Oxide 2K2 10% 0.25W
R7	Resistor Metal Oxide 1M 10% 0.25W
R8	Resistor Metal Oxide 2K2 10% 0.25W
R9	Resistor Metal Oxide 910R 10% 0.25W
R10	Resistor Metal Oxide 2K2 10% 0.25W
R11	Resistor Carbon Film 6M8 10% 0.25W
R12	Resistor Metal Oxide 22R 2% 0.25W
R13	Resistor Metal Oxide 51K 2% 0.25W
R14	Resistor Metal Oxide 24R 2% 0.25W
R15	Resistor Metal Oxide 24R 2% 0.25W
R16	Resistor Metal Oxide 51K 2% 0.25W
R17	Resistor Metal Oxide 24R 2% 0.25W
R18	Resistor Metal Oxide 51K 2% 0.25W
R19	Resistor Metal Oxide 51K 2% 0.25W
R20	Resistor Metal Oxide 24R 2% 0.25W
R21	Resistor Metal Oxide 33K 2% 0.25W
R22	Resistor Metal Oxide 33K 2% 0.25W
R23	Resistor Metal Oxide 33K 2% 0.25W
R24	Resistor Metal Oxide 33K 2% 0.25W
R25	Resistor Metal Oxide 24R 2% 0.25W
R26	Resistor Metal Oxide 51K 2% 0.25W
R27	Resistor Metal Oxide 22R 2% 0.25W
R28	Resistor Metal Oxide 22R 2% 0.25W
R29	Resistor Metal Oxide 22R 2% 0.25W
R30	Resistor Metal Oxide 22R 2% 0.25W
R31	Resistor Metal Oxide 33K 2% 0.25W
R32	Resistor Metal Oxide 33K 2% 0.25W
R34	Resistor Metal Oxide 33K 2% 0.25W
R35	Resistor Metal Oxide 33K 2% 0.25W
R36	Resistor Metal Oxide 24R 2% 0.25W
R37	Resistor Metal Oxide 51K 2% 0.25W
R38	Resistor Metal Oxide 24R 2% 0.25W
R39	Resistor Metal Oxide 51K 2% 0.25W
R40	Resistor Metal Oxide 24R 2% 0.25W
R41	Resistor Metal Oxide 51K 2% 0.25W
RV1-RV18	Variable Resistor 100K 20 Turn Top Adjust

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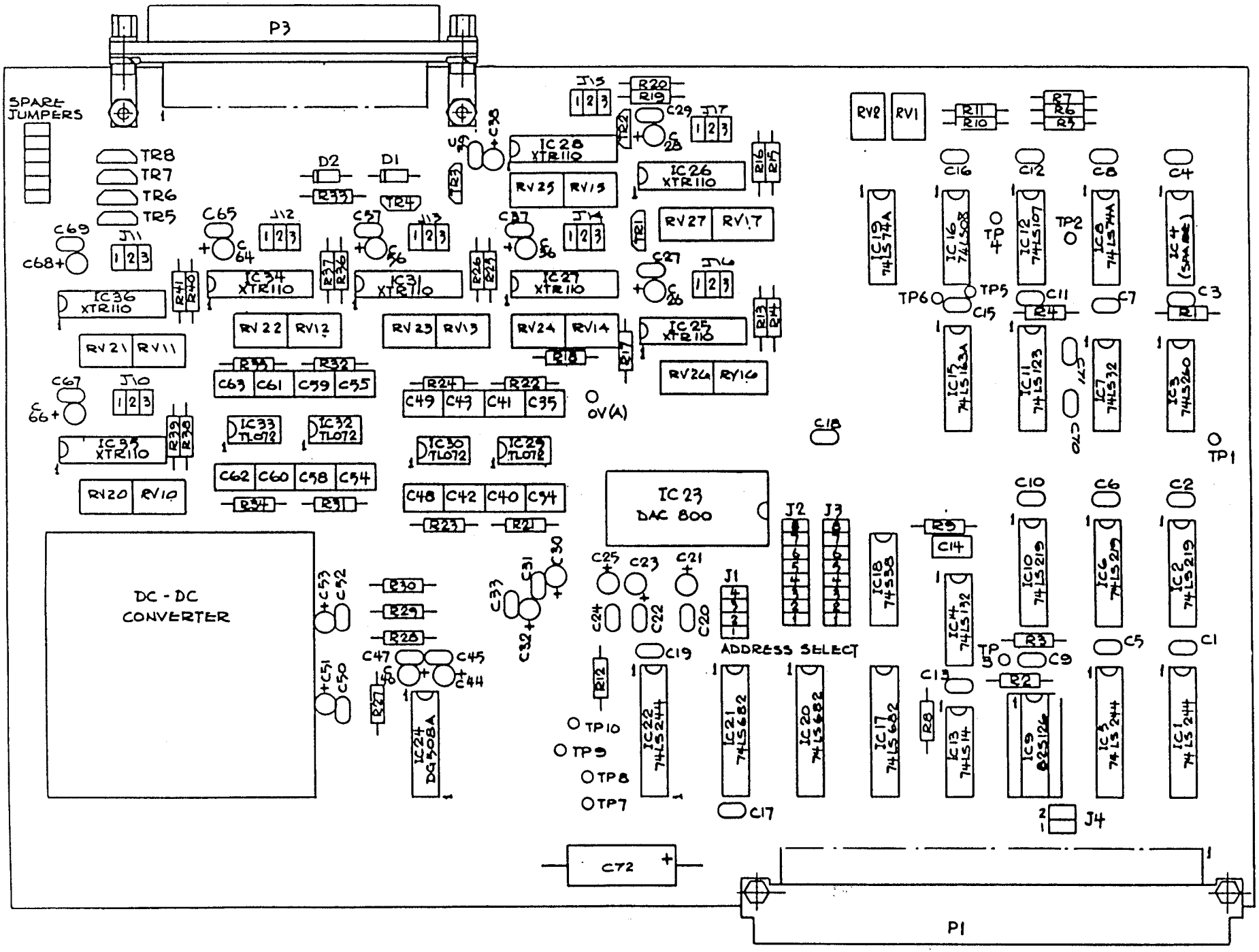
COMPONENT DESIGNATION	DESCRIPTION
C1-C13	Capacitor Ceramic Z5U 0.1uF 50V 20%
C14	Capacitor Polypropylene 0.01uF 63V 10%
C15-C20	Capacitor Ceramic Z5U 0.1uF 50V 20%
C21	Capacitor Tanatalum Tap 10uF 35V 20%
C22	Capacitor Ceramic Z5U 0.1uF 50V 20%
C23	Capacitor Tanatalum Tap 10uF 35V 20%
C24	Capacitor Ceramic Z5U 0.1uF 50V 20%
C25	Capacitor Tanatalum Tap 10uF 35V 20%
C26	Capacitor Tanatalum Tap 10uF 35V 20%
C27	Capacitor Ceramic Z5U 0.1uF 50V 20%
C28	Capacitor Tanatalum Tap 10uF 35V 20%
C29	Capacitor Ceramic Z5U 0.1uF 50V 20%
C30	Capacitor Tanatalum Tap 10uF 35V 20%
C31	Capacitor Ceramic Z5U 0.1uF 50V 20%
C32	Capacitor Tanatalum Tap 10uF 35V 20%
C33	Capacitor Ceramic Z5U 0.1uF 50V 20%
C34	Capacitor Polypropylene 68000pF 63V 10%
C35	Capacitor Polypropylene 68000pF 63V 10%
C36	Capacitor Tanatalum Tap 10uF 35V 20%
C37	Capacitor Ceramic Z5U 0.1uF 50V 20%
C38	Capacitor Tanatalum Tap 10uF 35V 20%
C39	Capacitor Ceramic Z5U 0.1uF 50V 20%
C40	Capacitor Polypropylene 68000pF 63V 10%
C41	Capacitor Polypropylene 68000pF 63V 10%
C42	Capacitor Polypropylene 68000pF 63V 10%
C43	Capacitor Polypropylene 68000pF 63V 10%
C44	Capacitor Tanatalum Tap 10uF 35V 20%
C45	Capacitor Ceramic Z5U 0.1uF 50V 20%
C46	Capacitor Tanatalum Tap 10uF 35V 20%
C47	Capacitor Ceramic Z5U 0.1uF 50V 20%
C48	Capacitor Polypropylene 68000pF 63V 10%
C49	Capacitor Polypropylene 68000pF 63V 10%
C50	Capacitor Ceramic Z5U 0.1uF 50V 20%
C51	Capacitor Tanatalum Tap 10uF 35V 20%
C52	Capacitor Ceramic Z5U 0.1uF 50V 20%
C53	Capacitor Tanatalum Tap 10uF 35V 20%
C54	Capacitor Polypropylene 68000pF 63V 10%
C55	Capacitor Polypropylene 68000pF 63V 10%
C56	Capacitor Tanatalum Tap 10uF 35V 20%
C57	Capacitor Ceramic Z5U 0.1uF 50V 20%
C58	Capacitor Polypropylene 68000pF 63V 10%
C59	Capacitor Polypropylene 68000pF 63V 10%
C60	Capacitor Polypropylene 68000pF 63V 10%
C61	Capacitor Polypropylene 68000pF 63V 10%
C62	Capacitor Polypropylene 68000pF 63V 10%
C63	Capacitor Polypropylene 68000pF 63V 10%
C64	Capacitor Tanatalum Tap 10uF 35V 20%
C65	Capacitor Ceramic Z5U 0.1uF 50V 20%
C66	Capacitor Tanatalum Tap 10uF 35V 20%
C67	Capacitor Ceramic Z5U 0.1uF 50V 20%

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COMPONENT DESIGNATION	DESCRIPTION
C68	Capacitor Tanatalum Tap 10uF 35V 20%
C69	Capacitor Ceramic Z5U 0.1uF 50V 20%
C70	Capacitor Ceramic 680pF 100V 20%
C71	Capacitor Ceramic 0.1uF 50V 20%
C72	Capacitor Alumin Electrolytic 1000uF 10V 20%
DI	Diodes IN4001
TR1-TR8	Transistor Mosfet Type VP0808L
IC1	SN74LS244
IC2	SN74LS219
IC5	SN74LS244
IC6	SN74LS219
IC7	SN74LS32
IC8	SN74LS74
IC9	PROM 82S126
IC10	SN74LS219
IC11	SN74LS123
IC12	SN74LS107
IC13	SN74LS14
IC14	SN74LS132
IC15	SN74LS163
IC16	SN74LS08
IC17	SN74LS682
IC18	SN74S38
IC19	SN74LS74
IC20	SN74LS682
IC21	SN74LS682
IC22	SN74LS244
IC23	DAC800P-CBI-V
IC24	DG508A
IC25	XTR 110
IC26	XTR 110
IC27	XTR 110
IC28	XTR 110
IC29	TL072
IC30	TL072
IC31	XTR 110
IC32	TL072
IC33	TL072
IC34	XTR 110
IC35	XTR 110
IC36	XTR 110

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Table 2.9
Address Modifier Codes

HEX CODE	ADDRESS MODIFIER 5	4	3	2	1	0	FUNCTION FUNCTION	DEFINED BY
3F	H	H	H	H	H	H	Standard Addressing Supervisory Ascending Access	VMEbus Spec.
3E	H	H	H	H	H	L	Standard Addressing Supervisory Program Access	VMEbus Spec.
3D	H	H	H	H	L	H	Standard Addressing Supervisory Data access	VMEbus Spec.
3C	H	H	H	H	L	L	Undefined	Reserved
3B	H	H	H	L	H	H	Standard Addressing Non-Privil. Ascending Access	VMEbus Spec.
3A	H	H	H	L	H	L	Standard Addressing Non-Privil. Program Access	VMEbus Spec.
39	H	H	H	L	L	H	Standard Addressing Non-Privil. Data access	VMEbus Spec.
38	H	H	H	L	L	L	Undefined	Reserved
30-37	H	H	L	X	X	X	Undefined	Reserved
2F	H	L	H	H	H	H	Undefined	Reserved
2E	H	L	H	H	H	L	Undefined	Reserved
2D	H	L	H	H	L	H	Short Addressing Supervisory I/O Access	VMEbus Spec.
2C	H	L	H	H	L	L	Undefined	Reserved
2B	H	L	H	L	H	H	Undefined	Reserved
2A	H	L	H	L	H	L	Undefined	Reserved
29	H	L	H	L	L	H	Short Addressing Non-Privileged I/O Access	VMEbus Spec.
28	H	L	H	L	L	L	Undefined	Reserved
20-27	H	L	L	X	X	X	Undefined	Reserved
10-1F	L	H	X	X	X	X	Undefined	Reserved
0F	L	L	H	H	H	H	Extended Supervisory Ascending Access	VMEbus Spec.
0E	L	L	H	H	H	L	Extended Supervisory Program Access	VMEbus Spec.
0D	L	L	H	H	L	H	Extended Supervisory Data Access	VMEbus Spec.
0C	L	L	H	H	L	L	Undefined	Reserved
0B	L	L	H	L	H	H	Extended Non-Privileged Ascending Access	VMEbus Spec.
0A	L	L	H	L	H	L	Extended Non-Privileged Program Access	VMEbus Spec.
09	L	L	H	L	L	H	Extended Non-Privileged Data Access	VMEbus Spec.
08	L	L	H	L	L	L	Undefined	Reserved
00-07	L	L	L	X	X	X	Undefined	Reserved

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Address Modifier Codes (Cont'd)

NOTES:

Short address uses 15 address lines (A01-A15)
Standard address uses 23 address lines (A01-A23)
Extended address uses 31 address lines (A01-A31)

Codes defined by the "VMEbus Spec." should not be used for purposes othe than those specified.

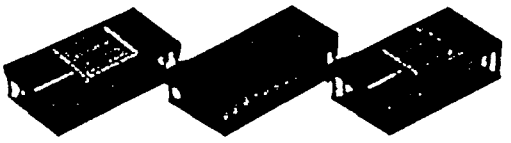
Codes defined by "User" may be used for any purpose which the VMEbus user (board vendor or customer) deems appropriate (page switching, memory protection, MASTER or task identification, privileged access to resources, etc.,).

Codes defined by "Reserved" should not be used by the user; they are reserved for system use and future enhancements.

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BURR-BROWN®

DAC800
DAC800P



Integrated Circuit
DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW COST HIGH RELIABILITY SINGLE-CHIP REPLACEMENT FOR INDUSTRY STANDARD DAC80
- 12-BIT RESOLUTION
- ±1/2LSB MAXIMUM NONLINEARITY, 0°C to +70°C
- GUARANTEED MONOTONICITY, 0°C to +70°C
- DUAL-IN-LINE PACKAGE WITH INDUSTRY STANDARD (DAC80) PINOUT
- HERMETIC PACKAGE (optional)
- TWO PACKAGE OPTIONS: hermetic side-brazed and molded plastic
- GUARANTEED SPECIFICATIONS WITH ±12V AND ±15V SUPPLIES

DESCRIPTION

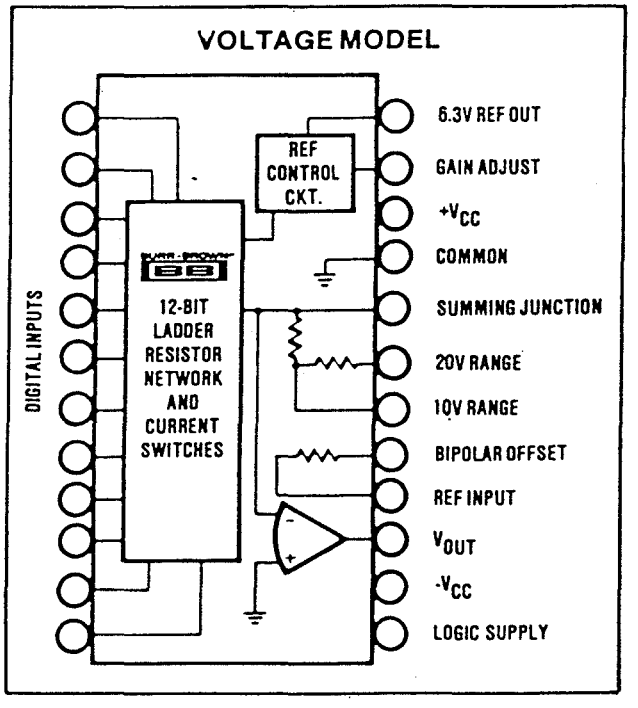
The DAC800 is a third-generation monolithic Integrated Circuit that is a pin-for-pin equivalent to the industry-standard DAC80 first introduced by Burr-Brown. It has all of the functions of its predecessor plus faster settling time and enhanced reliability because of its monolithic construction.

The current output model of the DAC800 is a single-chip integrated circuit containing a subsurface zener reference diode, high speed current switches, and laser-trimmed thin-film resistors. The DAC800 provides output voltage ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V (V models) or output current ranges of ±1.175mA or 0 to −2.35mA (I model).

This high accuracy converter offers a maximum nonlinearity error of ±1/2LSB, ±30ppm/°C maximum gain drift and guaranteed monotonicity, all over 0°C to +70°C. In the bipolar configuration, total drift is guaranteed to be less than 25ppm of FSR/°C.

The DAC800 is in a 24-pin dual-in-line package with the popular DAC80 pinout. Two package options are available: a hermetic ceramic side-brazed package and a low-cost molded plastic package (voltage out only).

For designs that require a wide temperature range, see Burr-Brown models DAC850 and DAC851.



Patents pending may apply upon the allowance and issuance of patents thereon. The product may also be covered in other countries by one or more international patents.

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PDS-440C

Printed in U.S.A. March, 1984

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SPECIFICATIONS

ELECTRICAL

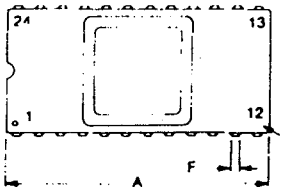
Typical at +25°C and $\pm V_{CC}$ = 12V or 15V unless otherwise noted.

MODEL	DAC800, DAC800P			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUT				
Resolution			12	bits
Logic Levels				
(over spec. temp range)[1]				
V_{IH} (Logic "1")	+2		16.5	VDC
V_{IL} (Logic "0")	0		+0.8	VDC
I_{IH} (V_{IH} = +2.4V)			+20	µA
I_{IL} (V_{IH} = +0.4V)			−0.36	mA
ACCURACY				
Linearity Error at 25°C		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	+1, −3/4	LSB
Gain Error[2]		±0.1	±0.3	%
Offset Error[2]		±0.05	±0.15	% of FSR[3]
POWER SUPPLY SENSITIVITY				
+15V and +5V Supplies		±0.0001	±0.001	% of FSR/%V_{CC}
−15V Supply		±0.003	±0.006	% of FSR/%V_{CC}
DRIFT[4](0°C to +70°C)				
Bipolar Drift (±full scale drift for the bipolar connection)		±10	±25	ppm of FSR/°C
Total error over 0°C to +70°C[5]				
Unipolar		±0.06	±0.15	% of FSR
Bipolar		±0.05	±0.12	% of FSR
Gain		±10	±30	ppm/°C
Unipolar Offset		±1	±3	ppm of FSR/°C
Bipolar Offset		±7	±15	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	+1, −7/8	LSB
Linearity Error 0°C to +70°C			±1/2	LSB
Monotonicity Temp. Range, min	0		+70	°C
CONVERSION SPEED, V models				
Settling Time to ±0.01% of FSR				
For FSR Change				
20V range, 2kΩ load		3	5	µsec
10V range, 2kΩ load		2.5	4	µsec
For 1LSB Change, Major Carry, 2kΩ load		1.5		µsec
Slew Rate, 2kΩ load	10	15		V/µsec
CONVERSION SPEED, I model (DAC800 only)				
Settling Time to ±0.01% of FSR				
For FSR Change				
10Ω to 100Ω load		300		nsec
1kΩ load		1		µsec
ANALOG OUTPUT, V models				
Ranges ($\pm V_{CC}$ = 15V)[6]	±2.5, ±5, ±10, 0 to +5, 0 to +10			V
Output Current	±5			mA
Output Impedance (DC)		0.05		Ω
Short Circuit to Common, Duration		Indefinite		
ANALOG OUTPUT, I model (DAC800 only)				
Ranges: Bipolar	±0.88	±1.175	±1.47	mA
Unipolar	0 to −1.76	0 to −2.35	0 to −2.94	mA
Output Impedance: Bipolar		3.1		kΩ
Unipolar		7.2		kΩ
Compliance	−2.5		+2.5	V
REFERENCE VOLTAGE OUTPUT	+6.23	+6.30	+6.37	V
Current (for external loads), Source	1.5	2.5		mA
Tempco of Drift		±10	±30	ppm/°C
POWER SUPPLY REQUIREMENTS				
$\pm V_{CC}$	±11.4	±15	±16.5	VDC
V_{DD}[7]	+4.5	+5.0	+16.5	VDC
Supply Drain				
+15V, −15V (no load)		+8, −20	+12, −25	mA
85V (logic supply)		+7	+10	mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating[8]	−25		+85	°C
Storage	−60		+100	°C

The information in this publication has been carefully checked and is believed to be reliable; however, no responsibility is assumed for possible inaccuracies or omissions. Prices and specifications are subject to change without notice. No patent rights are granted to any of the circuits described herein.

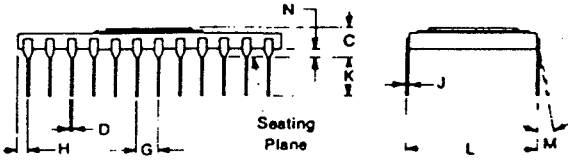
MECHANICAL

DAC800



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

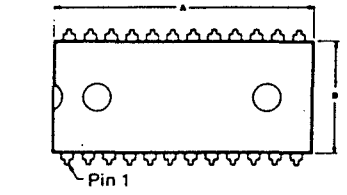
Pin numbers shown for reference only. Numbers may not be marked on kage package.



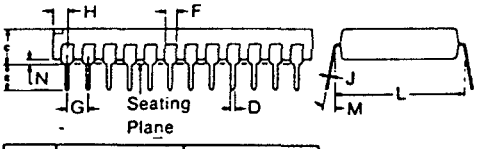
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

CASE: Ceramic
MATING CONNECTOR: 0245MC
WEIGHT: 4.1 grams (0.15 oz.)

DAC800P



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.



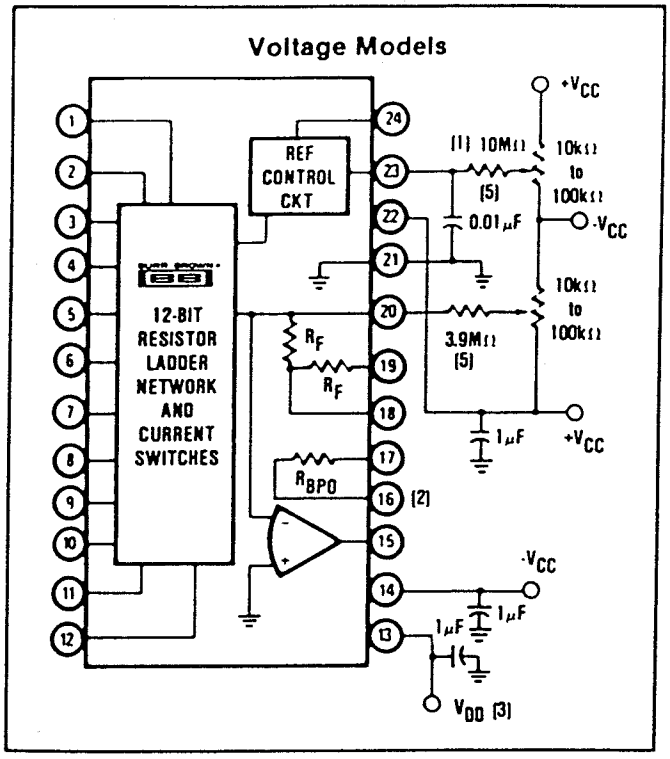
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.233	1.283	31.32	32.59
B	.538	.575	13.67	14.61
C	.169	.224	4.29	5.69
D	.015	.023	0.38	0.58
F	.043	.062	1.09	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.132	2.54	3.35
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.022	0.46	0.56

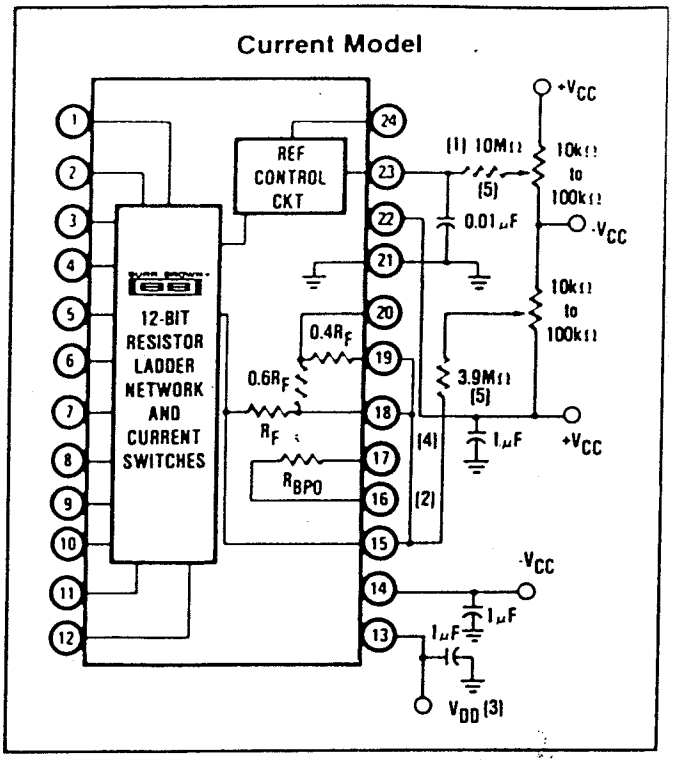
CASE: Plastic
MATING CONNECTOR: 0245MC
WEIGHT: 3.7 grams (0.13 oz.)

NOTES:
(1) Refer to Logic Input Compatibility section.
(2) Adjustable to zero with external trim potentiometer.
(3) FSR means "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc.
(4) To maintain drift spec internal feedback resistors must be used for current output models.
(5) Includes the effects of gain, offset and linearity drift. Gain and offset errors are adjusted to zero at +25°C.
(6) A minimum of ±13V supply is required for ±10V and 0 to 10V ranges. All other ranges accept ±12V supplies.
(7) Power dissipation is an additional 100mW, max, when V_{DD} is operated at +15V.
(8) Max operating temperature for DAC800P-CBI-V is +70°C.

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CONNECTION DIAGRAMS





PIN ASSIGNMENTS

I MODEL	PIN NO	V MODELS
MSB BIT 1	1	BIT 1 MSB
BIT 2	2	BIT 2
BIT 3	3	BIT 3
BIT 4	4	BIT 4
BIT 5	5	BIT 5
BIT 6	6	BIT 6
BIT 7	7	BIT 7
BIT 8	8	BIT 8
BIT 9	9	BIT 9
BIT 10	10	BIT 10
BIT 11	11	BIT 11
LSB BIT 12	12	BIT 12 LSB
LOGIC SUPPLY, V_{DD}	13	LOGIC SUPPLY, V_{DD}
$-V_{CC}$	14	$-V_{CC}$
I_{OUT}	15	V_{OUT}
REF. INPUT	16	REF. INPUT
BIPOLAR OFFSET	17	BIPOLAR OFFSET
SCALING NETWORK	18	10V RANGE
SCALING NETWORK	19	20V RANGE
SCALING NETWORK	20	SUMMING JUNCTION
COMMON	21	COMMON
$+V_{CC}$	22	$+V_{CC}$
GAIN ADJUST	23	GAIN ADJUST
6.3V REF. OUT	24	6.3V REF. OUT

NOTES.

1. DAC80 which may be replaced by DAC800 requires a 33MΩ resistor. DAC800 requires a 10MΩ resistor. DAC80's may also be operated with a 10MΩ resistor resulting in increased trim range.
2. Pin 16 of DAC800 is used only to connect the bipolar offset resistor. An external reference voltage may not be used with DAC800 as is possible with DAC80.
3. If connected to $+V_{CC}$, which is permissible, power dissipation increases 75mW typ, 100mW max.
4. For fastest settling time connect pins 19, 18, and 15 together.
5. Values shown are for ±15V supplies. For supplies below ±13.5V use 2.7MΩ in place of 3.9MΩ and 7.5MΩ in place of 10mΩ.

ORDERING INFORMATION

MODEL	OUTPUT	PACKAGE
DAC800-CBI-I	Current	Side-braze
DAC800-CBI-V	Voltage	Side-braze
DAC800P-CBI-V	Voltage	Molded Plastic

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DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC800 accepts complementary binary digital input codes. The CBI model may be connected by the user for any one of three complementary codes: CSB, CTC, or COB.

TABLE I. Digital Input Codes.

DIGITAL INPUT	ANALOG OUTPUT		
MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
000000000000	+Full Scale	+Full Scale	-1LSB
011111111111	+1/2 Full Scale	Zero	-Full Scale
100000000000	1/2 Full Scale -1LSB	-1LSB	+Full Scale
111111111111	Zero	-Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC800 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0°C to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0°C to +70°C range is guaranteed in the DAC800 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain Drift is established by: 1) testing the end point differences for each DAC800 model at 0°C, +25°C and +70°C; 2) calculating the gain change with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C.

Offset Drift is a measure of the change in output with all "1"s on the inputs over the specified temperature range. The Offset is measured at 0°C, +25°C and +70°C. The maximum change in Offset is referenced to the Offset at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

Bipolar Drift is a measure of the change in plus or minus full scale output over the specification temperature range for the bipolar connection. Because Bipolar Offset Drift and Gain Drift have canceling interactions, Bipolar Drift is not simply the sum of the two. Total bipolar error over temperature is calculated using Bipolar Drift, then adding ±1/2LSB of linearity error.

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

Voltage Output Models: Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output Model: Two settling times are specified to ±0.01% of FSR. Each is given for the current model connected with two different resistive loads: 10Ω to 100Ω and 1000Ω. Internal resistors are provided for connecting a nominal load resistance of approximately 1000Ω for output voltage ranges of ±1V and 0 to -2V.

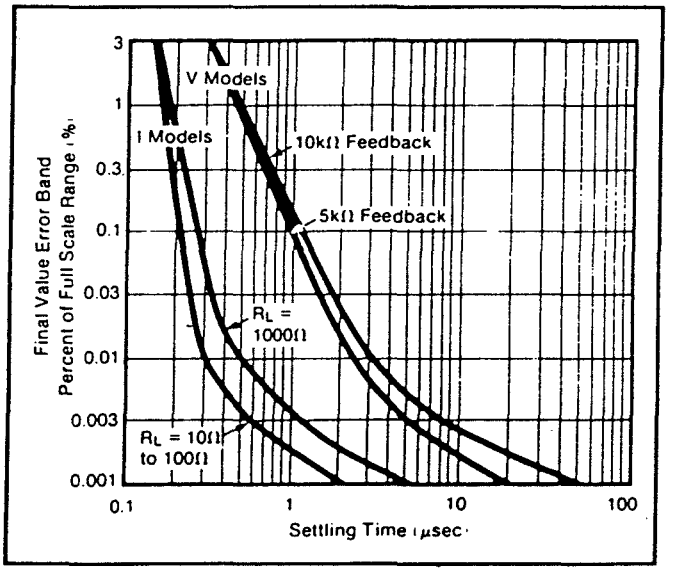


FIGURE 1. Full Scale Range Settling Time vs Final Value Error Band.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is -2.5V to +2.5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 2).

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For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is -10V. See Table II for corresponding codes and the Connection Diagrams for offset adjustment connections. Offset should be adjusted prior to gain.

Gain Adjustment: For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagrams for gain adjustment connections.

TABLE II. Digital Input/Analog Output.

Digital Input	Analog Output			
	Voltage*		Current	
MSB LSB	0 to +10V	±10V	0 to −2mA	±1mA
000000000000	+9.9976V	+9.9951V	−1.9995mA	−0.9995mA
011111111111	+5.0000V	0.0000V	−1.0000mA	0.0000mA
100000000000	+4.9976V	−0.0049V	−0.9995mA	+0.0005mA
111111111111	0.0000V	−10.0000V	0.0000mA	+1.0000mA
One LSB	2.44mV	4.88mV	0.488μA	0.488μA

*To obtain values for other binary ranges:
0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

VOLTAGE OUTPUT MODELS

Output Range Connections

Internal scaling resistors provided in the DAC800 may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.

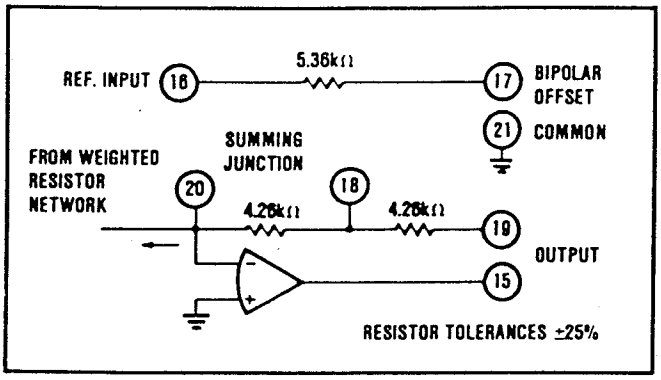


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

TABLE III. Output Voltage Range Connections - Voltage Model DAC800.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	NC	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other device components. Connections for various output-voltage ranges are shown in Table III. Settling time for a full scale range change is specified as 3μsec for the 20-volt range and 2.5μsec for the 10-volt range.

CURRENT OUTPUT MODEL

The resistive scaling network and equivalent output circuit of the current model differ from the voltage model and are shown in Figures 7 and 8.

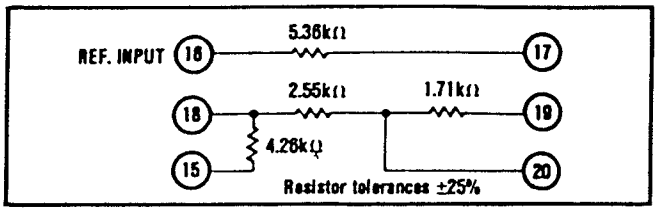


FIGURE 7. Internal Scaling Resistors.

Internal scaling resistors (Figure 7) are provided to scale an external op amp or to configure load resistors for a voltage output. These connections are described in the following sections.

If the internal resistors are not used for voltage scaling, external R_L (or R_F) resistors should have a TCR of

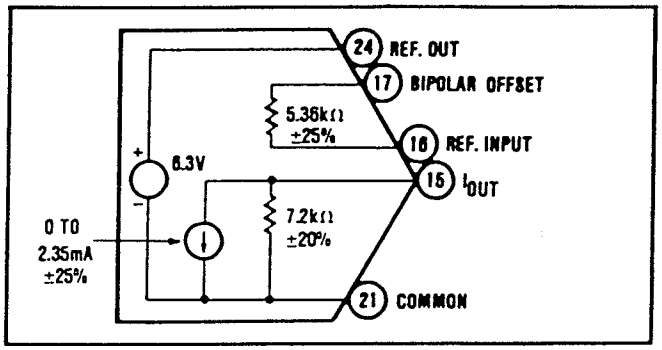


FIGURE 8. Current Output Model Equivalent Output Circuit.

±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 9 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2.35mA \left(\frac{R_L \times 7.2k\Omega}{R_L + 7.2k\Omega} \right)$$

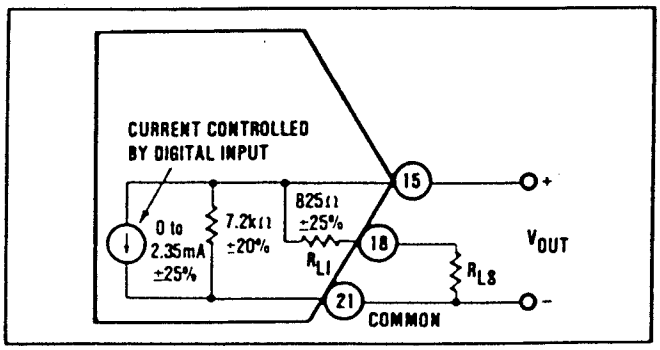


FIGURE 9. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.

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To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift. Tolerances on internal equivalent resistors are wide. R_{LS} will have to be selected for each unit.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is shown in Figure 10, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1.175mA\left(\frac{R_L \times 3.07k\Omega}{R_L + 3.07k\Omega}\right)$$

To achieve specified drift, connect 1.71kΩ and 2.55kΩ internal scaling resistors in parallel (R_{LI}) and add an external metal film resistor (R_{LS}) in series to obtain a full

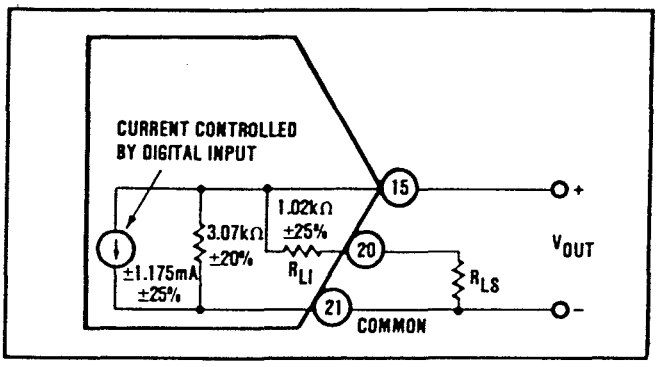


FIGURE 10. Current Output Model Connected for Bipolar Output Voltage with Resistive Load.

scale output range of ±1V. The tolerances on the internal equivalent resistors are wide. R_{LS} will have to be selected for each unit.

Driving An External Op Amp

The current output model DAC800 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. See Figure 11.

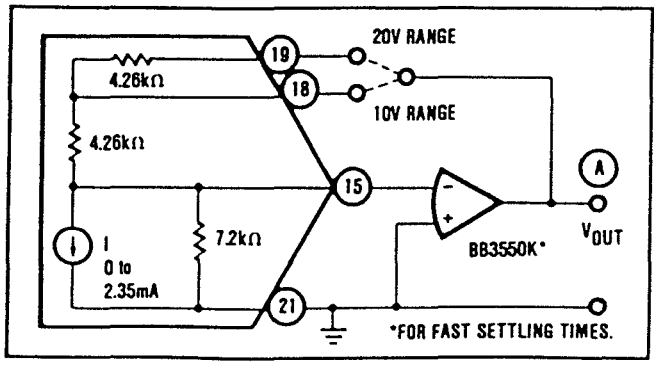


FIGURE 11. External Op Amp - Using Internal Feedback Resistors.

$$V_{OUT} = I_{OUT} \times R_f$$

where I_{OUT} is the DAC800 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current output model DAC800 provides output voltage ranges the same as the voltage model DAC800. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

TABLE IV. Voltage Range of Current Output DAC800.

Output Range	Digital Input Codes	Connect (A) to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	(A)	24
±5V	COB or CTC	18	15	NC	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	15	24

Output Larger Than 20V Range

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1.175mA ±25% for bipolar voltage ranges and -2.35mA ±25% for unipolar voltage ranges. See Figure 12. Use protection diodes when a high voltage op amp is used.

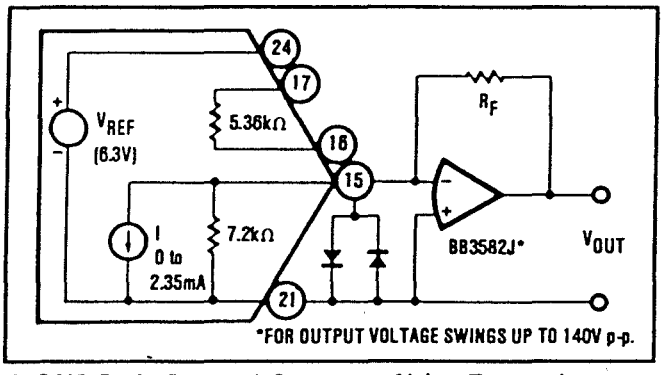


FIGURE 12. External Op Amp - Using External Feedback Resistors.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50 ppm/°C + R_F drift to total drift.

LOGIC INPUT COMPATIBILITY

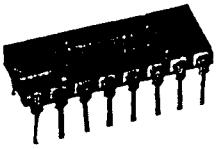
DAC800 digital inputs are TTL, LSTTL and 54/74HC CMOS compatible over the operating range of V_{DD}, +5 to +15V. The input switching threshold remains at the TTL threshold over supply range of V_{DD}, +5V to +15V.

Logic "0" input current over temperature is low enough to permit driving DAC800 directly from outputs of 4000B and 54/74C CMOS devices over the logic power supply range of +5V to +15V.

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XTR110



PRECISION VOLTAGE-TO-CURRENT CONVERTER/TRANSMITTER

FEATURES

- 4mA TO 20mA TRANSMITTER
- SELECTABLE INPUT/OUTPUT RANGES:
  0V to +5V, 0V to +10V Inputs
  0mA to 20mA, 5mA to 25mA Outputs
  Other Ranges
- 0.01% MAX NONLINEARITY, 12 BIT
- PRECISION +10V REFERENCE OUTPUT
- SINGLE SUPPLY OPERATION
- CURRENT SOURCING TO COMMON
- WIDE SUPPLY RANGE, 13.5V TO 40V

APPLICATIONS

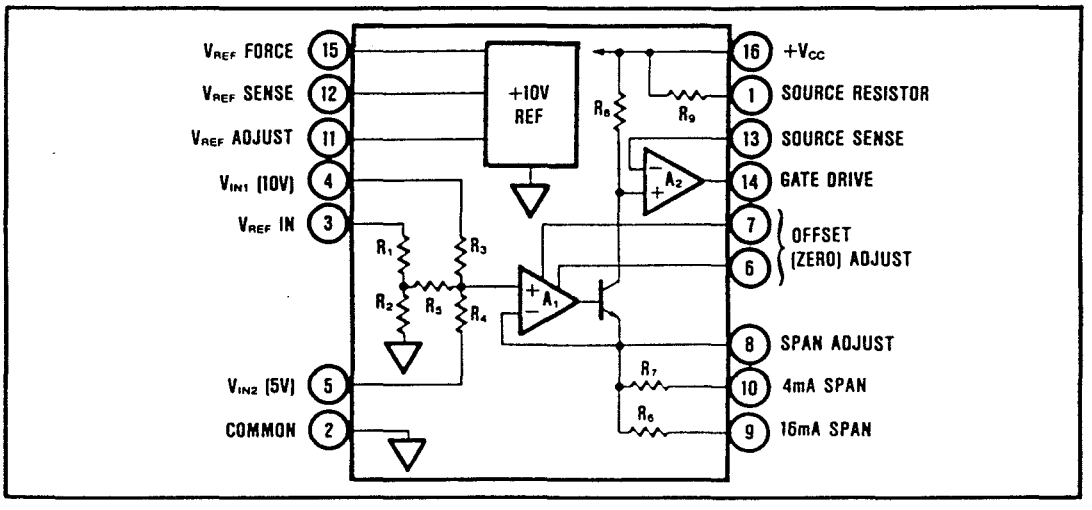
- INDUSTRIAL PROCESS CONTROL
- PRESSURE/TEMPERATURE TRANSMITTERS
- CURRENT-MODE BRIDGE EXCITATION
- GROUNDED TRANSDUCER CIRCUITS
- CURRENT SOURCE REFERENCE FOR DATA ACQUISITION
- PROGRAMMABLE CURRENT SOURCE FOR TEST EQUIPMENT
- AUTOMATED MANUFACTURING
- POWER PLANT/ENERGY SYSTEM MONITORING

DESCRIPTION

The XTR110 is a monolithic precision voltage-to-current converter. It can convert standard 0V to +10V or 0V to +5V inputs into 4mA to 20mA, or 5mA to 25mA outputs. The required external MOS transistor keeps heat outside the XTR110 package to optimize performance under all output conditions.

A precision +10V reference output can drive 10mA. An external transistor can be added for more current, e.g. 33mA for 300Ω bridges.

The XTR110 is a key data acquisition component, designed for high noise immunity current-mode transmission. It is also ideal as a precision programmable current source for transducer circuits and test equipment.



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PDS-555

Printed in U.S.A. November, 1984

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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_{CC} = +24V and R_L = 250Ω† unless otherwise specified. Test circuit: see Figure 1.

PARAMETER	CONDITIONS	XTR110AG MIN	XTR110AG TYP	XTR110AG MAX	XTR110BG MIN	XTR110BG TYP	XTR110BG MAX	UNITS
TRANSMITTER								
Transfer Function			$I_O = 10\,[(V_{REF}\ IN/16) + (V_{IN1}/4) + (V_{IN2}/2)]/R_{SPAN}$					
Input Range: V_{IN1}	Specified performance	0		+10	*		*	V
V_{IN2}	Specified performance	0		+5	*		*	V
Current, I_O	Specified performance[1]	4		20	*		*	mA
	Derated performance[1]	0		40	*		*	mA
Nonlinearity	16mA/20mA span[2]		0.01	0.025		0.002	0.005	% of span
Offset Current, I_{OS}	I_O = 4mA[1]							
Initial	[1]			0.4			0.1	% of span
vs Temp	[1]			0.005			0.003	% of span/°C
vs Supply, V_{CC}	[1]			0.005			*	% of span/V
Span Error	I_O = 20mA							
Initial	[1]			0.6			0.2	% of span
vs Temp	[1]			0.005			0.003	% of span/°C
vs Supply, V_{CC}	[1]			0.005			*	% of span/V
Output Resistance	From drain of FET (Q_{EXT})[3]		10×10^9			*		Ω
Input Resistance	V_{IN1}		27			*		kΩ
	V_{IN2}		22			*		kΩ
	V_{REF} IN		19			*		kΩ
Dynamic Response								
Settling Time	To 0.1% of span		15			*		µsec
	To 0.01% of span		20			*		µsec
Slew Rate			1.3			*		mA/µsec
VOLTAGE REFERENCE								
Output Voltage		+9.95	+10	+10.05	+9.98	*	+10.02	V
vs Temp				50			30	ppm/°C
vs Supply, V_{CC}	Line regulation			0.005			*	%/V
vs Output Current	Load regulation			0.01			*	%/mA
vs Time			100			*		ppm/1k hrs
Trim Range	[4]	−0.100		+0.25	*		*	V
Output Current[5]	Specified performance	10			*			mA
POWER SUPPLY								
Input Voltage, V_{CC}		+13.5		+40	*		*	V
Quiescent Current	Excluding I_O		3	4.5		*	*	mA
TEMPERATURE RANGE								
Specification		−40		+85	*		*	°C
Operating		−55		+125	*		*	°C
Storage		−55		+125	*		*	°C

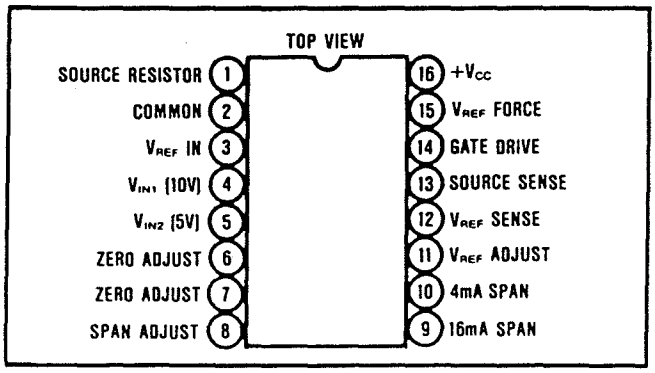
*Specification same as grade to the immediate left. †Specifications apply to the range of R_L shown in Typical Performance Curves.

NOTES: (1) Including internal reference. (2) Span is the change in output current resulting from a full-scale change in input voltage. (3) Within compliance range limited by (+V_{CC} − 2V) + V_{DS} required for linear operation of the FET. (4) For V_{REF} adjustment circuit see Figure 2. (5) For extended I_{REF} drive circuit see Figure 6.

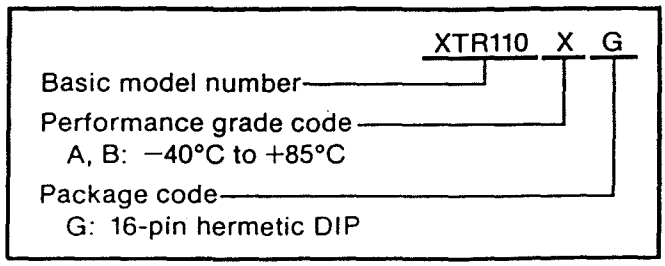
ABSOLUTE MAXIMUM RATINGS

Power Supply, +V_{CC}	40V
Input Voltage, V_{IN1}, V_{IN2}, V_{REF} IN	+V_{CC}
Storage Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10sec)	300°C
Output Short Circuit Duration, Gate Drive and V_{REF} Force	Continuous to common and +V_{CC}
Output Current Using Internal 50Ω Resistor	40mA

PIN CONFIGURATION

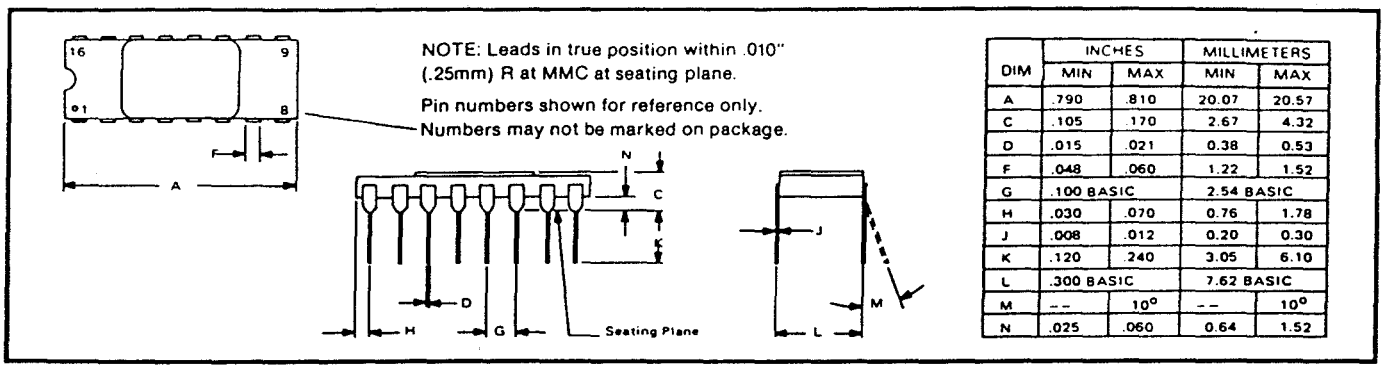


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MECHANICAL

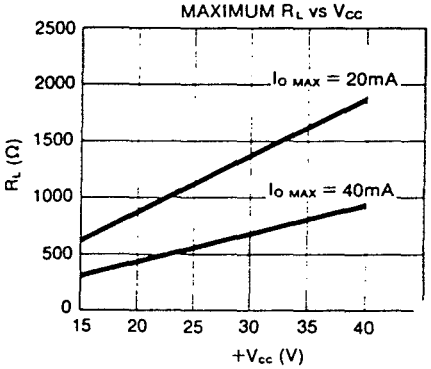


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.025	.060	0.64	1.52

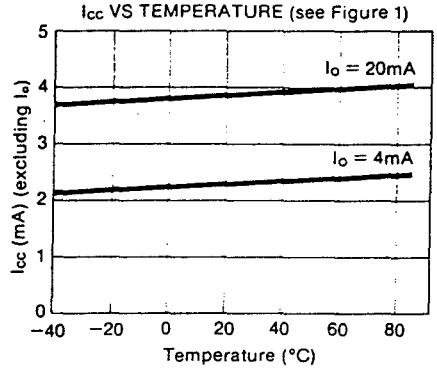
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = 24VDC, R_L = 250Ω unless otherwise noted.

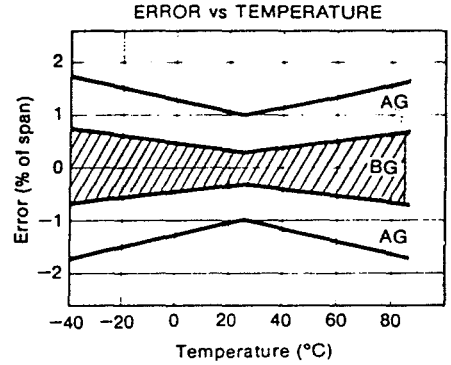
MAXIMUM R_L vs V_{CC}



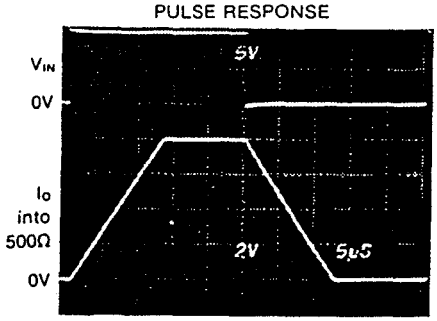
I_{CC} VS TEMPERATURE (see Figure 1)



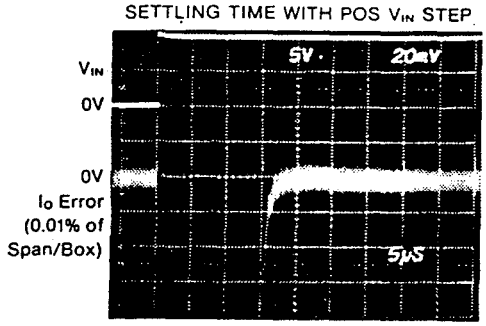
TOTAL OUTPUT ERROR vs TEMPERATURE



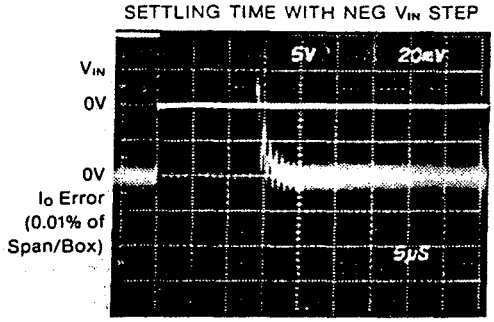
PULSE RESPONSE



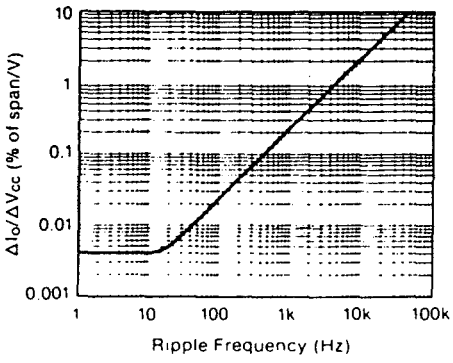
SETTLING TIME WITH POS V_{IN} STEP



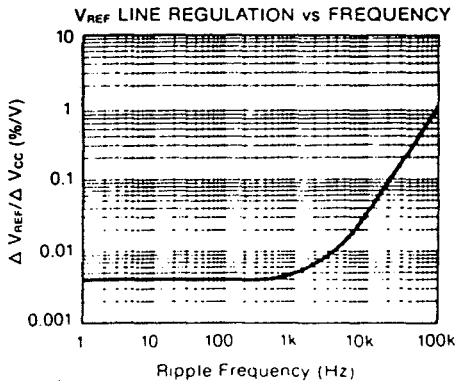
SETTLING TIME WITH NEG V_{IN} STEP



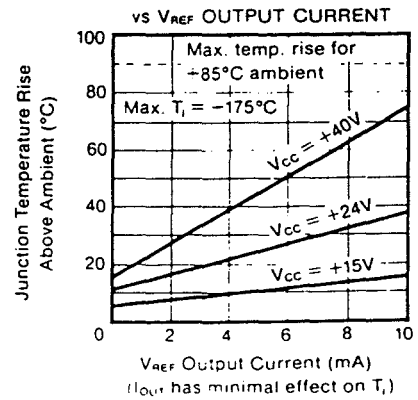
I_O POWER SUPPLY REJECTION vs FREQUENCY



V_{REF} LINE REGULATION vs FREQUENCY



JUNCTION TEMPERATURE RISE vs V_{REF} OUTPUT CURRENT



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THEORY OF OPERATION

The XTR110 is designed to convert a high level input voltage into a positive output current.

A block diagram of the XTR110 is shown in Figure 1. The circuit contains four main functional blocks: (1) a precision resistor divider network (R_1–R_5), (2) a voltage-to-current converter (A_1, Q_1, R_6, R_7), (3) a current-to-current converter (A_2, R_8, R_9, Q_{EXT}), and (4) a precision +10V reference.

The precision divider network sums three input voltages to the noninverting input of A_1. These are V_{IN1} (10V full scale), V_{IN2} (5V full scale), and V_{REF} IN (for offsetting).

In the voltage-to-current converter, the op amp, A_1, forces its input voltage across the span setting resistors, R_6 and R_7. Since Q_1 is a high gain Darlington, base current error is negligible and all current flows to the current-to-current converter (into R_8). The transfer function including input divider is as follows:

$$I_{R8} = [(V_{REF}\ IN/16) + (V_{IN1}/4) + V_{IN2}/2)]/R_{SPAN}$$

where R_{SPAN} is the resistance from Q_1 emitter to common.

The current-to-current converter is the output section of the XTR110 transmitter. The voltage across the 500Ω resistor (R_8) is forced across the 50Ω resistor (R_9) by A_2 and the external MOSFET (Q_{EXT}). Since no current flows in the gate of the MOSFET, all current is delivered to the output. This current (I_{OUT}) is ten times the internal current through R_8. Use of the external transistor keeps power out of the precision IC to maintain accuracy.

The overall transfer function for the XTR110 transmitter is:

$$I_O = 10[(V_{REF}\ IN/16) + (V_{IN1}/4) + (V_{IN2}/2)]/R_{SPAN}.$$

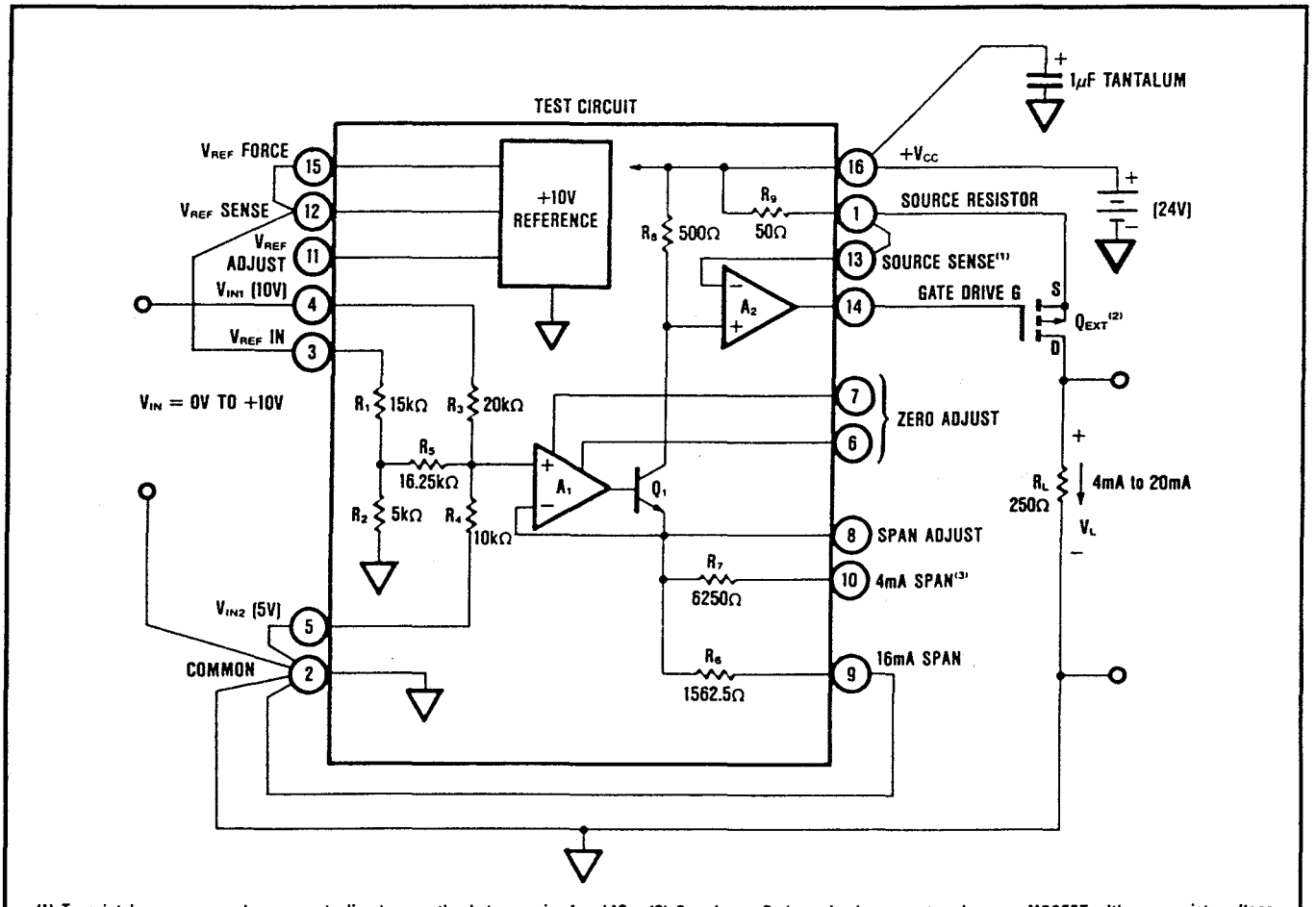
For output currents beyond 40mA an external resistor can be used in place of R_9.

The +10V reference provides input offsetting, e.g. 4mA offset for the 4ma to 20mA output configuration. The reference can deliver 10mA and is protected from shorts to common. Higher current can be provided for other applications by using an external NPN transistor connected to the sense and force pins.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CONNECTION

The basic connection of the XTR110 is the standard 0V to +10V input; 4mA to 20mA output configuration is shown in Figure 1.



(1) To maintain accuracy, make a separate direct connection between pins 1 and 13. (2) Q_{EXT} is any P-channel enhancement-mode power MOSFET with appropriate voltage and power rating. For fast response use FETs with low input capacitance (C_{ISS}). Some recommended devices are: Ferranti, ZVP01 series and Supertex VP01 series. (3) For 20mA span, strap 4mA and 16mA pins together to common.

FIGURE 1. Block Diagram of the XTR110 in Basic Connection: 0V to +10V in, 4mA to 20mA out.

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EXTERNAL TRANSISTOR

Connections to the MOSFET are gate drive (pin 14) and source resistor (pin 1). To eliminate errors due to resistance in the connection between pin 1 and the source of the external transistor, connect pin 13 directly to pin 1 as shown in Figure 1.

$+V_{CC}$ may originate at the XTR110 site or may be brought in as part of a three-wire twisted line. Be sure to use sufficient bypassing close to the XTR110 on the $+V_{CC}$ line.

COMMONS

Careful attention should be directed toward proper connection of the commons. All commons should be joined at one point as close to pin 2 of the XTR110 as possible. The exception is the I_{OUT} return. It can be returned to any place where it will not modulate the common at pin 2.

VOLTAGE REFERENCE

The reference voltage is accurately regulated at pin 12 (V_{REF} sense). To preserve accuracy, any load including pin 3 should be connected to this point.

The circuit in Figure 2 shows coarse and fine adjustment of the voltage reference.

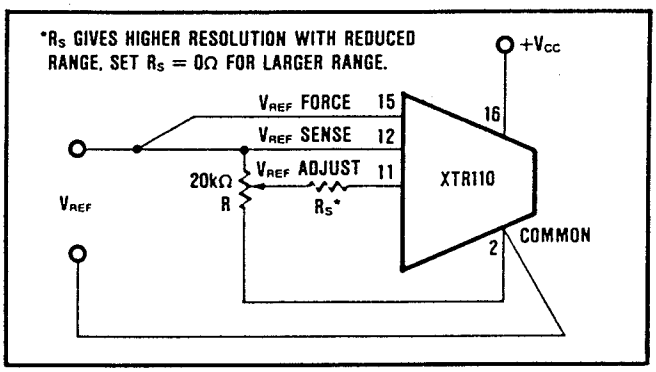


FIGURE 2. Optional Adjustment of Reference Voltage.

OFFSET (ZERO) ADJUSTMENT

The offset current can be adjusted by using the potentiometer, R_1, shown in Figure 3. The procedure is to set the input voltage to zero and then adjust R_1 to give 4mA at the output. For spans starting at 0mA, the following special procedure is recommended: set the input to a small nonzero value and then adjust R_1 to the proper output current. When the input is zero the output will be zero. Figure 4 and 5 show graphically how offset is adjusted.

SPAN ADJUSTMENT

The span is adjusted at the full-scale output current using the potentiometer, R_2, shown in Figure 3. This adjustment is interactive with the offset adjustment, and a few iterations may be necessary. For the circuit shown, set the input voltage to +10V full scale and then adjust R_2 to give 20mA full-scale output. Figures 4 and 5 show graphically how span is adjusted.

The values of R_2, R_3, and R_4 for adjusting the span are determined as follows: choose R_4 in series to slightly decrease the span; then choose R_2 and R_3 to increase the span to be adjustable about the center value.

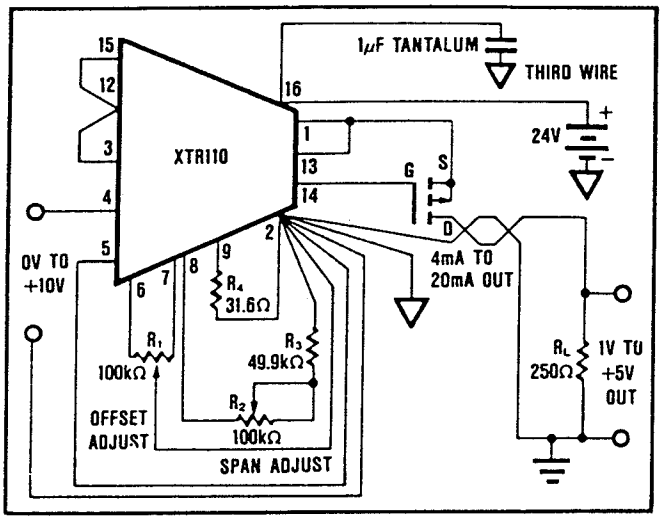


FIGURE 3. Offset and Span Adjustment Circuit for 0V to +10V Input, 4mA to 20mA Output.

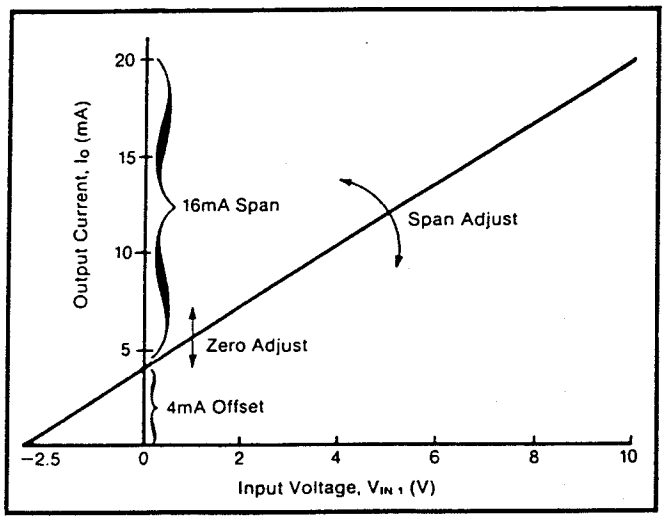


FIGURE 4. Zero and Span of 0V to +10V_{IN}, 4mA to 20mA Output Configuration.

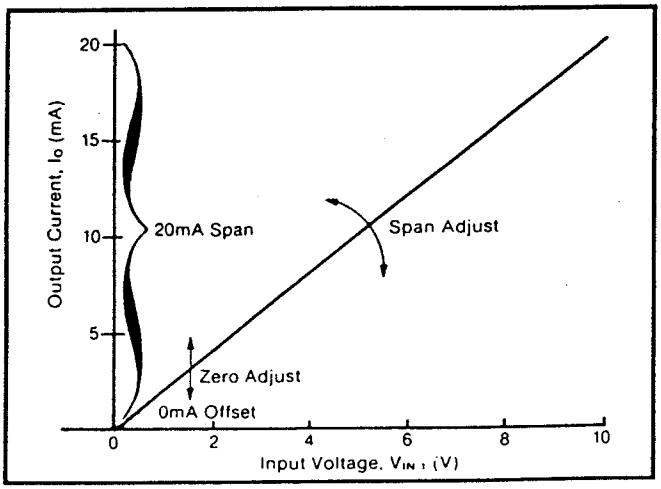


FIGURE 5. Zero and Span of 0V to +10V_{IN}, 0mA to 20mA Output Configuration.

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STANDARD CURRENT RANGES OR SPANS

Table I shows the pin connections for standard XTR110 current ranges.

TABLE I. Pin Connections for Standard Ranges.

Input Range (V)	Output Range (mA)	Pin 3	Pin 4	Pin 5	Pin 9	Pin 10
0 - 10 2 - 10	0 - 20 4 - 20	Com	Input	Com	Com	Com
0 - 10	4 - 20	+10V Ref	Input	Com	Com	Open
0 - 10	5 - 25	+10V Ref	Input	Com	Com	Com
0 - 5 1 - 5	0 - 20 4 - 20	Com	Com	Input	Com	Com
0 - 5	4 - 20	+10V Ref	Com	Input	Com	Open
0 - 5	5 - 25	+10V Ref	Com	Input	Com	Com

EXTENDED SPAN

For spans beyond 40mA, the internal 50Ω resistor (R_9) may be replaced by an external resistor connected between pins 13 and 16. This resistor should have a low TC. Also the self heating of this external resistor can cause nonlinearity. Choose one with an adequate power rating.

EXTENDED REFERENCE CURRENT DRIVE

The current drive capability of the XTR110's internal reference is 10mA. This can be extended if desired by adding an external NPN transistor shown in Figure 6.

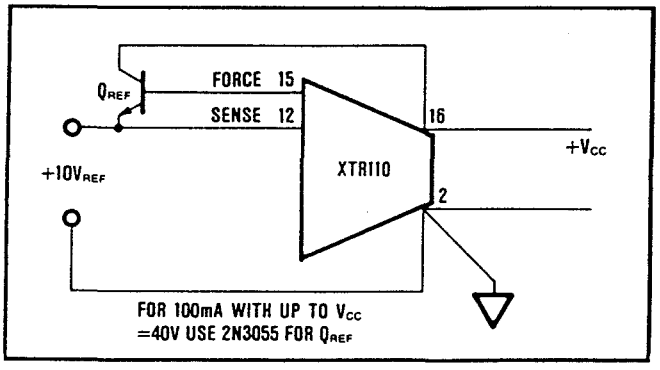


FIGURE 6. Extended Reference Current Drive.

LOW TEMPERATURE COEFFICIENT (TC) OPERATION

Although the precision resistors in the XTR110 track within 1ppm/°C, the output current depends upon the absolute temperature coefficient of any one of the resistors, R_6, R_7, R_8, and R_9. Since the absolute TC of the resistors is 20ppm/°C, maximum, the TC of the output current can have 20ppm/°C drift. For low TC operation, zero TC resistors can be substituted for either the span resistors (R_6 or R_7) or for the source resistor (R_9) but not both.

ERROR CALCULATIONS

Errors can be calculated by considering these key parameters:

1. Offset Current (Initial, vs Temperature, vs Supply)
2. Span Error (Initial, vs Temperature, vs Supply)
3. Nonlinearity

Lower errors can readily be obtained by externally adjusting the initial offset and span errors to zero (see Performance Curves).

TYPICAL APPLICATIONS

The XTR110 is ideal for a variety of applications requiring high noise immunity current-mode signal transmission. The precision +10V reference is convenient and can be exciting for bridges and transducers. Selectable ranges make it very useful as a precision programmable current source. The compact design and low price of the XTR110 allow versatility with a minimum of external components and design engineering expense.

Figures 7 through 12 show typical applications of the XTR110.

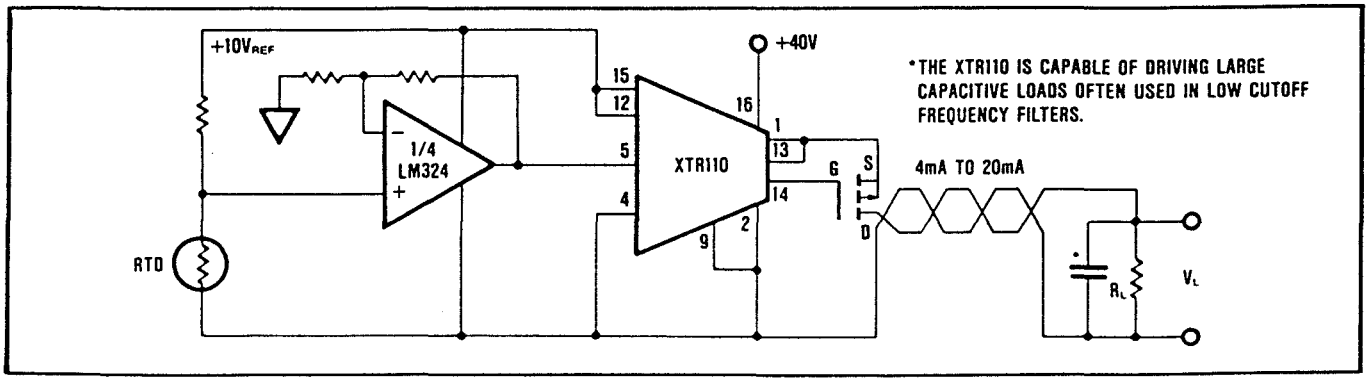


FIGURE 7. 4mA to 20mA Single-Supply RTD Transmitter.

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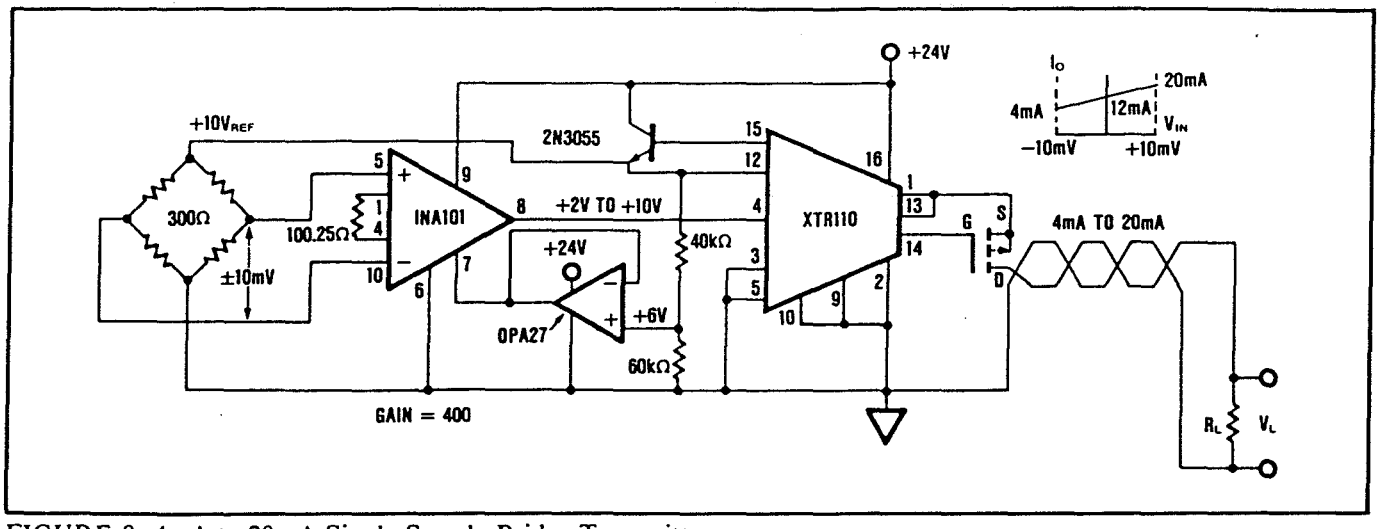


FIGURE 8. 4mA to 20mA Single-Supply Bridge Transmitter.

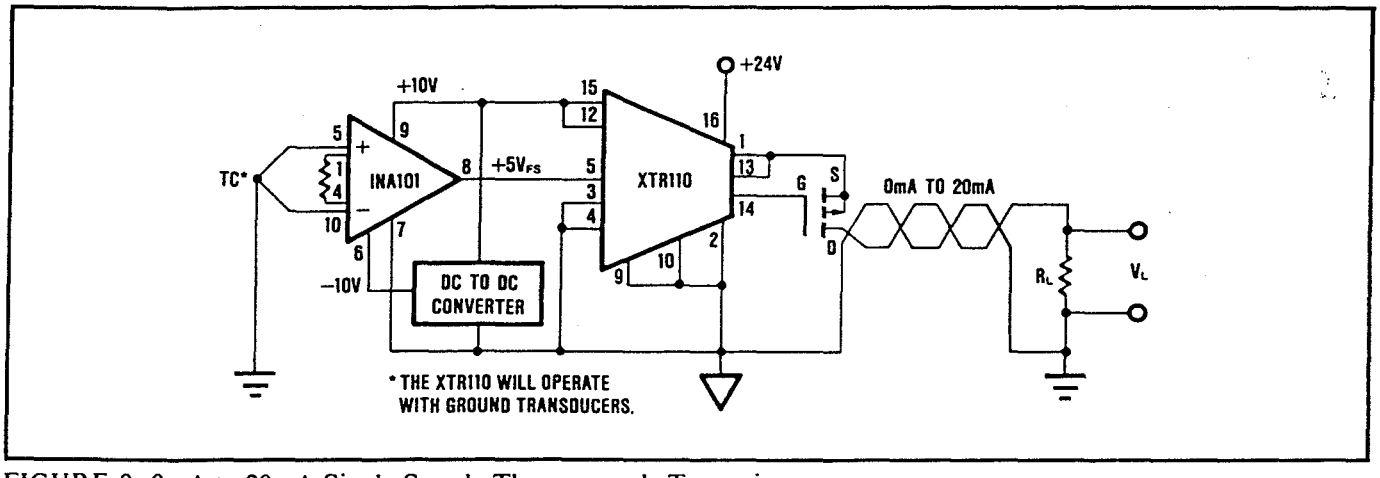


FIGURE 9. 0mA to 20mA Single-Supply Thermocouple Transmitter.

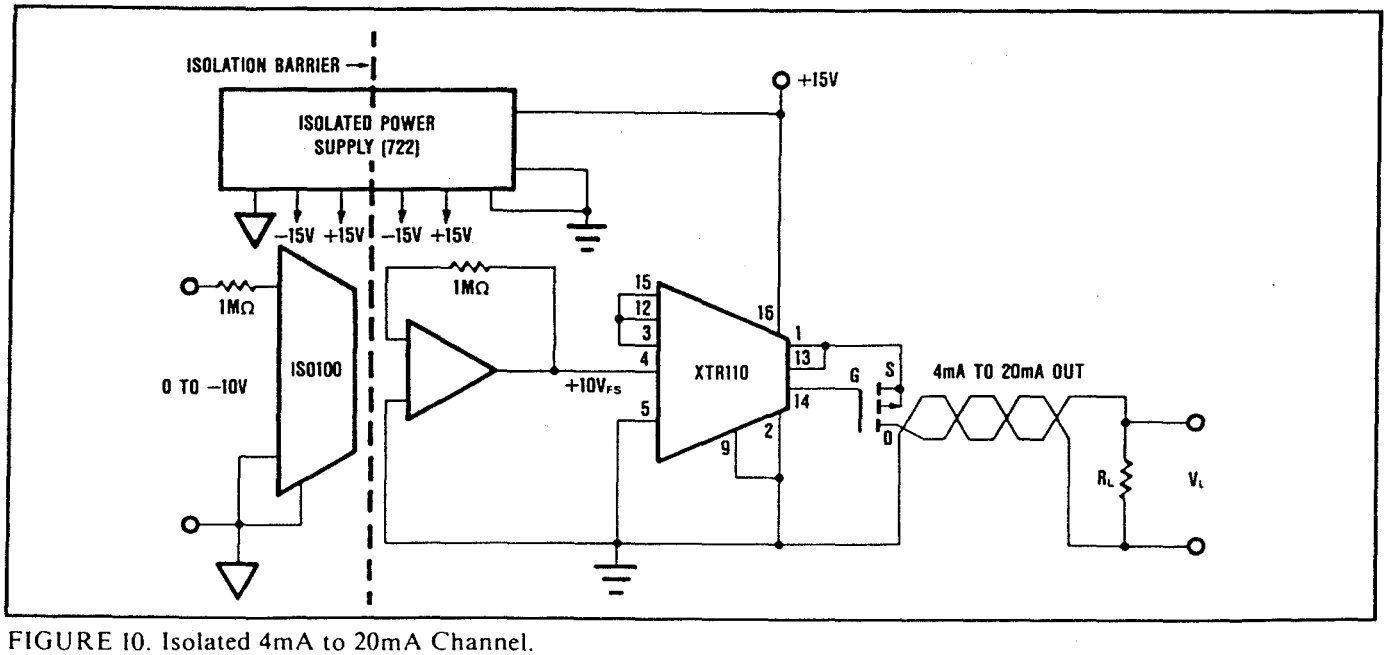


FIGURE 10. Isolated 4mA to 20mA Channel.

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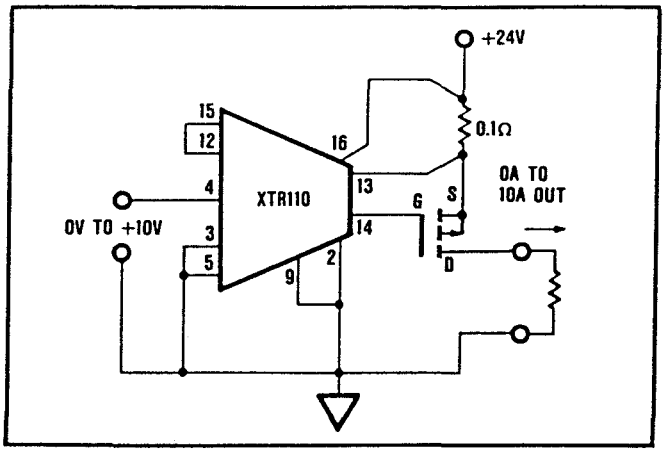


FIGURE 11. 0A to 10A High Current Voltage-to-Current Converter.

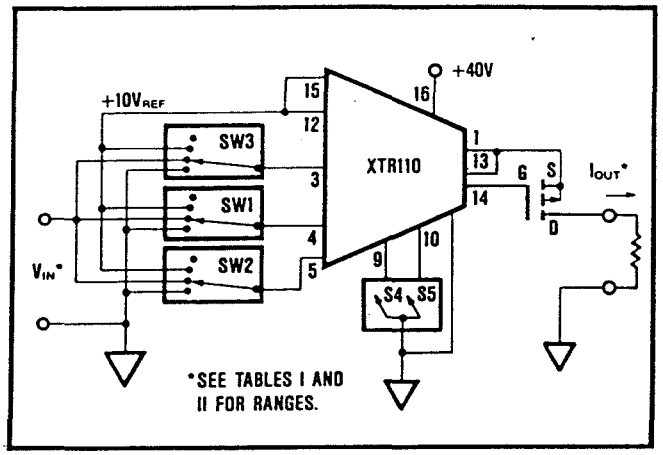


FIGURE 12. Programmable Current Source.

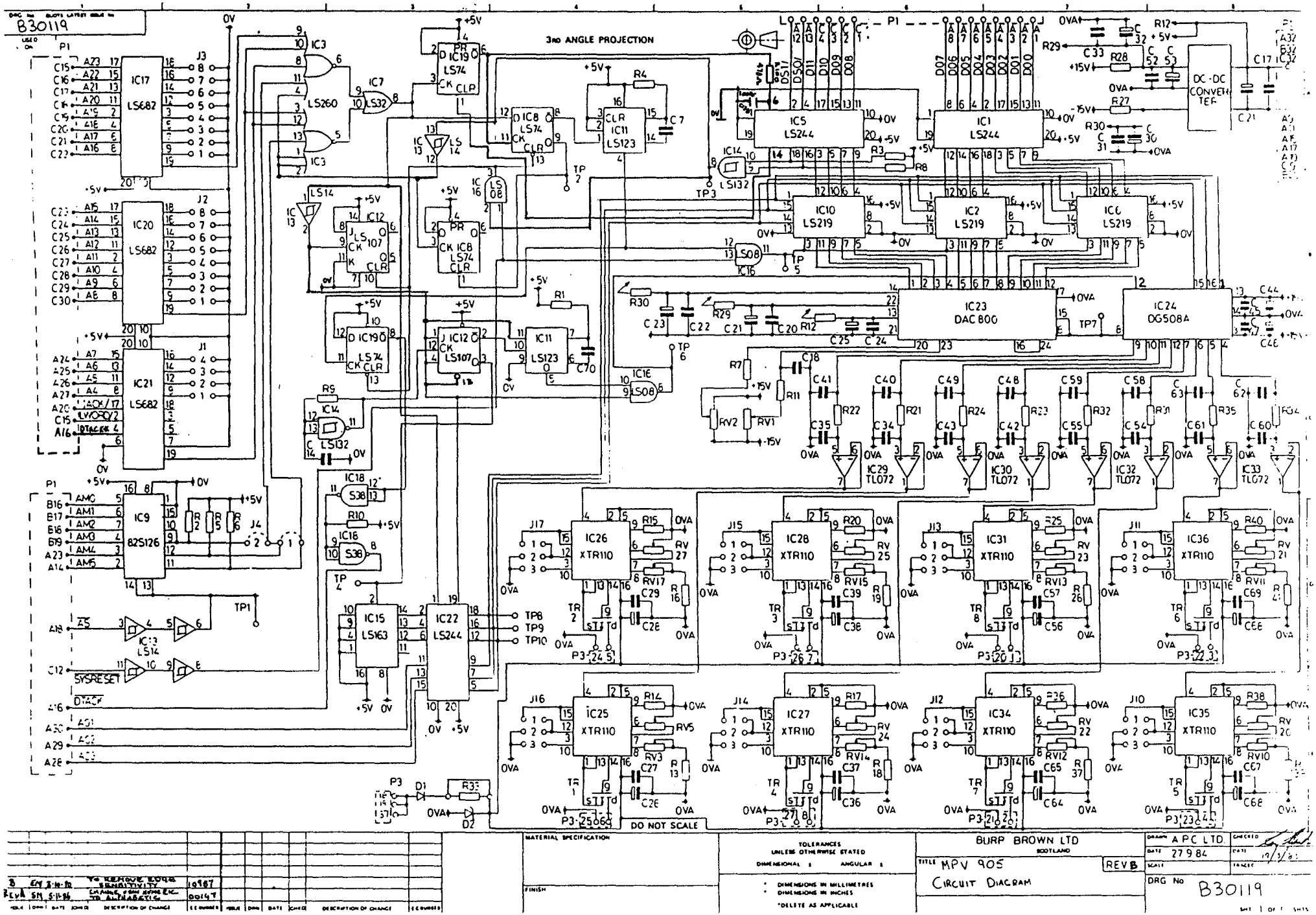
TABLE II. Possible Input/Output Ranges.

R_{span} = 6250Ω (S4) Pin 9 = Open (S5) Pin 10 = Common		R_{span} = 1562.5Ω (S4) Pin 9 = Common (S5) Pin 10 = Open		R_{span} = 1250Ω (S4) Pin 9 = Common (S5) Pin 10 = Common		Connection To Input Pins		
Transfer Ratio (mA/V)	Offset (mA)	Transfer Ratio (mA/V)	Offset (mA)	Transfer Ratio (mA/V)	Offset (mA)	(S3) Pin 3	(S1) Pin 4	(S2) Pin 5
1.3[2]	0	5.2	0	6.5	0	Input	Input	Input
1.22	0	4.88	0	6.10	0	Open	Input	Input
1.2	0	4.8	0	6	0	Common	Input	Input
1.2	1	4.8	4	6	5	10V	Input	Input
1.066	0	4.26	0	5.33	0	Common	Open	Input
1.066	1.33	4.26	5.33	5.33	6.66	10V	Open	Input
1	0	4	0	5	0	Input	Input	Open
0.9	0	3.6	0	4.5	0	Input	Common	Input
0.8	0	3.2	0	4	0	Common	Common	Input
0.8	1	3.2	4	4	5	10V	Common	Input
0.8	4	3.2	16	4	20	Common	10V	Input
0.8	5	3.2	20	4	25	10V	10V	Input
0.5	0	2	0	2.5	0	Input	Input	Common
0.5	8	2	32[3]	2.5	40[3]	Input	Input	10V
0.4	0	1.6	0	2	0	Common	Input	Common
0.4	1	1.6	4	2	5	10V	Input	Common
0.4	8	1.6	32[3]	2	40[3]	Common	Input	10V
0.4	9	1.6	36[3]	2	45[3]	10V	Input	10V
0.2	0	0.8	0	1	0	Input	Common	Open
0.2	8	0.8	32[3]	1	40[3]	Input	10V	Open
0.13	0	0.53	0	0.66	0	Input	Open	Common
0.13	10.66	0.53	42.66[3]	0.66	53.33[3]	Input	Open	10V
0.1	0	0.4	0	0.5	0	Input	Common	Common
0.1	4	0.4	16	0.5	20	Input	10V	Common
0.1	8	0.4	32[3]	0.5	40[3]	Input	Common	10V
0.1	12	0.4	48[3]	0.5	60[3]	Input	10V	10V

NOTES: (1) Maximum rated output current = 25mA for linear operation. Performance on nonstandard ranges not guaranteed. (2) Example: For a 1.3mA/V transfer ratio and a 0mA offset, the output will be 13mA full scale for an input of 10V full scale. (3) Maximum rated output current = 40mA with internal resistor R_s.

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APPENDIX A

VMEbus BACKPLANE CONNECTORS AND VME BOARD CONNECTORS

INTRODUCTION

This appendix identifies the VMEbus backplane J1/P1 connector pin assignments, and which ones are used on the MPV905 Series. The following table lists the pin assignments by pin number order. (The connector consists of three rows of pins labeled rows A, B, and C.)

J1/P1 Pin Assignments

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	D00	BBSY* (1)	D08
2	D01	BCLR* (1)	D09
3	D02	ACFAIL* (1)	D10
4	D03	BGOIN* (2)	D11
5	D04	BGOOUT* (2)	D12 (1)
6	D05	BG1IN* (3)	D13 (1)
7	D06	BG1OUT* (3)	D14 (1)
8	D07	BG21N* (4)	D15 (1)
9	GND	BG2OUT* (4)	GND
10	SYSCLK (1)	BG3IN* (5)	SYSFAIL* (1)
11	GND	BG3OUT* (5)	BERR* (1)
12	DS1*	BRO* (1)	SYSRESET*
13	DSO*	BR1* (1)	LWORD*
14	WRITE* (1)	BR2* (1)	AM5
15	GND	BR3* (1)	A23
16	DTACK*	AMO	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK (1)	A17
22	IACKOUT*	SERDAT (1)	A16
23	AM4	GND	A15
24	A07	IRQ7* (1)	A14
25	A06	IRQ6* (1)	A13
26	A05	IRQ5* (1)	A12
27	A04	IRQ4* (1)	A11
28	A03	IRQ3* (1)	A10
29	A02	IRQ2* (1)	A09
30	A01	IRQ1* (1)	A08
31	-12V (1)	+5V STDBY (1)	+12V (1)
32	+5V	+5V	+5V

NOTE:

(1) Indicates signals used by MPV905 Series and not connected on board.

(2) Signals connected together on Board MPV905 Series

(3) Signals connected together on Board MPV905 Series

(4) Signals connected together on Board MPV905 Series

(5) Signals connected together on Board MPV905 Series

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The product may have been damaged during shipment. Ensure that any damage is reported to the carrier and to your supplier as soon as possible after receipt. Keep all the packing materials, which may be required to assist in investigating the cause of the damage.

In the event of a failure requiring a product to be returned for repair or replacement, please proceed as follows. This will ensure that the time to repair or replace a faulty product is minimised. It is essential to provide the following information (preferably by Fax or other written means), whether or not the board is still under Warranty. This will help Pentland Systems to deal with the unit as quickly and effectively as possible. Please include a copy of this information with the returned product.

Before any product is returned, a Pentland Authorised Return (PAR) number should be obtained from the original supplier. Products should be returned in their original packing via the supplier from whom they were purchased. Pentland Systems will issue PAR numbers within 24 hours of receiving a request supported by the required information. Failure to supply sufficient information or to apply for a PAR number prior to return will cause delays.

INFORMATION REQUIRED PRIOR TO RETURN

1) The name and full address of the Company returning the product.

2) The name, telephone and fax numbers of a Technical Contact familiar with the reason for return.

3) The Product type (eg MPV901), its serial number (eg X12345), the name of the original Supplier and the date of purchase (if known).

4) Whether the product is to be returned Under Warranty. If so, specify if it is a New Product.

5) A complete description of the fault condition. This should include the precise symptoms of the fault plus all relevant and useful information concering the system the product is used in.

Please note:

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The product must be returned in its original packing, or be carefully protected in such a way as to avoid mechanical and electrostatic damage.

Use outwith the published specification and any unauthorised modification or repair will render the warranty void and may result in delays and additional repair costs.

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