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MPV920 Digital Input Board

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MPV 920

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MPV920 OPERATING MANUAL

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1- INTRODUCTION

1.1 ABOUT THIS MANUAL

The MPV920 Isolated Digital I/O Board from Pentland Systems, interfaces directly to the VMEbus and provides the user with 64 inputs arranged in 8 blocks of 8 channels each.

This manual includes a full description of the features of the MPV920, and instructions on how to configure, install and operate the board. Example programs are provided to illustrate the use of an MPV920 in a standard VMEbus system.

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GENERAL DESCRIPTION

2.1 INTRODUCTION

Chapter 2 provides a brief description of the MPV920, and includes a summary of its key features and a full technical specification.

2.2 KEY FEATURES

- Inputs can withstand voltages up to 1500Vrms, or 600V DC applied continuously
- Available in 24V and 5V versions
- Four 24 bit timers
- Debounce protection
- Wide range of compatible I/O racks are available

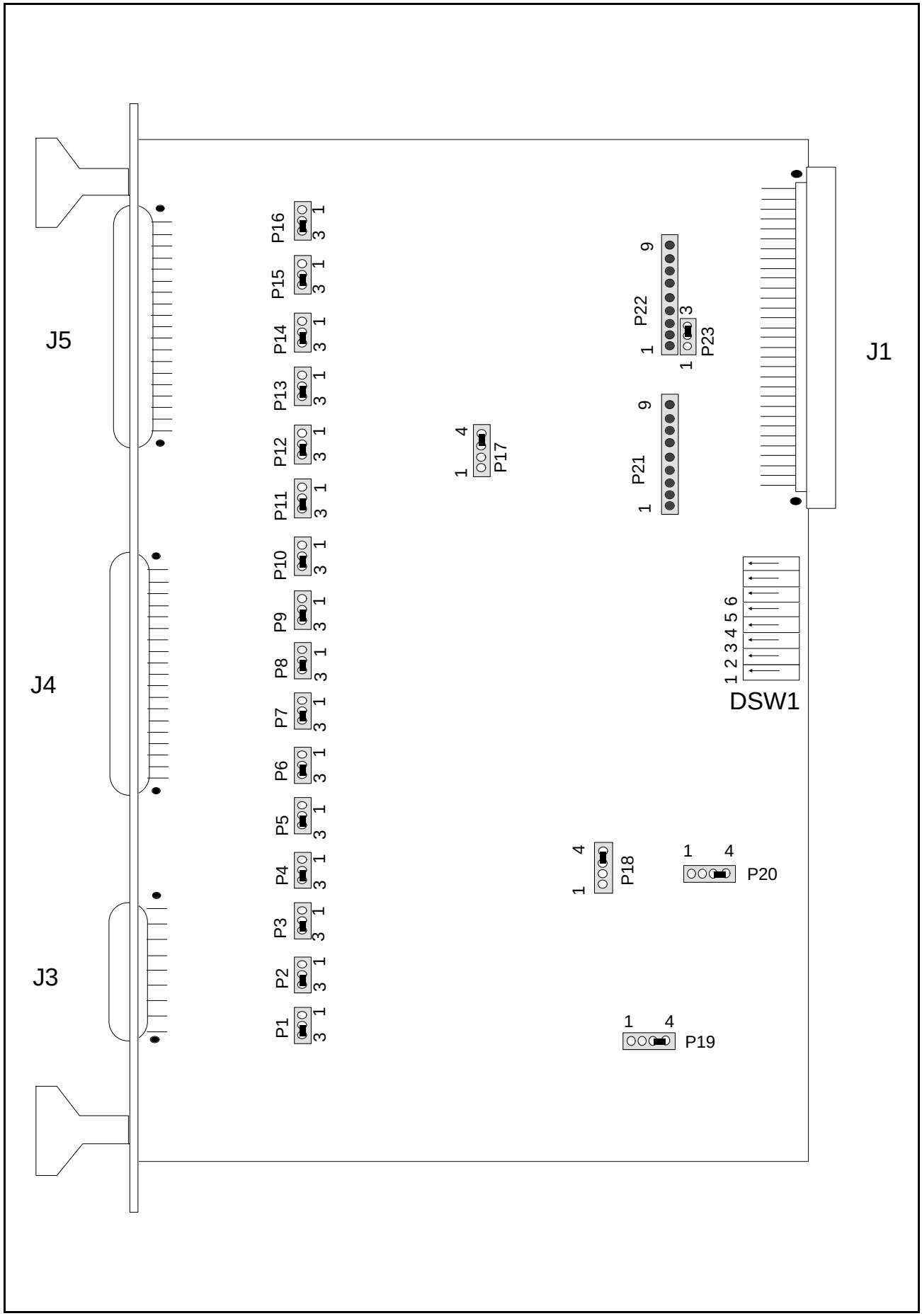
2.3 DESCRIPTION OF THE MPV920

The MPV920 is one in a family of boards designed for applications requiring high channel-count, opto-isolated, digital I/O on the VMEbus. They are each supplied on a single 6U card and are electrically and mechanically compatible with the VMEbus.

All the inputs are extremely well protected against voltage surges and each is able to withstand at least 1500V for 1 minute without damage. The boards can be interfaced using Pentlands industrial standard I/O racks which offer excellent flexibility when connecting to the real world.

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Figure 2.1 MPV920 Board Layout



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2.4 DESCRIPTION OF JUMPERS, CONNECTORS AND SWITCHES

Figure 2.2 shows the location of all the jumpers connectors and switches on the MPV920, Table 2.1 provides a brief description of each device.

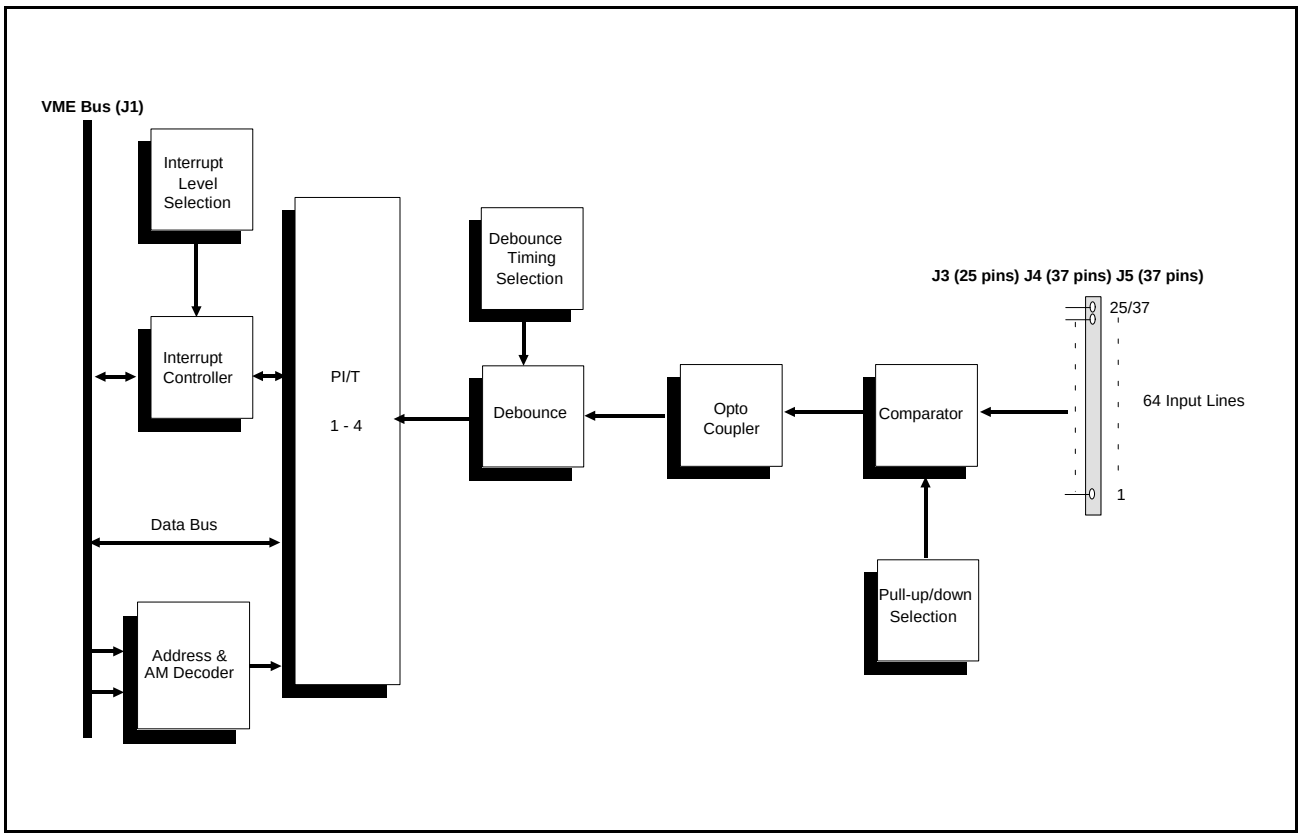
Table 2.1 Jumpers, Connectors and Switches

DESCRIPTION	FUNCTION
J1	VMEbus interface connector
J3	Inputs connector (input 49 - 64)
J4	Inputs connector (input 25 - 48)
J5	Inputs connector (input 1 - 24)
P1 - P16	Configures the inputs to close to either ground or to the supply voltage
P17 - P20	Input time delay selection
P21, P22	Interrupt level selection
P23	Addressing mode selection
DSW1	Board base address selection

2.5 MPV920 BLOCK DIAGRAM

Figure 2.2 shows a functional block diagram of the board.

Table 2.1 Jumpers, Connectors and Switches



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MPV920 Technical Specification

Input Characteristics

Opto-Isolated Inputs : 64 inputs, arranged in 8 banks of 8 channels
Opto-Isolated I/O Power Supply : +24V (MPV920A)
+5V (MPV920C)
Input Connector : 1x D Type - 25 male connector J3
2x D Type - 37 male connector J4 & J5
Input Stage : Pull-up to +24V/ +5* or pull-down to 0V configurable in blocks of 4 input channels
Input ON/OFF Threshold Voltage :
+24V version, MPV920A : Vin(low) = +7.0V, Vin(high) = +9.5V
+5V version, MPV920C : Vin(low) = +2.2V, Vin(high) = +3.2V
Hysteresis :
+24V version, MPV920A : 0.5V
+5V version, MPV920C : 0.1V
Maximum Input Current Drawn On One Channel : ±2.4mA
Input Power Capability : Each bank of four input channels can accept independant power supplies. These power supplies are supplied externally.
Current Drawn Per External Power Supply : 55mA
Input Protection : Protected from input voltage exceeding +24V/ +5V* and less than 0V
Debounce Delays : 70µs, 1ms, 7ms jumper selectable
Minimum detectable Signal Width : 27µs
I/O Isolation Voltage : 1500Vrms for 1 minute

Interrupt and Timer Characteristics

Interrupt Level : Jumper selectable
Interrupt Support : 16 inputs may assert an interrupt request on a rising or falling edge. Software configurable for each input.
Timers : Four 24 bit counters

Power Requirements

+5V at 1A

Environment

Operating Temperature : 0°C to 60°C
Storage requirements : -25°C to +85°C
Relative Humidity : 5% to 90% non-condensing

VME Interface

Board Type : Slave
Addressing Modes : A16
Data Mode : Byte D8 (Odd)

** Dependent on board version*

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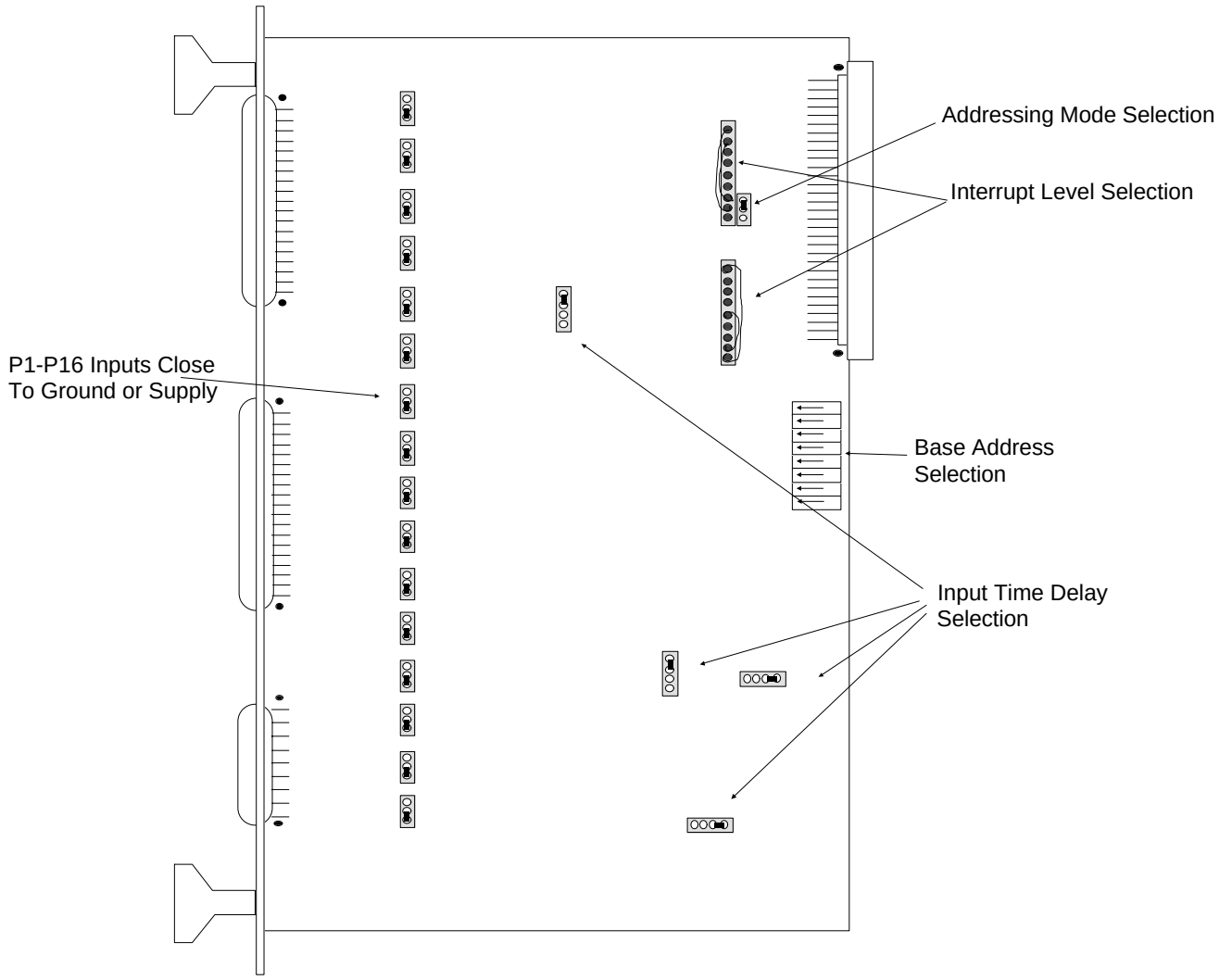
3 - HARDWARE CONFIGURATION

3.1 INTRODUCTION

The **MPV920 Digital Input Board** has a number of user definable options that are selected using a series of jumpers and wire-wraps. Boards are supplied in the configuration shown in table 3.1. Users who do not wish to alter the factory set default settings should proceed to chapter 4 "Cables and Connections."

Figure 3.1 Factory Set Default Settings

Jumper/Switch	Setting
P1-P16	Contacts Closing To The Supply Voltage
P17-P20	Debounce Delay Of 7ms
P21,P22	$\overline{\text{PIRQ}}$ generates a level 5 interrupt TIRQ generates a level 6 interrupt
P23	Address Modifiers not decoded
DSW1	Base Address FF0000H



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3.2 CHANGING THE BASE ADDRESS

The MPV920 occupies 1kbyte of space within the system memory map. It may be located on any 1k boundary within 64k, provided it does not conflict with the location of any other device already installed in the system. The location of the MPV920 is altered by changing the DSW1 switches, shown in figure 3.2.

The board is shipped from the factory with a base address of FF0000H. Only switches SW1 to SW6 inclusive are used to set the base address.

Table 3.2 shows the correspondence between the address line sand the DSW1 switches.

Table 3.2 summaries the position of the switches and the resulting base address of the MPV920. Switching to the ON position sets the corresponding address bit to a zero (0).

Figure 3.2 P23 Setting

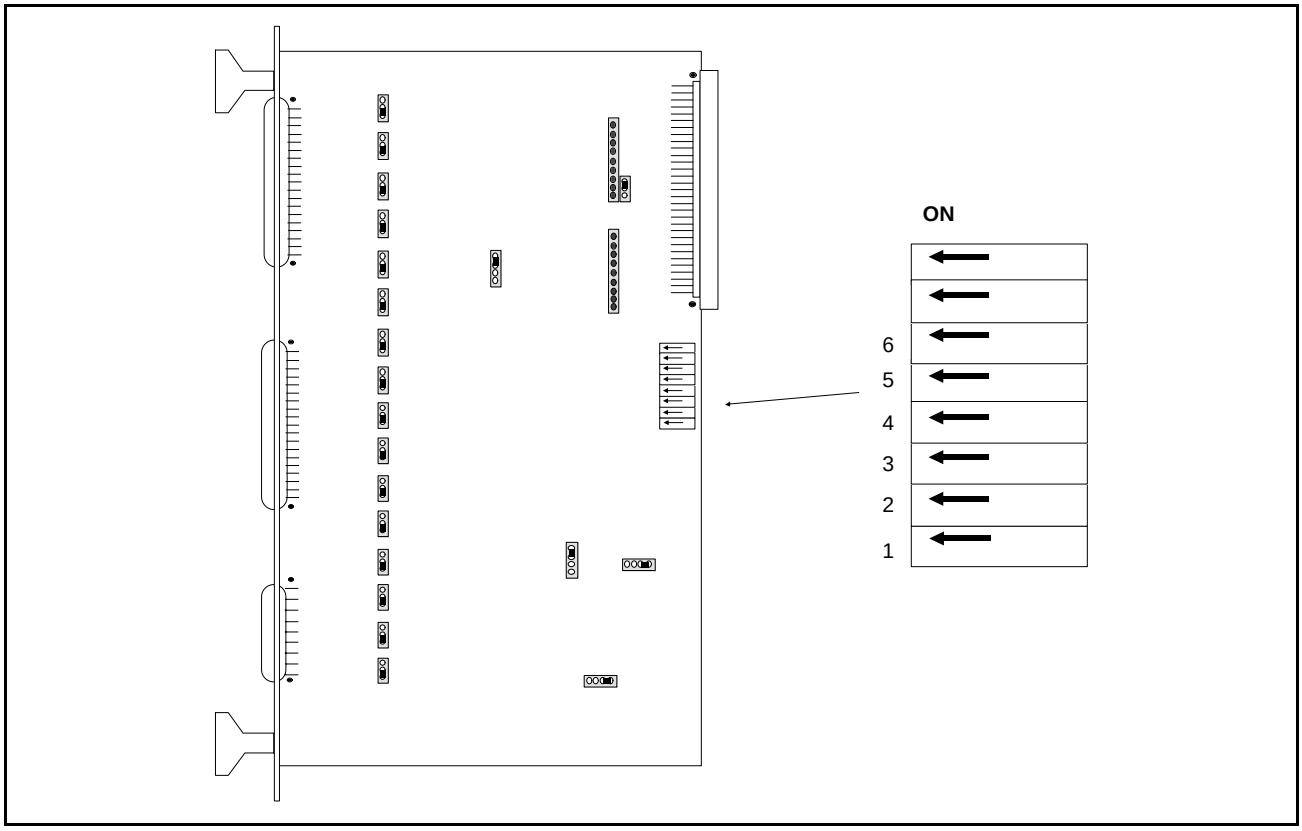


Table 3.2 Summary Of Base Address Options

SW1 (A15)	**SW2** (A14)	**SW3** (A13)	**SW4** (A12)	**SW5** (A11)	**SW6** (A10)	**BASE ADDRESS**
ON	ON	ON	ON	ON	ON	FF0000H
ON	ON	ON	ON	ON	OFF	FF0400H
ON	ON	ON	ON	OFF	ON	FF0800H
ON	ON	ON	ON	OFF	OFF	FF0C00H
ON	ON	ON	OFF	ON	ON	FF1000H

and so on until.....

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SW1	SW2	SW3	SW4	SW5	SW6	BASE ADDRESS
OFF	OFF	OFF	ON	OFF	OFF	FFEC900H
OFF	OFF	OFF	OFF	ON	ON	FFF000H
OFF	OFF	OFF	OFF	ON	OFF	FFF400H
OFF	OFF	OFF	OFF	OFF	ON	FFF800H
OFF	OFF	OFF	OFF	OFF	OFF	FFFC00H

3.3 ADDRESS MODIFIER DECODER

With jumper P23 inserted between pin 1 and pin 2 the board decodes address modifiers. In the short addressing mode the following two modifiers are allowed.

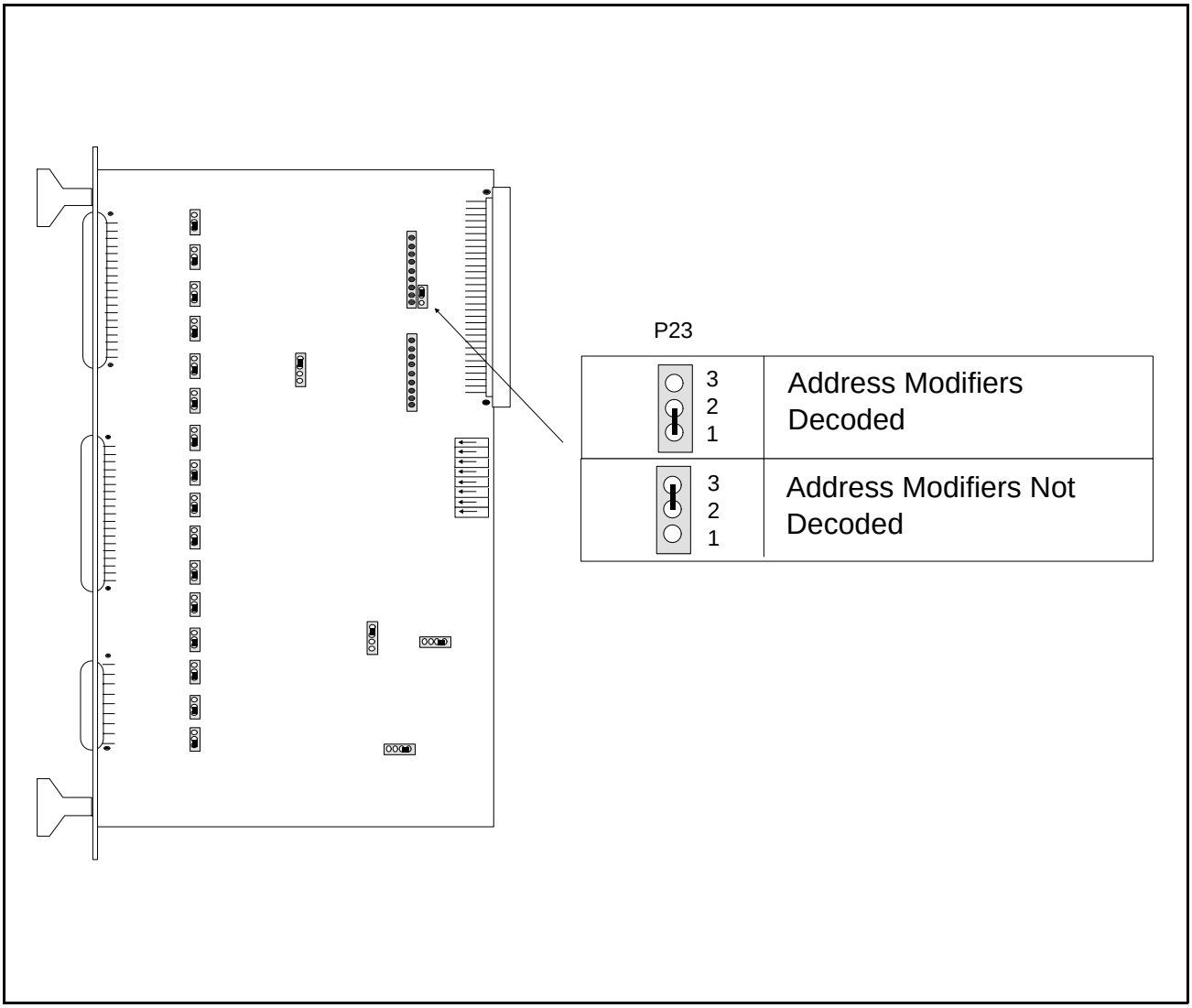
Code $2DH - Short Supervisory I/O Access

Code $29H - Short Non-Privileged I/O Access

With the jumper between pin 2 and pin 3 address modifiers are not decoded.

Figure 3.3 shows the possible settings of jumper P23.

Figure 3.3 Address Modifier Decoding



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3.4 CONFIGURATION OF THE INPUTS

Jumpers P1 to P16 are used to define the setting of the inputs, i.e., if they close to earth or the supply voltage. The input channels are arranged in groups of four. Table 3.3 shows how the input channels and jumpers P1 - P16 are configured.

Figure 3.4 shows the possible options for jumpers P1 - P16.

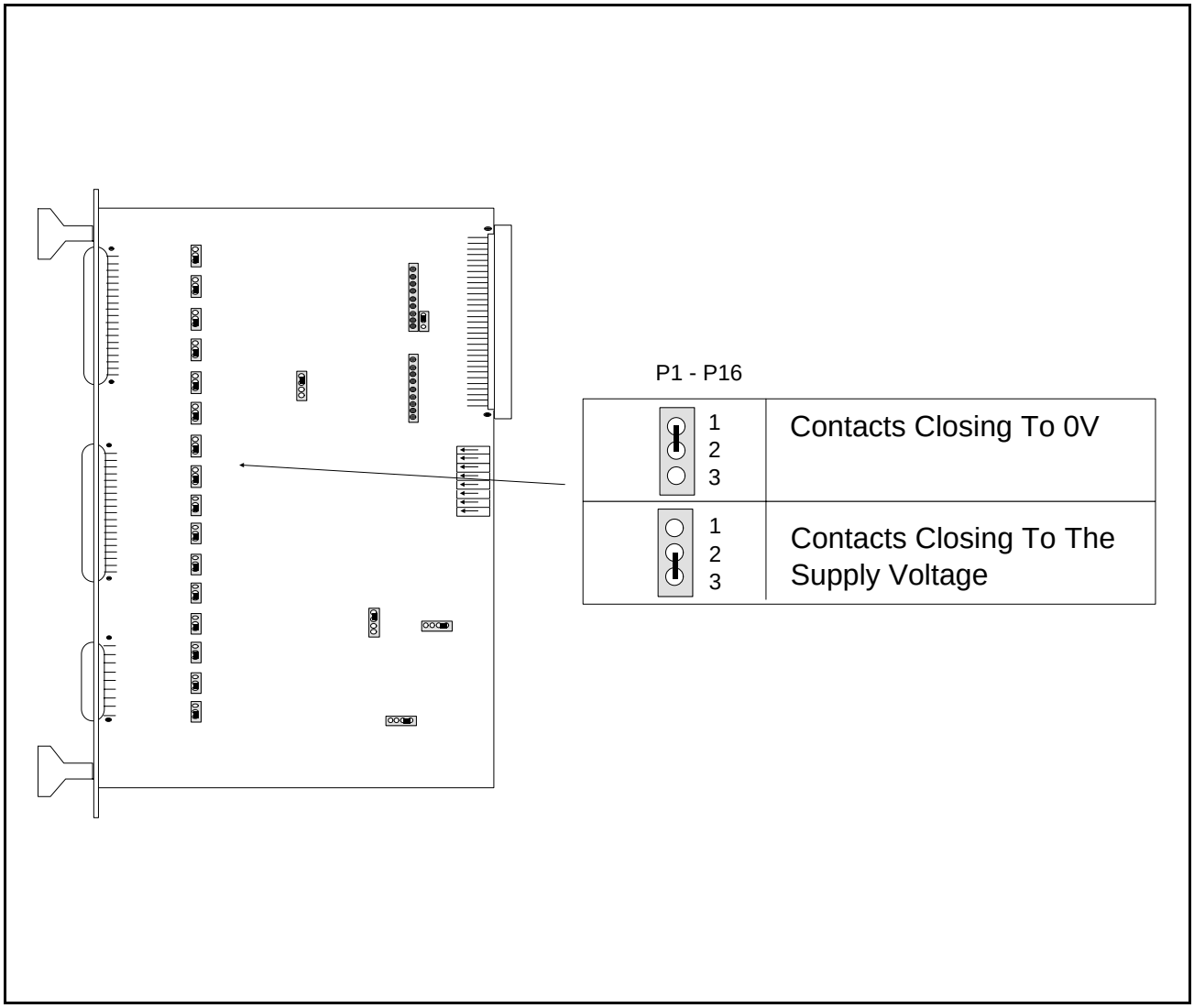
Table 3.3 Jumpers P1 - P16 Input Configuration

GROUP	INPUTS	JUMPER
1	01, 02, 03, 04	P16
2	05, 06, 07, 08	P15
3	09, 10, 11, 12	P14
4	13, 14, 15, 16	P13
5	17, 18, 19, 20	P12
6	21, 22, 23, 24	P11
7	25, 26, 27, 28	P10
8	29, 30, 31, 32	P9
9	33, 34, 35, 36	P8
10	37, 38, 39, 40	P7
11	41, 42, 43, 44	P6
12	45, 46, 47, 48	P5
13	49, 50, 51, 52	P4
14	53, 54, 55, 56	P3
15	57, 58, 59, 60	P2
16	61, 62, 63, 64	P1

Note: The input circuit inverts the signal; a low level (0V) on a PI/T pin corresponds to a high level (Vcc) on the corresponding connector.

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Figure 3.4 Configuration Of The Inputs



3.5 INPUT TIME DELAY

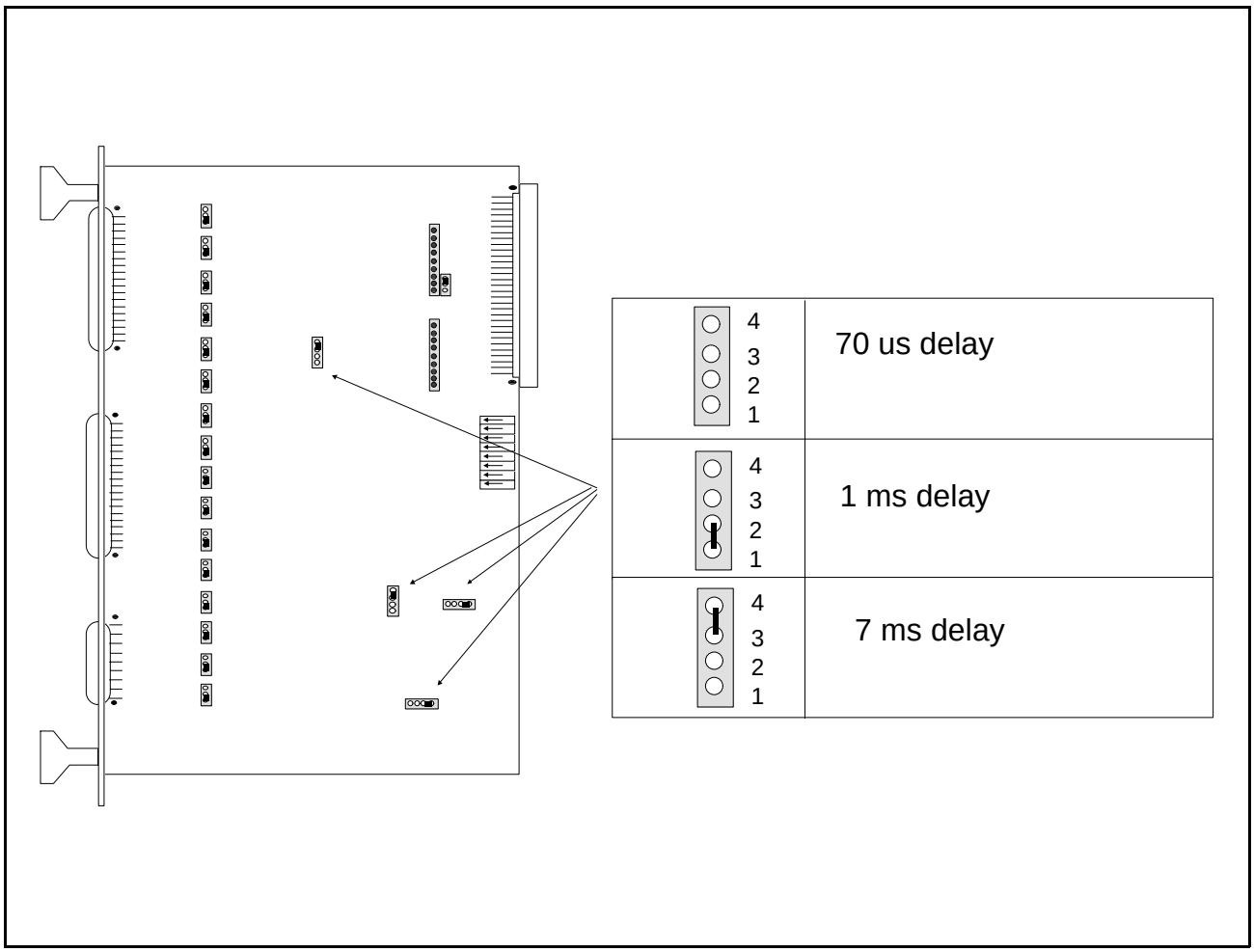
Debounce circuitry is incorporated to generate a delay between the input channels and the inputs to the PI/T's. The time delays are selected via jumpers P17 - P20. Table 3.4 shows the relationship between jumpers and the input channels. Figure 3.5 shows the time delay options available and the location of the jumpers.

Table 3.4 Relation Of Channels To Jumpers

JUMPER	INPUTS
P17	Input 01 - Input 16
P18	Input 17 - Input 32
P20	Input 33 - Input 48
P19	Input 49 - Input 64

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Figure 3.5 Debounce Time Delay selection



3.6 INTERRUPT LEVEL SELECTION

Sixteen of the inputs, if enabled, and the four timers can generate interrupts on the MPV920. Jumpers P21 and P22 select the level of the interrupt request asserted on the VMEbus (from 1 to 7). The input interrupt is designated the PIRQ interrupt, and the timer interrupt is called the TIRQ

3.6.1 $\overline{\text{PIRQ}}$ INTERRUPT

Table 3.5 shows how to select the required level of interrupt.

Table 3.5 PIRQ Interrupt

JUMPER		VME INTERRUPT LEVEL
P21	P22	GENERATED BY PIRQ*
1-3	8-1	7
1-5	8-2	6
1-9	8-3	5
1-8	8-4	4
1-7	8-5	3
1-6	8-6	2
1-4	8-7	1

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3.6.2 $\overline{\text{TIRQ}}$ INTERRUPT

Table 3.5 shows how to select the required level of interrupt.

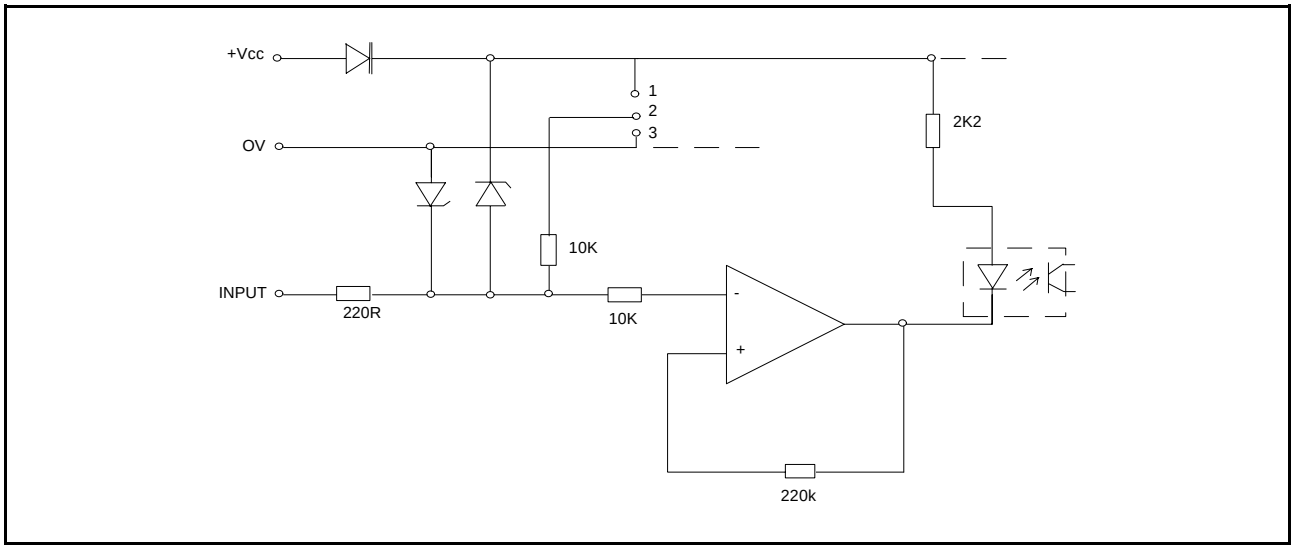
Table 3.5 TIRQ Interrupt

JUMPER		VME INTERRUPT LEVEL
P21	P22	GENERATED BY TIRQ*
2-3	9-1	7
2-5	9-2	6
2-9	9-3	5
2-8	9-4	4
2-7	9-5	3
2-6	9-6	2
2-4	9-7	1

3.7 INPUT CIRCUIT CONFIGURATION

The input circuitry for the MPV920 is detailed in Figure 3.6.

Figure 3.6 Input Circuit Configuration



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4 - CABLES AND CONNECTIONS

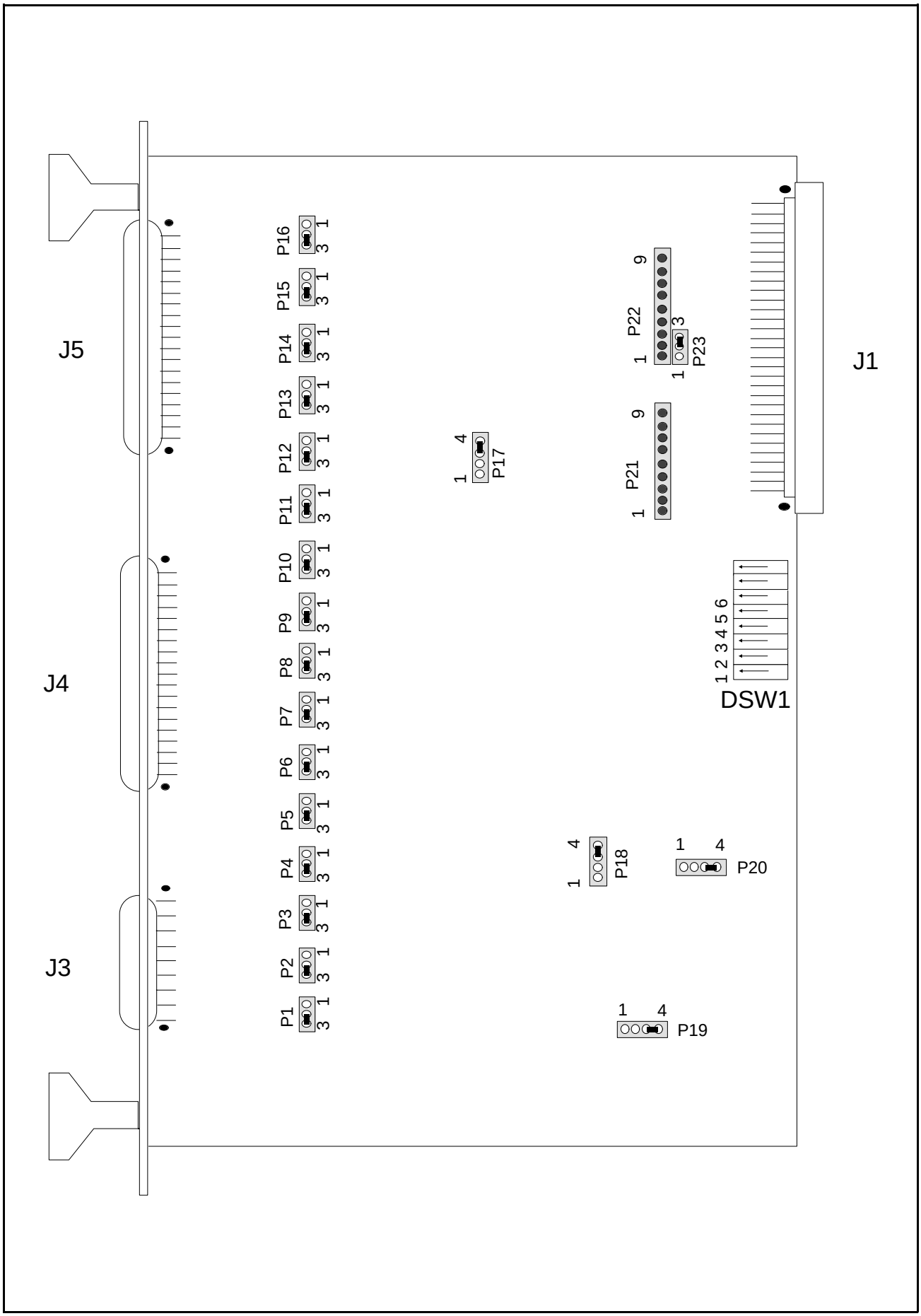
4.1 CONNECTING THE MPV920

Communication between the MPV920 and the VMEbus is performed via the J1 connector on the rear of the board. To install the MPV920 in the system, carefully align connectors J1 with the corresponding J1 connectors on the VMEbus backplane and press firmly home.

Ensure that power to the VMEbus system is turned off before installing the MPV920. The MPV920 is sensitive to the build-up of static electricity, therefore normal anti-static precautions should be observed when handling the board.

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Figure 4.1 Location Of Connectors



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4.2 CONNECTOR PIN ASSIGNMENTS

4.2.1 P1 PIN ASSIGNMENT

The 96-way J1 connector on the MPV920 mates with J1 connector on the VMEbus Backplane.

Table 4.1 J1 Pin Assignment

Pin	(a)	(b)	(c)
1	D00	N.C.	N.C.
2	D01	N.C.	N.C.
3	D02	N.C.	N.C.
4	D03	BG0IN*	N.C.
5	D04	BG0OUT*	N.C.
6	D05	BG1IN*	N.C.
7	D06	BG1OUT*	N.C.
8	D07	BG2IN*	N.C.
9	N.C.	BG2OUT*	GND
10	SYSCLK	BG3IN*	N.C.
11	GND	BG3OUT*	N.C.
12	N.C.	N.C.	SYSRESET*
13	DS0*	N.C.	N.C.
14	WRITE*	N.C.	AM5
15	GND	N.C.	A23
16	DTACK*	AM0	A22

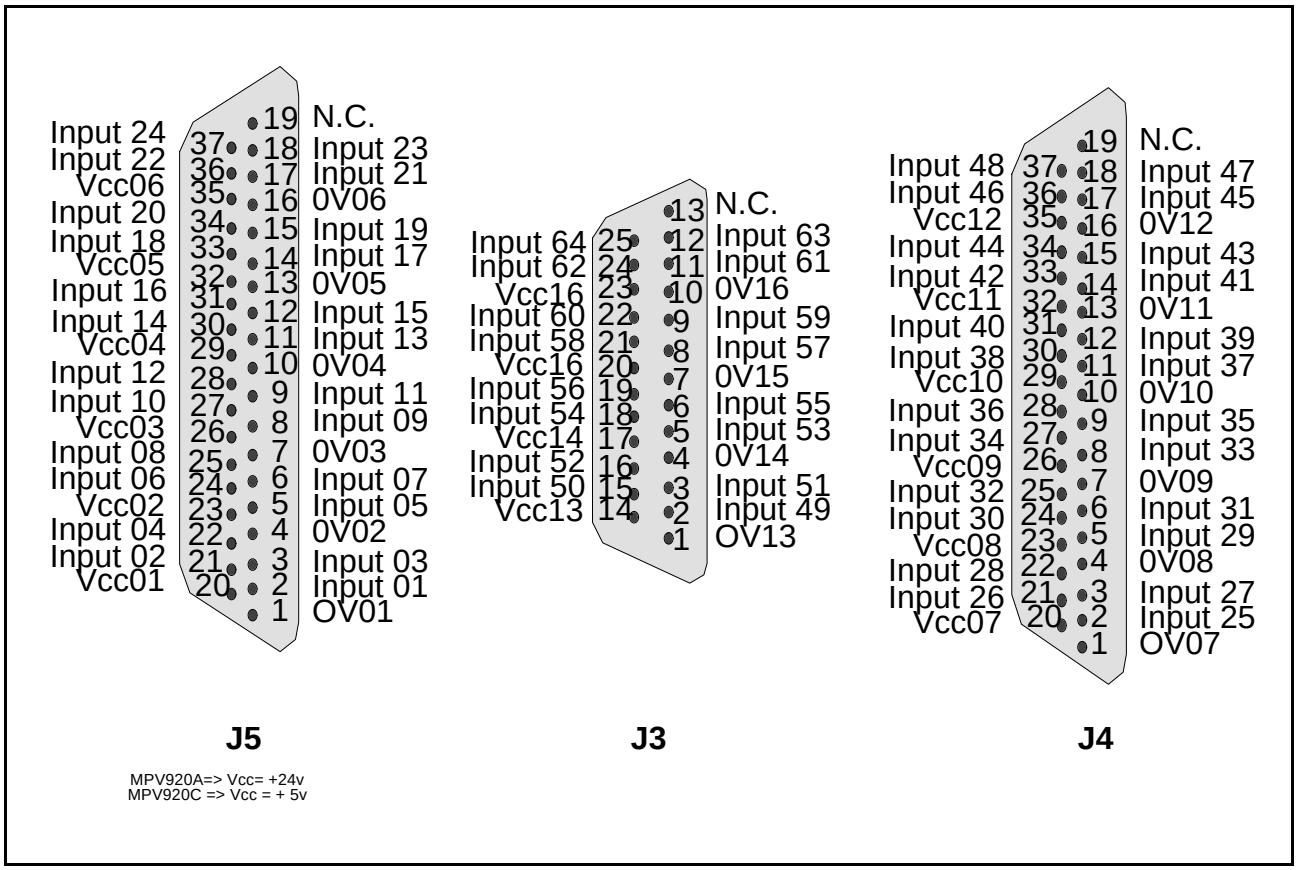
Pin	(a)	(b)	(c)
17	GND	AM1	A21
18	AS*	AM2	A2
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	N.C.	A17
22	IACKOUT*	N.C.	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	N.C.	N.C.	N.C.
32	+5V	+5V	+5V

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4.2.2 DIGITAL INPUT CONNECTIONS (J3, J4 & J5)

Up to 64 digital inputs can be connected to the MPV920. The pin assignments for the three front panel

Figure 4.2 Input Connections



connectors are shown in figure 4.2.

4.2.3 INPUT POWER SUPPLIES

Sixty-four inputs, divided into 16 groups of 4 inputs, are available. For each group of 4 a separate power supply can be connected. Each group will be an independent power supply, table 4.2 shows the assignment of the inputs and their independent power supply.

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Table 4.2 Inputs & Power Supply Configuration

Group	Inputs	Power Supply
1	Input01-Input04	0V 01, Vcc 01
2	Input05-Input08	0V 02, Vcc 02
3	Input09-Input12	0v 03, Vcc 03
4	Input13-Input16	0V 04, Vcc 04
5	Input17-Input20	0V 05, Vcc 05
6	Input21-Input24	0V 06, Vcc 06
7	Input25-Input28	0V 07, Vcc 07
8	Input29-Input32	0V 08, Vcc 08
9	Input33-Input36	0V 09, Vcc 09
10	Input37-Input40	0V 10, Vcc 10
11	Input41-Input44	0V 11, Vcc 11
12	Input45-Input48	0V 12, Vcc 12
13	Input49-Input52	0V 13, Vcc 13
14	Input53-Input56	0V 14, Vcc 14
15	Input57-Input60	0V 15, Vcc 15
16	Input61-Input64	0V 16, Vcc 16

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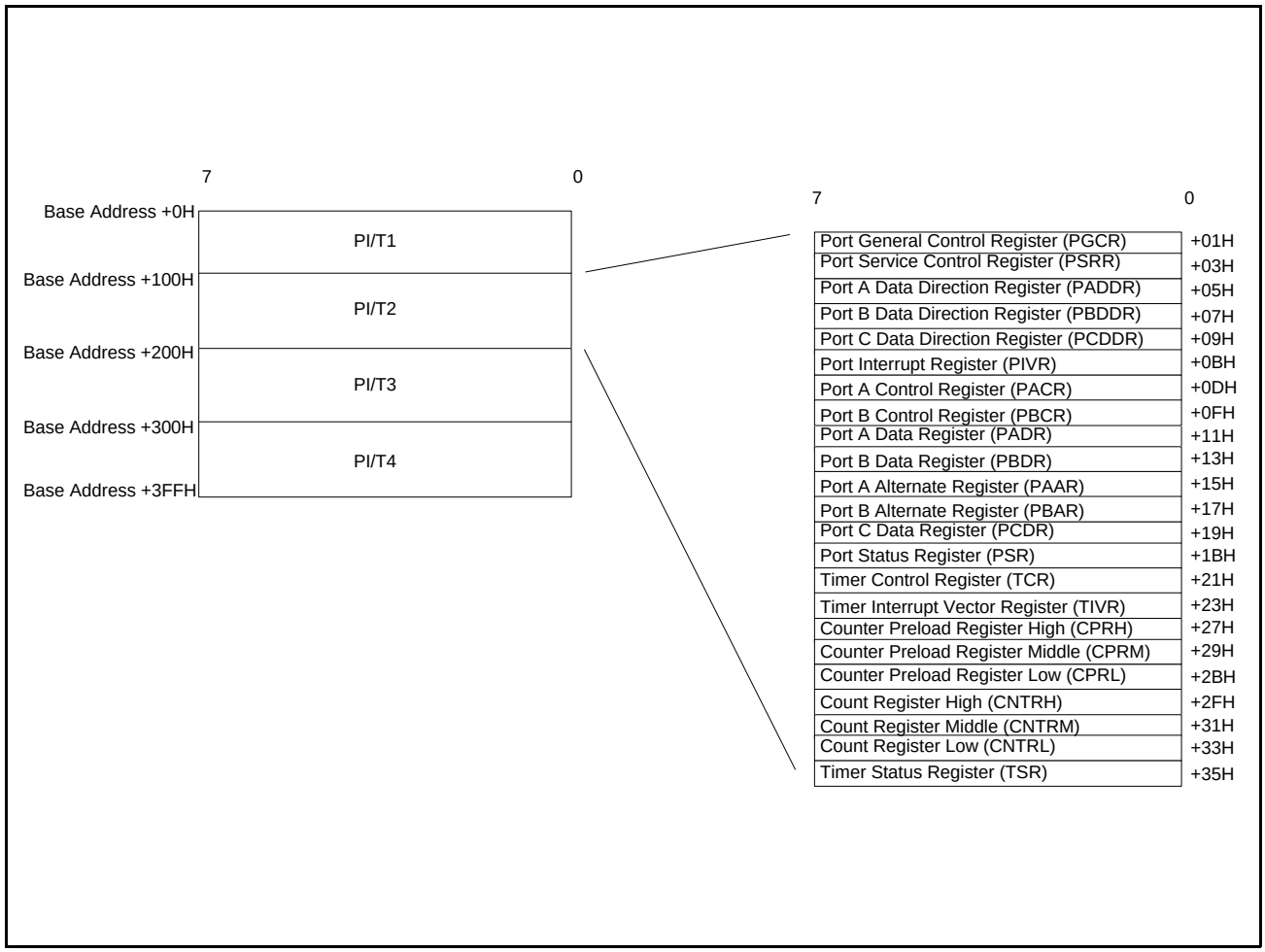
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5- SOFTWARE CONFIGURATION

5.1 INTRODUCTION

The MPV920 occupies 1kbyte of locations within the VME address space. Figure 5.1 shows a memory map of the board. The inputs to the board are controlled by four MC68230 Parallel Interface/Timers (PI/T's). It is important that the PI/T's are initialised correctly, see chapter 6 for example programs and the MC68230 data sheet provided.

Figure 5.1 MPV920 Memory Map



5.2 MC68230

The location of the four PI/T's is also shown in figure 5.1, their locations are also shown in table 5.1 below. VME address lines A08 and A09 are used to identify the individual PI/T's.

Table 5.1 PI/T Memory Locations

PI/T's	OFFSET
1	0
2	100H
3	200H
4	300H

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5.3 MPV920 INPUTS

The configuration of the inputs to the MC68320 is shown in the table 5.2 and table 5.3. VME address lines A01 to A05 identify the specific registers within the PI/T's.

Table 5.2 PI/T Registers

INPUTS	REGISTER	PI/T's	OFFSET
Input 01 - Input 08	PADR	1	11H
Input 09 - Input 16	PBDR	1	13H
Input 17 - Input 24	PADR	2	111H
Input 25 - Input 36	PBDR	2	113H
Input 37 - Input 42	PADR	3	211H
Input 43 - Input 48	PBDR	3	213H
Input 49 - Input 56	PADR	4	311H
Input 57 - Input 64	PBDR	4	313H

Table 5.3 PI/T Memory Locations

PI/T	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
1	PADR	08	07	06	05	04	03	02	01
1	PBDR	16	15	14	13	12	11	10	09
2	PADR	24	23	22	21	20	19	18	17
2	PBDR	32	31	30	29	28	27	26	25
3	PADR	40	39	38	37	36	35	34	33
3	PBDR	48	47	46	45	44	43	42	41
4	PADR	56	55	54	53	52	51	50	49
4	PBDR	64	63	62	61	60	59	58	57

5.3.1 EXAMPLE

If we wish to read the status of inputs 41-48, these inputs are mapped in register PBDR of PI/T number 3 (see table 5.3). Assuming that the board base address has been set at $FF0400H (switch 1-5 ON and switch 6 OFF), then it is necessary to perform a read cycle at address $FF0613, see below.

$FF0400H	Board Base Address
$ 13H	Address for PBDR Register
$ 200H	Offset PI/T number 3
$FF0613H	

5.4 INPUT GENERATED INTERRUPTS

The 16 inputs listed in table 5.4 are capable of generating interrupts.

The example programs and MC68230 PI/T data sheets describe the interrupt request handling.

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Table 5.4 Input Generated Interrupts

INPUT	REGISTER	**PI/T's**
Input 07	H2	1
Input 08	H1	1
Input 15	H4	1
Input 16	H3	1
Input 23	H2	2
Input 24	H1	2
Input 31	H4	2
Input 32	H3	2
Input 39	H2	3
Input 40	H1	3
Input 47	H4	3
Input 48	H3	3
Input 55	H2	4
Input 56	H1	4
Input 63	H4	4
Input 64	H3	4

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```
ME              equ             2       * Max error put 0 when error will be fixed
```

6.1 GLOBAL ROUTINES

```
public          _s920in         * d0 = group to initialise, return in a0 PIT
                                * base address (port A pit) if a0= non-existing
                                * group into a1 INPUTS handling routine address
```

6.2 MPV920 EQUATES

```
Base Address
Include “base 920.hs”       MPV920 base address declaration

pit1            equ             0                   * offset first  PIT
pit2            equ             $100                * offset second PIT
pit3            equ             $200                * offset third PIT
pit4            equ             $300                * offset fourth PIT

buserve equ     8                       * bus error vector
```

6.3 EQUATES PIT

```
Port Parameter
PP              equ             1                    * 0 = TVM-220
                                                     * 1 = TVM-200 TVM-742 TVM-743 TVM-745

                include "pit.hs"                    * “equates” file for PIT
                cseg
```

6.4 INITIALISE A GROUP OF 16 INPUTS

```
*d0= group to initialise, return into a0 PIT base address
(*port A pit) if a0=0 non-existing group,into al INPUTS handling routine
address

_s920movem.l d1/a6,-(a7)
                move.l          buserve,-(a7)       * save bus error vector
                move.l          a7,a6               * save into a6 stack pointer
                move.l          #berr742,buserve    * set vector non-exis. board routine
                move.l          d0,d1               * compute PIT base address
                lsl.w           #2,d1
                move.l          tapit+ME(pc,d1),a0  * PIT base address
                move.b          #$3f,pgcr(a0)       * mode 0, h12 - h34 enabled
                move.b          #$18,psrr(a0)       * vectorised interrupt
                move.b          #$80,pacr(a0)       * submode 1x
                move.b          #$80,pbcr(a0)       * submode 1x
```


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```
              move.b        #$00,paddr(a0)      * dir. pa = in
              move.b        #$00,pbddr(a0)      * dir. pb = in
              lea           t742in(pc),a1       * INPUTS handling routine

ent920        move.l        (a7)+,buserve
              movem.l (a7)+,d1/a6
              rts

*non-existing inputs handling
berr920 move.l              a6,a7               * restore stack pointer
              lea           920ne(pc),a1        * non-existing board handling routine
              sub.l         a0,a0               * a0=0 ( set unexist. board)
              bra.s         ent920

* PIT address array (each PIT has 16 inputs)
tapit         dc.l base1+pit1,base1+pit2,base1+pit3,base1+pit4
              dc.l base2+pit1,base2+pit2,base2+pit3,base2+pit4
              dc.l base3+pit1,base3+pit2,base3+pit3,base3+pit4
              dc.l base4+pit1,base4+pit2,base4+pit3,base4+pit4
              dc.l base5+pit1,base5+pit2,base5+pit3,base5+pit4
              dc.l base6+pit1,base6+pit2,base6+pit3,base6+pit4
              dc.l base7+pit1,base7+pit2,base7+pit3,base7+pit4
              dc.l base8+pit1,base8+pit2,base8+pit3,base8+pit4
```

6.5 INPUT OF 16 DIGITAL INPUTS

```
* into d0 return the data, into a0 is passed the address
920in         movep.w       padr(a0),d0
              rol.w         #8,d0
*             not.w         d0
              rts
PB                          PA
7 6 5 4 3 2 1               7 6 5 4 3 2 1
```

6.6 INPUT OF 16 DIGITAL INPUTS OF NON-EXISTING BOARD

```
920           moveq.l #-1,d0                    * return all inputs to 1
              rts

              end
```


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