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MPV921 Digital Input/Output Board

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MPV 921

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MPV921 OPERATING MANUAL

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1- INTRODUCTION

1.1 ABOUT THIS MANUAL

The MPV921 Isolated Digital I/O Board from Pentland Systems, interfaces directly to the VMEbus and provides the user with 16 inputs arranged in 4 blocks of 4 channels, and 64 outputs arranged in 8 blocks of 8 channels each.

This manual includes a full description of the features of the MPV921, and instructions on how to configure, install and operate the board. Example programs are provided to illustrate the use of an MPV921 in a standard VMEbus system.

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GENERAL DESCRIPTION

2.1 INTRODUCTION

Chapter 2 provides a brief description of the MPV921, and includes a summary of its key features and a full technical specification.

2.2 KEY FEATURES

- Outputs can withstand upto 1500Vrms
- Inputs can withstand voltages up to 1500Vrms, or 600V DC applied continuously
- Available in 24V and 5V versions
- Four 24 bit timers
- Debounce protection
- Wide range of compatible I/O racks are available
- User specified watchdog timer

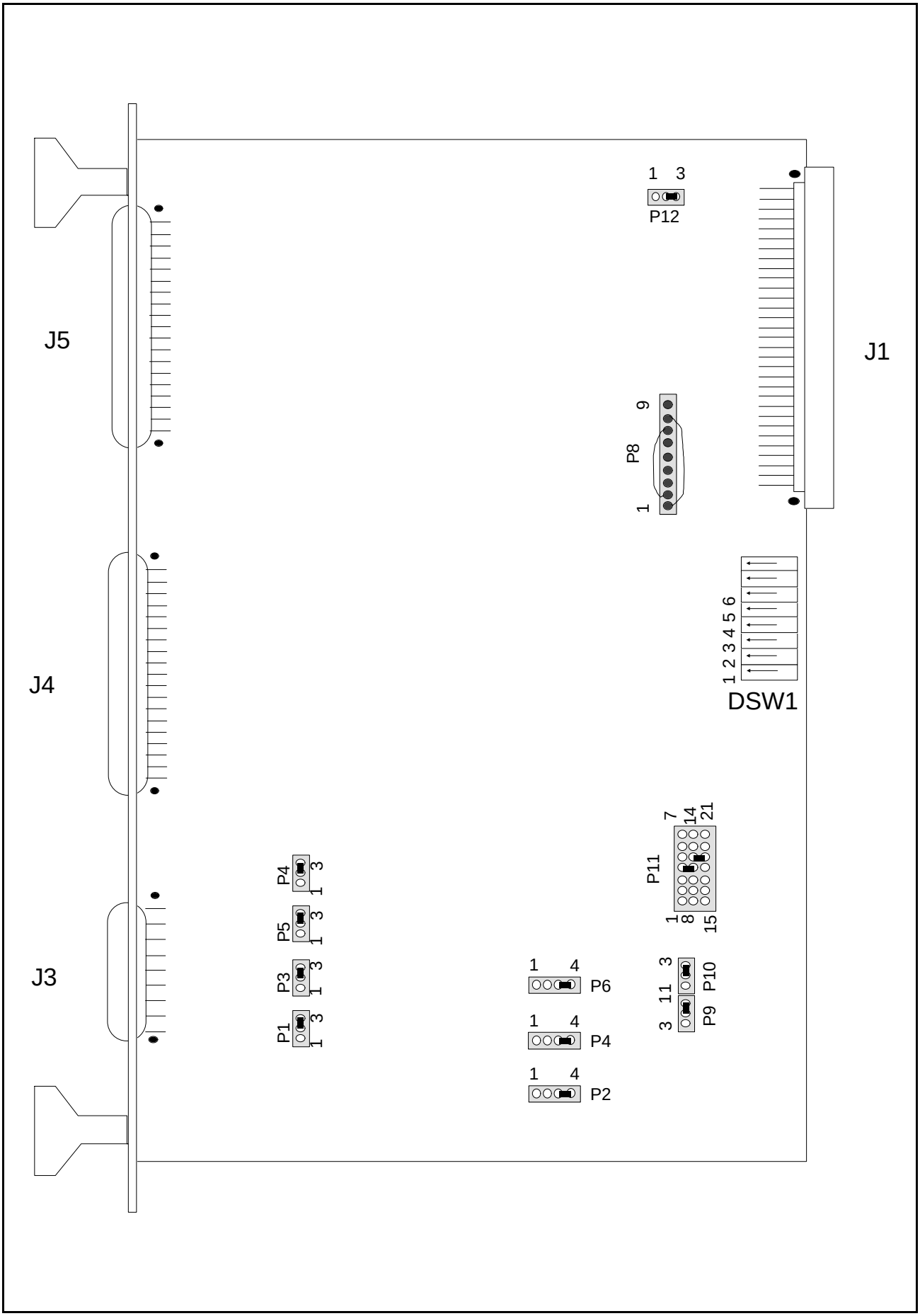
2.3 DESCRIPTION OF THE MPV921

The MPV921 is one in a family of boards designed for applications requiring high channel-count, opto-isolated, digital I/O on the VMEbus. They are each supplied on a single 6U card and are electrically and mechanically compatible with the VMEbus.

All the inputs are extremely well protected against voltage surges and each is able to withstand at least 1500V for 1 minute without damage. The boards can be interfaced using Pentlands industrial standard I/O racks which offer excellent flexibility when connecting to the real world.

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Figure 2.1 MPV920 Board Layout



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2.4 DESCRIPTION OF JUMPERS, CONNECTORS AND SWITCHES

Figure 2.2 shows the location of all the jumpers connectors and switches on the MPV921, Table 2.1 provides a brief description of each device.

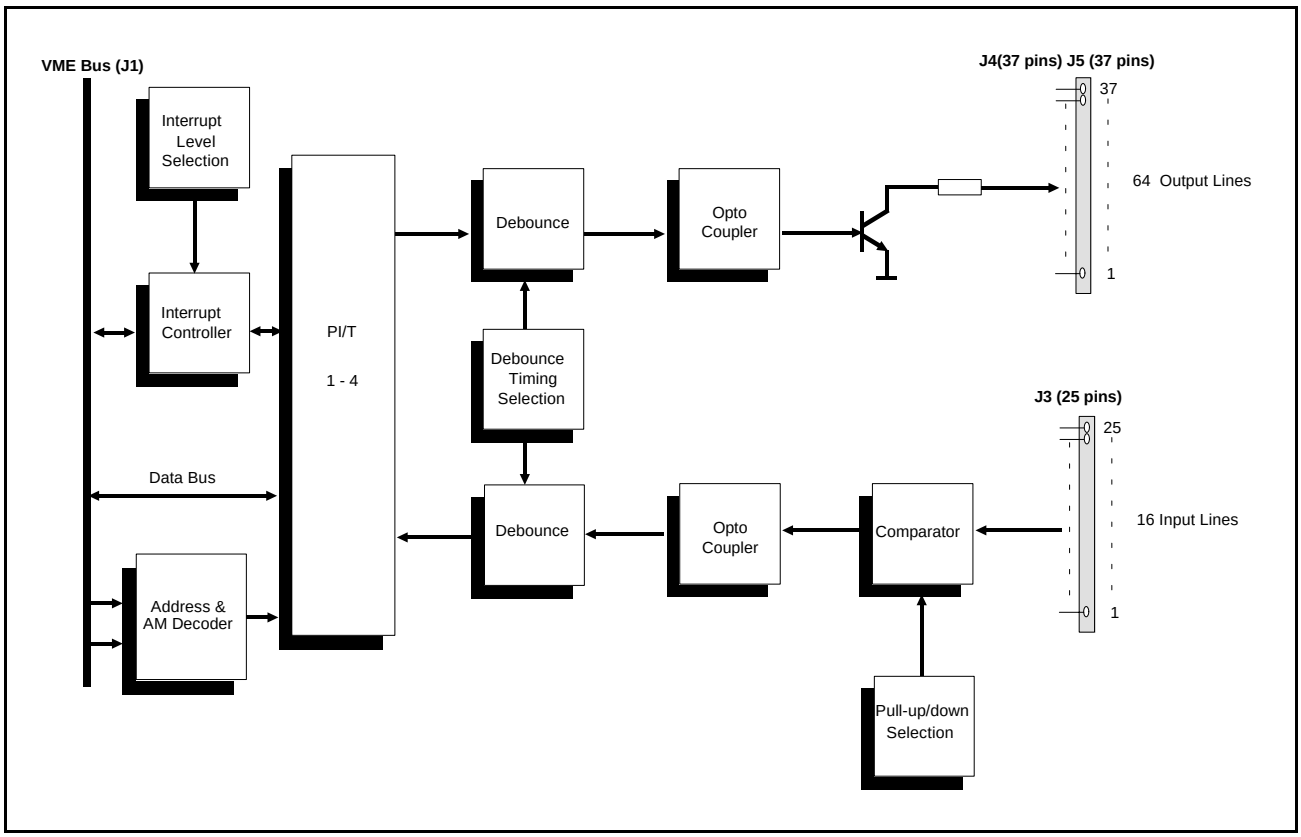
Table 2.1 Jumpers, Connectors and Switches

DESCRIPTION	FUNCTION
J1	VMEbus interface connector
J3	Inputs connector (input 1 - 16)
J4	Output connector (output 33 - 64)
J5	Output connector (input 1 - 32)
P1, P3, P5, P7	Configures the inputs to close to either ground or to the supply voltage
P2, P4, P6	Input time delay selection
P8, P11	Interrupt level selection
P9, P10	Watchdog timer disable, enable
P12	Addressing mode selection
DSW1	Board base address selection

2.5 MPV921 Block Diagram

Figure 2.2 shows a functional block diagram of the board.

Table 2.1 Jumpers, Connectors and Switches



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MPV921 Technical Specification

Input Characteristics

Opto-Isolated Inputs : 16 inputs, arranged in 4 banks of 4 channels

Opto-Isolated I/O Power Supply : +24V (MPV921A)
+5V (MPV921C)

Input Connector : 1 x D Type - 25 male connector J3

Input Stage : Pull-up to +24V/ +5V* or pull-down to 0V configurable in blocks of 4 input channels

Input ON/OFF Threshold Voltage :
+24V version, MPV921A:Vin(low) = +7.0V, Vin(high) = +9.5V
+5V version, MPV921C :Vin(low) = +2.2V, Vin(high) = +3.2V

Hysteresis : +24V version, MPV921A: 0.5V
+5V version, MPV921C : 0.1V

Maximum Input Current Drawn On One Channel : ±2.4mA

Input Power Capability : Each bank of four input channels can accept independant power supplies. These power supplies are supplied externally.

Current Drawn Per External Power Supply : 55mA

Input Protection : Protected from input voltage exceeding +24V/+5V* and less than 0V

Anti-bounce Delays : 70µs, 1ms, 7ms jumper selectable

Minimum detectable Signal Width : 27µs

I/O Isolation Voltage : 1500Vrms for 1 minute

Output Characteristics

Opto-Isolated Outputs : 64 outputs, arranged in 8 banks of 8 channels

Output Connector : 2 x D Type - 37 female connector J5 & J4

Output Buffer : Open Collector

Maximum Output Current In The ON state per channel : 150mA

Maximum Output Voltage In The OFF state : 50V

Output Protection : Protected from a power supply polarity inversion

Watchdog Timers : Then selected, if a location is not accessed within a specified time period the outputs will go to the OFF state. (Jumper Selectable)

Interrupt and Timer Characteristics

Interrupt Level : Jumper selectable

Interrupt Support : 16 inputs may assert an interrupt request on a rising or falling edge. Software configurable for each input.

Timers : Four 24 bit counters

Power Requirements

+5V at 1.5A

Environment

Operating Temperature : 0°C to 60°C

Storage requirements : -25°C to +85°C

Relative Humidity : 5% to 90% non-condensing

VME Interface

Board Type : Slave

Addressing Modes : A16

Data Mode : Byte D8 (Odd)

** Dependent on board version*

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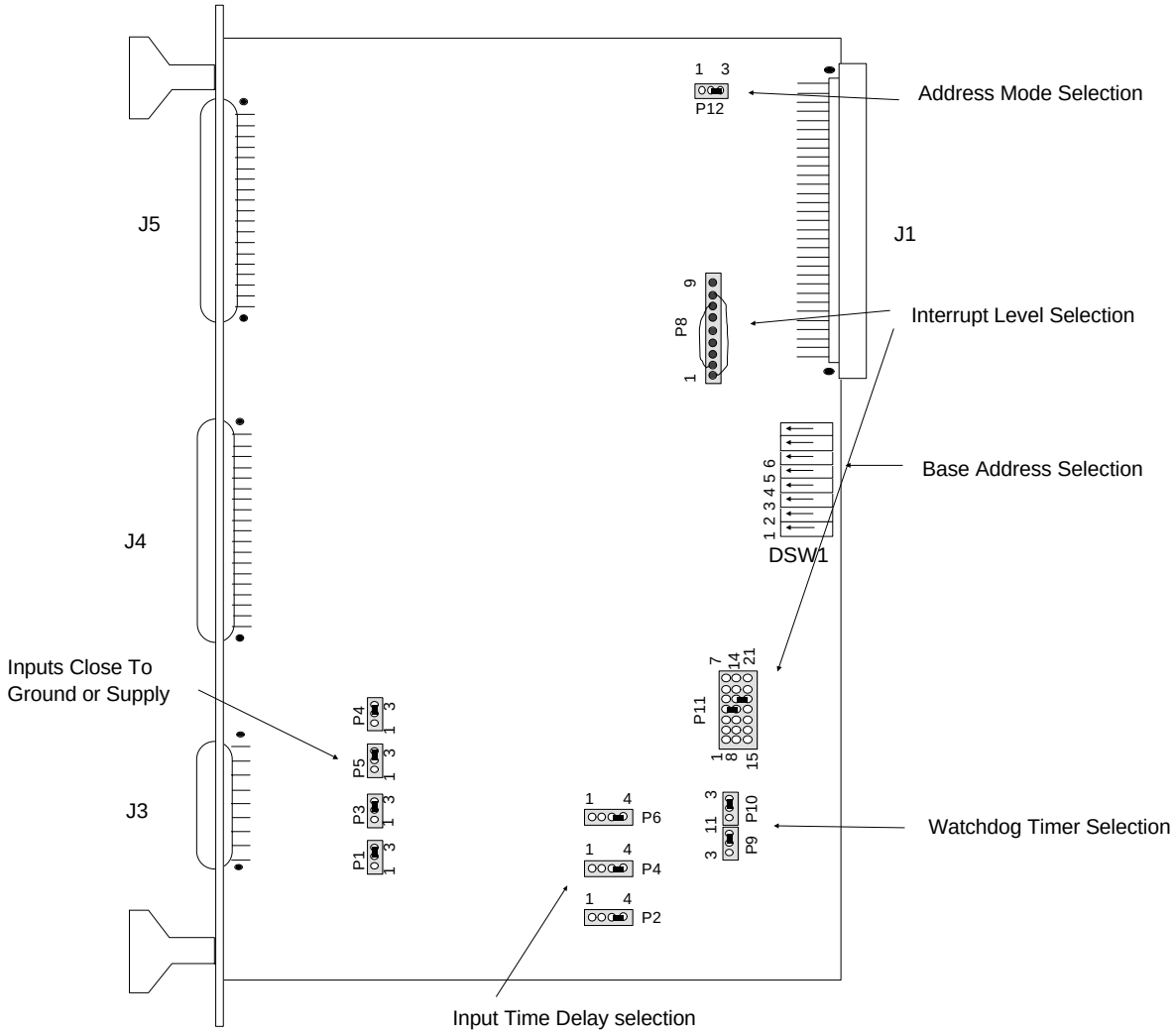
3 - HARDWARE CONFIGURATION

3.1 INTRODUCTION

The **MPV921 Digital Input/Output Board** has a number of user definable options that are selected using a series of jumpers and wire-wraps. Boards are supplied in the configuration shown in table 3.1. Users who do not wish to alter the factory set default settings should proceed to chapter 4 "Cables and Connections."

Figure 3.1 Factory Set Default Settings

Jumper/Switch	Setting
P1, P3, P5, P7	Contacts Closing To The Supply Voltage
P2, P4, P6	Debounce Delay Of 7ms
P8, P11	$\overline{\text{PIRQ}}$ generates a level 4 interrupt TIRQ generates a level 3 interrupt
P9, P10	Output 01-32 watchdog enabled Output 33-64 watchdog disabled
P12	Address Modifiers not decoded
DSW1	Base Address FF0000H



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3.2 CHANGING THE BASE ADDRESS

The MPV921 occupies 1kbyte of space within the system memory map. It may be located on any 1k boundary within 64k, provided it does not conflict with the location of any other device already installed in the system. The location of the MPV921 is altered by changing the DSW1 switches, shown in figure 3.2.

The board is shipped from the factory with a base address of FF0000H. Only switches SW1 to SW6 inclusive are used to set the base address.

Table 3.2 shows the correspondence between the address line sand the DSW1 switches.

Table 3.2 summaries the position of the switches and the resulting base address of the MPV921. Switching to the ON position sets the corresponding address bit to a zero (0).

Figure 3.2 P23 Setting

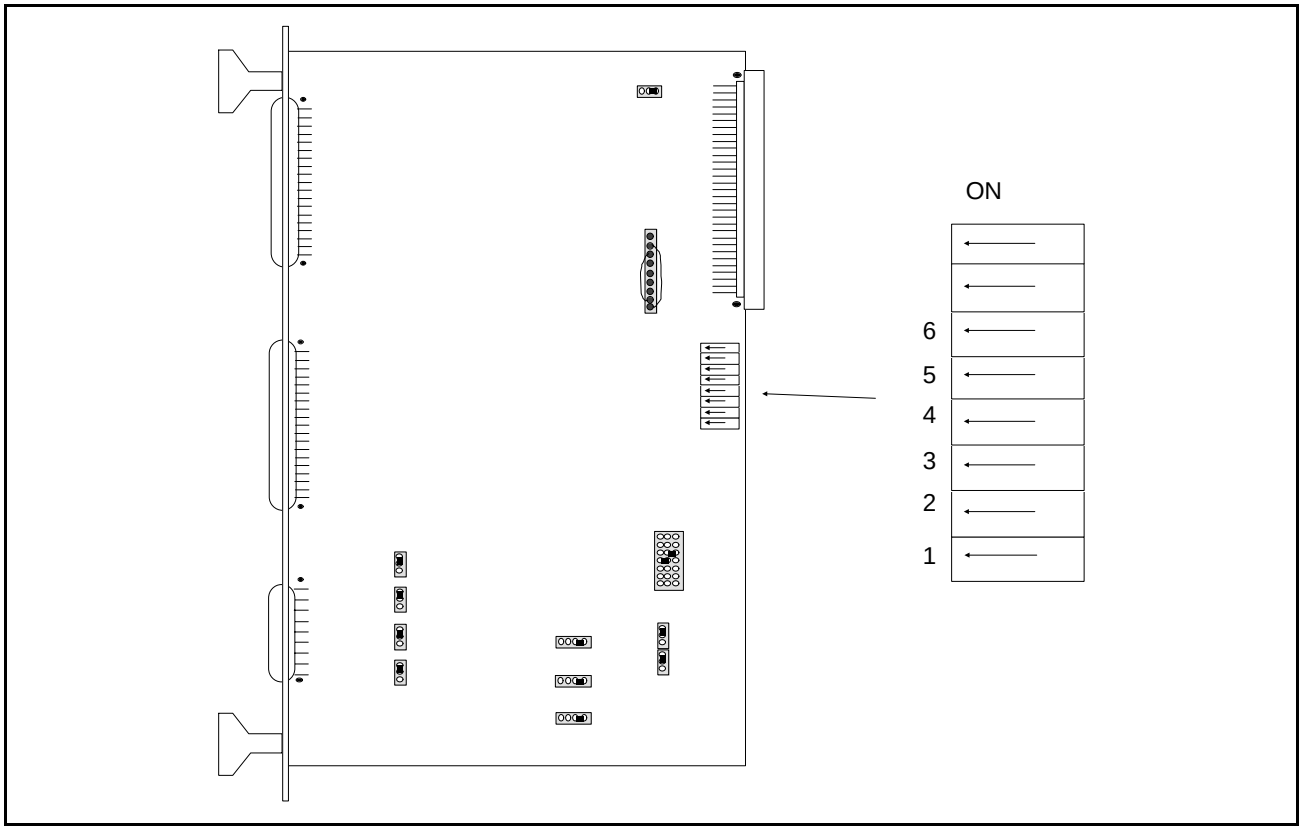


Table 3.2 Summary Of Base Address Options

SW1 (A15)	**SW2** (A14)	**SW3** (A13)	**SW4** (A12)	**SW5** (A11)	**SW6** (A10)	**BASE ADDRESS**
ON	ON	ON	ON	ON	ON	FF0000H
ON	ON	ON	ON	ON	OFF	FF0400H
ON	ON	ON	ON	OFF	ON	FF0800H
ON	ON	ON	ON	OFF	OFF	FF0C00H
ON	ON	ON	OFF	ON	ON	FF1000H

and so on until.....

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SW1	SW2	SW3	SW4	SW5	SW6	BASE ADDRESS
OFF	OFF	OFF	ON	OFF	OFF	FFEC900H
OFF	OFF	OFF	OFF	ON	ON	FFF000H
OFF	OFF	OFF	OFF	ON	OFF	FFF400H
OFF	OFF	OFF	OFF	OFF	ON	FFF800H
OFF	OFF	OFF	OFF	OFF	OFF	FFFC00H

3.3 ADDRESS MODIFIER DECODER

With jumper P12 inserted between pin 1 and pin 2 the board decodes address modifiers. In the short addressing mode the following two modifiers are allowed.

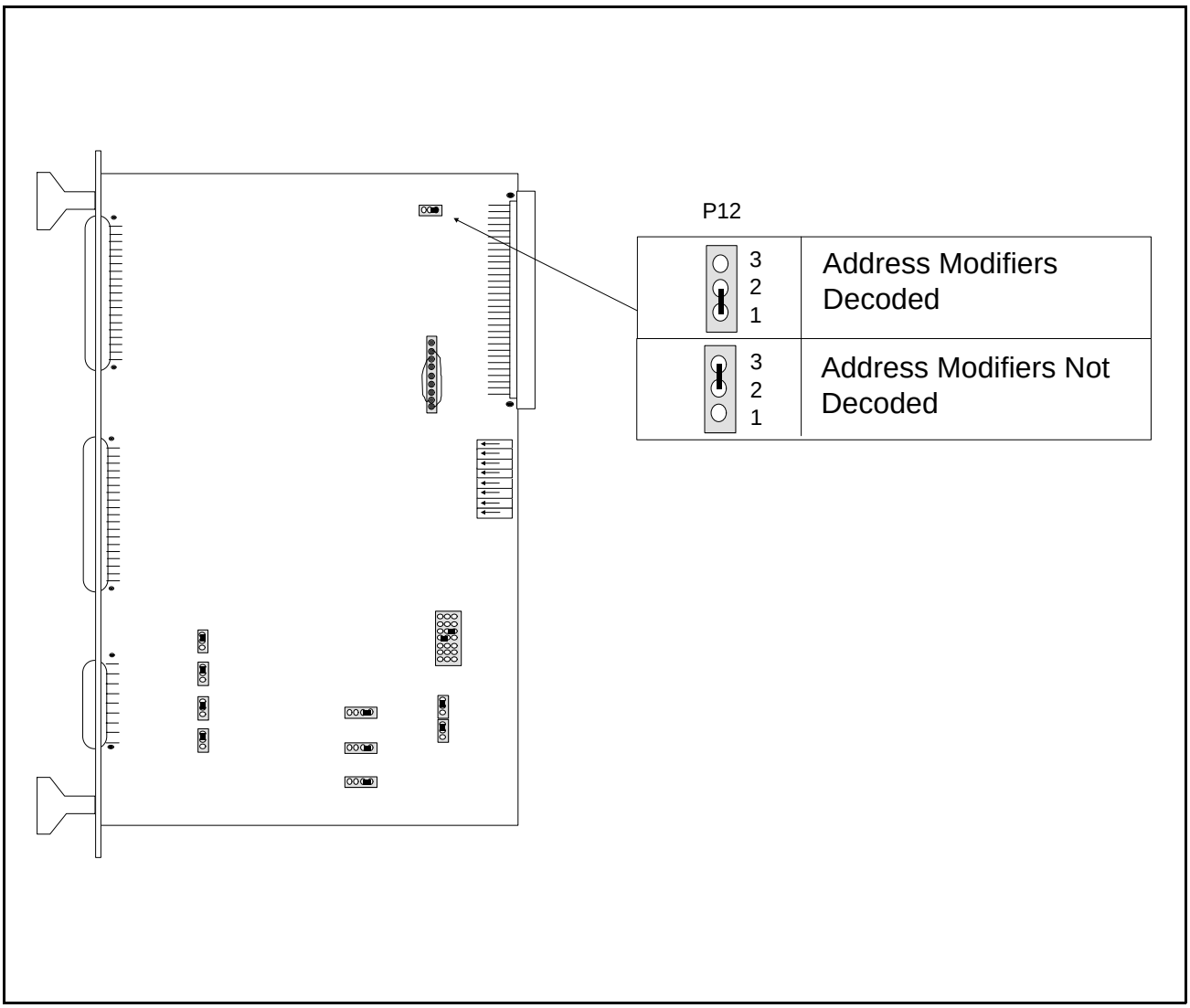
Code $2DH - Short Supervisory I/O Access

Code $29H - Short Non-Privileged I/O Access

With the jumper between pin 2 and pin 3 address modifiers are not decoded.

Figure 3.3 shows the possible settings of jumper P12.

Figure 3.3 Address Modifier Decoding



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3.4 CONFIGURATION OF THE INPUTS

Jumpers P1, P3, P5 and P7 are used to define the setting of the inputs, i.e., if they close to earth or the supply voltage. The input channels are arranged in groups of four. Table 3.3 shows how the input channels and jumpers are configured.

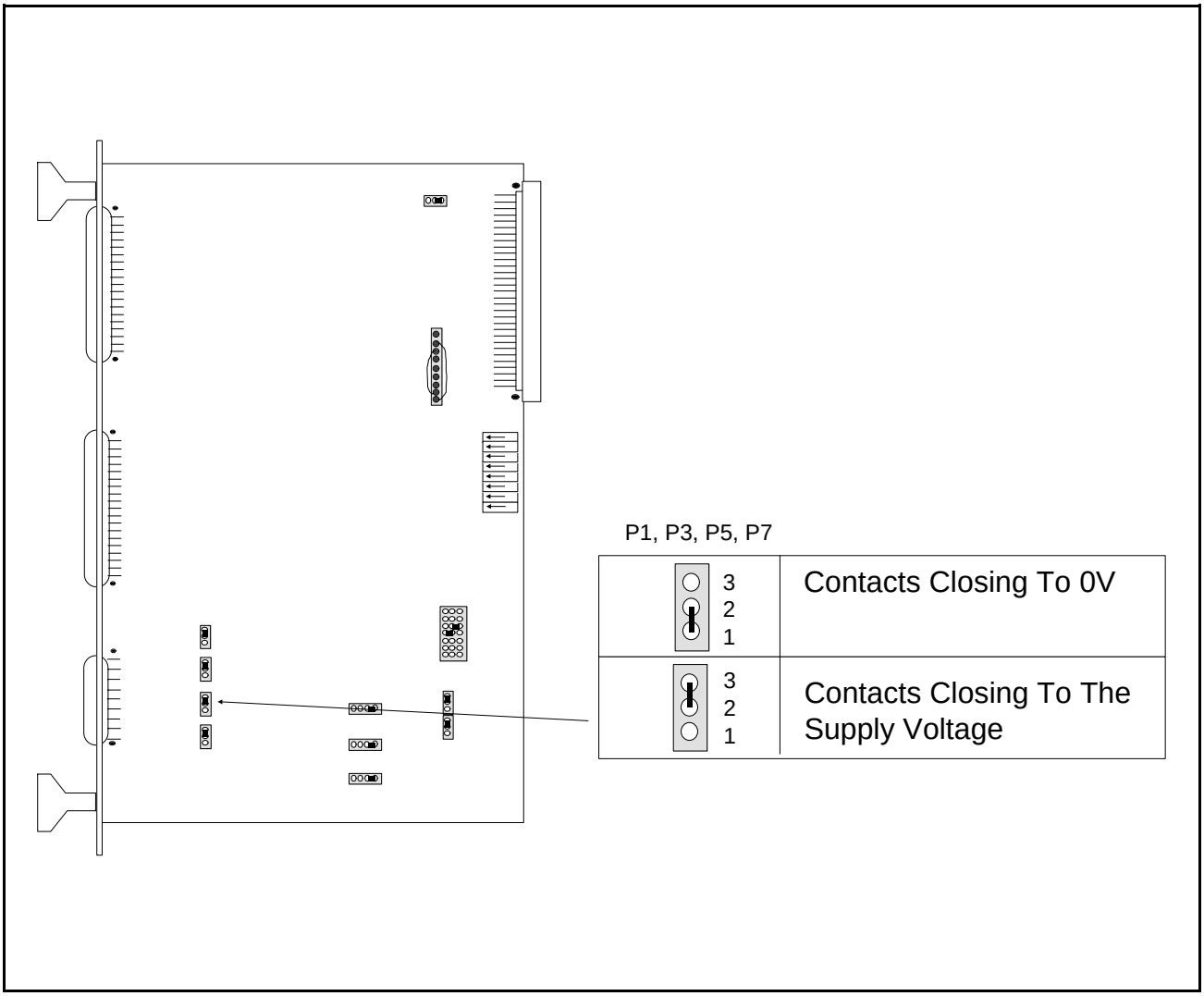
Figure 3.4 shows the possible options for jumpers P1, P3, P5 and P7.

Table 3.3 Input Configuration

GROUP	INPUTS	JUMPER
1	01, 02, 03, 04	P7
2	05, 06, 07, 08	P5
3	09, 10, 11, 12	P3
4	13, 14, 15, 16	P1

Note: The input circuit inverts the signal; a low level (0V) on a PI/T pin corresponds to a high level (Vcc) on the corresponding connector.

Figure 3.4 Configuration Of The Inputs



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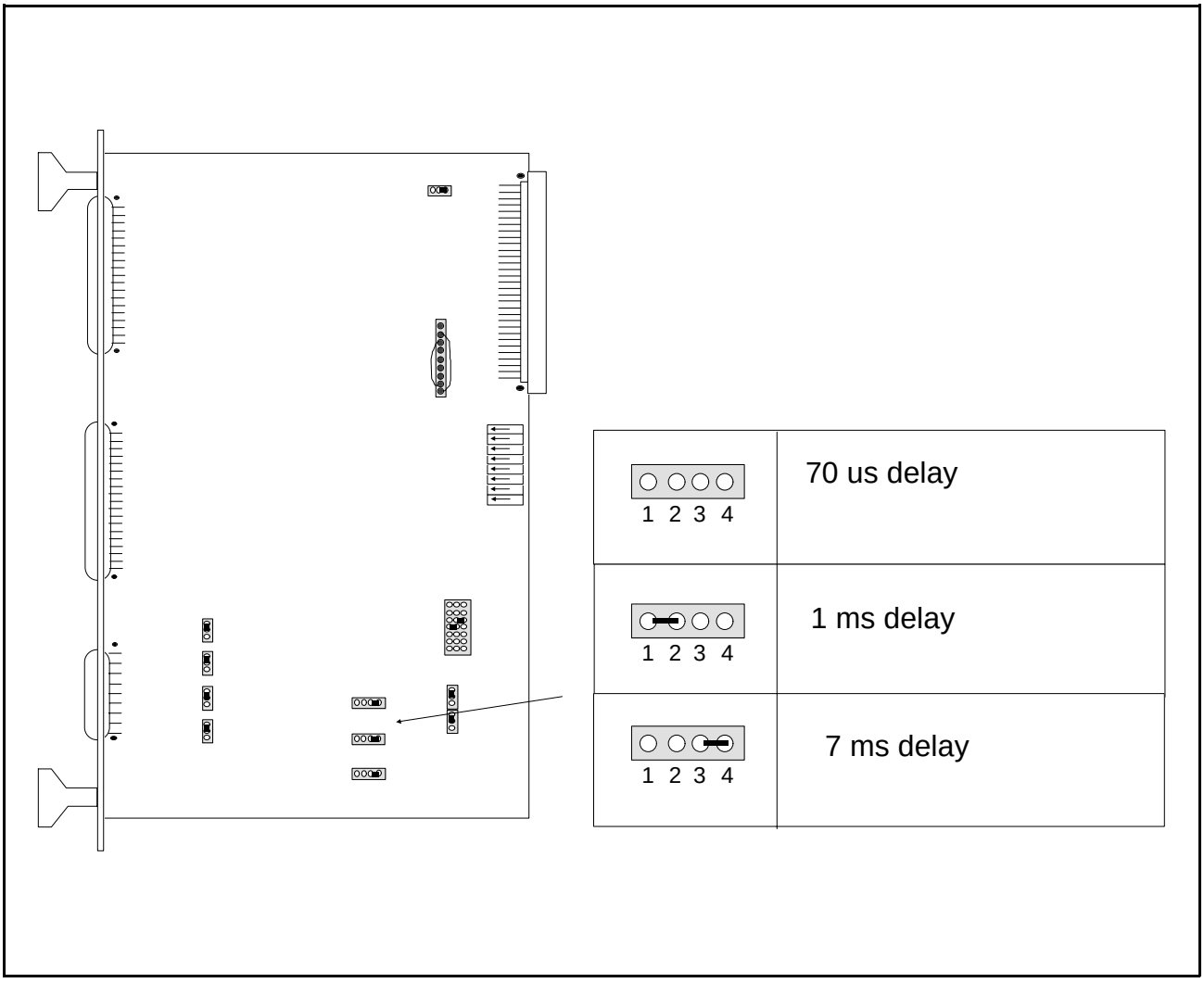
3.5 INPUT TIME DELAY

Debounce circuitry is incorporated to generate a delay between the input channels and the inputs to the PI/T's. The time delays are selected via jumpers P17 - P20. Table 3.4 shows the relationship between jumpers and the input channels. Figure 3.5 shows the time delay options available and the location of the jumpers.

Table 3.4 Relation Of Channels To Jumpers

JUMPER	INPUTS
P6	Input 01 - Input 6
P4	Input 7 - Input 10
P2	Input 11 - Input 16

Figure 3.5 Debounce Time Delay selection



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3.6 INTERRUPT LEVEL SELECTION

All sixteen of the inputs, if enabled, and the four timers can generate interrupts on the MPV921. Jumpers P8 and P11 select the level of the interrupt request asserted on the VMEbus (from 1 to 7). The input interrupt is designated the PIRQ interrupt, and the timer interrupt is called the TIRQ

3.6.1 $\overline{\text{PIRQ}}$ INTERRUPT

Table 3.5 shows how to select the required level of interrupt.

Table 3.6 PIRQ Interrupt

JUMPER		VME INTERRUPT LEVEL
P8	P11	GENERATED BY PIRQ*
1-3	8-1	7
1-5	9-2	6
1-9	10-3	5
1-8	11-4	4
1-7	12-5	3
1-6	13-6	2
1-4	14-7	1

3.6.2 $\overline{\text{TIRQ}}$ INTERRUPT

Table 3.5 shows how to select the required level of interrupt.

Table 3.7 TIRQ Interrupt

JUMPER		VME INTERRUPT LEVEL
P21	P22	GENERATED BY TIRQ*
2-3	15-8	7
2-5	16-9	6
2-9	17-10	5
2-8	18-11	4
2-7	19-12	3
2-6	20-13	2
2-4	21-14	1

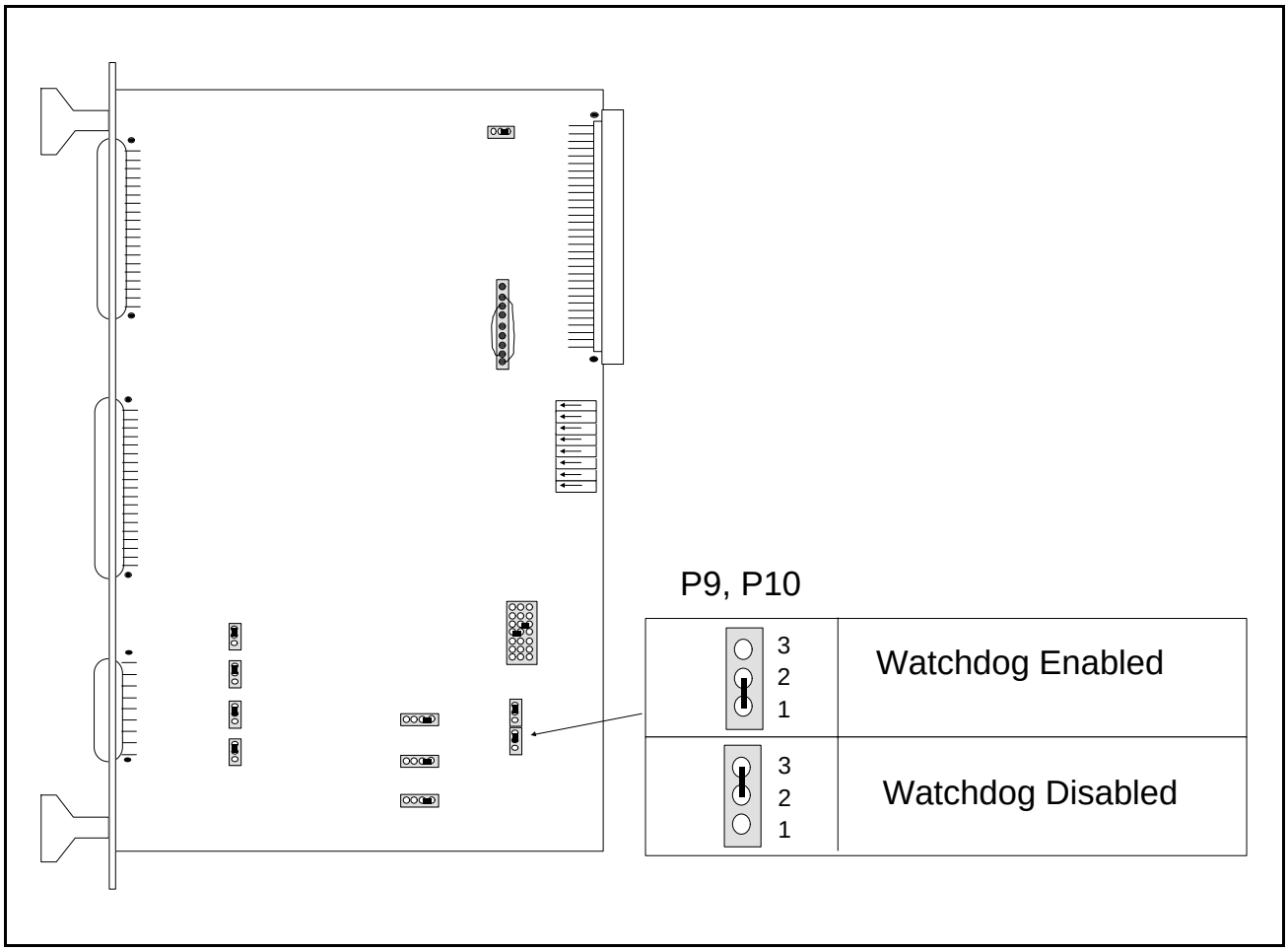
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3.7 CONFIGURING THE WATCHDOG TIMER

The MPV921 is provided with a security watchdog mechanism. This mechanism disables all the ouputs until it is retriggered by the master, by means of a periodic write cycle to an address equal to the board base address plus $C1.

Jumpers P9 and P10 allow the watchdog enabling and disabling, see figure 3.6. P9 controls the status of outputs 01-32 and jumper 10 controls outputs 33-64.

Figure 3.6 Watchdog Timer Enable/Disable



3.7.1 SETTING THE TIME DURATION OF THE WATCHDOG

The MPV921 watchdog timer is implemented using a 74LS123 monostable. The output pulse width is defined by the combination of R102 & C36 for outputs 01 to 32, and R101 & C35 for outputs 33 to 64. The location of these components is shown in figure 3.6.

The output pulse width is defined as $tw=0.45CR$

where C=C36 & R=R102 for outputs 01-32

and C=C35 & R=R101 for outputs 33-64

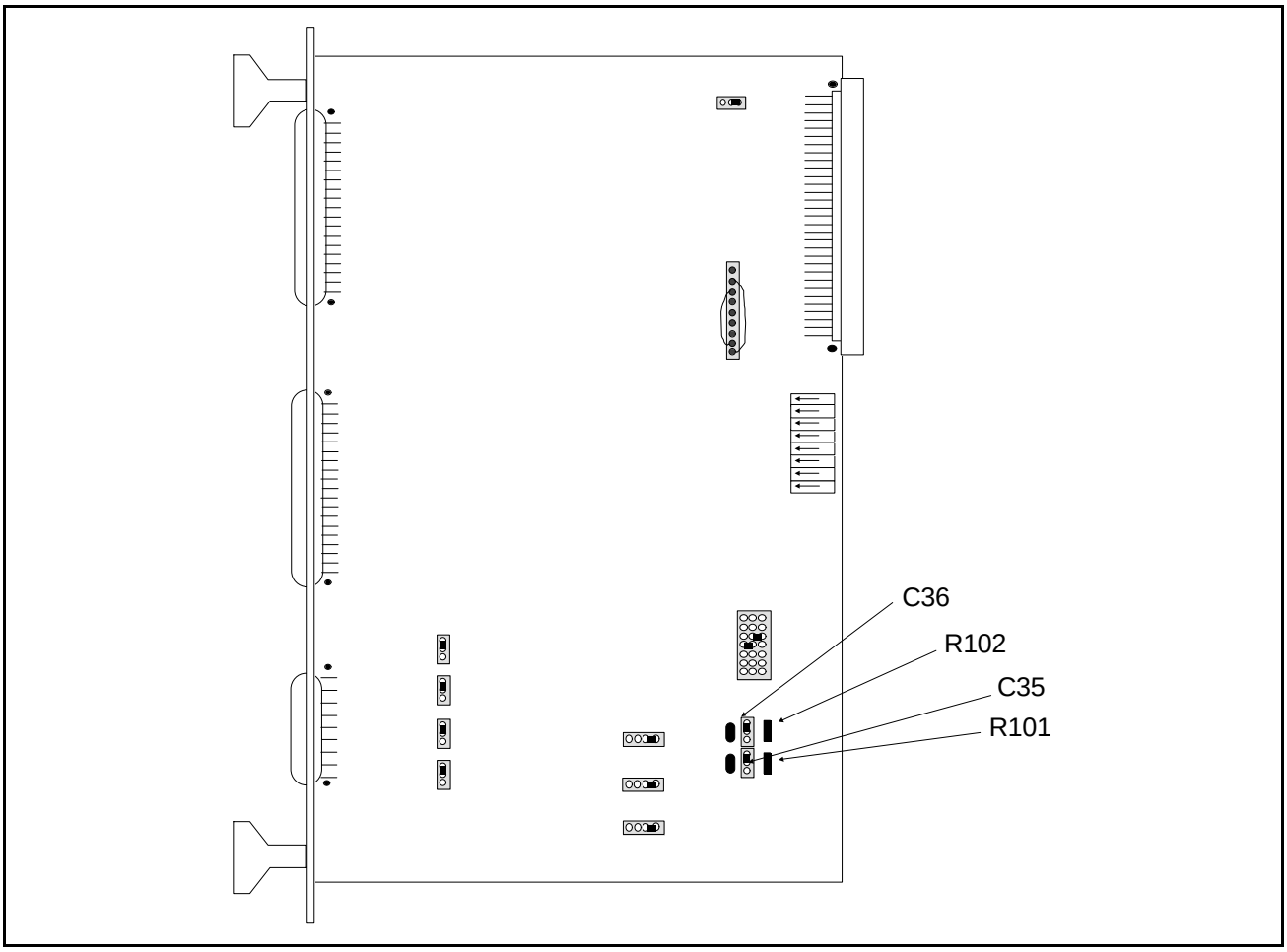
The value of R must not exceed 220kΩ.

For example if R=220kΩ and C=470nF, then tw=46ms.

If the watchdog timer register is not written to prior to the timeout, the board will automatically clamp the outputs at 0V, assuming the watchdog timer is enabled. The timeout period may be altered by changing the value of R & C.

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Figure 3.7 Watchdog Timer Duration

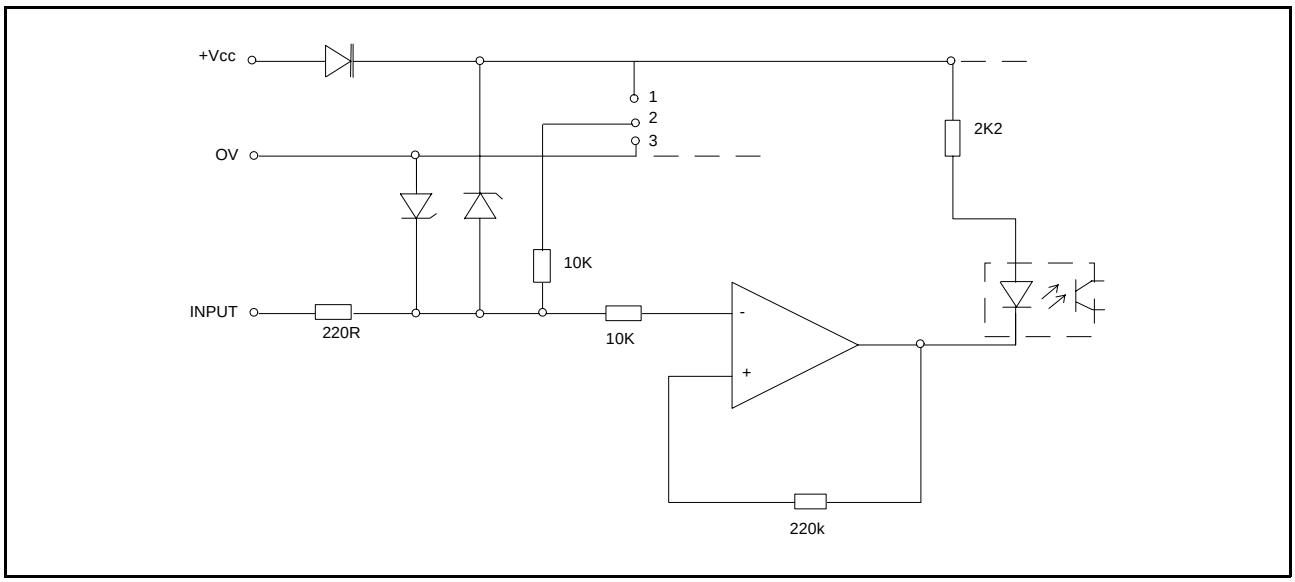


3.8 INPUT / OUTPUT CIRCUIT CONFIGURATION

3.8.1 Input Circuit Configuration

The input circuitry for the MPV921 is as detailed in Figure 3.8

Figure 3.8 Input Circuit Configuration

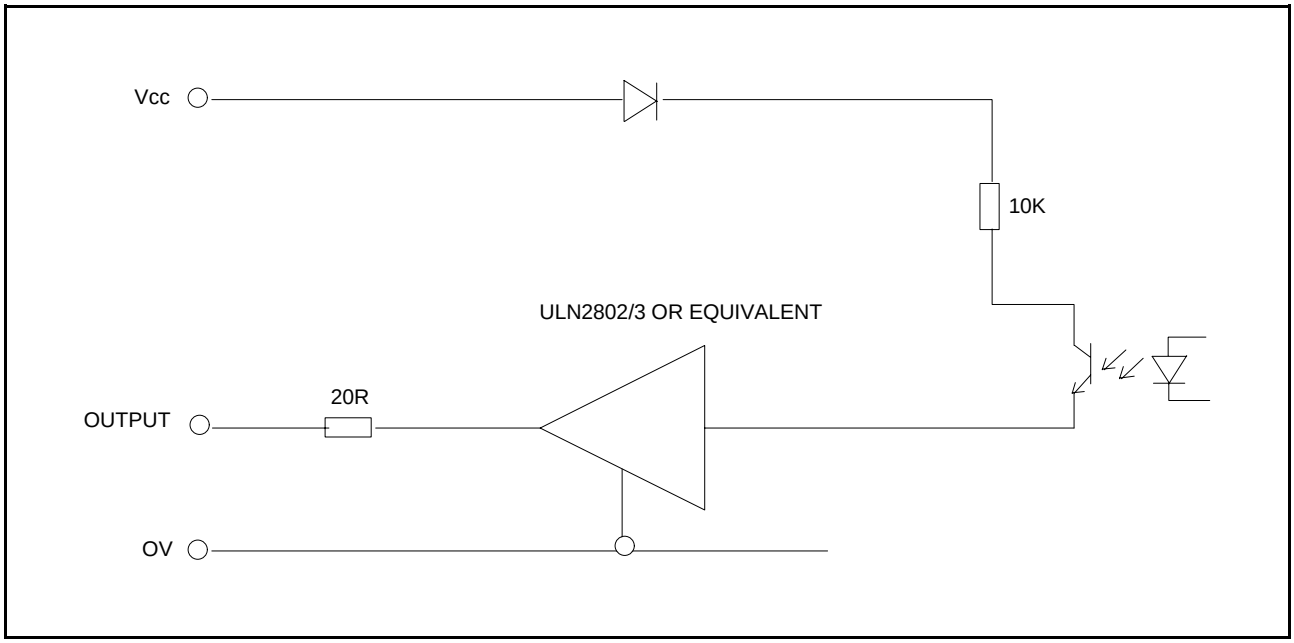


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3.8.2 Output Circuit Configuration

The output circuitry for the MPV921 is as detailed in Figure 3.9

Figure 3.9 Output Circuit Configuration



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4 - CABLES AND CONNECTIONS

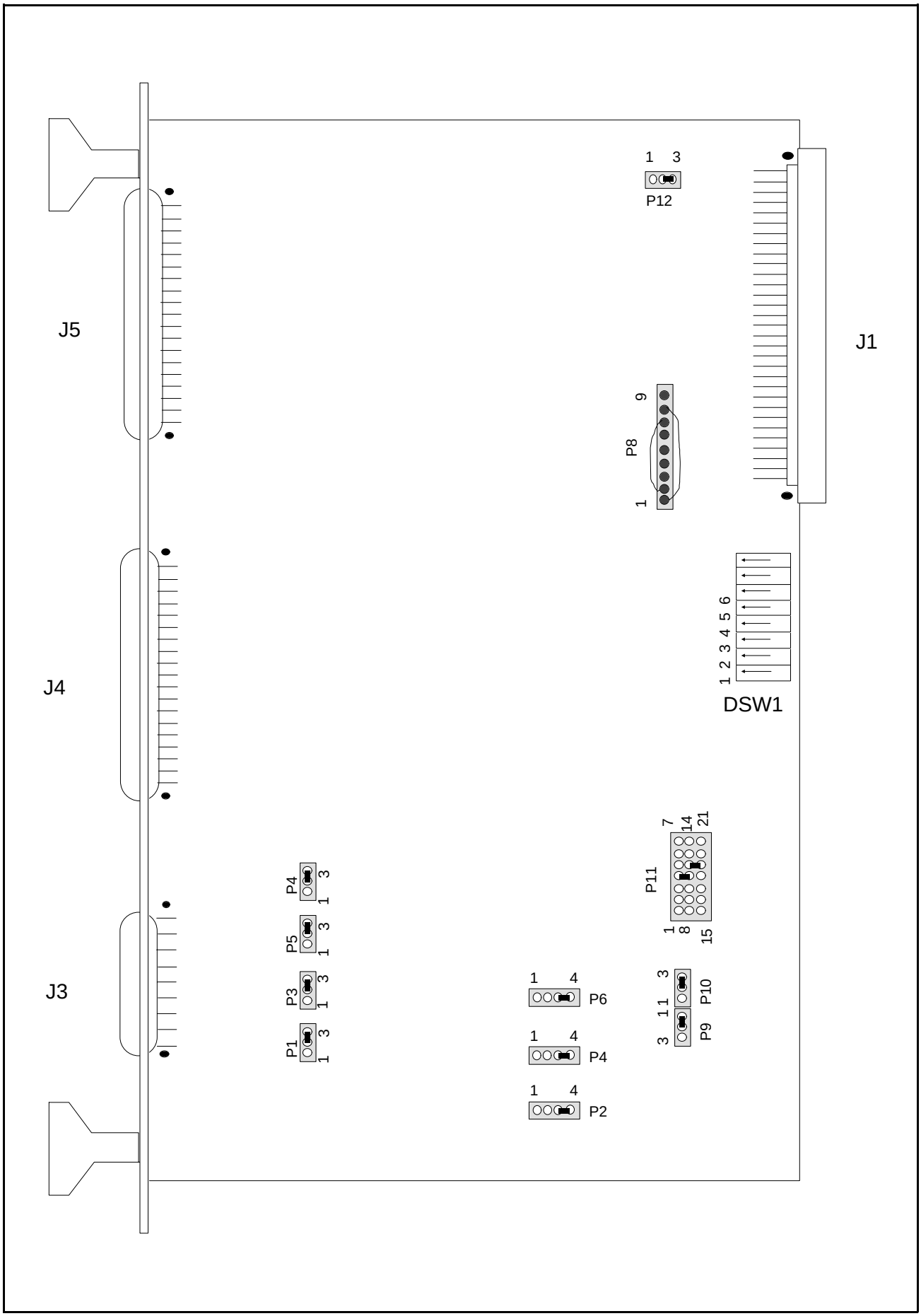
4.1 CONNECTING THE MPV921

Communication between the MPV921 and the VMEbus is performed via the J1 connector on the rear of the board. To install the MPV921 in the system, carefully align connectors J1 with the corresponding J1 connectors on the VMEbus backplane and press firmly home.

Ensure that power to the VMEbus system is turned off before installing the MPV921. The MPV921 is sensitive to the build-up of static electricity, therefore normal anti-static precautions should be observed when handling the board.

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Figure 4.1 Location Of Connectors



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4.2 CONNECTOR PIN ASSIGNMENTS

4.2.1 P1 Pin Assignment

The 96-way J1 connector on the MPV921 mates with J1 connector on the VMEbus Backplane.

Table 4.1 J1 Pin Assignment

Pin	(a)	(b)	(c)
1	D00	N.C.	N.C.
2	D01	N.C.	N.C.
3	D02	N.C.	N.C.
4	D03	BG0IN*	N.C.
5	D04	BG0OUT*	N.C.
6	D05	BG1IN*	N.C.
7	D06	BG1OUT*	N.C.
8	D07	BG2IN*	N.C.
9	N.C.	BG2OUT*	GND
10	SYSCLK	BG3IN*	N.C.
11	GND	BG3OUT*	N.C.
12	N.C.	N.C.	SYSRESET*
13	DS0*	N.C.	N.C.
14	WRITE*	N.C.	AM5
15	GND	N.C.	A23
16	DTACK*	AM0	A22

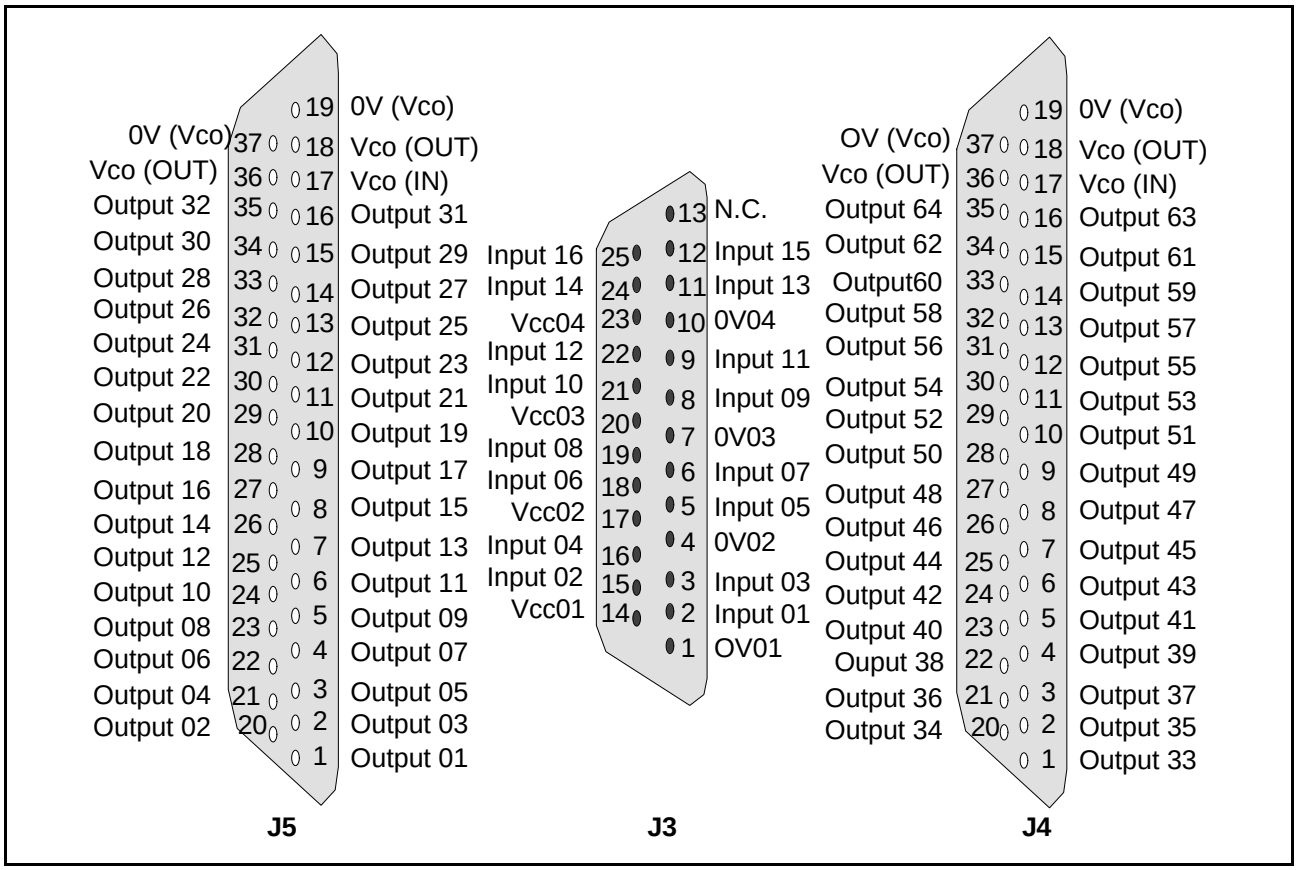
Pin	(a)	(b)	(c)
17	GND	AM1	A21
18	AS*	AM2	A2
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	N.C.	A17
22	IACKOUT*	N.C.	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	N.C.	N.C.	N.C.
32	+5V	+5V	+5V

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4.3 DIGITAL INPUT/OUTPUT CONNECTIONS (J3, J4 & J5)

Up to 64 digital outputs and 16 digital inputs can be connected to the MPV921. The pin assignments for the three front panel connectors are shown in figure 4.2.

Figure 4.2 Input Connections



4.3.1 INPUT POWER SUPPLIES

Sixteen inputs, divided into 4 groups of 4 inputs, are available. For each group of 4 a separate power supply can be connected. Each group will be an independent power supply, table 4.2 shows the assignment of the inputs and their independent power supply.

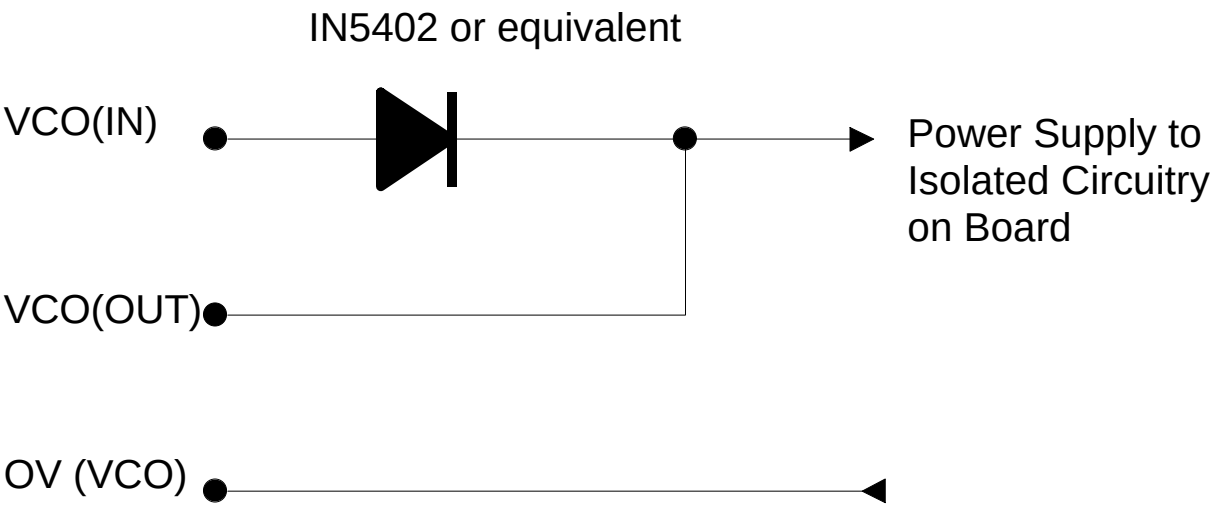
Table 4.2 Inputs & Power Supply Configuration

Group	Inputs	Power Supply
1	Input01-Input04	0V 01, Vcc 01
2	Input05-Input08	0V 02, Vcc 02
3	Input09-Input12	0V 03, Vcc 03
4	Input13-Input16	0V 04, Vcc 04

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4.3.2 OUTPUT POWER SUPPLIES

Figure 4.3 details the output circuitry and its power connection

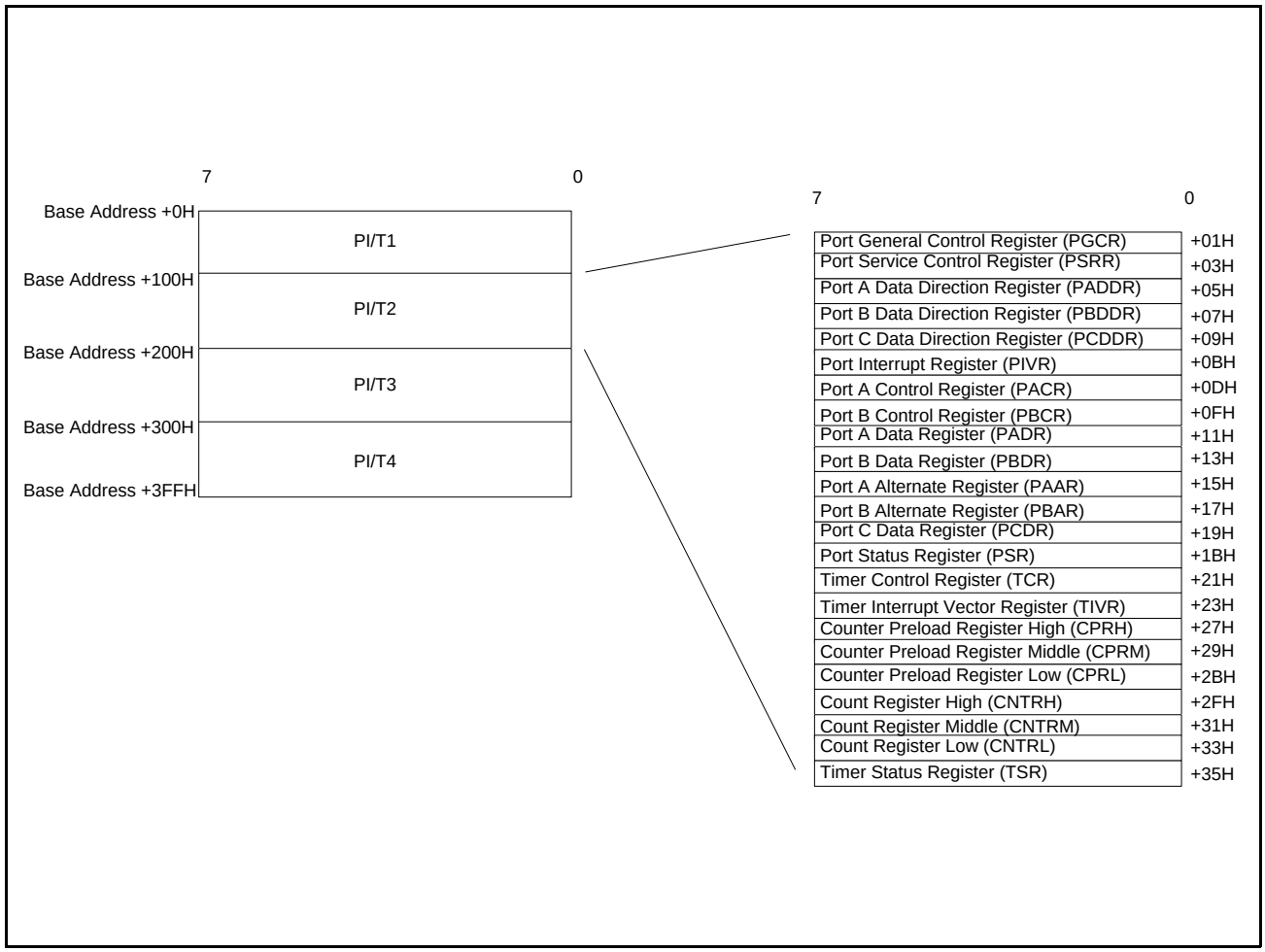


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5.1 INTRODUCTION

The MPV921 occupies 1kbyte of locations within the VME address space. Figure 5.1 shows a memory map of the board. The inputs to the board are controlled by four MC68230 Parallel Interface/Timers (PI/T's). It is important that the PI/T's are initialised correctly, see chapter 6 for example programs and the MC68230 data sheet provided.

Figure 5.1 MPV921 Memory Map



5.2 MC68230

The location of the four PI/T's is also shown in figure 5.1, their locations are also shown in table 5.1 below. VME address lines A08 and A09 are used to identify the individual PI/T's.

Table 5.1 PI/T Memory Locations

PI/T's	OFFSET
1	0
2	100H
3	200H
4	300H

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5.3 MPV921 OUTPUTS

The configuration of the outputs to the MC68320 is shown in the table 5.2 and table 5.3. VME address lines A01 to A05 identify the specific registers within the PI/T's.

Table 5.2 PI/T Registers

INPUTS	REGISTER	PI/T's	OFFSET
Output01 - Output08	PBDR	2	113H
Output09 - Output16	PBDR	1	13H
Output17 - Output24	PADR	2	111H
Output25 - Output32	PADR	1	11H
Output33 - Output40	PBDR	4	313H
Output41 - Output48	PBDR	3	213H
Output49 - Output56	PADR	4	311H
Output57 - Output64	PADR	3	211H

Table 5.3 PI/T Memory Locations

PI/T	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
2	PBDR	08	07	06	05	04	03	02	01
1	PBDR	16	15	14	13	12	11	10	09
2	PADR	24	23	22	21	20	19	18	17
1	PADR	32	31	30	29	28	27	26	25
4	PBDR	40	39	38	37	36	35	34	33
3	PBDR	48	47	46	45	44	43	42	41
4	PADR	56	55	54	53	52	51	50	49
3	PADR	64	63	62	61	60	59	58	57

5.3.1 EXAMPLE

If we wish to set the status of outputs 41-48, these outputs are mapped in register PBDR of PI/T number 3 (see table 5.3). Assuming that the board base address has been set at $FF0400H (switch 1-5 ON and switch 6 OFF), then it is necessary to perform a write cycle at address $FF0613, see below.

$FF0400H	Board Base Address
$ 13H	Address for PBDR Register
$ 200H	Offset PI/T number 3
$FF0613H	

5.4 EXAMINING THE OUTPUTS

It is possible to examine the logical state by reading the PAAR and PBAR read only registers, the offsets with respect to the base address is shown in table 5.4 below.

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Table 5.4 Examining The Outputs

PI/T	REGISTER	OFFSET
2	PBAR	117H
1	PBAR	17H
2	PAAR	115H
1	PAAR	15H
4	PBAR	317H
3	PBAR	217H
4	PAAR	315H
3	PAAR	215H

5.5 MPV921 INPUTS

The inputs to the board can be accessed by reading the locations shown in table 5.5 and table 5.6.

Table 5.5 PI/T Input Registers

INPUTS	REGISTER	PI/T	OFFSET
Input 01-04	PSR	1	1BH
Input 05-08	PSR	2	11BH
Input 09-12	PSR	3	21BH
Input 13-16	PSR	4	31BH

Table 5.6 PI/T Input Memory Locations

PI/T	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
1	PSR	04	03	02	01				
2	PSR	08	07	06	05				
03	PSR	12	11	10	09				
4	PSR	16	15	14	13				

5.6 INPUT GENERATED INTERRUPTS

The 16 inputs listed in table 5.7 are capable of generating interrupts.

The example programs and MC68230 PI/T data sheets describe the interrupt request handling.

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Table 5.7 Input Generated Interrupts

INPUT	REGISTER	**PI/T's**
Input 01	H1	1
Input 02	H2	1
Input 03	H3	1
Input 04	H4	1
Input 05	H1	2
Input 06	H2	2
Input 07	H3	2
Input 08	H4	2
Input 09	H1	3
Input 10	H2	3
Input 11	H3	3
Input 12	H4	3
Input 13	H1	4
Input 14	H2	4
Input 15	H3	4
Input 16	H4	4

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```
ME              equ             2           * Manx ass. error put 0 when error will be
                                            * fixed
GLOBAL ROUTINES
                public          _s921in     * d0 = goup to initialise, reurn in a0 PIT
                                            * base address (pit 1), if a0=0 nonexistent
                                            * group, into a1 INPUTS handling routine
                                            * address
MPV921 EQUATES
Base Address
                include         "base921.hs"        * MPV921 base address declaration

pit1            equ             0                   * offset first PIT
offpit          equ             $100                * offset between 2 PITS

buserve         equ             8                   * bus error vector
EQUATES PIT
Port Parameter
PP              equ             1                    * 0 = TVM-220
                                                     * 1 = TVM-200 TVM-742 TVM-743 TVM-745
                include "pit.hs"
                cseg
INITIALISE A GROUP OF 16 INPUTS
* d0 = group to initialise, return in a0 PIT1 base address
* if a0-0 unexisting group,
* into a1 INPUTS handling routine address
* MPV921 inputs are H1-H4 inputs of the 4 board PITS.
* A group is composed of 16 inputs Hx present on the board.
* If one of the 4 PIT doesn't answer (provoke a bus error signal generation)
the whole group is considered nonexistent
_s921in movem.l d1/a6,-(a7)
                move.l          buserve,-(a7)       * save bus error vector
                move.l          a7,a6               * save SP into a6
                move.l          #berr743,buserve    * set vector unexis. board routine
                move.l          d0,d1               * compute PIT base address
                lsl.w           #2,d1
                move.l          tapit+ME(pc,d1),a0  * PIT base address
                move.l          a0,a1

                moveq.l         #4-1,d1             * initialise the board's 4 PITS
nexpit          move.b          #$3f,pgcr(a1)        * mode 0, h12 - h34 enabled
                move.b          #$18,psrr(a1)        * vectorised interrupts
```


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```
                move.b      #$80,pacr(a1)       * submode 1x
                move.b      #$80,pbcr(a1)       * submode 1x
                lea         offpit(a1),a1       * PIT address
                dbf         d1,nexpit
                lea         t743in(pc),a1       * INPUTS handling routine
ent921          move.l      (a7)+,buserve
                movem.l     (a7)+,d1/a6
                rts
nonexistent inputs handling
berr921 move.l              a6,a7               * restore stack pointer
                lea         t743ne(pc),a1       * nonexis. board handling routine
                sub.l       a0,a0               * a0=0 ( set nonexisting board )
                bra.s       ent743
PIT address array (each Pit has 4 inputs (H1-H4); a group is composed with Hx
inputs of 4 PITS)
tapit           dc.l base1+pit1
                dc.l base2+pit1
                dc.l base3+pit1
                dc.l base4+pit1
*               dc.l base5+pit1
*               dc.l base6+pit1
*               dc.l base7+pit1
*               dc.l base8+pit1
```

INPUT OF 16 DIGITAL INPUTS

```
* into a0 is passed the address, into d0.w is returned the data
* the read inputs are H1-H4 inputs of the 4 boards' PITS
MPV921in        move.b      pssr+offpit*3(a0),d0
                lsl.l       #4,d0                   * first 4 inputs
                move.b      pssr+offpit*2(a0),d0
                lsl.l       #4,d0                   * second 4 inputs
                move.b      pssr+offpit*1(a0),d0    * third 4 inputs
                lsl.l       #4,d0
                move.b      pssr+offpit*0(a0),d0
                lsr.l       #4,d0                   * fourth 4 inputs
*               not.w       d0                      * If inversion needed
                rts
```

INPUT OF 16 DIGITAL INPUTS OF NONEXISTANT BOARDS

```
MPV921ne        moveq.l #-1,d0                  * return all inputs = 1
                rts
                end
```


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