Operating Manual

MPV922 Digital Input/Output Board

PENTLAND SYSTEMS LIMITED

MPV 922

Digital I/O Board

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MPV922 OPERATING MANUAL

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1- INTRODUCTION

1.1 ABOUT THIS MANUAL

The MPV922 Isolated Digital I/O Board from Pentland Systems, interfaces directly to the VMEbus and provides the user with 40 inputs arranged in 2 blocks of 4 channels and 4 blocks of 8 channels, and 32 outputs arranged in 4 blocks of 8 channels each.

This manual includes a full description of the features of the MPV922, and instructions on how to configure, install and operate the board.

GENERAL DESCRIPTION

2.1 INTRODUCTION

Chapter 2 provides a brief description of the MPV922, and includes a summary of its key features and a full technical specification.

2.2 KEY FEATURES

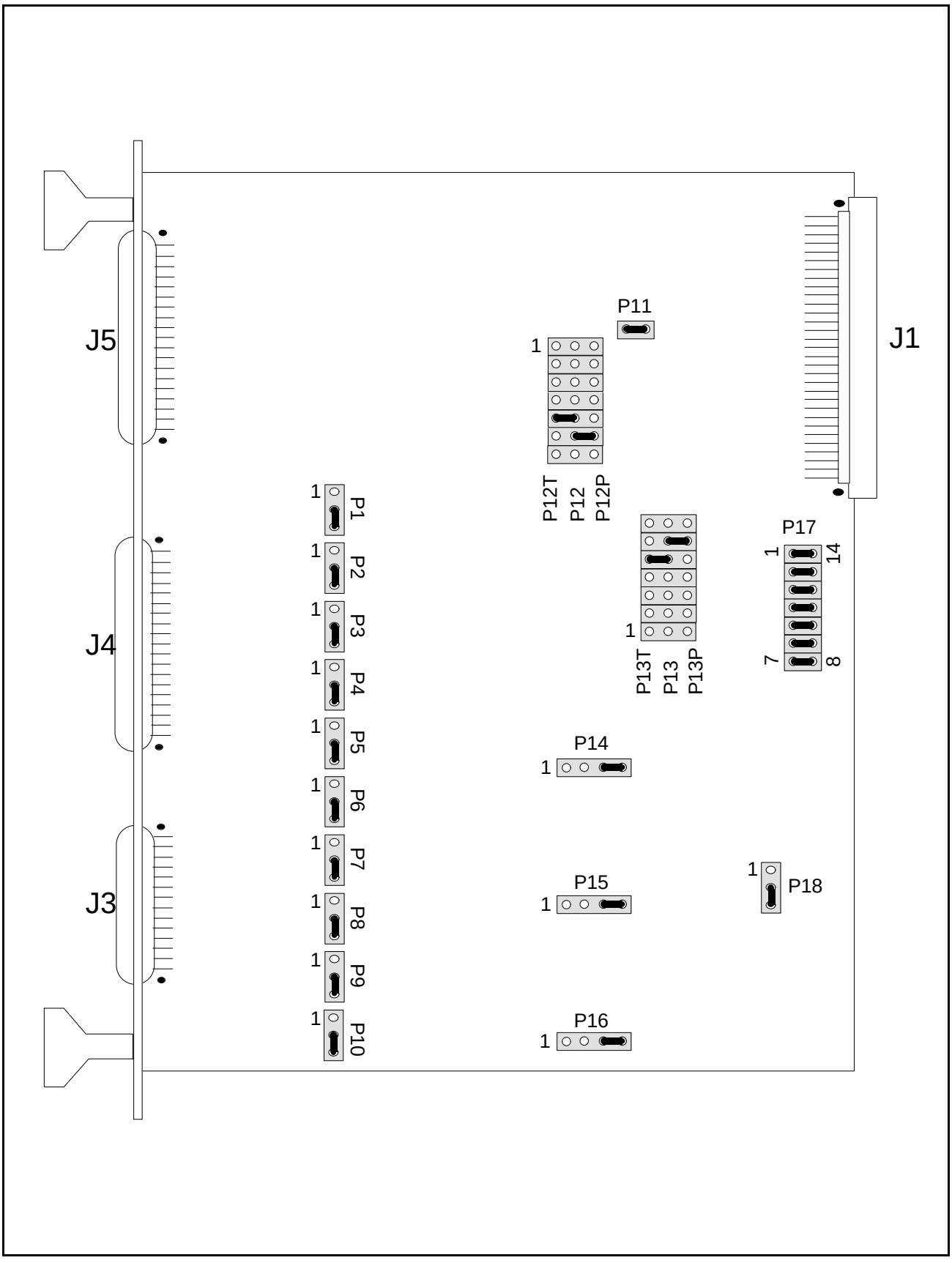
- Outputs can withstand upto 1500Vrms
- Inputs can withstand voltages up to 1500Vrms, or 600V DC applied continuously
- Available in 24V and 5V versions
- Four 24 bit timers
- Debounce protection
- Wide range of compatible I/O racks are available
- User specified watchdog timer

2.3 DESCRIPTION OF THE MPV922

The MPV922 is one in a family of boards designed for applications requiring high channel-count, opto-isolated, digital I/O on the VMEbus. They are each supplied on a single 6U card and are electrically and mechanically compatible with the VMEbus.

All the inputs are extremely well protected against voltage surges and each is able to withstand at least 1500Vrms for 1 minute without damage. The boards can be interfaced using Pentlands industrial standard I/O racks which offer excellent flexibility when connecting to the real world.

Figure 2.1 MPV922 Board Layout



2.4 DESCRIPTION OF JUMPERS AND CONNECTORS

Table 2.1 shows the location of all the jumpers and connectors on the MPV922, Table 2.1 provides a brief description of each device.

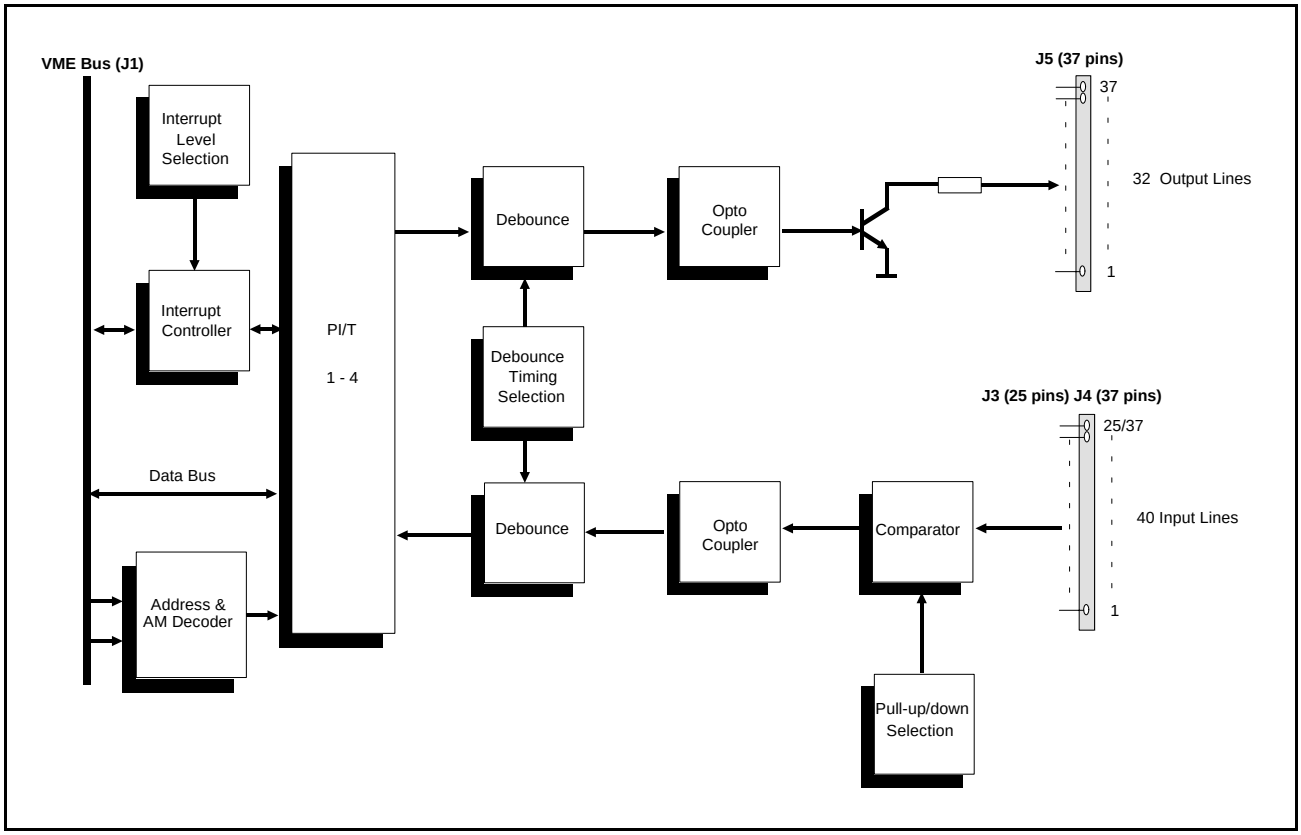
Table 2.1 Jumpers, Connectors and Switches

DESCRIPTION	FUNCTION
J1	VMEbus interface connector
J3	Inputs connector (input 25-40)
J4	Input connector (input 1-24)
J5	Output connector (output 1 - 32)
P1 - P10	Configures the inputs to close to either ground or to the supply voltage
P14 - P16	Input time delay selection
P12, P13	Interrupt level selection
P11	Addressing mode selection
P17	Board base address selection
P18	Watchdog timer disable, enable

2.5 MPV922 Block Diagram

Figure 2.2 shows a functional block diagram of the board.

Figure 2.2 MPV922 Block Diagram



MPV922 Technical Specification

Input Characteristics

Opto-Isolated Inputs : 40 inputs, arranged in 2 banks of 4, and 4 banks of 8 channels
Opto-Isolated I/O Power Supply :+24V (MPV922A)
:+5V (MPV922C)
Input Connector : 1 DB - 25 male connector J3
1 DB - 37 male connector J4
1 DB - 37 female connector J5
Input Stage : Pull-up to +24V/+5V* or pull-down to 0V configurable in blocks of 4 input channels
Input ON/OFF Threshold Voltage
+24V version, MPV922A : Vin(low) = +7.0V, Vin(high) = +9.5V
+5V version, MPV922C : Vin(low) = +2.2V, Vin(high) = +3.2V :
Hysteresis
+24V version, MPV922A : 0.5V
+5V version, MPV922C : 0.1V
Maximum Input Current Drawn On One Channel : ±2.4mA
Input Power Capability : Each bank of four input channels can accept independant power supplies. These power supplies are supplied externally.
Current Drawn Per External Power Supply : 55mA
Input Protection : Protected from input voltage exceeding +24V/+5V* and less than 0V
Anti-bounce Delays : 70µs, 1ms, 7ms jumper selectable
Minimum detectable Signal Width : 27µs
I/O Isolation Voltage : 1500Vrms for 1 minute

Output Characteristics

Opto-Isolated Outputs : 32 outputs, arranged in 4 banks of 8 channels
Output Connector : 1 DB - 37 female connector J5
Output Buffer : Open Collector
Maximum Output Current In The ON state per channel : 150mA
Maximum Output Voltage In The OFF state : 50V
Output Protection : Protected from a power supply polarity inversion
Watchdog Timer : Then selected, if a location is not accessed within a specified time period the outputs will go to the OFF state. (Jumper Selectable)

Interrupt and Timer Characteristics

Interrupt Level : Jumper selectable
Interrupt Support : 16 inputs may assert an interrupt request on a rising or falling edge. Software configurable for each input.
Timers : Four 24 bit counters

Power Requirements

+5V at 1.5A

Environment

Operating Temperature : 0℃ to 60℃
Storage requirements : -25℃ to +85℃
Relative Humidity : 5% to 90% non-condensing

VME Interface

Board Type : Slave
Addressing Modes : A16
Data Mode : Byte D8 (Odd)

** Dependent on board version*

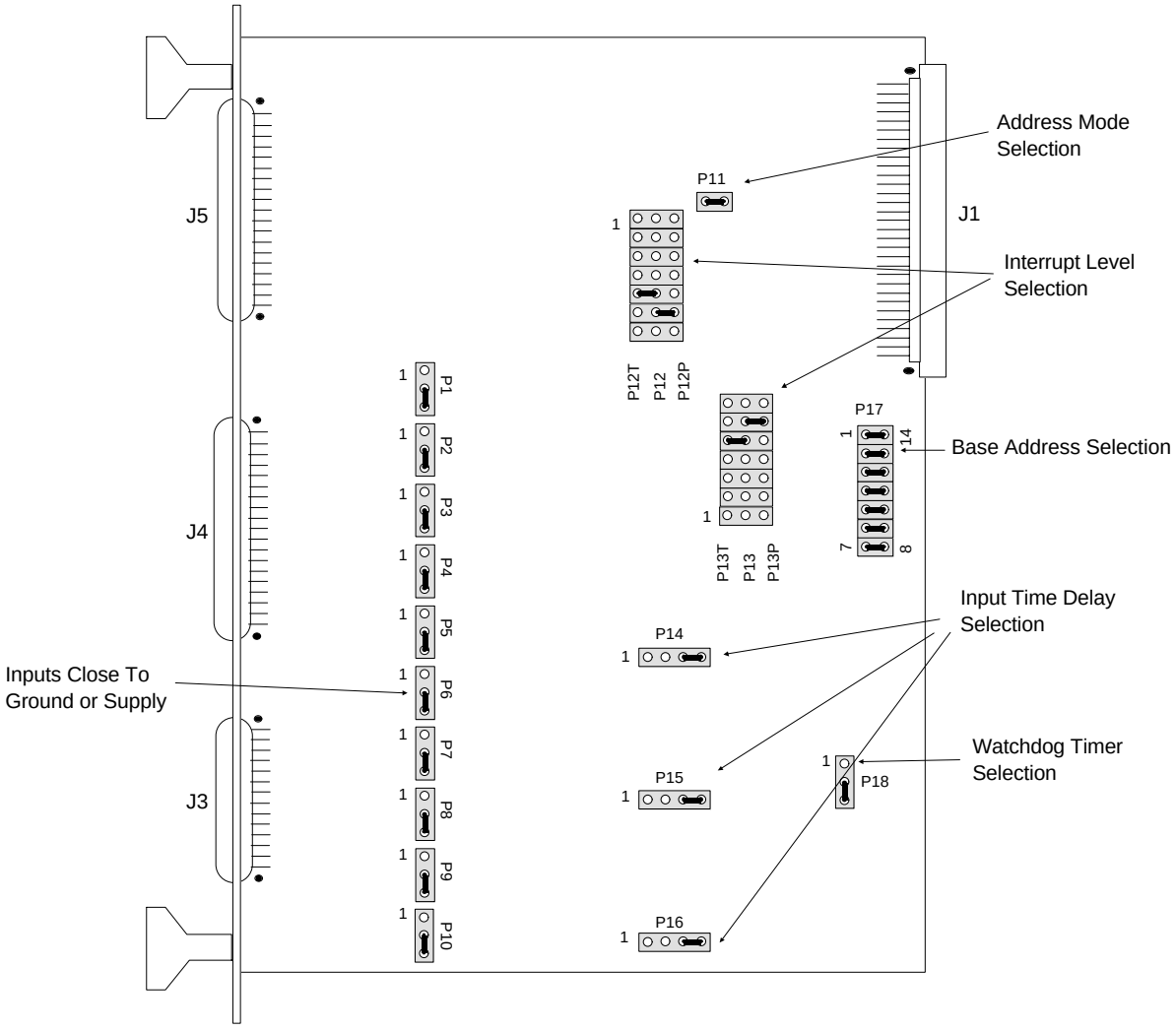
3 - HARDWARE CONFIGURATION

3.1 INTRODUCTION

The **MPV922 Digital Input/Output Board** has a number of user definable options that are selected using a series of jumpers. Boards are supplied in the configuration shown in table 3.1. Users who do not wish to alter the factory set default settings should proceed to chapter 4 "Cables and Connections."

Figure 3.1 Factory Set Default Settings

Jumper/Switch	Setting
P1 - P10	Contacts Closing To 0V
P11	Address Modifiers not decoded
P12, P13	$\overline{\text{PIRQ}}$ generates a level 2 interrupt $\overline{\text{TIRQ}}$ generates a level 3 interrupt
P14, P15, P16	Debounce Delay of 7ms
P17	Base Address FF0000H
P18	Watchdog Timer Disabled



3.2 CHANGING THE BASE ADDRESS

The MPV922 occupies 512byte of space within the system memory map. It may be located on any 512 byte boundary within 64k, provided it does not conflict with the location of any other device already installed in the system. The location of the MPV922 is altered by changing jumper P17 configuration, shown in figure 3.2.

The board is shipped from the factory with a base address of FF0000H.

Table 3.2 shows the correspondence between the address line and the jumper settings. Inserting a jumper asserts a 0 on the corresponding address line, and removing a jumper asserts a 1.

Figure 3.2 P23 Setting

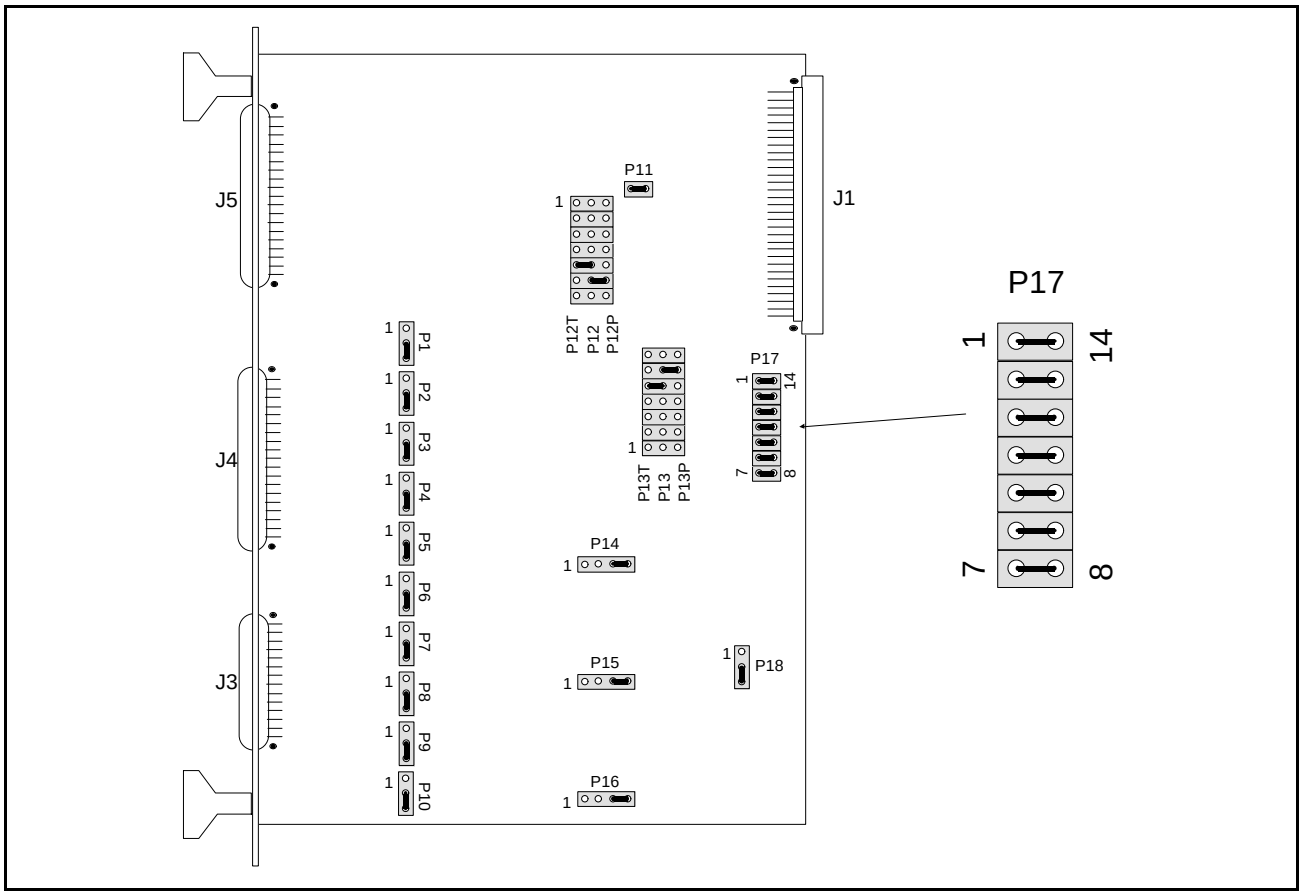


Table 3.2 Summary Of Base Address Options

Pins 7-8 (A15)	Pins 6-9 (A14)	**Pins** 5-10 (A13)	**Pins** 4-11 (A11)	**Pins** 3-12 (A11)	**Pins** 2-13 (A10)	**Pins** 1-14 (A9)	**BASE ADDRESS**
IN	IN	IN	IN	IN	IN	IN	FF0000H
IN	IN	IN	IN	IN	IN	OUT	FF0200H
IN	IN	IN	IN	IN	OUT	IN	FF0400H
IN	IN	IN	IN	IN	OUT	OUT	FF0600H
IN	IN	IN	IN	OUT	IN	IN	FF0800H

and so on until.....

Pins 7-8	**Pins** 6-9	**Pins** 5-10	**Pins** 4-11	**Pins** 3-12	**Pins** 2-13	**Pins** 1-14	**BASE ADDRESS**
OUT	OUT	OUT	OUT	IN	OUT	OUT	FFF600H
OUT	OUT	OUT	OUT	OUT	IN	IN	FFF800H
OUT	OUT	OUT	OUT	OUT	IN	OUT	FFFA00H
OUT	OUT	OUT	OUT	OUT	OUT	IN	FFFC00H
OUT	OUT	OUT	OUT	OUT	OUT	OUT	FFFE00H

3.3 ADDRESS MODIFIER DECODER

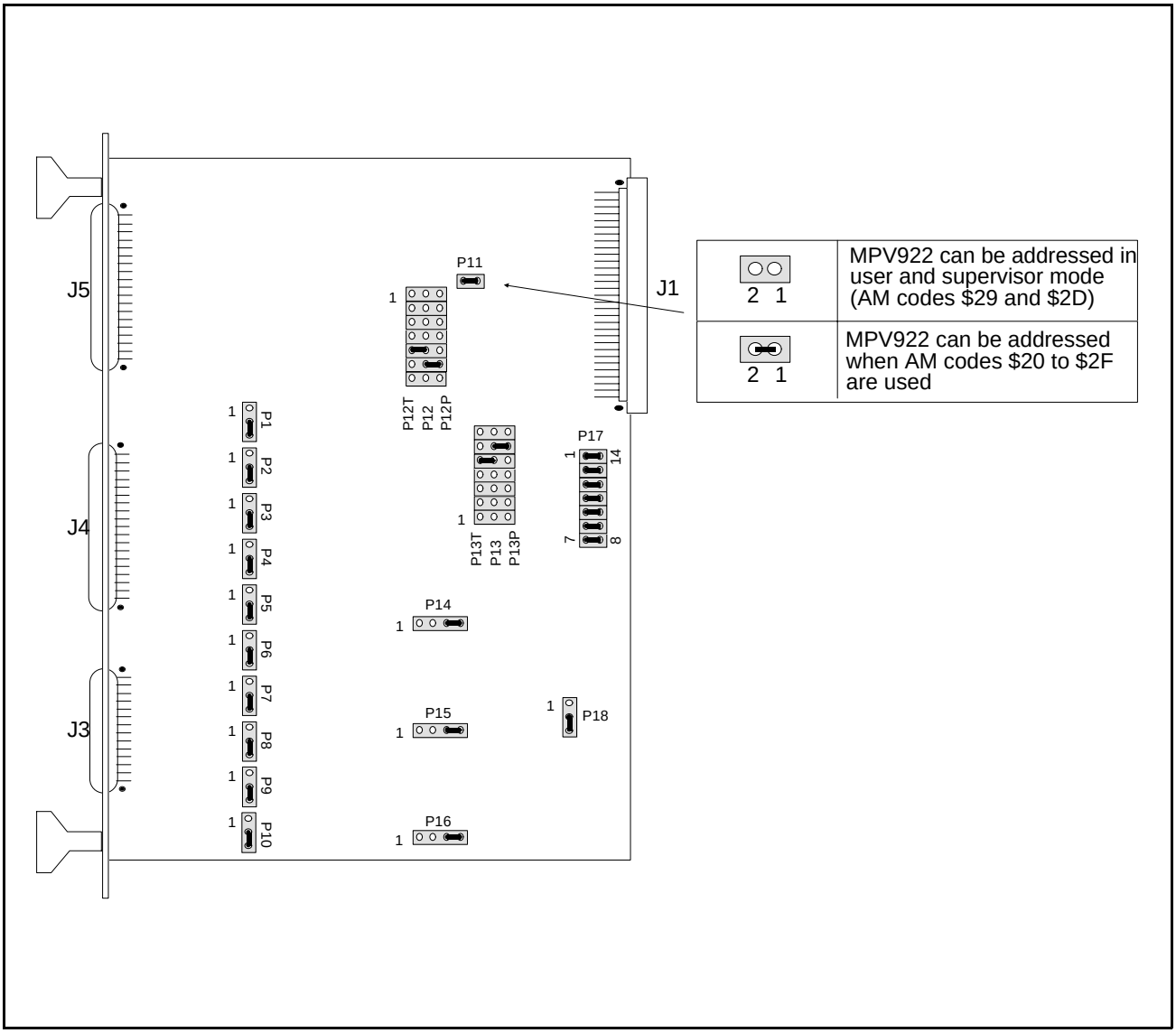
With jumper P11 inserted between pin 1 and pin 2 the board decodes address modifiers. In the short addressing mode the following two modifiers are allowed.

Code $2DH - Short Supervisory I/O Access

Code $29H - Short Non-Privileged I/O Access

Figure 3.3 shows the settings of jumper P11.

Figure 3.3 Address Modifier Decoding



3.4 CONFIGURATION OF THE INPUTS

Jumpers P1 to P10 are used to define the setting of the inputs, i.e., if they close to earth or the supply voltage. The input channels are arranged in groups of four. Table 3.3 shows how the input channels and jumpers are configured.

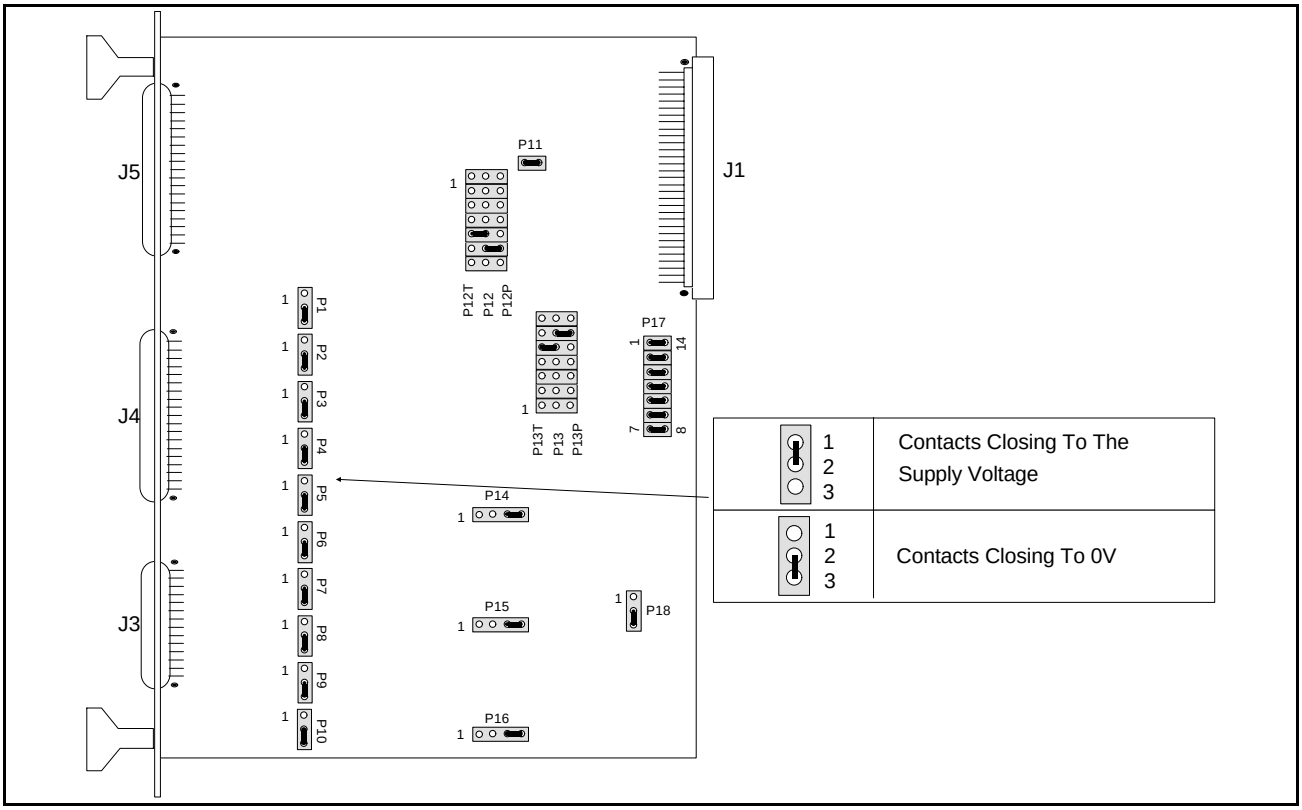
Figure 3.4 shows the possible options for jumpers P1 to P10.

Table 3.3 Input Configuration

GROUP	INPUTS	JUMPER
1	01, 02, 03, 04	P1
2	05, 06, 07, 08	P2
3	09, 10, 11, 12	P3
4	13, 14, 15, 16	P4
5	17, 18, 19 20	P5
6	21, 22, 23, 24	P6
7	25, 26, 27, 28	P7
8	29, 30, 31, 32	P8
9	33, 34, 35, 36	P9
10	37, 38, 39, 40	P10

Note: The input circuit inverts the signal; a low level (0V) on a PI/T pin corresponds to a high level (Vcc) on the corresponding connector.

Figure 3.4 Configuration Of The Inputs



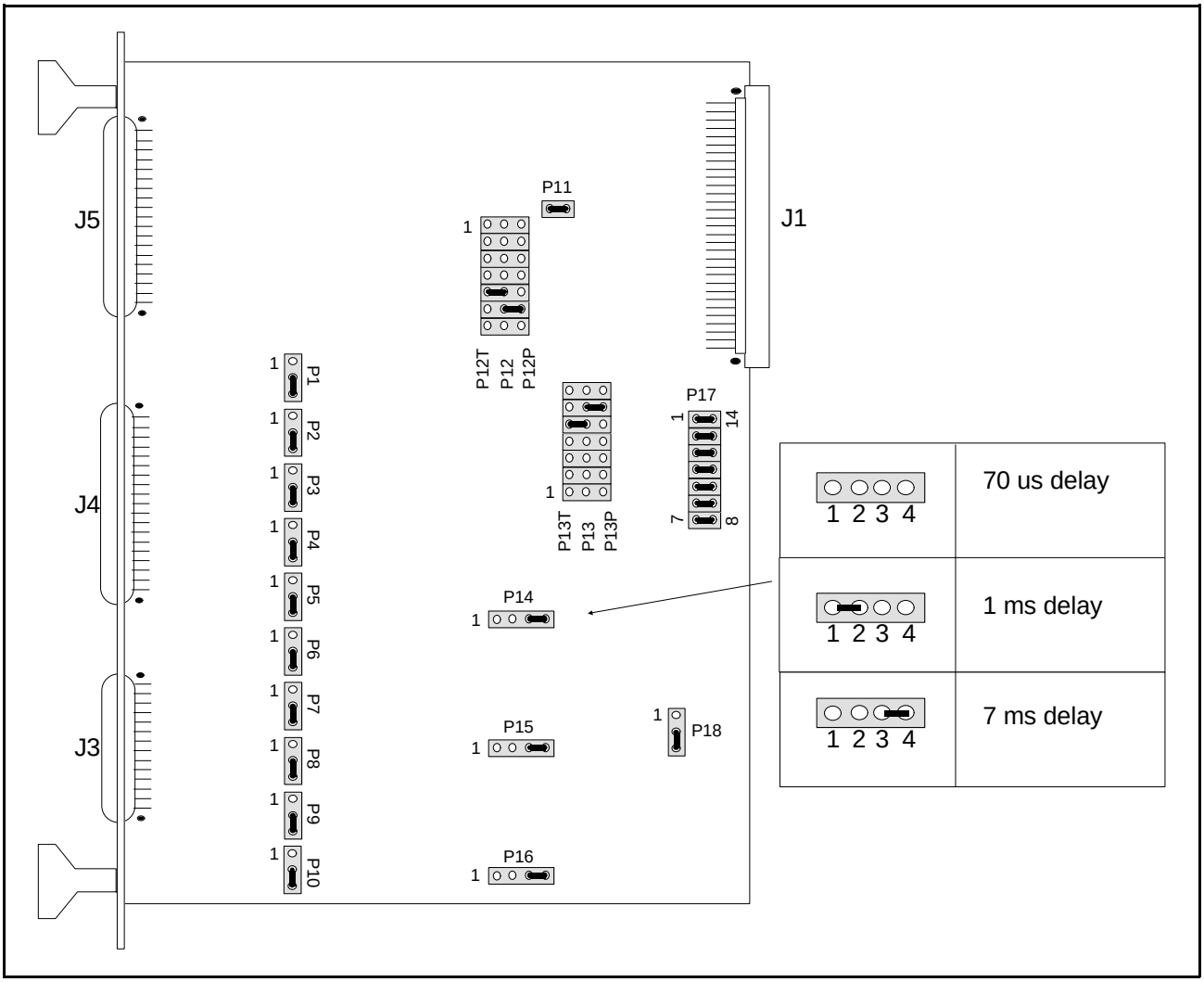
3.5 INPUT TIME DELAY

Debounce circuitry is incorporated to generate a delay between the input channels and the inputs to the PI/T's. The time delays are selected via jumpers P14 - P16. Table 3.4 shows the relationship between jumpers and the input channels. Figure 3.5 shows the time delay options available and the location of the jumpers.

Table 3.4 Relation Of Channels To Jumpers

JUMPER	INPUTS
P14	Input 1 - Input 8
P15	Input 9 - Input 24
P16	Input 25 - Input 40

Figure 3.5 Debounce Time Delay selection



3.6 INTERRUPT LEVEL SELECTION

All sixteen of the inputs, if enabled, and the four timers can generate interrupts on the MPV922. Jumpers P12 and P13 select the level of the interrupt request asserted on the VMEbus (from 1 to 7). The input interrupt is designated the $\overline{\text{PIRQ}}$interrupt, and the timer interrupt is called the $\overline{\text{TIRQ}}$

The location of jumpers P12 and P13 are shown in figure 3.6.

3.6.1 $\overline{\text{PIRQ}}$ INTERRUPT

Table 3.5 shows how to select the required level of interrupt.

Table 3.6 PIRQ Interrupt

JUMPER		VME INTERRUPT LEVEL
P12P - P12	P13P - P13	GENERATED BY PIRQ*
7-7	7-7	1
6-6	6-6	2
5-5	5-5	3
4-4	4-4	4
3-3	3-3	5
2-2	2-2	6
1-1	1-1	7

3.6.2 $\overline{\text{TIRQ}}$ INTERRUPT

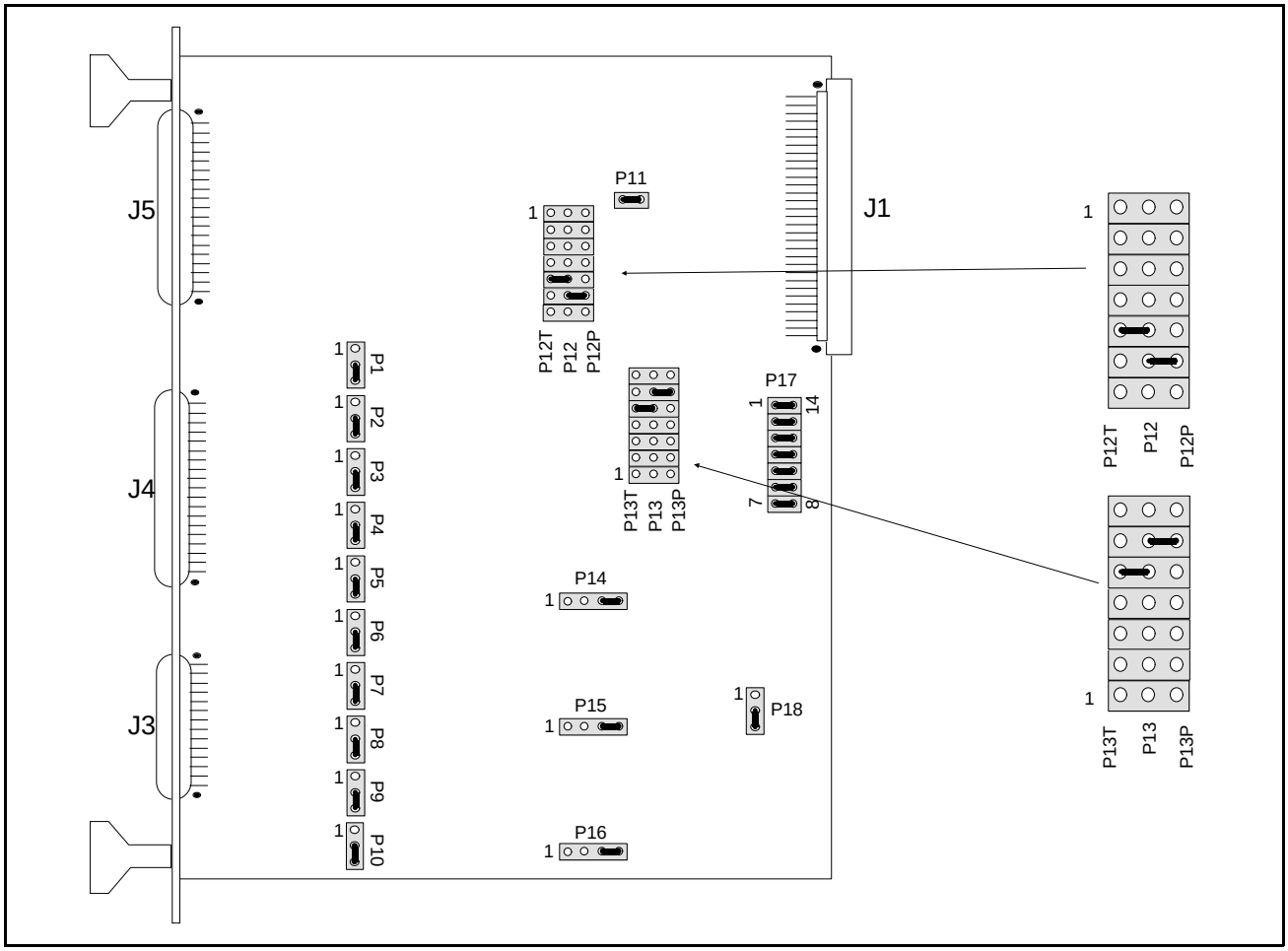
Table 3.7 shows how to select the required level of interrupt.

Figure 3.6 shows the location of the interrupt jumpers.

Table 3.7 TIRQ Interrupt

JUMPER		VME INTERRUPT LEVEL
P12 - P12T	P13 - P13T	GENERATED BY TIRQ*
7-7	7-7	1
6-6	6-6	2
5-5	5-5	3
4-4	4-4	4
3-3	3-3	5
2-2	2-2	6
1-1	1-1	7

Figure 3.6 Interrupt Level Selection



3.7 CONFIGURING THE WATCHDOG TIMER

The MPV922 is provided with a security watchdog mechanism. This mechanism disables all the ouputs until it is retriggered by the master, by means of a periodic write cycle to an address equal to the board base address plus $101.

Jumper P18 allow the watchdog enabling and disabling, see figure 3.7.

3.7.1 SETTING THE TIME DURATION OF THE WATCHDOG

The MPV922 watchdog timer is implemented using a 74LS123 monostable. The output pulse width is defined by the combination of R129 & C47. The location of these components is shown in figure 3.8.

The output pulse width is defined as $tw=0.45CR$

The value of R must not exceed 220kΩ.

For example if R=220kΩ and C=470nF, then tw=46ms (factory set condition).

If the watchdog timer register is not written to prior to the timeout, the board will automatically switch the outputs to the off state (floating output) assuming the watchdog timer is enabled. The timeout period may be altered by changing the value of R & C.

Figure 3.7 Watchdog Timer Enable/Disable

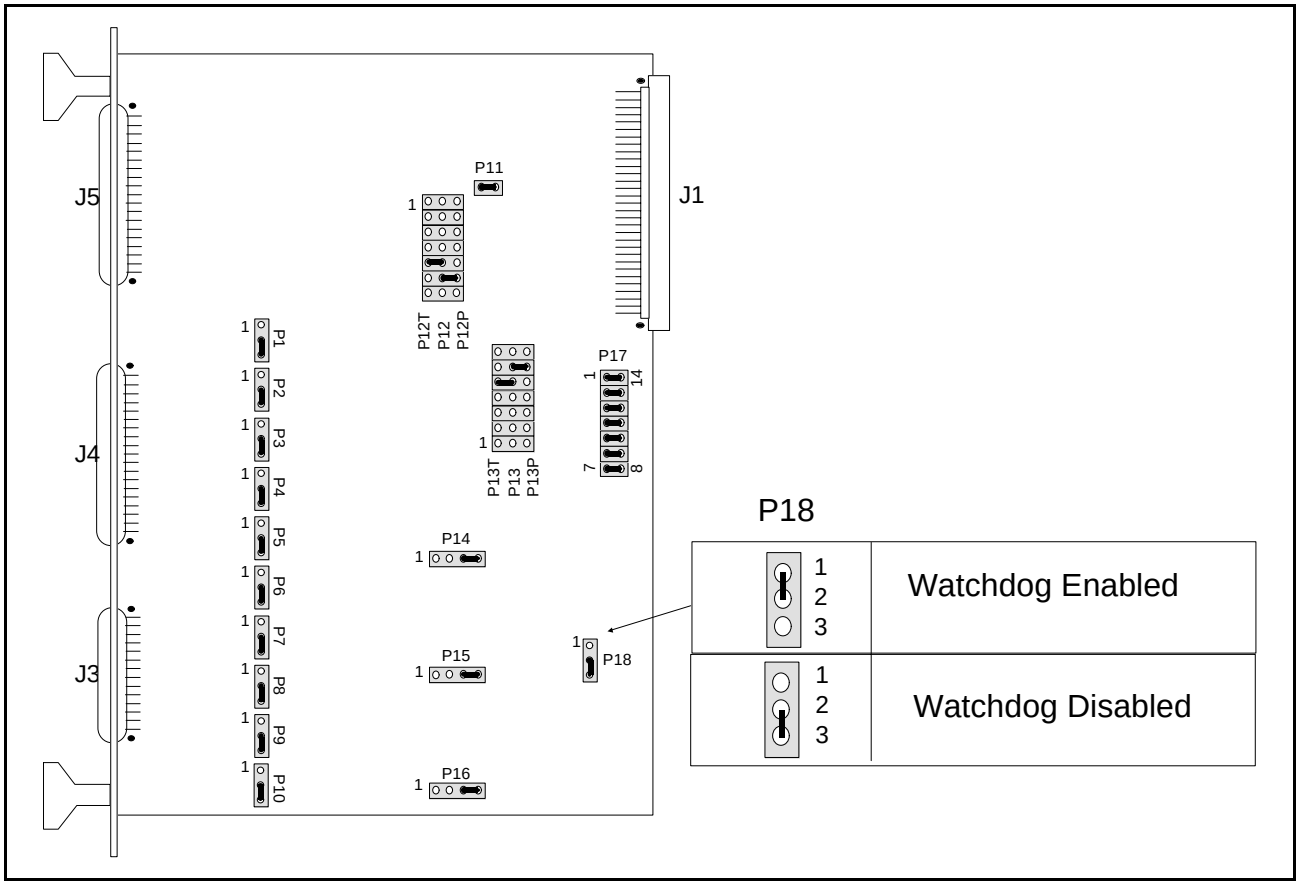
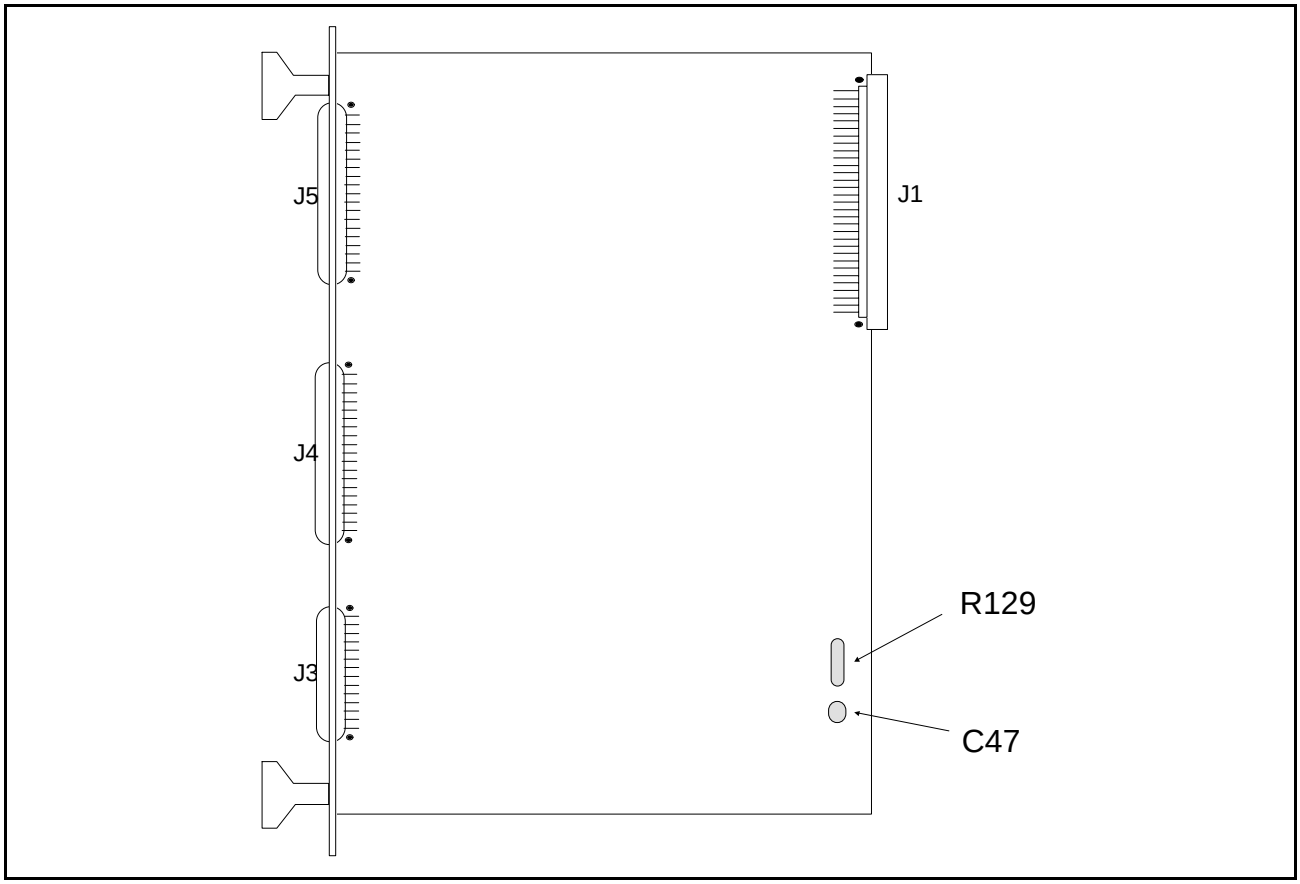


Figure 3.8 Watchdog Timer Components

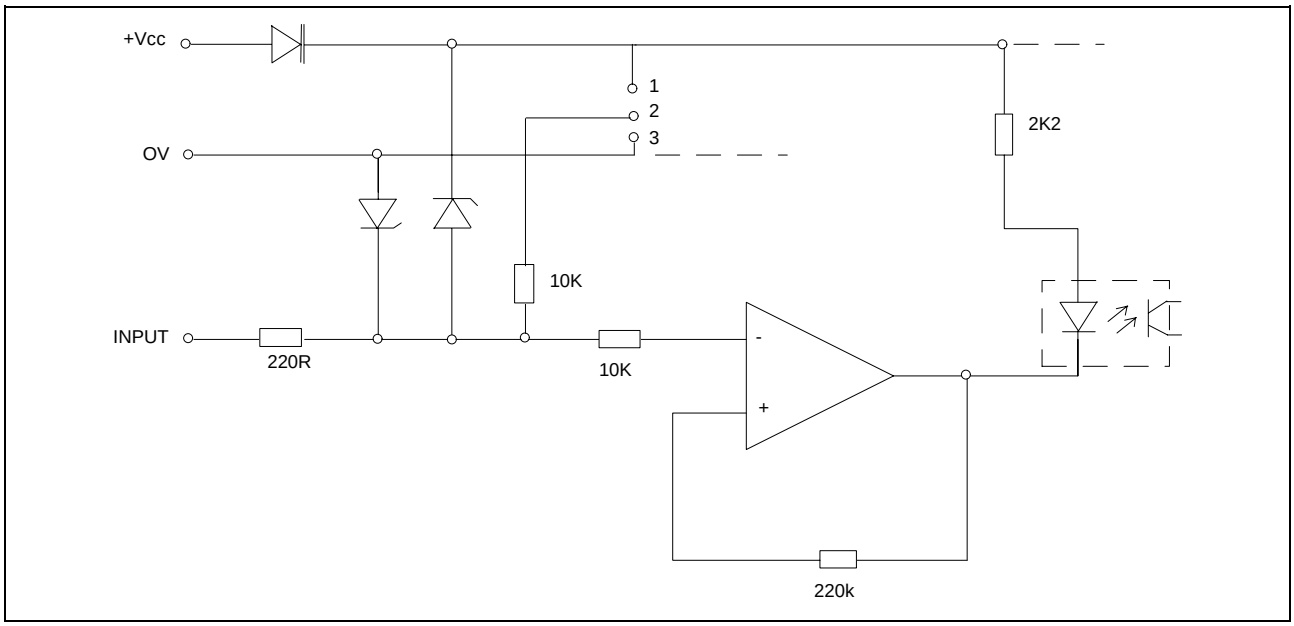


3.8 INPUT / OUTPUT CIRCUIT CONFIGURATION

3.8.1 Input Circuit Configuration

The input circuitry for the MPV922 is detailed in Figure 3.9.

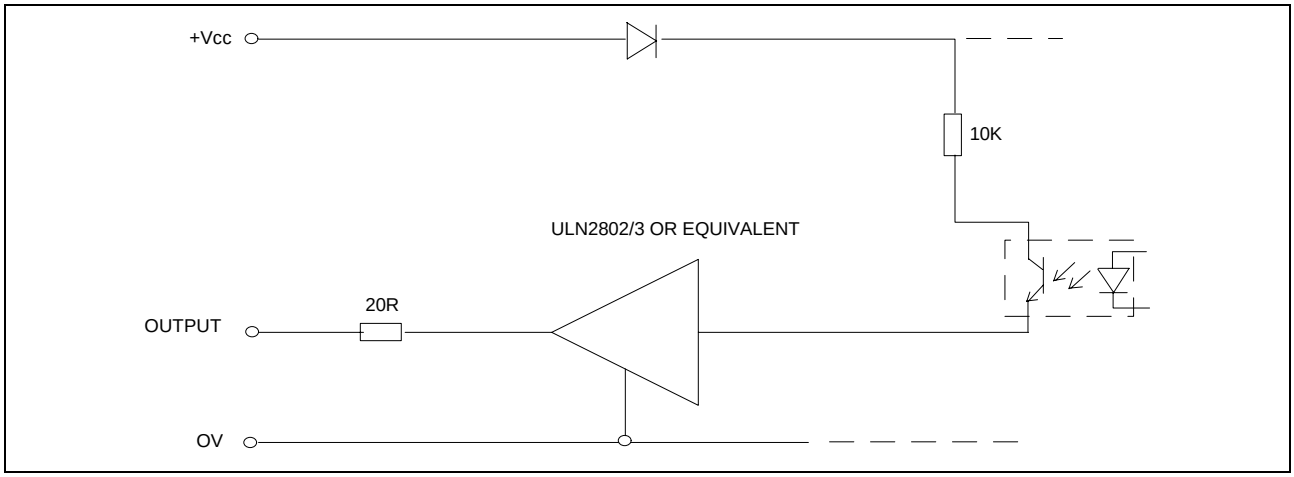
Figure 3.9 Input Circuit Configuration



3.8.2 Output Circuit Configuration

The output circuitry for the MPV922 is detailed in Figure 3.10.

Figure 3.10 Output Circuit Configuration



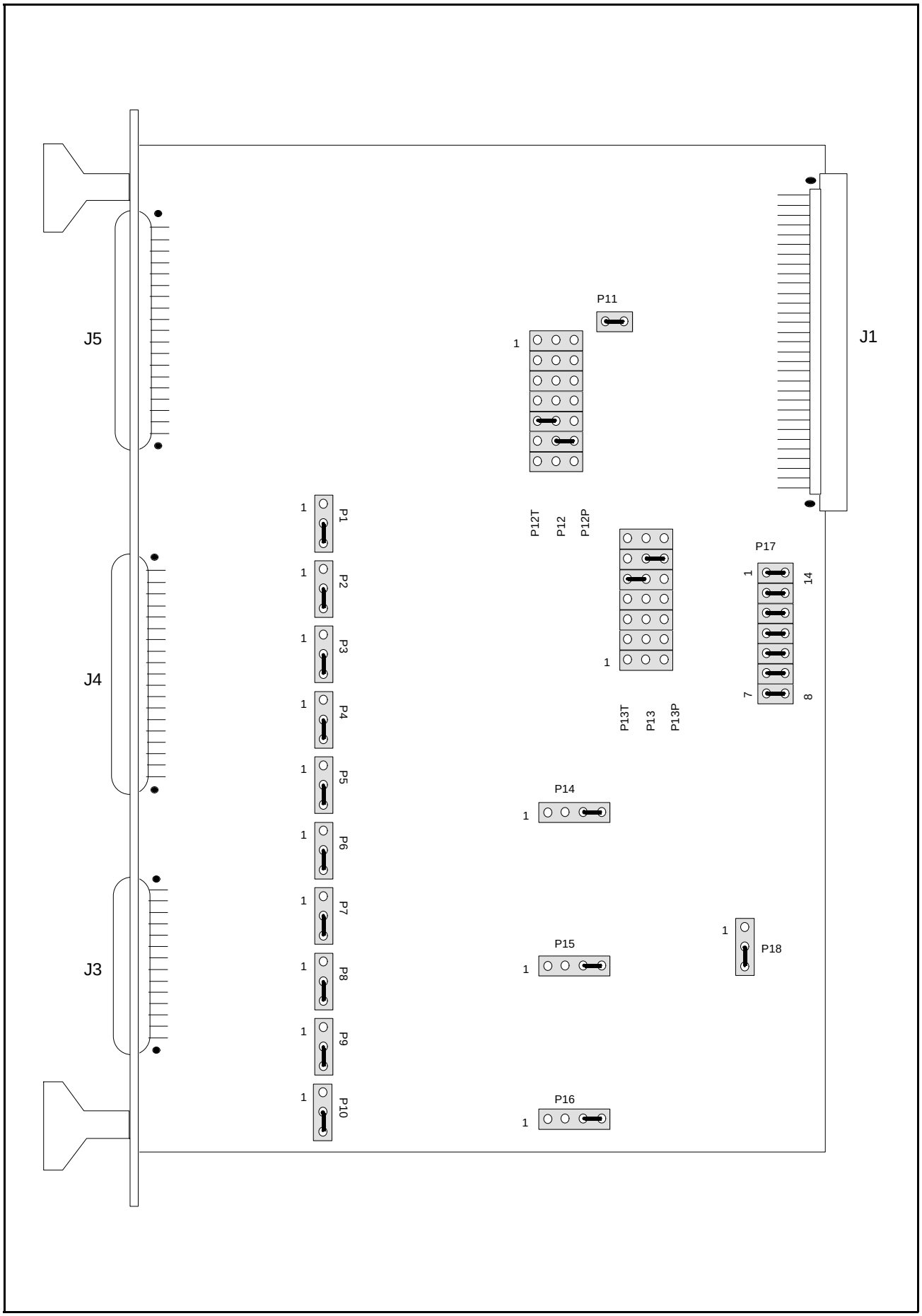
4 - CABLES AND CONNECTIONS

4.1 CONNECTING THE MPV922

Communication between the MPV922 and the VMEbus is performed via the J1 connector on the rear of the board. To install the MPV922 in the system, carefully align connectors J1 with the corresponding J1 connectors on the VMEbus backplane and press firmly home.

Ensure that power to the VMEbus system is turned off before installing the MPV922. The MPV922 is sensitive to the build-up of static electricity, therefore normal anti-static precautions should be observed when handling the board.

Figure 4.1 Location Of Connectors



4.2 CONNECTOR PIN ASSIGNMENTS

4.2.1 P1 Pin Assignment

The 96-way J1 connector on the MPV922 mates with J1 connector on the VMEbus Backplane.

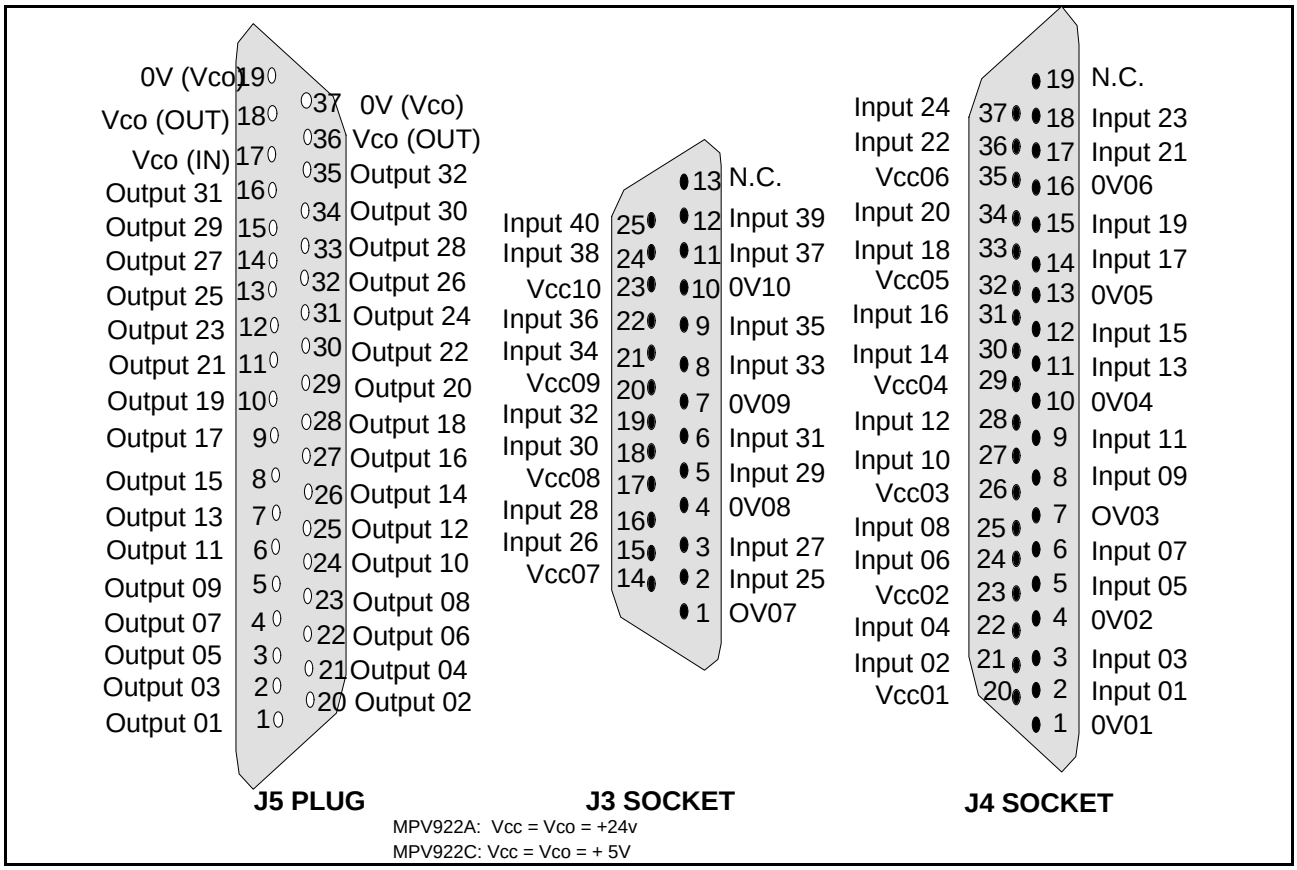
Table 4.1 J1 Pin Assignment

Pin	(a)	(b)	(c)	Pin	(a)	(b)	(c)
1	D00	N.C.	N.C.	**17**	GND	AM1	A21
2	D01	N.C.	N.C.	**18**	AS*	AM2	A2
3	D02	N.C.	N.C.	**19**	GND	AM3	A19
4	D03	BG0IN*	N.C.	**20**	IACK*	GND	A18
5	D04	BG0OUT*	N.C.	**21**	IACKIN*	N.C.	A17
6	D05	BG1IN*	N.C.	**22**	IACKOUT*	N.C.	A16
7	D06	BG1OUT*	N.C.	**23**	AM4	GND	A15
8	D07	BG2IN*	N.C.	**24**	A07	IRQ7*	A14
9	N.C.	BG2OUT*	GND	**25**	A06	IRQ6*	A13
10	SYSCLK	BG3IN*	N.C.	**26**	A05	IRQ5*	A12
11	GND	BG3OUT*	N.C.	**27**	A04	IRQ4*	A11
12	N.C.	N.C.	SYSRESET*	**28**	A03	IRQ3*	A10
13	DS0*	N.C.	N.C.	**29**	A02	IRQ2*	A09
14	WRITE*	N.C.	AM5	**30**	A01	IRQ1*	A08
15	GND	N.C.	A23	**31**	N.C.	N.C.	N.C.
16	DTACK*	AM0	A22	**32**	+5V	+5V	+5V

4.3 DIGITAL INPUT/OUTPUT CONNECTIONS (J3, J4 & J5)

Up to 32 digital outputs and 40 digital inputs can be connected to the MPV922. The pin assignments for the three front panel connectors are shown in figure 4.2.

Figure 4.2 Input Connections



4.3.1 INPUT POWER SUPPLIES

Forty inputs, divided into 10 groups of 4 inputs, are available. For each group of 4 a separate power supply can be connected. Each group will be an independent power supply, table 4.2 shows the assignment of the inputs and their independent power supply.

4.3.2 OUTPUT POWER SUPPLIES

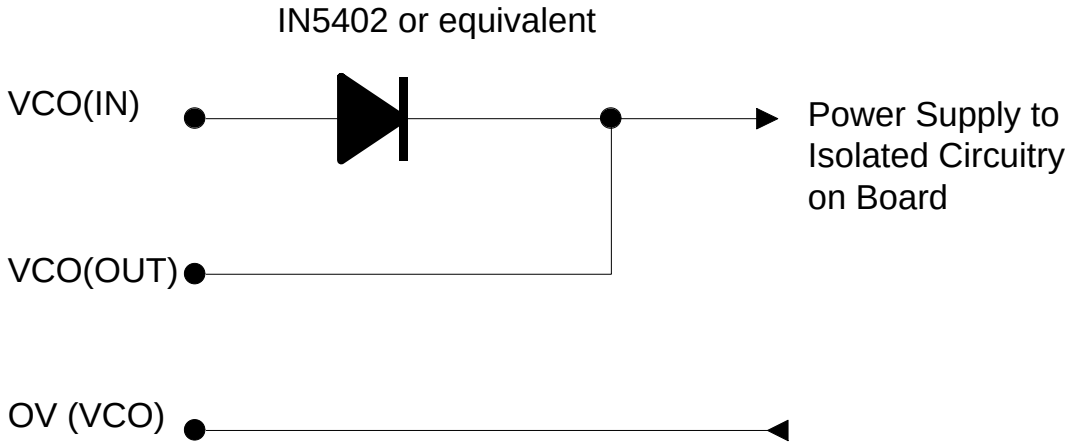


Table 4.2 Inputs & Power Supply Configuration

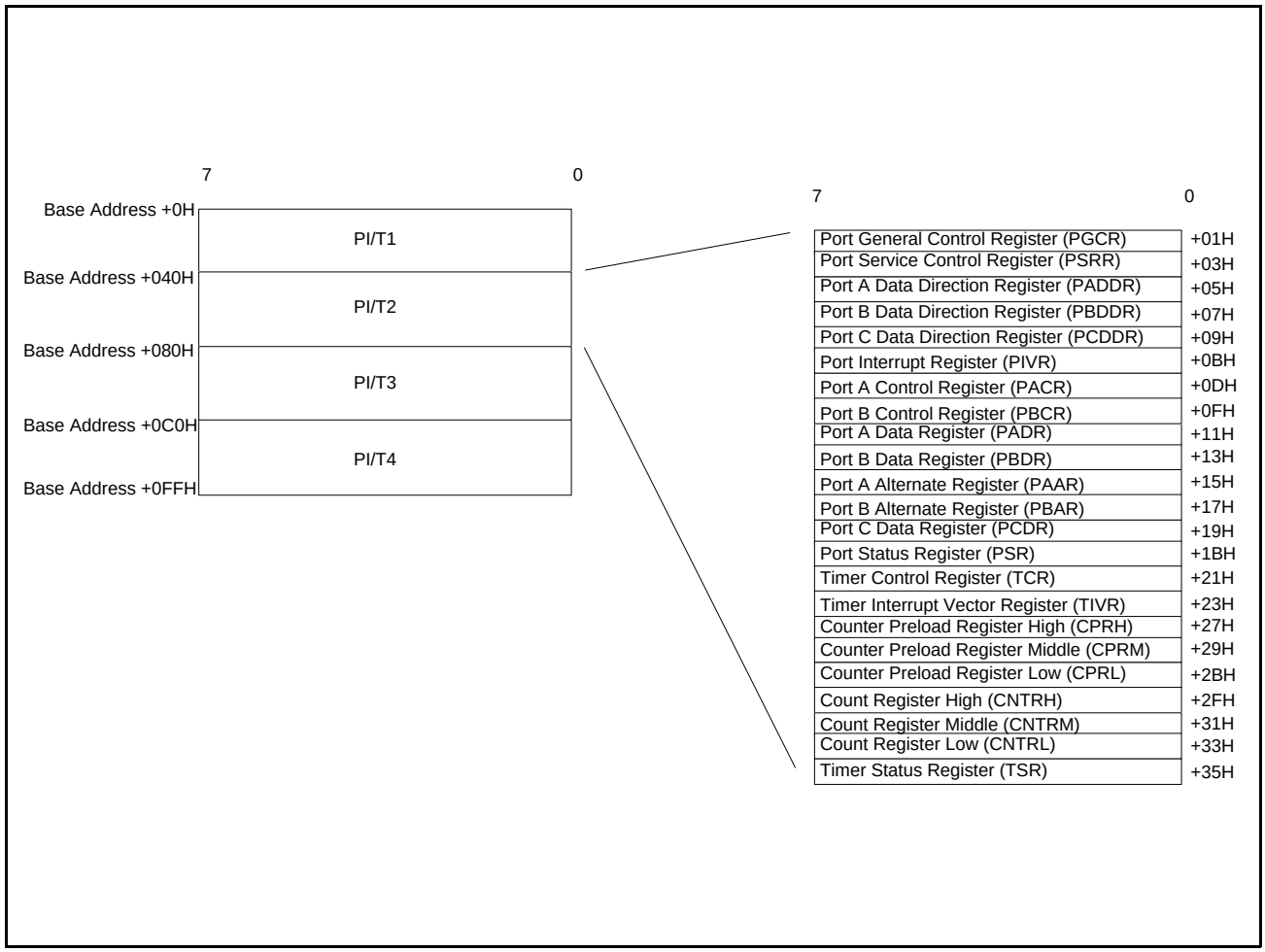
Group	Inputs	Power Supply
1	Input01-Input04	0V 01, Vcc 01
2	Input05-Input08	0V 02, Vcc 02
3	Input09-Input12	0V 03, Vcc 03
4	Input13-Input16	0V 04, Vcc 04
5	Input17-Input20	0V 05, Vcc 05
6	Input21-Input24	0V 06, Vcc 06
7	Input25-Input28	0V 07, Vcc 07
8	Input29-Input32	0V 08, Vcc 08
9	Input33-Input36	0V 09, Vcc 09
10	Input37-Input40	0V 10, Vcc 10

5.1 INTRODUCTION

The MPV922 occupies 512byte of locations within the VME address space. Figure 5.1 shows a memory map of the board. The inputs to the board are controlled by four MC68230 Parallel Interface/Timers (PI/T's). It is important that the PI/T's are initialised correctly, see the Motorola MC68230 manual provided.

5.2 MC68230

Figure 5.1 MPV921 Memory Map



The location of the four PI/T's is also shown in figure 5.1, their locations are also shown in table 5.1 below. VME address lines A06 and A07 are used to identify the individual PI/T's.

Table 5.1 PI/T Memory Locations

PI/T	OFFSET
1	0
2	40H
3	80H
4	C0H

5.3 MPV922 OUTPUTS

The configuration of the outputs to the MC68320 is shown in the table 5.2 and table 5.3. VME address lines A01 to A05 identify the specific registers within the PI/T's.

Table 5.2 PI/T Registers

INPUTS	REGISTER	PI/T	OFFSET
Output01 - Output08	PBDR	3	93H
Output09 - Output16	PBDR	4	D3H
Output17 - Output24	PADR	3	91H
Output25 - Output32	PADR	4	D1H

Table 5.3 PI/T Memory Locations

PI/T	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
3	PBDR	08	07	06	05	04	03	02	01
4	PBDR	16	15	14	13	12	11	10	09
3	PADR	24	23	22	21	20	19	18	17
4	PADR	32	31	30	29	28	27	26	25

5.3.1 EXAMPLE

If we wish to set the status of outputs 25-32, these outputs are mapped in register PADR of PI/T number 4 (see table 5.3). Assuming that the board base address has been set at $FF0400H, then it is necessary to perform a write cycle at address $FF04D1, see below.

$FF0400H	Board Base Address
$ 11H	Address for PADR Register
$ 40H	Offset PI/T number 4
$FF04D1H	

5.4 EXAMINING THE OUTPUTS

It is possible to examine the logical state by reading the PAAR and PBAR read only registers, the offsets with respect to the base address is shown in table 5.4 below.

Table 5.3 PI/T Memory Locations

PI/T	REGISTER	OFFSET
3	PBAR	97H
4	PBAR	D7H
3	PAAR	95H
4	PAAR	D5H

5.5 MPV922 INPUTS

The inputs to the board can be accessed by reading the locations shown in table 5.5 and table 5.6.

Table 5.5 PI/T Input Registers

INPUTS	REGISTER	**PI/T**	**OFFSET**
Input 01-04	PSR	3	9BH
Input 05-08	PSR	4	DBH
Input 09-16	PADR	1	11H
Input 17-24	PBDR	1	13H
Input 25-32	PADR	2	51H
Input 33-40	PBDR	2	53H

Table 5.6 PI/T Input Memory Locations

PI/T	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
3	PSR	04	03	02	01				
4	PSR	08	07	06	05				
1	PADR	16	15	14	13	12	11	10	09
1	PBDR	24	23	22	21	20	19	18	17
2	PABR	32	31	30	29	28	27	26	25
2	PBDR	40	39	38	37	36	35	34	33

5.6 INPUT GENERATED INTERRUPTS

The 16 inputs listed in table 5.7 are capable of generating interrupts.
The MC68230 PI/T manual describes interrupt request handling.

Table 5.7 Input Generated Interrupts

MPV922 INPUT	PI/T INPUT	**PI/T**
Input 01	H1	3
Input 02	H2	3
Input 03	H3	3
Input 04	H4	3
Input 05	H1	4
Input 06	H2	4
Input 07	H3	4
Input 08	H4	4
Input 15	H1	1
Input 16	H2	1
Input 17	H3	1
Input 18	H4	1
Input 31	H1	2
Input 32	H2	2
Input 33	H3	2
Input 34	H4	2

5.7 TIMER GENERATED INTERRUPTS

The 4 registers listed in table 5.8 are capable of generating interrupts.
The MC68230 PI/T manual details the timer interrupt operation.

Table 5.8 Timer Generated Interrupts

TIMER	REGISTER	**PI/T**	**OFFSET**
TIRQ 1	TCR	1	21 H
TIRQ 2	TCR	2	61 H
TIRQ 3	TCR	3	A1 H
TIRQ 4	TCR	4	E1 H

5.8 WATCHDOG TIMER

5.8.1 Watchdog Timer Register = Base Address + Offset$101

The watchdog timer disables all outputs, unless it is re-triggered by writing any value to its register within the timeout period. Refer to section 3.7.

The outputs can be re-enabled by writing to the register, should the register not be written to within the timeout period.