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Modular Computers ®

CP604-PM

6U CompactPCI
Pentium III-based Peripheral CPU Board

Manual ID 22654, Rev. Index 02
Mar 01

The product described in this manual is in compliance with all applied CE standards.

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Revision History

Revision History			
Manual/Product Title:	**CP604-PM**		
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01	Initial Issue	00	Feb. 01
02	Addition of rear I/O appendix	00	Mar. 01

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Explanation of Symbols



CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please see also the section “Applied Standards” in this manual.



Caution!

This symbol and title warn you of hazards due to electrical shocks (> 60 V) when touching products or parts of them. Failure to observe the necessary precautions as described and/or prescribed by the law may result in damage to your product and/or endanger your life/health.

Please see also the section “High Voltage Safety Instructions”.



ESD-Sensitive Device!

This symbol and title highlight the fact that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following pageof this manual.



Attention!/Warning!

This symbol and title emphasize aspects which, if not understood and taken into consideration by the reader, may result in hazards to health and/or material damage.



PEP Advantage

This symbol and title accompany information highlighting positive aspects of a *PEP* product and/or procedure.



Troubleshooting

This symbol and title accompany information about troubleshooting and problem solving.



Note:

This symbol and title relate to useful/important supplementary information.

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For your safety

Your new *PEP* product has been developed and carefully tested in order to provide all the features necessary to ensure full compliance with all electrical safety requirements. It has also been designed for a long fault-free life. However, the life expectancy of your product will be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interests of your own safety and of the correct operation of your new *PEP* product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions



Warning!

All operations on this device must be carried out by sufficiently skilled personnel.



Caution!

The power supply must always be disconnected before installation, repair and maintenance operations are carried out on this product. Failure to comply with this basic precaution will subject the operator to serious electrical shock hazards. Always unplug the power cable before such operations.
Before installing your new *PEP* product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Care must therefore be exercised at all times during handling and inspection of the board, in order to ensure product integrity.

- Do not handle this product while it is outside its protective enclosure while it is not used for operational purposes, unless it is otherwise protected.
- Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where safe work stations are not guaranteed, it is important for the user to be electri-cally discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.
- It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or tracks on the board.

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General Instructions on Usage

- In order to maintain *PEP's* product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by *PEP Modular Computers* and described in this manual or received from *PEP* Technical Support as a special handling instruction, will void your warranty.
- This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.
- In performing all necessary installation and application operations, please, follow only the instructions supplied by the present manual.
- Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.
- Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instructions on the previous page of this manual.

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Two Year Warranty

PEP Modular Computers grants the original purchaser of a *PEP* product a ***TWO YEAR LIMITED HARDWARE WARRANTY*** as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of *PEP* are valid unless the customer has the express written consent of *PEP Modular Computers*.

PEP Modular Computers warrants their own products, excluding software, to be free from manufacturing and material defects for a period of 24 consecutive months from the date of purchase. This warranty is not transferable nor extendible to cover any other users or long-term storage of the product. It does not cover products which have been modified, altered or repaired by any other party than *PEP Modular Computers* or their authorized agents. Furthermore, any product which has been, or is suspected of being damaged as a result of negligence, improper use, incorrect handling, servicing or maintenance, or which has been damaged as a result of excessive current/voltage or temperature, or which has had its serial number(s), any other markings or parts thereof altered, defaced or removed will also be excluded from this warranty.

If the customer's eligibility for warranty has not been voided he should, in the event of any claim, return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application in which the product has been used and a description of the defect. Please pack the product in such a way as to ensure safe transportation (see our safety instructions).

PEP provides for repair or replacement of any part, assembly or sub-assembly at the company's own discretion, or to refund the original cost of purchase, if appropriate. In the event of repair, refunding or replacement of any part, the ownership of the removed or replaced parts reverts to *PEP Modular Computers*, and the remaining portion of the original guarantee, or any new guarantee to cover the repaired or replaced items, will be transferred to cover the new or repaired items. Any extensions to the original guarantee are considered gestures of goodwill, and will be defined in the "Repair Report" issued by *PEP* with the repaired or replaced item.

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Chapter 1

Introduction

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1. Introduction

1.1 Introduction to CompactPCI

The CompactPCI board described in this manual operates with the PCI bus architecture to support additional I/O and memory-mapped devices as required by various industrial applications. For detailed information concerning the CompactPCI standard, please consult the complete Peripheral Component Interconnect (PCI) and CompactPCI Specifications. For further information regarding these standards and their use, visit the homepage of the *PCI Industrial Computer Manufacturers Group (PICMG)*.

Many system-relevant CompactPCI features that are specific to *PEP Modular Computers* CompactPCI systems may be found described in the *PEP* CompactPCI System Manual. Due to its size, this manual cannot be downloaded via the internet. Please refer to the section “Related Publications” at the end of this chapter for the relevant ordering information.

The CompactPCI System Manual includes the following information:

- Common information that is applicable to all system components, such as safety information, warranty conditions, standard connector pinouts etc.
- All the information necessary to combine *PEP's* racks, boards, backplanes, power supply units and peripheral devices in a customized CompactPCI system, as well as configuration examples.
- Data on rack dimensions and configurations as well as information on mechanical and electrical rack characteristics.
- Information on the distinctive features of *PEP* CompactPCI boards, such as functionality, hotswap capability. In addition, an overview is given for all existing *PEP* CompactPCI boards with links to the relating datasheets.
- Generic information on the *PEP* CompactPCI backplanes, such as the slot assignment, PCB form factor, distinctive features, clocks, power supply connectors and signalling environment, as well as an overview of the *PEP* CompactPCI standard backplane family.
- Generic information on the *PEP* CompactPCI power supply units, such as the input/output characteristics, redundant operation and distinctive features, as well as an overview of the *PEP* CompactPCI standard power supply unit family.

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1.2 *PEP* Double-height CPU Boards

The CP604 is a high performance 64-bit/33 MHz CompactPCI system controller board designed to utilize the Intel® Mobile Pentium®III Coppermine™ microprocessors and future processors. This board is based on the Intel® 440BX AGP sets and can support CPU speeds of 400 MHz through 700 MHz and host bus speeds up to 100 MHz.

The CP604-PM is a non-system controller which is identical to the CP604 apart from having a different PCI/PCI (non-transparent) bridge at J1/J2. This makes possible the addition of further CP604-PM's together with a system controller CPU on one CompactPCI bus, i.e. multiprocessing.

1.3 CP604-PM Product Overview

The CP604-PM is a highly integrated single-board computer that is designed around the Intel® Mobile Pentium® III family of microprocessors.

The principal difference between the system controller board CP604 and the peripheral controller CP604-PM lies in the nature of the CompactPCI architecture. The system controller generates all necessary PCI control signals, reset, clock and arbitration, and uses a transparent bridge for the PCI interface, therefore all PCI devices are visible to the CP604 and all standard drivers may be used.

The CP604-PM uses a non-transparent PCI bridge, a so called "drawbridge". This bridge is specifically designed to bridge between two processor domains, one on the CompactPCI interface and the other local on the CP604-PM controller. The drawbridge is the first PCI bridge to enable multiprocessing on a CompactPCI system. This bridge can isolate two PCI busses.

The CP604-PM with all onboard PCI devices is to the CompactPCI bus visible as a single PCI device. With this configuration the CP604 could control all PCI devices on the CompactPCI bus, while the CP604-PM controls all onboard PCI devices.

The CP604-PM is hotswappable, which means it may be installed in and removed from a hotswap compliant backplane whilst the system is powered-up and running. The board may also be used in a standard CompactPCI system without Hotswap support.

Communication between the master CP604 and the peripheral CP604-PM may be effected via the *PEP* TCP/IP backplane software package RackNet.

Finding an optimum equilibrium between performance and power dissipation, the CP604-PM is a reliable Mobile Pentium®III controlled board supporting a clock speed of 400 Mhz through 700 MHz and higher when available.

The onboard PCI bus supports two Fast Ethernet ports and one PMC slot. System features include soldered memory options between 256 MB up to 2 GB (with optional ECC support), high-performance AGP VGA video support with CRT and LVDS output, two IDE ports, four COM ports, a parallel port, two USB interfaces, an optional onboard Flash disk (DiskOnChip or 2.5" Flash Disk) and an independent IPMI compliant baseboard management controller.

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Designed for stability and packaged in a rugged format, the board fits into all applications situated in industrial environments. The low power consumption of the board is further assured through the use of 3.3 V and 1.5V I/O technology.

The board is compatible with the Microsoft Windows NT® operating system. However, the performance of CompactPCI can be tailored to suit real-time applications and operating systems such as Linux®, QNX® or VxWorks® which are instrumental to the success of CompactPCI in these market sectors.

All standard PC interfaces are implemented and assigned to the front panel and to the rear connectors J3, J4 and J5.

1.4 CP604-PM Board Introduction

The CP604-PM is a CompactPCI Mobile Pentium®III Coppermine™ based single-board computer specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

The CP604-PM's outstanding features include:

- suitable for all Intel® Mobile Pentium®III Coppermine™ processors in the 495-pin BGA2 package
- compliance with 64-bit CompactPCI Interface 2.0 R3.0 at 33 MHz
- compliance with CompactPCI hotswap specificaton PICMG 2.1, version 1,0
- 4HP 6U CompactPCI
- up to 2 GB SDRAM main memory with ECC
- 256 kB FLASH for BIOS
- 4 MB onboard Flash
- Flash Disk up to 288 MB
- two EIDE interfaces
- onboard 2.5" EIDE device: HDD or Flash disk
- two Fast Ethernet devices which each support 10BaseT & 100BaseTX
- onboard high performance AGP VGA controller with CRT and LVDS output
- integrated Hardware monitor
- IPMI compliant baseboard management controller
- rear I/O on J3, J5 and optionally on J4
- floppy disk interface
- keyboard/USB controller
- four serial ports(ESD protected and EMI compliant)
- counter/timers
- watchdog timer
- real-time clock
- parallel port
- PMC interface with Rear I/O support and breakout on Front Panel

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1.5 CP604-PM Main Specifications

Table 1-1: CP604-PM Main Specifications

CP604-PM	Specifications
CPU	Intel® Mobile Pentium®III Coppermine™ processor up to 700 MHz with 256 kB L2 on-die cache in 495 BGA2 packaging
Memory	100 MHz system memory bus 256 kB L2 on-die full speed processor cache BX memory support: 256 MB up to 512 MB soldered with ECC and up to 1 GB SDRAM with memory extension module GX memory support: 256 MB up to 1 GB soldered with ECC and up to 2 GB SDRAM with memory extension module 512 kB Flash (or optional SRAM with 256 kB or 512 kB) 4 MB soldered Flash memory Optional DiskOnChip™ module up to 288 MB 2 x 256 byte EEPROM for storing CMOS data when operating without battery and 2 x 256 byte EEPROM for user purposes
Super I/O	The FDC37C672 from SMSC is an ISA Plug and Play compatible I/O device that provides the following functions: - Two 16C550 compatible COM ports with 16 bytes FIFO - PS/2 keyboard and mouse interface - Floppy disk controller up to 2.88 MB - Parallel port ECP/EPP compatible
UART	Dual UART, 16C550 compatible, with support for an additional two COM ports
Chipset	Intel® 82440BX or 82440GX PCI/AGP controller - GTL processer interface - Integrated DRAM controller: BX up to 1 GB and GX up to 2 GB - AGP and PCI interface Intel® 82371EB PCI/ISA EIDE Xcelerator (PIIX4E) - Multifunction PCI to ISA bridge - Enhanced DMA controller - Interrupt controller based on two 82C59's - Timer based on 82C84 - Real-time clock - Power management logic - Supports two USB interfaces - Supports two EIDE interfaces
AGP/VGA Interface	Controller: 69030 Video memory: 4 MB Resolution: up to 1600x1200x16 bits per pixel @ 60 Hz two independent video data output channels one Flatpanel LVDS interface one CRT output
Fast Ethernet Interfaces	Controller: two Intel® 82559ER Fast Ethernet controllers Data Rate: 10 & 100 MBit/s Ethernet: Full 802.2 & 802.3 IEEE compliance supporting 10Base-T and 100Base-TX Cabling: Category 5 two-pair cabling

Table continued on following page

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Table 1-1: CP604-PM Main Specifications

CP604-PM	Specifications
IPMI	Onboard independent IPMI compliant baseboard management (BMC) controller The Qlogic Zircon LT BMC controls all onboard voltages, the CPU temperature and optional external fans connected via the rear I/O interface J4 and J3
CompactPCI Bus Interface	Compatible with CompactPCI Specification V 2.0, Rev. 3.0 and CompactPCI Hotswap specification PICMG 2.1 version 1.0 64-bit/33 MHz peripheral interface 3.3V/5.0V compatible (Intel drawbridge 21554/21555)
Rear I/O	To optimize cabling rear I/O is available via the J3, J5 and, optionally, J4 connectors in conjunction with the Rear I/O transition module CP-RIO6-04 The IPMI control signals and the COM3 and COM4 TTL signals are only available on the Rear I/O interface
Hotswap	The CP604-PM is compliant with the CompactPCI Hotswap Spec. PICMG 2.1 Version 1.0 The board may also be used in a standard CompactPCI system without Hotswap support
PMC Interface	PCI mezzanine connector for standard PMC module. 32-bit/33 MHz master interface 3.3V/5.0V compatible with rear I/O support via CompactPCI connector J5
General	Dimensions: 233.35 mm x 160 mm Operating temp.: 0°C to +60°C E1 (optional): -25°C to +75°C E2 (optional): -40°C to +85°C Storage temp.: -55°C to +85°C (without onboard hard disk) Operating humidity: 0% to 95% non-condensing at 40°C Weight: CP604-PM 4HP with heatsink: 442 grams
Front Panel Interfaces	PS-2 style connector for Keyboard/Mouse via Y-cable (6-pin mini-DIN) COM1: 9-pin D-sub (RS232, RS422, RS485) COM2: 9-pin D-sub (RS232, RS422, RS485) USB: one 4-pin connector two Ethernets: RJ-45 connectors with integral LED's VGA: 15-pin D-sub SVGA connector or 20-pin high density D-sub LVDS connector LED's: 5 different types of LED: ACT, SPEED: Ethernet status TH: Overtemperature status: red GP: General purpose: green HS/W: Hotswap removal indicator: blue Ethernet status LED's: ACT: network activity: yellow SPEED: network speed: green Reset button, guarded PMC breakout (opening) for PMC front panel

Table continued on following page

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Table 1-1: CP604-PM Main Specifications

CP604-PM	Specifications
Onboard Interfaces	Two EIDE interfaces supporting Ultra/DMA for 2 hard disks or CD-ROM on 40-pin 2.54mm connector and on a 44-pin 2.0 mm connector for mounting a 2.5 “ diskdrive onboard One floppy disk interface (up to 2.88 MB) Memory extension connection
Thermal Management / System Monitoring	Watchdog: software configurable watchdog generates an IRQ, NMI, or hardware reset Hardware monitor: LM81 monitoring temperature, fan speed and all onboard voltages (+ battery voltage) Temperature monitor: MAX 1617 monitoring the CPU on-die and board temperature
Common Features	DC power monitors (3.3V and 5V) Battery socket and 3.0V lithium battery for RTC: - VARTA Type CR2025 - PANASONIC BR2020
Software Support	Award BIOS within 256 kB of Flash memory and having the following features: - Award Preboot Agent included; this allows BIOS updates and service functions without VGA or a local disk - LAN-boot capability for diskless systems - Boot from USB floppy - Software enable/disable function for the rear I/O Ethernet and COM port configuration - Plug&Play capability - The BIOS parameters are saved in the EEPROM - Board serial number in EEPROM - Support for PEP RackNet (TCP/IP over the PCI backplane) - Operating systems supported: Linux®, QNX®, VxWorks®, Windows NT®4.0, Windows 2000 etc.

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1.6 Software Support

Real-time operating systems such as QNX®, VxWorks®, and others are supported. The standard PC features supported by the BIOS also allow for PC operating systems such as Linux®, MS-DOS®, Windows 9X®, Windows 2000®, Windows NT 4.0® Embedded.

1.6.1 Windows® 2000, Windows® NT Embedded

The Microsoft® platforms Windows® 2000/NT and Windows® NT Embedded are rapidly gaining popularity as the solution for embedded application requirements, such as medical systems, industrial automation and, in network devices, routers and switches.

In addition to being a modern, powerful 32-bit operating system platform, Windows provides a number of unique advantages not found in any other embedded operating system.

The familiar Windows Win32® API, with its associated broad range of development tools and knowledge base, provides a broad base of development talent, tools, and expertise.

Windows also offers comprehensive networking support and connectivity to non-embedded and enterprise information systems.

For systems with advanced operator interfaces, there is also the familiar Windows Graphical User Interface (GUI).

A major benefit of the Windows operating system in embedded applications is the ability to leverage existing off-the-shelf software components, either those in Windows itself or components from a wide range of third party developers.

Embedded system designers who create applications that maximize the use of existing components, and minimize the number of software components that must be written, will realize the lowest development costs and fastest time to market.

Any application, device driver, or service that runs on Windows® NT can be adapted to run on Windows® Embedded. Windows® Embedded is becoming the foundation of a growing number of embedded designs.

Any hardware that supports Windows® NT automatically supports Windows® NT Embedded. With Windows® NT Embedded, developers use off-the-shelf hardware and software to reduce their development costs and accelerate the time to market.

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Windows® NT Embedded includes the following embedded enabling features and tools:

- Flash memory support for diskless operation.
- Flexible page file support, including support for "No page file".
- Headless operation for systems without display, keyboard, and mouse.
- Remote management tools including a remote command shell and remote GUI desktop.
- Enhanced error support for auto-handling and logging of error dialogs.
- Target Designer - a GUI tool for selecting the Windows® NT Embedded components your system needs.
- Component Designer - a GUI tool for making your application, or any software your application may need, a Windows® NT Embedded component.

Using Target Designer, developers can configure Windows® NT Embedded as a stand-alone system requiring only 8 MB of persistent storage and 12 MB of RAM.

Windows® NT Embedded provides unprecedented benefits for embedded system developers, especially for those deploying applications with high software content and high performance requirements. By combining the capabilities of the Windows® NT operating system with design and operating system creation tools such as the Target Designer and Component Designer, Windows® NT Embedded is destined to become an outstanding solution in the embedded systems marketplace.

1.6.2 WindRiver: VxWorks® RTOS

Tornado was originally designed to solve the problems inherent in a cross-development environment, such as limited host-target communication, limited target resources and poorly integrated tools. With Tornado® II, WindRiver built upon the Tornado® framework, focusing developer time-to-productivity.

VxWorks,® the run-time component of the Tornado® II embedded development platform, is the most widely adopted real-time operating system (RTOS) in the embedded industry.

Tornado II also includes a comprehensive suite of core and optional cross-development tools and utilities and a full range of communications options for the target connection to the host.

The flexible VxWorks RTOS comprises the core capabilities of the WindRiver® microkernel along with advanced networking support, powerful file system and I/O management and C++ and other standard run-time support (more than 1800 powerful application program interfaces (HPIS)).

These core capabilities can be combined with add-on components available from Wind River Systems and PEP Modular Computers GmbH (e.g. VxWorks driver support for various PEP CompactPCI boards).

The VxWorks is designed for scalability, enabling developers to allocate scarce memory resources to their application, rather than to the operating system. From deeply embedded designs requiring a few kilobytes of memory, to complex high-end real-time systems where more operating system functions are needed, the developer may choose from over 100 different options to create hundreds of configurations. Individual modules may be used in development and omitted in production systems.

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Furthermore, these individual subsystems are themselves scalable, allowing the developer to optimally configure VxWorks run-time software for the widest range of applications. Additionally, TCP, UDP, sockets, and standard Berkeley network services can all be scaled in or out of the networking stack as necessary.

These configuration options may be easily selected by means of the Tornado II project facility´s graphical interface.

***PEP* Support**

PEP is one of the few CompactPCI and VME vendors providing inhouse support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software manufacturers, *PEP* is able to produce and support BSP's and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

Finally, customers possessing a maintenance agreement with *PEP* can be guaranteed hotline software support and are supplied with regular software updates. A dedicated web-site is also provided for online updates and release downloads.

1.6.3 QNX® RTOS

Consisting of a microkernel and a range of optional modules, QNX® employs an efficient division of labor to handle all OS services. When you need a file-system, a network, a GUI - whatever - simply run the modules you need.

Microkernel architecture, distributed processing for PCs, and built-in fault-tolerant networking are among the technologies QNX® pioneered. Using QNX® enables the customer to access the latest technologies such as CORBA, a WIN32API, an embeddable web browser, and more.

QNX® can be implemented in a real-time POSIX environment and full windowing system consuming less than 1 MB. The scalability of QNX® responds to the special needs of diverse applications from the lower end of the embedded market to a factory-wide control system, for example; automation or telecommunication.

Being more than just a true real-time operating system, QNX® is also physically small and suits ROMable embedded applications. It is powerful enough to run a distributed network comprising several hundred processors and is extremely fast. In fact, the QNX® microkernel handles process scheduling, inter-process communication, memory management, network communication and interrupt dispatching.

1.6.4 Other Operating Systems

Contact *PEP* for information on other operating systems.

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1.7 Environmental Considerations

1.7.1 Absolute Maximum Electrical Ratings

Absolute Maximum Ratings indicate limits beyond which damage to the board may occur. Do not operate the CP604-PM at or beyond these maximum values.

Table 1-2: Voltage Limits

Supply Voltage	Maximum Permitted Value
3.3V	+4.5V
5V	+5.5V
+12V	+14V
-12V	-14V

1.7.2 DC Operating Characteristics

Operating Ratings indicate the parameters within which the board is functional. The CP604-PM cannot be guaranteed to function if the board is not operated under the limits described.

Table 1-3: Voltage Range

Supply Voltage	Limit
3.3V	3.20V min. to 3.47V max.
5V	4.85V min. to 5.25V max.
+12V	11.4V min. to 12.6V max.
-12V	-11.4V min. to -12.6V max.

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1.7.3 Power Consumption

The CP604-PM board is based on the Intel® Mobile Pentium®III processor. Intel® has developed mobile processors to meet the specific needs of mobile PC's. As such, they operate at lower voltages than their desktop counterparts, are significantly smaller in size, consume less power and dissipate less heat. The design is optimized for low power consumption applications.

The goal of this description is to provide a method to calculate the power consumption for the CP604-PM base board and for additional configurations. The processor dissipates the majority of the thermal power.

The power consumption table lists the voltage and current specifications for the CP604-PM board and the CP604-PM accessories. The values were measured with an 8-slot passive CompactPCI backplane and two power supplies, one for the CPU and the other one for the hard disk. During measurement the power consumption of the backplane was ignored. The operating systems in use were DOS 6.22 without power management and Windows 2000 with power management. All measurements were conducted at a temperature of 25°C. The measured values varied, because power consumption was dependent on processor activity. All Mobile Pentium®III processors are powered with 1.35V core voltage (low power version)

Table 1-4: Power Consumption Table with DOS Running (without keyboard)

Power	400 MHz 256 MB (128 Mbit chips) with VGA	400 MHz 512 MB (128 Mbit chips) with VGA	500 MHz 512 MB (128 Mbit chips) with VGA	500 MHz 1 GB (256 Mbit chips) with VGA	700 MHz 512 MB (128 Mbit chips) with VGA	700 MHz 1 GB (256 Mbit chips) with VGA
Core Voltage	1.35 V	1.35 V	1.35 V	1.35 V	1.35 V	1.35 V
5 V	5.5 W	5.5 W	7.0 W	7.0 W	9.1 W	9.1 W
3.3 V	7.9 W	11.6 W	11.7 W	9.3 W	11.8 W	9.4 W
Total	13.4 W	17.1 W	18.7 W	16.3 W	20.9 W	18.5 W

Table 1-5: Power Consumption Table with Windows 2000 Running (no application started and without keyboard)

Power	400 MHz 256 MB (128 Mbit chips) with VGA	400 MHz 512 MB (128 Mbit chips) with VGA	500 MHz 512 MB (128 Mbit chips) with VGA	500 MHz 1 GB (256 Mbit chips) with VGA	700 MHz 512 MB (128 Mbit chips) with VGA	700 MHz 1 GB (256 Mbit chips) with VGA
Core Voltage	1.35 V	1.35 V	1.35 V	1.35 V	1.35 V	1.35 V
5 V	1.3 W	1.3 W	1.8 W	1.8 W	2.1 W	2.1 W
3.3 V	5.2 W	10.3 W	10.3 W	8.0 W	10.2 W	8.0 W
Total	6.5 W	11.6 W	12.1 W	9.8 W	12.3 W	10.1 W

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Table 1-6: Power Consumption Table for CP604-PM Accessories

Module	Power 5V	Power 3.3V
Keyboard	100 mW	--
DiskOnChip™ 16 MB	100 mW	--
DiskOnChip™ 144 MB	100 mW	--
Memory extension module: additional 512 MB or 1 GB	--	TBD



Note:

The 512 MB version is equipped with 128 Mbit SDRAM devices. The 1 GB version is equipped with 256 Mbit SDRAM devices. Power consumption for both versions is approximately the same.

1.7.4 Temperature Range

The CP604 family are amongst the first CompactPCI boards having the capability to operate over the extended temperature range from -40°C up to + 85°C. All onboard components are specially selected for the higher temperature range. For the higher temperatures the desktop processors are not suitable, because the power consumption is higher and the allowable case temperature is lower. The only suitable processor is the Intel® Mobile Pentium®III processor family. These processors are produced with the new 0.18-micron process which have lower power consumption and support higher case temperatures (100°C).

1.7.4.1 Temperature Range and Air Flow

These values have been measured with typical applications under DOS and Windows 2000. In worst case situations the values and the temperature range must be reduced accordingly. For all situations the maximum case temperature of the Mobile Pentium III processor must be below 100°C. This temperature value can be measured with the onboard remote temperature sensor. In instances of overtemperature the hardware monitor will reduce the processor clock to lower the generated power.

Table 1-7: Typical Temperature Range and Required Air Flow

Heat Sink Version	Range	400 MHz	500 MHz	700 MHz
4HP	0°C to 60°C	0 m/s	0 m/s	0.2 m/s
	-25°C to 75°C	0 m/s	0.4 m/s	1.0 m/s
	-40°C to 85°C	*0.4 m/s*	--	--

Important note relating to this table appears on the next page

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Warning!

The temperature ranges detailed above assume that any appended hard disk is capable of operating at these temperatures. The user must ensure that any appended hard disk can function at the operating temperatures expected.

0 m/s air flow means standard convection cooling with the board in an upright position. An airflow of 1 m/s is a typical value for a standard *PEP* ASM 4 rack (6U CompactPCI rack with 1U cooling fans). For other racks or housings the available airflow will be different. The maximum ambient temperature must be recalculated and / or measured for such environments. For the calculation of the maximum ambient temperature the processor case temperature must never exceed 100°C. The maximum heatsink temperature depends on the physical characteristics of the heatsink and thermal connection to the processor. To ensure that the heatsink temperature does not exceed its limits an airflow may be needed for a given ambient temperature. Heatsink temperature is measured at the top of the heatsink base, closest to the processor.

Warning!

- It is the responsibility of the end user to ensure that the processor case temperate never exceeds 100° Celsius in order to protect the board against overheating. Permanent overheating can damage the board.
- If the temperature on the processor die is greater than 100°C the maximum ambient temperature must be reduced or an external airflow must be provided by means of an additional fan.

1.7.5 Storage Temperatures

- Storage temperature without hard disk –55°C to +85°C
- Storage temperature with hard disk –40°C to +65°C
- Humidity non-condensing 0% to 95% at 40°C

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1.8 Applied Standards

1.8.1 CE Compliance

The *PEP Modular Computers'* CompactPCI systems comply with the requirements of the following CE-relevant standards:

- Emission — Residential, commercial and light industrial: EN50081-1
- Immunity — Industrial environment: EN50082-2
- Immunity — IT equipment: EN55024
- Electrical Safety — EN60950

1.8.2 Mechanical Compliance

- Mechanical Dimensions IEEE 1101.10
- The CP604-PM is compliant with CompactPCI Spec. V2.0 Rev 3.0.

1.8.3 Environmental Tests

Table 1-8: Qualification Parameters

Product Requirements	Applied Standard	Test Level (Ruggedised Version)
Single shock requirements	IEC-68-2-27	30g/9ms/18/5s peak acceleration / shock duration / number of shocks / recovery time in sec.
Continuous Shocks	IEC-68-2-29	15g/11ms/3000/1s peak acceleration / shock duration half sine / number of shocks / recovery time
Mechanical vibration requirements	IEC-68-2-6	2g/12-300Hz/10 acceleration / frequency range / test cycles
Vibration, broad band	IEC 68-2-64	20-500Hz,0.1g²/500-2000Hz,0.01g²/7g rms/3/30min frequency range1 / frequency range2 /acceleration / cycle / duration



Important:

The values in the above table are valid for boards which are ordered with the ruggedised service. For more information please contact your local *PEP* office.

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1.9 Related Publications

1.9.1 CompactPCI Systems/Boards

- CompactPCI Specification, V. 2.0, Rev. 3.0
- CompactPCI Hotswap Specification, PICMG 2.1 version 1.0 compliant

1.10 Trademarks

CompactPCI is a trademark of the PCI industrial Computers manufacturers group.

Ethernet is a registered trademark of Xerox corporation.

IEEE is a registered trademark of the Institute of Electrical and Electronics Engineers Inc.

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Functional Description and Configuration

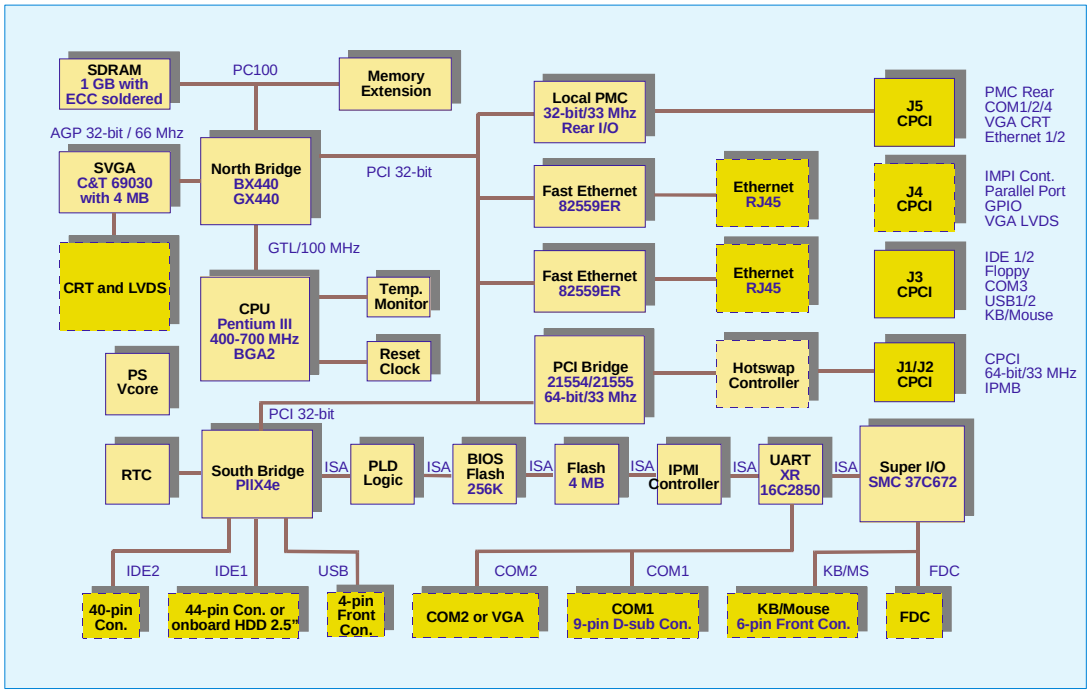
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2. Functional Description and Configuration

2.1 Functional Block Diagram

Figure 2-1: CP604-PM Functional Block Diagram



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2.2 Front Panels

Figure 2-2: CP604-PM Front Panels

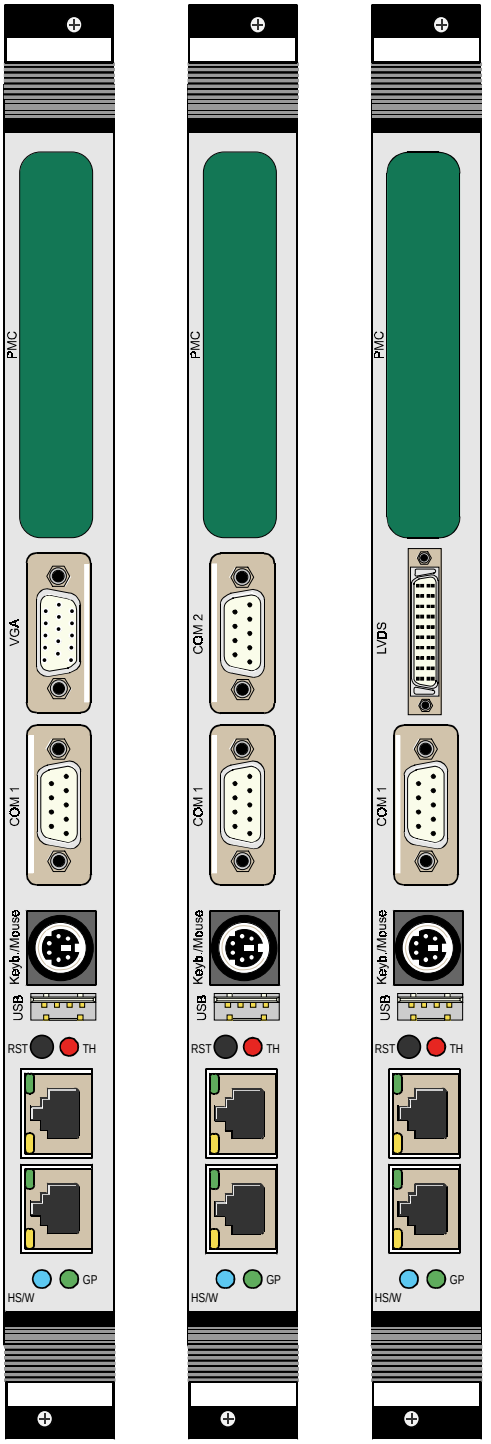
The front panel includes three LED's, one placed under the USB interface connector and two beneath the Ethernet connectors ("Board LED's"). In addition, each Ethernet has two integral LED's, one green and one yellow ("Ethernet LED's"). The functions of the LED's are as follows:

Board LED:

- TH (red) = Temperature alarm; if ON, an overtemperature has occurred. The CPU clock speed is reduced automatically.
- GP (green) = general purpose LED
- HS/W (blue) = hotswap LED; this will light to signal that the board may be removed

Ethernet LED's:

- ACT (yellow) = if ON link is active and transmission is in progress via the Ethernet link.
- SPEED (green) = if ON transmission speed is 100 MBit/s.

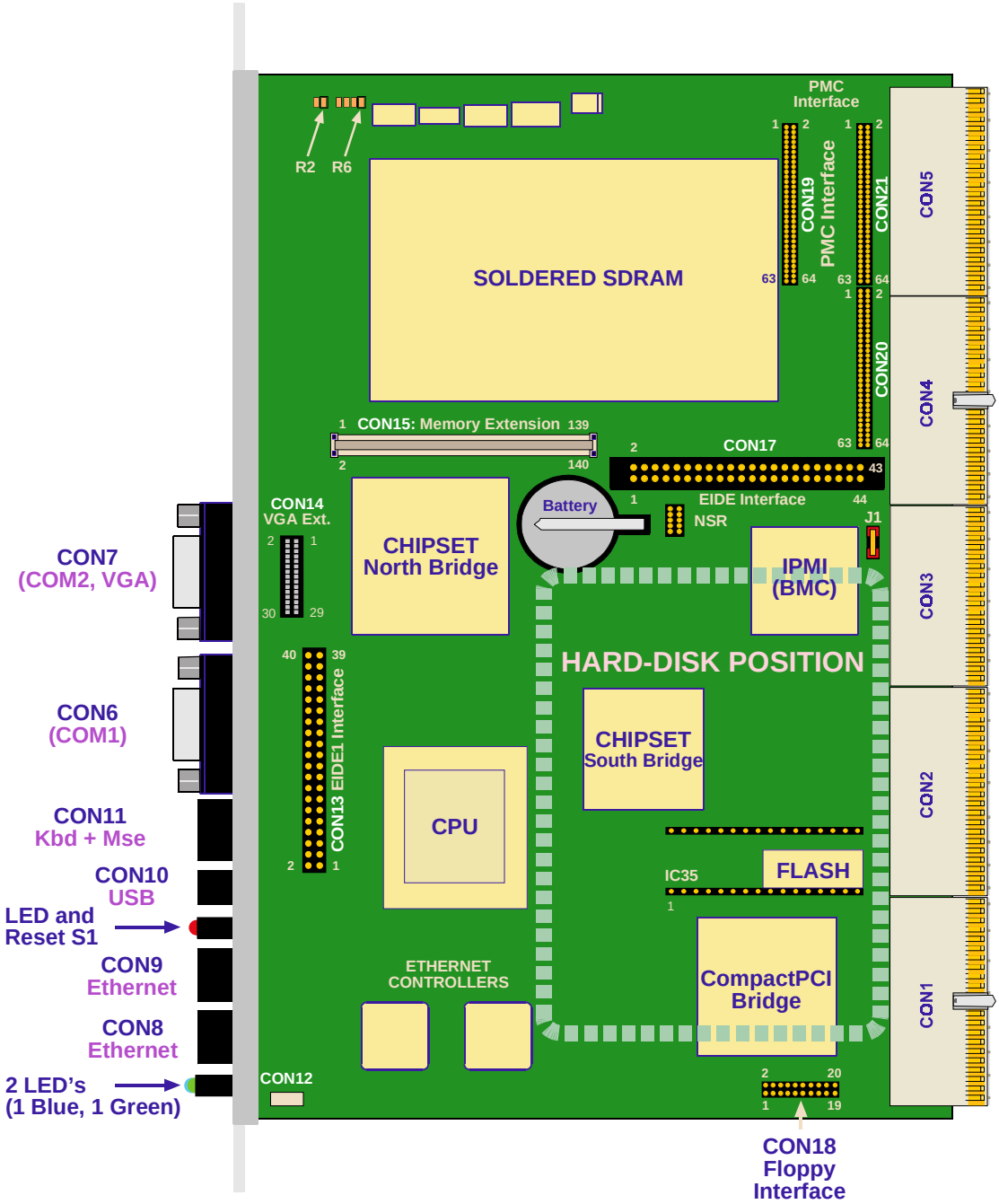


Version with VGA-CRT **Version with 2nd COM port** **Version with VGA LVDS**

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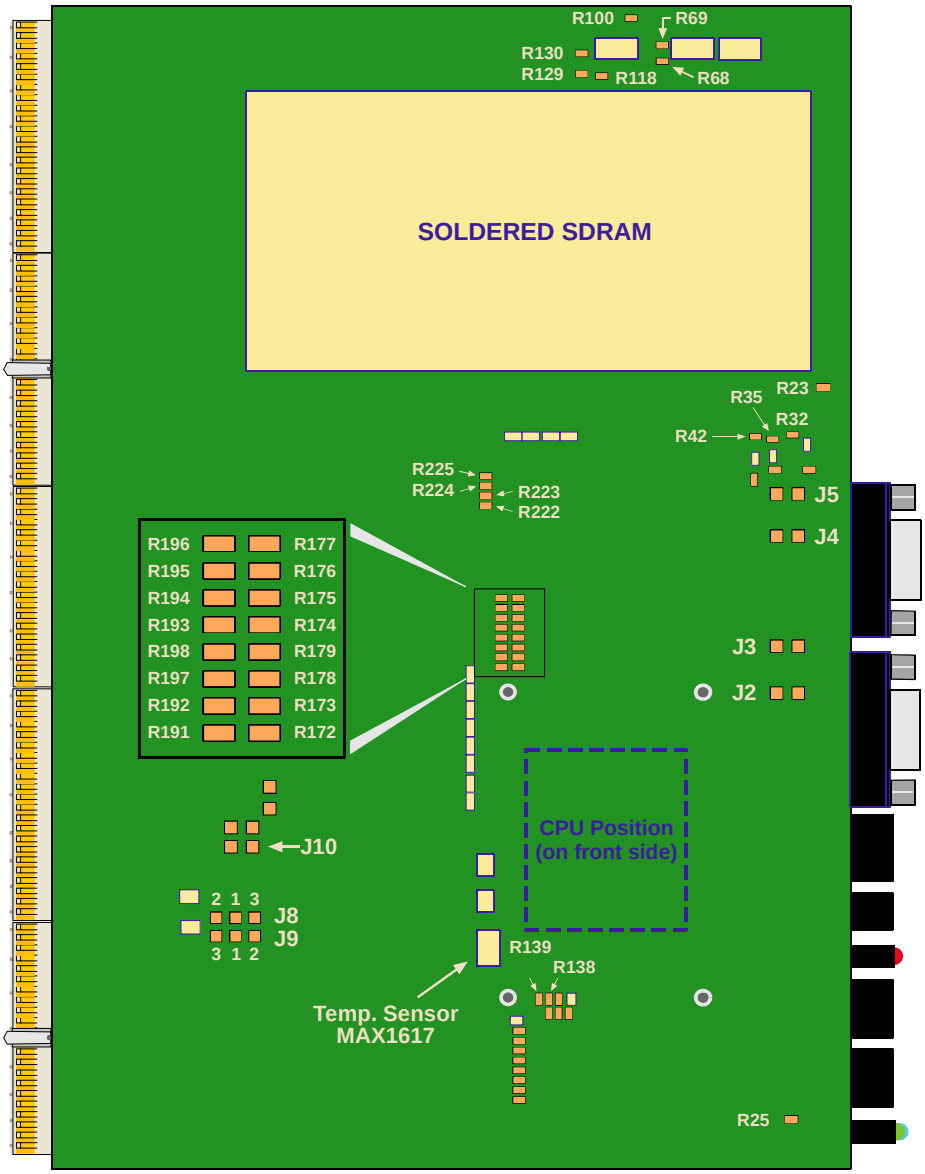
2.3 Board Layouts

Figure 2-3: CP604-PM Board Layout (Front Side)



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Figure 2-4: CP604-PM Board Layout (Reverse Side)



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2.4 CPU and Chipset

2.4.1 CPU

The CP604-PM supports the Intel® Mobile Pentium®III Coppermine™ processor family up to 700 MHz with 256 kB L2 on-die cache in a 495-pin BGA2 package. The processor speed is automatically selected. The onboard voltage regulator is automatically programmed by the processor's VID pins to provide the required voltage. All supported onboard memory can be cached.

The CP604-PM is available with a variety of Intel® processors as set out in the following table:

Table 2-1: Supported Intel® Processors on the CP604-PM

Processor	Speed	L2 Cache	Core Voltage	Front Side Bus
Pentium® III Mobile	400 MHz	256 kB	1.35 core voltage	100 MHz
Pentium® III Mobile	500 MHz	256 kB	1.35 core voltage	100 MHz
Pentium® III Mobile	700 MHz	256 kB	1.35 core voltage	100 MHz
Celeron® Mobile	400 MHz	128 kB	1.35 core voltage	100 MHz
Plus future Intel® Pentium® III processors with 100 MHz front side bus				

2.4.2 Memory

The CP604-PM has two locations for installing memory; up to 1 GB may be soldered with ECC support and a further 1 GB with ECC support may be attatched as via a memory extension module. The board supports a maximum of 1 GB memory with the BX chipset and a maximum of 2 GB with the GX chipset. All installed memory will be automatically detected, so there is no need to set any jumpers.

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2.4.3 Chipset

The CP604-PM design is based on the advanced Intel® 440BX and 440GX AGP Chipset. The main difference between the BX and the GX chipsets are in the degree of memory support.

82443 AGP Host Bridge Controller (North Bridge)

- Optimized for all Intel® Pentium® III and Intel® Pentium® III Mobile processors
- Meets all PC98 requirements
- AGP graphics port
- Supports up to 2 GB SDRAM with GX (1 GB SDRAM with BX)
- External system bus up to 100 MHz
- PCI Rev. 2.1 3.3V and 5.0V interface compliant
- Supports up to 5 onboard PCI bus masters
- Integrated power management functions

82371 PIIX4E PCI-to-ISA/IDE Xcelerator (South Bridge)

- Multifunction PCI to ISA bridge
- Enhanced DMA controller
- Interrupt controller based on two 82C59's
- Timer based on 82C84
- Real-time clock
- SMBus interface
- Power management logic
- Supports two USB interfaces
- Supports two EIDE interfaces
- Integrated power management functions

2.4.4 Interrupts

Two enhanced 8259-style interrupt controllers provide a total of fifteen interrupt inputs with features which include level and edge-triggered inputs, fixed and rotating priorities and individual input masking. Interrupt sources include: Counter/timers, serial I/O, RTC, keyboard/mouse, printer, floppy disk, EIDE interfaces and four interrupt sources on the CompactPCI backplane.

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2.5 Peripherals

The following standard peripherals are available on the CP604-PM board:

- *Real-Time Clock*

  The real-time clock performs time-keeping functions and includes 256 bytes of general purpose battery-backed CMOS RAM. Features include an alarm function, programmable periodic interrupt and a 100-year calendar. All battery-backed CMOS RAM data remains stored in an additional EEPROM. This prevents data loss.

- *Counter/Timer*

  Three 8254-style counter/timers are included on the CP604-PM as defined for the PC/AT.

2.5.1 Watchdog Timer

A watchdog timer is provided, which forces either an IRQ5, NMI, or Reset condition (configurable in the watchdog register). The watchdog time can be programmed in 12 steps ranging from 125 msec up to 256 seconds. If the watchdog timer is enabled, it cannot be stopped.

2.5.2 Battery

The CP604-PM is provided with a 3.0V “coin cell” lithium battery for the RTC.

To replace the battery please proceed as follows:

- Turn off power
- Remove the battery
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. Suitable batteries include the VARTA CR2025 and PANASONIC BR2020

Important notes concerning the battery appear on the next page

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Important:

- Care must be taken to ensure that the battery is correctly replaced.
- The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instructions.
- The typical life expectancy of a 170 mAh battery (VARTA CR2025) is 4 - 5 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.
  To ensure that the lifetime of the battery has not been exceeded it is recommended to exchange the battery after 3 - 4 years.

2.5.3 Reset

The CP604-PM is automatically reset by a precision voltage monitoring circuit that detects a drop in voltage below the acceptable operating limit of 4.725 V for the 5V line and below 3.0V for the 3.3V line, or in the event of a power failure of the DC/DC converter. Other reset sources include the watchdog timer, the drawbridge reset and the local push-button switch. The CP604-PM responds to any of these sources by initializing local peripherals.

The CP604-PM has a variety of reset options:

- Front panel push button
- Watchdog
- Drawbridge reset (from 21554/21555)
- Power control (5V, 3.3V and CPU core voltage)

2.5.4 SMBus Devices

The CP604-PM provides a System Management Bus (SMBus) for access to several system monitoring and configuration functions. The SMBus consists of a two-wire I2C bus interface. The following table describes the function and address of every onboard SMBus device.

Table 2-2: SMBus Device Addresses

Device	SMB Address
PIIX4 slave port	0001000Xb
Temperature sensor MAX1617	0011000Xb
Hardware Monitor LM81	0101100Xb
EEPROM	1010XXXXb

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2.5.5 Thermal Management / System Monitoring

The LM81 can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds and temperatures; all of which are very important for the proper operation and stability of a high-end computer system. The LM81 provides an I2C™ serial bus interface.

The voltages of the onboard power supply +12V, -12V, +5V, +3.3V, +1.5V and the battery voltage are supervised. Two fan tachometer outputs can be measured using the LM81's FAN1 and FAN2 inputs. The DAC output of the LM81 can be used for controlling fan speed. The presence of the fans is automatically detected. All three signals, FAN1 and FAN2 input and the DAC output for fan speed control are connected to the CompactPCI rear I/O interface J5.

The integrated MAX1617 temperature sensors monitor the CPU temperature and the ambient temperature around the CPU to make sure that the system is operating at a safe temperature level. If the temperature is too high, the sensors automatically reduces the CPU clock frequency, depending on the mode chosen in the BIOS set. Thermal management operations are controlled by the PIIX4E chipset and settings are available in the BIOS.

2.5.6 Serial EEPROM

A serial EEPROM is provided, organised into 4 blocks with 256 bytes per block (24LC08). This EEPROM is connected to the I2C™ bus provided by the PIIX4E.

Table 2-3: EEPROM Address Map

Address	Function
1010000xb	Reserved
1010001xb	Reserved
1010010xb	Reserved
1010011xb	Reserved
1010100xb	VxWorks parameter
1010101xb	Free for user purposes
1010110xb	Free for user purposes
1010111xb	CMOS backup and Board serial number

It is strongly recommended that users access only the two free EEPROM banks

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2.5.7 Flash Memory

There are three Flash devices available as described below, one for the BIOS, one 32-pin socket for a flexible Flash configuration and one onboard Flash.

1. BIOS Flash

The CP604-PM uses a 256 kB flash memory to store BIOS firmware. It can be updated as new versions of the BIOS become available. You may easily upgrade your BIOS using the AWARD *awdflash* utility .

2. Socket Memory

Different flash module versions are available. In order to achieve flexibility with low cost the flash memory is not soldered, but connected via a special module from M-Systems (DiskOnChip™ 2000).

- Standard flash memory of up to 512 KB in a 32-pin DIL package
  - AMD29F010
  - AMD29F040
- Standard EEPROM memory in a 32-pin DIL package
  - AMD27C010
  - AMD27C020
- DiskOnChip™ flash memory:
  - 8 - 288 MB

For higher flash memory capacity it is recommended to use the onboard 2.5” flash disk.

3. Onboard 4 MB Flash Memory

For small flash extensions the 4 MB onboard flash memory can be used. The 32 Mbit Flash device (4 MB with unique 64 kB sectors) is located in a TSOP package.

The flash memory may only be viewed in 256 pages with a size of 16 kB. The active page can be selected via a register.

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2.5.8 Non-transparent PCI-to-PCI Bridge

The CP604-PM is a peripheral controller based on the 21554/21555 bridge from Intel®. This “non-transparent” PCI-to-PCI bridge makes it possible to isolate two PCI bus segments. The 21554/21555 PCI-to-PCI bridge is fully compliant with the PCI Local Bus Specification Rev. 2.1.

The 21554/21555 is specifically designed to bridge between two processor domains. The processor domain on the primary interface of the 21554/21555 is referred to as the host domain, this interface resides to the CompactPCI connector. The secondary bus interfaces referred to as the local domain and resides to all onboard PCI devices of the CP604-PM.

The 21554/21555 bridge maps the entire CP604-PM subsystem as a single virtual device. The 21554/21555 PCI-to-PCI bridge is designed to allow configuration and addressing isolation, so that the local processor can effectively control the subsystem.

Key features of the Intel® 21554/21555 bridge:

- optimized for multiprocessor application
- supports asynchronous PCI clock (primary and secondary interface)
- address translation between the two domains (host and slave)
- full 64-bit 33 MHz PCI interface
- I2O support
- Hotswap status and control register



Note:

The CP604-PM has been designed for use in a peripheral slot only; it is not intended for use in the system slot.

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2.6 Hotswap

2.6.1 Technical Background of CompactPCI Hotswap

In many modern application systems downtime is costly and/or unacceptable. Server applications, telecommunications networks and automated systems requiring continuous monitoring call for a system design in which a single card can be inserted or extracted without affecting the rest of the system. The ease with which a board may be removed and replaced is dependent on the mechanical design (form factor), the possibility of deactivating the software drivers for the board (operating system) and the possibilty of removing and inserting the board without disturbing the signal quality on the bus.

CompactPCI hotswap is currently the most effective way to meet this need. Staggered pins on the backplane guarantee controlled power sequencing of the board, while the signals ENUM, BDSEL, HEALTHY and the hotswap control and status register bits may be used to control board access from the software side.

2.6.2 Hotswap System

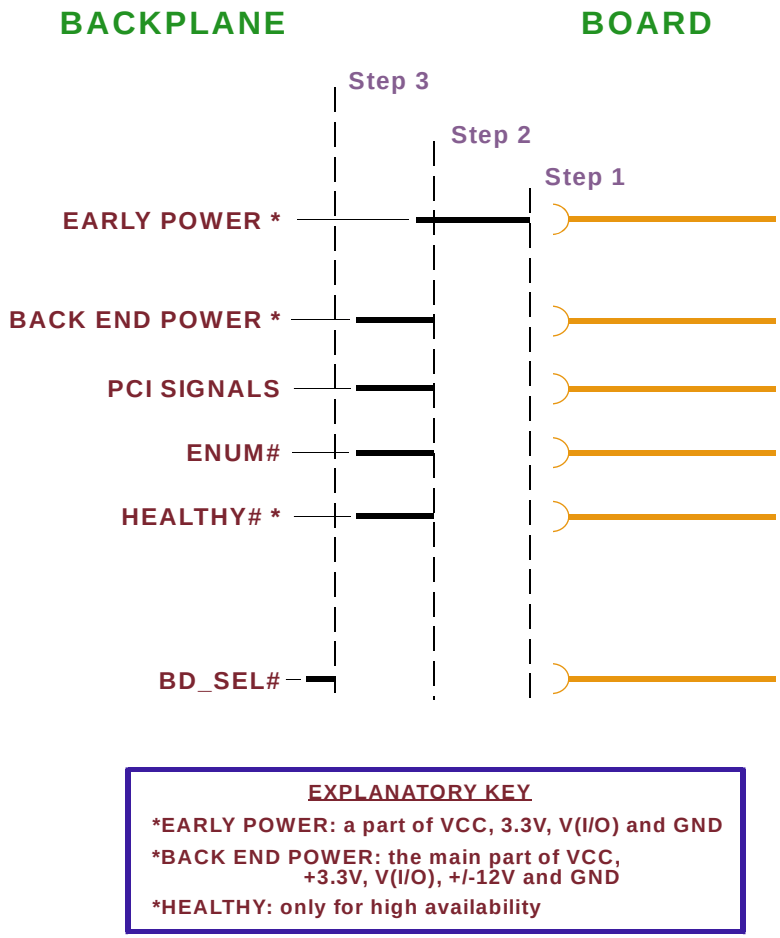
A hotswap system consists of a hotswap platform which comprises a hotswap backplane, the system host (CPU) with hotswap features, cooling, power supplies etc. plus the boards to be hotswapped. Hotswapping is not possible unless the operating system has the capability to enable and disable the board specific driver during normal operation.

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2.6.2.1 The Hotswap Backplane

The hotswap backplane has staggered pins to ensure defined power sequencing.

Figure 2-5: Illustration of Staggered Pinning on the Hotswap Backplane



Note:

Some special signals (e.g. ENUM, HEALTHY, BDSEL...) have particular routing requirements.

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2.6.2.2 The System Host (System Controller)

The System Controller must have the possibility to utilize the special signals defined by the CompactPCI hotswap specification. If a high availability system is used it must additionally be able to control the hardware connection with the peripheral boards (Hardware Connection Control).

2.6.2.3 The Hotswap Board

To ensure that a board may be removed and replaced in a working bus without disturbing the system it requires the following additional features.

- precharge
- power ramping
- hotswap control and status register bits
- automatic interrupt generation whenever a board is about to be removed or replaced.
- an LED to indicate that the board may be safely removed.

2.6.3 Design Implementation on CP604-PM

2.6.3.1 Power Ramping

On the CP604-PM, a special hotswap controller is used to ramp up the onboard supply voltage . This is done to avoid transients on the 3.3V, 5V, +12V and -12V power supplies from the Hotswap system. When the power supply is stable, the hotswap controller generates a reset on the PMC slots to put the devices into a definite state.

2.6.3.2 Precharge

Precharge is provided on the CP604-PM by a resistor on each signal line (PCI bus), connected to a 1V reference voltage.

2.6.3.3 Handle Switch

A microswitch is situated in the extractor handle. Opening the handle initiates the generation of the ENUM interrupt (produced by the onboard logic). The microswitch is routed to CON12 on the board.

2.6.3.4 ENUM# Interrupt

The onboard logic generates a low active interrupt signal to indicate that the board is about to be extracted from the system or inserted into the system.

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2.7 Intelligent Platform Management Interface (IPMI)

2.7.1 Technical Background of IPMI

The CP604-PM has been configured to support the "Intelligent Platform Management Interface" (IPMI) subsystem which is another step in providing high availability platforms. Intelligent Platform Management means monitoring the health of the entire system beyond the confines of the board itself, so that the status of the complete system is available to be used, for example, for control and intervention purposes. A range of variables is monitored on every board, to provide information on the system status, e.g. voltages, temperature, powergood signals, reset signals etc. Additionally, the IPMI Baseboard controller can intervene, regulating the operating status of the system by controlling fans, shutting down systems and generating alarm signals as and when fault conditions occur. These fault conditions are simultaneously logged in non-volatile memory for analysis and for fault recovery. IPMI also defines a protocol (software stack) for exchanging the status messages of the board, so that "IPMI ready" boards/systems from different suppliers can be monitored. In addition, a clear interface (registers, addresses etc.) is defined for guaranteeing that System-Management software can work with every compliant IPMI hardware.

The electrical interconnection between IPMI capable boards is an I2C interface (IPMB). On CompactPCI systems, this interface is provided on IPMI-prepared backplanes and guarantees the data path between the boards.

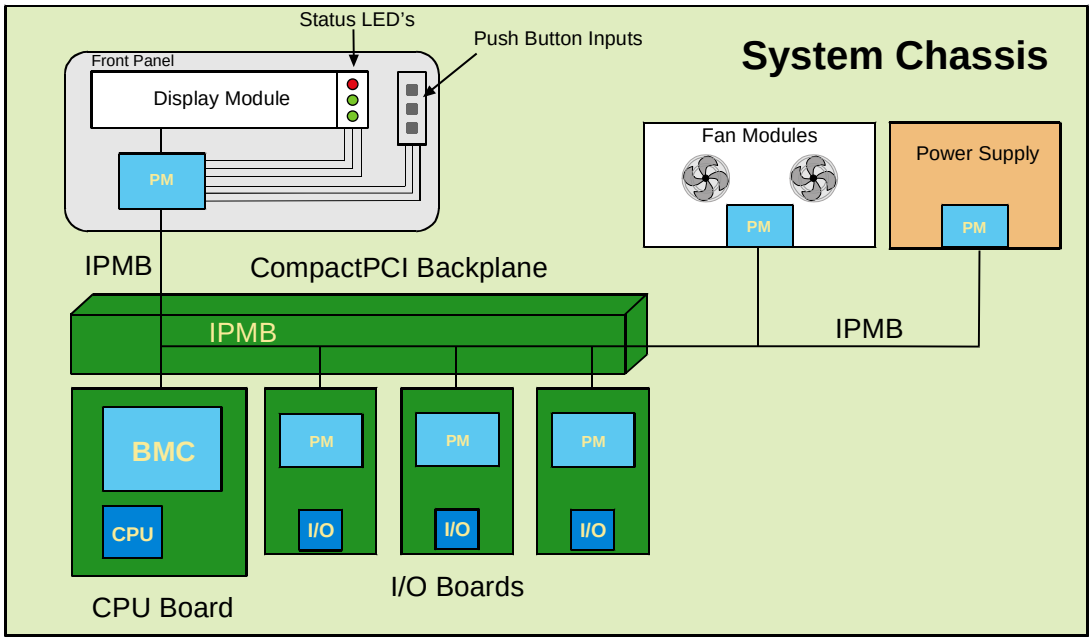
The devices which handle the measurements and the protocol stack are microcontrollers which are named Baseboard-Management-Controller (BMC) and Peripheral-Management-Controller (PM) depending on their position in a CompactPCI backplane. The IPMI microcontroller which is on the System Master board in a CompactPCI system is called BMC and the IPMI controller which is on a Peripheral board is named PM.

The interface between the system controller CPU’s System Management software and the BaseBoard Management Controller can be realized in two different ways, a keyboard controller style interface (KCS) or a block transfer interface (BT) which can be found in the system master’s IO-space.

A Functional Block Diagram for the IPMI appears on the next page

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Figure 2-6: IPMI Functional Block Diagram



2.7.2 IPMI Implementation on the CP604-PM

On the CP604-PM, the IPMI functionality is realized using the ZIRCON-Lite controller from QLogic, which is an ARM7TDMI core-based IPMI controller. Due to the fact that this controller can act as BMC and as PM on all versions of the CP604, the same controller can be used. All the information collected by the ZIRCON-Lite is then accessible by software through a keyboard-style Interface (see IPMI-Intelligent Platform Management Interface Specification V.1.0 for more information) whose address space is available in the IO space of the Intel CPU's address map, or via the IPMB-Bus.

2.7.3 Measurement of Onboard Voltages

On the CP604-PM all voltages are monitored by the ZIRCON-Lite. This means 5V, 3.3V, 2.5V, VCORE, VTT, VIO, 12V and -12V.

2.7.4 Measurement of Temperatures

An onboard sensor measures the temperature in the vicinity of the CPU (positioned below the heatsink).

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2.7.5 Fan Control

Four Tacho inputs and two PWM outputs are routed to the rear I/O connector. These make it possible to control the Fan speed to regulate the CPU cooling.

2.7.6 Data Repositories

All the data gathered by the ZIRCON is stored in a non-volatile memory, providing the possibility to obtain information about working conditions and failure situations.

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2.8 Board Interfaces

2.8.1 Keyboard/Mouse Interface

The onboard keyboard controller is 8042 software compatible.

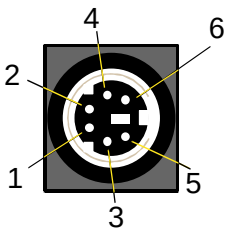
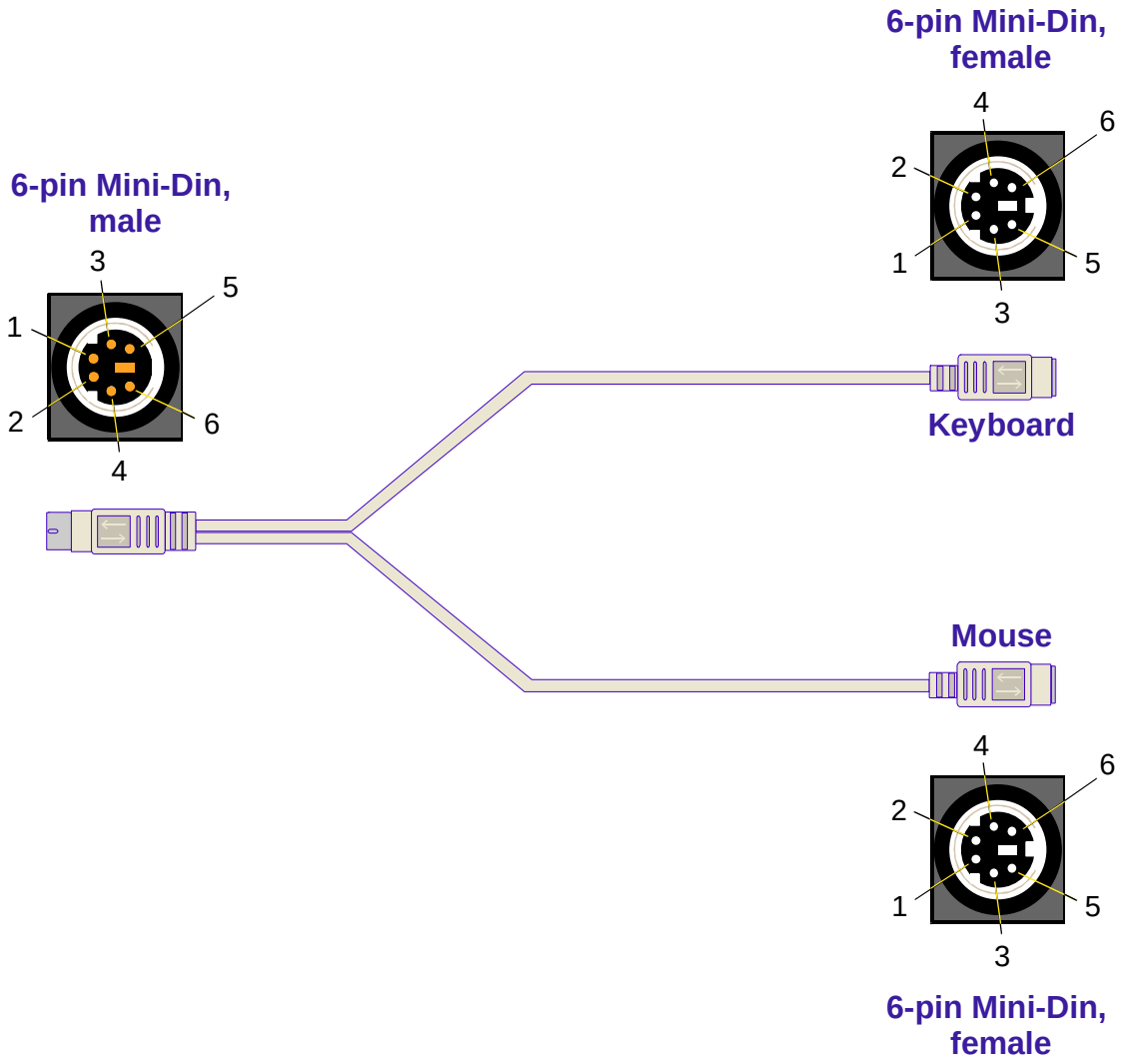


Figure 2-7: Keyboard/Mouse Connector

The PC/AT standard keyboard/mouse connector is a PS/2-type 6-pin shielded mini-DIN connector. The keyboard power supply unit is protected by a 500 mA fuse. All signal lines are EMI-filtered.

A special adapter to connect a mouse device and/or a keyboard to the PS/2 connector is available from *PEP*. This adapter is illustrated below.

Figure 2-8: Adapter for Connecting Mouse/Keyboard via PS/2



Keyboard connector CON11 pinout follows on next page

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2.8.1.1 Keyboard Connector CON11 Pinout

The CP604-PM has the AT keyboard connector implemented on a 6-pin Mini-Din connector with the following pinout.

Table 2-4: Keyboard Connector CON11 Pinout

Pin	Name	Function	In/Out
1	KDATA	Keyboard data	In/Out
2	MDATA	Mouse data	In/Out
3	GND	Ground signal	--
4	VCC	VCC signal	--
5	KCLK	Keyboard clock	Out
6	MCLK	Mouse clock	Out



Note:

The keyboard power supply is protected with a fuse (500mA) and all the signal lines are EMI-filtered.

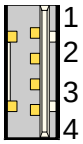
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2.8.2 USB Interface

The Universal Serial Bus, or USB, is a versatile port. This one port type can function as a serial, parallel, mouse, keyboard, or joystick port and is capable of supporting up to 127 daisy-chained peripheral devices.

Figure 2-9: USB Connector

One USB interface with a maximum transfer rate of 12 Mbit is provided. One USB peripheral may be connected to this port. To connect one or more USB devices an external hub is required.



2.8.2.1 USB Connector CON10 Pinout

The CP604-PM has one USB interface implemented on a 4-pin connector.

Table 2-5: USB Connector CON10 Pinout

Pin	Name	Function	In/Out
1	VCC	VCC signal	--
2	UV0-	Differential USB-	--
3	UV0+	Differential USB+	--
4	GND	GND signal	--



Note:

The USB power supply feeding the USB connector is protected with a fuse (1500 mA) and all the signal lines are EMI-filtered.

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2.8.3 Graphics Controller

The CP604-PM board is equipped with the integrated Chips&Technologies 69030 VGA chip with 4 MB SDRAM memory. This chip contains a UVGA controller which is fully compatible with the CGA, EGA, Hercules Graphics, MDA, VGA, SVGA, XGA and SXGA video standards. The controller connects directly to the onboard 66 MHz AGP Interface with a maximum data transfer rate of 266 MB per second. The video controller supports dual display mode with simultaneous FlatPanel and CRT operation capability and provides pixel resolutions of up to 1600 x 1200 or up to 16.7 million colors. In addition to the standard CRT interface, the UVGA controller supports digital FlatPanels with a maximum vertical retrace non-interlaced frequency of 60 Hz. The refresh rates can be independently programmed for both ports (CRT and FlatPanel).

2.8.3.1 CRT Interface and Connector CON7

(Version with VGA-CRT Interface)

Figure 2-10: D-sub CRT Connector

The 15-pin female connector CON7 is used to connect a CRT monitor to the CP604-PM board.

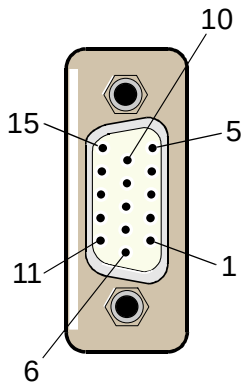


Table 2-6: CRT Connector CON7 Pinout

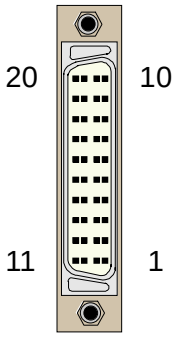
D-sub 15	Signal	Function	In/Out
1	Red	Red video signal output	Out
2	Green	Green video signal output	Out
3	Blue	Blue video signal output	Out
13	Hsync	Horizontal sync.	TTL out
14	Vsync	Vertical sync.	TTL out
12	Sdata	I2C™ data	In/Out
15	Sclk	I2C™ clock	Out
9	VCC	Power +5V 200 mA no fuse protection	Out
5,6,7,8,10	GND	Signal ground	--
4,11	Free	--	--

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2.8.3.2 LVDS Flatpanel Interface and Connector CON7 Pinout

(Version with VGA-LVDS Interface)

Figure 2-11: Deltaribbon LVDS Connector CON7



For connecting LVDS TFT displays, the CP604-PM is equipped with a 6-bit per color FPD-Link LVDS transmitter from National Semiconductor (DS90C363A). The programmable version of this device is used to provide the ability to switch between falling edge and rising edge triggering (default is falling edge). The pixel clock of this device has a range between between 20 and 65 MHz.

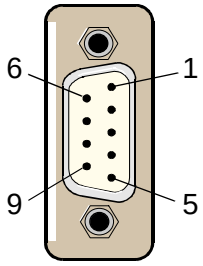
Table 2-7: LVDS Connector CON7 Pinout

Pin Number	Signal	Description
1	TXOUT1+	LVDS signal
2	TXOUT1-	LVDS signal
3	Shield	Ground
4	Shield	Ground
5	TXCLK_OUT+	LVDS clock signal
6	TXCLK_OUT-	LVDS clock signal
7	GND	Ground
8	+5V	Power: max. 200 mA
9	RXD	Serial Receive
10	TXD	Serial Transmit
11	TXOUT2+	LVDS signal
12	TXOUT2-	LVDS signal
13	Shield	Ground
14	Shield	Ground
15	TXOUT0+	LVDS signal
16	TXOUT0+	LVDS signal
17	+12V	Power: max. 200 mA
18	FPVEE	Backlight Control
19	DDAT	I2C™ data
20	DCCK	I2C™ clock

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2.8.4 Serial Port Interfaces COM1 and COM2

Figure 2-12: PC-compatible D-Sub Serial Connector)



Two PC-compatible serial 9-pin D-sub ports are available with 5V charge-pump technology eliminating the need for a +12V and -12V supply. The two COM ports, which are fully compatible with the 16550 controller, include a complete set of handshaking and modem control signals, maskable interrupt generation and data transfer of up to 460.8 kB/s.

Serial Ports COM1 and COM2 can be enabled/disabled under SW control. Selection can be made inside the BIOS or via the rear I/O configuration register. The standard software configuration is front I/O.

The two COM interfaces may be configured as RS232, RS422 or RS485 ports by setting the appropriate solder jumpers. The standard setting of the two COM ports envisages the RS232 configuration.

RS-422 configuration:

The RS-422 interface use two differential data lines RX and TX for communication (Full-Duplex)

RS-485 configuration:

The RS-485 interface use one differential data line. It differs from the RS-422 modes in that it provides the ability to transmit and receive over the same wire. The RTS signal is used to enable the RS-485 transmitter.

The Serial Port connector pinouts appear on the next page

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2.8.4.1 Serial Port Connectors CON6 (COM1) and CON7 (COM2) Pinout

The pinout of the 9-pin D-sub connectors depends on the configuration.

Table 2-8: Serial Port Connectors CON6 (COM1) and CON7 (COM2) Pinout

Pin	RS232 (Standard PC)	RS422	RS485
1	DCD	+RXD	NC
2	RXD	NC	NC
3	TXD	+TXD	+TRXD
4	DTR	NC	NC
5	GND	GND	GND
6	DSR	-RXD	NC
7	RTS	NC	NC
8	CTS	-TXD	-TRXD
9	RIN	NC	NC

2.8.5 Serial Port Interfaces COM3 and COM4

Additionally, two PC-compatible serial ports with the TTL signal level are available. The two COM ports, which are fully compatible with the 16550 controller, include a complete set of handshaking and modem control signals, maskable interrupt generation and data transfer. **The COM3 and COM4 ports are only available on the CompactPCI rear I/O interface**.

2.8.6 Parallel Port Interface

The CP604-PM is provided with an IEEE1284, ECP/EPP-compatible parallel port/printer interface. **The parallel port is only available on the CompactPCI rear I/O interface**.

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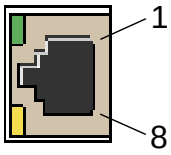
2.8.7 Fast Ethernet

The CP604-PM board includes two 10BASE-T/100BASE-TX ethernet ports based on the Intel® 82559ER Fast Ethernet PCI Bus Controller. The controller contains two receive and transmit FIFO buffers that prevent data overruns or underruns while waiting for access to the PCI bus.

Two LED's monitor network conditions. The Boot from LAN feature is supported, for details please refer to section 4.5, BIOS Features Setup, in chapter 4.

Figure 2-13: Ethernet/Fast Ethernet Connector

The Ethernet connectors are realized as RJ45 twisted-pair connectors. The interfaces provides automatic detection and switching between 10Base-T and 100Base-TX data transmission. The two Ethernet channels may be configured via the BIOS setting or the rear I/O Configuration Register for front I/O or rear I/O. The standard software configuration is front I/O.



2.8.7.1 RJ45 Connectors CON8 and CON9 Pinouts

The CON8 and CON9 connectors supply the 10Base-TX/100Base-TX interfaces to the Ethernet controller.

Table 2-9: RJ45 Connectors CON8 and CON9 Pinouts

RJ45	Signal	Function
1	TX+	Transmit +
2	TX-	Transmit -
3	RX+	Receive +
4	NC	--
5	NC	--
6	RX-	Receive -
7	NC	--
8	NC	--

2.8.8 Ethernet LED Status

Yellow: ACT: This LED monitors network connection and activity. The LED lights up when network packets are sent or received through the RJ45 port. When this LED is not lit it means that either the computer is not sending or receiving network data or that the cable connection is faulty.

Green: SPEED: This LED lights up to indicate a successful 100Base-TX connection. When not lit the connection is operating at 10Base-T.

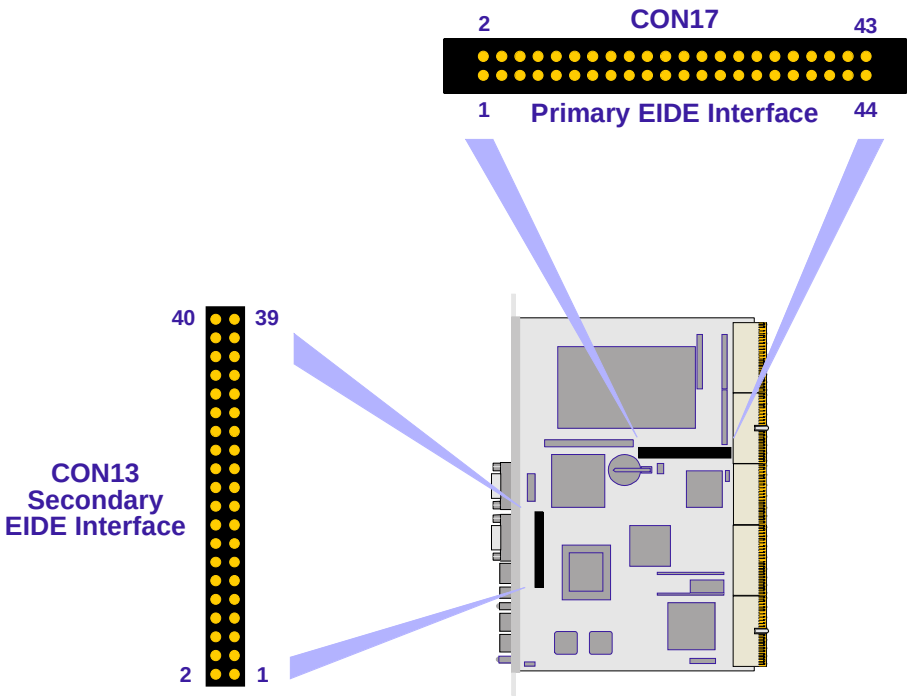
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2.8.9 EIDE Interfaces

The two EIDE interfaces support PIO mode 4 with transfers up to 14 MB per second and Bus Master Ultra-DMA 33 transfer up to 33 MB per second. The EIDE controller can sustain a maximum transfer rate of 33 MB per second between the EIDE drive buffer and PCI.

There are two independent EIDE ports available. The primary EIDE interface is a 44-pin, 2-row male connector AT standard interface for an EIDE hard disk. This connector provides support for one hard disk and/or CD-ROM drive and also provides the power supply (5V/1A) for Notebook 2.5” HDD drives. A 2.5” hard disk or flash disk can be mounted directly on the CP604-PM. The secondary EIDE interface is a 40-pin, 2-row male connector AT standard interface for an EIDE hard disk.

Figure 2-14: CON13 and CON17 Connectors: EIDE Interfaces



Each EIDE interface provides support for two devices (one master and one slave). All hard disks can be used in cylinder head sector (CHS) mode with the BIOS also supporting the logical block addressing (LBA) mode..



Important:

Each EIDE interface supports a maximum of two devices connected in the master-slave mode. To configure the first as a master disk and the second as a slave disk, please refer to the hard disk manufacturer’s documentation.

EIDE connector pinouts appear on the following pages

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2.8.9.1 CON17 (Primary EIDE Interface) Pinout

The pin numbering uses the normal signals as used by 2.5” Notebook hard disk drives. The following table sets out the pinout of the CON17 connector, giving the corresponding signal names. The maximum length of cable that may be used is 35 cm.

Table 2-10: CON17 (Primary EIDE) Pinout

Pin Number	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C	--	--
33	A1	Address 1	Out
34	N/C	--	--
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	N/C	--	--
40	GND	Ground signal	--
41	VCC	+5V power	--
42	VCC	+5V power	--
43	GND	Ground signal	--
44	VCC	+5V power	--

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2.8.9.2 CON13 (Secondary EIDE Interface) Pinout

The following table sets out the pinout of the CON13 connector, giving the corresponding signal names. The maximum length of cable that may be used is 35 cm.

Table 2-11: CON13 (Secondary EIDE) Pinout

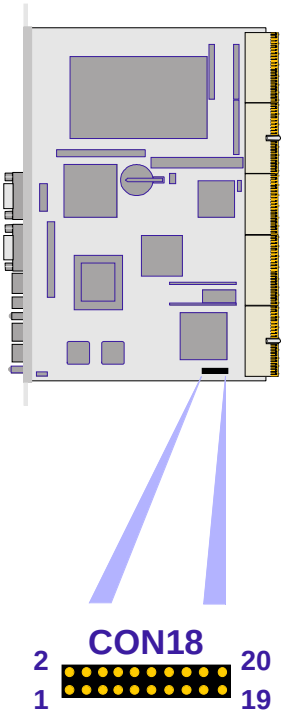
Pin Number	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C	--	--
33	A1	Address 1	Out
34	N/C	--	--
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	LED	LED driving	In
40	GND	Ground signal	--

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2.8.10 Floppy Drive Interface

The onboard floppy disk controller supports either 5.25 inch or 3.5 inch (1.44 or 2.88 MB) floppy disks. A 20-pin male connector provides the signals for a floppy-drive that can be installed by means of a special adapter.

Figure 2-15: CON18: Floppy Drive Interface



Floppy drive connector pinout follows on next page

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2.8.10.1 Floppy Drive Connector CON18 Pinout

Table 2-12: Floppy Drive Connector CON18 Pinout

Pin Number	Signal	Function	In/Out
1-4	GND	Ground signal	--
5	DSKCH	Disk change	In
6	HDSEL	Head select	Out
7	RDATA	Read data	In
8	WP	Write protect	In
9	TRK0	Track 0 signal	In
10	WGAT	Write enable	Out
11	WDAT	Write data	Out
12	STEP	Step pulse	Out
13	DIR	Step direction	Out
14	MTR1	Motor 1 enable	Out
15	DS0	Driver select 0	Out
16	DS1	Driver select 1	Out
17	MTR0	Motor 0 enable	Out
18	INDEX	Index pulse	In
19	DRVDEN1	Drive and media select	Out
20	DRVDEN0	Drive and media select	Out



Note:

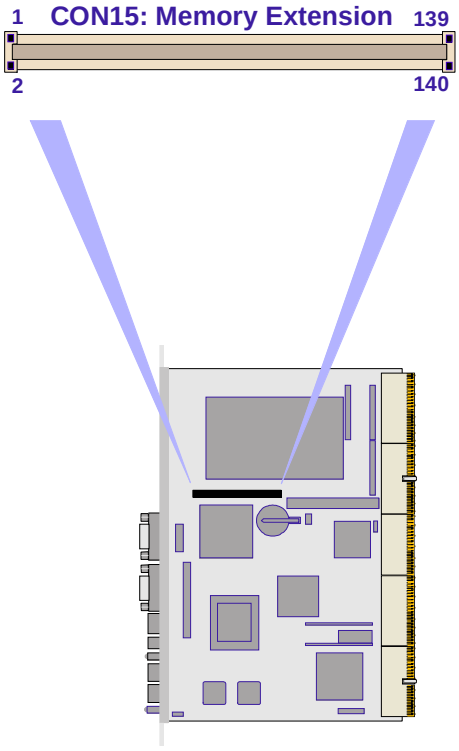
The adapter must be mounted directly onto the floppy drive. There is, therefore, no necessity for an intermediate cable between the floppy drive and the adapter.

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2.8.11 Memory Extension Connector CON15

The memory extension connector CON15 provides all the necessary signals for the memory extension module.

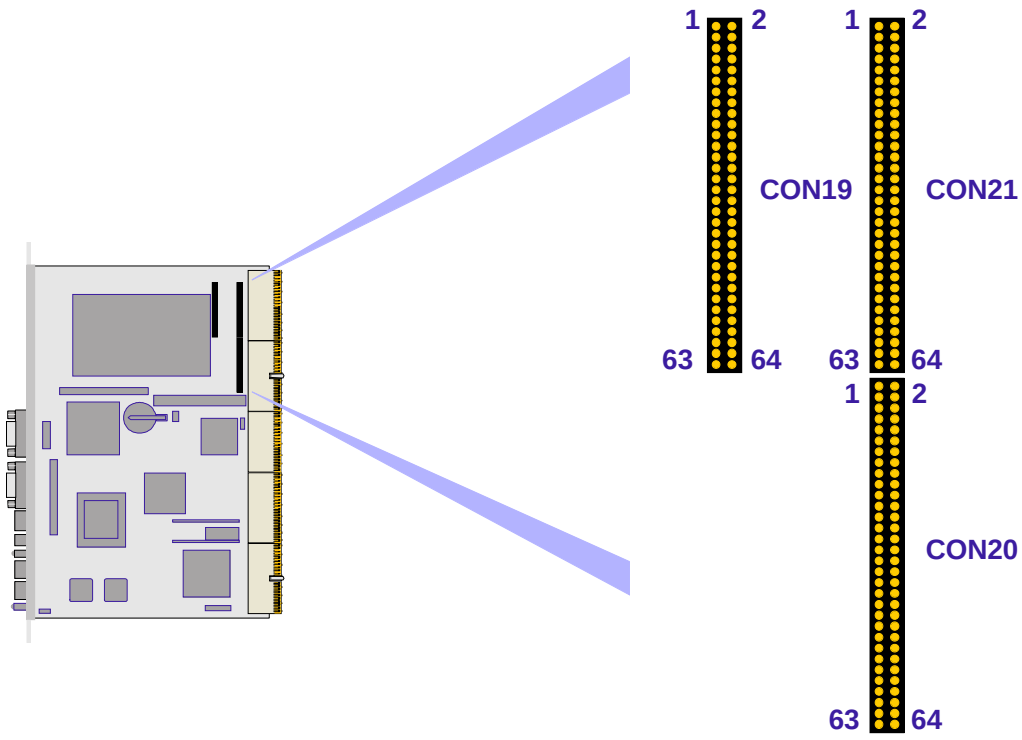
Figure 2-16: Memory Extension Connector CON15



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2.8.12 PMC Interface

Figure 2-17: PMC Connectors CON19, 20 and 21



For flexible and easy configuration one onboard PMC socket is available. The PN1 and PN2 connectors provide the signals for the 32-bit PCI Bus. The 64-bit interface for the PMC interface is not implemented. User defined I/O signals are supported and are connected to the CompactPCI rear I/O connector J5.

This interface has been designed to comply with the IEEEP1386.1 specification which defines a PCI electrical interface for the CMC (Common Mezzanine Card) form factor. The CP604-PM provides for either a 5V or 3.3V PMC PCI signaling environment.

PMC connector pinouts follow on next page.



Note:

The PMC rear I/O signals from CON20 are routed to CompactPCI connector J5, whose pinout is provided in Table 2-20.

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2.8.12.1 PMC Connectors CON19 and CON21 Pinouts

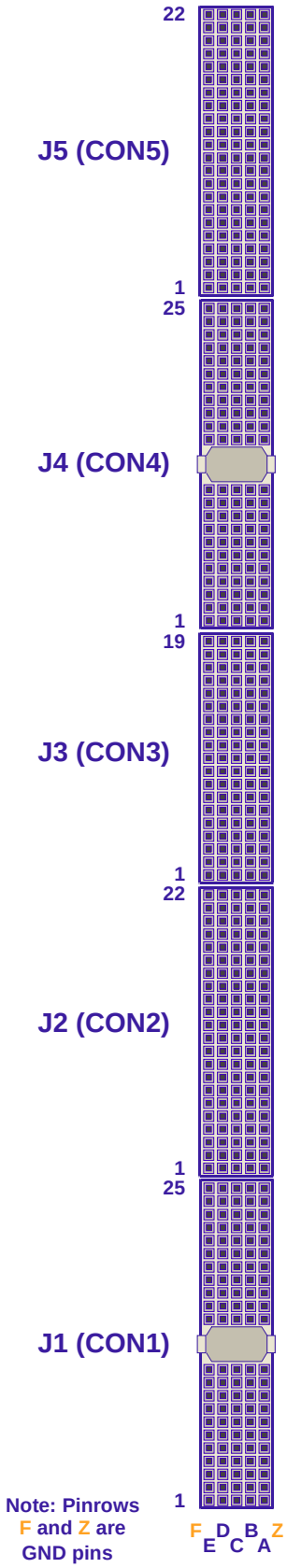
Table 2-13: PMC Connectors CON19 and CON21 Pinouts

PN1/JN1 (CON19)				PN2/JN2 (CON21)			
Pin #	**Signal Name**	**Signal Name**	**Pin #**	**Pin #**	**Signal Name**	**Signal Name**	**Pin #**
1	Signal	-12V	2	1	+12V	Signal	2
3	Ground	Signal	4	3	Signal	Signal	4
5	Signal	Signal	6	5	Signal	Ground	6
7	BUSMODE1#	+5V	8	7	Ground	Signal	8
9	Signal	Signal	10	9	Signal	Signal	10
11	Ground	Signal	12	11	BUSMODE2#	+3.3V	12
13	Signal	Ground	14	13	Signal	BUSMODE3#	14
15	Ground	Signal	16	15	+3.3V	BUSMODE4#	16
17	Signal	+5V	18	17	Signal	Ground	18
19	V (I/O)	Signal	20	19	Signal	Signal	20
21	Signal	Signal	22	21	Ground	Signal	22
23	Signal	Ground	24	23	Signal	+3.3V	24
25	Ground	Signal	26	25	Signal	Signal	26
27	Signal	Signal	28	27	+3.3V	Signal	28
29	Signal	+5V	30	29	Signal	Ground	30
31	V (I/O)	Signal	32	31	Signal	Signal	32
33	Signal	Ground	34	33	Ground	Signal	34
35	Ground	Signal	36	35	Signal	+3.3V	36
37	Signal	+5V	38	37	Ground	Signal	38
39	Ground	Signal	40	39	Signal	Ground	40
41	Signal	Signal	42	41	+3.3V	Signal	42
43	Signal	Ground	44	43	Signal	Ground	44
45	V (I/O)	Signal	46	45	Signal	Signal	46
47	Signal	Signal	48	47	Ground	Signal	48
49	Signal	+5V	50	49	Signal	+3.3V	50
51	Ground	Signal	52	51	Signal	Signal	52
53	Signal	Signal	54	53	+3.3V	Signal	54
55	Signal	Ground	56	55	Signal	Ground	56
57	V (I/O)	Signal	58	57	Signal	Signal	58
59	Signal	Signal	60	59	Ground	Signal	60
61	Signal	+5V	62	61	Signal	+3.3V	62
63	Ground	Signal	64	63	Ground	Signal	64

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2.8.13 CompactPCI Bus Interface

Figure 2-18: CompactPCI Connectors J1-J5 (CON1-CON5)



The complete CompactPCI connector configuration comprises five connectors named J1 to J5. Their functions are as follows:

- J1/J2: 64-bit CompactPCI interface with PCI bus signals, arbitration, clock and power.
- J3 and J5 have rear I/O interface functionality.
- J4 only has optional rear I/O interface functionality.

The CP604-PM is designed for a CompactPCI bus architecture. The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

The CP604-PM is hotswappable, which means it may be installed in and removed from a hotswap compliant backplane whilst the system is powered-up and running. The board may also be used in a standard CompactPCI system without Hotswap support.

2.8.13.1 CompactPCI Connector Keying

CompactPCI connectors support guide lugs to ensure a correct polarized mating. A proper mating is further assured by the use of color coded keys for 3.3V and 5V operation.

Color coded keys prevent inadvertent installation of a 5V peripheral board into a 3.3V slot. The CP604-PM hotswap board is a 5V version. Backplane connectors are always keyed according to the signaling (VIO) level. Coding key colors are defined as follows:

Table 2-14: Coding Key Colors

Signaling Voltage	Key Color
3.3V	Cadmium Yellow
5V	Brilliant Blue
Universal board (5V and 3.3V)	None

CompactPCI connector pinouts appear on the following pages

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2.8.13.2 CompactPCI Connectors CON1 and CON2 Pinouts

The CP604-PM is provided with two 2 mm x 2 mm pitch female CompactPCI bus connectors, J1 and J2.

Table 2-15: CompactPCI Bus Connector J1 (CON1) Pinout

Pin #	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O) 2)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V 2)	AD[2]	GND
22	GND	AD[7]	GND	3.3V 2)	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND 2)	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB SCL	IPMB SDA	GND 2)	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD SEL# 1)	TRDY#	GND
12-14	Key Area						
11	GND	AD[18]	AD[17]	AD[16]	GND 2)	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL 1)	AD[23]	GND 2)	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND 2)	AD[27]	GND
6	GND	REQ#	GND	3.3V 2)	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND 2)	GNT#	GND
4	GND	IPMB PWR	HEALTHY#	V(I/O) 2)	NC	NC	GND
3	GND	INTA#	INTB#	INTC#	5V 2)	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND

Key:-

1) short pins (front only)

2) long pins (front only)

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Table 2-16: CompactPCI Bus Connector J2 (CON2) Pinout

Pin #	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	NC	NC	NC	NC	NC	GND
20	GND	NC	NC	NC	GND	NC	GND
19	GND	NC	NC	NC	NC	NC	GND
18	GND	NC	NC	NC	GND	NC	GND
17	GND	NC	GND	NC	NC	NC	GND
16	GND	NC	NC	NC	GND	NC	GND
15	GND	NC	GND	NC	NC	NC	GND
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	GND	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	GND	C/BE[5]	64EN#	V(I/O)	C/BE[4]#	PAR64	GND
4	GND	V(I/O)	NC	C/BE[7]#	GND	C/BE[6]#	GND
3	GND	NC	GND	NC	NC	NC	GND
2	GND	NC	NC	NC	NC	NC	GND
1	GND	NC	GND	NC	NC	NC	GND

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2.8.13.3 CompactPCI Rear I/O Connectors J3-J5 (CON3-CON5) and Pinouts

The CP604-PM conducts all I/O signals through the rear I/O connectors J3, J4 and J5. The CP604-PM board provides optional rear I/O connectivity for peripherals for special compact systems. All standard PC interfaces are implemented and assigned to the front panel and to the rear I/O connectors J3, J4 and J5 (CON3, CON4 and CON5).

When the rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus the rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the system rear I/O feature a special backplane is necessary. The CP604-PM with rear I/O is compatible with all standard 6U CompactPCI passive backplanes with rear I/O support on the system slot.

The CP604 conducts all I/O signals through the rear I/O connectors J3, J4 and J5.

Table 2-17: Backplane J3 Pin Definitions

Pin	Z	A	B	C	D	E	F
19	GND	IDERST 6)	IDE-ICHRDYB 8)	IDE-ICHRDYA 6)	IDEIRQB 8)	IDEIRQA 6)	GND
18	GND	IDECSB0 8)	IDECSB1 8)	IDECSA0 6)	IDECSA1 6)	IDEDAKB 8)	GND
17	GND	IDEDA15 6)	IDPDA14 6)	IDEDA13 6)	IDEDA12 6)	IDEDRQB 8)	GND
16	GND	IDEDA11 6)	IDEDA10 6)	IDEDA9 6)	IDEDA8 6)	IDEDAKA 6)	GND
15	GND	IDEAA0 6)	IDEAA1 6)	VCC	IDEAA2 6)	IDEDRQA 6)	GND
14	GND	IDEDA7 6)	IDEDA6 6)	IDEDA5 6)	IDEDA4 6)	IDEIOWA 6)	GND
13	GND	IDEDA3 6)	IDEDA2 6)	IDEDA1 6)	IDEDA0 6)	IDEIORA 6)	GND
12	GND	FD.DS0 7)	FD.DENSEL1 7)	FD.MTR0 7)	FD.INDEX 7)	FD.WDATA 7)	GND
11	GND	FD.DS1 7)	FD.DSKCHG 7)	FD.MTR1 7)	FD.DENSEL0 7)	FD.RDATA 7)	GND
10	GND	FD.WP 7)	FD.HDSEL 7)	FD.DIR 7)	FD.TRK0 7)	FD.STEP 7)	GND
9	GND	FD.WGATE 7)	IDEDB15 8)	IDEDB14 8)	IDEDB13 8)	USB0+ 2)	GND
8	GND	IDEDB12 8)	IDEIOWB 8)	VCC	IDEIORB 8)	USB0- 2)	GND
7	GND	IDEAB2 8)	IDEAB1 8)	IDEAB0 8)	IDEDB0 8)	IDEDB1 8)	GND
6	GND	IDEDB2 8)	IDEDB3 8)	IDEDB4 8)	IDEDB5 8)	IDEDB6 8)	GND
5	GND	SMBCLK 1)	PMDAT 5)	SPKR 1)	KDAT 5)	SMBDAT 1)	GND
4	GND	PRST 1)	PMCLK 5)	VCC	KCLK 5)	S3RXD 3)	GND
3	GND	S3CTS 3)	S3RTS 3)	S3DSR 3)	S3DCD 3)	S3TXD 3)	GND
2	GND	IDEDB7 8)	IDEDB8 8)	S3RIN 3)	S3DTR 3)	S4RXD 4)	GND
1	GND	IDEDB9 8)	IDEDB10 8)	IDEDB11 8)	BATT 1)	S4TXD 4)	GND

The legend for this table appears on the following page

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Legend for Backplane J3 Table

Table 2-18: Backplane J3 Signal Functions

Signal	Function
Control Signals	
SPKR 1)	Speaker output signal
BATT 1)	Battery input signal for RTC; max. 3.3V
PRST 1)	Reset input signal
SMBCLK, SMBDAT 1)	Onboard SMBus signals
USB port 0	
USB0+/- 2)	USB data differential data signals
Serial Port 3	
S3* 3)	Serial port signals; TTL level
Serial Port 4	
S4RXD S4TXD 4)	Serial port signals; TTL level
Mouse + Keyboard	
KDAT 5), KCLK 5)	Keyboard data and clock
PMDAT 5), PMCLK 5)	Mouse data and clock
IDE*A 6)	IDE Primary signals
Blue signals 7)	Floppy signals
IDE*B 8)	IDE Secondary signals

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Table 2-19: Backplane J4 Pin Definitions

Pin	Z	A	B	C	D	E	F
25	GND	VCC	RES 4)	RES 4)	+3.3V	VCC	GND
24	GND	RES 4)	PD0 1)	INIT 1)	RES 4)	RES 4)	GND
23	GND	+3.3V	RES	RES 4)	VCC 2)	RES 4)	GND
22	GND	RES 4)	PD1 1)	RES 4)	RES 4)	RES 4)	GND
21	GND	+3.3V	RES 4)	AUTOFD 1)	RES 4)	J2ALERT 2)	GND
20	GND	RES 4)	PD2 1)	SLCTIN 1)	J2SCL 2)	J2SDA 2)	GND
19	GND	+3.3V	PD3 1)	STROBE 1)	RES 4)	IPMIGPIO2 2)	GND
18	GND	RES 4)	PD4 1)	RES 4)	PWM1 2)	PWM0 2)	GND
17	GND	+3.3V	PD5 1)	BUSY 1)	RES 4)	TACH_IN3 2)	GND
16	GND	RES	PD6 1)	RES 4)	TACH_IN2 2)	TACH_IN1 2)	GND
15	GND	+3.3V	PD7 1)	ACK 1)	RES 4)	TACH_IN0 2)	GND
12-14	GND						GND
11	GND	RES 4)	IPMI VCC 1)	PE 1)	RES 4)	CONN_ID_DRV 2)	GND
10	GND	RES 4)	RES 4)	RES 4)	ID_XMIT_EN 2)	CONN_ID1 2)	GND
9	GND	RES 4)	IPMI VCC	SLCT 1)	RES 4)	CONN_ID0 2)	GND
8	GND	RES	GND	RES 4)	XMIT_EN 2)	UART0_RI 2)	GND
7	GND	GND	LVDS TX_P2 3)	ERROR 1)	RES 4)	UART0_RTS 2)	GND
6	GND	RES 4)	LVDS TX_N2 3)	RES 4)	UART0_DCD	UART0_CTS 2)	GND
5	GND	GND	GND	LVDS TX_P1 3)	UART0_DOUT 2)	UART0_DIN 2)	GND
4	GND	RES 4)	GND	LVDS TX_N1 3)	GND	GND	GND
3	GND	LVDS ENAVDD 3)	LVDS FPVEE 3)	GND	LVDS TX_P0 3)	LVDS TXCLKP 3)	GND
2	GND	RES 4)	RES 4)	GND	LVDS TX_N0 3)	LVDS TXCLKN 3)	GND
1	GND	VCC	-12V	GND	+12V	VCC	GND

Legend for Backplane J4 Table

1) Parallel Port signals

2) IPMI control signals

3) VGA LVDS signals

4) Reserved

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Table 2-20: Backplane J5 Pin Definitions

Pin	Z	A	B	C	D	E	F
22	GND	PMCR4	PMCR3	PMCR2	PMCR1	PMCR0	GND
21	GND	PMCR9	PMCR8	PMCR7	PMCR6	PMCR5	GND
20	GND	PMCR14	PMCR13	PMCR12	PMCR11	PMCR10	GND
19	GND	PMCR19	PMCR18	PMCR17	PMCR16	PMCR15	GND
18	GND	PMCR24	PMCR23	PMCR22	PMCR21	PMCR20	GND
17	GND	PMCR29	PMCR28	PMCR27	PMCR26	PMCR25	GND
16	GND	PMCR34	PMCR33	PMCR32	PMCR31	PMCR30	GND
15	GND	PMCR39	PMCR38	PMCR37	PMCR36	PMCR35	GND
14	GND	PMCR44	PMCR43	PMCR42	PMCR41	PMCR40	GND
13	GND	PMCR49	PMCR48	PMCR47	PMCR46	PMCR45	GND
12	GND	PMCR54	PMCR53	PMCR52	PMCR51	PMCR50	GND
11	GND	PMCR59	PMCR58	PMCR57	PMCR56	PMCR55	GND
10	GND	+3.3V	PMCR63	PMCR62	PMCR61	PMCR60	GND
9	GND	TDN2 2)	RDN2 2)	S1RXD 4)	TDN1 2)	RDN1 2)	GND
8	GND	TDP2 2)	RDP2 2)	S1TXD 4)	TDP1 2)	RDP1 2)	GND
7	GND	COM2_ENABLE 1)	COM1_ENABLE 1)	S1RTS 4)	USB1+ 3)	+3.3V	GND
6	GND	S1DTR 4)	S1CTS 4)	S1DSR 4)	S1DCD 4)	S1RIN 4)	GND
5	GND	S2RXD 5)	S2TXD 5)	S2RTS 5)	S2DTR 5)	ROUT 8)	GND
4	GND	S2DSR 5)	S2DCD 5)	S2RIN 5)	S2CTS 5)	HSYNC 8)	GND
3	GND	S4DTR 6)	S4CTS 6)	S4DSR 6)	GPLED 1)	BOUT 8)	GND
2	GND	S4RTS 6)	S4RIN 6)	FANSENSE2 7)	FANPWM 7)	VSYNC 8)	GND
1	GND	S4DCD 6)	RIOPRESENT 1)	FANSENSE1 7)	USB1- 3)	GOUT 8)	GND

The legend for this table appears on the following page

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Legend for Backplane J5 Table

Table 2-21: Backplane J5 Signal Functions

Signal	Function
Control signals	
COM1_ENABLE 1)	Serial port 1 enable signal for front I/O and rear I/O Low = Front I/O High = Rear I/O
COM2_ENABLE 1)	Serial port 2 enable signal for front I/O and rear I/O Low = Front I/O High = Rear I/O
GPLED 1)	General purpose LED output
RIOPRESENT 1)	Low = rear I/O module is present High = rear I/O module is not present This signal must be set on the rear I/O module to GND
Ethernet 1	
TDP1 2)	Ethernet high transmit Data line
TDN1 2)	Ethernet low transmit Data line
RDP1 2)	Ethernet high receive Data line
RDN1 2)	Ethernet low receive Data line
Ethernet 2	
TDP2 2)	Ethernet high transmit Data line
TDN2 2)	Ethernet low transmit Data line
RDP2 2)	Ethernet high receive Data line
RDN2 2)	Ethernet low receive Data line
USB port 1	
USB1+/- 3)	USB data differential data signals
Serial Port 1	
S1* 4)	Serial port signals; TTL level
Serial Port 2	
S2* 5)	Serial port signals; TTL level
Serial Port 4	
S4* 6)	Serial port signals; TTL level
FAN control	
FANPWM 7)	DAC output that can be used to control fan speed; 0V to +1.25V output
FANSENSE1/2 7)	Schmitt Trigger fan tachometer inputs; TTL level
VGA CRT signals	
ROUT 8)	Red signal
GOUT 8)	Green signal
BOUT 8)	Blue signal
HSYNC 8)	Horizontal Sync.
VSYNC 8)	Vertical Sync.
PMC Rear I/O signals	PMCR0 to PMCR63 (Spec.) carry the signals from PMC rear I/O connector CON20 pins 1 to 64

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2.8.13.4 Rear I/O Configuration

Rear I/O interfaces are only available on the rear I/O version of the board.

Ethernet Interface

Ethernet signals are available on the front RJ45 connector and on the rear I/O interface.

The combination of both front and rear I/O is not supported. Both Fast Ethernet channels are decoupled, but enabled separately. It is not possible to operate both the rear and front I/O at the same time. Switching over from front to rear I/O or vice versa is effected under BIOS control without the need to plug/unplug Ethernet cables.

VGA CRT Interface

The VGA signals are available on rear I/O and front I/O. In this configuration both interfaces are active. The 75 ohm termination resistor for the red, green and blue video signals are equipped on the CP604-PM.



Note:

Both VGA ports are electrically identical and not separated. Do not connect devices at both connectors (front I/O and rear I/O) at the same time.

VGA LVDS Interface

The VGA LVDS signals are available both on the rear I/O and front I/O, but only one interface may be used at a time. To configure the LVDS port for rear I/O requires the installation of zero ohm resistors on the board to connect the signals to the rear I/O connector.

Serial Interface COM1 and COM2

Only one interface may be used (rear I/O or front I/O). If the rear I/O interface is enabled the drivers for the COM1 and COM2 port on the CP604-PM must be disabled. The configuration can be accomplished via the BIOS.

Serial Interface COM3 and COM4

Only on rear I/O interface available.

Parellel Port LPT1

Only on rear I/O interface available.

Keyboard/Mouse Interface

All PS2 connectors are electrically identical. Due to this it is not possible to use a mouse at the front I/O and a second mouse at the rear I/O port at the same time.

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USB Interface

There are two independent USB interfaces available, one port is routed to the 4-pin front I/O connector. This port may also be used on the rear I/O interface. The second port is only available on the rear I/O connector.

The USB 1 port is electrically identical and not separated. Do not connect devices at both connectors (front I/O and rear I/O) at the same time.

EIDE Interface

Only one EIDE connector may be used at any one time through the same port; connecting both EIDE devices to the CP604-PM baseboard and the CP-RIO6-04 simultaneously will result in malfunction and data loss. EIDE channels 1 and 2 are separate channels - it is possible to use EIDE channel 1 onboard and channel 2 via the rear I/O.

Floppy Interface

Only one floppy connector may be used at any one time; connecting both floppy drives to the CP604-PM baseboard and the CP-RIO6-04 simultaneously will result in malfunction and data loss.

2.8.14 Non-System Relevant Connectors

CON12, CON14 and CON16 are non-system relevant. CON12 used to connect the hotswap handle switch. CON14 is used for the front panel VGA configuration and CON16 is used to program onboard logic.

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2.9 Jumper Description

2.9.1 External BIOS

It is possible to redirect the first CPU fetch from the onboard flash to the Flash socket. If jumper J1 is open, the board boots from the BIOS in the onboard flash memory. When J1 is closed, the board boots from the socket flash.

Table 2-22: External BIOS Setting

J1	Function	Comment
Closed	External Bios	Use this setting only if the onboard flash does not work
Open	*Internal Bios*	*Normal boot from the onboard BIOS*

The default setting is indicated by italics.

2.9.2 Memory Type Selection

This solder jumper selects the memory type to be installed on the flash socket IC35.

Table 2-23: Memory Type Selection

J9	J8	Memory type
1-2	1-2	SRAM with 256 kB or 512 kB
1-3	*1-3*	*All DiskOnChip ™, Flash and EPROM types up to 4 Mbit*

The default setting is indicated by italics.

2.9.3 Flash Type Selection

This solder jumper selects the flash type to be installed on the flash socket IC35.

Table 2-24: Flash Type Selection

J10	Function
Closed	4 Mbit flash type
Open	*2 Mbit flash type*

The default setting is indicated by italics.

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2.9.4 PCI VI/O setting

The CP604-PM provides for either a 5V or 3.3V onboard PCI signaling environment.

The BVI/O power jumpers on the board are used to power the buffers on the peripheral boards and the PMC interface. The BVI/O does not provide power to the CompactPCI interface. The CompactPCI VI/O must be configured via the backplane.

Table 2-25: PCI VI/O setting

Board VI/O setting	R139	R138
5V	*Open*	*Closed*
3.3V	Closed	Open

The default setting is indicated by italics.

2.9.5 Shorting Chassis GND (Shield) to Logic GND

The front panel and the front panel connectors are isolated to the logic ground. These zero Ohm resistors enable connection between the chassis GND and logic GND.

Table 2-26: Shorting Chassis GND (Shield) to Logic GND

R23/R25	Function
Open	*Connectors are isolated to logic GND*
Closed	Connectors are connected to logic GND and chassis GND

The default setting is indicated by italics.

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2.9.6 Panel Selection

The jumper/resistor settings necessary to select one of the supported panels are shown in the following table.

Table 2-27: Display Type Selection

N°	Panel Parameters/Type	R225	R223	R224	R222
1	1024 x 768 DSTN Color	Closed	Closed	Closed	Closed
2	1280 x 1024 TFT Color	Closed	Closed	Closed	Open
3	640 x 480 DSTN Color	Closed	Closed	Open	Closed
4	800 x 600 DSTN Color	Closed	Closed	Open	Open
5	640 x 480 SHARP TFT Color	Closed	Open	Closed	Closed
6	640 x 480 TFT Color 18-bit	Closed	Open	Closed	Open
7	**Sharp LQ 150X1DG11** 1024 x 768 TFT LCD	Closed	Open	Open	Closed
8	**NEC NL 8060AC31-12** 800 x 600 TFT LCD	Closed	Open	Open	Open
9	800 x 600 TFT Color	Open	Closed	Closed	Closed
10	800 x 600 TFT Color	Open	Closed	Closed	Open
11	800 x 600 DSTN Color	Open	Closed	Open	Closed
12	800 x 600 DSTN Color	Open	Closed	Open	Open
13	***Toshiba LTM 10C306L*** *1024 x 768 TFT Color*	*Open*	*Open*	*Closed*	*Closed*
14	1280 x 1024 DSTN Color	Open	Open	Closed	Open
15	1024 x 600 DSTN Color	Open	Open	Open	Closed
16	1024 x 600 TFT Color	Open	Open	Open	Open
Note: The logical panel code values are inverted, i.e. “closed” is equal to 0, “open” to 1.					

The default setting is indicated by italics.

Panel numbers refer to BIOS panel numbering. Panel numbers 7 and 8 correspond to preset panel types.



Note:

To see the location of the resistors R222, R223, R224 and R225 on the board, please refer to Figure 2-4 on page 2-8 of this chapter.

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2.9.7 Serial Port Jumper and Resistor Setting

2.9.7.1 COM1 Jumper and Resistor Setting

The serial interfaces CON6 (COM1) and CON7 (COM2) on the CP604-PM may be configured for either RS232, RS422 or RS485 by setting solder jumpers.

Table 2-28: Resistor Setting to Configure COM1

Resistor	RS232	RS422	RS485
R100	*Open*	Closed	Closed
R129	*Open*	Open	Closed
R130	*Closed*	Closed	Open
R118	*Open*	Closed	Open

The default setting is indicated by italics.



Note:

The serial port may be disabled by the BIOS.

RS422 and RS485 COM1 Termination

When the CP604-PM is using the onboard RS485 interface and is the last device on the RS422 or RS485 bus, then the RS422 or RS485 interface must provide termination resistance. The purpose of jumpers J3 and J2 are to enable this line termination resistor (120 R).

Table 2-29: Jumper Setting for RS422 RXD Termination (COM1)

Termination	J3
ON	Closed
OFF	*Open*

The default setting is indicated by italics.

Table 2-30: Jumper Setting for RS422 TXD and RS485 Termination (COM1)

Termination	J2
ON	Closed
OFF	*Open*

The default setting is indicated by italics.

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2.9.7.2 COM2 Jumper and Resistor Setting

Table 2-31: Resistor Setting to Configure COM2

Resistor	RS232	RS422	RS485
R2	*Open*	Closed	Closed
R68	*Open*	Open	Closed
R69	*Closed*	Closed	Open
R6	*Open*	Closed	Open

The default setting is indicated by italics.

RS422 and RS485 COM2 Termination

When the CP604-PM is using the onboard RS485 interface and is the last device on the RS422 or RS485 bus, then the RS422 or RS485 interface must provide termination resistance. The purpose of jumpers J5 and J4 are to enable this line termination resistor (120 R).

Table 2-32: Jumper Setting for RS422 RXD Termination (COM2)

Termination	J5
ON	Closed
OFF	*Open*

The default setting is indicated by italics.

Table 2-33: Jumper Setting for RS422 TXD and RS485 Termination (COM2)

Termination	J4
ON	Closed
OFF	*Open*

The default setting is indicated by italics.

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2.9.8 Jumper/Resistor Setting for Rear I/O

CRT Interface

The VGA CRT signals are available on the rear I/O and on the front I/O. In this configuration both interfaces are active. The 75 Ohm termination resistor for the red, green and blue video signals are equipped on the CP604-PM.

Table 2-34: VGA Interface Configuration

Configuration	Location
75 Ohm for red	R35
75 Ohm for green	R32
75 Ohm for blue	R42



Note:

Both VGA ports are electrically identical and not separated. Do not connect devices at both connectors (front I/O and rear I/O) at the same time.

VGA LVDS Interface

The VGA LVDS signals are available on the rear I/O and on the front I/O. To configure the LVDS port for rear I/O requires the installation of zero Ohm resistors on the board to connect the signals to the rear I/O connector.

Table 2-35: VGA LVDS Interface Configuration

Configuration	Front I/O	Rear I/O
R172 – R179	*Closed*	Open
R191 – R198	*Open*	Closed

The default setting is indicated by italics



Important:

The combination of both front and rear I/O is not supported.

2.9.9 Reserved Jumpers

All other jumpers that are not specifically described are reserved for future configurations.

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2.10 Memory Map

The CP604-PM board uses the standard AT ISA memory map.

The following table displays the memory map for the first megabyte:

Table 2-36: Memory Map for the 1st Megabyte

Memory Range (Hex.)	Size	Function
0xE0000-0xFFFFF	**128k**	BIOS implemented in Flash Reset vector FFFF0h
0xD0000-0xDFFFF	**8k/64k**	Flash disk: min. 8 kB, max. 64 kB
0xCB000-0xCFFFF	**16k**	Onboard Flash
0xC0000-0xCBFFF	**48k**	BIOS of the VGA card
0xA0000-0xBFFFF	**128k**	Normally used as video RAM as follows: CGA video: 0xB8000-0xBFFFF Monochrome video: 0xB0000-0xB7FFF EGA/VGA video: 0xA0000-0xAFFFF
0x00000-0x9FFFF	**640k**	DOS reserved memory space

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2.11 I/O Address Map

Table 2-37: I/O Address Map

Address Range (Hex.)	Device
000,00F	DMA controller #1
020,021	Interrupt controller #1
022,02F	Reserved
040,043	Timer
060,063	Keyboard interface
070,071	RTC port
080,08F	DMA page register
0A0,0A	Interrupt controller #2
0C0,0DF	DMA controller #2
0E0,0EF	Reserved
0F0,0FF	Math coprocessor
170,17F	Hard disk secondary
1F0,1FF	Hard disk primary
278,27F	Parallel port LPT2
280	Watchdog trigger
282	Watchdog time
284	Interrupt routing
285	PCI master reset
286	I/O status
288	Board version
289	Hardware index
28A	Jumper status
28B	Logic index
28C	PCI Interrupt routing
28E	Memory management
28F	Flash Socket Page
2E8,2EF	Serial port COM4
2F8,2FF	Serial port COM2
378,37F	Parallel printer port LPT1
3BC,3BF	Parallel printer port LPT3
3E8,3EF	Serial port COM3
3F0,3F7	Floppy Disk + Super-I/O #1 Com.
3F8,3FF	Serial port COM1
340	LED control
E0,E7	IPMI controller
CA0,CA3	IPMI controller

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2.12 Interrupts

The CP604-PM board uses the standard AT IRQ routing (8259 Controller).

This interrupt routing is default but it can be modified within the BIOS.

Table 2-38: Interrupt Configuration

IRQ	Priority	Standard Function
IRQ0	1	System Timer
IRQ1	2	Keyboard Controller
IRQ2	--	Input of the second IRQ controller (IRQ8-IRQ15)
IRQ3	11	COM2
IRQ4	12	COM1
IRQ5	13	Watchdog, COM3
IRQ6	14	Floppy Disk Controller
IRQ7	15	COM4 or parallel port
IRQ8	3	System Real Time Clock
IRQ9	4	PCI or ACPI
IRQ10	5	PCI or IPMI controller
IRQ11	6	PCI
IRQ12	7	PCI or PS/2 mouse
IRQ13	8	Coprocessor error
IRQ14	9	Primary hard disk
IRQ15	10	Secondary hard disk
NMI	--	Watchdog

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2.13 Special Registers Description

The following registers are special registers for the CP604-PM to watch the onboard hardware special features and the CompactPCI control signals.

Normally, only the system BIOS uses these registers, but they are documented here for application use as required. Take care when modifying the contents of these registers as the system BIOS may be relying on the state of the bits under its control.

2.13.1 Watchdog

The CP604-PM has one watchdog timer. This timer is provided with a programmable timeout ranging from 125 msec to 256 sec. Failure to retrigger the watchdog timer within a set time period results in a system reset, NMI, or an interrupt. These can be configured via the register 0x284.

To enable the watchdog bit 4 of the register 0x282 must be set. If the watchdog is enabled via bit 4” this bit cannot later be cleared.

With a write access to the register 0x280 the watchdog is re-triggered. Once the watchdog is enabled, it must be continuously strobed within the terminal count period to avoid expiry of the watchdog.

2.13.1.1 Watchdog Trigger

A write access triggers the watchdog.

The I/O location for the watchdog trigger is 0x280.

The Watchdog Timer section appears on the following page

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2.13.1.2 Watchdog Timer

The CP604-PM has one watchdog timer with a programmable timeout ranging from 125 msec. to 256 sec.

The I/O location for the watchdog configuration is 0x282.

Table 2-39: Watchdog Configuration

Bits	Type	Default	Function
7-5	R	0	Reserved
4	RW	0	1 = enable watchdog (write) 0 = disable watchdog (read only)
3-0	RW	0	The nominal timeout period is 20% longer than the minimum. 0 = 125 msec 1 = 250 msec 2 = 500 msec 3 = 1 sec 4 = 2 sec 5 = 4 sec 6 = 8 sec 7 = 16 sec 8 = 32 sec 9 = 64 sec 10 = 128 sec 11 = 256 sec 12-15 reserved

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2.13.2 Interrupt Configuration Register

The interrupt configuration register holds a series of bits defining the interrupt routing for the watchdog. If the watchdog timer timesout, it can generate three independent hardware events: a reset, NMI, or an IRQ5 interrupt.

The I/O location for the interrupt configuration is 0x284.

Table 2-40: Onboard Interrupt Configuration

Bits	Type	Default	Function
7	RW	0	Watchdog NMI routing 1 = enable NMI 0 = disable NMI
6-3	R	0	Reserved
2	RW	0	Watchdog hardware reset 1 = enable reset 0 = disable reset
1	RW	0	Watchdog IRQ5 routing 1 = enable IRQ5 0 = disable IRQ5
0	RW	0	Reserved

2.13.3 PCI Master Reset

This register controls the reset signal from the CompactPCI interface to the local reset controller.

If the reset is disabled, the CP604-PM ignores the reset signal from the CompactPCI interface.

The default configuration is enabled.

The I/O location of the PCI master reset is 0x285.

Table 2-41: PCI Master Reset

Bits	Type	Default	Function
7-0	R	1	1 = enables the reset routing from the CompactPCI interface 0 = disabled

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2.13.4 I/O Status

This register describes the local and CompactPCI control signals. The watchdog status bit indicates the status of the watchdog timer. If the timer is not re-triggered within the previously set time period, the bit is set to “0”.

The I/O location for the I/O status is 0x286.

Table 2-42: I/O Status

Bits	Type	Default	Function
7	R	--	Watchdog status 0 = watchdog interrupt
6	R	--	Reserved
5	R	--	Reserved
4	R	--	Reserved
3	R	--	System slot identification 0 = System slot
2	R	--	Reserved
1	R	--	Reserved
0	R	--	Reserved

2.13.5 Board ID

This register describes the board index.

The I/O location for the Board ID is 0x288.

Table 2-43: Board ID

Bits	Type	Default	Function
7-0	R	--	Board version 0 = reserved 0x48 = CP604 0x49 = CP604-PM 0x4A = CP604-PM-O 0x4B = CP604-R

The content of this register is unique for each *PEP* CompactPCI board.

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2.13.6 Hardware Index

The hardware index will signal to the software when differences in the hardware require different handling by the software. It starts with the value “0” and will be incremented with each change in hardware as development continues.

The I/O location for the hardware index is 0x289.

Table 2-44: Hardware Index

Bits	Type	Default	Function
7-0	R	--	Revision ID 0 = Index 0000

2.13.7 Jumper Status

This register can be used to read the onboard jumper configuration.

The I/O location for the jumper status is 0x28A.

Table 2-45: Jumper Status

Bits	Type	Default	Function
7	R	1	Boot jumper 1 = onboard flash 0 = socket flash
6-3	R	--	Reserved
2	R	--	Rear I/O module status 1 = no rear I/O module plugged in 0 = rear I/O module plugged in
1	R	--	Reserved
0	R	--	Reserved

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2.13.8 Logic Version

The logic version register may be used to identify the logic status of the board by software. It starts with the value 0 and will be incremented with each logic update.

The I/O location for the logic version is 0x28B.

Table 2-46: Logic Version

Bits	Type	Default	Function
7-0	R	--	Logic version 0 = Index 0000

2.13.9 PCI Interrupt Routing

This register is used by the CPU to control the PCI interrupt routing. Every interrupt line of the backplane can be enabled or disabled. The interrupt mask register bits enable the appropriate bits when low, and disable them when high. The default configuration is “all interrupts disabled”.

The I/O location for the PCI interrupt routing is 0x28C.

Table 2-47: PCI Interrupt Routing

Bits	Type	Default	Function
7-4	R	--	Reserved
3	RW	1	P1 INTD
2	RW	1	P1 INTC
1	RW	1	P1 INTB
0	RW	1	P1 INTA

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2.13.10 Memory Management of Onboard and Socket Flash

The onboard and socket flash devices are accessed in paged mode. The maximum onboard memory size is 4 MB and the socket size is 512 kB. Both flash types (onboard and socket flash) use the same memory management register to control the page selection.

The page size for the socket flash depends on the setting of the Flash Socket Page register; the Flash access is 8 pages with 64 kB, 16 pages with 32 kB, 32 pages with 16 kB and 64 pages with 8 kB.

The onboard flash page is fixed at 16 kB with 256 pages.

The Memory Management Register selects the individual pages.

If both flash types are active (onboard and socket) the Flash Socket Page register must be set to 16 kB.

The I/O location for memory management is 0x28E.

Table 2-48: Memory Management

Bits	Type	Default	Page 8 kB	Page 16 kB	Page 32 kB	Page 64 kB
7	RW	0	--	A21	--	--
6	RW	0	--	A20	--	--
5	RW	0	A18	A19	--	--
4	RW	0	A17	A18	--	--
3	RW	0	A16	A17	A18	--
2	RW	0	A15	A16	A17	A18
1	RW	0	A14	A15	A16	A17
0	RW	0	A13	A14	A15	A16

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2.13.11 Flash Socket Page

The Flash socket page register is used to select the page size to be addressed. The size can be programmed from 8 kB to 64 kB. The default value is 8 kB which results in the following address window: 0xDE000 - 0xDFFFF.

The onboard flash page size cannot be programmed, the page is set to 16 kB and the memory address starts at 0xCC000 – 0xCFFFF.

The I/O location for the Flash socket page is 0x28F.

Table 2-49: Flash Socket Page

Bits	Type	Default	Function
7-0	RW	3	3 = 16 kB 0xDC000 – 0xDFFFF 2 = 64 kB 0xD0000 – 0xDFFFF 1 = 32 kB 0xD8000 – 0xDFFFF 0 = 8 kB 0xDE000 – 0xDFFFF

2.13.12 LED Control

With the LED control register the LED on the front panel may be switched on and off.

The I/O location of the LED control is 0x340.

Table 2-50: LED Control

Bits	Type	Default	Function
7-0	RW	0	1 = LED on 0 = LED off

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2.13.13 Rear I/O Configuration

The direction (front or rear I/O) of the two Ethernet ports, the COM1 and the COM2 port may be controlled with four general purpose outputs of the PIIX4E chip. The four GPO output signals can be controlled via the GPOREG register located in Function 3 (Power Management) system IO space at address PMBase+34h.

The default configuration is the front I/O interface.

For more information please see the INTEL PIIX4E datasheet.

Table 2-51: Rear I/O Configuration

Bits	Type	Default	Function
GPO27	RW	1	Ethernet 2 interface 0 = rear I/O interface 1 = front I/O interface
GPO28	RW	1	Ethernet 1 interface 0 = rear I/O interface 1 = front I/O interface
GPO29	RW	1	COM2 interface 1 = rear I/O interface 0 = front I/O interface
GPO30	RW	1	COM1 interface 1 = rear I/O interface 0 = front I/O interface

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Chapter 3

Installation

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3. Installation

3.1 Board Installation



Caution!

If your board type is not specifically qualified as hotswap capable, please switch off the CompactPCI system before installing the board in a free CompactPCI slot. Failure to do so could endanger your life/health and may damage your board or system.



Note:

Certain CompactPCI boards require bus master and/or rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure your system is provided with an appropriate free slot to insert the board.



ESD Equipment!

Your CompactPCI board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

Chapters 2 and 4 of this manual describe the hardware and software setup of the CP604-PM controller board, its CPU and the following related devices:

- serial ports
- floppy disk interface
- EIDE device interfaces
- keyboard/mouse interface on the front panel
- VGA
- USB
- Fast Ethernets



PEP Advantage

One or more of the above mentioned mass storage and I/O devices may be connected to your CP604-PM controller board. However, none of these devices have to be installed for the CP604-PM to function, as it is designed to be bootstrapped solely from the FLASH device.

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3.1.1 Placement of the CP604-PM

The CP604-PM is hotswappable, which means it may be installed in and removed from a hotswap compliant backplane whilst the system is powered-up and running. The board may also be used in a standard CompactPCI system without Hotswap support.

To use the CP604-PM as a hotswappable board it must first be ensured that the backplane and system controller are hotswap compliant.

To install the CP604-PM board into a system:

The operator takes the board and inserts it into a peripheral slot, in the course of which:-

- The board enters the card guide.
- Hardware lights up the blue LED.
- Once fully inserted the extractor handles should be closed.
- Hardware switches off the blue LED.
- The front panel fixing bolts should now be secured.

To remove the CP604-PM from the system:

- Loosen the front panel fixing bolts.
- Open the lower extractor handle. This will activate a switch which signals to the board that it is about to be disengaged.
- Wait for the blue LED to light up.
- Using the handles, carefully extract the board from the backplane and remove from the slot.

The *PEP* CompactPCI system configuration is characterized by the fact that its system slot (slot 1) is on the right end of the backplane, thus allowing for physical CPU growth (heat sink, cooling fan etc.) associated with higher performance processors.



Important:

- The CP604-PM will fit into any peripheral slot. Therefore it is important to ensure that it is not inadvertently fitted into the system slot.
- The CP604-PM supports rear I/O on J3 and J5. To utilize this feature the backplane must be configured for rear I/O.

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3.1.2 EIDE Interfaces

The CP604-PM board is provided with two EIDE interfaces. The primary interface utilises a 44-pin connector which may be used to connect either an external or an onboard 2.5" disk drive. The other EIDE interface is a 40-pin connector which is used for the connection of external drives.

The EIDE interfaces each allow installation of up to two devices (one master-slave pair). If installed, the devices are automatically recognized by the BIOS at system "power on".



Important:

Each EIDE interface supports a maximum of two devices connected in the master-slave mode. To configure the first as a master disk and the second as a slave disk please refer to the hard disk manufacturer's documentation.

Hard Disk Installation

To install a hard disk, it is necessary to perform the following operations in the given order:

1. Install the hardware;
2. Initialize the software necessary to run the chosen operating system.



Warning!

The incorrect connection of power or data cables may damage your hard disk unit and/or CP604-PM board.

3.1.3 Keyboard/Mouse Connector

The CP604-PM uses a PC/AT standard keyboard/mouse connection realized as a 6-pin shielded mini-DIN connector. To connect both a mouse and keyboard to your mini-DIN connector, a suitable keyboard/mouse Y-adapter may be used



Warning!

When plugging in your keyboard and mouse, or when plugging anything into a Serial or Com port, make sure that the power is off. Connecting these devices while the power is on, which is known as "hot plugging", may damage your system.

3.2 Software Installation

The installation of the Ethernet and all other onboard peripheral drivers is described in detail in the relevant Driver Kit files.

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Chapter 4

CMOS Setup

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4. CMOS Setup

This chapter describes the Award BIOS Setup program, EliteBIOS, version 4.51PG. The Setup program lets you modify basic system configuration settings.

4.1 Proprietary Notice

Unless otherwise noted, chapter 4 of this manual, which concerns the EliteBIOS setup program, as well as the information herein disclosed are proprietary to AWARD Software International, Inc. Any person or entity to whom this document is furnished or who otherwise has possession thereof, by acceptance agrees that it will not be copied or reproduced in whole or in part, nor used in any manner except to meet the purposes for which it was delivered.

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4.2 Introduction to Setup

This manual describes the Award BIOS Setup program. The Setup program lets you modify basic system configuration settings. The settings are then stored in a dedicated battery-backed memory, called CMOS RAM, that retains the information when the power is turned off.

A special feature of *PEP's* CompactPCI boards is that all Setup information is additionally saved in a non-volatile serial EEPROM. This feature provides the user with enhanced data security in comparison with a standard PC board, because setup data will not be lost should the battery fail.

The Award BIOS in your computer is a customized version of an industry-standard BIOS for IBM PC AT–compatible personal computers. It supports the Intel®x86 and compatible processors. The BIOS provides critical low-level support for the system central processing, memory, and I/O subsystems.

The Award BIOS has been customized by adding important, but nonstandard, features such as virus and password protection, power management, and detailed fine-tuning of the chipset controlling the system.

The rest of this manual is intended to guide you through the process of configuring your system using Setup.

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Starting Setup

The Award BIOS is immediately activated when you first turn on the computer. The BIOS reads system configuration information in CMOS RAM and begins the process of checking out the system and configuring it through the Power-on Self Test (POST).

When these preliminaries are finished, the BIOS seeks an operating system on one of the data storage devices (hard drive, floppy drive, etc.). The BIOS launches the operating system and hands control of system operations to it.

During POST, you can start the Setup program in one of two ways:

- By pressing <Del> immediately after switching the system on, or
- By pressing the <Del> key or by simultaneously pressing <CTRL>, <ALT>, and <ESC> keys when the following message appears briefly at the bottom of the screen during POST:

Press DEL to enter SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the RESET button on the system case. You may also restart by simultaneously pressing <CTRL>, <ALT>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message appears and you are again asked to

Press F1 to continue, DEL to enter SETUP

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Setup Keys

The following table describes how to navigate in Setup using the keyboard.

Table 4-1: Keyboard Commands

Up Arrow	Move to previous item
Down Arrow	Move to next item
Left Arrow	Move to the item to the left
Right Arrow	Move to the item to the right
Esc Key	Main Menu: Quit without saving changes into CMOS RAM. Status Page Setup Menu and Option Page Setup Menu: Exit current page and return to Main Menu
PgUp Key	Increase the numeric value or make changes
PgDn Key	Decrease the numeric value or make changes
+ Key	Increase the numeric value or make changes
- Key	Decrease the numeric value or make changes
F1 Key	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2 Key **Shift-F2**	Change color from total of 16 colors. F2 to select color forward, Shift-F2 to select color backward
F3 Key	Calendar, only for Status Page Setup Menu
F4 Key	Reserved
F5 Key	Restore the previous CMOS value from CMOS, only for Option Page Setup Menu
F6 Key	Load the default CMOS RAM value from BIOS default table, only for Option Page Setup Menu
F7 Key	Load the default
F8 Key	Reserved
F9 Key	Reserved
F10 Key	Save all the CMOS changes, only for Main Menu

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Getting Help

Press F1 and a small help window pops up that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

In Case of Problems

If, after making and saving system changes with Setup, you discover that your computer is no longer able to boot, the Award BIOS supports an override to the CMOS settings that resets your system to its default configuration.

You can invoke this override by immediately pressing <Insert> when you restart your computer. You can restart by either using the ON/OFF switch, the RESET button or by pressing <CTRL>, <ALT> and <Delete> at the same time.

The best advice is to only alter settings that you thoroughly understand. In particular, do not change settings in the Chipset screen without good reason. The Chipset defaults have been carefully chosen by *PEP Modular Computers* for optimum performance and reliability. Even a seemingly small change to the Chipset setup may result in the system becoming unstable.

Setup Variations

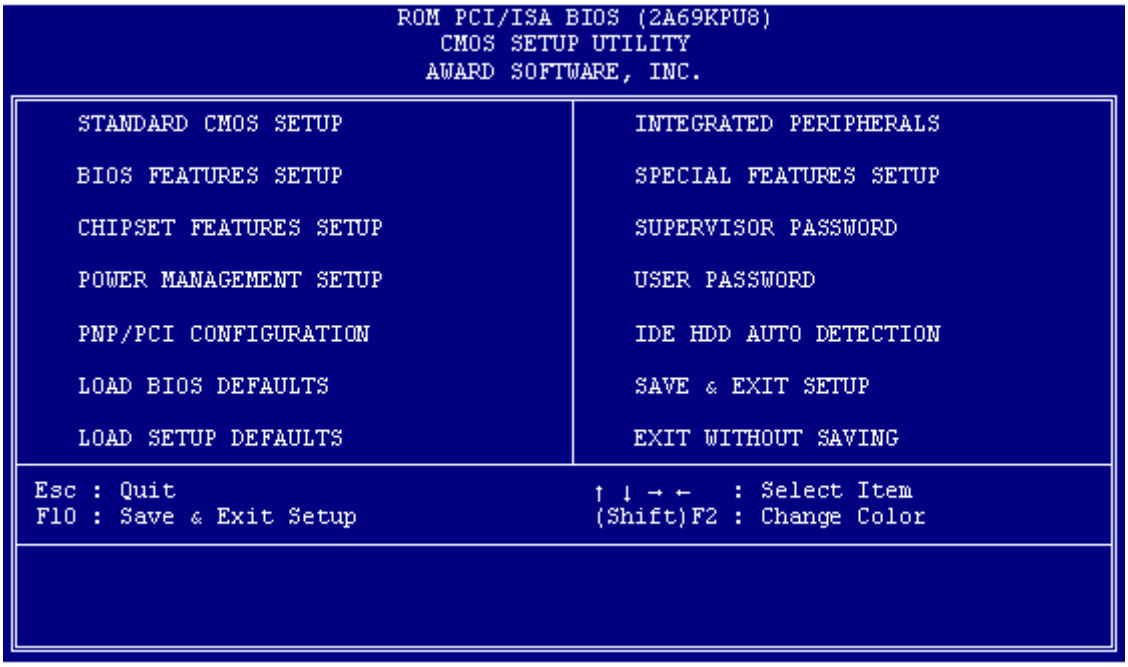
Not all systems have the same Setup. While the basic look and function of the Setup program remains the same for all systems, the appearance of your Setup screens may differ from the screens shown here. Each system design and chipset combination require customized configurations. In addition, the final appearance of the Setup program depends on your system designer. Your system designer may decide that certain items should not be available for user configuration and remove them from the Setup program.

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4.3 Main Setup Menu

When you enter the Award BIOS CMOS Setup Utility, a Main Menu, similar to the one shown below, appears on the screen. The Main Menu allows you to select from several Setup functions and two exit choices. Use the arrow keys to select items and press ↵ to accept and enter the sub-menu.

Figure 4-1: CMOS Setup Utility Main Menu — Screen Display



A brief description of each highlighted selection appears at the bottom of the screen.

Following is a brief summary of each Setup category.

Standard CMOS Setup

Options in the original PC AT-compatible BIOS.

BIOS Features Setup

Award enhanced BIOS options.

Chipset Features Setup

Options specific to your system chipset.

Power Management Setup

Advanced Power Management (APM) options.

PNP/PCI Configuration

PlugandPlay standard and PCI Local Bus configuration options.

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Integrated Peripherals

I/O subsystems, that depend on the integrated peripherals controller in your system.

Special Features Setup

Items related to features of this board, which are not common to standard motherboard designs.

Supervisor/User Password

Change, set, or disable a password. In BIOS versions that allow separate user and supervisor passwords, only the supervisor password permits access to Setup. The user password generally allows only power-on access.

EIDE HDD Auto Detection

Automatically detect and configure EIDE hard disk parameters.

Load BIOS Defaults

BIOS defaults are factory settings for the most stable, minimal-performance system operations.

Load Setup Defaults

Setup defaults are factory settings for optimal-performance system operations.

Save & Exit Setup

Save settings in non-volatile CMOS RAM and exit Setup.

Exit Without Save

Abandon all changes and exit Setup.

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4.4 Standard CMOS Setup

In the Standard CMOS menu you can set the system clock and calendar, record disk drive parameters and the video subsystem type, and select the type of errors that stop the BIOS POST.

Date

The BIOS determines the day of the week from the other date information. This field is for information only.

Press the → or ← key to move to the desired field (date, month, year). Press the “PgUp” or “PgDn” key to increment the setting, or type the desired value into the field.

Time

The time format is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Press the → or ← key to move to the desired field. Press the PgUp or PgDn key to increment the setting, or type the desired value into the field.

Hard Disks

The BIOS supports up to four EIDE drives. This section does not show information relating to other EIDE devices, such as a CD-ROM drive, or about other hard drive types, such as SCSI drives.



Important:

We recommend that you select the AUTO type for all drives.

Figure 4-2: Standard CMOS Setup Menu — Screen Display

```
                    ROM PCI/ISA BIOS (2A69KPU8)
                      STANDARD CMOS SETUP
                      AWARD SOFTWARE, INC.

   Date (mm:dd:yy) : Thu, Jan 11 2001
   Time (hh:mm:ss) : 15 : 52 : 47

   HARD DISKS         TYPE    SIZE   CYLS HEAD PRECOMP LANDZ SECTOR  MODE

   Primary Master   :    0       0      0    0       0     0       0 NORMAL
   Primary Slave    :    0       0      0    0       0     0       0 NORMAL
   Secondary Master :    0       0      0    0       0     0       0 NORMAL
   Secondary Slave  :    0       0      0    0       0     0       0 NORMAL

   Drive A : None
   Drive B : None

   Video   : EGA/VGA
   Halt On : All Errors

ESC : Quit              ↑ ↓ → ←   : Select Item       PU/PD/+/- : Modify
F1  : Help              (Shift)F2 : Change Color
```


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The BIOS has the capability to automatically detect the specifications and optimal operating mode of almost all EIDE hard drives. When you select type AUTO for a hard drive, the BIOS detects its specifications during POST, every time the system boots.

If you do not want to select drive type AUTO, other methods of selecting the drive type are available as follows:

1. Match the specifications of your installed EIDE hard drive(s) with the pre-programmed values for drive types 1 through 45.
2. Select USER and enter values into each drive parameter field.
3. Use the EIDE HDD AUTO DECTECTION function in “Setup”.

The following table provides a brief explanation of drive specifications:

Table 4-2: Description of Drive Specifications

Spec.		Description
Type		The BIOS contains a table of pre-defined drive types. Each defined drive type has a specified number of cylinders, number of heads, write pre-compensation factor, landing zone, and number of sectors. Drives whose specifications do not accommodate any pre-defined type are classified as type USER.
Size		Disk drive capacity (approximate). Note that this size is usually slightly greater than the size of a formatted disk given by a disk-checking program.
Cyls.		Number of cylinders
Head		Number of heads
Precomp.		Write pre-compensation cylinder
Landz		Landing zone
Sector		Number of sectors
Mode	Auto	Auto: The BIOS automatically determines the optimal mode.
	Normal	The maximum number of cylinders, heads, and sectors supported are 1024, 16, and 63 respectively.
	Large	For drives that do not support LBA and have more than 1024 cylinders.
	LBA	During drive accesses, the EIDE controller transforms the data address described by sector, head, and cylinder number into a physical block address, significantly improving data transfer rates. For drives with greater than 1024 cylinders.

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Drive A / Drive B

Selects the correct specifications for the diskette drive(s) installed in the computer.

Table 4-3: Diskette Drives

None	No diskette drive installed
360K, 5.25 in	5-1/4 inch PC-type standard drive; 360 kilobyte capacity
1.2M, 5.25 in	5-1/4 inch AT-type high-density drive; 1.2 megabyte capacity
720K, 3.5 in	3-1/2 inch double-sided drive; 720 kilobyte capacity
1.44M, 3.5 in	3-1/2 inch double-sided drive; 1.44 megabyte capacity
2.88M, 3.5 in	3-1/2 inch double-sided drive; 2.88 megabyte capacity

Video

Selects the type of primary video subsystem in your computer. The BIOS usually detects the correct video type automatically. The BIOS supports a secondary video subsystem, however, this is not selected in Setup.

Table 4-4: Primary Video Subsystem Selection

EGA/VGA	Enhanced Graphics Adapter/Video Graphics Array. For EGA, VGA, SEGA, SVGA or PGA monitor adapters.
CGA 40	Color Graphics Adapter, power-up in 40 column mode
CGA 80	Color Graphics Adapter, power-up in 80 column mode
MONO	Monochrome adapter, includes high resolution monochrome adapters

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Halt On

During the power-on self-test (POST), the computer stops if the BIOS detects a hardware error. You can program the BIOS to ignore certain errors during POST and continue the boot-up process. The possible selections are listed in the following table.

Table 4-5: POST Specific Commands

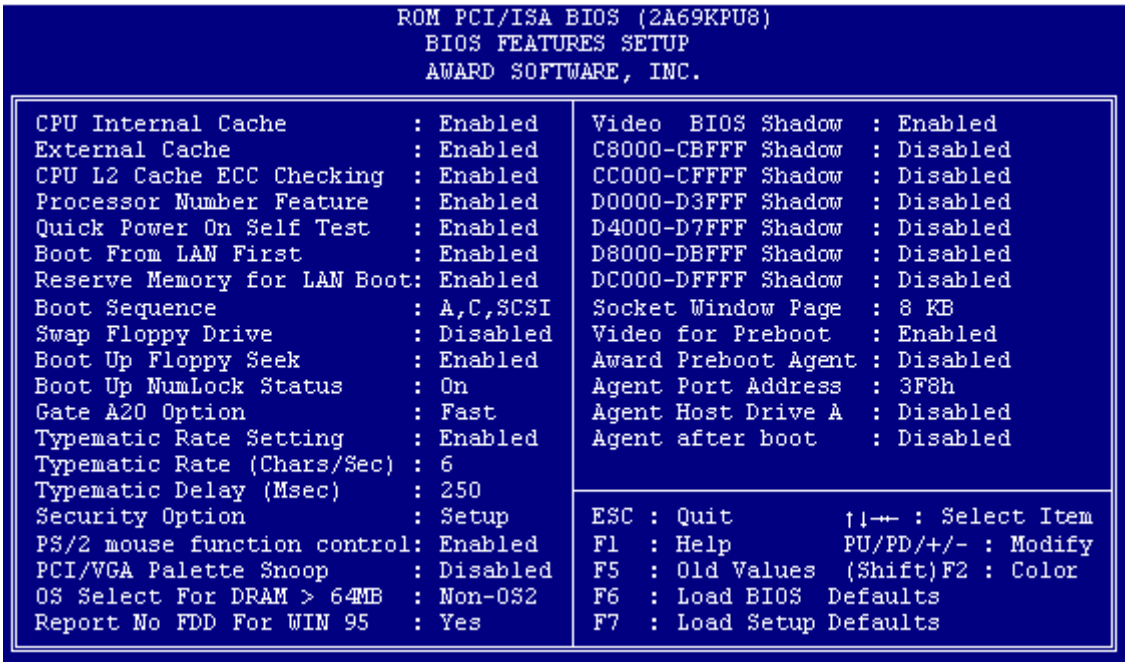
Command	POST Action
No errors	POST does not stop for any errors.
All errors	If the BIOS detects any non-fatal error, POST stops and prompts you to take corrective action.
All, But Keyboard	POST does not stop for a keyboard error, but stops for all other errors.
All, But Diskette	POST does not stop for diskette drive errors, but stops for all other errors.
All, But Disk/Key	POST does not stop for a keyboard or disk error, but stops for all other errors.

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4.5 BIOS Features Setup

This screen contains industry-standard options additional to the core PC AT BIOS. This section describes all fields presented by Award Software in this screen. The example screen below may vary somewhat from the one in your Setup program; your system board designer may omit or modify some fields

Figure 4-3: BIOS Features Setup — Screen Display



CPU Internal Cache / External Cache

Cache memory is additional memory that is much faster than conventional DRAM (system memory). CPU's from 486-type on up contain internal cache memory, and most, but not all, modern PC's have additional (external) cache memory. When the CPU requests data, the system transfers the requested data from the main DRAM into cache memory, for even faster access by the CPU.

The External Cache field may not appear if your system does not have external cache memory.

CPU L2 Cache ECC Checking

When you select *Enabled*, memory checking is enabled when the external cache contains ECC SRAM's.

Quick Power-on Self Test

Select Enabled to reduce the amount of time required to run the power-on self-test (POST). A quick POST skips certain steps. We recommend that you normally disable quick POST. Better to find a problem during POST than lose data during your work.

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Boot from LAN first

This BIOS includes a feature for booting from LAN using the BOOTP / DHCP protocol.

Lan-Boot is based on Etherboot-4.5.6, a LAN-Boot implementation, which is covered by the GNU public licence. It has been adopted for use with *PEP* CompactPCI Hardware. As required by the GNU public licence, the complete sourcecode is included on the tool-kit floppy-disk.

Using this option requires an understanding of the BOOTP and/or DHCP mechanisms and knowledge in configuring a BOOTP or DHCP server. These topics are not described within this manual.

For further information please unpack the file PEP-etherboot-4.5.6.tar.gz in the directory TOOLS\ETHERBOOT in the boards toolkit or download the Etherboot from www.sourceforge.net

Reserve Memory for LAN Boot

If “Reserve Memory for LAN Boot” is set to enable, the LAN Boot reserves for itself 32 KB memory from the 640 MB Base Memory. It does this to avoid compatibility problems with other drivers, which simply “grab” memory. An obvious disadvantage is that main memory is reduced by 32 KB. When “Reserve Memory for LAN Boot” is set to disable, it uses memory without reserving it in any way. This is the original setup of the Etherboot. When, for example, DiskOnChip (and possibly also other drivers) do exactly the same, it will unfortunately result in a crash. In conclusion, it should only be set to disable when DOS booting is required and 640 KB Main Memory is needed. Otherwise it should be set to enable.

Boot Sequence

The original IBM PC’s loaded the operating system from drive A (floppy disk), so IBM PC-compatible systems are designed to search for an operating system first on drive A, and then on drive C (hard disk). However, modern computers usually load the operating system from the hard drive, and may even load it from a CD-ROM drive. The BIOS now offers 10 different boot sequence options of three drives each. In addition to the traditional drives A and C, options include EIDE hard drives D, E and F; plus an SCSI hard drive and a CD -ROM drive.

Swap Floppy Drive

This field is effective only in systems with two floppy drives. Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B.

Boot Up Floppy Seek

When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360-KB floppy drives have 40 tracks; drives with 720 KB, 1.2 MB, and 1.44 MB capacity all have 80 tracks. Because very few modern PC’s have 40-track floppy drives, we recommend that you set this field to Disabled to save time.

Boot Up Numlock Status

Toggle between On or Off to control the state of the NumLock key when the system boots. When toggled On, the numeric keypad generates numbers instead of controlling cursor operations.

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Gate A20 Option

Gate A20 refers to the way the system addresses memory above 1 MB (extended memory). When set to Fast, the system chipset controls Gate A20. When set to Normal, a pin in the keyboard controller controls Gate A20. Setting Gate A20 to Fast improves system speed, particularly with OS/2 and Windows.

Typematic Rate Setting

When Disabled, the following two items (Typematic Rate and Typematic Delay) are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system.

When Enabled, you can select a typematic rate and typematic delay.

Typematic Rate (Chars/Sec)

When the typematic rate setting is enabled, you can select a typematic rate (the rate at which a character repeats when you hold down a key) of 6, 8, 10, 12, 15, 20, 24 or 30 characters per second.

Typematic Delay (ms)

When the typematic rate setting is enabled, you can select a typematic delay (the delay before key strokes begin to repeat) of 250, 500, 750 or 1000 milliseconds.

Security Option

If you have set a password, select whether the password is required every time the System boots, or only when you enter Setup.

PS/2 Mouse Function Control

If your system has a PS/2 mouse port and you instal a serial pointing device, select *Disabled*.

PCI/VGA Palette Snoop

Your BIOS Setup may not contain this field. If the field is present, leave at Disabled.

OS Select for DRAM>64MB

Select OS2 only if you are running the OS/2 operating system with greater than 64 MB of RAM in your system.

Report No FDD for WIN 95

Select *Yes* to release IRQ6 when the system contains no floppy drive, for compatibility with Windows 95 logo certification. In the **Integrated Peripherals** screen, select *Disabled* for the **Onboard FDC Controller** field.

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Shadow

Software that resides in a read-only memory (ROM) chip on a device is called *firmware*. The Award BIOS permits *shadowing* of firmware such as the system BIOS, video BIOS, and similar operating instructions that come with some expansion peripherals, such as, for example, a SCSI adaptor.

Shadowing copies firmware from ROM into system RAM, where the CPU can read it through the 16-bit or 32-bit DRAM bus. Firmware not shadowed must be read by the system through the 8-bit X-bus. Shadowing improves the performance of the system BIOS and similar ROM firmware for expansion peripherals, but it also reduces the amount of high memory (640 KB to 1 MB) available for loading device drivers, etc.

Enable shadowing into each section of memory separately. Many system designers hardwire shadowing of the system BIOS and eliminate a System BIOS Shadow option.

Video BIOS shadows into memory area C0000-C7FFF. The remaining areas shown on the BIOS Features Setup screen may be occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct area of RAM.

Socket Window Page

The CP604-PM is equipped with a 32-pin socket to take additional Flash-ROM. This Flash-ROM may be addressed by a paging mechanism. The size of one Flash page can be set at this point as follows:

Table 4-6: Setting Flash Page Size

Page Size	Address Space used by Socket Flash EPROM
8 KB	0xDE000 - 0xDFFFF
16 KB	0xDC000 - 0xDFFFF
32 KB	0xD8000 - 0xDFFFF
64 KB	0xD0000 - 0xDFFFF

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Award Preboot Agent

The Award Preboot Agent is a BIOS extension which redirects console input/output to a serial port with the following capabilities:-

- Supports direct RS-232C serial (null modem) connection
- Receives keystrokes from the Manager
- Sends 16 color text-mode video to the Manager (before and after OS load)
- Enables video snooping at OS load for full run-time video output to Manager
- Recognizes a subset of VT100/320 escape sequences and control codes
- Floppy Disk Redirection
- POST code viewing, with descriptions
- Full color video output to Manager
- Supports DOS diagnostic and flash utilities

To be able to take full advantage of the Award Preboot Agent capabilities, the Software Award Preboot Manager Version 3.02 or later is required.

If only the console redirection is required, any other terminal emulation SW may be used (for example: Windows Hyper Terminal)

Agent Port Address

Select the UART address to be used by Agent software.

The recommended address is 3F8h (equivalent to COM1) or 2F8h (equivalent to COM2 under DOS). It is inadvisable to select "auto".

If no connection is established, check that you have already configured the UART in the INTEGRATED PERIPHERALS setup page. If your system is equipped with rear I/O please ensure also that the front or rear configuration in SPECIAL FEATURES SETUP is correct and that the appropriate port is connected.

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Agent Host Drive A

When the administrative host is using the Preboot Manager application, the Agent can boot and run applications from host floppy drive A. INT13 calls intended for the Agent floppy drive A are redirected by the Agent extension to the host floppy drive A. All other INT13 calls are passed along to the original interrupt handler. The Manager application can receive the Agent drive A interrupt and interpret the commands. It then calls its own INT13 handler to read or write the requested sectors to host drive A. Both Manager and Agent serial version software use Xmodem protocol for all transfers.

The floppy drive redirection feature permits support personnel to remotely administer two vital tools on the Agent system:

- PC DIAG diagnostics package from Unicore Software (available through Award Software as part of the Manager application).
- AWDFLASH BIOS flash upgrade utility. (in batch mode, this means giving the parameters at the command line; e.g. awdflash <filename> /Sn/Py, DO NOT USE INTERACTIVE MODE!!!)

Select Enabled to enable this feature, default is Disabled.

Agent after Boot

In the "standard" Agent product, Agent software continues to function after the operating system loads. However, some non-DOS operating systems are not compatible with the Agent BIOS extension, so the Agent should disable when the OS loads. Selecting Disabled turns off the Agent software just as the BIOS transfers control to the operating system. Default is Disabled.

Award Baud Rate

Selects the speed at which the UART is to operate. Default is 19,200.

Null-Modem Cable Pinout

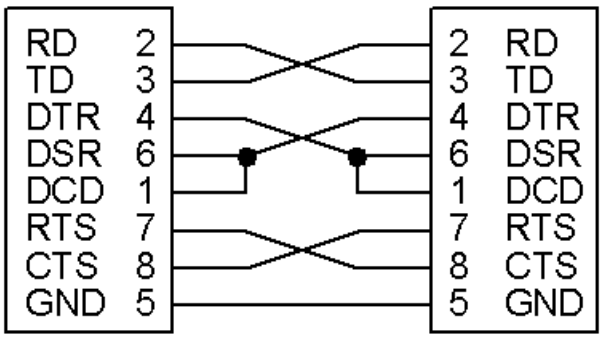


Figure 4-4: Null-Modem Cable Connection

A null-modem cable is a serial cable designed to connect two PC's. Each end has a 9-pin, female RS-232C connector. If you are creating your own 9-pin cable, connect the two ends through the cable as shown here.

Further Information

For further information please refer to the manual for the Award Preboot Agent™ 2.0 which accompanies the manual for the Award Preboot Manager™ 2.0.

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4.6 Chipset Features Setup

This section describes features of the PIIX4 PCIset. If your system contains a different chipset, this section will bear little resemblance to what you see on your screen..

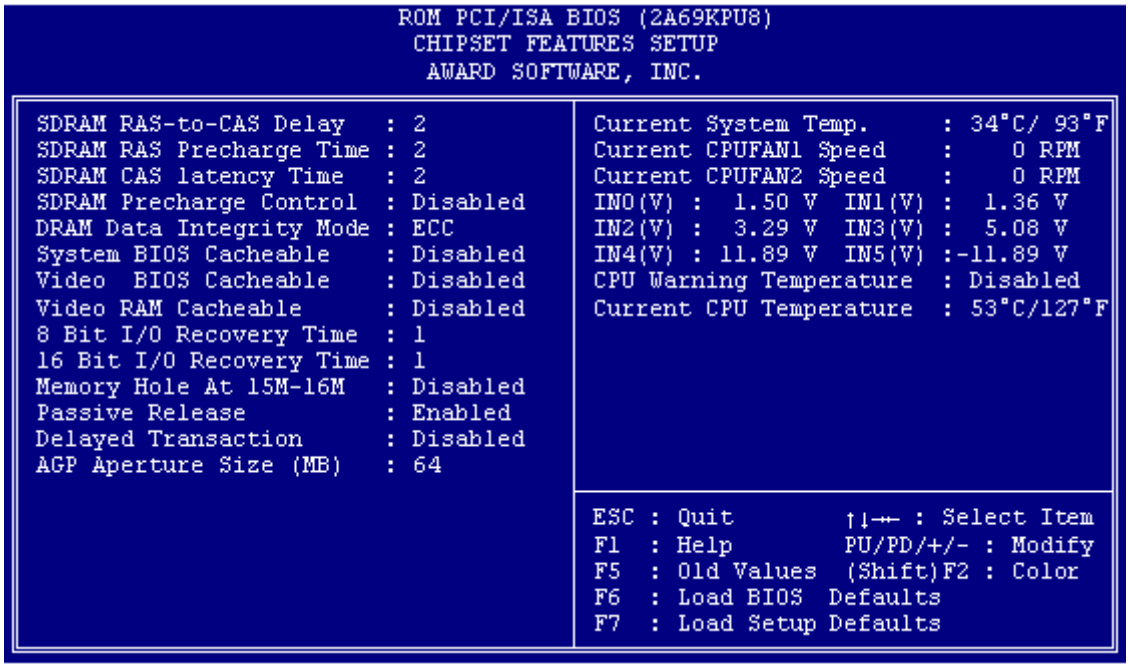
PEP Advantage

This section describes all the fields presented on this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Advanced Options

The parameters in this screen are for system designers, service personnel, and technically competent users only. Do not reset these values unless you understand the consequences of your changes.

Figure 4-5: Chipset Features Setup — Screen Display



SDRAM RAS To CAS Delay

Select the RAS to CAS delay time. See Refresh Cycle Time for information about the Auto Configuration of this value.

SDRAM RAS Precharge Time

The precharge time is the number of cycles it takes for the RAS to accumulate its charge before DRAM refresh. If insufficient time is allowed, refresh may be incomplete and the DRAM may fail to retain data.

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SDRAM CAS Latency Time

When synchronous DRAM is installed, you can control the number of CLK's between the SDRAM's sample of a read command and the time when the controller samples read data from the SDRAM's. Do not reset this field from the default value specified by the system designer.

SDRAM Precharge Control

When *Enabled*, all CPU cycles to SDRAM result in an All Banks Precharge Command on the SDRAM interface.

DRAM Data Integrity Mode

Select *Non-ECC* or *ECC* (error-correcting code), according to the type of installed DRAM. The onboard memory supports ECC. For this reason the default value is ECC.

System BIOS Cacheable

Selecting *Enabled* allows caching of the system BIOS ROM at 0xF0000 to 0xFFFFF, resulting in better system performance. However, if any program writes to this memory area, a memory access error may result.

Video BIOS Cacheable

Selecting *Enabled* allows caching of the video BIOS ROM at 0xC0000 to 0xC7FFF, resulting in better video performance. However, if any program writes to this memory area, a memory access error may result.

Video RAM Cacheable

Selecting *Enabled* allows caching of the video memory (RAM) at 0xA0000 to 0xAFFFF, resulting in better video performance. However, if any program writes to this memory area, a memory access error may result.

8/16-bit I/O Recovery Time

The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is so much faster than the ISA bus.

These two fields let you add recovery time (in bus clock cycles) for 16-bit and 8-bit I/O.

Memory Hole at 15M-16M

You can reserve this area of system memory for ISA adaptor ROM. When this area is reserved, it cannot be cached. The user information for peripherals that need to use this area of system memory usually discusses their memory requirements.

Passive Release

When *Enabled*, CPU to PCI bus accesses are allowed during passive release. Otherwise, the arbiter only accepts another PCI master access to local DRAM.

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Delayed Transaction

The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select *Enabled* to support compliance with PCI specification version 2.1.

AGP Aperture Size (MB)

Select the size of the Accelerated Graphics Port (AGP) aperture. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without any translation. See http://www.agpforum.org for AGP information.

CPU Warning Temperature

Select the combination of lower and upper limits for CPU temperature, if your computer contains an environmental monitoring system. If the CPU temperature extends beyond either limit, any warning mechanism programmed into your application is activated.

Current CPU Temperature

This field displays the *current* CPU temperature, if your computer contains an environmental monitoring system.

Current CPU Fan 1

Monitors the onboard Fan mounted on the CPU heat sink, if available.

Current CPU Fan 2

Monitors the Fan signal routed to the rear I/O connector.

Voltage Monitor

Displays all onboard voltages for diagnostic purposes.

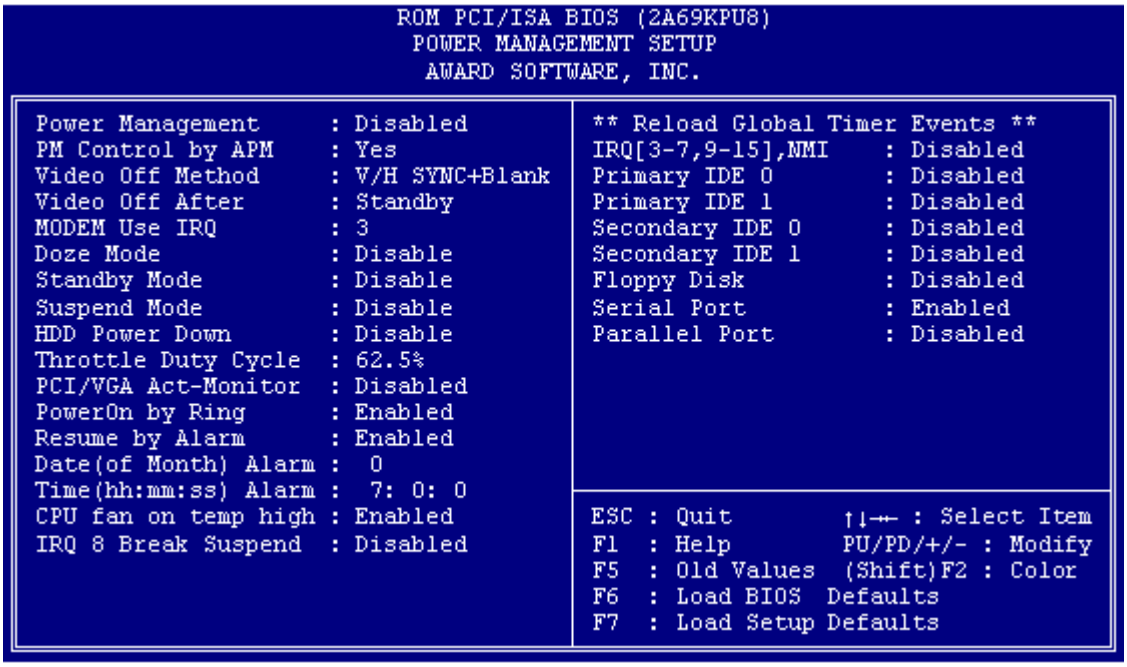
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4.7 Power Management

PEP Advantage

This section describes all fields presented on this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Figure 4-6: Power Management Setup — Screen Display



ACPI Function (optional)

Select *Enabled* only if your computer's operating system supports the Advanced Configuration and Power Interface (ACPI) specification. Currently, Windows 98®, Windows 2000® and Windows NT® support ACPI.

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Power Management

This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. See the section *PM Timers* for a brief description of each mode.

The following table describes each power management mode:

Table 4-7: Power Management Modes

Mode	Description
Max. Saving	Maximum power savings. Inactivity period is 1 minute in each mode.
User Defined	Sets each mode individually. Select time-out periods in the *PM Timers* section, which follows.
Min. Saving	Minimum power savings. Inactivity period is one hour in each mode (except the hard drive).

PM Control by APM

If Advanced Power Management (APM) is installed in your system, selecting *Yes* gives improved power savings.

Video-Off Method

Determines the manner in which the monitor is blanked.

Table 4-8: Video-Off Commands

V/H SYNC+Blank	System switches off vertical and horizontal synchronization ports and writes blanks to the video buffer.
DPMS Support	Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsystem to select video power management values.
Blank Screen	System writes blanks only to the video buffer.

Video-Off Option

This item determines the power management modes the monitor will enter before entering the Off-state as defined by the Video Off Method below. The Video Off Option moves from the low (doze) to the medium (standby) to high (suspend) power saving modes.

Modem Use IRQ

Name the interrupt request (IRQ) line assigned to the modem (if any) on your system. Activity by the selected IRQ always awakens the system.

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4.8 PM Timers

The following modes are Green PC power saving functions. They are user-configurable only during User Defined Power Management mode.

Doze Mode

After the selected period of system inactivity (1 minute to 1 hour), the CPU clock runs at a slower speed while all other devices still operate at full speed.

Stand-By Mode

After the selected period of system inactivity (1 minute to 1 hour), the fixed disk drive and the video shut down while all other devices still operate at full speed.

Suspend Mode

After the selected period of system inactivity (1 minute to 1 hour), all devices except the CPU shut down.

HDD Power Down

After the selected period of drive inactivity (1 to 15 minutes), the hard disk drive powers down while all other devices remain active.

Throttle Duty Cycle

When the system enters Doze mode, the CPU clock runs only part of the time. You may select the percentage of the time that the clock runs.

Soft-Off by PWR-BTTN

When you select *Instant Off* or *Delay 4 Sec.*, turning the system off with the on/off button places the system in a very low power usage state, either immediately or after 4 seconds, with only enough circuitry receiving power to detect power button activity or Resume by Ring activity.

Power-on by Ring

When *Enabled*, an input signal on the serial Ring Indicator (RI) line (in other words, an incoming call on the modem) awakens the system from a soft off state.

Resume by Alarm

When *Enabled*, you can set the date and time at which the RTC (real-time clock) alarm awakens the system from suspend mode.

Date (of Month) Alarm

Select a date in the month when you want the alarm to go off.

Time (hh:mm:ss) Alarm

Set the time at which you want the alarm to go off.

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IRQ8 Break (Event From) Suspend

You can select *Enabled* or *Disabled* for monitoring of IRQ8 (the Real Time Clock) so that it does not awaken the system from Suspend mode.

Reload Global Timer Events

When Enabled, an event occurring on each of the devices listed below restarts the global timer for Standby mode:

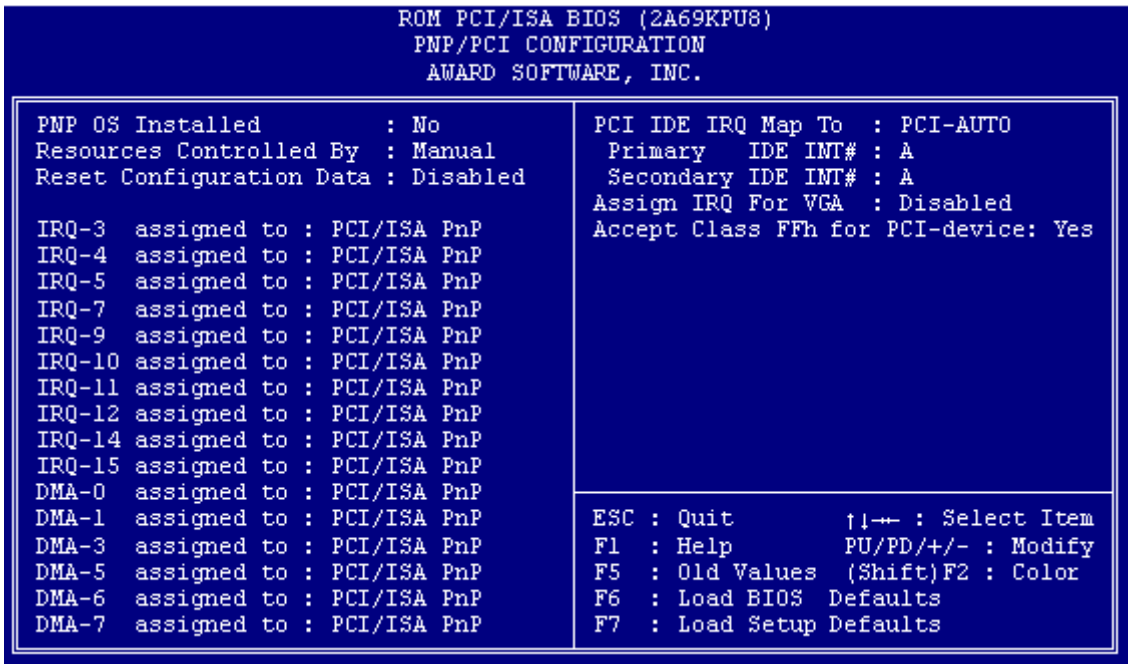
- IRQ§-7, 9-15, NM1,
- Primary EIDE 0,
- Primary EIDE 1,
- Secondary EIDE 0,
- Secondary EIDE 1,
- Floppy Disk,
- Serial Port,
- Parallel Port, and
- IRQ9 (IRQ2 Redir).

4.9 PNP/PCI Configuration

PEP Advantage

This section describes all the fields presented by this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Figure 4-7: PNP/PCI Configuration — Screen Display



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PNP OS Installed

Select “Yes” if the system operating environment is PlugandPlay aware (e.g. Win 95).

Resources Controlled by

The Award PlugandPlay BIOS can automatically configure all the boot and PlugandPlay-compatible devices. If you select *Auto*, all the interrupt request (IRQ) and DMA assignment fields disappear, as the BIOS automatically assigns them.

Reset Configuration Data

Normally this field is left *Disabled*. Select *Enabled* to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system re-configuration has caused such a serious conflict that the operating system cannot boot.

IRQ *n* Assigned to

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt.

Legacy ISA	Devices compliant with the original PC AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).
PCI/ISA PnP	Devices compliant with the PlugandPlay standard, whether designed for PCI or ISA bus architecture.

DMA *n* Assigned to

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt.

Legacy ISA	Devices compliant with the original PC AT bus specification, requiring a specific DMA channel
PCI/ISA PnP	Devices compliant with the PlugandPlay standard, whether designed for PCI or ISA bus architecture.

PCI EIDE IRQ Map to

This field lets you select PCI EIDE IRQ mapping or PC AT (ISA) interrupts. If your system does not have one or two PCI EIDE connectors on the system board, select values according to the type of EIDE interface(s) installed in your system (PCI or ISA). Standard ISA interrupts for EIDE channels are IRQ14 for primary and IRQ15 for secondary.

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Primary/Secondary EIDE INT#

Each PCI peripheral connection is capable of activating up to four interrupts: *INT# A*, *INT# B*, *INT# C* and *INT# D*. By default, a PCI connection is assigned *INT# A*. Assigning *INT# B* has no meaning unless the peripheral device requires two interrupt services rather than just one. Because the PCI EIDE interface in the chipset has two channels, it requires two interrupt services. The primary and secondary EIDE INT# fields default to values appropriate for two PCI EIDE channels, with the primary PCI EIDE channel having a lower interrupt than the secondary.

Accept Class FFh for PCI-device

Some PCI boards use the class code 0FFh. Boards with class code FF are distributed by some vendors in the knowledge that there will be different handling of such devices. The PCI standard does not define configuration rules for class code FF.

To make it transparent to the user that such a board has been identified in the system, the BIOS will display the text "Class-Code FF Device" highlighted and blinking in the PCI device list, which is displayed on system startup before booting.

By setting this field to “No”, these non-standard boards will be ignored. By setting this field to “Yes”, these non-standard boards will also be configured by the BIOS and made operable.

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4.10 Integrated Peripherals



Important:

This section describes all the fields presented by Award Software in this screen display. Please note that your system board designer may omit or modify some fields.

Figure 4-8: Integrated Peripherals — Screen Display

```
                    ROM PCI/ISA BIOS (2A69KPU8)
                     INTEGRATED PERIPHERALS
                      AWARD SOFTWARE, INC.

IDE HDD Block Mode       : Enabled      Onboard FDC Controller   : Enabled
IDE 32-bit Transfer Mode : Disabled     Onboard Serial Port 1    : 3F8/IRQ4
PCI IDE 2nd Channel :      Enabled      Onboard Serial Port 2    : 2F8/IRQ3
On-Chip Primary   PCI IDE: Enabled      Onboard Serial Port 3    : 3E8/IRQ5
IDE Primary Master PIO   : Auto         Onboard Serial Port 4    : 2E8/IRQ7
IDE Primary Slave  PIO   : Auto         Onboard Parallel Port    : Disabled
IDE Primary Master UDMA  : Auto
IDE Primary Slave  UDMA  : Auto
On-Chip Secondary PCI IDE: Enabled
IDE Secondary Master PIO : Auto
IDE Secondary Slave  PIO : Auto
IDE Secondary Master UDMA: Auto
IDE Secondary Slave  UDMA: Auto

USB Keyboard Support     : Disabled
Init Display First       : PCI Slot     ESC : Quit        ↑↓→← : Select Item
Watchdog Timer           : NMI          F1  : Help        PU/PD/+/- : Modify
WDT Active for Booting   : Enabled      F5  : Old Values  (Shift)F2 : Color
WDT Active Time          : 125 ms       F6  : Load BIOS  Defaults
                                        F7  : Load Setup Defaults
```

PCI IDE 2nd Channel

Used to enable the 2nd PCI EIDE interface

IDE HDD Block Mode

Select *Enabled* only if your hard drives support block mode.

IDE 32-bit Transfer Mode

Enables or disables 32-bit Data transfers.

On-Chip PCI IDE (Primary/Secondary)

The Intel® 82C440BX chipset contains a PCI EIDE interface with support for two EIDE channels. Select *Enabled* to activate the primary and/or secondary EIDE interface. Select *Disabled* to deactivate this interface if you instal a primary and/or secondary add-in EIDE interface.

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IDE PIO Modes (Primary/Secondary Master/Slave)

The four EIDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of up to four EIDE devices that the internal PCI EIDE interface supports. Modes 0 through 4 provide successively increased performance. In *Auto* mode, the system automatically determines the best mode for each device.

IDE Primary/Secondary Master/Slave UDMA

UDMA (Ultra DMA) is a DMA data transfer protocol that utilizes ATA commands and the ATA bus to allow DMA commands to transfer data at a maximum burst rate of 33 MB/s. When you select *Auto* in the four EIDE UDMA fields (for each of up to four EIDE devices that the internal PCI EIDE interface supports), the system automatically determines the optimal data transfer rate for each EIDE device.

USB Keyboard Support

Select *Enabled* if your system contains a Universal Serial Bus (USB) controller and you have a USB keyboard.

Init Display First

Initialize the AGP video display before initializing any other display device on the system. Thus the AGP display becomes the primary display.

Watchdog Timer

When enabled, the Watchdog Timer may be used to select the watchdog routing to NMI, IRQ5 or Reset.

WDT Active for Booting

Select *Enable* if the watchdog timer requires to be started before the operating system is booted from the BIOS.

WDT Active Time

Select the time after which the action selected occurs, if the watchdog timer is not retriggered.

Onboard FDC Controller

Select *Enabled* if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install an add-on FDC or the system has no floppy drive, select *Disabled* in this field.

Onboard Serial Ports: 1 to 4

Selects a logical COM port address and corresponding interrupt for the four serial ports.

Onboard Parallel Port

Select a logical LPT port address and corresponding interrupt for the physical parallel port.

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Parallel Port Mode

Select an operating mode for the onboard parallel port. Select *Normal* unless you are certain that both your hardware and software support one of the other available modes.

ECP Mode Use DMA

Select a DMA channel for the parallel port for use during ECP mode.

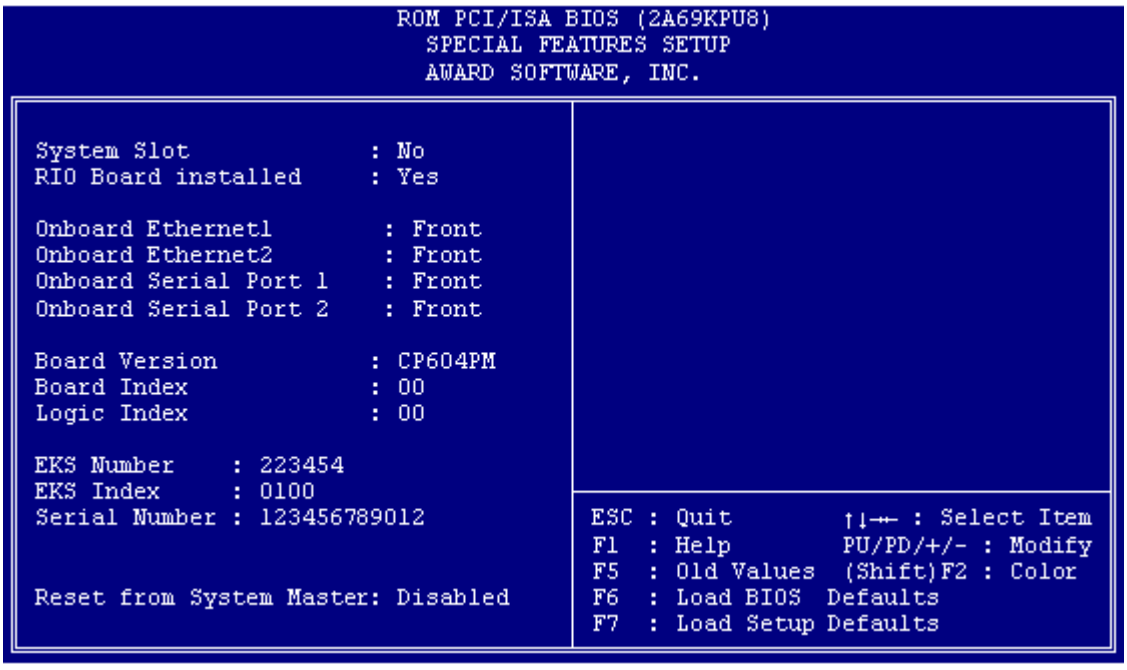
4.11 Special Features Setup



Important:

This section describes all the fields presented by Award Software in this screen display. Your system board designer may omit or modify some fields.

Figure 4-9: Special Features Setup — Screen Display



System Slot

This is a display only field. Yes indicates that this CPU is the system controller configuring the backplane and handling all interrupts relating to the backplane. No indicates that this CPU is a slave CPU.

RIO Board Installed

This is a display only field, which shows, if a RIO board is installed in the system

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Onboard Ethernet1/2, Serial Port 1/2

This item allows EtherNet1/2 and Serial Port1/2 to be configured, wether they should be connected physically to the front panel (Front) or to the Rear IO-Connector (BACK)

EKS Number, EKS Index, Serial Number :

This is a display only field, which shows PEP internal information about the board. EKS-Number and EKS-Index inform about production number and version.

The serial number is unique to each board produced by PEP. It could be used also by the customer to identify specific boards.

Board Version

This is a display only field, which reflects the value of an onboard register. This must always correspond with the CPU on which the BIOS is installed.

Board Index

This is a display only field, which reflects the value of an onboard register. It shows the index of the hardware.

Logic Index

This is a display only field, which reflects the value of an onboard register. It shows the index of the onboard logic. When the Board Index is 00 this item is not displayed.

Reset from System Master

Enabled (default):

When the reset button on the system master frontpanel (which may be, for example, a CP604) is pressed the CP604-PM board will also perform a Hardware Reset.

Disabled:

The reset signal generated by the system master is ignored by the CP604-PM.

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4.12 Password Setting

When you select this function, the following message appears at the center of the screen:

`Enter password:`

Type the password, up to eight characters in length, and press "↵". Typing a password clears any previously entered password from the CMOS memory.

After having pressed "↵" the message changes to:

`Confirm password:`

Type the password again and press "↵". To abort the process at any time, press "Esc".

In the "Security Option" item in the "BIOS Features Setup" screen, select `System` or `Setup`:

Table 4-9: Security Options

System	Enter a password each time the system boots and whenever you enter Setup.
Setup	Enter a password whenever you enter Setup.



Important:

To clear the password, simply press "↵" when asked to enter a password. Then the password function is disabled.

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4.13 POST Messages

During the Power-on Self Test (POST), the BIOS displays a message whenever it detects a correctable error. Any error message is followed by this prompt:

`Press “F1” to continue, “Ctrl-Alt-Esc” or “Del” to enter setup.`

Following is a list of POST error messages for both the ISA and the EISA BIOS.

CMOS Battery Has Failed

The CMOS battery is no longer functional. It should be replaced.

CMOS Checksum Error

Checksum of CMOS is incorrect. This can indicate that the CMOS has become corrupted. This error may have been caused by a weak battery. Check the battery and replace it, if necessary.

Disk Boot Failure, Insert System Disk and Press Enter

No boot device was found. This could mean that either a boot drive was not detected or that the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

Diskette Drives or Types Mismatch Error - Run Setup

Type of floppy-disk drive installed in the system is different from the CMOS definition. Run “Setup” to reconfigure the drive type correctly.

Display Switch is Set Incorrectly

Display switch on the motherboard can be set to either monochrome or color. This error message indicates that the switch has a setting other than that indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the video selection.

Display Type Has Changed Since Last Boot

Since the last powering-down of the system, the display adapter has been changed. You must configure the system for the new display type.

EISA Configuration Checksum Error - Please Run EISA Configuration Utility

The EISA non-volatile RAM checksum is incorrect or cannot correctly read the EISA slot. This can indicate either the EISA non-volatile memory has become corrupted or the slot has been configured incorrectly. Ensure also that the card is installed firmly in the slot.

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EISA Configuration Is Not Complete - Please Run EISA Configuration Utility

The slot configuration information stored in the EISA non-volatile memory is incomplete.



Note:

When either of the above EISA error messages appears, the system boots in ISA mode so that you can run the EISA Configuration Utility.

Error Encountered Initializing Hard-Drive

Hard drive cannot be initialized. Make sure that the adapter is installed correctly and that all cables are correctly and firmly attached. Ensure also that the correct hard drive type is selected in “Setup”.

Error Initializing Hard-Disk Controller

Cannot initialize controller. Make sure that the cord is correctly and firmly installed in the bus. Ensure also that the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

Floppy-Disk Controller Error or No Controller Present

Cannot find or initialize the floppy drive controller. Make sure that the controller is installed correctly and firmly. If there are no floppy drives installed, ensure that the floppy-disk drive selection in “Setup” is set to NONE.

Invalid EISA Configuration - Please Run EISA Configuration Utility

The non-volatile memory containing EISA configuration information was programmed incorrectly or has become corrupted. Re-run EISA configuration utility to correctly program the memory.



Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

Keyboard Error or No Keyboard Present

Cannot initialize the keyboard. Make sure that the keyboard is attached correctly and that no keys are being pressed during the boot process.

If you are deliberately configuring the system without a keyboard, set the “Error Halt” condition in “Setup” to HALT ON ALL, BUT KEYBOARD. This causes the BIOS to ignore the missing keyboard and continue the boot process.

Memory Address Error at ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

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Memory Parity Error at ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory Size Has Changed Since Last Boot

Memory has been added or removed since the last boot. In EISA mode use the configuration utility to reconfigure the memory configuration. In ISA mode enter “Setup” and enter the new memory size into the memory fields.

Memory Verify Error at ...

Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

Offending Address not Found

This message is used in conjunction with the “I/O Channel Check” and “RAM Parity Error” messages whenever the segment that has caused the problem cannot be isolated.

Offending Segment

This message is used in conjunction with the “I/O Channel Check” and “RAM Parity Error” messages whenever the segment that has caused the problem has been isolated.

Press a Key to Reboot

This message appears at the bottom of the screen when an error occurs that requires you to reboot. Press any key to reboot the system.

Press “F1” to Disable NMI, “F2” to Reboot

When the BIOS detects a non-maskable interrupt condition during boot, you can disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

RAM Parity Error - Checking for Segment ...

Indicates a parity error in the random access memory.

Should Be Empty But EISA Board Found - Please Run EISA Configuration Utility

A valid board ID was found in a slot that was configured as having no board ID.



Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

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Should Have EISA Board but not Found - Please Run EISA Configuration Utility

The board installed is not responding to the ID request, or no board ID has been found in the indicated slot.



Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

Slot not Empty

Indicates that a slot designated as empty by the EISA Configuration Utility actually contains a board.



Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

System Halted, <CTRL-ALT-DEL> to Reboot ...

Indicates that the present boot attempt has been aborted and that the system must be rebooted. Press and hold down the “CTRL” and “ALT” keys and press “DEL”.

Wrong Board in Slot - Please Run EISA Configuration Utility

The board ID does not match the ID stored in the EISA non-volatile memory.



Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

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4.14 POST Codes

ISA and PCI POST codes are routed to port address 80H.

Table 4-10: Early POST Codes before System BIOS is Shadowed

POST Code	Action
Reset	RTC & KBC initialization
0CFh	Early CPU Detection
0C0h	Early Chipset initialization
0C1h	Memory presence test: detects memory modules and programs chipset accordingly
0C6h	L2 Cache sizing test
0C3h	Decompresses Bios
0C5h	Shadows Main Bios and jumps to POST

Table 4-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
03h	Set 40h, 72h to 1234h if it was a warm boot
04h	Reserved
05h	SuperIO early programming Clear Screen Initializes KBC
06h	Tests whether F000-Segment read/writeable Detects flash type
07h	Tests CMOS access If supported: Test if overide key (Insert) pressed during reset
08h 0BEh	-- Programs chipset defaults
09h	Reads CPU ID Cache initialization if necessary If supported: Restores CMOS from flash backup if required
0Ah	Initializes interrupt vectors Copies CMOS to stack If supported: Checks for dual processor

Table continued on following page

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Table 4-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
0Bh	Detects Coprocessor Initializes Power Management chipset Updates CPU microcode if P6 CPU Reads existing ESCD Scans PCI devices and busses, assigns I/O and Memory to PCI devices Initializes Clock generator Initializes Hardware monitoring / temperature sensor
0Ch	Initializes keyboard buffer in BDA
0Dh 0BFh 0Dh	-- Program chipset Measures CPU core speed Initializes VGA video If VGA video not found: Checks for CGA If none found: Beepcode -..
0Eh	If CGA video found: Checks video memory If supported: Tries to init Award preboot agent If supported: Shows graphic logo, otherwise shows EPA logo If not full screen graphic logo, shows copyright message and CPU type and speed If ISA VGA video: Switches on ISA video ROM shadowing
0Fh	Tests DMA Channel 0
10h	Tests DMA Channel 1
11h	Tests DMA Page Registers
12h	--
13h	--
14h	Tests and init timer (8254)
15h	If not warm boot: tests MasterPIC mask register bits
16h	If not warm boot: tests SlavePIC mask register bits
17h	--
18h	Tests PIC’s by use of timer. Restores timer
19h	--
1Ah	--
1Bh	--
1Ch	--
1Dh	--
1Eh	--

Table continued on following page

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Table 4-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
30h	Measures total memory size
31h	Initialize USB Tests all memory above 1MB, shows memory size
32h	Scans for ISA PnP devices, isolates and assigns CSN to ISA PnP devices Disables SuperIO COM/LPT ports Detects and records COM/LPT ports Programs Super IO according to setup and detects any other COM/LPT ports present in the system Programs Audio system Initializes chipset EIDE channels
33h	--
34h	--
35h	--
36h	--
37h	--
38h	--
39h	--
3Ah	--
3Bh	--
3Ch	Enables going to setup
3Dh	Installs PS/2 mouse if present If ACPI supported: checks for compressed ACPI table
3Eh	Attempts to enable L2 Cache
3Fh	--
40h	--
41h 0BFh	-- Programs chipset Chipset auto configuration if required SuperIO COM/LPT auto configuration if required Records system device nodes Assigns resources to ISA PnP devices Installs Floppy disk
42h	Installs EIDE hard disk and ATAPI drives
43h	Checks and initializes COM/LPT ports
44h	--

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Table 4-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
45h	Initializes coprocessor
46h	--
47h	Saves boot_sector_buffer
48h	--
49h	--
4Ah	--
4Bh	--
4Ch	--
4Dh	--
4Eh	Checks for USB keyboard Displays previously detected POST errors. If any, checks for "Halt on" condition setting and if necessary, waits for keys "F1" or "Del".
4Fh	Checks for password entry if necessary
50h	Saves CMOS values in stack back to CMOS
51h	Switches all ISA PnP devices into "Wait For Key" state
52h	USB final initialization Decompresses embedded PCI Option ROM's Assigns IRQ's to PCI devices Programs onboard SCSI if present and activated If ACPI supported: Decompresses and installs ACPI table Checks for and runs non-video option ROM's Switches on ISA option ROM shadowing Fetches and runs embedded SCSI Option ROM's Fetches and runs embedded ISA Option ROM's Disables unused shadow areas Releases lower 32KB of E000 Segment
53h	--
54h	--
55h	--
56h	--
57h	--
58h	--
59h	--
5Ah	--
5Bh	--

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Table 4-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
5Ch	--
5Dh	--
5Eh	--
5Fh	--
60h	Prepares EIDE/ATAPI/SCSI for boot
61h	Sets speed turbo/deturbo Final chipset initialization Final power management initialization Clears screen Shows system info
62h	Programs keyboard numlock/typerate
63h	Builds ESCD and saves ESCD in flash Checks for correct century in CMOS Setup timer tick in BDA Clears any pending keys in BDA Flushes cache Releases upper 32KB of E000 Segment if Award Preboot Agent not present and active
0FFh	Boot

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Appendix A

Rear I/O Module CP-RIO6-04

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A Rear I/O Module CP-RIO6-04

A.1 Introduction

The CP-RIO6-04 rear I/O module has been designed for use with the CP604 and CP604-PM 6U CompactPCI boards from *PEP* Modular Computers. This rear I/O module provides comprehensive rear I/O functionality and may also be configured for use in other applications.

Everything that can be routed through the front panel may also be routed through the rear I/O. A particular advantage of the rear I/O capability is that there is no cabling on the CPU board which makes it much easier to remove the CPU in the rack.

The rear I/O is plugged in from the back of the system into the backplane connectors P3, P4 and P5 in line with the CPU board.

A.1.1 Dimensions

The dimensions of the 6U rear I/O module CP-RIO6-04 are as follows:

233.35 mm x 80 mm (6U rear I/O card size).

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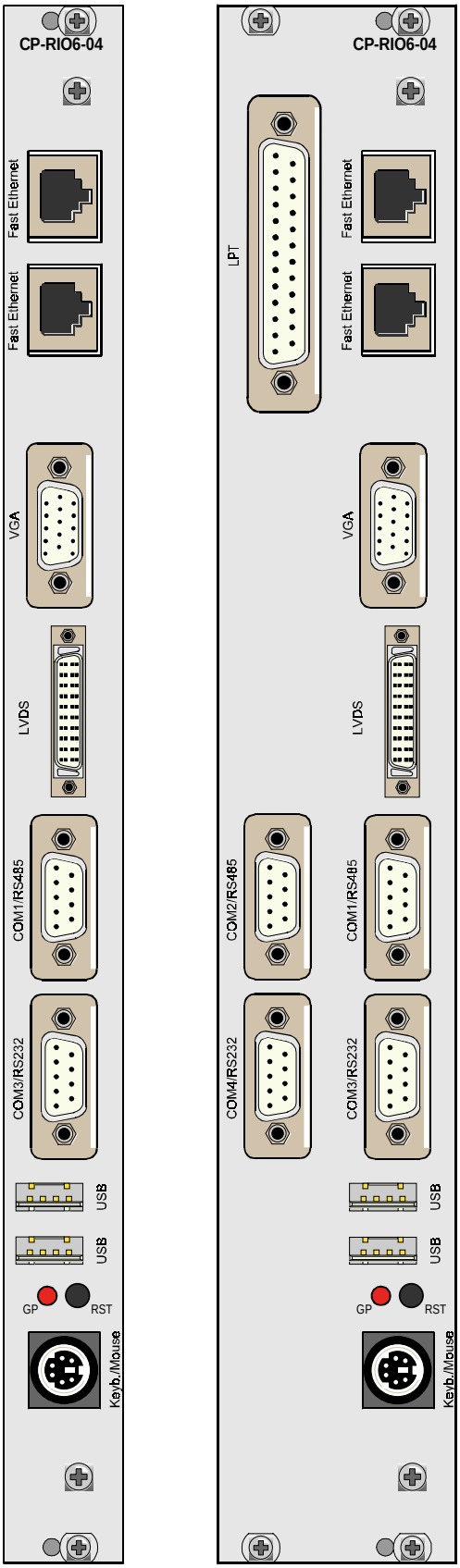
A.2 Front Panels

Figure A-1: CP-RIO6-04 Front Panels

There is one board LED on each front panel, situated beneath the USB connectors.

Board LED:

- GP (red) = general purpose LED

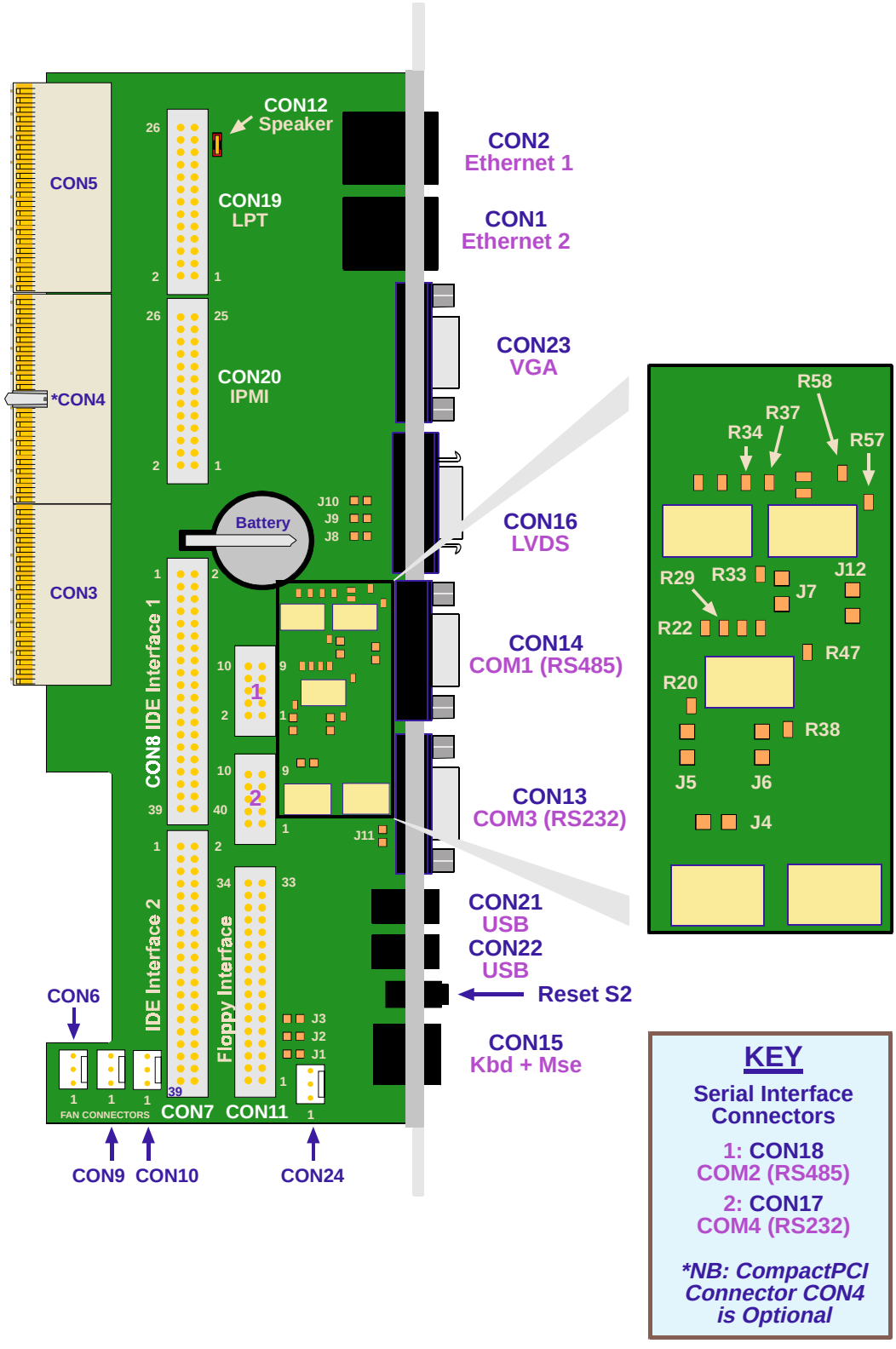


4HP Version **8HP Version with 4 COM ports**

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A.3 Board Layout

Figure A-2: CP-RIO6-04 Module Board Layout



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A.4 Overview of Module Interfaces

A.4.1 Overview of Module Interfaces and other Features

A.4.1.1 Front Panel (width 4HP) Interfaces and Features

Interfaces located directly on the CP-RIO6-04, available via the front panel connectors:-

- Two Fast Ethernet channels, each with 8-pin RJ45 modular jack
- VGA-CRT interface, 15-pin female high-density DSUB
- VGA-LVDS port for connecting a FlatPanel
- Two USB ports
- PS/2 Connector for mouse and keyboard, 6-pin MiniDIN
- Reset button
- COM1 interface (RS422/RS485)
- COM3 interface (RS232)

A.4.1.2 Internal interfaces (Accessible via Onboard Connectors)

- CompactPCI specification 6U rear I/O on J3, J4 and J5
- Floppy disk interface with a 34-pin 2.54 mm pinrow connector
- Two EIDE interfaces (EIDE1, EIDE2) with 40-pin 2.54 mm pinrow connectors
- IPMI interface and a connector for its power supply with differential voltage (selected via Jumpers J1-3)
- Optional serial interface COM2 (RS485/RS422)
- Optional serial interface COM4 (RS232)
- LPT-Interface
- Speaker connector
- Fan power connectors
- Optional battery for RTC on the rear I/O

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A.5 Detailed Description of Module Interfaces

A.5.1 Keyboard/Mouse Interface

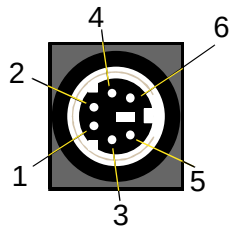


Figure A-3: Keyboard/Mouse Connector

The PC/AT standard keyboard/mouse connector is a PS/2-type 6-pin shielded mini-DIN connector.

A.5.1.1 Keyboard/Mouse Connector CON15 Pinout

Table A-1: Keyboard Connector CON15 Pinout

Pin Number	Name	Function	In/Out
1	KDATA	Keyboard data	In/Out
2	MDATA	Mouse data	In/Out
3	GND	Ground signal	--
4	VCC	VCC signal	--
5	KCLK	Keyboard clock	Out
6	MCLK	Mouse clock	Out



Note:

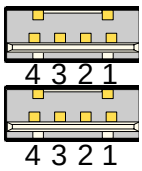
The keyboard/mouse power supply units are each protected by a 500 mA fuse. All signal lines are EMI-filtered.

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A.5.2 USB Interfaces

Figure A-4: USB Connectors CON21 and CON22

There are two identical USB interfaces on the CP-RIO6-04 module each with a maximum transfer rate of 12 Mbit provided for connecting USB devices. One USB peripheral may be connected to each port. To connect more than two USB devices an external hub is required.



A.5.2.1 USB Connectors CON21 and CON22 Pinouts

Table A-2: USB Connector CON21 and CON22 Pinouts

Pin Number	Name	Function	In/Out
1	VCC	VCC signal	--
2	UV0-	Differential USB-	--
3	UV0+	Differential USB+	--
4	GND	GND signal	--



Note:

The USB power supply feeding the two ports is protected by a 1.5 A fuse. All signal lines are EMI-filtered.

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A.5.3 VGA-CRT Interface

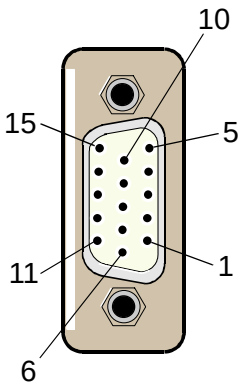


Figure A-5: D-sub VGA-CRT Connector CON23

A.5.3.1 VGA Connector CON23 Pinout

The 15-pin female connector CON23 is used to connect a VGA monitor to the CP-RIO6-04 rear I/O board.

Table A-3: VGA connector CON23

D-sub 15	Signal	Function	In/Out
1	Red	Red video signal output	Out
2	Green	Green video signal output	Out
3	Blue	Blue video signal output	Out
13	Hsync	Horizontal sync.	TTL Out
14	Vsync	Vertical sync.	TTL Out
12	Sdata	I2C™ data	In/Out
15	Sclk	I2C™ clock	Out
9	VCC	Power +5V 200 mA no fuse protection	Out
5,6,7,8,10	GND	Signal ground	--
4,11	Free	--	--

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A.5.4 LVDS Interface

For connecting LVDS TFT displays, the module is equipped with a 6-bit per color FPD-Link LVDS transmitter from National Semiconductor (DS90C363A). The programmable version of this device is used to provide the ability to switch between falling edge and rising edge triggering (default is falling edge). The pixel clock of this device has a range between between 20 and 65 MHz.

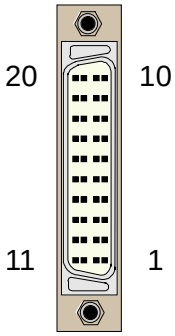


Table A-4: LVDS Connector CON16 Pinout

Pin Number	Function
1	+RTX 1
2	-RTX 1
3	Shield
4	Shield
5	+RTXCLK
6	-RTXCLK
7	GND
8	VCC (if J9 set), otherwise:NC
9	NC
10	NC
11	+RTX 2
12	-RTX 2
13	Shield
14	Shield
15	+RTX 0
16	-RTX 0
17	+12V (if J10 set), otherwise:NC
18	RFPVEE (if J8 set), otherwise:NC
19	NC
20	NC
21	Shield
22	Shield

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A.5.5 Serial Port Interfaces

The serial port interfaces COM1 (CON14) and COM3 (CON13) are situated on the front panel of the rear I/O, while COM2 (CON18) and COM4 (CON17) are onboard.

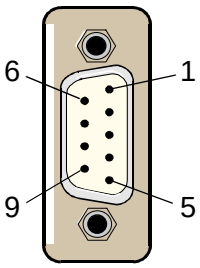


Figure A-6: PC-compatible D-Sub Serial Connectors CON13 and CON14

Two PC-compatible serial 9-pin D-sub ports are available with 5V charge-pump technology eliminating the need for a +12V and -12V supply. The two COM ports, which are fully compatible with the 16550 controller, include a complete set of handshaking and modem control signals, maskable interrupt generation and data transfer of up to 460.8 kB/s.

The functions of each serial port interface are shown in the following table:-

Table A-5: Functions of the Serial Port Interfaces

Interface	Function
COM1	RS485/RS422
COM2	RS485/RS422
COM3	RS232
COM4	RS232

The Serial Port connector pinouts appear on the following pages

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A.5.5.1 Serial Port Connectors CON18 (COM2) and CON17 (COM4) Pinout

The following table gives the pinout of the optional onboard flatcable pinrow connectors COM2 and COM4

Table A-6: Serial Port Connectors CON18 (COM2) and CON17 (COM4) Pinout

Pin	RS232 (COM4)	RS422 (COM2)	RS485(COM2)
1	DCD	+RXD	NC
2	DSR	–RXD	NC
3	RXD	NC	NC
4	RTS	NC	NC
5	TXD	+TXD	+TRXD
6	CTS	–TXD	–TRXD
7	DTR	NC	NC
8	RIN	NC	NC
9	GND	GND	GND
10	NC	NC	NC



Note:

The RS422 connector is *PEP*-specific and the serial control signals are not available.

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A.5.5.2 Serial Port Connectors CON14 (COM1) and CON13 (COM3) Pinout

The pinout of the 9-pin D-sub connectors depends on the configuration.

Table A-7: Serial Port Connectors CON14 (COM1) and CON13 (COM3) Pinout

Pin Number	RS232 (COM3) (Standard PC)	RS422 (COM1)	RS485 (COM1)
1	DCD	+RXD	NC
2	RXD	NC	NC
3	TXD	+TXD	+TRXD
4	DTR	NC	NC
5	GND	GND	GND
6	DSR	–RXD	NC
7	RTS	NC	NC
8	CTS	–TXD	–TRXD
9	RIN	NC	NC



Note:

- The RS422 connector is *PEP*-specific and the serial control signals are not available.
- To ensure the proper functioning of the rear I/O serial interfaces, the drivers for COM1 and COM2 port on the CP604-PM must be disabled.

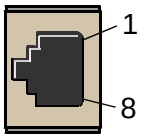
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A.5.6 Fast Ethernet Interfaces

The selection of rear I/O or baseboard front panel Fast Ethernet ports is made via the BIOS setup.

Figure A-7: Ethernet/Fast Ethernet Connectors

The Ethernet connector is realized as an RJ45 twisted-pair connector. The Interface provides automatic detection and switching between 10Base-T and 100Base-TX data transmission.



A.5.6.1 Fast Ethernet Connectors CON1 and CON2 Pinout

The CON1 and CON2 connectors provide the 10Base-TX/100Base-TX interface to the Ethernet controller. These interfaces are enabled/disabled via the BIOS setting or the rear I/O configuration register.

Table A-8: Fast Ethernet Connectors CON1 and CON2 Pinout

RJ45	Signal	Function
1	TX+	Transmit +
2	TX–	Transmit –
3	RX+	Receive +
4	NC	--
5	NC	--
6	RX–	Receive –
7	NC	--
8	NC	--

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A.5.7 IPMI Interface

The Intelligent Platform Management Interface is described in full in section 2.7 in chapter 2. It is accessed from the CP-RIO6-04 by means of the onboard connector, CON20.

A.5.7.1 IPMI Connector CON20 Pinout

Table A-9: IPMI Connector CON20 Pinout

Pin Number	Signal Name	Signal Name	Pin Number
1	UART0_DIN	UART0_DOUT	2
3	UART0_CTS	UART0_DCD	4
5	UART0_RTS	UART0_RI	6
7	XMIT_EN	ID_XMIT_EN	8
9	CONN_ID0	CONN_ID1	10
11	CONN_ID_DRV	3.3V	12
13	IPMI_VCC	GND	14
15	TACH_IN0	TACH_IN1	16
17	TACH_IN2	TACH_IN3	18
19	PWM0	PWM1	20
21	IPMIGPIO2	GND	22
23	IPMI_VCC	J2ALERT	24
25	J2SDA	J2SCL	26

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A.5.8 Fan Control Interface

A.5.8.1 Fan Control Connector Pinouts

The fan control connectors, CON6, CON9 and CON10, and the optional connector for an external cooling fan, CON24, have the following pinouts:-

Table A-10: Fan Control Connector CON 6 Pinout

Pin Number	Function
1	Ground
2	Fan Supply Voltage
3	Fansense (2)

Table A-11: Fan Control Connector CON 9 Pinout

Pin Number	Function
1	Ground
2	Fan Supply Voltage
3	Fansense (1)

Table A-12: Fan Control Connector CON 10 Pinout

Pin Number	Function
1	Ground
2	Fan Supply Voltage
3	Fansense(3)

Table A-13: External Cooling Fan CON24 Pinout (Optional)

Pin Number	Function
1	Ground
2	External Fan Power
3	Ground

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A.5.9 EIDE Ports

A.5.9.1 EIDE Connectors EIDE1 (CON8) and EIDE2 (CON7) Pinouts

The following table sets out the pinning of connectors CON8 and CON7 and details their corresponding signal names and functions.

The maximum length of cable that may be used is 25 cms.

Table A-14: Pinout of AT Standard Connectors EIDE1 and EIDE2

Pin	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	NC	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	NC		--
33	A1	Address 1	Out
34	NC	--	--
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	NC	--	--
40	GND	Ground signal	--

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A.5.10 Floppy Drive Interface

The CP-RIO6-04 is provided with a 2-row 34-pin male standard connector, CON11, realized as a connector which provides the signals for up to two floppy drives.

Warning!

If the floppy disk drive connection cable is inverted (pin 1 in place of pin 34), at “power on”, the floppy disk drive will work uninterruptedly, with consequent risk of damage to the floppy disk inserted.

A.5.10.1 Floppy Drive Connector CON11 Pinout

Table A-15: Floppy Drive Connector CON11 Pinout

Pin Number	Signal	Function	In/Out
2	RWC	Write precompensation	Out
4	NC	--	--
6	NC	--	--
8	INDEX	Index pulse	In
10	MOTEN1	Motor 1 enable	Out
12	DRVSEL2	Driver select 2	Out
14	DRVSEL1	Driver select 1	Out
16	MOTEN2	Motor 2 enable	Out
18	DIRECTION	Step direction	Out
20	STEP	Step pulse	Out
22	WRDATA	Write data	Out
24	WREN	Write enable	Out
26	TRACK0	Track 0 signal	In
28	WRPROT	Write protect	In
30	RDDATA	Read data	In
32	HEADSEL	Head select	Out
34	DSKCHG	Disk change	In
ODD NR.	GND	Ground signal	--

A.5.10.2 Floppy Drive “A+B” Configuration

Important:

The floppy drive connection cable is suitable for use with two PC-compatible floppy disk drives. Make sure you plug the cable into the connector assigned to floppy drive “A:”. If it is plugged into the drive “B:” connector, no boot from the floppy drive is possible.

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A.5.11 LPT Interface

The LPT interface is routed through a 26-pin 2.54 mm pinrow connector. To use a standard parallel port device a special adapter is necessary.

Table A-16: LPT Interface Connector CON19 Pinout

Pin Number	Signal	Pin Number	Signal
1	STROBE	14	GND
2	AUTOFD	15	PD6
3	PD0	16	GND
4	ERROR	17	PD7
5	PD1	18	GND
6	INIT	19	ACK
7	PD2	20	GND
8	SLCTIN	21	BUSY
9	PD3	22	GND
10	GND	23	PE
11	PD4	24	GND
12	GND	25	SLCT
13	PD5	26	GND

A.5.12 Speaker Interface

A speaker may be connected using the onboard connector CON12.

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A.5.13 CompactPCI Interface

The standard rear I/O module is equipped with CON3 and CON5. Users requiring LVDS, IPMI or LPT functionality will need an additional CompactPCI connector, CON4.

A.5.13.1 CompactPCI Connectors J3-J5 (CON3-CON5) Pinouts

The CP-RIO6-04 is provided with two, optionally three, female rear I/O connectors J3, J4 and J5. The same pinouts apply to the matching rear I/O connectors P3, P4 and P5 of the CP604-PM baseboard. For convenience these tables are presented both here and in Chapter 2, “Functional Description and Configuration” of this manual.

Table A-17: Backplane J3 Pin Definitions

Pin	Z	A	B	C	D	E	F
19	GND	IDERST 6)	IDE-ICHRDYB 8)	IDE-ICHRDYA 6)	IDEIRQB 8)	IDEIRQA 6)	GND
18	GND	IDECSB0 8)	IDECSB1 8)	IDECSA0 6)	IDECSA1 6)	IDEDAKB 8)	GND
17	GND	IDEDA15 6)	IDPDA14 6)	IDEDA13 6)	IDEDA12 6)	IDEDRQB 8)	GND
16	GND	IDEDA11 6)	IDEDA10 6)	IDEDA9 6)	IDEDA8 6)	IDEDAKA 6)	GND
15	GND	IDEAA0 6)	IDEAA1 6)	VCC	IDEAA2 6)	IDEDRQA 6)	GND
14	GND	IDEDA7 6)	IDEDA6 6)	IDEDA5 6)	IDEDA4 6)	IDEIOWA 6)	GND
13	GND	IDEDA3 6)	IDEDA2 6)	IDEDA1 6)	IDEDA0 6)	IDEIORA 6)	GND
12	GND	FD.DS0 7)	FD.DENSEL1 7)	FD.MTR0 7)	FD.INDEX 7)	FD.WDATA 7)	GND
11	GND	FD.DS1 7)	FD.DSKCHG 7)	FD.MTR1 7)	FD.DENSEL0 7)	FD.RDATA 7)	GND
10	GND	FD.WP 7)	FD.HDSEL 7)	FD.DIR 7)	FD.TRK0 7)	FD.STEP 7)	GND
9	GND	FD.WGATE 7)	IDEDB15 8)	IDEDB14 8)	IDEDB13 8)	USB0+ 2)	GND
8	GND	IDEDB12 8)	IDEIOWB 8)	VCC	IDEIORB 8)	USB0- 2)	GND
7	GND	IDEAB2 8)	IDEAB1 8)	IDEAB0 8)	IDEDB0 8)	IDEDB1 8)	GND
6	GND	IDEDB2 8)	IDEDB3 8)	IDEDB4 8)	IDEDB5 8)	IDEDB6 8)	GND
5	GND	SMBCLK 1)	PMDAT 5)	SPKR 1)	KDAT 5)	SMBDAT 1)	GND
4	GND	PRST 1)	PMCLK 5)	VCC	KCLK 5)	S3RXD 3)	GND
3	GND	S3CTS 3)	S3RTS 3)	S3DSR 3)	S3DCD 3)	S3TXD 3)	GND
2	GND	IDEDB7 8)	IDEDB8 8)	S3RIN 3)	S3DTR 3)	S4RXD 4)	GND
1	GND	IDEDB9 8)	IDEDB10 8)	IDEDB11 8)	BATT 1)	S4TXD 4)	GND

The legend for this table appears on the following page

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Legend for Backplane J3 Table

Table A-18: Backplane J3 Signal Functions

Signal	Function
Control Signals	
SPKR 1)	Speaker output signal
BATT 1)	Battery input signal for RTC; max. 3.3V
PRST 1)	Reset input signal
SMBCLK, SMBDAT 1)	Onboard SMBus signals
USB port 0	
USB0+/- 2)	USB data differential data signals
Serial Port 3	
S3* 3)	Serial port signals; TTL level
Serial Port 4	
S4RXD S4TXD 4)	Serial port signals; TTL level
Mouse + Keyboard	
KDAT 5), KCLK 5)	Keyboard data and clock
PMDAT 5), PMCLK 5)	Mouse data and clock
IDE*A 6)	EIDE Primary signals
Blue signals 7)	Floppy signals
IDE*B 8)	EIDE Secondary signals

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Table A-19: Backplane J4 Pin Definitions

Pin	Z	A	B	C	D	E	F
25	GND	VCC	RES 4)	RES 4)	+3.3V	VCC	GND
24	GND	RES 4)	PD0 1)	INIT 1)	RES 4)	RES 4)	GND
23	GND	+3.3V	RES	RES 4)	VCC 2)	RES 4)	GND
22	GND	RES 4)	PD1 1)	RES 4)	RES 4)	RES 4)	GND
21	GND	+3.3V	RES 4)	AUTOFD 1)	RES 4)	J2ALERT 2)	GND
20	GND	RES 4)	PD2 1)	SLCTIN 1)	J2SCL 2)	J2SDA 2)	GND
19	GND	+3.3V	PD3 1)	STROBE 1)	RES 4)	IPMIGPIO2 2)	GND
18	GND	RES 4)	PD4 1)	RES 4)	PWM1 2)	PWM0 2)	GND
17	GND	+3.3V	PD5 1)	BUSY 1)	RES 4)	TACH_IN3 2)	GND
16	GND	RES	PD6 1)	RES 4)	TACH_IN2 2)	TACH_IN1 2)	GND
15	GND	+3.3V	PD7 1)	ACK 1)	RES 4)	TACH_IN0 2)	GND
12-14	GND						GND
11	GND	RES 4)	IPMI VCC 1)	PE 1)	RES 4)	CONN_ID_DRV 2)	GND
10	GND	RES 4)	RES 4)	RES 4)	ID_XMIT_EN 2)	CONN_ID1 2)	GND
9	GND	RES 4)	IPMI VCC	SLCT 1)	RES 4)	CONN_ID0 2)	GND
8	GND	RES	GND	RES 4)	XMIT_EN 2)	UART0_RI 2)	GND
7	GND	GND	LVDS TX_P2 3)	ERROR 1)	RES 4)	UART0_RTS 2)	GND
6	GND	RES 4)	LVDS TX_N2 3)	RES 4)	UART0_DCD	UART0_CTS 2)	GND
5	GND	GND	GND	LVDS TX_P1 3)	UART0_DOUT 2)	UART0_DIN 2)	GND
4	GND	RES 4)	GND	LVDS TX_N1 3)	GND	GND	GND
3	GND	LVDS ENAVDD 3)	LVDS FPVEE 3)	GND	LVDS TX_P0 3)	LVDS TXCLKP 3)	GND
2	GND	RES 4)	RES 4)	GND	LVDS TX_N0 3)	LVDS TXCLKN 3)	GND
1	GND	VCC	-12V	GND	+12V	VCC	GND

Legend for Backplane J4 Table

1) Parallel Port signals

2) IPMI control signals

3) VGA LVDS signals

4) Reserved

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Table A-20: Backplane J5 Pin Definitions

Pin	Z	A	B	C	D	E	F
22	GND	PMCR4	PMCR3	PMCR2	PMCR1	PMCR0	GND
21	GND	PMCR9	PMCR8	PMCR7	PMCR6	PMCR5	GND
20	GND	PMCR14	PMCR13	PMCR12	PMCR11	PMCR10	GND
19	GND	PMCR19	PMCR18	PMCR17	PMCR16	PMCR15	GND
18	GND	PMCR24	PMCR23	PMCR22	PMCR21	PMCR20	GND
17	GND	PMCR29	PMCR28	PMCR27	PMCR26	PMCR25	GND
16	GND	PMCR34	PMCR33	PMCR32	PMCR31	PMCR30	GND
15	GND	PMCR39	PMCR38	PMCR37	PMCR36	PMCR35	GND
14	GND	PMCR44	PMCR43	PMCR42	PMCR41	PMCR40	GND
13	GND	PMCR49	PMCR48	PMCR47	PMCR46	PMCR45	GND
12	GND	PMCR54	PMCR53	PMCR52	PMCR51	PMCR50	GND
11	GND	PMCR59	PMCR58	PMCR57	PMCR56	PMCR55	GND
10	GND	+3.3V	PMCR63	PMCR62	PMCR61	PMCR60	GND
9	GND	TDN2 2)	RDN2 2)	S1RXD 4)	TDN1 2)	RDN1 2)	GND
8	GND	TDP2 2)	RDP2 2)	S1TXD 4)	TDP1 2)	RDP1 2)	GND
7	GND	COM2_ENABLE 1)	COM1_ENABLE 1)	S1RTS 4)	USB1+ 3)	+3.3V	GND
6	GND	S1DTR 4)	S1CTS 4)	S1DSR 4)	S1DCD 4)	S1RIN 4)	GND
5	GND	S2RXD 5)	S2TXD 5)	S2RTS 5)	S2DTR 5)	ROUT 8)	GND
4	GND	S2DSR 5)	S2DCD 5)	S2RIN 5)	S2CTS 5)	HSYNC 8)	GND
3	GND	S4DTR 6)	S4CTS 6)	S4DSR 6)	GPLED 1)	BOUT 8)	GND
2	GND	S4RTS 6)	S4RIN 6)	FANSENSE2 7)	FANPWM 7)	VSYNC 8)	GND
1	GND	S4DCD 6)	RIOPRESENT 1)	FANSENSE1 7)	USB1- 3)	GOUT 8)	GND

The legend for this table appears on the following page

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Legend for Backplane J5 Table

Table A-21: Backplane J5 Signal Functions

Signal	Function
Control signals	
COM1_ENABLE 1)	Serial port 1 enable signal for front I/O and rear I/O Low = Front I/O High = Rear I/O
COM2_ENABLE 1)	Serial port 2 enable signal for front I/O and rear I/O Low = Front I/O High = Rear I/O
GPLED 1)	General purpose LED output
RIOPRESENT 1)	Low = rear I/O module is present High = rear I/O module is not present This signal must be set on the rear I/O module to GND
Ethernet 1	
TDP1 2)	Ethernet high transmit Data line
TDN1 2)	Ethernet low transmit Data line
RDP1 2)	Ethernet high receive Data line
RDN1 2)	Ethernet low receive Data line
Ethernet 2	
TDP2 2)	Ethernet high transmit Data line
TDN2 2)	Ethernet low transmit Data line
RDP2 2)	Ethernet high receive Data line
RDN2 2)	Ethernet low receive Data line
USB port 1	
USB1+/- 3)	USB data differential data signals
Serial Port 1	
S1* 4)	Serial port signals; TTL level
Serial Port 2	
S2* 5)	Serial port signals; TTL level
Serial Port 4	
S4* 6)	Serial port signals; TTL level
FAN control	
FANPWM 7)	DAC output that can be used to control fan speed; 0V to +1.25V output
FANSENSE1/2 7)	Schmitt Trigger fan tachometer inputs; TTL level
VGA CRT signals	
ROUT 8)	Red signal
GOUT 8)	Green signal
BOUT 8)	Blue signal
HSYNC 8)	Horizontal Sync.
VSYNC 8)	Vertical Sync.
PMC Rear I/O signals	

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A.6 Jumper/Resistor Setting

A.6.1 Serial Ports COM1-COM4 Jumper/Resistor Setting

The following tables detail the range of Jumpers/Resistors used to select and terminate the serial interfaces:

A.6.1.1 COM1 Jumper/Resistor Setting

Table A-22: COM1: RS422/RS485 Selection

Resistor	Setting	Description
R58	*Closed*	*RS485 mode (= half duplex)*
	Open	RS422 mode (= full duplex)

The default setting is indicated by italics.

Table A-23: COM1: Bus Termination

Jumper	Setting	Description
J7*	Closed	Transmit Data line: termination on
	Open	*Transmit Data line: termination off*
J12	Closed	Receive Data line: termination on
	Open	*Receive Data line: termination off*

The default setting is indicated by italics.



Note:

In RS485 mode, termination for common transmit and receive lines is enabled by J7*.

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A.6.1.2 COM2 Jumper/Resistor Setting

Table A-24: COM2: RS422/RS485 Selection

Resistor	Setting	Description
R47	*Closed*	*RS485 mode (= half duplex)*
	Open	RS422 mode (= full duplex)

The default setting is indicated by italics.

Table A-25: COM2: Bus Termination

Jumper	Setting	Description
J5*	Closed	Transmit Data line: termination on
	Open	*Transmit Data line: termination off*
J6	Closed	Receive Data line: termination on
	Open	*Receive Data line: termination off*

The default setting is indicated by italics.



Note:

In RS485 mode, termination for common transmit and receive lines is enabled by J5*.

A.6.1.3 COM3 Jumper Setting

Table A-26: COM3: RS232 ON/OFF

Jumper	Setting	Description
J11	*Open*	*RS232 active*
	Closed	RS232 disabled

The default setting is indicated by italics.

A.6.1.4 COM4 Jumper Setting

Table A-27: COM4: RS232 ON/OFF

Jumper	Setting	Description
J4	*Open*	*RS232 active*
	Closed	RS232 disabled

The default setting is indicated by italics.

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A.6.2 Fan Power Supply Voltage Selection

The voltage for the cooling fans may be configured for either 5V or 12V using jumpers J1, J2 and J3

Table A-28: Fan Power Supply Voltage Setting

Jumper Settings	Voltage
J1 closed	Enable external cooling fan power
J2 closed	Supply voltage Vcc (5V)
J3 closed	*Supply voltage 12V*

The default setting is indicated by italics.

A.6.3 LVDS Interface CON16

Table A-29: Voltage Configuration for LVDS Interface

Jumper Setting	Voltage
J8 closed	RFPVEE
J9 closed	*Vcc*
J10 closed	+12V

The default setting is indicated by italics.



Reference:

For details about how to configure the LVDS of the CP-RIO6-04 rear I/O module for the CP604-PM baseboard, please see section 2.9.6, Panel Selection and section 2.9.8, Jumper Setting for rear I/O in chapter 2, Functional Description and Configuration in this manual.

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