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PB-DIO3

I/O Piggyback Module

for VMOD-2 and IMOD

Manual ID 12456, Rev. Index 0101
Nov 98

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Preface

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Revision History

Revision History			
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Manual ID Number:	**12456**		
Rev. Index	**Brief Description of Changes**	**Hardware Index**	**Date of Issue**
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For your safety

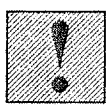
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- In performing all necessary installation and application operations, please, follow only the instructions supplied by the present manual.
- Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.
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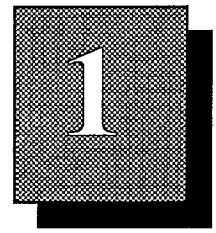
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1. INTRODUCTION

1.1 Product Overview

The PB-DIO3 is a 20 channel parallel Input/Output piggyback with eight optoisolated common GND inputs, eight optoisolated outputs with either common Vcc or common GND (depending on board version ordered), and four handshake lines.

The PB-DIO3 can be used either with the VMOD-2 (non-intelligent Input/Output module for the VMEbus), or with the IMOD.

1.2 Ordering Information

Product	Description	Inputs	Outputs	Order Number
PB-DIO3	Industrial Input/Output piggyback with eight optoisolated inputs, eight optoisolated outputs and timer	Cmn GND 24V	Cmn GND 24V	523-23 *Old* 2994 *New*
PB-DIO3	Industrial Input/Output piggyback with eight optoisolated inputs, eight optoisolated outputs and timer	Cmn GND 24V	Cmn Vcc 24V	523-23/1 *Old* 2995 *New*

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1.3 Specifications

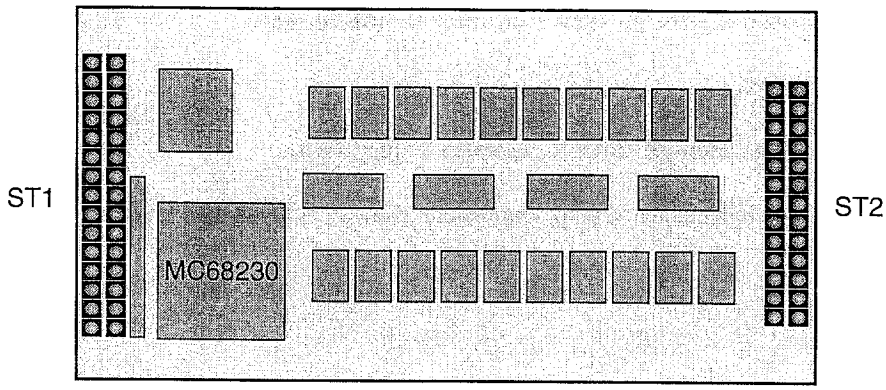
Input channels	8 digital inputs plus 2 handshake lines, all channels optoisolated; common GND
Output channels	8 digital output lines plus 2 handshake lines, all channels optoisolated.; common Vcc or GND
Input voltage	24V DC typically
Input current	5mA at 24V typically
Output voltage	24V
Output current	100mA maximum
Switching level	<5V = low, >7.5V = high
Input frequency	6.5 KHz maximum
Isolation voltages	2500V RMS input to system 100V DC between inputs
Timer	24 bit
Timer clock	8 MHz
Identification byte	$FD
Address range	128 byte
DTACK generation	On-board
Power requirements	+5V DC (+/- 5%) 500mA typically
Temperature range Standard Extended Storage	 0...+70°C -40...+85°C -55 to +85°C
Operating humidity	0 to 95% (Non-condensing)
Piggyback dimensions	Width: 48mm Length: 100mm Depth: 12 mm
VMOD-2 interface	Two sets of twin row header pins providing all necessary communication paths and a mechanical mounting method.

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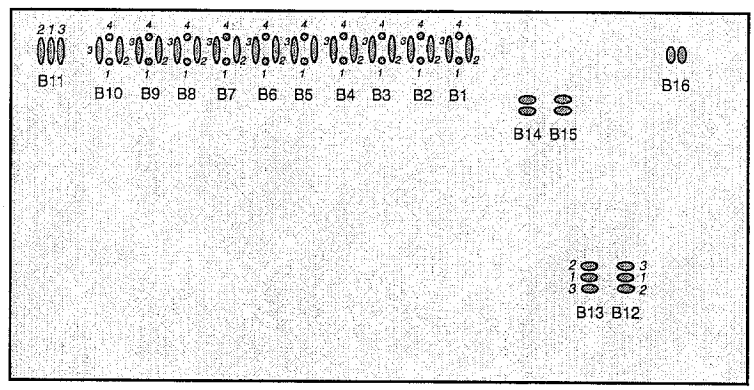
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1.4 Board Overview

Component Side



Solder Side



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1.5 Features

- Eight optoisolated inputs with common GND and two handshake lines;
- Eight optoisolated outputs with either common Vcc or common GND (depending on the board version ordered) and two handshake lines;
- Software selectable channels; ports can work in a variety of different ways;
- 24-bit programmable timer;
- Interrupt request line. Thge interrupt vector is generated by piggybacks;
- Each channel is fully and independently programmable to work as either simple bit Input/Output lines or a fully handshake controlled port.

1.6 Advantages

The PB-DIO3 module is designed to provide an easy to use interface for customer applications, resulting in maximum design flexibility. They provide a cost-effective solution, quick and easy implementation as well as full compatibility with existing PEP products.

The piggyback can be used with the VMOD-2 or the IMOD carrier modules.

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1.7 Typical Applications

The PB-DIO3 is typically used for Inputs/Outputs requiring 24V, which would include end switches, alarms, emergency stop devices, sensors, actuators and relays/switches.

1.8 Glossary of Terms

PSU Power Supply Unit

PCB Printed Circuit Board

PI/T Parallel Interface/Timer

1.9 Related Publications

VMEbus Specifications Revision C1
Data Sheet for the MC68230 from Motorola

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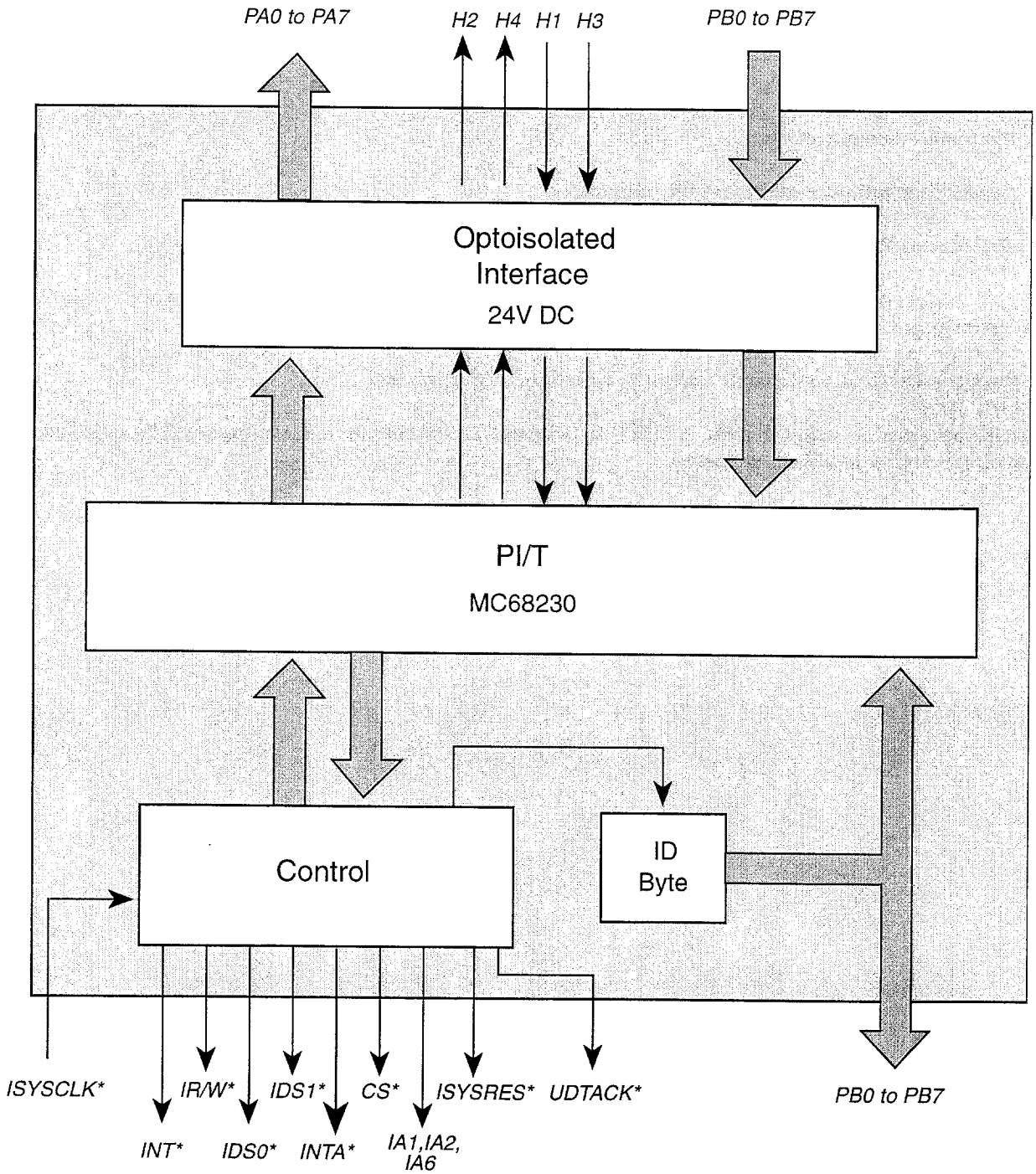
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2

2. FUNCTIONAL DESCRIPTION

This chapter describes the functionality of the main blocks of the PB-DIO3 piggyback.

Figure 2.0.0.1: PB-DIO3 Block Diagram



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2.1 The MC68230 Parallel Interface and Timer Chip (PI/T)

The MC68230 parallel interface and timer (PI/T) provides versatile double buffered interfaces and a system-oriented timer for MC68000 systems. The parallel interfaces operate either at 8 or 16 bits wide in unidirectional mode. An associated data direction register has to be set for input.

The PI/T timer contains a 24-bit counter and a 5-bit prescaler. The timer is clocked by the system clock (PI/T CLK pin) and the 5-bit prescaler may be used. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. It can also be used for elapsed time measurement or as a device watchdog.

The main features of the PI/T include:

- MC68000 bus compatible;
- Port Modes: Bit I/O
  Unidirectional 8 and 16 bit
- 24-bit programmable timing modes;
- 5 seperate interrupt vectors;
- Seperate port and timer interrupt service requests;
- Registers are Read/Write and directly accessable.

The PI/T consists of two logically independent sections: the ports and the timer. The port section consists of port A (PA0 to PA7), port B (PB0 to PB7) and four handshake pins (H1, H2, H3 and H4).

The timer consists of a 24-bit counter, optionally clocked by a 5-bit prescaler.

The handshake pins are routed as inputs (H1, H3) and outputs (H2, H4), but due to the optocouplers the signal path could be too slow for handshake protocols.

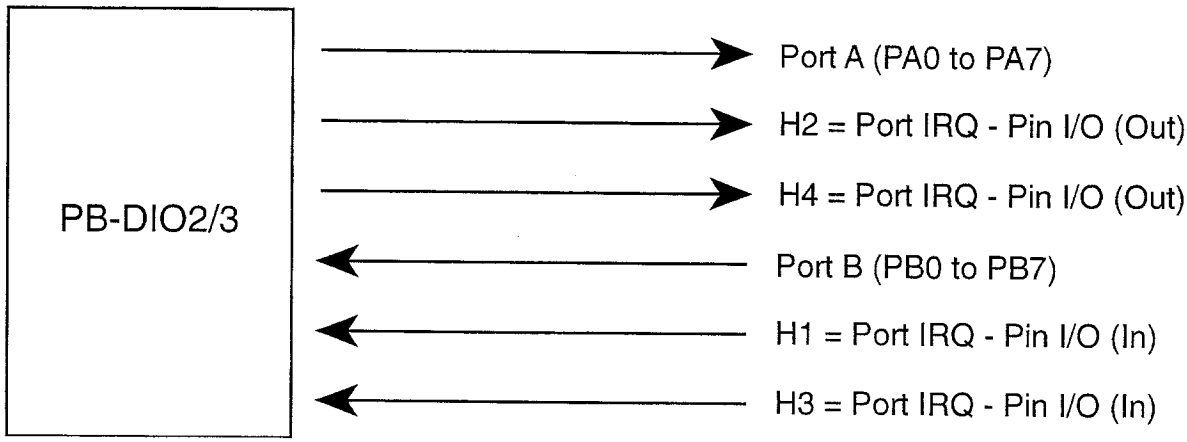
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2.2 The Input/Output Ports

The two input ports each consist of eight unidirectional lines and two multifunction handshake lines. This is illustrated in the Figure below.

Figure 2.2.0.1: The PB-DIO3 Input/Output Ports



Above all, the TTL input port enables the realisation of simple bit input of industrial applications such as switch operation or polling for the control of user-defined peripherals. Implementation of the individual bits is left completely up to the user.

Note

Simple output is easily programmed on port A pins PA0 to PA7. This is also true of simple input on Port B, which does not require constant monitoring. In this case, the handshake pins H1 and H3 should be used for "change of state" IRQ input, avoiding the need for constant polling.

The examples in chapter 4 illustrate the necessary initialisation procedures for the applications discussed above.

2.2.1 PI/T Port Modes

The PI/T can generally be used in 4 different port modes:

Mode 0:	Unidirectional 8-bit mode	
Mode 1:	*Unidirectional 16-bit mode*	*Not intended for the PB-DIO3*
Mode 2:	*Bidirectional 8-bit mode*	*Not intended for the PB-DIO3*
Mode 3:	*Bidirectional 16-bit mode*	*Not intended for the PB-DIO3*

2.2.2 Input Line Specification

- The interrupt inputs H1-H4 are connected via Schmidt triggers to the MC68230;
- H1, H3 and TIN have the option of being connected with a low pass input filter (jumper selectable).

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2.2.3 The Handshake Pins H1, H2, H3 and H4

Table 2.2.3.1: Use of the Handshake Pins

Description	Handshake Pins
Input Pin	H1, H3
Output Pin	H2, H4
Change of State IRQ Pin	H1, H3
Port A Handshake Pin	H1, H2
Port B Handshake Pin	H3, H4

These pins can be controlled by several of the PI/T registers. For more details please refer to the *Programming* chapter in this manual.

2.3 Timer Operation

The MC68230 timer can provide several facilities required by the MC68000 operating systems. It can generate periodic interrupts, or a single interrupt after a programmed time period. Also, it can be used for elapsed time measurement or as a device watchdog.

The PI/T timer contains a 24-bit synchronous down counter that is loaded from three 8-bit counter preload registers. The 24-bit counter may be clocked by the output of a 5-bit prescaler. If the prescaler is used, it may be clocked by the system clock (CLK pin). The counter signals the occurance of an event primarily through zero detection (a zero is detected when the counter of the 24-bit timer is equal to zero). This sets the Zero Detection Status (ZDS) bit in the timer status register. It may be checked by the processor or may be used to generate a timer interrupt. The ZDS bit can be reset by writing a one (1) to the timer status register in that bit position, independent of timer operation.

The general operation of the timer is flexible and easily programmable. The timer is fully configured and controlled by programming the 8-bit timer control register. It controls:

1) the choice between the port C operation and timer operation of three timer pins;
2) whether the counter is loaded from the counter preload register or rolls over when zero detect is reached;
3) the clock input;
4) whether the prescaler is used, and
5) whether the timer is enabled.

2.3.1 Run/Halt Definition

The overall operation of the timer is described in terms of the run or halt states. The control of the current state is determined by programming the timer control register.

When in the halt state, all of the following takes place:

1) The prior contents of the counter is not altered and is reliably readable via the count registers.
2) The prescaler is forced to $1F, whether or not it is used.
3) The ZDS status bit is forced to zero, regardless of the possible zero contents of the 24-bit counter.

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The run state is characterized by:

1) The counter is clocked by the source programmed in the timer control register.
2) The counter is not readily readable.
3) The prescaler is allowed to decrement if programmed for use.
4) The ZDS status bit is set when the 24-bit counter changes from $000001 to $000000.

Note

The TIN (external timer input) cannot be used.

2.4 VMEbus Interrupts

The desired interrupt level to the VMEbus can be set by the jumpers provided on the VMOD-2/IMOD module for this particular purpose. The Interrupt Vector is handled by the respective PI/T requesting the interrupt.

2.5 Logic Interface

An important task performed by the logic interface is the generation of an ID byte. This built-in test feature allows an interrogation of the VMOD-2/IMOD, supplying an ID for each of the fitted piggybacks. If this is integrated into the application software, it can be used to check that any given tasks are valid for the fitted piggyback. Offsets $7F (for location A) and $FF (for location B), allow a software check of which piggybacks are fitted.

The PB-DIO3 has an ID Byte of "$FD".

Other ID Bytes are:

$EE	*PB-BIT*	*BITBUS communications controller*
$EF	*PB-DIO4*	*Digital I/O piggyback (high voltage)*
$F0	*PB-CNT*	*Counter piggyback*
$F1	*PB-DAC/2*	*D to A converter piggyback*
$EA	*PB-DAC3*	*D to A output piggyback*
$F2	*PB-DIO*	*Digital I/O piggyback*
$F3	*PB-DIN/3*	*Digital input piggyback*
$F4	*PB-ADC/2*	*A to D converter piggyback*
$EB	*PB-ADC3*	*A to D input piggyback*
$F5	*PB-CIO/2*	*Counter/I/O piggyback*
$F7	*PB-SIO4*	*Quad serial piggyback RS232*
$E7	*PB-SIO4A*	*Quad serial piggyback RS422/RS485*
$F8	*PB-DOUT*	*12 channel high voltage digital output*
$ED	*PB-DOUT2*	*16 channel high voltage digital output*
$F9	*PB-DIN2*	*Digital input piggyback*
$FB	*PB-DIO2*	*Digital I/O piggyback*
$FC	*PB-REL*	*Relay piggyback*
$FE	*PB-STP*	*Stepper motor controller piggyback*

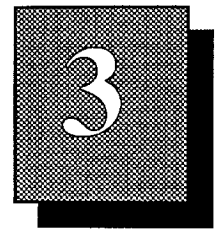
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3. CONFIGURATION

The PB-DIO3 has 16 jumpers found on the solder side of the board. The jumper settings are shown below.

Figure 3.0.0.1: PB-DIO3 Jumper Layout (Solder Side)

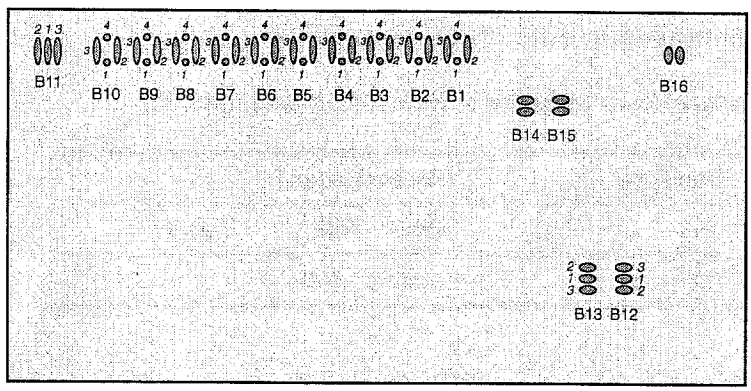


Table 3.0.0.2: PB-DIO3 Default Jumper Settings

Jumper	Setting	Board Version
B1 - B10 B11	1-3 and 2-4 1-3	Common GND Order Number 2994
B1 - B10 B11	1-2 and 3-4 1-2	Common Vcc Order Number 2995
B12	1-3	H4 --> H4E
B13	1-2	H3E --> H3
B14	set	No input filter for H1 connected
B15	set	No input filter for H3 or Tin connected
B16	set	Tout may generate interrupts

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3.1 Jumpers B1 - B11: Board Configuration

These jumpers are factory configured and are dependent on the board ordered (common GND or common Vcc).

Jumper	Setting	Description
B1 - B10 B11	1-3 and 2-4 1-2	Common GND Order Number 2994
B1 -B10 B11	1-2 and 3-4 1-2	Common Vcc Order Number 2995

3.2 Jumper B12: Handshake Line H4E Connection

This jumper determines whether H4E is connected to H4 or Tout of the MC68230.

Jumper	Setting	Description
B12	*1-3*	*H4 --> H4E* *Default*
	1-2	Tout --> H4E

3.3 Jumper B13: Handshake Line H3E Connection

This jumper determines whether H3E is connected to H3 or Tin of the MC68230.

Jumper	Setting	Description
B12	*1-2*	*H3E --> H3* *Default*
	1-3	H3E --> Tin

3.4 Jumper B14: H1 Input Filter Connection

This jumper determines an input filter network is connected to H1.

Jumper	Setting	Description
B14	*set*	*R1, C6 not assembled; no input filter for H1* *Default*
	open	R1, C6 assembled; customised input filter for H1

3.5 Jumper B15: H3 or Tin Input Filter Connection

This jumper determines an input filter network is connected to H3 or Tin.

Jumper	Setting	Description
B15	*set*	*R1, C6 not assembled; no input filter for H3 or Tin* *Default*
	open	R1, C6 assembled; customised input filter for H3 or Tin

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3.6 Jumper B16: Tout Interrupts

This jumper determines whether Tout is able to generate interrupts.

Jumper	Setting	Description	
B16	*set*	*Tout may generate interrupts*	*Default*
	open	Tout is not able to generate interrupts	

3.7 VMOD-2/IMOD Jumper Configuration

In order for the PB-DIO3 to be put into use on either the VMOD-2 or IMOD boards, the IRQ and Base Address jumper settings on these boards must be correctly configured.

For more details on these jumper configurations, please refer to the VMOD-2 or IMOD user manuals.

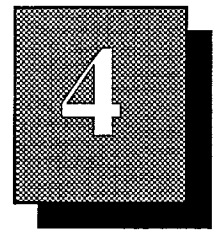
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4. PROGRAMMING

The base address of the PB-DIO2/3 in the upper piggyback position (location A) is the same as that set for the VMOD-2/IMOD used (default: $87FE2400/$F70000), whereas the base address in the lower piggyback position (location B) is +$80 of that set for the VMOD-2/IMOD (default: $87FE2480/$F70080).

4.1 PB-DIO2/3 Address Map

Address	Register Name	Register Function	Status after Reset
BASE+$01	Port General Control Register	Sets PI/T operating mode, controls handshake pins H1-H4	All bits to zero
BASE+$03	Port Service Request Register	Sets internal PI/T interrupt priorities	All bits to zero
BASE+$05	Port A Data Direction Register	Describes the bit in port A as either input or output	All bits to 1
BASE+$07	Port B Data Direction Register	Describes the bit in port B as either input or output	All bits to zero
BASE+$09	Port C Data Direction Register	Used as an output enable for port A outputs	All bits to zero
BASE+$0B	Port Interrupt Vector Register	Contains the interrupt vector numbers of the interrupt handler	Register = $0F
BASE+$0D	Port A Control Register	Steers the functions of the input port A. Contains the enable flag for port IRQ (H1 and H2)	All bits to zero
BASE+$0F	Port B Control Register	Steers the functions of the input port B. Contains the enable flag for port IRQ (H3 and H4)	All bits to zero
BASE+$11	Port A Data Register	Holds data for port A	All bits to zero
BASE+$13	Port B Data Register	Holds data for port B	All bits to zero
BASE+$15	Port A Alternate Register		
BASE+$17	Port B Alternate Register		
BASE+$19	Port C Data Register		
BASE+$1B	Port Status Register	Internal flip-flops occur in this register, designated by status bits H1S-H4S. Flip-flops returned to original state by writing a 1 to the appropriate status bit	All bits to zero
BASE+$21	Timer Control Register	Controls all timer operations	All bits to zero
BASE+$23	Timer Interrupt Vector Register	Contains the timer interrupt vector number	Register = $0F
BASE+$27 BASE+$29 BASE+$2B	Counter Preload Register High Counter Preload Register Middle Counter Preload Register Low	The counter preload registers are a group of three 8-bit registers used for storing data to be transfered to the counter	Value before RESET

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BASE+$2F BASE+$31 BASE+$33	Timer Count Register High Timer Count Register Middle Timer Count Register Low	The count registers are a group of three 8-bit addresses at which the counter can be read	Value before RESET
BASE+$35	Timer Status Register (TSR)	The timer status register contains one bit from which the zero detect status can be determined	All bits to zero
BASE+$7F	ID Register	Contains the value of the ID Byte	Register = $FD

4.1.1 Port General Control Register ($01)

This register sets the operating mode of the PI/T and controls the handshake pins H1-H4 (port IRQ or Input/Output).

Register Description

Bits	Setting	Function
7 6	0 0	Mode 0 Unidirectional 8-bit mode *Not Used*
5	0 1	H3 and H4 disabled H3 and H4 enabled
4	0 1	H1 and H2 disabled H1 and H2 enabled
3 2 1 0	x x x x	H4 H3 Bit = 1: Low = negated / High = asserted H2 Bit = 0: Low = negated / High = asserted H1

Note

After a RESET, all bits are returned to 0. This puts the PI/T into an input device mode on all ports, resulting in active outputs due to the pull-up resistor after the optocoupler.

The PB-DIO3 should be used in Mode 0 (Unidirectional 8-bit)

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Port Mode Control Summary

Mode 0 - Unidirectional 8-bit mode

Port A

Submode 00	Pin Definable Single Buffered Output
H1	Latches input data.
H2	Status/interrupt generating input, general purpose output, or operation with H1 in the interlocked or pulsed handshake mode.
Submode 01	Pin Definable Double Buffered Output
H1	Indicates data received by peripheral.
H2	Status/interrupt generating input, general purpose output, or operating with H1 in the interlocked or pulsed handshake protocols.
Submode 1x	Pin Definable Single Buffered Output
H1	Status/interrupt generating input.
H2	Status/interrupt generating input or general purpose output.

Port B

H3 and H4	Identical to port A, H1 and H2

Example

```
            .
            .
            .
        move.w    #$CF,BASE+$00      convert channel 0, bipolar
wait:   btst.b    #2,BASE+$31        EOC?
        bne.s     wait
        move.w    #$9,BASE+$00       convert channel 5, bipolar
wait2:  bfst.b    #2,BASE+$31        EOC?
        bne.s     wait2
        move.w    BASE+$00,d0        get channel 0 conversion result
            .
            .
            .
```


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4.1.2 Port Service Request Register ($03)

This register controls the double function on some of the PI/T pins and sets internal PI/T interrupt priorities.

Register Description

Bits 7 6 5 4 3 2 1 0	Function
0 0 0 1 1	Fixed when port EOC IRQs are used
	Interrupt Priority
0 0 0	H1 > H2 > H3 > H4 **Default**
0 0 1	H2 > H1 > H3 > H4
0 1 0	H1 > H2 > H4 > H3
0 1 1	H2 > H1 > H4 > H3
1 0 0	H3 > H4 > H1 > H2
1 0 1	H3 > H4 > H2 > H1
1 1 0	H4 > H3 > H1 > H2
1 1 1	H4 > H3 > H2 > H1

Note

After a reset all bits are returned to zero.

Example

```
            .
            .
            .
          move.w    #$C000,BASE+$10     read command for EPROM address offset 0
wait:     btst.b    #2,BASE+$31         End of Shift?
          bne.s     wait
          move.w    BASE+$10,d0         get EEPROM read result
            .
            .
            .
```


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4.1.3 Port A and B Data Direction Registers (Port A $05, Port B $07)

This register describes the bit in the ports A and B as either input or output. To use unidirectional 8-bit Input/Output, the port A data direction should be output (all bits are set to "1"). Port B data direction should be input (default after reset).

Note

After a reset all bits are returned to zero.

4.1.4 Port Interrupt Vector Register ($0B)

This register contain the interrupt vector numbers of the port interrupts. The upper six bits are programmable, the lower two bits are self-modifying.

Register Description

Bits 7 6 5 4 3 2 1 0	Function
	Interrupt Vectors
1 1 1 1 0 0	Example: $F0 - $F3
0 0	H1 IRQ
0 1	H2 IRQ
1 0	H3 IRQ
1 1	H4 IRQ

Note

After a reset this register contains $0F.

Example

```
            .
            .
            .
            move.w    #$C000,BASE+$10     read command for EPROM address offset 0
wait:       btst.b    #2,BASE+$31         End of Shift?
            bne.s     wait
            move.w    BASE+$10,d0         get EEPROM read result
            .
            .
            .
```


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4.1.5 Port A and B Control Registers (Port A $0D, Port B $0F)

These registers control the functions of ports A and B, and contain enable flags for port IRQ inputs H3 and H4.

4.1.6 Port A and B Data Registers (Port A $11, Port B $13)

These registers hold the data for the PI/T ports A and B.

4.1.7 Port Status Register ($1B)

With the approprate edge on pins H1 through H4 of the PI/T, internal flip-flops are set in the port status register. These flip-flops are identified by status bits H1S through H4S. The flip-flops can be returned to their original state by writing a 1 to the status bit. Use of the port IRQs requires that at the end of the IRQ service routine, bits H1S through H4S be erased in the port status register, allowing for new interrupts.

Register Description

Bits								Function
7	6	5	4	3	2	1	0	
x	x	x	x					Current levels at H1-H4 pins
				x	x	x	x	H4S, H3S, H2S, H1S status pins

Note

After a reset all bits are returned to zero.

Example

```
            .
            .
            .
            move.w    #$C000,BASE+$10     read command for EPROM address offset 0
wait:       btst.b    #2,BASE+$31         End of Shift?
            bne.s     wait
            move.w    BASE+$10,d0         get EEPROM read result
               .
               .
               .
```

4.1.8 Port C Data and Port C Data Direction Registers ($19, $09)

PC0 is used as an output enable for port A outputs. After reset, port C is input hence disabling port A outputs. To enable port A outputs, port C data direction must be set to output (at least for PC0), and bit 0 of the port C data register must be set to "0" (default on reset).

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4.1.9 Timer Control Register ($21)

This register controls all timer operations.

Register Description

Bits 7 6 5 4 3 2 1 0	Function
0 1 x	*Timer Output (Tout) Control* The Tout pin is a square wave output in run state, and moves the counter once for the passage of all zeros. In halt state, the Tout pin is set low.
0	*Zero Detect Control* After passage of all zeros in the first clock cycle, the contents of the Counter Preload Register are placed in the counter and decrementation begins.
x	Any setting.
0 0	*Clock Control* The timer's internal 8-bit prescaler is enabled. The 8 MHz onboard clock decrements the prescaler and the prescaler decrements the counter from $00 to $1F.
0 1	The Tin pin serves as a timer enable input for the timer enable flag (active high). The internal clock is used and the prescaler is enabled.
1 0	The counter is timed with the falling edge on the Tin pin. The prescaler is enabled.
1 1	The counter is timed with the falling edge on the Tin pin. The prescaler is disabled.
0	*Timer Enable* Disabled. Timer in halt state.
1	Enabled. Timer in run state.

Note

After a reset all bits are returned to zero.

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Example

```
            .
            .
            .
          move.w    #$C000,BASE+$10     read command for EPROM address offset 0
wait:     btst.b    #2,BASE+$31         End of Shift?
          bne.s     wait
          move.w    BASE+$10,d0         get EEPROM read result
            .
            .
            .
```

4.1.10 Timer Interrupt Vector Register ($23)

This register contains the timer interrupt vector number.

Note

After reset, this register contains $0F.

4.1.11 Counter Preload Registers ($27 High, $29 Middle, $2B Low)

This group of three 8-bit registers contains the beginning timer value which is carried over to the timer count register after timer enable or zero detect impulse.

Note

After reset, all bits remain unaffected.

4.1.12 Timer Count Registers ($2F High, $31 Middle, $33 Low)

The current timer count is contained in this group of registers.

Note

After reset, all bits remain unaffected.

4.1.13 Timer Status Register ($35)

Bit 0 of this register contains information regarding zero detect status. This bit is set when the counter moves from $000001 to $000000 and is reset through a direct reset, or when the timer is placed in a halt state.

Note

After reset, all bits are returned to zero.

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4.1.14 ID Register ($7F)

This register contains the ID byte, allowing automatic recognition of the piggyback fitted to the VMOD-2 or IMOD. This feature is particulary useful in a system with several piggybacks fitted. The ID byte is read using a byte read access.

PB-DIO3 ID byte = $FD

Note

After reset, all bits remain unaffected.

For more information on the ID byte, please see the ID Byte section in the Functional Description chapter.

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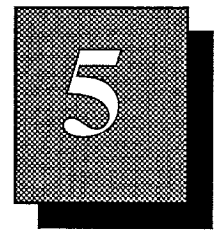
4.2 Address Map Overview

Register	Address Offset	Accessible	Affected by Reset	Affected by Read Cycle
Port General Control Register (PGCR)	$01	R/W	Yes	No
Port Service Request Register (PSRR)	$03	R/W	Yes	No
Port A Data Direction Register (PADDR)	$05	R/W	Yes	No
Port B Data Direction Register (PBDDR)	$07	R/W	Yes	No
Port C Data Direction Register (PCDDR)	$09	R/W	Yes	No
Port Interrupt Vector Register (PIVR)	$0B	R/W	Yes	No
Port A Control Register (PACR)	$0D	R/W	Yes	No
Port B Control Register (PBCR)	$0F	R/W	Yes	No
Port A Data Register (PADR)	$11	R/W	No	* *
Port B Data Register (PBDR)	$13	R/W	No	* *
Port A Alternate Register (PAAR)	$15	R	No	No
Port B Alternate Register (PBAR)	$17	R/W	No	No
Port C Data Register (PCDR)	$19	R/W	No	No
Port Status Register (PSR)	$1B	R/W	Yes	No
Timer Control Register (TCR)	$21	R/W	Yes	No
Timer Interrupt Vector Register (TIVR)	$23	R/W	Yes	No
Counter Preload Register High (CPRH)	$27	R/W	No	No
Counter Preload Register Middle (CPRM)	$29	R/W	No	No
Counter Preload Register Low (CPRL)	$2B	R/W	No	No
Timer Count Register High (CNTRH)	$2F	R	No	No
Timer Count Register Middle (CNTRM)	$31	R	No	No
Timer Count Register Low (CNTRL)	$33	R	No	No
Timer Status Register (TSR)	$35	R/W	Yes	No
Identification Byte	$41	R	No	No

* * Mode dependent

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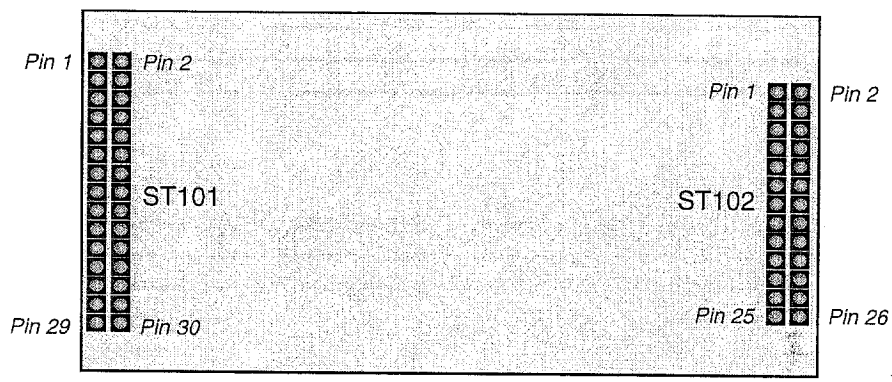


5. PINOUTS

The PB-DIO3 has two sets of connectors. ST101 is the rearmost row of 30 pins. At the front end of the piggyback there is ST102 with 26 pins.

5.1 Main Board

Figure 5.1.0.1: Board Connector Overview



5.1.1 ST101 Connector

The ST101 connector is fitted into the socket row BU1A or BU1B on the IMOD and VMOD-2 (depending if there is one or two piggybacks to be fitted) to the VMEbus interface logic.

Pin#	Signal	Pin#	Signal
1	GND	2	+5V (Vcc)
3	+12V	4	-12V
5	R/W	6	CLK
7	RESET*	8	UDTACK*
9	INTA*	10	CS*
11	INT	12	N/C
13	ID7	14	IDS0*
15	ID6	16	IAS*
17	ID5	18	IA6
19	ID4	20	IA5
21	ID3	22	IA4
23	ID2	24	IA3
25	ID1	26	IA2
27	ID0	28	IA1
29	GND	30	+5V (Vcc)

* *Active Signal Low*

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5.1.2 ST102 Connector

The ST102 connector is fitted into the socket row BU2A or BU2B on the IMOD and VMOD-2 (depending if there is one or two piggybacks to be fitted), directly to half of the 50-way VMOD-2 front panel connector, and ultimately to the user's external interfaces.

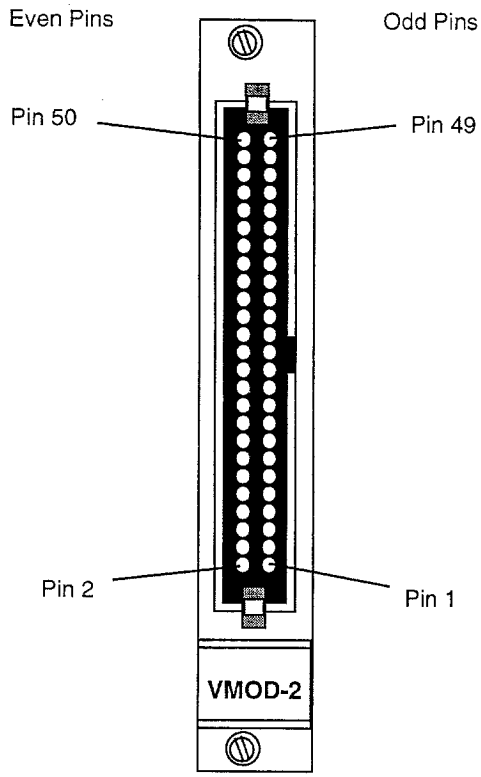
Pin#	Signal	Pin#	Signal
1	Vcc Ext.	2	Vcc Ext.
3	PA0	4	PB0
5	PA1	6	PB1
7	PA2	8	PB2
9	PA3	10	PB3
11	PA4	12	PB4
13	PA5	14	PB5
15	PA6	16	PB6
17	PA7	18	PB7
19	H1	20	H3
21	H2	22	H4
23	GND Ext. A	24	GND Ext. A
25	GND Ext. B	26	GND Ext. B

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5.2 VMOD-2/IMOD Front Panel

Figure 5.2.0.1: VMOD-2/IMOD Front Panel



Piggyback A

Pin #	Signal	Pin #	Signal
50	Ext. Vcc	49	Ext. GND B
48	PA0E	47	PB0E
46	PA1E	45	PB1E
44	PA2E	43	PB2E
42	PA3E	41	PB3E
40	PA4E	39	PB4E
38	PA5E	37	PB5E
36	PA6E	35	PB6E
34	PA7E	33	PB7E
32	H1E	31	H3E
30	H2E	29	H4E
28	Ext. GND A	27	Ext. GND A
26	Ext. Reset GND	25	Ext. Reset Vcc

Piggyback B

Pin #	Signal	Pin #	Signal
24	Ext Vcc	23	Ext GND B
22	PA0E	21	PB0E
20	PA1E	19	PB1E
18	PA2E	17	PB2E
16	PA3E	15	PB3E
14	PA4E	13	PB4E
12	PA5E	11	PB5E
10	PA6E	9	PB6E
8	PA7E	7	PB7E
6	H1E	5	H3E
4	H2E	3	H4E
2	Ext GND A	1	Ext. GND A

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The relevant half of the VMOD-2 and IMOD front panel 50-way connector (pins 1..24 for lower position and pins 27..50 for upper) assumes the relationship of PB-DIO2/3 signals and its ST102.

An optional 50-way header behind the front panel connector has an identical pin-out to the front panel connector. It is provided for applications where the flat band cable is to be routed internally, or where an alternative front panel is to be fitted and used. In some cases, cables can be routed through the systems interior i.e. to the back panel (from this optional connector) and some from the external connector on the front panel. In doing so take care not to exceed the fan out ability of the piggyback's driver circuits.

Note

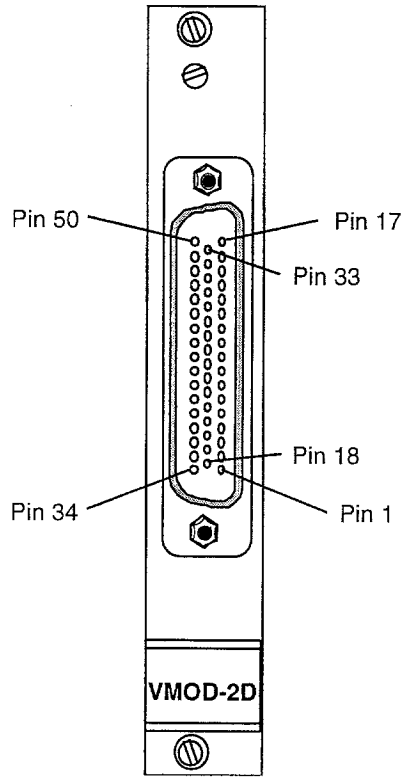
With systems that have more than one of this type of connector , or which use several VMOD-2 or IMODs with various piggybacks, it is advisable to put a drop of paint on the back of the mating connector and on the front panel of the VMOD-2 or IMOD, for correct connection. The connector splits virtually in half (pins 1-24 and 27-50) for connection to the rear piggyback location.

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5.3 VMOD-2D Front Panel

Figure 5.3.0.1: VMOD-2D Front Panel



Piggyback A

Pin #	Signal	Pin #	Signal	Pin #	Signal
50	Ext. Vcc	33	PA0E	17	Ext. GND B
49	PB0E	32	PB1E	16	PA1E
48	PA2E	31	PA3E	15	PB2E
47	PB3E	30	PB4E	14	PA4E
46	PA5E	29	PA6E	13	PB5E
45	PB6E	28	PB7E	12	PA7E
44	H1E	27	H2E	11	H3E
43	H4E	26	Ext. GND A	10	Ext. GND A
42	Ext. Reset GND			9	Ext. Reset Vcc

Piggyback B

Pin #	Signal	Pin #	Signal	Pin #	Signal
		25	Ext. Vcc		
41	Ext. GND B	24	PB0E	8	PA0E
40	PA1E	23	PA2E	7	PB1E
39	PB2E	22	PB3E	6	PA3E
38	PA4E	21	PA5E	5	PB4E
37	PB5E	20	PB6E	4	PA6E
36	PA7E	19	H1E	3	PB7E
35	H3E	18	H4E	2	H2E
34	Ext. GND A			1	Ext. GND A

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5.4 VMOD-2 / VMOD-2D Pinout Relationship

Piggyback A

Signal	VMOD-2 Pin #	VMOD-2D Pin #	Signal	VMOD-2 Pin #	VMOD-2D Pin #
Ext Vcc	50	50	Ext. GND B	49	17
PA0E	48	33	PB0E	47	49
PA1E	46	16	PB1E	45	32
PA2E	44	48	PB2E	43	15
PA3E	42	31	PB3E	41	47
PA4E	40	14	PB4E	39	30
PA5E	38	46	PB5E	37	13
PA6E	36	29	PB6E	35	45
PA7E	34	12	PB7E	33	28
H1E	32	44	H3E	31	11
H1E	30	27	H4E	29	43
Ext. GND A	28	10	Ext. GND A	27	26

Signal	VMOD-2 Pin #	VMOD-2D Pin #	Signal	VMOD-2 Pin #	VMOD-2D Pin #
Ext. Reset GND	26	42	Ext Reset Vcc	25	9

Piggyback B

Signal	VMOD-2 Pin #	VMOD-2D Pin #	Signal	VMOD-2 Pin #	VMOD-2D Pin #
Ext Vcc	24	25	Ext. GND B	23	41
PA0E	22	8	PB0E	21	24
PA1E	20	40	PB1E	19	7
PA2E	18	23	PB2E	17	39
PA3E	16	6	PB3E	15	22
PA4E	14	38	PB4E	13	5
PA5E	12	21	PB5E	11	37
PA6E	10	4	PB6E	9	20
PA7E	8	36	PB7E	7	3
H1E	6	19	H3E	5	35
H2E	4	2	H4E	3	18
Ext GND A	2	34	Ext GND A	1	1

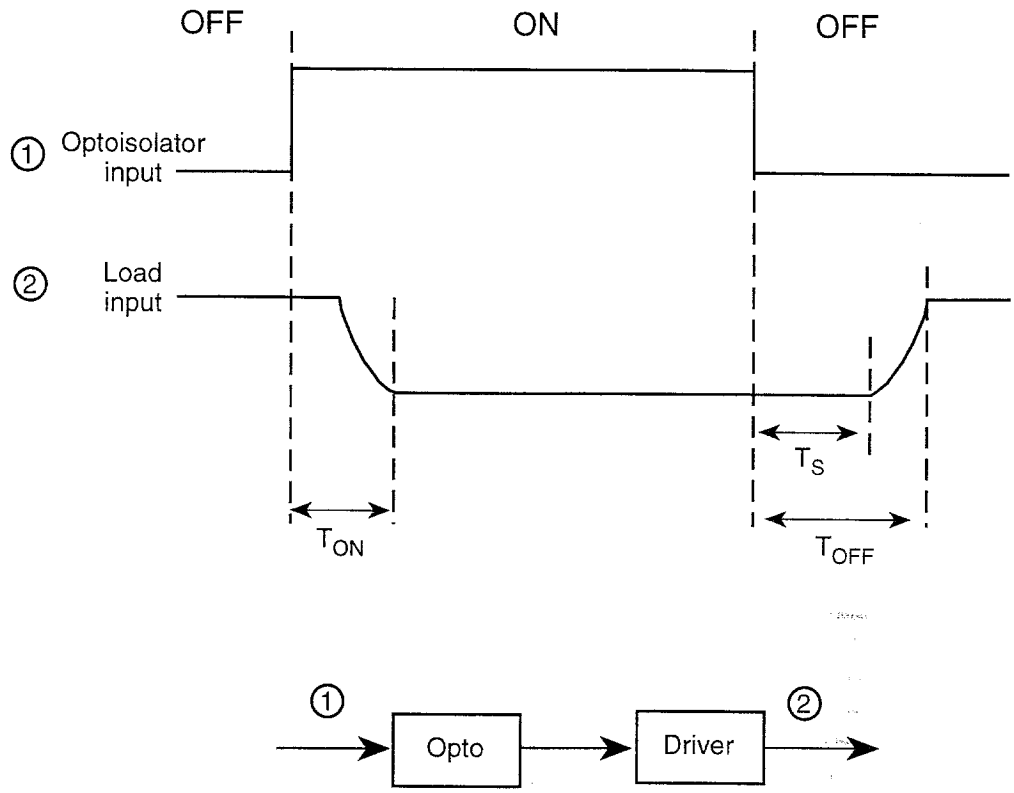
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5.5 Switching Behavior

The Table below provides some typical values for turning the output channel on and off. Similar values also apply turning the input on and off (port B).

Figure 5.5.0.1: Switching Behaviour



R_L	T_S	T_{ON}	T_{OFF}
470Ω	40µs	3.5µs	140µs
220Ω	25µs	3.5µs	80µs

5.6 Power On/Off

During power up, the output drivers are tristate and therefore the optocouplers are turned off. In addition, if the system power is turned off, the optocoupler diode is off.

Enabling the output drivers is performed by setting PC0 as output to "0".

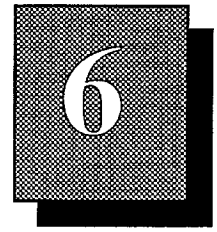
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6. INSTALLATION

6.1 VMEbus Connection

Caution!

Before installing or removing any VMEbus boards, always turn off the power to the bus and any external peripherals.

Inserting or removing modules, while the power is on, could result in damage to the VME module or peripherals interface.

Please refer to VMOD-2/IMOD user's manual for details on installing or removing.

Note

The VMEbus backplane uses automatic daisy-chaining (no BG/IACK jumpers), therefore does not need to be configured by the user.

For users with VBP backplanes, please refer to the *VBP Users Manual* for configuration information.

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6.2 Installing the PB-DIO3

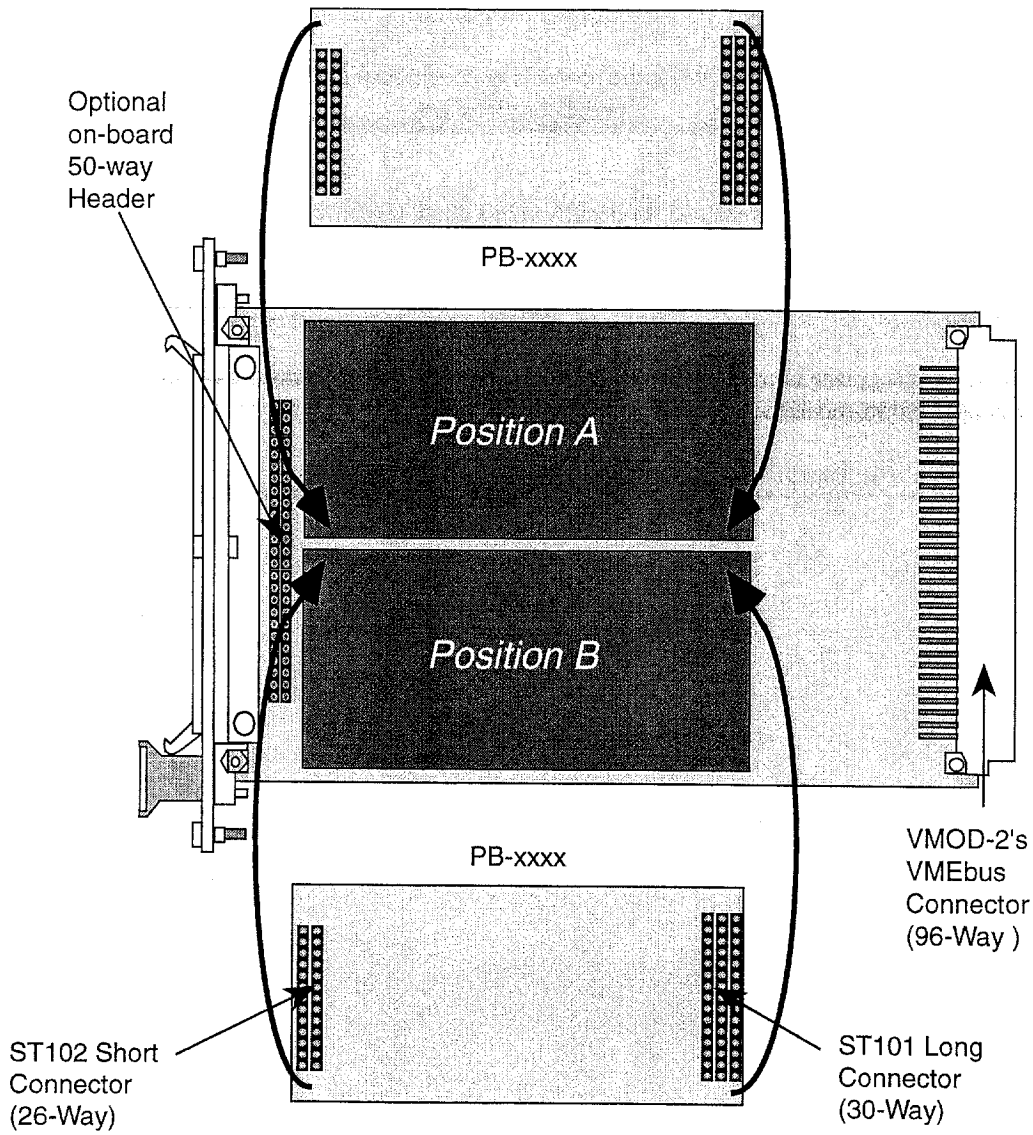
The PB-DIO3 may be plugged into any free piggyback position (A or B) on the VMOD-2 or IMOD. Please ensure the correct location before fitting.

Note

1. One connector on the PB-DIO2/3 has fewer pins than the other.

2. ST101 has two-rows which are to fit the front two-rows of the VMOD-2 amd IMOD three-row interface socket. Take care to ensure that the piggyback is in its correct position.

Figure 6.2.0.1: PB-DIO3 Installation Overview



Mechanical fastening and support is provided by the two interface connectors. In addition, the piggyback can be attached to the motherboard by screws and stand-off pillars at the front end of the piggyback, and at the corresponding location on the VMOD-2 and IMOD at the two holes provided for this purpose.

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6.3 General Notes for Using the System

Having designed a system, it is necessary to keep it in good working order. The three biggest risks to the system occur when:

- Connecting peripherals, disk-drives, printers, terminals and external power sources;
- Adding or changing modules, address settings and locations, etc;
- Becoming complacent and not referring to the manuals when altering or adding modules.

These risks can be reduced by:

- Checking the electrical compatibility of all devices to be connected;
- Ensuring that they are powered from the same mains supply branch (phase) and grounded to the same reference point;
- Shutting down all power before making or breaking any connections to modules or attachments to the system, including power to the peripherals;
- Observing sensible static protection procedures before handling any modules, piggybacks or memory IC's;
- Keeping all manuals available by the system and refer to them when required.

Some tips are:-

PEPCards are not over sensitive to static, but it is generally advisable to observe normal antistatic procedures.

When configuring the module, it should not be taken out of the original packing unless necessary. The clear packs can be opened and the jumpers set, piggybacks added, etc. without removing the card. This prevents inadvertent shorting of any on-board devices.

When inserting modules into a system, the power should be turned off and the mains lead not removed! The ground wire prevents the rack floating with dangerous static voltages, which could destroy circuits on the module being inserted.

The front panel of the module and the shell of the connector should be touched to any part of the rack before fitting. This discharges any static from the user.

Modules should not be pulled straight out of a rack and the back of the front panel checked to see if there are cables to unplug (such as the VSBC-1's 40-pin parallel on-board headers). Any leads should be disconnected from a module before unscrewing the front panel and removing from the rack. It should be ensured that, when fitted, these cables have enough play to allow the modules to be removed far enough to detach these cables. Modules should be put into the rack before connecting any front-panel connectors.

The "pulled" jumpers should be parked on to one of the pins they would normally bridge, so they can be quickly replaced.

It should be remembered to check the mains input voltage selector switch before installing or using any PSU!

A record should be kept of settings and a copy forwarded with any board returned to PEP for failure analysis.

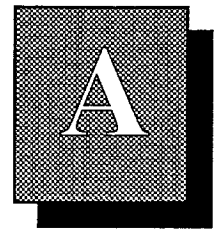
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APPENDIX A. EXAMPLES

WARNING!

The programs found in this chapter are only examples!
They may or may not run on your system, depending on your system configuration.

A.1 Initialisation of Port A

```
move.b      #0, pgcr        Select mode 00
move.b      #$18, psrr      Enable port IRQ
move.b      #$FF, paddr     Set port A to output
move.b      #$F0, pivr      Install IRQ vector
move.b      #$40, pacr      Submode 01
move.b      #1, pcddr       Set PC0 to output
move.b      #0, pcdr        Write "0" to PC0
move.b      #$55, padr      Output
```

A.2 Initialisation of the Timer

```
move.b      #$F0, tivr      Timer IRQ vector
move.b      #$10, cprh      Timer preload
move.b      #$10, cprm      Timer preload
move.b      #$FF, cprl      Timer preload
move.b      #$01, tcr       Start timer
```


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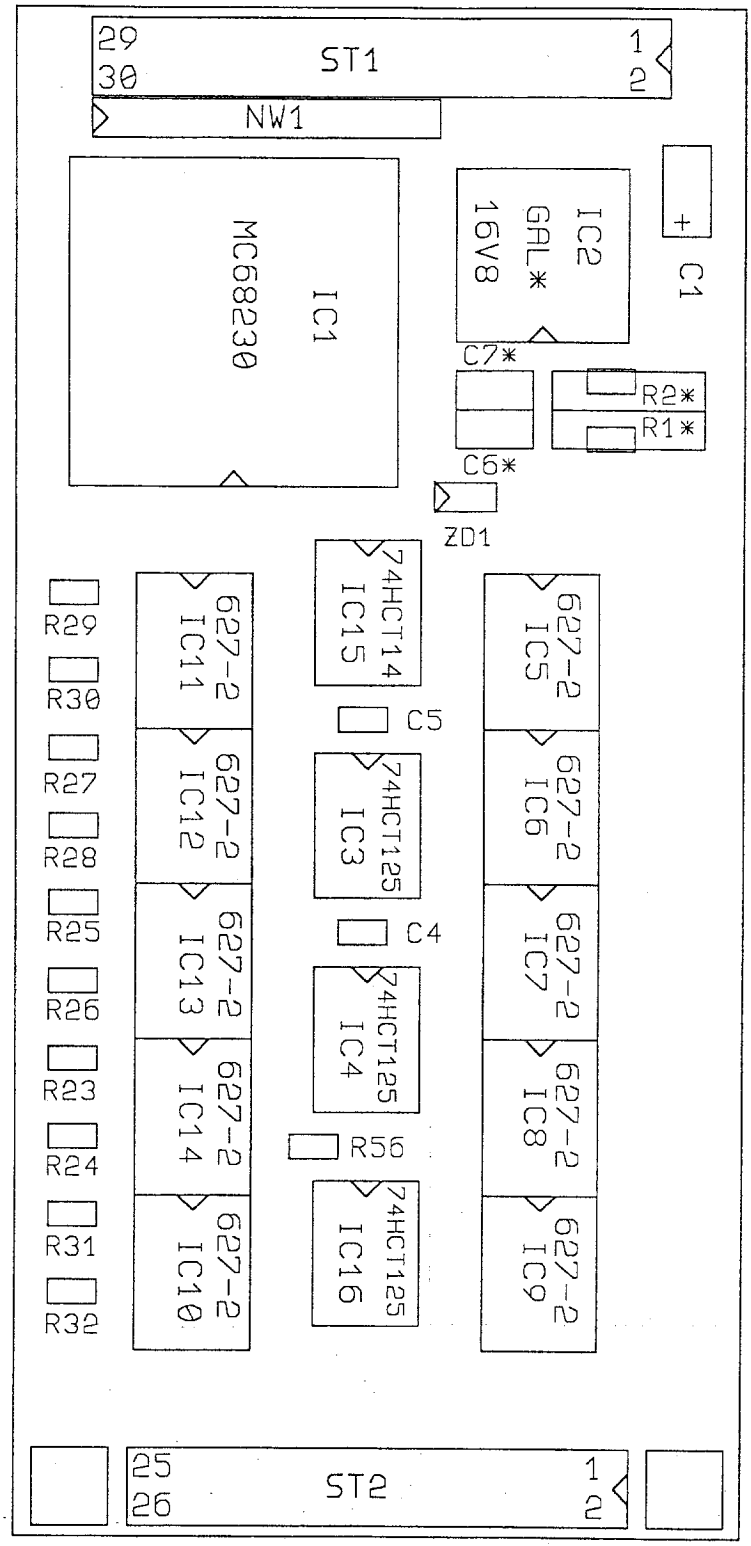
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* entsprechend Bestell-Nr. /according to order-no 523-23x

B1 - B11 auf L-Seite / on L-side

B-Seite/ b-side

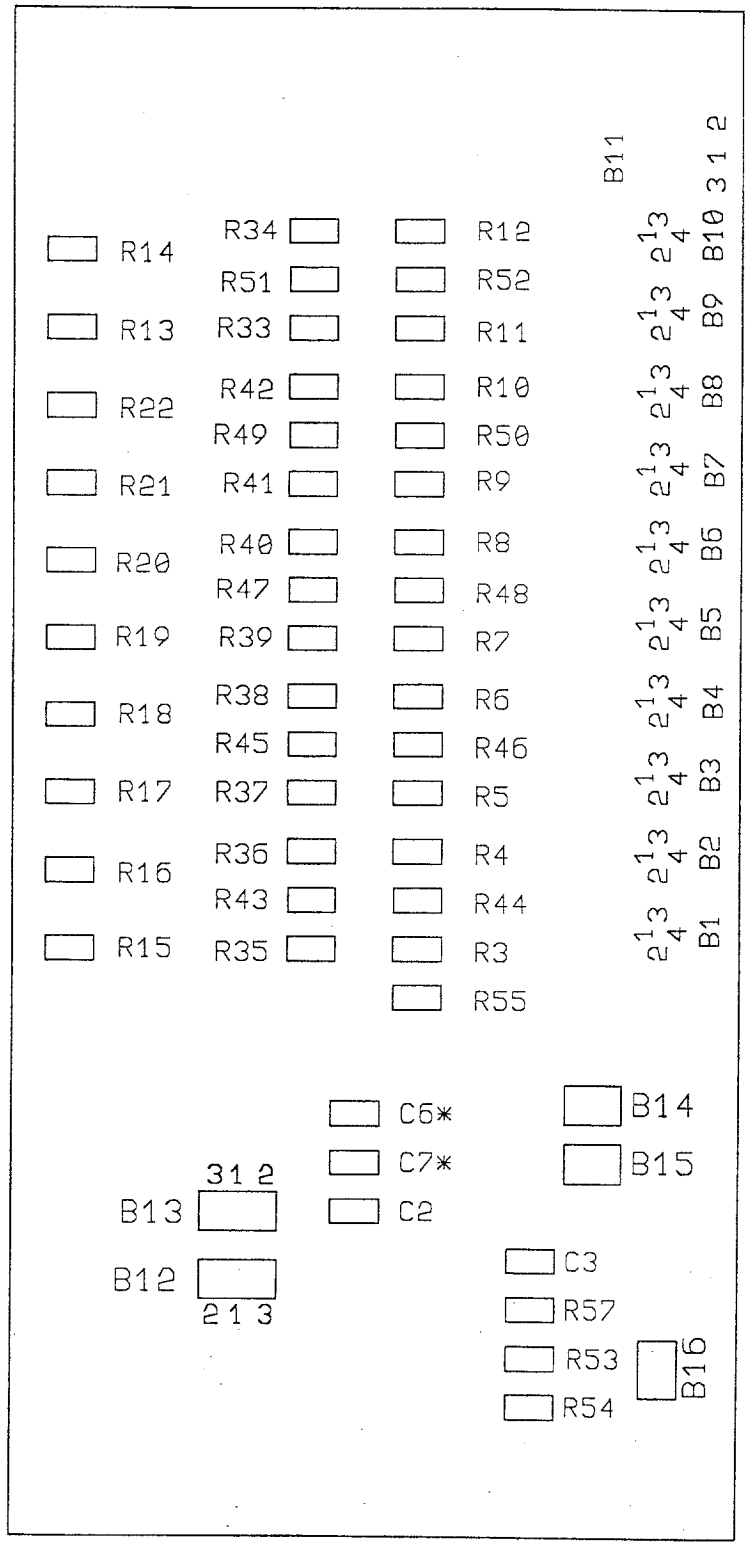
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	Datum: Apr 18, 1994	31.112-1110.1 IND.02
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ORIGINAL

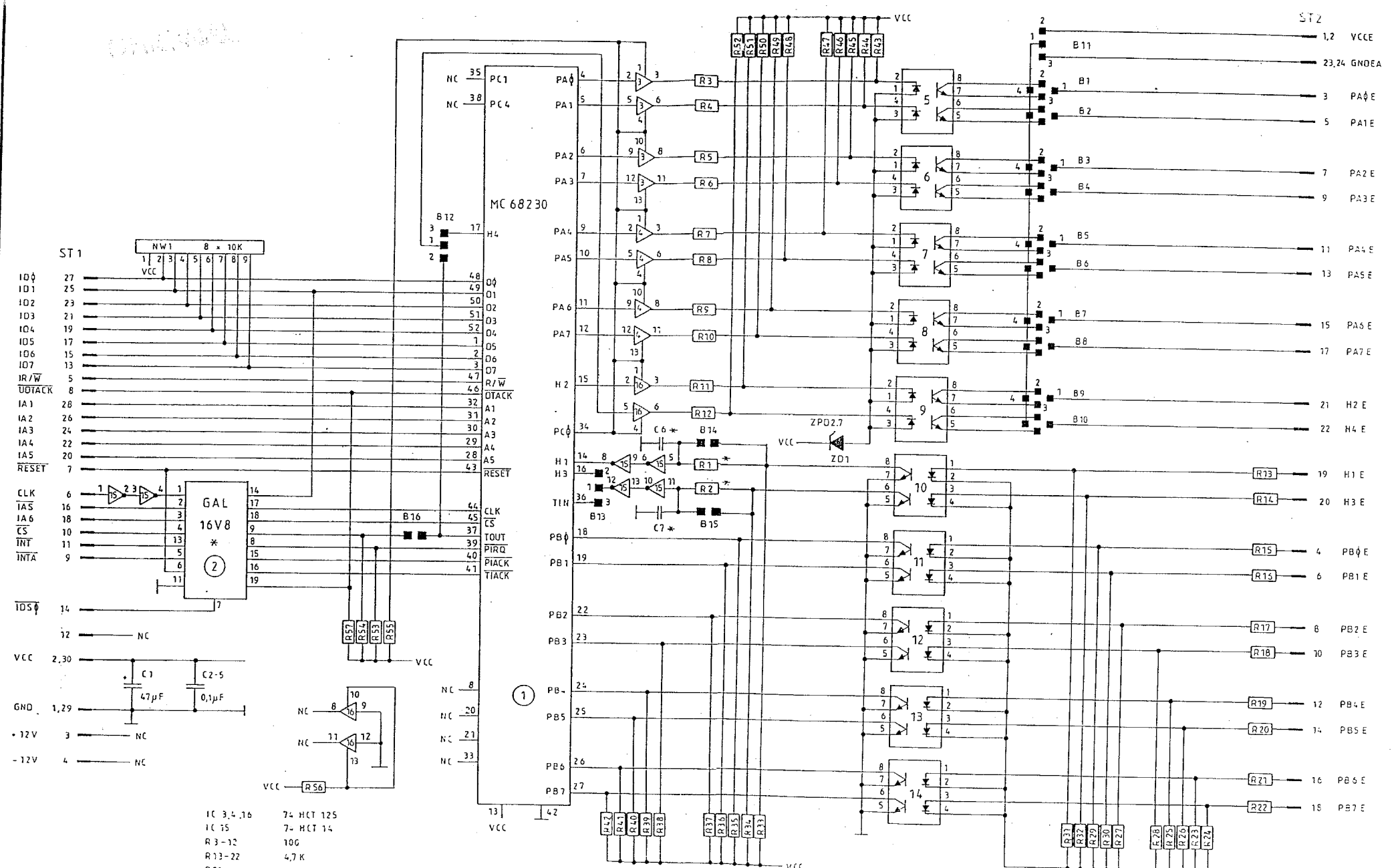
L-Seite/ l-side



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IC 3,4,16	74 HCT 125
IC 15	74 HCT 14
R3-12	10Ω
R13-22	4,7 K
R23-32	1K
R33-42	470
R43-52	68Ω
R53-57	10K
IC5-14	TLP 627-2

* entspr. Bestell-Nr. / according to order-no 523-23x

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