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CPC324

24-Port T1/E1/J1 Edge Processor

Hardware Manual

Performance Technologies
205 Indigo Creek Drive
Rochester, NY 14626 USA
585.256.0248
support@pt.com

www.pt.com

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126P0446.41	June 26, 2008	Added Interpreting Sensor Events topic. Enhanced SW3 Settings documentation. Updated manual format.
126P0446.42	June 12, 2009	Corrected SW3 Settings documentation. Updated RoHS/Non-RoHS Versions. Removed references to non-RoHS parts. Removed references to 8-port RTM324. Updated manual format.

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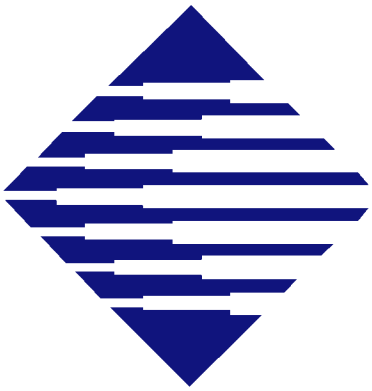
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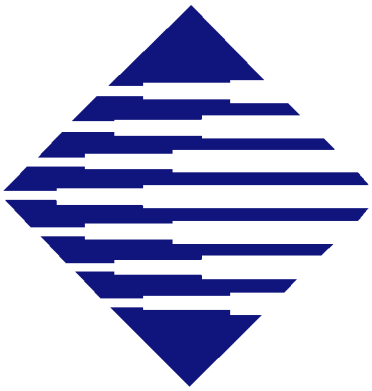
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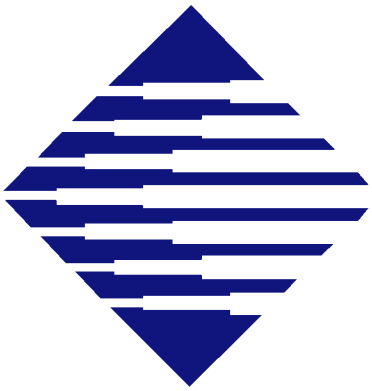
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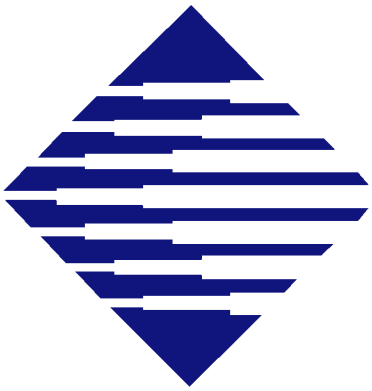
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Chapter

1

About This Guide

Overview

This guide describes Performance Technologies, Inc. CPC324 24-Port T1/E1/J1 Edge Processor. Here is a brief description of the information that you will find in this manual:

Chapter 2, “Introduction,” on page 17 provides an overview of the CPC324 as well as an in-depth product diagram for visualization of product workflow. It also contains detailed information regarding controllers, buses, interfaces and system notification specifics.

Chapter 3, “Getting Started,” on page 57 contains detailed information on unpacking and installing the CPC324 and the RTM324 into the CompactPCI Chassis.

Chapter 4, “Reset,” on page 77 discusses the various reset types and reset sources on the CPC324.

Chapter 5, “Connectors,” on page 79 describes PTMC connections and pinouts, Ethernet pin assignments and CompactPCI connections.

Chapter 6, “Rear Transition Module,” on page 97 includes functional descriptions of the two versions of the RTM324. It also includes switch and connector information for the RTMs as well as cabling information and a discussion about the 19” Break Out Box.

Chapter 7, “References,” on page 115 lists standards and specifications pertinent to the CPC324 and provides links to datasheets for components used on the CPC324.

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In February 2003, the European Union issued *Directive 2002/95/EC* regarding the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment (RoHS) and *Directive 2002/96/EC* on Waste Electrical and Electronic Equipment (WEEE).

This product is compliant with *Directive 2002/95/EC*. It may also fall under the *Directive 2002/96/EC*.

Performance Technologies' complete position statements on the RoHS and WEEE Directives can be viewed on the Web at: http://pt.com/page/about-us/ehsms/.

RoHS/Non-RoHS Versions

This manual covers only the RoHS version of the CPC324. The following table lists the RoHS and Non-RoHS related part numbers.

Item	RoHS Part Number	Non-RoHS Part Number
CPC324	Model PT-CPC324-11964	Model PT-CPC324-11679
RTM324	Model PT-RTM324-11965	Model PT-RTM324-11743
Console Port Cable	Model ACC324-11977	Model ACC324-11815
19” Break Out Box	Model ACC324-11967	Model ACC324-11747
RJ21 to RJ21 Cable	Model ACC324-11968	Model ACC324-11745

Text Conventions

This guide uses the following conventions:

Convention	Used For
`Monospace font`	Monospace font represents sample code.
Bold font	Bold font represents: • paths • file names • UNIX commands • user input
Italic font	Italic font represents: • notes that supply useful advice • supplemental information • referenced documents
$ARCH	Indicates the processor architecture of the target, currently this is ppc, mips, arm and i386.
Overline	An overline is used to represent an Active Low signal.
< >	Angle brackets are used to represent variables (for example, file names, passwords).
ALL CAPITALS	All capital letters are used for the keys on your keyboard (for example, the ENTER, the TAB, and the SPACEBAR keys).

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Chapter

2

Introduction

Overview

This chapter provides an introduction to the CPC324 24-Port T1/E1/J1 Edge Processor. It includes a product definition, Figure 2-1, “CPC324 Front Panel,” on page 19, a list of product features, Figure 2-2, “CPC324 Functional Block Diagram,” on page 21 and a description of each functional block.

Unpacking, initial blade configuration and other setup information are provided in Chapter 3, “Getting Started,” on page 57.

The following topics are covered in this chapter:

- “Product Description,” on page 17
- “CPC324 Features,” on page 20
- “CPC324 Functional Blocks,” on page 21

Product Description

The CPC324 PICMG 2.16 CompactPCI® blade is a high-density, 24-span, T1/E1/J1 voice and data platform intended for data communication processing and voice applications in PSTN and IP telephony systems.

The CPC324 provides a comprehensive, high-density solution for processing HDLC channels for internetworking applications such as:

- Frame Relay
- ISDN D-channel signaling
- X.25
- Signaling System 7 (SS7)

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- DXI
- ISUP
- LAN/WAN data transport

The main processor, an AMCC 440GX, runs at 800 MHz. The AMCC 440GX is an embedded RISC processor with integrated modules that provide interfaces for:

- The local 33 MHz, 32-bit PCI bus
- Dual UARTs
- 10/100/1G data rate Ethernet RGMII
- An on-chip Double Data Rate (DDR) SDRAM controller

On-board memory consists of:

- 512 MB of 166 MHz DDR SDRAM with ECC
- 8 MB boot flash
- 128 MB of application flash

A 10/100/1G unmanaged Ethernet switch interfaces to the AMCC 440GX's RGMII Ethernet ports. The Ethernet switch provides seven ports of 10/100/1G Base-T routing and connectivity to:

- The PICMG 2.16 CompactPCI packet switching backplane
- Two PTMC mezzanine slots
- RJ45 connectors on the front and rear panel faceplates

Three IDT 82P2288 T1/E1/J1 octal transceivers integrate eight universal T1/E1/J1 Line Interface Units (LIU) and eight framers in a single monolithic device. Egress and ingress spans to and from the network side are coupled into the transceiver's receive and transmit ports and pass through the built-in impedance terminations. In T1/J1 mode, the recovered data and clock of each link can be configured in the following formats:

- Super Frame (SF)
- Extended Super Frame (ESF)
- T1 Digital Multiplexer (DM)
- Switch Line Carrier - 96 (SLC-96)

A Zarlink MT90866 digital timeslot switch provides switching capacities of:

- 4,096 x 2,432 channels between the H.110 backplane and the CPC324's local streams
- 2,432 x 2,432 channels among local streams
- 2,048 x 2,048 channels among backplane streams

Minimal host supervision is required for the three Mindspeed CN8478 eight-port Multichannel Synchronous Communications Controllers (MUSYCC) that manage linked lists of channel data buffers in host memory by performing Direct Memory Access (DMA) on HDLC channels. MUSYCC operates at Layer 2 of the Open Systems Interconnection (OSI) protocol reference model. Each MUSYCC interfaces to 256 TS data streams from the Zarlinks local TDM side. Processed data is transferred across the 32-bit local PCI bus to system memory.

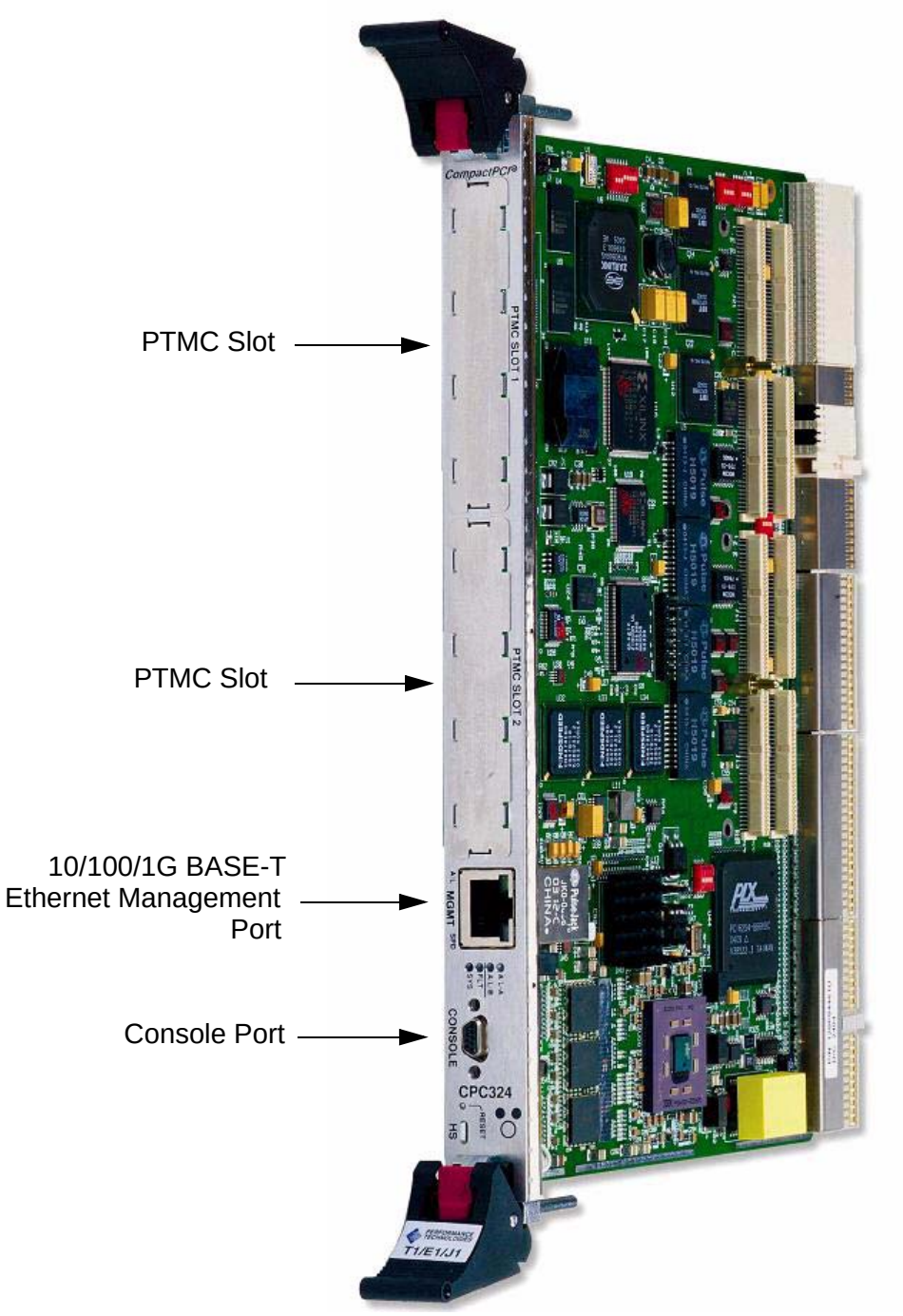
Two sets of PTMC slot locations are provided for two single or one dual PTMC (PCI Telecom Mezzanine Card) module. See Figure 2-1, "CPC324 Front Panel," on page 19 for locations. The PTMC interfaces are identical and support the following under PICMG 2.15 PTMC configuration 2:

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- 32-bit PCI
- H.110 style TDM
- RMII
- 10/100/1G Ethernet

The 10/100/1G Ethernet is pinned on J4 with pin assignments defined the same as PTMC Configuration 5. See Chapter 5, “Connectors,” on page 79 for more information.

Figure 2-1: CPC324 Front Panel



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CPC324 Features

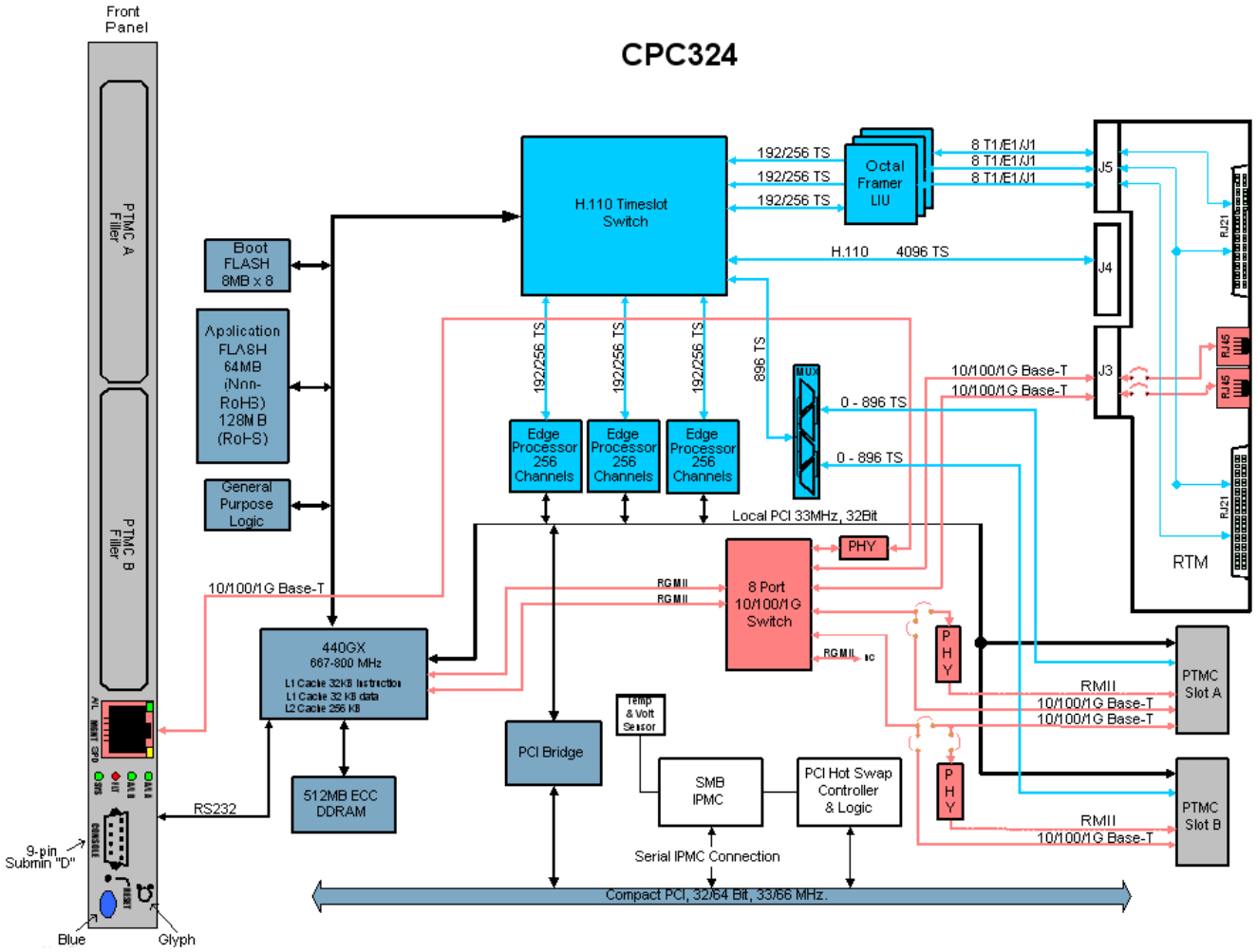
- PIC Industrial Computers Manufactures Group Implementations:
  - PICMG 2.0 CompactPCI
  - PICMG 2.1 Hot Swap
  - PICMG 2.5 Computer Telephony
  - PICMG 2.9 System Management
  - PICMG 2.15 PTMC Carrier
  - PICMG 2.16 CompactPCI Packet Switching Backplane (CPSB) Node Card. 24-Port (Span), T1/E1/J1 Edge Processor high-throughput communications controller for terminating voice or synchronous link-layer applications
- Rear Transition Module (RTM) faceplate provides:
  - 24 T1/E1/J1 port connections on two 50-pin, high-density telco connectors (12 ports on each connector)
  - Two 10/100/1G Ethernet CPSB node connections optionally available on RJ45 connectors
  - An alternate RTM with eight T1/E1/J1 port connections on RJ48 connectors is available
- AMCC 440GX PowerPC processor core operating at 800 MHz:
  - With 32 KB Instruction and Data caches
  - 256 MB L2 Cache
  - TCP/IP Acceleration Hardware (TAH)
  - Double Data Rate (DDR) Synchronous DRAM interface (166 MHz)
  - RGMII Ethernet 10/100M1G bps full duplex interface
  - Serial port (16750 compatible UART)
  - Dual PCI bus interfaces
- Memory:
  - 512 MB of 166 MHz DDR DRAM with 8-bit ECC
  - 128 MB application flash
  - 8 MB boot PROM
  - Integrated 8-port 10/100/1G Base-T Ethernet switch
  - Multichannel Synchronous Communications Controller (MUSYCC) supports OSI layer 2
  - General purpose ISO3309 HDLC
  - Signaling System Seven (SS7)
  - Local PCI bus interface
- Time Division Multiplexed (TDM) switch:
  - H.110 Compliant
  - 2,432 x 2,432 non-blocking TDM switching among local streams
  - 4,096 x 2,432 blocking TDM switching between backplane and local streams
  - 2,048 x 2,048 non-blocking TDM switching among backplane streams
  - H.110 primary master, secondary master, and slave

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CPC324 Functional Blocks

Figure 2-2, “CPC324 Functional Block Diagram,” presents the functional blocks of the CPC324. The topics following the figure provide an overview of each functional block found on the CPC324.

Figure 2-2: CPC324 Functional Block Diagram



- “Introduction,” on page 22
- “AMCC 440GX,” on page 23
- “Local PCI and CompactPCI Buses,” on page 25
- “Memory Components,” on page 26
- “SPI Interface,” on page 26
- “Gigabit Ethernet Switch,” on page 27
- “T1/E1/J1 Framers and LIU,” on page 30
- “TDM Clock Distribution and Control,” on page 33
- “H.110 Switch,” on page 38
- “T1/E1/J1 Layer 2 Communications Controller,” on page 41
- “Zircon UL Peripheral Monitor,” on page 44

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- “ADM1026 Peripheral and Management Controller,” on page 49
- “Serial EEPROM,” on page 50
- “IPMI Commands,” on page 50
- “Sensors,” on page 53
- “LED Visual Indicators,” on page 54

Introduction

The CompactPCI CPC324 is a full-featured, 24-port, T1/E1/J1 telecommunications adapter and time-division access controller with three T1/E1/J1 octal transceivers and ECTF H.110 time division multiplex (TDM) switch. The CPC324 also features an on-board Ethernet switch that supplies CompactPCI 2.16 connectivity to the backplane for the AMCC 440GX processor and the dual PTMC sites.

The CPC324 is composed of a main CompactPCI blade and a rear I/O transition module (RTM).

The main blade contains all of the active components, including the T1/E1/J1 Line Interface Unit (LIU) and framers, ECTF H.110 controller, CompactPCI hot-swap bus interface, AMCC 440GX processor, memory and Ethernet switching. T1/E1/J1 digital bit streams enter and exit through the RTM.

The RTM provides passive components, including line protection, galvanic protection, and external Ethernet connectivity if desired. A pair of RJ21 Telco connectors can be connected to a break-out box that provides the receiver/transmitter metallic connectors (RJ48C) for customer interface connections. For more information about the RTM, see Chapter 6, “Rear Transition Module,” on page 97.

The CPC324 is a universal I/O blade, with no key on J1, accepting either 5V or 3.3V for the PCI I/O signals.

Three on-board octal T1/E1/J1 LIU and framers receive and transmit framed, serialized T1/E1/J1 bit streams, recover timing information, and demultiplex the T1/E1/J1 data directly to the DS0 level. The result is six streams of 96/128 T1/E1/J1 DS0 timeslots that may be terminated in several fashions, including termination to the:

- CompactPCI bus
- H.110 bus
- PTMC sites
- CPU main memory

In the receive direction, the LIU and framers accept T1/E1 or J1 bipolar signals, perform equalization, convert the signals into binary digital data streams, receive frame synchronization, data recovery, frame overhead extraction, and provide data connection paths to the various on-board terminating interfaces via the H.110 switch.

In the transmit direction, the LIU and framers accept digital data from one of the terminating interfaces via the H.110 switch. The LIU and framers perform frame generation overhead insertion and convert the digital clock and data to the appropriate wave shapes for transmission as bipolar T1/E1 or J1 streams.

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The H.110 switch interfaces the T1/E1/J1 LIU and framers with the AMCC 440GX's main memory through one of three Mindspeed multichannel communication controllers. The switch can also route the TDM data to or from the two on-board PTMC sites. The TDM switch is fully compliant with the ECTF H.100/H.110 specification and has no restrictions to the possible types of switching connections that can be made. Each local timeslot can be assigned to any of the possible 4096 H.110 external timeslots or reassigned to any other local timeslot.

The hot-swap CompactPCI interface provides PCI bus initiator/target mode capability of 32/64-bit data accesses at 33/64 MHz bus rates. The hot-swap controller supports high availability, which implements a high degree of control and allows orderly insertion and extraction of the CPC324.

The on-board Ethernet switch allows the AMCC 440GX CPU to be interconnected with the dual on-board PTMC sites and the external CompactPCI 2.16 backplane connections. An option on the RTM allows the 2.16 connections to be routed out the RTM's face plate to allow connection to external connections. The CPC324 also supports an Ethernet management port on its front panel.

AMCC 440GX

The AMCC 440GX is a Power PC processor. It is used for Gigabit Ethernet, I2O Messaging Units, and TCP/IP acceleration hardware.

AMCC 440GX Local PCI Bus

The AMCC 440GX PCI interface allows connection of local on-board PCI devices to the PowerPC processor and local memory. This interface is designed to version 2.3 of the PCI specification and supports 32 bit, 33 MHz transfers. The AMCC 440GX features three on-chip buses:

- Processor Local Bus (PLB)
- On-Chip Peripheral Bus (OPB)
- Device Control Register Bus (DCR)

The high performance, high bandwidth cores such as the PowerPC 440 processor core, the DDR SDRAM memory controller, and the PCI bridge connect to the PLB. The OPB hosts lower data rate peripherals. The daisy-chained DCR provides a lower bandwidth path for passing status and control information between the processor core and the other on-chip cores.

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Local CompactPCI Bus Devices

The AMCC 440GX processor performs PCI configuration cycles to assign addresses to its devices. This is implemented by connecting the higher order PCI address/data bits to the IDSEL inputs of the devices. This is summarized in Table 2-1, “Local Bus Devices,” below.

Table 2-1: Local Bus Devices

AD bit	Device	Device Number
S_PCI_AD17	CN8478 “A”	1
S_PCI_AD18	CN8478 “B”	2
S_PCI_AD19	CN8478 “C”	3
S_PCI_AD20	PCI6254	4
S_PCI_AD21	PTMC “A” {idsel}	5
S_PCI_AD22	PTMC “A” {idselB}	6
S_PCI_AD23	PTMC “B” {idsel}	7
S_PCI_AD24	PTMC “B” {idselB}	8
S_PCI_AD25	AMCC 440GX	9

440GX DDR SDRAM Controller

The DDR_SDRAM memory controller supports Double Data Rate (DDR) SDRAMs. It can provide 32- or 64-bit interface to SDRAM memory with optional Error Checking and Correction (ECC). The controller supports page mode operation with bank interleaving and maintains up to four open pages. The controller supports up to four 512 MB logical banks in limited configurations, providing memory up to 2GB. Global memory timings, address and bank sizes, and memory addressing modes are programmable. System power can be reduced by placing the DDR_SDRAM controller in sleep and/or self-refresh mode.

CPU Interrupts

Table 2-2, “AMCC 440GX Processor Interrupts,” lists the interrupts to the AMCC 440GX Processor.

Table 2-2: AMCC 440GX Processor Interrupts

Interrupt Request	Source
IRQ00	MUSYCC “A”
IRQ01	MUSYCC “B”
IRQ02	MUSYCC “C”
IRQ03	Framer “A”
IRQ04	Framer “B”
IRQ05	Framer “C”
IRQ06	PRI FAIL
IRQ07	SEC FAIL
IRQ08	FAILA
IRQ09	FAILB

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Table 2-2: AMCC 440GX Processor Interrupts (Continued)

Interrupt Request	Source
IRQ10	BCM5388
IRQ11	Not used (pin shared with PCI Request)
IRQ12	Not used (pin shared with PCI Grant)
IRQ13	PMC INT A 1
IRQ14	PMC INT A 2
IRQ15	PMFAULT
IRQ16	PLX S INT A
IRQ17	TOD

Peripheral Timing

- Peripheral clock frequency is 1/4 of the MemClk (DDR Clock) frequency
- DDR333, which has a 166.66 MHz clock, results in a 41.6 MHz peripheral clock
- DDR266, which has a 133.33 MHz clock, results in a 33.3 MHz peripheral clock
- All peripheral timing is based on the peripheral clock timing
- Chips selects are assigned according to access types

Local PCI and CompactPCI Buses

A 32-bit, 33 MHz local PCI bus provides connectivity between the AMCC 440GX processor, the MUYSCC, the two PTMC slots, and the PLX PCI6254 bridge chip. The AMCC 440GX is the local bus controller. The PLX PCI6254 provides bus arbitration.

The PLX PCI6254 bridge chip is also the interface to the 32/64-bit, 33/66 MHz CompactPCI bus. Hot swap is supported.

CompactPCI Bus Interface

The full 64-bit CompactPCI Address/Data Bus (AD) is connected to the PLX PCI6254 to support 32/64-bit transfers. The control signals are connected per the industry standard. Bus operation at 33 or 66 MHz is supported, as determined by backplane signal P1_66EN.

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Memory Components

Boot Flash

The CPC324 has one 8 MB boot flash device, an Intel StrataFlash 28F640J3-120. This part is 64 Mb, organized 8 M x 8, with 120 ns access time. Boot flash is supported on the peripheral bus only. The PCI bus boot option is not supported and expansion ROM is disabled on the PCI bus.

Application Flash

The CPC324 has two 64 MB application flash devices, using Spansion S29L512N10 parts. These parts are 512 Mb, organized 64 M x 8, with 100 ns access time. Application flash starts at base address 0x1_3000_0000 and supports 128 MB.

SDRAM

The CPC324 has 512 MB of DDR SDRAM with 8-bit ECC, made up of ten Micron MT46V32M16FN-6 parts. These parts are 512 Mb, organized as 32M x 16, running at 166 MHz, with CAS Latency =2.5. This memory is organized as two external banks (chip selects). Each bank is 64 bits wide with ECC.

SPI Interface

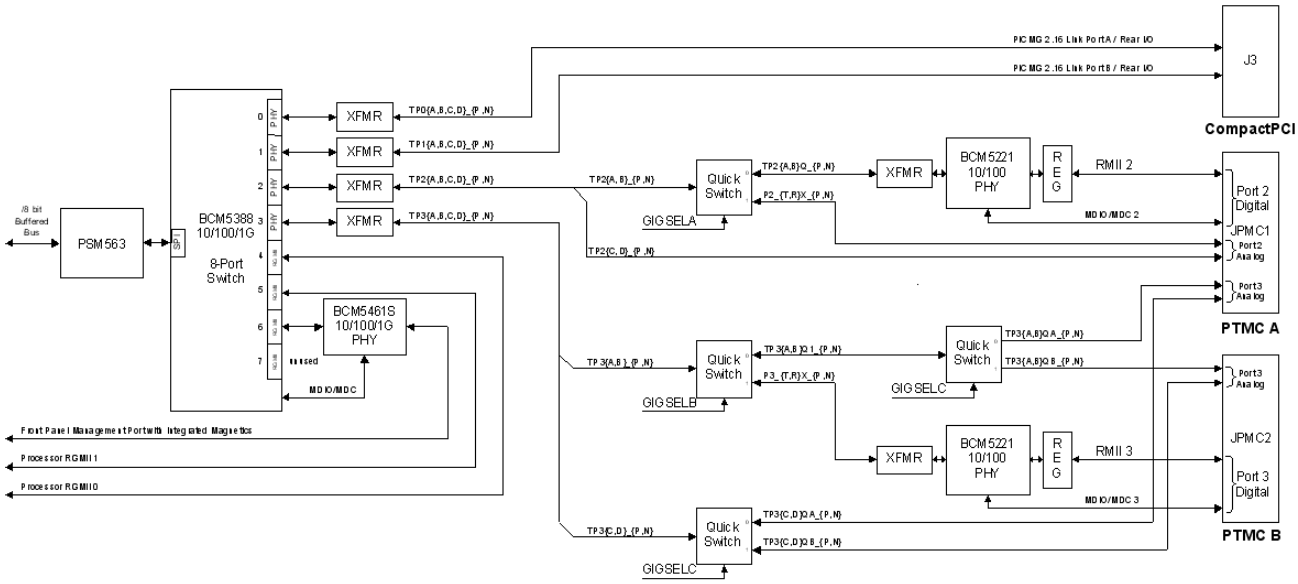
The Serial Peripheral Interface (SPI) is a full-duplex, synchronous, serial data link that is standard across many microprocessors, microcontrollers, and peripherals. It enables communication between microprocessors and peripherals and/or inter-processor communication. The SPI interface is used by the AMCC 440GX to configure the BCM5388 Ethernet switch’s internal registers. The interface is implemented in a CPLD and consists of I/O interface signals for the SPI and a CPU interface on the 440GX’s General Purpose Bus.

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Gigabit Ethernet Switch

The Ethernet connectivity of the CPC324 is shown in Figure 2-3, “Ethernet Block Diagram,” below.

Figure 2-3: Ethernet Block Diagram



The CPC324 uses an 8-port, gigabit Ethernet switch, implementing seven ports of IP connectivity between the processor, the two PTMC mezzanines, the two PICMG 2.16 link ports (or rear I/O) and the management port. The Broadcom BCM5388 is used for this function. The BCM5388 integrates the switch with four 10/100/1000 Mbps PHYs and four RGMII ports. A short feature list of this switch includes:

- 3.5Mb on-chip packet control buffer to aid in the non-blocking, wire speed operation
- Jumbo frames support up to 9728 bytes
- 4K unicast addresses
- 4K 802.1Q Tag VLANs
- MAC-based trunking
- Port, DiffServ, Weighted/Strict priority, and 802.1p-based QoS for four queues
- Port mirroring support
- Integrated SPI interface for light management

Table 2-3, “BCM5288 Port Mapping,” identifies the port mapping.

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Table 2-3: BCM5288 Port Mapping

Port Number	Use	Interface
0	PICMG 2.16 Link Port A / Rear I/O	10/100/1000Base-T
1	PICMG 2.16 Link Port B / Rear I/O	10/100/1000Base-T
2	PTMC A	10/100/1000Base-T or RMII[1]
3	PTMC B	10/100/1000Base-T or RMII[1]
4	Processor Port RGMII 0	RGMII
5	Processor Port RGMII 1	RGMII
6	Management Port (front panel)	RGMII to on-board 10/100/1000 PHY
7	Unused	RGMII

1. The RMII interface is a PHY function requiring an external MAC.

The BCM5388 is programmed across the SPI interface. This interface provides read and write access to the BCM5388 internal register space. It is compatible with the Motorola SPI protocol. It uses a 2 MHz typical clock rate. The BCM5388 always operates as a SPI slave device, in that it never initiates a transfer on the SPI and only responds to read and write requests issued from a master device. Normal SPI and fast SPI are supported. These two mechanisms should not be mixed in the implementation – the master should always initiate transfers consistently with only one of the two mechanisms. The EEPROM interface is not supported on the CPC324. Processor peripheral support by the SPI interface is outlined in “SPI Interface,” on page 26.

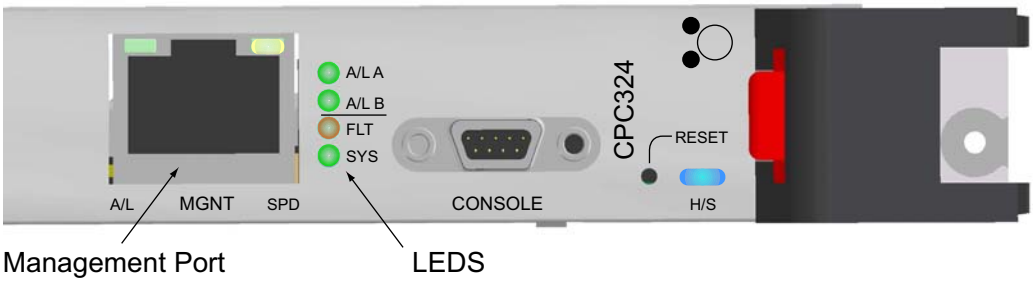
The BCM5388 provides LED outputs for the eight Ethernet ports. LEDs for Ports 0 and 1, the PICMG 2.16 link ports (or rear I/O ports) are provided on the front panel. See Figure 2-4, “RJ45 Management Port and LED Location,” below. A/L-A and A/L-B are configured as a link and activity indicator for PICMG 2.16 link port A and link port B respectively. The panel LEDs are ON (green) when link is established and blink at a 12 Hz rate when link is up and the port is transmitting or receiving.

Management Port

A 10/100/1000Mb Ethernet port is provided on the front panel as a management port, as shown in Figure 2-4, “RJ45 Management Port and LED Location,” on page 29. This is provided from switch port 6.

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Figure 2-4: RJ45 Management Port and LED Location



The management port connector has integrated LEDs (green for link/activity and yellow for speed) and an integrated magnetic. An MDC/MDIO interface controls the management PHY. See “10/100/1G BASE-T Ethernet Management Port,” on page 81 for more information.

PTMC Ethernet Ports

Two PTMC configuration 2 mezzanine sites are provided on the CPC324. Each site provides support for MAC based RMII interfaces and 10/100/1000Base-T interfaces. The RMII interfaces are pinned on J3 per the PTMC Configuration 2 definition. The 10/100/1G Ethernet is pinned on the configuration 2 user defined J4 connector, with pin assignments defined the same as PTMC configuration 5. See “CompactPCI Connectors,” on page 91 for pin definitions. The interface is selected by user switch settings. See “Switches,” on page 58 for more information.

RMII PHYs

The CPC324 provides two PHY based RMII interfaces. Two Broadcom BCM5221 10/100 PHYs are used to convert two of the 10/100Base-T Ethernet switch interfaces to RMII signaling. The PHY is set up with a programmable PHY address from 0-3. On-board switches are used for this selection. See “Switches,” on page 58 for more information. The default PHY address = 0. No LED indicators are used on the 10/100 PHY. The PHYs power with auto negotiation enabled. Management, if required, can be accomplished via the MDC/MDIO management signals with control from MACs on each PTMC sites.

PICMG 2.16 Ethernet Ports

The Ethernet switch provides two dedicated 10/100/1000Base-T ports for PICMG 2.16, supporting node link ports A and B. Switch port 0 is connected to link port A and switch port 1 to link port B. In non-2.16 systems these ports can be rerouted out to the RTM. LEDs are provided on the front panel indicating link/activity. See Figure 2-4, “RJ45 Management Port and LED Location,” on page 29.

Processor Ethernet Ports

Switch ports 4 and 5 are connected from the on-board Ethernet switch to the AMCC 440GX processor’s RGMII interfaces. Ethernet switch port 4 connects to 440GX processor port RGMII 0 and Ethernet switch port 5 connects to 440GX processor port RGMII 1.

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T1/E1/J1 Framers and LIU

Three IDT 82P2288 octal transceivers provide framing and line interface functionality for 24-port connectivity on 24 T1, E1 or J1 telecom trunks. Each octal transceiver has the capability of providing any two of eight recovered clocks to the local reference (LREF) inputs of the Zarlink H.110 switch. The recovered clocks are 1.544 MHz in T1/J1 applications and 2.048 MHz in E1 applications.

IDT 82P2288 General Specifications

The IDT 82P2288 transceiver meets the requirements of ITU, ETSI and AT&T jitter specifications. The high level of integration eliminates external components for line equalization. Integrated jitter attenuators (JAT) are incorporated in both the transmit and receive directions of each channel. Dual JATs allow the 82P2288 transceiver to simultaneously reduce jitter from both the line and system clocks.

IDT 82P2288 features include:

- Links configuration as T1, E1 or J1
- Frame alignment/generation for T1 (per ITU-T G.704, TA-TSY-000278, TR-TSY-000008), E1 (per ITU-T G.704), J1 (per JT G.704) and un-framed mode
- Supports T1/J1 Super Frame and Extended Super Frame, T1 Digital Multiplexer and Switch Line Carrier - 96, E1 CRC Multi-frame and Signaling Multi-Frame
- Signaling extraction/insertion for CAS and RBS signaling

Framer Board Level Integration

The three framers serve as the line side receivers for the T1, E1 or J1 external interfaces. Each framer has eight transmit and receive pairs associated with it. They transform the external data formats to a common Time Domain Multiplexed (TDM) digital standard signal that is fed to an on-board TDM switch. There the channels can be routed to the PTMC slots for further signal processing, to the H.110 CompactPCI backplane connection for offboard processing, or to the on-board, multi-channel, data communication transceiver for data termination or sourcing. See Figure 2-5, “Framer Block Diagram,” on page 31 for more information.

Line Receive Signal Path

Receive path signals from the line side are coupled into the RTIPn and RRINGn pins of the line interface unit (LIU) and pass through an internal programmable receive impedance terminator. There is a single resistor of 120 ohms external to the part to terminate the receive pair. The internal programmable adjustment is used to set the exact line termination conditions depending on the interface standard desired. An adaptive equalizer is provided to increase the sensitivity for small signals. Internal registers in the framer handle all other line conditioning requirements needed for the incoming signals. The registers are accessed over the CPU’s general-purpose bus.

The receive path data through the framer allows recovered data and clock of each link can be decoded in Super Frame (SF), Extended Super Frame (ESF), T1 Digital Multiplexer or Switch Line Carrier - 96 (SLC-96) formats. The T1 DM and SLC-96 formats exist only in T1 mode. The de-framing can also be bypassed to receive in unframed mode.

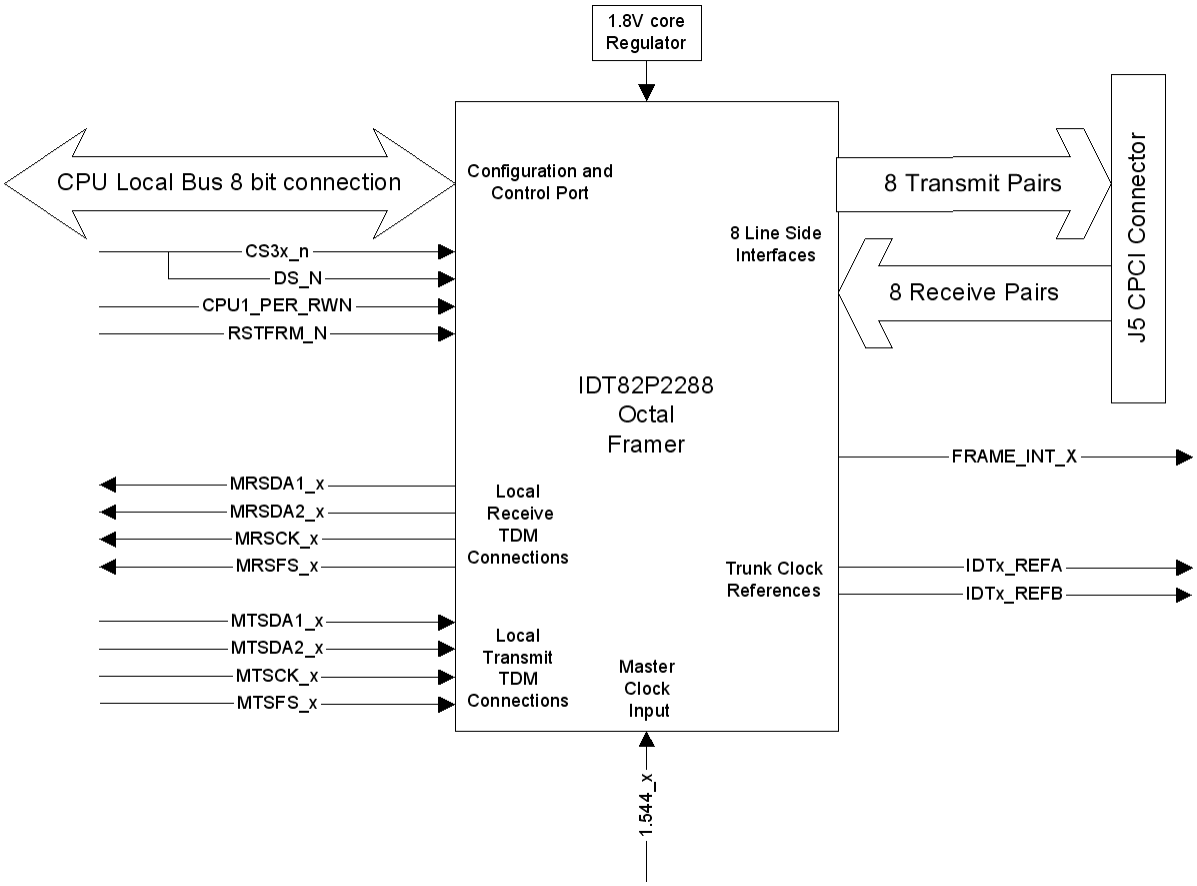
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Line Transmit Signal Path

In the transmit path LIU data is encoded using AMI or B8ZS (for T1/J1) and HDB3 (for E1) line code rules. A transmit jitter attenuator is available to provided a FIFO in the transmit data path. A de-jittered clock is generated by an integrated digital phase-locked loop and is used to read data from the FIFO. The shapes of the pulses are user programmable to ensure that the T1/E1/J1 pulse template is met after the signal passing through different cable lengths and types. In addition to the pulse shaping capabilities, the LIU has a built in programmable transmit line termination. There are individual settings for the transmit termination depending on the chosen signaling standard and the length of the link being configured. The CPU makes these settings through a set of transmit configuration registers accessible over the general-purpose bus.

The framer transmit path allows recovered data and clock of each link to be configured in Super Frame (SF), Extended Super Frame (ESF), T1 Digital Multiplexer or Switch Line Carrier - 96 (SLC-96) formats. The transmit path of each transceiver can be configured to generate SF, ESF, T1 DM or SLC-96. The framer can also be disabled and run in unframed mode. Basic Frame, CRC Multi-Frame and Signaling Multi-Frame can be generated as a transmit function of each transceiver.

Figure 2-5: Framer Block Diagram



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LOCAL TDM Connections

On the local side of the TDM bus the IDT82P2288 is hardware configured to operate in the transmit/receive multiplexed mode. Two 128 TS input (MRSDA1_x and MRSDA2_x) and two 128 TS output (MTSDA1_x and MTSDA2_x) buses are used to transfer data between the Zarlink MT90866 TDM switch and the eight links of the IDT framer. In the transmit path the data of link 1 to link 4 is a byte-interleaved input to pins MTSDA1_x. The data of link 5 to link 8 is byte-interleaved input to pins MTSDA2_x. Similarly in the receive path the data of link 1 to link 4 is a byte-interleaved output from pins MRSDA1_x. The data of link 5 to link 8 is byte-interleaved input to pins MRSDA2_x. The framer's TDM interface can support a few different byte-interleaving formats. The initial format chosen for the framer to TDM switch is the continuous channels mode.

In the transmit/receive multiplexed mode, the timing clock on the MTSCK_x, MRSCK_x pins and framing pulses on the MTSFS_x, MRSFS_x pins are provided by the system side and common to all eight links. They are derived from signals outputted by the TDM switch and buffered and passed to each framer connection as required.

Framer Clocks

Each framer has one input clock that is sourced from a buffered and distributed 25 ppm 1.544 MHz clock oscillator. There are selection pins on each framer that set up its internal logic to accept this frequency for the framer's internal use.

The framer outputs two trunk references on the IDTx_REFA and IDTx_REFB lines. These reference clocks are each recovered from one of the eight trunk inputs. The clocks are routed into the clock muxer CPLD where they can be turned on/ turned off and selected as inputs for the TDM switch's reference input.

Loopback Control

A number of local and line side loopback configurations are available to aid in debugging and fault finding. For the analog signal portion of the circuit, there is an analog loopback at the RX/TX pins. There is also a remote loopback capability that incorporates the internal terminations, receive adaptive equalizer, data slicer, clock and data recovery DPLL, receive and transmit jitter attenuator, transmit waveform shaper/line build out block and the line driver. There is also a line side loopback from the receive side elastic store to the transmit side payload control that allows the line side data to traverse almost the entire chip internally.

Similarly, for the local side loopback there is a system loopback at the TDM pins that loops back from the TDM transmit to the receive, a digital loopback from the transmit framer to the receive framer and a digital loopback from the transmit jitter attenuator to the receive jitter attenuator.

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Processor Interface

There is a parallel connection to the AMCC 440GX CPU. This connection is used for the configuration and control of each framer. The IDT82P2288 itself supports two modes of parallel bus operation, Motorola or Intel. The CPC324 makes use of the Motorola mode of operation. Each framer has an interrupt output that is connected directly to the 440GX. Table 2-4, “Framer Interrupt Mapping,” shows the mapping.

Table 2-4: Framer Interrupt Mapping

Framer	440GX Interrupt Connection
A	IRQ03
B	IRQ04
C	IRQ05

TDM Clock Distribution and Control

The TDM clock distribution is centralized about the Zarlink MT90866 H.110 TDM switch. This device generates all of the local TDM frame pulses and data clocks. It uses a variety of clock sources to lock up its internal digital phase locked loop (DPLL) to a system reference. This ability ensures that the data transferred on the blade stays in synchronization with the system and no timing slips occur. See Figure 2-6, “CPC324 TDM Clock Tree,” on page 37, for a visual representation of the circuit.

H.110 DPLL

The core of the part is the DPLL. It has a 20 MHz, 25 ppm signal source as its primary clock input. This clock directly drives the DPLL. The DPLL accuracy and the 25 ppm input clock allows the H.110 switch to function as a Stratum 4 enhanced clock source when it runs in a free run mode. In a normal integration into a telephony system, synchronized timing is maintained by locking the PLL to a system-supplied reference. Some of the important PLL specifications are listed in Table 2-5, “H.110 DPLL Operating Specifications,” below.

Table 2-5: H.110 DPLL Operating Specifications

Parameter	Value
Acceptable Reference Clock Input Frequencies	1.544 MHz, 2.048 MHz or 8 KHz per AT&T TR62411
Skew Control	8 taps @ 1.9 ns each, allows 0 to13.3 ns total skew adjustment between reference input and clock outputs. This translates to static phase offset of 1.28 µs to 1.293 µs for reference clock input of 1.544 MHz. For a reference clock input of 8KHz or 2.048 MHz, the static phase offset is 960 ns to 973 ns.
Phase Offset, dependent on reference clock frequency	For 1.544 MHz reference clock, maximum phase offset ±1.28 µs, minimum phase adjustment 10 ns. For 8kHz or 2.048 MHz reference clock, maximum phase offset ±0.96 µs, minimum phase adjustment 7.5 ns.
Phase Slope Limiter	Maximum phase slope response for input transient 4.6 ns per 125 µs. Meets AT&T TR62411 standard.
Loop Filter	Equivalent to a first order low pass filter with 1.52 Hz cutoff.
Intrinsic Jitter	6.25 nspp for the 80 MHz Master clock.

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Table 2-5: H.110 DPLL Operating Specifications (Continued)

Parameter	Value
Jitter Transfer	Rate limited by Phase Slope Limiter to 4.6 ns/125 µs. Jitter Transfer Function Cutoff frequency 1.52 Hz with slope of 20 db/decade. Refer to the datasheet for the actual curves and the UI calculations.
Frequency Accuracy	Master Clock/ppm + DPLL/ppm= 25+.03=25.03 ppm of selected frequency.
Holdover accuracy	Same as above calculation
Locking Range	±273 ppm
Maximum Time Interval Error (MTIE)	21 ns for every reference switch.
Phase Continuity	Maintained to within 4.6 ns at the instance (over one frame) of all reference switches.
Phase Lock Time	Less than 25 seconds

As mentioned above, the DPLL can choose from several input sources to obtain the signal it needs to lock to. This mechanism is what supplies the system synchronization. These clock sources can be selected via the reference mux internal to the part (LREF0…LREF6).

Internal Reference Clock Sources

The internal reference selector mux for the DPLL has a redundant configuration. The primary and secondary muxes both have access to the same set of clock sources. These sources include any of the eight local reference inputs, the A and B CT bus clocks or the CT Net references from the CT bus.

Internal Reference Monitors

There are two reference monitor circuits: one for the primary reference (PRI_REF) and one for the secondary reference (SEC_REF). These two circuits monitor the selected input reference signals and detect failures by setting up the adequate internal fail outputs (FAIL_PRI and FAIL_SEC). These fail signals are used in the autodetect mode as the internal LOS_PRI and LOS_SEC signals to indicate when the reference is failed. The method of generating failure depends on the selected reference:

- For all references, the "minimum 90 ns" check is made. This is the requirement by the H110 specifications. Both low level and high level of the reference must last for a minimum of 90 ns each.
- The "period in the specified range" check is done for all references. The length of the period of the selected input reference is checked if it is in the specified range. For the E1 (2.048 MHz clock) or the T1 (1.544 MHz clock) reference, the period of the clock can vary within the range of 1 ±1/4 of the defined clock period (488 ns for the E1 clock and 648 ns for T1 clock). For the 8 KHz reference, the variation is from 1 ±1/32 period.
- If the selected reference is E1 or T1, the "64 periods in the specified range" check is made. The selected reference is observed for long period (64 reference clock cycles) and checked if it is within the specified range - from 62 to 66 clock periods.

These reference signal verifications include a complete loss or a large frequency shift of the selected reference signal. When the reference signal returns to normal, the LOS_PRI and LOS_SEC signals return to logic low.

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The MT90866 has two interrupts that are associated with the detection of the primary or secondary reference loss. They are FAIL_PRI and FAIL_SEC. They are connected directly to the AMCC 440GX's external interrupt inputs.

CT Clock and Frame Monitor Circuits

These monitor circuits check the period of the CTC8_A and the CTC8_B clocks and the CTFRMA# and CTFRMB# frame pulses. According to the H.110 signal specification, the C8 period is 122 ns with a tolerance of ±35 ns measured between rising edges. If C8 falls outside the range of [87 ns,157 ns], the clock is rejected and the fail signal (FAIL_A or FAIL_B) becomes high. The frame pulse period is measured with respect to the C8 clock. The frame pulse period must have exactly 1024 C8 cycles. Otherwise, the fail signal (FAILA_INT or FAILB_INT) becomes high. They are connected directly to the AMCC 440GX's external interrupt inputs.

External Reference Clock Sources

These sources include any of the recovered clocks from the IDT82P2288 framer's receivers or an on-board 1.544 MHz, 25 ppm crystal oscillator. The recovered clocks and oscillator are mapped to the MT90866's local reference source (LREF0-6) inputs through CPLD as shown in Table 2-6, "MT90866 Local Reference Sources," below.

Table 2-6: MT90866 Local Reference Sources

MT90866 Input Signal	Referenced Input
LREF0	FRAMER A reference output A
LREF1	FRAMER A reference output B
LREF2	FRAMER B reference output A
LREF3	FRAMER B reference output B
LREF4	FRAMER C reference output A
LREF5	FRAMER C reference output B
LREF6	On-board 1.544 MHz crystal oscillator

H.110 Clock Operating Modes

The MT90866 contains clock distribution and control circuitry that supports both master and slave modes of H.110 operation. The H.110 switch provides primary and secondary clock and frame synchronization sources for the local TDM streams. The synchronization is distributed to all of the local TDM devices as described in the previous sections. H.110 backplane clocks CT_C8_A and CT_C8_B are supported at 8 MHz operation exclusively. Local clocks are supported at 8 MHz operation exclusively.

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When it is operating in CT bus master mode, the H.110 switch accepts two of several local clock references that may be recovered by the E1/T1/J1 framers, provided by the PTMC module or generated by an optional local precision oscillator. These are divided down to create an 8 KHz clock reference. These primary and secondary reference clocks are used to drive CTREF1 or CTREF2 to the H.110 backplane for primary or secondary master operation. They are also provided to a PLL that generates and drives the CT_FRAME_A or CT_FRAME_B synchronization, and CT_C8_A or CT_C8_B clock, to the H.110 backplane. The selected local reference clocks are monitored and cause an interrupt upon failure. Local status and masking is provided for these interrupt sources.

In slave mode, the H.110 switch accepts CTREF1, CTREF2, CT_C8_A and CT_C8_B clocks. One CTREF and one CT_C8 clock are selected for primary operation, while the alternate pair stands by as secondary clocks.

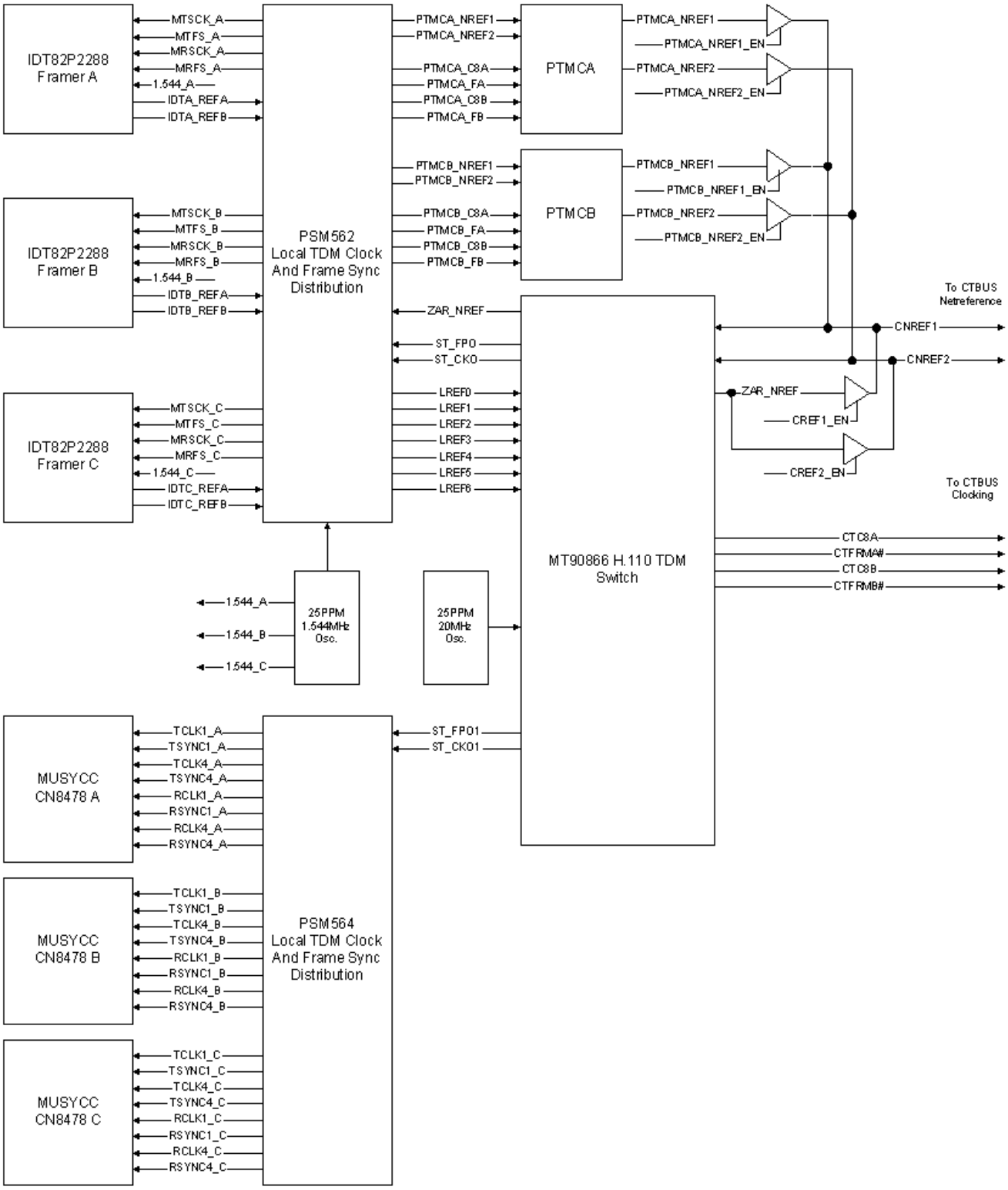
Support is included to allow A-side and B-side source termination resistors on CT_C8_A/B and CT_FRAME_A/B to be bypassed.

A and B side clock and frame synchronization are monitored by the H.110 switch. Failure causes the corresponding FAIL_A or FAIL_B signal to be asserted. This signal is intercepted and provided as an interrupt to the AMCC 440GX. A 20 MHz crystal oscillator is provided for the H.110 switch as its primary clock input. This is a dedicated clock without control options.

The H.110 switch can also source the CT bus net reference signals. The H.110 CT bus net reference can also be sourced from one of the PTMC slots.

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Figure 2-6: CPC324 TDM Clock Tree



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H.110 Switch

The CPC324 uses the Zarlink MT90866 to connect the various time domain multiplexed (TDM) interface streams together. It has local side connections to the on-board multichannel communications controller (Mindspeed MUSYCC CN8478), both on-board PTMC slots and the three IDT octal framers. Its backplane connection is to the 32-bit H.110 CT bus.

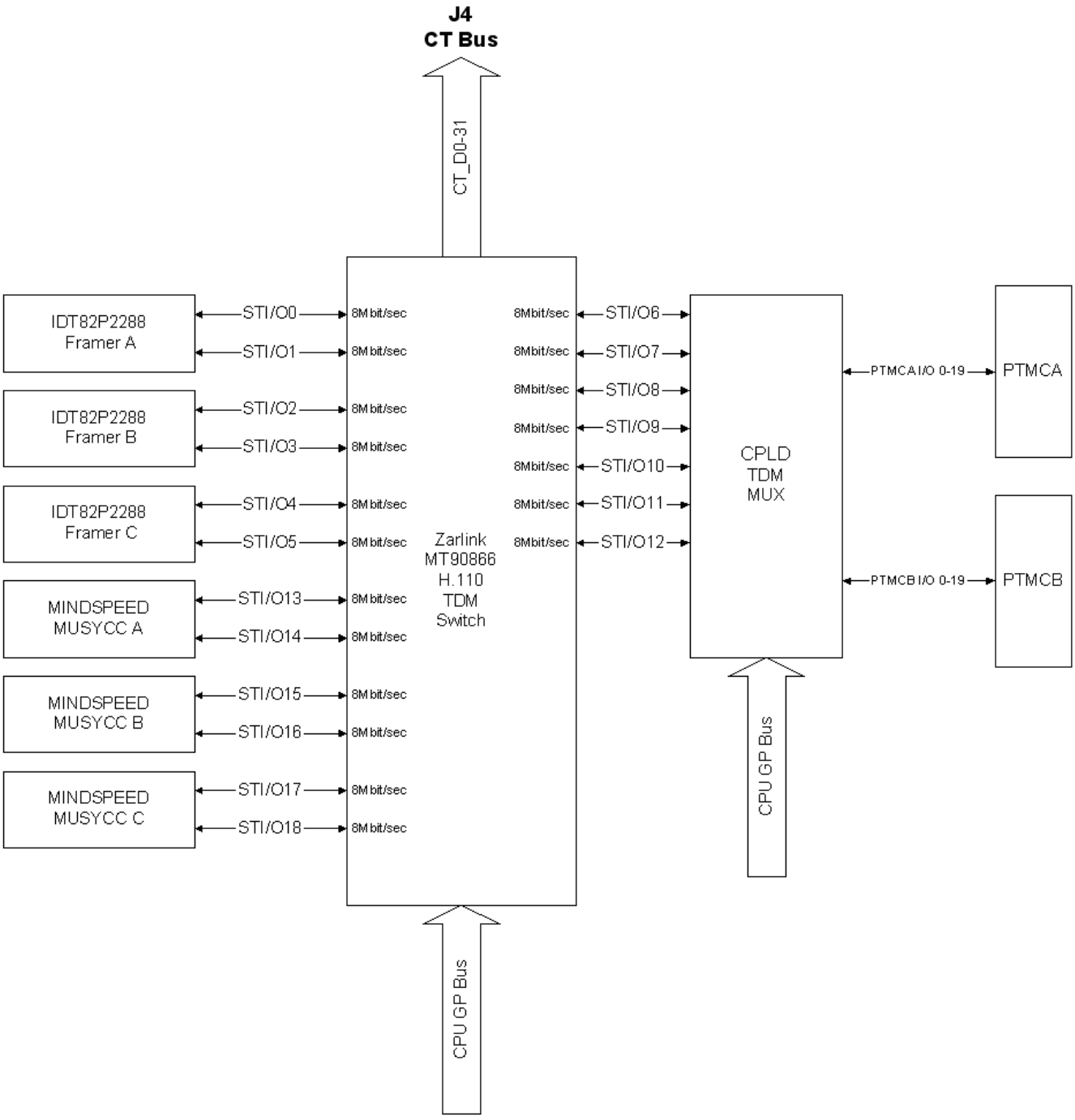
General Specifications

The MT90866 digital switch provides switching capacities of 4,096 x 2,432 channels between the H.110 bus backplane and local streams, 2,432 x 2,432 channels among local streams and 2,048 x 2,048 channels among backplane streams. The local connected serial inputs and outputs have 128 64 kb/s channels per frame with a data rate of 8.192 Mb/s. The backplane connected serial inputs and outputs have 128 64 kb/s channels per frame with a data rate of 8.192 Mb/s. The device has features that are programmable on a per-stream or per-channel basis, including message mode, input delay offset, output advancement offset, direction control, and high impedance output control.

On the CPC324 the MT90866 switch connects to the IDT 82P2288 framers local side TDM bus, the mindspeed multichannel communications controllers TDM connections, and the CPLD TDM mux, which ultimately allow both PTMC slots to have a flexible TDM I/O connection. The MT90866 TDM switch is also the CPC324's connection to the J4 CompactPCI CT bus (H.110). See Figure 2-7, "H.110 Data and Control Block Diagram," on page 39 for further information.

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Figure 2-7: H.110 Data and Control Block Diagram



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Processor Interface

There is a parallel connection to the AMCC 440GX CPU. This connection is used for the configuration and control of the TDM switch.

For information on how to use the registers in the H.110 TDM switch, refer to the *Zarlink Semiconductor MT9866 WAN Access Switch Datasheet*.

The H.110 TDM switch has several interrupt outputs that connect directly to the 440GX. They are mapped as shown in Table 2-7, “TDM Interrupt Mapping,” below.

Table 2-7: TDM Interrupt Mapping

MT90866 Interrupt	440GX Interrupt Connection
FAIL_PRI_INT	IRQ06
FAIL_SEC_INT	IRQ07
FAILA_INT	IRQ08
FAILB_INT	IRQ09

The FAIL_PRI_INT and FAIL_SEC_INT interrupts indicate that the system timing reference inputs have either stopped or are out of specification according to the internal detection logic. The FAILA_INT and FAILB_INT indicate that there has been a failure in the A or B side clocks on the J4 CT bus.

TDM Multiplexer Registers

The TDM multiplexer CPLD connects local TDM input and output streams on the MT90866 switch to various TDM connections on the two PTMC slots. The connection from the switch to the CPLD is unidirectional and fixed. The CPLD outputs to the PTMC slots are unidirectional but can be programmed as inputs or outputs individually. There is a register file inside the CPLD that determines what the direction of the PTMC connection is and to which port on the MT90866 that the PTMC line is mapped.

TDM Multiplexer Reverse Endian

The TDM multiplexer PLD has the capability of reversing the endian of the TDM bit stream. The reverse endian function may be performed on up to 896 DS0s (seven streams, STI/O 6 – 12) of the dedicated lines from the Zarlink to TDM multiplexer interface. The minimum connection allocation of the reverse endian function is 128 DS0s (1 stream). Once a bit stream has been allocated to implement the reverse endian function it can no longer be used as an available PTMC connection stream. The reverse endian function is accomplished by writing a control command in the respective TDM switch input (6 – 12) mux register that has been chosen to perform the reverse endian function. Implementing the reverse endian function reverses the individual bit order, however the TDM mux PLD inserts one timeslot delay per DS0 channel.

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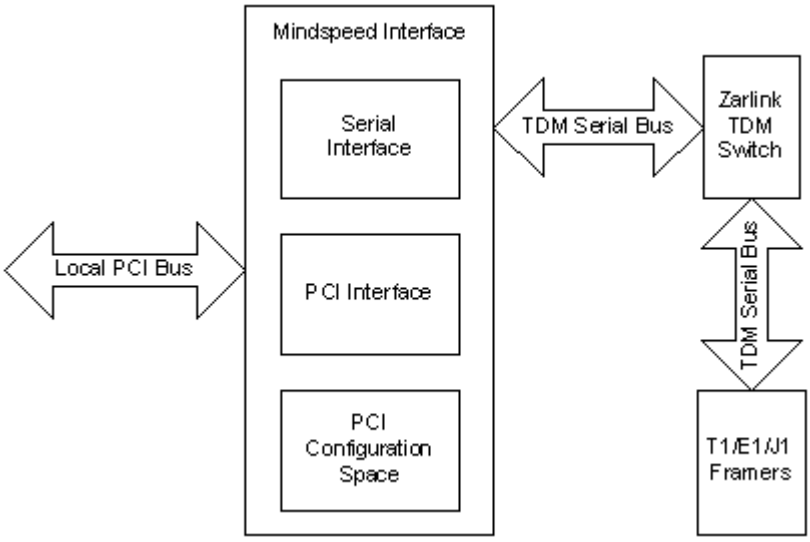
T1/E1/J1 Layer 2 Communications Controller

The CPC324 utilizes three Mindspeed CN8478 8-port multichannel synchronous communications controllers (MUSYCC) that manage linked lists of channel data buffers in host memory by performing direct memory access (DMA) on HDLC channels. Each MUSYCCs chip formats and de-formats up to 256 HDLC channels. The MUSYCCs operate at layer 2 of the open systems interconnection (OSI) protocol reference model and provide a comp for processing HDLC channels for internetworking applications such as Frame Relay, ISDN D-channel signaling, X.25, Signaling System 7 (SS7), DXI, ISUP, and LAN/WAN data transport.

Under minimal host supervision, MUSYCCs manage a linked list of channel data buffers in host memory by performing DMA of the HDLC channels. Each MUSYCC processes eight independent T1/E1 spans worth data as serial TDM data streams running at 8.192 MHz. Processed data streams are then transferred data across the local PCI bus to system memory at a rate of 33 MHz. Logical channels can be mapped as any combination of DS0 time slots to support ISDN hyper channels (Nx64 kbps) or as any number of bits in a DS0 for sub channeling applications (Nx8 kbps).

The Mindspeed PCI host interface acts as both a PCI master and PCI slave, and contains MUSYCC's PCI configuration space and internal registers. MUSYCC behaves as a PCI slave when providing access from the AMCC 440GX local PCI host to its internal on-chip bus and a master when accessing host memory for DMA transfers.

Figure 2-8: MUSYCC Function Block Diagram

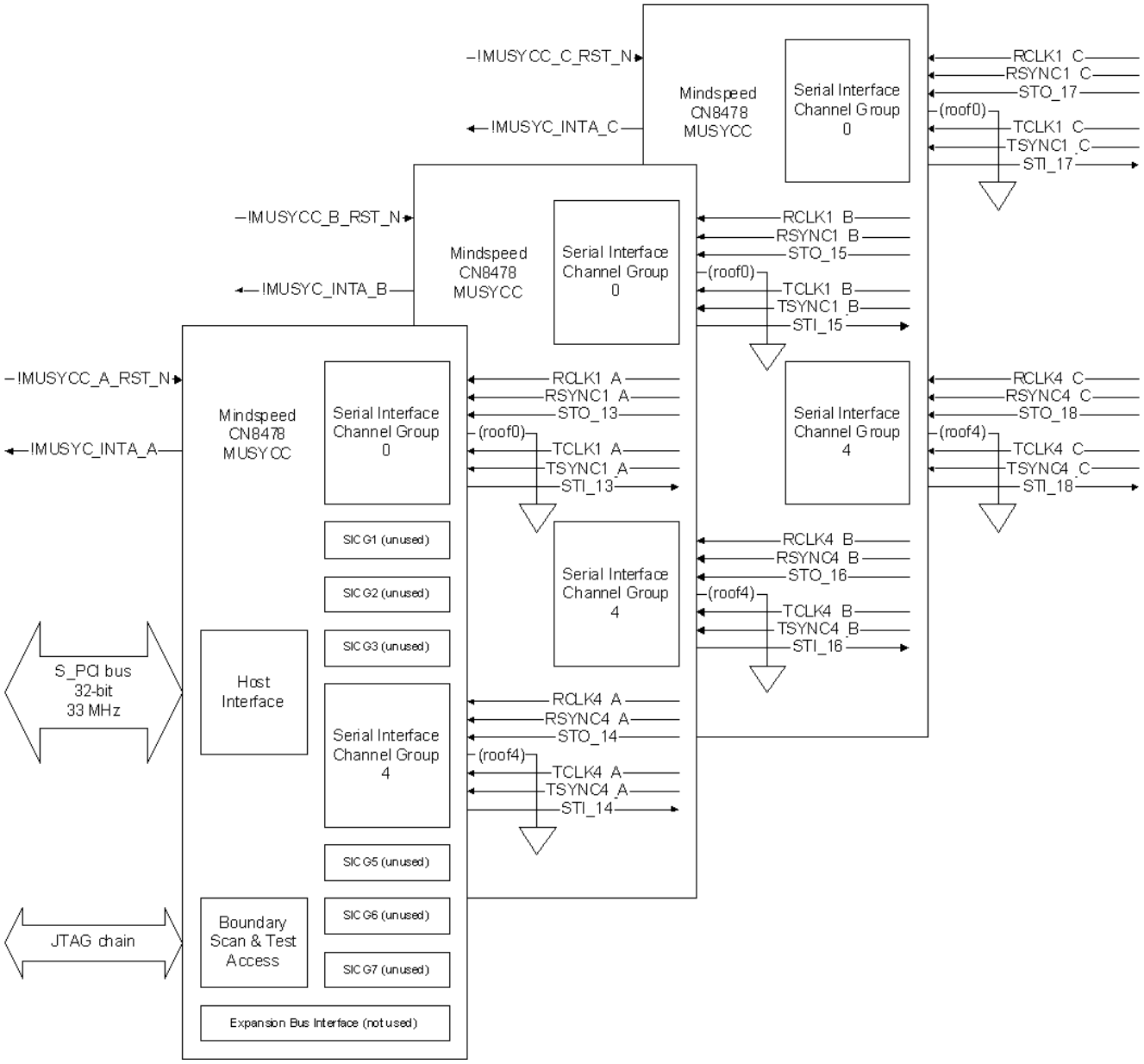


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System Interconnection

Figure 2-9, “MUSYCC Block Diagram,” illustrates how the three MUSYCCs are connected on the CPC324.

Figure 2-9: MUSYCC Block Diagram



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Interrupts

The MUSYCC provides an interrupt pin that must be programmed using the interrupts of the AMCC 440GX processor to use this function. The MUSYCC should be taken out of reset prior to setting the local enable (or clearing the local mask) of the interrupt.

The interrupts are listed in Table 2-8, “MUSYCC Interrupt Mapping,” below.

Table 2-8: MUSYCC Interrupt Mapping

MUSYCC	440GX Interrupt Connection
A	IRQ00
B	IRQ01
C	IRQ02

PCI Initialization

When the AMCC 440GX processor initializes a module containing a PCI device, the software reads the configuration space of each PCI device on a PCI bus. Hardware signals select a specific PCI device based on a bus number, a slot number, and a function number. If the addressed device (via signal lines) responds to the configuration cycle by claiming the bus, that function’s configuration space is read out from the device during the cycle. Because any PCI device can be a multifunction device, every supported function’s configuration space must be read from the device. Based on the information read, the configuration manager assigns system resources to each supported function within the device. Sometimes new information must be written to the function’s configuration space; this is accomplished with a configuration write cycle. MUSYCC is a multifunction device with device-resident memory to store the required configuration information. MUSYCC supports function 0 and function 1 and, as such, only responds to function 0 and function 1 configuration cycles, defined as listed below:

- Function 0: All HDLC processing as an HDLC network controller. Can master the PCI bus or respond to slave accesses from another bus master.
- Function 1: EBUS bridge to local devices. Responds only when another bus master performs a memory access into the function 1 address range.

PCI Bus Operations

MUSYCC behaves either as a PCI master or a PCI slave at any time and switches between these modes as required during device operation. As a PCI slave, MUSYCC responds to the following PCI bus operations:

- Memory read
- Memory write
- Configuration read
- Configuration write
- Memory read multiple (treated like memory read in slave mode)
- Memory read line (treated like memory read in slave mode)
- Memory write and invalidate (treated like memory write)

All other PCI cycles are ignored by MUSYCC. Only memory cycles are mapped to operations on the EBUS.

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As a PCI-master, MUSYCC generates the following PCI bus operations:

- Memory Read Multiple (generated only in master mode)
- Memory Write
- Dual Address Cycle

DMA Controller

The DMA controllers (Rx-DMAC and Tx-DMAC) manage all memory operations between a corresponding BLP and the host interface. DMAC takes requests from BLP to either fill or flush internal FIFO buffers, sets up an access to data buffers in shared memory, and requests access to the PCI bus through the host interface.

Interrupt Controller

The interrupt controller takes receive and transmit events from Rx-BLP and Tx-BLP, respectively. The INTC coordinates the transfer of internally queued descriptors to an interrupt queue in shared memory and also coordinates the notification to the host of pending interrupts.

Zircon UL Peripheral Monitor

The CPC324 incorporates a Zircon UL RISC microprocessor Intelligent Platform Management Controller (IPMC) for the support of the Intelligent Platform Management Bus (IPMB) in a CompactPCI environment. The IPMB is an I2C-based bus that provides a standardized interconnection between different boards within a CompactPCI chassis for auxiliary management of CPCI baseboards.

System management software and the OS can provide a higher level of control, error handling, and alarms. The IPMC can support monitoring, logging, and control recovery functions independent of the AMCC 440GX main processor and operating software. The IPMC is used by IPMC system management software to provide an high level of emergency manageability by providing access to the IPMI management information and integrating IPMI with the additional management functions provided by OS management application software.

The IPMC includes support for storing and accessing multiple sets of non-volatile field replaceable unit (FRU) information for CPC324. The FRU data includes information such as serial number, part number, and model. IPMC FRU information can be made accessible via the IPMB and IPMC. FRU information can be retrieved at any time, independent of the AMCC 440GX. This allows FRU information to be retrieved via out-of-band interfaces, such as the chassis or system management controller, a remote management blade, or other device connected to the IPMB. FRU information can even be available when the system is powered down. These abilities allow FRU information to be obtained under failure conditions when FRU access mechanisms that rely on the main processor become unavailable.

Features:

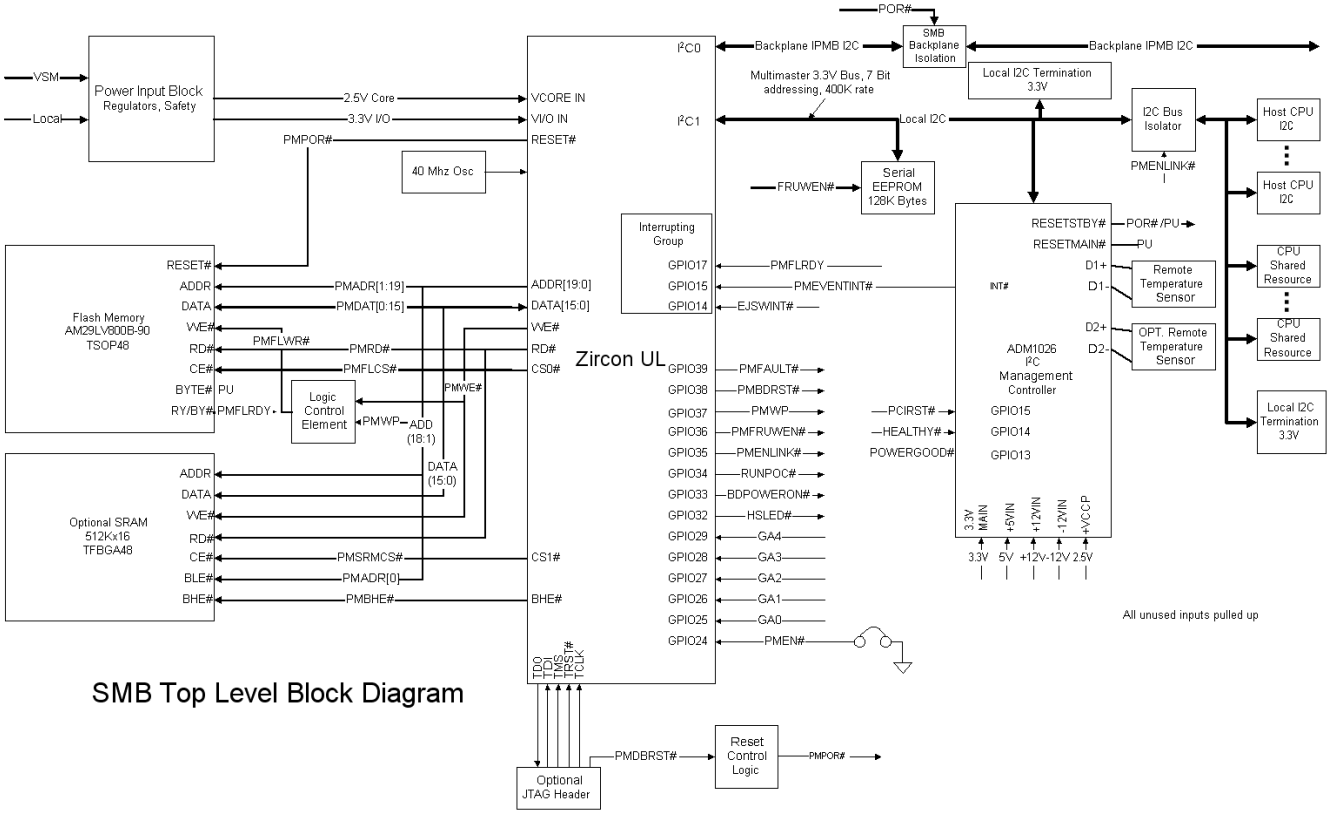
- ARM RISC CPU running at 40 MHz
- 16 KB of internal SRAM
- External non-multiplexed bus supporting 16-bit wide flash memory, 29LV800B-90 implemented as 512Kx16
- Optional 16-bit wide SRAM, implemented as 512Kx16 (for debug and trouble shooting only)

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- Two identical master/slave I2C supporting a variety of bus speed modes
- One I2C interface supports the IPMB backplane connection
- One I2C interface supports the local resources and Local CPU communication connection. Bus is 3.3V, 7-bit addressing at 400 KHz clock rate.
- Three general-purpose timers, one with watchdog capabilities that can interrupt or reset the ARM CPU
- Six analog comparators referenced to an internal 1.2V source
- 18 general purpose/dual function I/Os, some with interrupting capability
- GPIO17-14 have interrupting capabilities
- Local I2C peripherals
    - ADM1026 I2C management controller
    - 1Mbit EEPROM
    - QS384 used for I2C bus isolator

Figure 2-10, “Zircon UL Block Diagram,” shows the top-level functional blocks of the Zircon UL. The following topics explain each functional block and contain any setup and configuration information associated with that block.

Figure 2-10: Zircon UL Block Diagram

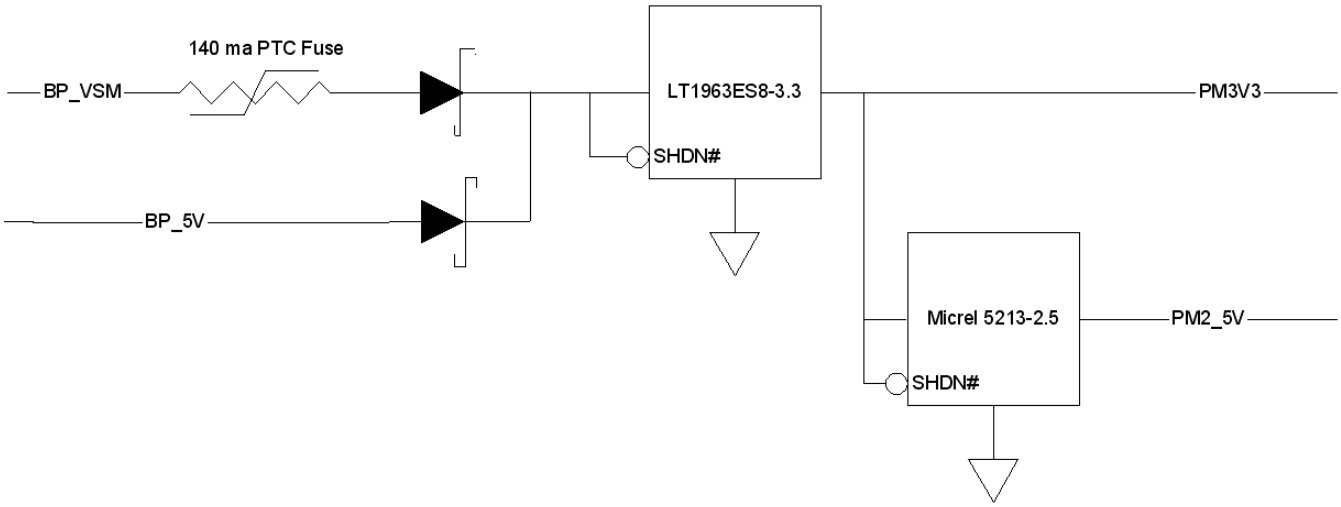


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Power Distribution

The power input block consists of the backplane power connections, voltage regulators for operating, I/O and core voltages and a 3.3 V power monitor. See Figure 2-11, “Power Distribution Block Diagram,” below.

Figure 2-11: Power Distribution Block Diagram



The primary power is sourced from the CompactPCI VSM pin on J1-A4. The VSM power is +5V at 100 mA steady state, 500 mA peak. The 140 mA PTC fuse provides the PICMG 2.9 required overcurrent protection circuit in the VSM supply. The power is diode ORed with the backplane +5V supply to provide an alternate power source when VSM is not available. This may occur in a non-2.9 compliant backplane.

The power is then routed to a Linear Tech 1963 low dropout linear regulator rated at 1.5 A. This regulator supplies the 3.3V I/O power for the Zircon UL as well as the operating power for the rest of the PM circuitry. This voltage in turn is fed into a Micrel 5213 linear regulator rated at 80 mA, that creates a 2.5V supply for the Zircon UL core voltage.

Zircon UL ARM7 CPU

The QLOGIC Zircon UL has an internal ARM7 CPU that is used to execute code contained in the AM29LV800B flash device. This code contains an operating system based on the Thread-X real time operating system (RTOS). QLogic supplies a modular application code set that runs under Thread-X and allows the Zircon UL to conform to the IPMI protocol. The RTOS and the application code configure most of the internal registers on a default basis. Refer to the *Zircon UL Technical Manual* and *Zircon UL Programmers Hardware Reference Manual* for more information on the chip’s default internal settings.

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Flash Memory

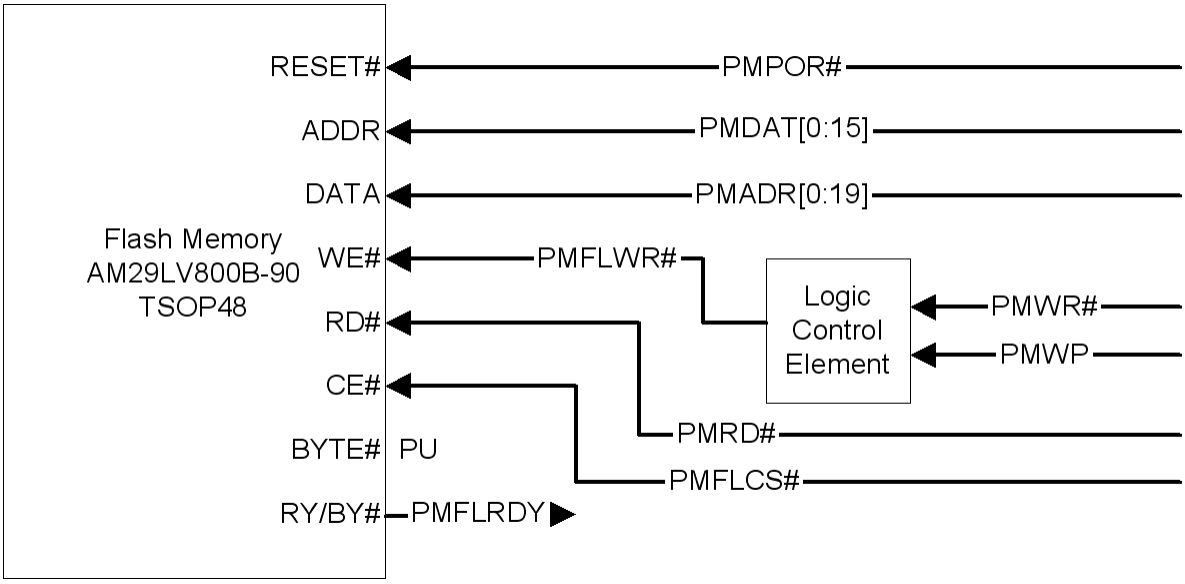
The memory block consists of an AM 29LV800B-90 flash device from the Spansion line of Advanced Micro Devices (AMD). It has a 512Kx16 bit data configuration, which is also the maximum address capability of the Zircon's external bus for an individual chip selection. The memory read mode access time is 90 ns maximum. The flash is physically located in a 48-pin TSOP surface mount package on the secondary (bottom) side of the PCB. For additional information, refer to the AMD's *Am29LV800B Spansion Datasheet*.

For the IPMI application, the flash is powered from 3.3V provided by the PM power distribution block. The flash is directly controlled by the Zircon UL's parallel interface control lines. There are, however, two exceptions to this:

The first is the flash's RESET# input control. This line is the logical OR of the CPU's reset output and the ADM1026 I2C peripheral. This input is designed to protect the flash device from an accidental erasure or overwrite during power up and power down events.

The second exception is the write protect bit (PMWP). When set high, this bit prevents the flash from being written under any circumstances. The PMWP bit is controlled by an output from the ADM1026 peripheral located on the local I2C bus. The default signal's reset state automatically disables writing.

Figure 2-12: Flash Device Implementation



The PMFLRDY# control signal connects to the GPIO bit 17 input on the Zircon UL. When set low, it indicates that the flash is doing an extended time internal operation, such as a block erasure. When high, it indicates that the flash's internal controller is idle or has completed a long-term operation.

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UL I2C Bus Operation

The Zircon UL provides two I2C ports, each port having master and slave capability. A master-slave port contains a master engine and a slave engine where each engine contains one 8-byte deep physical FIFO used for sending (TX) and receiving (RX) bytes to and from the I2C bus.

For the FIFO of each master and slave engine, hardware generates a set of FIFO status flags that are relevant when the FIFO is receiving data, and a separate set of status flags that are relevant when the FIFO is transmitting data.

When an engine is transferring data over the I2C bus, the master or the slave automatically extends the low period of SCL (clock-stretch) on the I2C bus in the following situations:

- By the master when the master TX FIFO becomes empty during a master write transaction
- By the slave when it receives a byte during a write access but the slave RX FIFO is already full
- By the slave after every byte it receives, if the slave RX FIFO has not been enabled. In this configuration, the slave is processing received bytes on a byte-by-byte basis, giving firmware the opportunity to evaluate bytes on a byte-by-byte basis.

Slave address decoding can be enabled for secondary and broadcast (general call) addresses as defined by the I2C specification

I2C0 PM Implementation

In the PM implementation, I2C0 is assigned to the IPMB and is used to receive commands from system IPMI controller. The operational specifications for the IPMB are contained in the *CompactPCI System Management Specification PICMG 2.9*. The interface circuit on the UL was designed to conform to these specifications and operates as a Peripheral Manager (PM) on the IPMB. Refer to the *Zircon UL Programmers Hardware Reference Manual* for further information.

The Zircon UL processes commands and operations conforming to the IPMI protocol. See “IPMI Commands,” on page 50 for a list of those commands and operations supported by PM implementation.

I2C1 PM Implementation

In the PM implementation, I2C1 is assigned to the local I2C bus and is used to communicate with on-board control peripherals, blade sensors and the blade host processor. The electrical operational specifications for the local I2C bus are similar to the IPMB. These specifications are contained in the *CompactPCI System Management Specification PICMG 2.9* and for the most part can be used to implement the local bus. The major departure from the specification is that the local bus operates at 400 KHz (vs. 100 KHz for IPMB) and the UL operates in a manner similar to the baseboard management controller (BMC). Refer to the *Zircon UL Programmers Hardware Reference Manual* for further information.

I2C1

The Zircon UL issues commands and operations conforming to the IPMI protocol for standard services already defined in the IPMI protocol. See “IPMI Custom Commands,” on page 52 for a list of those commands and operations supported by PM implementation. In addition to this a set of custom commands and operations are implemented to support blade-specific commands and operations. See “IPMI Bus Supported Commands,” on page 50 for specific information.

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The I2C1 also has a unique feature that allows it to isolate itself from the parts of the entire local I2C bus. This is done primarily to enable the Zircon UL to operate and perform the PM function while the main part of the PCB is in a powered down or failed mode. The isolation mechanism is controlled by the PMENLINK# signal. When the link is enabled, the entire local I2C bus is available to the Zircon UL. When the link is disabled, the Zircon UL, the control peripherals, the sensors, and other PM specific devices are isolated from the main blade but still available to one another.

ADM1026 Peripheral and Management Controller

The ADM1026 is an I2C based device that controls and monitors several PCB level functions typically found on embedded controllers and server motherboards. These general-purpose functions used to be done by discrete logic or low integrated devices. The type of functions and the information gathered by the monitor is used by the system level managers to determine the physical state and general health of the embedded controller.

Among the functions integrated into the device are:

- Up to 19 analog measurement channels (including internal measurements)
- Up to eight fan speed measurement channels
- Up to 17 general purpose logic I/O pins
- Remote temperature measurement with remote diode (two channels)
- On-chip temperature sensor
- Analog and PWM fan speed control outputs
- 2-wire serial system management bus (IPMBus)
- 8 KB on-chip EEPROM
- Full IPMBus 1.1 support including Packet Error Checking (PEC)
- Chassis intrusion detection
- Interrupt output (SMBAlert)
- Reset input, reset outputs
- Thermal interrupt (THERM) output
- Limit comparison of all monitored values

ADM1026 I2C Address

The ADM1026 has the ADD pin pulled low. This forces the device to be I2C address 0x58.

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Serial EEPROM

The Serial EEPROM is located on the local I2C bus. It is a 1-megabit device that is used to store the custom Field Replacement Unit (FRU) data. It also be used to store blade-specific data and records as the need arises. The EEPROM is powered from the PM V3V bus. The EEPROM operates at the local bus rate of 400 KHz and offers the required 7-bit addressing mode. The address of the FRU is fixed at A4 by pulling up the A1 input to PM V3V. The EEPROM can be write inhibited by the PMFRUWEN# line being driven to a high state. The default state for this signal is false, leaving the EEPROM in a read only state. The bit is controlled by the ADM1026.

IPMI Commands

IPMI Bus Supported Commands

The Zircon UL PM supports the following IPMI commands that are issued by the system management bus controller on the IPMBus. The exact structure of the commands is found in the *IPMI Intelligent Platform Management Specification Version 1.5*. This command structure allows the PM to support the minimum set of cTCA required commands for the PM to be cTCA compatible. See Table 2-9, “Supported IPMI Commands,” below.

Table 2-9: Supported IPMI Commands

Command Name	CMD
IPMI Global Commands	
Get Device ID	0x01
Cold Reset	0x02
Warm Reset	0x03
Get Self Test Results	0x04
Manufacturing Test On	0x05
Set ACPI Power State	0x06
Get ACPI Power State	0x07
Get Device GUID	0x08
Broadcast “Get Device ID”	0x01
Event Commands	
Set Event Receiver	0x00
Get Event Receiver	0x01
Sensor Device Commands	
Get Device SDR Info	0x20
Get Device SDR	0x21
Reserve Device SDR Repository	0x22
Set Sensor Threshold	0x26
Get Sensor Threshold	0x27
Get Sensor Reading	0x2D
FRU Device Commands	

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Table 2-9: Supported IPMI Commands (Continued)

Get FRU Inventory Area Info	0x10
Read FRU Data	0x11
Write FRU Data	0x12
SDR Device Commands	
Enter SDR Repository Update Mode	0x2A
Exit SDR Update Mode	0x2B

Table 2-10, "Supported cTCA Platform Specific Command Extensions," lists the initial additional commands implemented to support cTCA protocol.

Table 2-10: Supported cTCA Platform Specific Command Extensions

Command Name	CMD
Get PICMG Properties	0x00
Get Address Info	0x01
Get Shelf Address Info	0x02
Se Shelf Address Info	0x03
FRU Control	0x04
Get FRU LED Properties	0x05
Get LED Color Properties	0x06
Set FRU LED State	0x07
Get FRU LED State	0x08
Set IPMB State	0x09
Set FRU Activation Policy	0x0A
Get FRU Activation Policy	0x0B
Set FRU Activation	0x0C
Get Device Locator Record ID	0x0D
Set Port State	0x0E
Get Port State	0x0F
Compute Power Properties	0x10
Bused Resource Control	0x17

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IPMI Custom Commands

The Zircon UL PM supports the following IPMI commands that are issued by PM on the local I2C bus to the local CPU. Table 2-11, “Custom Command Structure,” outlines the custom command structure:

Table 2-11: Custom Command Structure

Command Name	CMD	Comment
OEM Commands (NetFN=0x30)		
Set GUID	0x07	Writes the GUID to the PM. The PM will use this value in response to a "Get GUID" command.
Get Firmware Version	0x08	Returns four bytes (ASCII) that translate into the PM firmware version.
Diagnostic Echo	0x09	Used for diagnostic testing, returns the data passed in the request.
Get Slave Address	0x0a	Returns two bytes, first is the geographical address of the target, second is the IPMB slave address.
Set Self Test Results	0x0b	Writes the POC test results to the PM.
Application Booted	0x0c	Notifies the PM that the application is running, and the blue (hot swap) LED should be turned off.
Application Halted	0x0d	Notifies the PM that the application is halted, and the blue (hot swap) LED should be turned on.
Shutdown Request	0x0e	Requests the PM to initiate a shutdown.
Firmware Update Commands		
Identify Chip	0x00	Returns information on the flash memory component based on the "Requested Flash Family" parameter.
Erase Sector in Flash	0x01	Erases the selected sector in flash memory.
Write to Flash	0x02	Programs flash memory.

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Sensors

Several on-board sensors collect status data and relay the information to the Intelligent Platform Management Controller. Table 2-12, “CPC324 Sensors,” describes each on-board sensor.

Table 2-12: CPC324 Sensors

Sensor Number (dec)	Sensor Name	Sensor Function
0x50 (80)	Temp1	Local to ADM1026 - Middle of Blade
0x51 (81)	Temp2	D1 - Exhaust
0x52 (82)	Temp3	D2 - Inlet
0x60 (96)	V2.5 2.5V	Core Voltages for HDLC Controller, Ethernet Switch and PHYs, DRAM
0x61 (97)	V3V 3.3V	Payload 3.3V from CPCI Backplane
0x62 (98)	PMV3V 3.3V	Management 3.3V
0x63 (99)	VDD 5V	Payload 5V from CPCI Backplane
0x64 (100)	+12V	Payload +12V from CPCI Backplane
0x65 (101)	-12V	Payload -12V from CPCI Backplane
0x66 (102)	PMPOR 3.3V	Power-On Reset
0x70 (112)	FRNT PNL EJECT	Front Panel Eject Switch

Interpreting Sensor Events

Performance Technologies adopts the following philosophy with respect to threshold sensor event severity levels:

- Non-critical — A warning that things are somewhat out of normal range, but not really a “problem” yet. See “Non-Critical Events” below.
- Critical — Things are still in valid operating range, but are getting close to the edge; unit still operating within specified tolerances. See “Critical Events” below.
- Non-recoverable — The unit is no longer operating within specified tolerances. See “Non-Recoverable Events” below.

Non-Critical Events

Non-critical events are informative only - they do not indicate that the blade is outside of its operating limits. In general, no action is required. However, in certain contexts, system/shelf management software may decide that preventive action should be taken. For example, if several blades in a shelf report upper non-critical temperature events, the shelf manager might decide to increase fan speed.

Critical Events

Critical events indicate that the blade is still within its operating limits, but it is close to exceeding one of those limits. Possible action in this case is to closely monitor the alarming sensor and take more aggressive action if it approaches the non-recoverable threshold.

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Non-Recoverable Events

Non-recoverable events indicate that the blade may no longer be functioning because it is now outside of its operating limits. It is likely that action is required or has already been taken by the local hardware/firmware. For example, a processor may have shut itself down because its maximum die temperature was exceeded, or a shelf manager may decide to deactivate the blade because the processor is too hot.

LED Visual Indicators

This section describes the front panel LED indicators on the CPC324.

Hot-Swap LED

The blue hot-swap LED, when illuminated, indicates that the CPC324 can safely be hot swapped (electrically). The impact on system operation depends on the application software being run.

The hot-swap LED can be controlled by the PLX PCI6254 L_STAT bit, the Zircon UL peripheral manager GPIO32, or the general purpose CPLD register. They are connected in an “OR” configuration. Any source can turn on the LED, but all must agree to turn it off.

SYSTEM LED

This LED is software programmable and can be green, yellow, or off. It is controlled by the general purpose CPLD register. Its meaning is dependent on the application software being run.

FAULT LED

This LED is software programmable and can be green, red, or off. It is controlled by the general purpose CPLD register. Its meaning is dependent on the application software being run.

Ethernet LEDs

This section describes the LEDs associated with the CPC324 Ethernet ports.

Management Port (Integrated LEDs)

The LEDs are built in to the RJ45 connector.

The ACT/LNK LED is directly connected to BCM5461s PHY. It uses the receive LED output set to activity/link mode to indicate the link status and transmit/receive activity. The green LED will turn on if there is a good link at any speed and will flash at a 167 ms (6Hz) rate, 50% duty cycle if link is established and there is transmit or receive activity. The LED will be off while the device is in reset.

Note: *This LED will blink ½ the speed of the BCM5388 LEDs (for the PICMG 2.16 link ports).*

The speed LED is directly connected to BCM5461s PHY. It uses a combination of the Link[2] and Link[1] outputs for the speed LED indication. The yellow speed LED will turn on when link is established at 1000 Mb. The yellow LED will be off for 10 Mb or 100 Mb link.

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See Figure 2-4, “RJ45 Management Port and LED Location,” on page 29.

CPSB Link Ports A and B

There is a separate ACT/LNK LED for the PICMG 2.16 CPSB Link Ports A and B. The LEDs are connected directly to the BCM5388 Ethernet Switch and illuminate green when an Ethernet link is established. They will flash at a 12 Hz rate if Transmit or Receive activity is detected.

See Figure 2-4, “RJ45 Management Port and LED Location,” on page 29.

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Chapter

3

Getting Started

Overview

The following topics are covered in this chapter:

- “Unpacking,” on page 57
- “System Requirements,” on page 58
- “Switches,” on page 58
- “Installing the CPC324,” on page 66
- “Blade Extraction,” on page 69
- “Installing a PMC/PTMC/PPMC Module,” on page 72
- “Handle Keys,” on page 75

Unpacking

Inspect the packing container for any damage. If this container appears damaged, immediately contact the company responsible for the shipping and report the damage before opening and unpacking the container. It is recommended that you also notify Performance Technologies (see “Customer Support and Services,” on page 15).

Caution:
To reduce the risk of damage to the CPC324, this equipment must be protected from electrostatic discharge (EMC) and physical shock. Never remove any of the socketed parts except in a static-free environment. Use the anti-static bag shipped with the product to handle the blade.

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Caution:
Avoid touching areas of integrated circuitry. Static discharge can damage these circuits.

System Requirements

Rear Access

In a rear access configuration, the CPC324 is installed in the front of the card cage and an RTM324 is installed in the rear part of the card cage. For more information about the RTM, see Chapter 6, “Rear Transition Module,” on page 97.

Environmental Requirements

Operating: 0° to 50° C (32° to 122° F)

Non-operating: -20° to 80° C (-4° to 176° F)

Power Requirements

The typical power consumption of the CPC324 (without a PTMC module installed) is shown in Table 3-1, “Blade Power Consumption,” below.

Table 3-1: Blade Power Consumption

Maximum Power Consumption	Voltage	Current	Power
CPC324 w/o PTMC	3.3V	4.5	15 W
	5V	2A	10 W
	+12V	5mA	60 mW
	-12V	-12V	40 mW

With 200 LFM cooling, each PTMC mezzanine slot can accommodate 15 W or a total of 30 W for both slots. This value is added to the base blade’s 25.1 W, for total power dissipation of 55.1 W maximum.

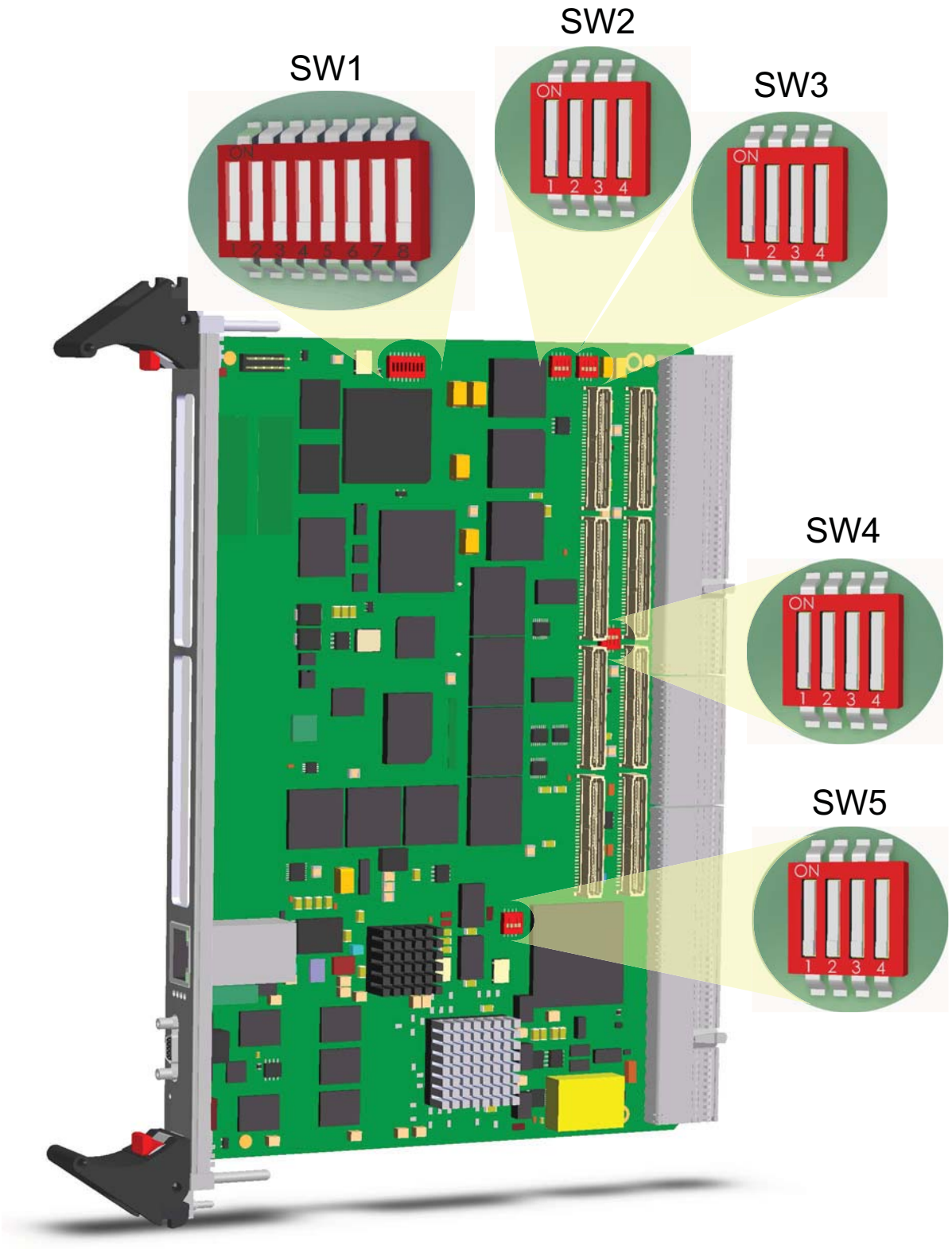
Switches

The CPC324 incorporates five switch banks, SW1-SW5, for configuring blade options. The following topics present the five switch banks in numerical order and provide a detailed description of each switch setting. Each switch in the switch banks are identified in the form SWx-N, where x is the switch bank and -N is the switch number (for example, SW2-3 means "switch bank 2, switch number 3").

See Figure 3-1, “CPC324 Switch Locations,” on page 59 for switch locations.

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Figure 3-1: CPC324 Switch Locations



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SW1

Table 3-2: SW1 Settings

Switch	Description	Off (1)	On (0)
SW1-1	HOT SWAP BLUE LED - This switch places the front panel blue hot-swap LED under the control of software and the on-board IPMC. Normally it should be enabled. • Enable - Software and the IPMC controls the hot-swap LED. **Normal position.** • Disable - Software and the IPMC does not control the hot-swap LED.	Disable	Enable
SW1-2	FORCE POWER ON - This switch bypasses the CompactPCI hot-swap BDSEL# [1] signal. It is used to force the CPC324 to power on regardless of backplane or chassis type. It should be normally disabled. • Enabled - Force blade to power on. • Disabled - Do not force blade power on. **Normal position.**	Disabled	Enabled
SW1-3	BREAK DETECT - This switch allows the 440GX MPU to reset on serial port break detect. It should be normally disabled. • Enabled - Reset on console port break detect. **Normal position.** • Disabled - Do not rest on console port break detect.	Disabled	Enabled
SW1-4	GIGSELA - This switch is used to set RMII and Ethernet PTMC connection options on PTMC slot 1 and 2. • Port 2 RMII connections (see Table 3-3 below). • Port 2 10/100/1000Base-T connections (see Table 3-3 below).	1	0
SW1-5	GIGSELB - This switch is used to set RMII and Ethernet PTMC connection options on PTMC slot 1 and 2. • Port 3 RMII connections (see Table 3-3 below). • Port 3 10/100/1000Base-T connections (see Table 3-3 below).	1	0
SW1-6	GIGSELC - This switch is used to set RMII and Ethernet PTMC connection options on PTMC slot 1 and 2. • Port 3 10/100/1000Base-T connections (see Table 3-3 below). • Port 3 10/100/1000Base-T connections (see Table 3-3 below).	1	0
SW1-7	JTG_TRST - This switch is used for factory diagnostic purposes to enable JTAG component chain. **It should always be left on to disable JTAG functions**. • Enabled - JTAG Test Reset off. • Disable - JTAG Test Reset on. **Normal position.**	Enabled	Disabled
SW1-8	CPU JTAG RST - This switch is used for factory diagnostic purposes to isolate 440GX JTAG header. Switch this to off if the JTAG based debugger is attached during power-on sequence as the debugger may hold TRTS high and prevent the TAP controller from being reset. **This switch should always be left on to disable JTAG functions**. • Enabled - 440GX JTAG reset off. • Disable - 440GX JTAG reset on. **Normal position.**	Enabled	Disabled

1. BDSEL# is used on CompactPCI hot-swap backplanes to control blade back-end power. On non-hot swap backplanes this signal is usually ground.

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PTMC Ethernet Ports

Two PTMC Configuration 2 mezzanine sites are provided on the CPC324. Each site provides support for MAC based RMII interfaces and 10/100/1000Base-T interfaces.

The interface is selected by user switch SW1 positions 4, 5, and 6, described in Table 3-2, “SW1 Settings,” on page 60. See Figure 3-1, “CPC324 Switch Locations,” on page 59 for switch locations. These switch settings control the RMII and 10/100/1G Ethernet data path mux. The database mux establishes connectivity to and from the on-board Ethernet switch ports 2 and 3 to PTMC A and PTMC B respectively. Note that switch port 3 can be redirected to PTMC A to provide two ports of 10/100/1000Base-T Ethernet connectivity. See Table 3-3, “PTMC A /B Ethernet Port Configuration Options,” below.

Table 3-3: PTMC A /B Ethernet Port Configuration Options

GIGSELC On=0, Off=1	GIGSELB On=0, Off=1	GIGSELA On=0, Off=1	Connections to PTMC A	Connections to PTMC B
0	0	0	Port 2 & 3 Ethernet	---
0	0	1	invalid	invalid
0	1	0	invalid	invalid
0	1	1	invalid	invalid
1	0	0	port 2 Ethernet	port 3 Ethernet
1	0	1	port 2 RMII	port 3 Ethernet
1	1	0	port 2 Ethernet	port 3 RMII
1	1	1	port 2 RMII	port 3 RMII

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SW2

Table 3-4: SW2 Settings

Switch	Description	Off (1)[1]	On (0)
SW2-1	P2PHYAD1	Port 2 PHY Address bit 1 = 0. **Normal position.**	Port 2 PHY Address bit 1 = 1
SW2-2	P2PHYAD0	Port 2 PHY Address bit 0 = 0. **Normal position.**	Port 2 PHY Address bit 0 = 1
SW2-3	P3PHYAD1	Port 3 PHY Address bit 1 = 0. **Normal position.**	Port 3 PHY Address bit 1 = 1
SW2-4	P3PHYAD0	Port 3 PHY Address bit 0 = 0. **Normal position.**	Port 3 PHY Address bit 0 = 1

1. Factory Default

SW3

Table 3-5: SW3 Settings

Switch	Description	Off (1)	On (0)
SW3-1	BUSMODE 2 signal to PTMC A slot. [1]	Off = 1	On = 0
SW3-2	BUSMODE 3 signal to PTMC A slot. [1]	Off = 1	On = 0
SW3-3	BUSMODE 4 signal to PTMC A slot. [1]	Off = 1	On = 0
SW3-4	PMEN - CPC324 power management may be controlled by the CPC324's on board Intelligent Platform Management Controller (IPMC) or off board by an Intelligent Shelf Manager (ISM) located elsewhere in the same card rack. Users should determine their preferred choice of management and configure SW3-4 appropriately as indicated by the following: • Enable - IPMC power control enabled. This setting is recommended for systems without an ISM. • Disable - IPMC power control disabled. This setting is recommended for systems with an ISM. If BDSEL is asserted via a backplane jumper, neither the ISM nor the IPMC will be able to turn off blade power. If the IPMC management controller is selected to control power and an ISM is present in the system, the ISM should not assert BDSEL. SW3-4 configurations do not disable the ISM from powering up the blade but may prevent the ISM from turning off blade power if set improperly.	Disable	Enable

1. User configured switches that may be used to implement busmode signals based on Common Mezzanine Card specification P1386.

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SW4

Table 3-6: SW4 Settings

Switch	Description	Off (1)	On (0)
SW4-1	PMC BUSMODE 2 signal to PTMC B slot (see Table 3-7 below). [1]	Off = 1	On = 0
SW4-2	PMC BUSMODE 3 signal to PTMC B slot (see Table 3-7 below). [1]	Off = 1	On = 0
SW4-3	PMC BUSMODE 4 signal to PTMC B slot (see Table 3-7 below). [1]	Off = 1	On = 0
SW4-4	EXTENDED DIAGS - Software readable by the 440GX MPU 0 = Run extensive memory test. 1 = Skip test for fast boot. **Normal position.**	Off = 1	On = 0

1. User configured switches that may be used to implement busmode signals based on Common Mezzanine Card specification P1386.

Table 3-7: BUSMODE Configuration Encoding

BUSMODE 4	BUSMODE 3	BUSMODE 2	Mode
0	0	0	Card Present Test: “Card Present” only if a card is plugged into the slot, no bus protocol should be used.
0	0	1	Return “Card Present if PCI capable and uses PCI protocol
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	No host present

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SW5

Table 3-8: SW5 Settings

Switch	Description	Off (1)	On (0)
SW5-1	H.110 PRECHARGE - This switch allows the H.110 termination resistors to pre charge. It should be enable for H.110 operation on CompactPCI in hot-swap applications otherwise it may be disabled.	Disabled	Enabled
SW5-2	STANDALONE - This switch allows the CPC324's PCI controller to drive PCI clock from it's own internal source when an external PCI system clock is not available. Standalone should be enabled in CompactPCI chassis when: • The PCI bus is not used (i.e. PCI_PRESENT# [1] signal is not valid in applications such as PICMG 2.16). • System host blade is not available to supply system clock in PCI Bus applications even though the PCI_PRESENT# signal is valid. Standalone - When disabled this switch allows the CompactPCI PCI bus termination resistors to pre charge. This switch should be disabled when the PCI_PRESENT# is valid and a system host is supplying system clock.	Disabled	Enabled
SW5-3	ENABLE ENUM - This switch is gated with the CompactPCI Bus PCI_PRESENT# signal. It allows CPC324 to drive ENUM# [2], which is controlled by the CPC324's PLX CompactPCI bus bridge interface controller. ENUM# is a CompactPCI bus hot-swap interrupt signal used to indicate a change in blade status. It should be enabled in CompactPCI hot-swap environments. • On = CompactPCI hot-swap ENUM# signal enabled. • Off = CompactPCI hot-swap ENUM# signal disabled.	Disabled	Enabled
SW5-4	SW_BYPASS - This switch is a special hot-swap override to generate HEALTHY# [3] in non-standard systems. When enabled, HEALTHY# will be generated, but only if the if the CPC324's hot-swap controller has established that blade power is good. • On = Generate override HEALTHY#. • Off = Generate normal HEALTHY#. **Normal position.**	Disabled	Enabled

1. PCI_PRESENT# serves two purposes. It allows a blade's CompactPCI bus interface to be appropriately configured when the CompactPCI Bus is not connected to the corresponding slot. In a hot-swap environment, it partially determines when the blade must locally manage the handle switch, Blue LED, ENUM# and quiescence of critical blade resources. When low, this active-low signal indicates that the CompactPCI Bus signals are connected to the corresponding slot.
2. The ENUM# signal is provided to notify the system host that either a blade has been freshly inserted or is about to be extracted. This signal informs the system host that the configuration of the system has changed. The system host then performs any necessary maintenance such as installing a device driver upon blade insertion, or quiescing a device driver and the blade, prior to the blade's extraction.
3. During hot-swap insertion the Host System software detects that the blade is present and orders it to power on. The CPC308's hardware connection layer indicates that it is powered up and healthy by asserting the HEALTHY# signal. The system then releases the blade from reset (using radial PCI_RST#), and allows it to be electrically connected.

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Power Control Switch Configurations

The CPC324 offers the following types of power control on the blade:

- Option override - blade powers up regardless of any other option settings
- ISM power control
- IPMC power control

Option Override

Setting switch SW1-2 to the ON position forces the blade to power up regardless of any other option settings. This switch is normally in the OFF position.

ISM Power Control

In many CompactPCI installations the Intelligent Shelf Manager (ISM), which is external to the blade, controls blade power by use of the CompactPCI signal BD-SEL# (connector J1, pin D15). When asserted (logical 0), BD-SEL# forces the blade to power up. Alternatively, this signal may be connected to a permanent logical level on the backplane. When BD-SEL# is asserted, the blade powers up and remains powered up.

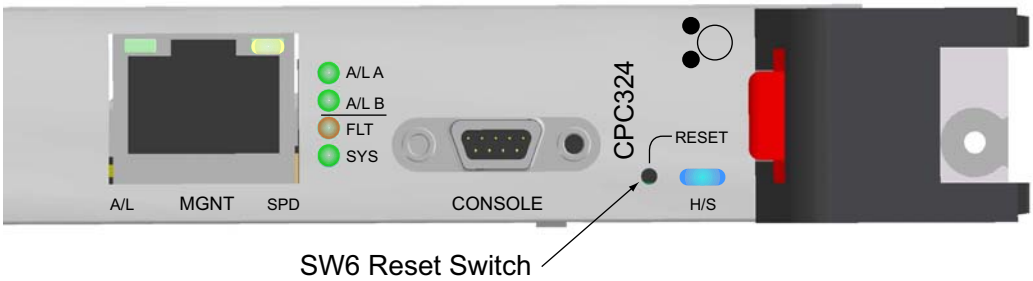
IPMC Power Control

Intelligent Peripheral Management Controller (IPMC) control of power is enabled when SW3-4 is ON. The IPMC then controls when power is applied to the blade. Note that this control is overridden by setting SW1-2 to ON or by asserting BD-SEL#. For IPMC power control to operate properly SW1-2 must be OFF and the BD-SEL# signal must be at logical high. The Intelligent Peripheral Management Controller is described in the section “Zircon UL Peripheral Monitor” on page 44.

Push-button Reset

SW6 is a push-button RESET switch, accessible from the front panel, shown in Figure 3-2 below. It generates !SYS_RESET_N, which is equivalent to the power-up reset generated by the DS1233A micro monitor.

Figure 3-2: SW6 Reset Switch Location



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Installing the CPC324

Warning:
Electronic components on printed circuit boards are extremely sensitive to static electricity. Ordinary amounts of static electricity generated by your clothing or work environment can damage the electronic equipment. It is required that when installing the CPC324 in a system that anti-static grounding straps and anti-static mats are used to help prevent damage due to electrostatic discharge.

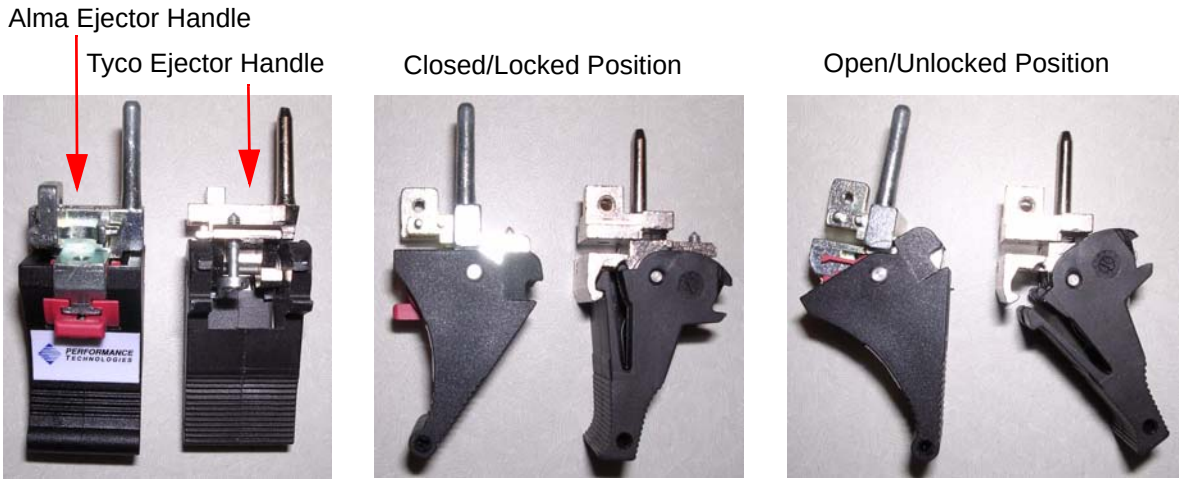
Before blade installation, consider the following mechanical aspects of the blade:

- The CPC324 has been tested for mechanical compatibility and installs in most systems without issue
- The CPC324 is PICMG 2.0, R3.0 compliant
- The CPC324 is PICMG 2.1, R2.0 hot-swap compliant.
- The CPC324 is PICMG 2.16, R1.0 Packet Switching Backplane compliant

Ejector Handles

There are two different types of ejector handles used on the CPC324. See Figure 3-3, “Ejector Handle Type Samples,” for the visual differences.

Figure 3-3: Ejector Handle Type Samples



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Installing the CPC324 in a Non Hot-Swap Chassis

Following are the steps to install the CPC324 in a non hot-swap CompactPCI chassis:

1. Quit all applications. Power down the chassis and any attached peripherals.
2. Configure the CPC324 as described in the following tables:
   - Table 3-2, “SW1 Settings,” on page 60
   - Table 3-3, “PTMC A /B Ethernet Port Configuration Options,” on page 61
   - Table 3-4, “SW2 Settings,” on page 62
   - Table 3-5, “SW3 Settings,” on page 62
   - Table 3-6, “SW4 Settings,” on page 63
   - Table 3-7, “BUSMODE Configuration Encoding,” on page 63
   - Table 3-8, “SW5 Settings,” on page 64
3. Select an available 6U, 32-bit (or 64-bit) CompactPCI slot.
4. Cock the ejector handles into the open position and slide the CPC324 into the chassis. Make sure the front plate on the CPC324 blade mounts flush with the chassis panel opening by using the ejector/injector handle to firmly seat the blade by locking the ejectors into the latched position.
5. Install and secure the front plate screws (one at the top of the blade and another under the ejector/injector handle) to secure the CPC324 blade into the chassis. This also provides a chassis ground connection to the CPC324.
6. Install the appropriate RTM into the chassis in the rear I/O slot associated with the blade slot, if required.
7. Reconnect any cables from peripheral devices.

This completes the hardware installation. At this point, turn power back on to the CompactPCI chassis and proceed to any software installation instructions that may have been provided.

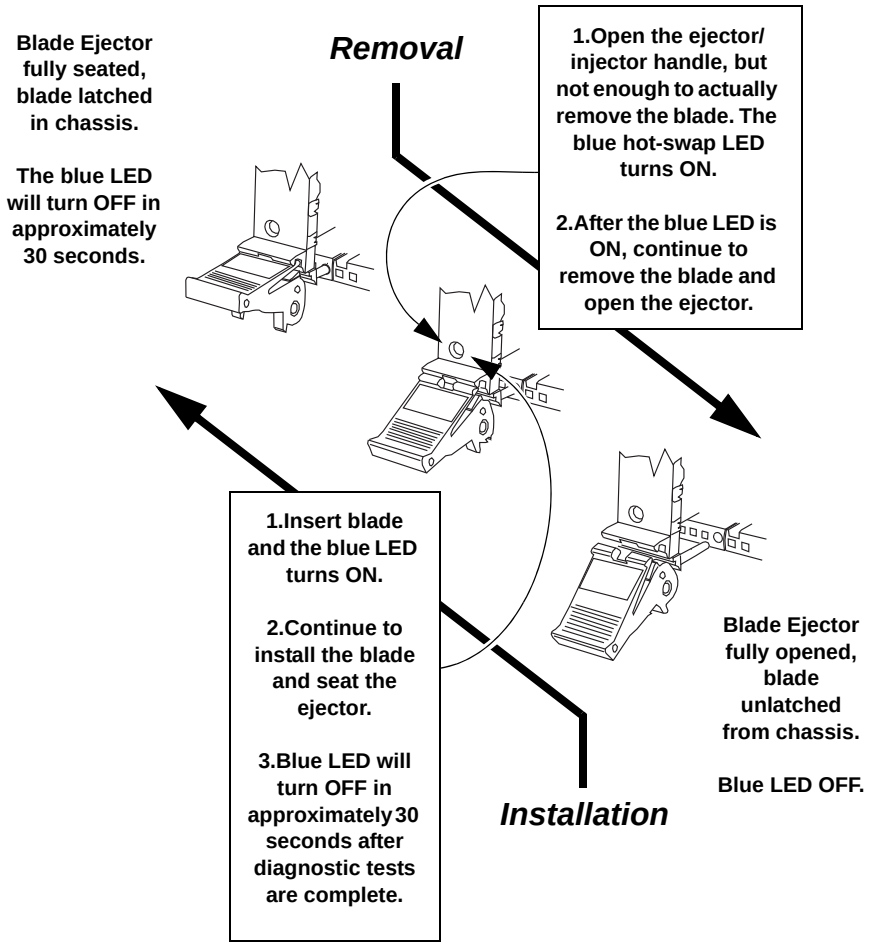
Installing the CPC324 in a Hot-Swap Chassis

The following procedure assumes the chassis power is on and the host supports hot-swap capabilities.

Note: *If an RTM is used, the chassis must be powered down to install or remove the RTM. Only the CPC324 front blade is hot-swap compatible.*

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Figure 3-4: Installing the CPC324



Following is the installation procedure for the CPC324:

1. Configure the CPC324 as described in the following tables:
   - Table 3-2, “SW1 Settings,” on page 60
   - Table 3-3, “PTMC A /B Ethernet Port Configuration Options,” on page 61
   - Table 3-4, “SW2 Settings,” on page 62
   - Table 3-5, “SW3 Settings,” on page 62
   - Table 3-6, “SW4 Settings,” on page 63
   - Table 3-7, “BUSMODE Configuration Encoding,” on page 63
   - Table 3-8, “SW5 Settings,” on page 64
2. Select an available 6U, 32-bit (or 64-bit) CompactPCI slot.
3. Cock the ejector handles into the open position and slide the blade into the chassis. Ensure the front plate on the blade mounts flush with the chassis panel opening by using the ejector/injector handle to firmly seat the blade by locking the ejector/injector into the latched position.

   When the blade makes contact with the CompactPCI backplane the blue hot-swap LED is illuminated and the hardware connection process begins. When the hardware connection process is complete the blue hot-swap LED turns OFF.

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4. Install and secure the front plate screws to secure the blade to the chassis. The screws also provide an electrical ground function.

   Note: *If an RTM is used, the chassis must be powered down to install the RTM.*

5. Install the appropriate RTM into the chassis in the rear I/O slot associated with the blade just installed.
6. Install the serial port cables to the RTM connectors.
7. Reconnect any cables from peripheral devices.

Blade Extraction

Hot-Swap Extraction

Following are instructions for extracting the CPC324:

1. Locate the blade to be removed.
2. Unscrew the front plate screws.
3. Open the ejector/injector handle just enough to unlock the handle but not enough to actually remove the blade. This will close the ejector/injector handle switch causing assertion of the ENUM interrupt to the host and sets the ENUM Status Indicator for blade removal bit. The host can write a 1 to the LED software ON/OFF switch bit to illuminate the blue hot-swap LED indicating the software is ready for the removal of the blade. The hardware connection process protects the hardware system from extractions if the blade is pulled before the blue hot-swap LED is illuminated.
4. After the blue hot-swap LED is illuminated open the ejector/injector handle fully to unseat the blade and remove it from the chassis.

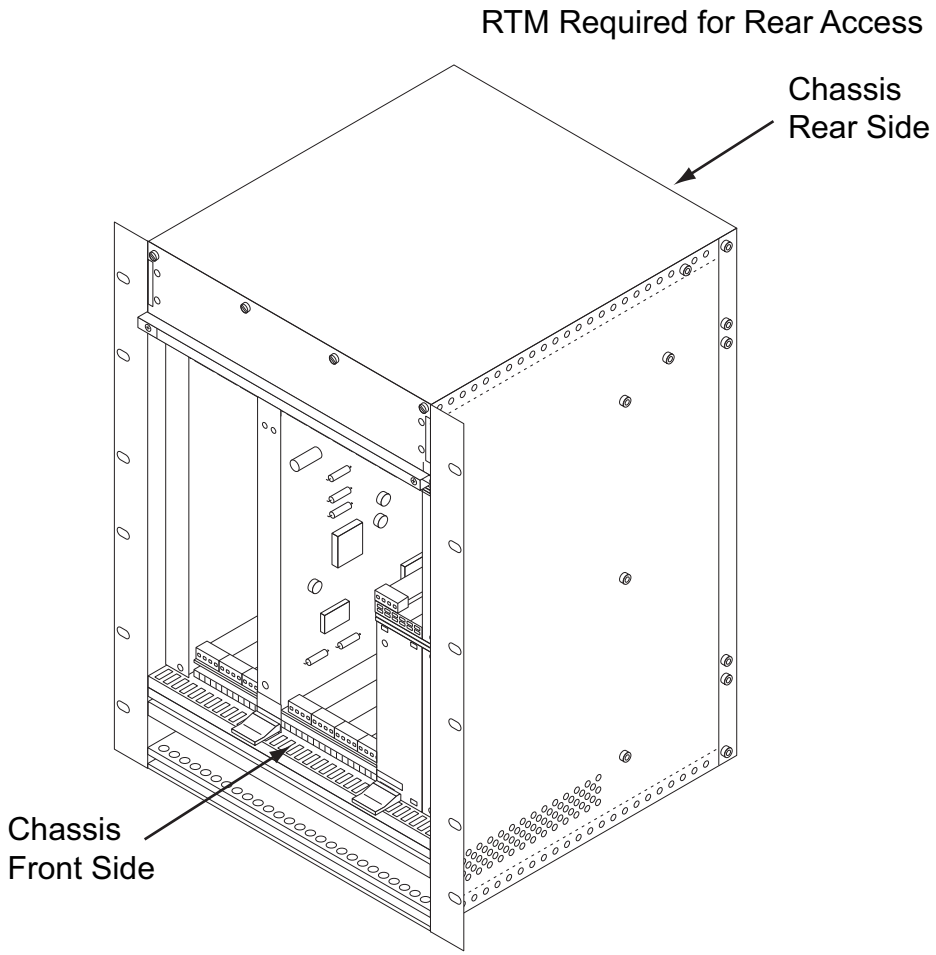
Non Hot-Swap Extraction

Following are instructions for extracting the CPC324:

1. Quit all applications. Power down the CPCI chassis and any attached peripherals.
2. Locate the blade to be removed.
3. Unscrew the front plate screws.
4. Open the ejector/injector handle and extract the blade.

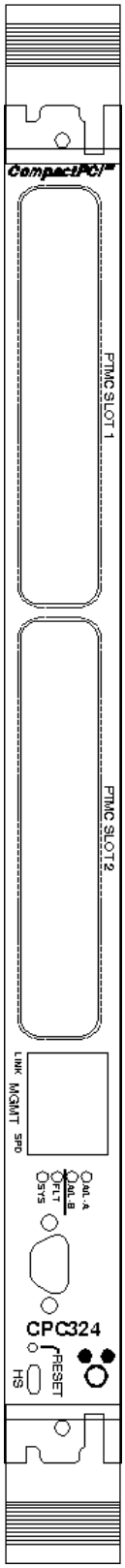
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Figure 3-5: CompactPCI Chassis



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Figure 3-6: CPC324 Front Panel



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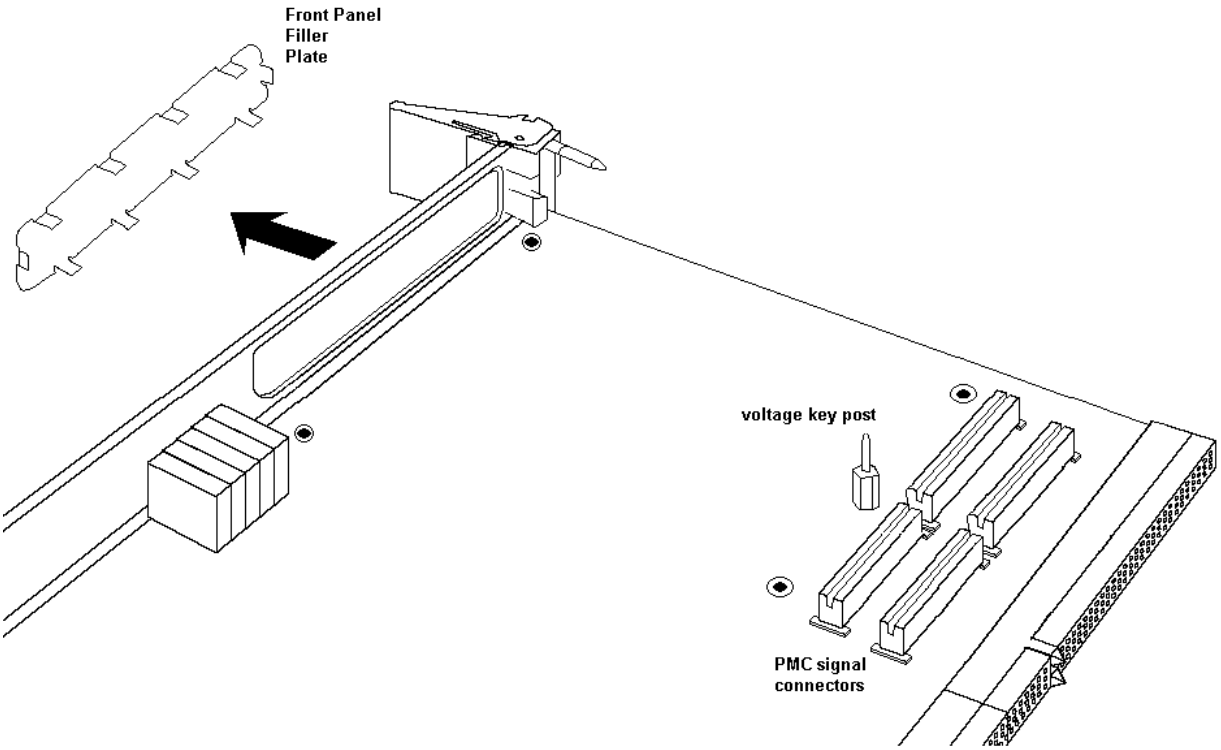
Installing a PMC/PTMC/PPMC Module

Warning:
Electronic components on printed circuit boards are extremely sensitive to static electricity. Ordinary amounts of static electricity generated by your clothing or work environment can damage the electronic equipment. It is recommended that when installing your PMC/PTMC/PPMC module in a system that anti-static grounding straps and anti-static mats are used to help prevent damage due to electrostatic discharge.

Following are instructions on installing a PMC module:

1. This view of the CPC324 shows the front panel opening, the voltage key post and the PMC signal connectors. Remove the filler plate from the front panel of the CPC324.

Figure 3-7: Top View of CPC324 (One of two PMC card slots shown)



2. The PMC card must be positioned with care to avoid damaging components against the voltage keying post. The next view expresses the proper alignment and rotation to install the PMC card. As the PMC bezel enters the front panel of the CPC324 lower the card into alignment with the signal connectors. Insure that the key post hole is properly aligned and press the PMC card to mate the connectors.

   Note: *The CPC324 can take two PMC cards or one as necessary. When a single card is populated the default location is PTMC Slot A.*

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Figure 3-8: PMC Card Side View

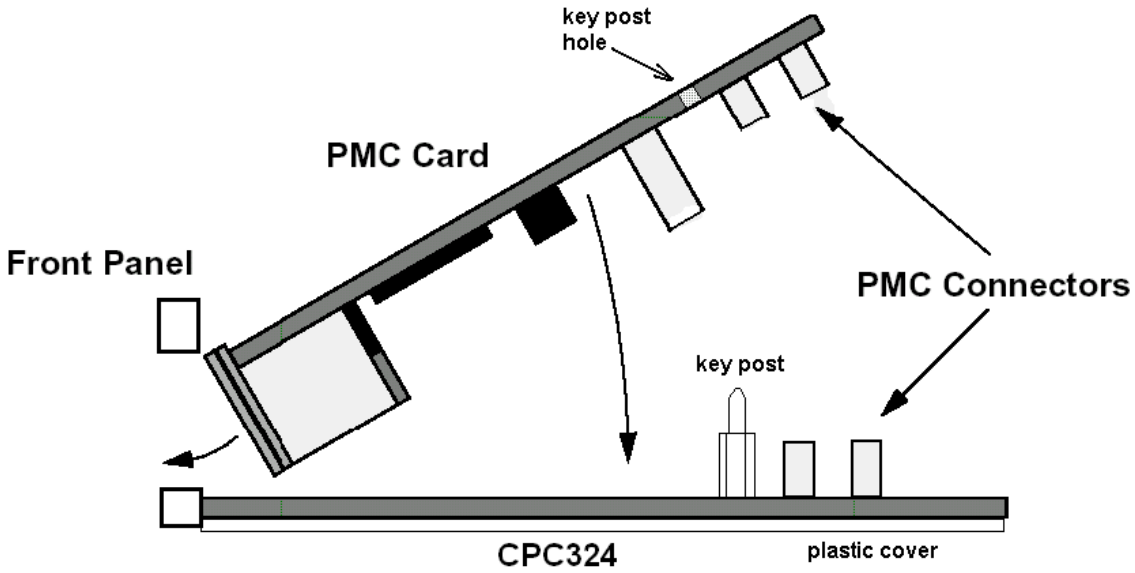
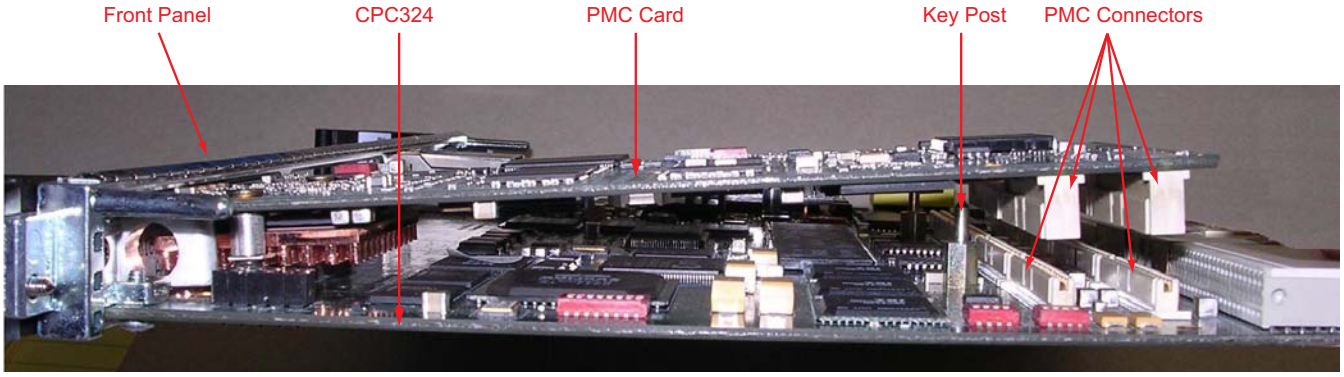


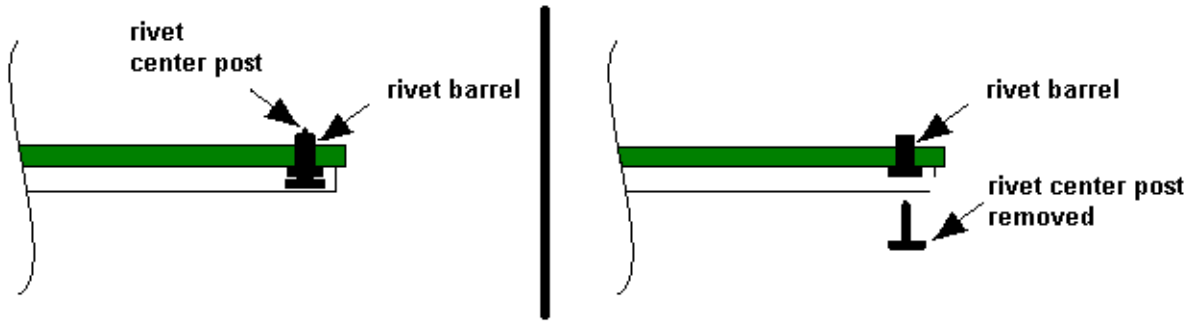
Figure 3-9: Side View PMC Card Installation



3. The plastic cover must be removed to apply the PMC card screws. Begin by removing the two plastic rivets that hold the plastic cover in place. Apply pressure on the rivet center post to extract them as shown. Then remove the rivet barrels.

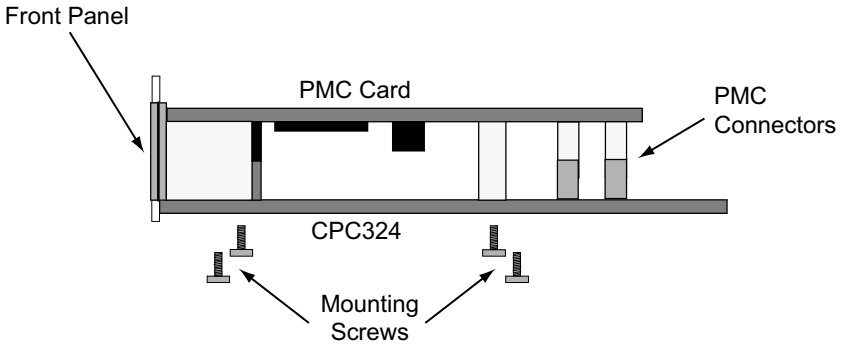
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Figure 3-10: Plastic Rivet Removal Example



4. The plastic cover can be rotated by removing one of the front panel screws and loosening the second screw about ½ turn.
5. Now install the screws provide with the PMC card.

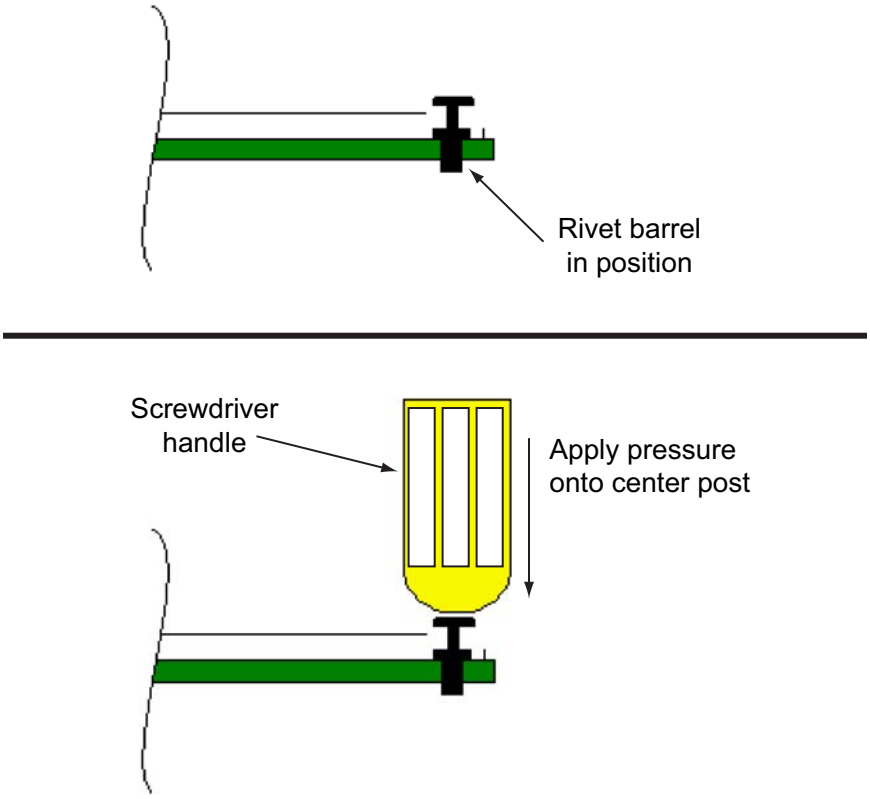
Figure 3-11: Side View of PMC Card Mounting Screws



6. Rotate the plastic cover back into proper position and reinstall the screws and plastic rivets. We suggest using fresh rivets rather than struggling with the deformed barrels of the used rivets. The rivet barrel must be positioned first, then using the handle of a large screwdriver apply pressure to the rivet center pin until it snaps into place. Tighten the front panel screws after the rivets are in place.

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Figure 3-12: Side View of Rivet Seating



7. Install any supplied cable(s) to your module.
8. Reinstall the CPC324 into the CompactPCI chassis.
9. Reconnect any cables from external devices.

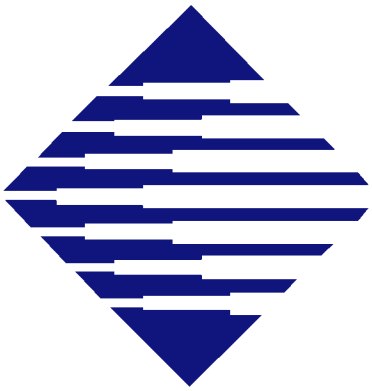
This completes the hardware installation. At this point, turn power back on to the units and proceed to any software installation instructions that may have been provided.

Handle Keys

The CPC324 is shipped with no handle keys installed. A bag of eight handle keys (Rittal 3684325) is provided with the CPC324. If it is desired to differentiate slot-specific, user-defined I/O functions, these keys can be installed by the user per *PICMG 2.10 Keying of CompactPCI Boards and Backplanes*.

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Chapter

4

Reset

Overview

This chapter discusses the various reset types and reset sources on the CPC324. Because many embedded systems have different requirements for blade reset functions, the incorporation of this sub-system on the CPC324 has been designed to provide maximum flexibility.

The following topics are covered in this chapter:

- “Reset,” on page 77
- “Reset Operation,” on page 78
- “Software Reset,” on page 78
- “Watchdog Timer Reset,” on page 78
- “Break Detector Reset,” on page 78
- “Push-button Reset,” on page 78

Reset

This section describes the initial state of the CPC324 after power-up reset or hardware reset, and describes the initialization of CPC324 peripherals and configuration registers required for application execution. In general, the contents of registers and other facilities within the 440GX core and external devices are configured to reset default states.

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Reset Operation

All devices on the CPC324, with the exception of the IPMC management controller may be reset by depressing the momentary push-button reset switch, SW6 located behind the front panel faceplate. This switch is connected to the system reset input on the 440GX MPU. When the system reset signal is asserted the 440GX responds by performing a board-level system reset. The system reset signal to the 440GX affects the processor core, all on-chip peripherals, and all devices connected to it or to the 440GX external reset out pin.

System reset can also be initiated or internally by software, from the IPMC controller, from the CompactPCI interface bridge chip, and from the Non-volatile SRAM reset signal.

Software Reset

A software system reset may be generated a system reset request from by the 440GX MPU processor core or the PCI power management logic. The duration of a system reset will last 10 system clocks beyond the longest of chip PLL locking.

Watchdog Timer Reset

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the watchdog register. The microprocessor can perform a write of the watchdog register. The time-out period then starts over.

Break Detector Reset

The RS232 console port can be monitored in hardware for loss of signal with the Break Detector monitor. The Breaker Detector, which is implemented in the CPLD. It is composed of a series of counters that have a 3 msec timeout period. If a receiver mark (binary 1) has not occurred with in a 3 msec window, a timeout occurs. If a mark has been received, the break detect counters will reset and restart the count process. If a timeout occurs the CPLD issues a hard reset to the AMCC 440GX by driving system reset active low. The break detect function is enabled by closing switch SW1–3 and disabled by setting to open (off) switch SW1-3. See “SW1,” on page 60 for jmore information.

Push-button Reset

SW6 is a push-button RESET switch, accessible through an access hole in the front panel. It generates complete board-level reset that is equivalent to the power-up reset. See Figure 3-2, “SW6 Reset Switch Location,” on page 65.

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Chapter

5

Connectors

Overview

The CPC324 includes several connectors to interface with application-specific devices. A brief description of each connector is given in Table 5-1, “Connector Assignments,” below.

A detailed description and pinout for each connector is given in the following topics.

Table 5-1: Connector Assignments

Connector	Location
“Console Port,” on page 80	Front Panel Connectors
“10/100/1G BASE-T Ethernet Management Port,” on page 81	
“PTMC Connectors,” on page 82	Internal Connectors
“Processor PMC Compatibility,” on page 85	
“PTMC J13/J23 and J14/J24 Connectors,” on page 87	
“Battery Backup Characteristics,” on page 90	
“CompactPCI J1/J2,” on page 92	CompactPCI Connectors
“CompactPCI J3,” on page 94	
“CompactPCI J4,” on page 95	
“CompactPCI J5,” on page 96	

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Front Panel Connectors

See Figure 2-1, “CPC324 Front Panel,” on page 19 for front panel connector locations.

Console Port

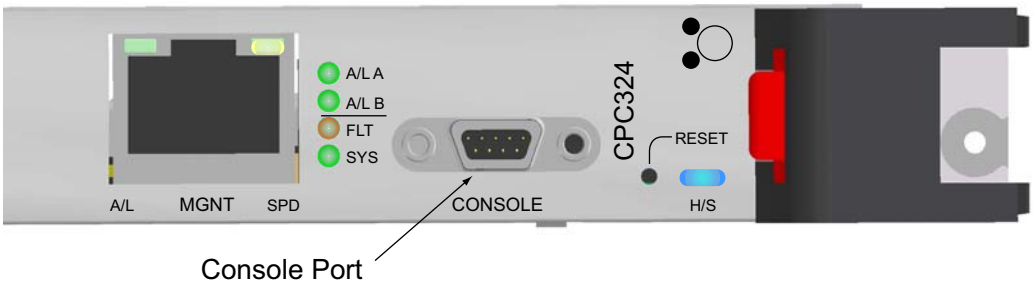
An RS232 interface to the 440GX MPU and the Zircon UL IPMC management controller is provided by a 9-pin micro D connector, located on the CPC324 front panel. Use PTI console port cable part number PT-ACC324-11977 (included with the software connectivity kit). The factory default console port baud rate is 9600.

Table 5-2, “Micro DB9F Console Port Pinout,” shows the Console Port pinout and Figure 5-1, “Console Port 9-Pin Submin "D" Location,” shows its location.

Table 5-2: Micro DB9F Console Port Pinout

Pin Number	Signal Name
1	nc
2	RXD from 440GX CPU
3	TXD from 440GX CPU
4	nc
5	gnd
6	nc
7	gnd
8	PMDBGRXD from IPMC
9	PMDBGTXD from IPMC

Figure 5-1: Console Port 9-Pin Submin "D" Location



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10/100/1G BASE-T Ethernet Management Port

Port 6 of the Broadcom BCM5388 Ethernet switch can be accessed through J7, an RJ45 connector located on the CPC324 faceplate. See Figure 2-4, “RJ45 Management Port and LED Location,” on page 29. This port supports 10/100/1G Ethernet. The RJ45 pinout is based on the Medium Dependent Interface (MDI) DTE-to-DTE of IEEE Std 802.3ab 2000 Edition CSMA/CD Access Method and Physical Layer Specification. The link topology supports a crossover function for a DTE-to-DTE connection. The J7 connector pinout is shown in Figure 5-2, “RJ45 Jack Pin Assignments,” below.

1000BASE-T Ethernet employs full duplex baseband transmission over four pairs of Category 5 balanced cabling. The 1000 Mb/s aggregate data rate is achieved by a transmission data rate of 250 Mb/s over each wire pair. Baseband signaling with a modulation rate of 125 MBaud is used on each of the wire pairs.

Figure 5-2: RJ45 Jack Pin Assignments

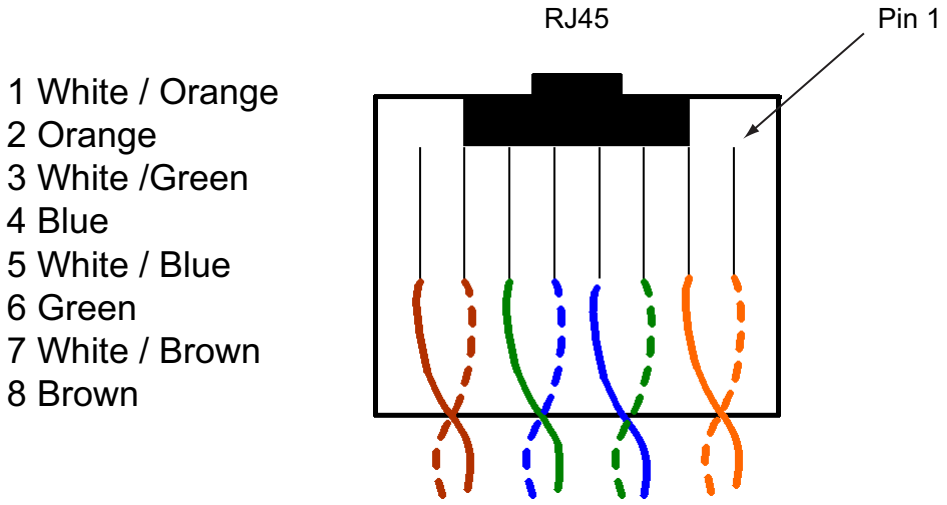


Table 5-3: 10/100/1G Management Connections

Contact Number	MDI	PTI	10/100 Base-T
1	BI_DA+	PHYB_DA+	TX+
2	BI_DA–	PHYB_DA-	TX-
3	BI_DB+	PHYB_DB+	RX+
4	BI_DC+	PHYB_DC+	
5	BI_DC–	PHYB_DC-	
6	BI_DB–	PHYB_DB-	RX-
7	BI_DD+	PHYB_DD+	
8	BI_DD–	PHYB_DD-	

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Internal Connectors

PTMC Connectors

There are two PTMC slots available, PTMC A and PTMC B. See Figure 5-3, “PTMC Slot and Connector Locations,” on page 84. The default location for a single populated mezzanine card is the PTMC A slot. PTMC A is designated by connectors J21- J24, which equate to the PTMC 2.15 specification pin mapping J1-J4 respectively. PTMC B is designated by connectors J11-J14, which equate to the PTMC 2.15 specification pin mapping J1-J4 respectively. Both sets of PTMC connectors carry all of the appropriate signals for the required operation of PTMC Configuration 2, which is comprised of TDM and RMII on J3 and user defined I/O on J4 pined. The J4 user I/O is pin mapped for PTMC Configuration 5 and is mapped for 10/100/1G Ethernet. See Table 5-4, “Generic Signals on PTMC J11/J21 and J12/J23 Connectors,” below.

The local PCI interface signals to the PTMC slots originate from the secondary PCI bus. A PCI bus controller is provided by a PLX PCI6254 dual PCI bridge. The CPC324 acts as the host processor and operates with PTMC mezzanine and PMC Processor cards configured as non-monarchs. The CPC324 supports one load per PTMC slot but does not support optional second PCI agents.

Table 5-4: Generic Signals on PTMC J11/J21 and J12/J23 Connectors

Pin	J11/J21 Signal	Pin	J11/J21 Signal	Pin	J12/J22 Signal	Pin	J12/J22 Signal
1	(TCK)[1]	2	-12V	1	+12V	2	TRST#[1]
3	GND	4	INTA#[2]	3	TMS[1]	4	TDO (tied to TDI)[1]
5	(INTB#)	6	(INTC#)	5	TDI (tied to TDO)[1]	6	GND
7	PRESENT#[3]	8	5V	7	GND	8	(PCI-Reserved)
9	(INTD#)	10	(PCI-Reserved)	9	(PCI-Reserved)	10	(PCI-Reserved)
11	GND	12	(3.3Vaux)	11	BUSMODE2#[4]	12	3.3V
13	PCICLK	14	GND	13	PCI_RST#	14	BUSMODE3#[4]
15	GND	16	GNT#	15	3.3V	16	BUSMODE4#[4]
17	REQ#	18	5V	17	(PME#)	18	GND
19	V3V (VI/O)	20	AD[31]	19	AD[30]	20	AD[29]
21	AD[28]	22	AD[27]	21	GND	22	AD[26]
23	AD[25]	24	GND	23	AD[24]	24	3.3V
25	GND	26	C/BE3#	25	IDSEL	26	AD[23]
27	AD[22]	28	AD[21]	27	3.3V	28	AD[20]
29	AD[19]	30	5V	29	AD[18]	30	GND
31	V3V (VI/O)	32	AD[17]	31	AD[16]	32	C/BE[2]#
33	FRAME#	34	GND	33	GND	34	IDSELB
35	GND	36	IRDY#	35	TRDY#	36	3.3V
37	DEVSEL#	38	5V	37	GND	38	STOP#
39	GND	40	LOCK#	39	PERR#	40	GND
41	(PCI-Reserved)	42	(PCI-Reserved)	41	3.3V	42	SERR#
43	PAR	44	GND	43	C/BE[1]#	44	GND

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Table 5-4: Generic Signals on PTMC J11/J21 and J12/J23 Connectors (Continued)

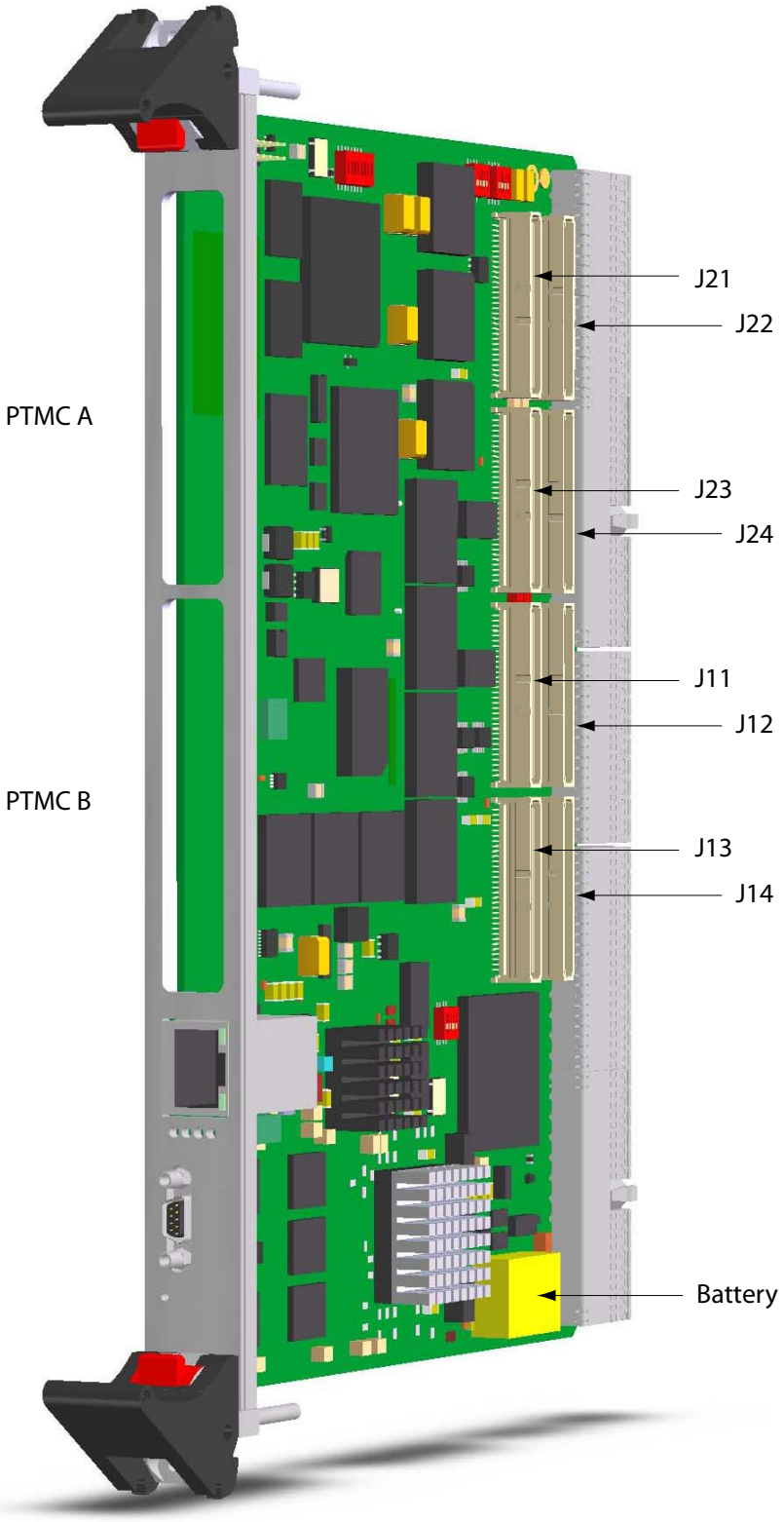
45	V3V (VI/O)	46	AD[15]	45	AD[14]	46	AD[13]
47	AD[12]	48	AD[11]	47	GND (M66EN)	48	AD[10]
49	AD[9]	50	5V	49	AD[8]	50	3.3V
51	GND	52	C/BE[0]#	51	AD[7]	52	REQB#[5]
53	AD[6]	54	AD[5]	53	3.3V	54	GNTB#
55	AD[4]	56	GND	55	(PMC-Reserved)	56	GND
57	V3V (VI/O)	58	AD[3]	57	(PMC-Reserved)	58	EREADY[3]
59	AD[2]	60	AD[1]	59	GND	60	RESETOUT#[3]
61	AD[0]	62	5V	61	pu (ACK64#)	62	3.3V
63	GND	64	pu (REQ64#)	63	GND	64	MONARCH#[6]

1. JTAG signals not implemented.
2. Input, maskable interrupt. Weak pull up.
3. Input, register readable by 440GX CPU. Weak pull up. New signal or new signal definition not in IEEE 1386.1.
4. Output, high or low switchable.
5. Weak pull up.
6. Weak pull up. New signal not in IEEE 1386.1.

Shaded areas denote no connection.

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Figure 5-3: PTMC Slot and Connector Locations



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Processor PMC Compatibility

Table 5-5, “Connector PTMC Signal Support List,” outlines how the Processor PMC (PrPMC) signals are supported on the CPC324 PTMC J11/J21 and J12/J22 connectors for each PTMC slot. These signals are generally per the PCI local bus specification except where noted.

Table 5-5: Connector PTMC Signal Support List

Signal Name	Signal Type	Notes
PCICLK	33 MHz PCI clock generated on the CPC324	
PCI_RST#	PCI reset generated by CPC324	
AD[31:0]	Tri-state bi-directional address/data lines	
C/BE[3:0]#	Tri-state bi-directional command and byte enable lines	
PAR	Tri-state bi-directional even parity across AD[31:0] and C/BE[3:0]#	
FRAME#	Tri-state bi-directional Cycle Frame Start signal	Pulled up on CPC324
IRDY#	Tri-state bi-directional Initiator Ready signal	Pulled up on CPC324
TRDY#	Tri-state bi-directional Transfer Ready signal	Pulled up on CPC324
STOP#	Tri-state bi-directional Stop Transaction signal	Pulled up on CPC324
LOCK#	Tri-state bi-directional Atomic Operation request signal	Pulled up on CPC324
IDSEL	Initialization Device Select signal wired to ADx for each slot	AD20 on PTMCA AD22 on PTMCB
IDSELB	Secondary device Initialization Device Select signal wired to ADx for each slot	AD21 on PTMCA AD23 on PTMCB
DEVSEL#	Tri-state bi-directional Device Select signal	Pulled up on CPC324
REQ#	Tri-state bi-directional request for bus mastership for PTMC A and B slots. REQ4# for PTMC A and REQ6# for PTMC B.	Pulled up on CPC324
REQB#	Secondary device tri-state bi-directional request for bus mastership for PTMC A and B slots. REQ5# for PTMC A and REQ7# for PTMC B.	Pulled up on CPC324
GNT#	Tri-state bi-directional bus mastership grant issued to this slot by the central arbiter for PTMC A and B slots. GNT4# for PTMC A and GNT6# for PTMC B.	Pulled up on CPC324
GNTB#	Secondary device tri-state bi-directional bus mastership grant issued by the central arbiter for PTMC A and B slots. GNT5# for PTMC A and GNT7# for PTMC B.	Pulled up on CPC324
PERR#	Tri-state bi-directional parity error signal	Pulled up on CPC324
SERR#	Tri-state bi-directional system error signal	Pulled up on CPC324
INTA#	Input, interrupts IRQ13 for PTMC A, and IRQ14 for PTMC B	Pulled up on CPC324
INTB# - INTD#	Unused	No connection
M66EN	Enable 66 MHz Clock	Grounded on CPC324 indicating 33 MHz operation
PME#	Open drain power management event	Not supported on CPC324. No connection to this pin.

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Table 5-5: Connector PTMC Signal Support List (Continued)

Signal Name	Signal Type	Notes
3.3Vaux		Not supported on CPC324. No connection to this pin.
REQ64#	Tri-state bi-directional request for 64 bit transfer	Only pulled up on CPC324. 64 bit transfers are not supported on the CPC324.
ACK64#	Tri-state bi-directional acknowledge for 64 bit transfer	Only pulled up on CPC324. 64 bit transfers are not supported on the CPC324.
PRESENT#	Board present indication signal	Pulled up on CPC324 and read by register location.
BUSMODE[2:4]	Bus mode signals indicate J11/J21 and bus operation mode compatibility	Switch selectable on CPC324
MONARCH#	Indication to PrPMC module that it is the PCI bus monarch	Pulled up on CPC324 indicating the CPC324 is always the monarch.
EREADY#	Open drain PrPMC output signal indicating that the PrPMC module is ready to be initialized	Pulled up by the CPC324 and read by a register location.
RESETOUT#	Open drain PrPMC output signal indicating that the PrPMC module is signaling the CPC324 to reset itself	Pulled up by the CPC324 and read by a register location.
3.3V	3.3V power	
5V	5V power	
V3V(VI/O)	PCI VIO hard wired to 3.3V	
GND	Digital ground	
nc	No connect on CPC324	

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PTMC J13/J23 and J14/J24 Connectors

The following tables (Table 5-6 and Table 5-7) outline how the TDM and Ethernet I/O signals are supported on the CPC324 PTMC J13/J23 and J14/J24 connectors for each PTMC slot. These signals are generally per the *PCI Telecom Mezzanine/Carrier Card Specification*, PICMG 2.15 and its ECN. The major exception to the standard is that the CPC324 supports type 2 mapping on J13/J23 and the type 5 mapping on J14/J24. The type 2 mapping was chosen to support the existing RMII type interface between the PTMC and the baseboard. The type 5 mapping was chosen on J14/J24 to allow for the newer 10/100/1G MDI pin assignments.

Table 5-6: PTMCA J13 - J14 Connectors

Pin	J13 Signal		Pin	Pin	J14 Signal		Pin
1	MDIO	GND	2	1	LPa_DA+	LPa_DC+	2
3	GND	nc (STX)	4	3	LPa_DA-	LPa_DC-	4
5	MDC	nc (SRX)	6	5	GND	GND	6
7	RXER	GND	8	7	LPa_DB+	LPa_DD+	8
9	PTID2	TXD0	10	9	LPa_DB-	LPa_DD-	10
11	PTGNDZ	TXD1	12	11	GND	GND	12
13	REFCLK	GND	14	13	LPb_DA+	LPb_DC+	14
15	GND	RXD0	16	15	LPb_DA-	LPb_DC-	16
17	LCT_FA	RXD1	18	17	GND	GND	18
19	LCT_FB	GND	20	19	LPb_DB+	LPb_DD+	20
21	PTID0	TXEN	22	21	LPb_DB-	LPb_DD-	22
23	PTGNDZ	CAS_DV	24	23	GND	GND	24
25	LCT_C8A	GND	26	25	USER	USER	26
27	GND	LCT_D19	28	27	USER	USER	28
29	LCT_D18	LCT_D17	30	29	USER	USER	30
31	LCT_D16	GND	32	31	USER	USER	32
33	GND	NETREF2	34	33	USER	USER	34
35	LCT_D14	USER1Z	36	35	USER	USER	36
37	LCT_D12	GND	38	37	USER	USER	38
39	PTENB#	USER2Z	40	39	USER	USER	40
41	PTGNDZ	NETREF1	42	41	USER	USER	42
43	LCT_C8B	GND	44	43	USER	USER	44
45	GND	LCT_D15	46	45	USER	USER	46
47	LCT_D10	LCT_D13	48	47	USER	USER	48
49	LCT_D8	LCT_D11	50	49	USER	USER	50
51	GND	LCT_D9	52	51	USER	USER	52
53	LCT_D6	LCT_D7	54	53	USER	USER	54
55	LCT_D4	GND	56	55	USER	USER	56
57	PTID1	LCT_D5	58	57	USER	USER	58
59	LCT_D2	LCT_D3	60	59	USER	USER	60
61	LCT_D0	GND	62	61	USER	USER	62
63	GND	LCT_D1	64	63	USER	USER	64

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Table 5-7: PTMCB J23 – J24 Connectors

Pin	J23 Signal		Pin	Pin	J24 Signal		Pin
1	MDIO	GND	2	1	LPa_DA+	LPa_DC+	2
3	GND	nc (STX)	4	3	LPa_DA-	LPa_DC-	4
5	MDC	nc (SRX)	6	5	GND	GND	6
7	RXER	GND	8	7	LPa_DB+	LPa_DD+	8
9	PTID2	TXD0	10	9	LPa_DB-	LPa_DD-	10
11	PTGNDZ	TXD1	12	11	GND	GND	12
13	REFCLK	GND	14	13	USER	USER	14
15	GND	RXD0	16	15	USER	USER	16
17	LCT_FA	RXD1	18	17	GND	GND	18
19	LCT_FB	GND	20	19	USER	USER	20
21	PTID0	TXEN	22	21	USER	USER	22
23	PTGNDZ	CAS_DV	24	23	GND	GND	24
25	LCT_C8A	GND	26	25	USER	USER	26
27	GND	LCT_D19	28	27	USER	USER	28
29	LCT_D18	LCT_D17	30	29	USER	USER	30
31	LCT_D16	GND	32	31	USER	USER	32
33	GND	NETREF2	34	33	USER	USER	34
35	LCT_D14	USER1Z	36	35	USER	USER	36
37	LCT_D12	GND	38	37	USER	USER	38
39	PTENB#	USER2Z	40	39	USER	USER	40
41	PTGNDZ	NETREF1	42	41	USER	USER	42
43	LCT_C8B	GND	44	43	USER	USER	44
45	GND	LCT_D15	46	45	USER	USER	46
47	LCT_D10	LCT_D13	48	47	USER	USER	48
49	LCT_D8	LCT_D11	50	49	USER	USER	50
51	GND	LCT_D9	52	51	USER	USER	52
53	LCT_D6	LCT_D7	54	53	USER	USER	54
55	LCT_D4	GND	56	55	USER	USER	56
57	PTID1	LCT_D5	58	57	USER	USER	58
59	LCT_D2	LCT_D3	60	59	USER	USER	60
61	LCT_D0	GND	62	61	USER	USER	62
63	GND	LCT_D1	64	63	USER	USER	64

The J13 and J24 connectors carry the various TDM and Ethernet style I/O signals to and from the PTMC module.

The CT bus implemented has some restrictions on it due to the limitations on the on-board TDM switch. The CT TDM data bits are bi-directional on a bus bit basis. They are unidirectional on a channel (TDM timeslot) basis within a bus bit. Therefore when a bus bit is configured to be an input or an output, all of the channels (TDM timeslots) on that bus bit are configured as input or output as well.

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The CPC324 internal TDM operates at 8.192 MHz and each bus bit stream can carry 128 TDM timeslots. On the TDM switch there are seven input and seven output streams allocated for PTMC operation. This allows for 896 TDM inputs and 896 TDM outputs. These available streams can be divided between the two PTMC slots on a stream-by-stream basis. Table 5-8, “PTMC to H.110 Switch TDM I/O Lines,” shows how they are mapped between the PTMC module and the TDM switch inputs and outputs.

Table 5-8: PTMC to H.110 Switch TDM I/O Lines

TDM Switch Output Port	PTMC A H.110 Lines	TDM Switch Input Port
STo 6	LCT_D0	STi 6
STo 7	LCT_D1	STi 7
STo 8	LCT_D2	STi 8
STo 9	LCT_D3	STi 9
STo 10	LCT_D4	STi 10
STo 11	LCT_D5	STi 11
STo 12	LCT_D6	STi 12
STo 6	LCT_D7	STi 6
STo 7	LCT_D8	STi 7
STo 8	LCT_D9	STi 8
STo 9	LCT_D10	STi 9
STo 10	LCT_D11	STi 10
STo 11	LCT_D12	STi 11
STo 12	LCT_D13	STi 12
STo 6	LCT_D14	STi 6
STo 7	LCT_D15	STi 7
STo 8	LCT_D16	STi 8
STo 9	LCT_D17	STi 9
STo 10	LCT_D18	STi 10
STo 11	LCT_D19	STi 11
STo 6	LCT_D1	STi 6
STo 7	LCT_D2	STi 7
STo 8	LCT_D3	STi 8
STo 9	LCT_D4	STi 9
STo 10	LCT_D5	STi 10
STo 11	LCT_D6	STi 11
STo 12	LCT_D7	STi 12
STo 6	LCT_D8	STi 6
STo 7	LCT_D9	STi 7
STo 8	LCT_D10	STi 8
STo 9	LCT_D11	STi 9
STo 10	LCT_D12	STi 10
STo 11	LCT_D13	STi 11
STo 12	LCT_D14	STi 12
STo 6	LCT_D15	STi 6

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Table 5-8: PTMC to H.110 Switch TDM I/O Lines (Continued)

TDM Switch Output Port	PTMC A H.110 Lines	TDM Switch Input Port
STo 7	LCT_D16	STi 7
STo 8	LCT_D17	STi 8
STo 9	LCT_D18	STi 9
STo 10	LCT_D19	STi 10
STo 11	LCT_D0	STi 11

Note: *You can apply a switch output to any LCT bit to which it is mapped on either PTMC slot. All of the assigned LCT bits can be active as outputs at the same time. The TDM switch inputs however, should be assigned individually and not be repeated either on a particular PTMC slot or between the PTMC slots.*

Battery Backup Characteristics

The battery backup circuit on the CPC324 contains a Snaphat® battery and crystal (M4T28-BR12SH1) with 48 mAH capacity. The expected battery life exceeds 10 years if the product is in storage at an ambient temperature of 30°C or lower.

Battery Replacement

Under normal operating conditions, it is not anticipated the battery will require replacement during the life of the product. Each customer must evaluate their operating conditions to determine if a battery maintenance program is required as part of a regular maintenance cycle for their board.

There are two options in the event the battery must be replaced:

- Return the board to Performance Technologies to have the battery replaced.
- Contact Performance Technologies to obtain a list of vendors of batteries approved for the product. You should also request detailed instructions for battery replacement in the field.

Note: *If you decide to replace the battery in the field, you are responsible for any damage that may occur to the board during battery replacement.*

Battery Voltage: 2.8 V

Battery Capacity: 48 mAh

Electrochemical Construction: Lithium (Li(CF)) battery

Battery Socket Location: See Figure 5-3, “PTMC Slot and Connector Locations,” on page 84.

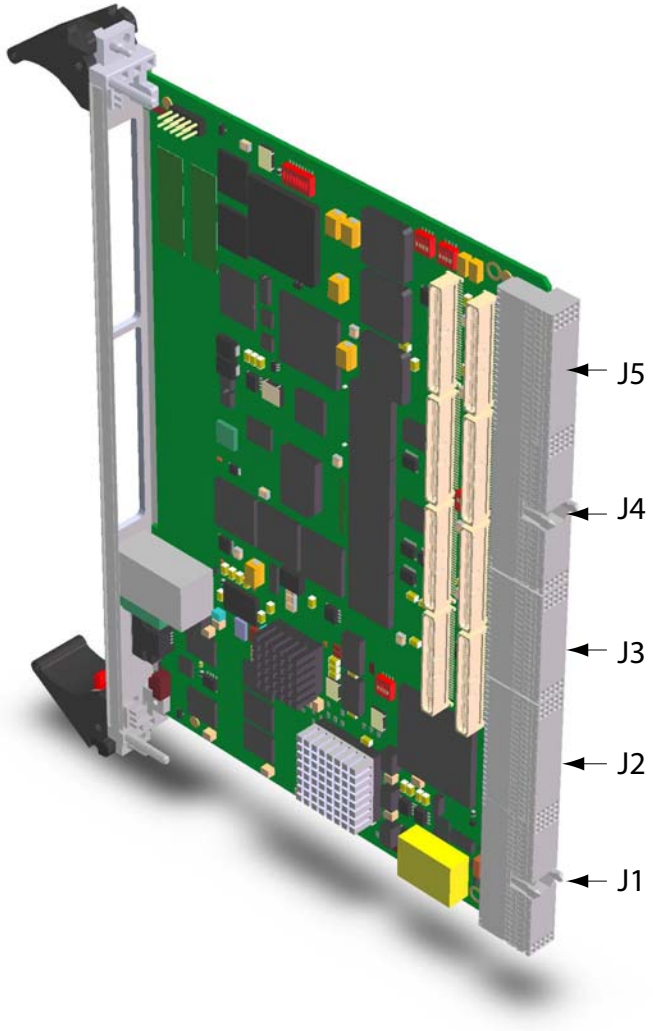
Caution:
The CPC324 contains a lithium battery. There is a danger of explosion if the battery is incorrectly replaced or handled. Do not disassemble or recharge the battery. Do not dispose of the battery in fire. When the battery is replaced, the same type or an equivalent type recommended by the manufacturer must be used. Used batteries must be disposed of according to the manufacturer’s instructions.

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CompactPCI Connectors

The CPC324 implements CompactPCI connectors J1 through J5. See Figure 5-4, “CompactPCI Connector Locations,” below. Their pin assignments are presented in the following sections.

Figure 5-4: CompactPCI Connector Locations



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CompactPCI J1/J2

The CompactPCI J1/J2 connectors are implemented as a standard 64-bit CompactPCI interface. Refer to the *CompactPCI Specification PICMG 2.0 Revision 3.0* for the definition of the signals.

The pinout is listed in Table 5-9, “CompactPCI J1 Pinouts,” and Table 5-10, “CompactPCI J2 Pinout,” on page 93.

Table 5-9: CompactPCI J1 Pinouts

Row Number	A	B	C	D	E	F
1	EVDD	-12V	TRST#	+12V	EVDD	Ground
2	TCK	EVDD	TMS	TDO	TDI	Ground
3	INTA#	INTB#	INTC#	LVDD	INTD#	Ground
4	VSM	HEALTHY#	LVIO	Reserved	Reserved	Ground
5	Reserved	Reserved	RST#	Ground	GNT#	Ground
6	REQ#	Ground	LV3V	CLK	AD31	Ground
7	AD30	AD29	AD28	Ground	AD27	Ground
8	AD26	Ground	EVIO	AD25	AD24	Ground
9	CBE3#	IDSEL	AD23	Ground	AD22	Ground
10	AD21	Ground	EV3V	AD20	AD19	Ground
11	AD18	AD17	AD16	Ground	CBE2#	Ground
12	Key	Key	Key	Key	Key	Key
13	Key	Key	Key	Key	Key	Key
14	Key	Key	Key	Key	Key	Key
15	EV3V	FRAME#	IRDY	BDSEL#	TRDY#	Ground
16	DEVSEL#	Ground	EVIO	STOP#	LOCK#	Ground
17	EV3V	IPMB_SCL	IPMB_SDA	Ground	PERR#	Ground
18	SERR#	Ground	EV3V	PAR	CBE1#	Ground
19	EV3V	AD15	AD14	Ground	AD13	Ground
20	AD12	Ground	EVIO	AD11	AD10	Ground
21	EV3V	AD9	AD8	M66EN	CBE0#	Ground
22	AD7	Ground	LV3V	AD6	AD5	Ground
23	EV3V	AD4	AD3	LVDD	AD2	Ground
24	AD1	EVDD	LVIO	AD0	ACK64#	Ground
25	EVDD	REQ64#	ENUM#	EV3V	EVDD	Ground

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Table 5-10: CompactPCI J2 Pinout

Row Number	A	B	C	D	E	F
1	NC	Ground	NC	NC	NC	Ground
2	NC	NC	NC	NC		Ground
3	NC	Ground	NC	NC	NC	Ground
4	EVIO	Reserved	CEB7#	Ground	CEB6#	Ground
5	CEB5#	64EN#	EVIO	CEB4#	PAR64	Ground
6	AD63	AD62	AD61	Ground	AD60	Ground
7	AD59	Ground	EVIO	AD58	AD57	Ground
8	AD56	AD55	AD54	Ground	AD53	Ground
9	AD52	Ground	EVIO	AD51	AD50	Ground
10	AD49	AD48	AD47	Ground	AD46	Ground
11	AD45	Ground	EVIO	AD44	AD43	Ground
12	AD42	AD41	AD40	Ground	AD39	Ground
13	AD38	Ground	EVIO	AD37	AD36	Ground
14	AD35	AD34	AD33	Ground	AD32	Ground
15	Reserved	Ground	NC	NC	NC	Ground
16	Reserved	Reserved	NC	Ground	Reserved	Ground
17	Reserved	Ground	NC	NC	NC	Ground
18	Reserved	Reserved	Reserved	Ground	Reserved	Ground
19	NC	NC	NC	NC	NC	Ground
20	NC	NC	NC	Ground	NC	Ground
21	NC	NC	NC	NC	NC	Ground
22	GA4	GA3	GA2	GA1	GA0	Ground

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CompactPCI J3

The CompactPCI J3 connector provides the PICMG 2.16 dual Ethernet bus and accepts the RTM ID bits. Table 5-11, “CompactPCI J3 Pinout,” lists the J3 pinouts.

Table 5-11: CompactPCI J3 Pinout

Row Number	A	B	C	D	E	F
19	GND	GND	GND	GND	GND	GND
18	LPa DA+	LPa DA-	GND	LPa DC+	LPa DC-	GND
17	LPa DB+	LPa DB-	GND	LPa DD+	LPa DD-	GND
16	LPb DA+	LPb DA-	GND	LPb DC+	LPb DC-	GND
15	LPbDB+	LPbDB-	GND	LPbDD+	LPbDD-	GND
14	NC	NC	GND	NC	NC	GND
13	NC	NC	NC	NC	NC	GND
12	NC	NC	NC	NC	NC	GND
11	NC	NC	NC	NC	NC	GND
10	NC	NC	NC	NC	NC	GND
9	NC	NC	NC	NC	NC	GND
8	NC	NC	NC	NC	NC	GND
7	NC	NC	NC	NC	NC	GND
6	NC	NC	NC	NC	NC	GND
5	NC	NC	NC	NC	NC	GND
4	RTM_ID0 [1]	RTM_ID1 [1]	NC	NC	NC	GND
3	RTM_ID2 [1]	RTM_ID3 [1]	RTM_ID4 [1]	NC	NC	GND
2	RTM_ID5 [1]	RTM_ID6 [1]	RTM_ID7 [1]	NC	NC	GND
1	NC	NC	NC	NC	NC	GND

1. RTM_ID[7:0] 8-bit rear panel RTM Identifier, zero ohm resistors to ground build option on RTM.

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CompactPCI J4

The CompactPCI J4 connector carries the H.110 CT Bus, which is implemented according to the *CompactPCI Computer Telephony Specification, PICMG 2.5 R1.0*. Refer to the specification for signal details. Table 5-12, “CompactPCI J4 Pinout,” lists the J4 pinouts.

Table 5-12: CompactPCI J4 Pinout

Row Number	A	B	C	D	E	F
25	SGA4	SGA3	SGA2	SGA1	SGA0	NC
24	GA4	GA3	GA2	GA1	GA0	NC
23	NC	CT_RESET#	CT_EN#	NC	CT_MC	NC
22	PFS0#	RSVD	RSVD	RSVD	RSVD	NC
21	NC	PFS1#	NC	NC	NC	NC
20	NP	NP	NP	NP	NP	NP
19	NP	NP	NP	NP	NP	NP
18	NC	NC	NC	NC	NC	NP
17	NP	NP	NP	NP	NP	NP
16	NP	NP	NP	NP	NP	NP
15	NC	NC	NC	NC	NC	NP
14	Key	Key	Key	Key	Key	Key
13	Key	Key	Key	Key	Key	Key
12	Key	Key	Key	Key	Key	Key
11	A_CTD29	A_CTD30	A_CTD31	HLVIO	A_CTFRMA#	Ground
10	A_CTD27	EV3V	A_CTD28	LVDD	A_CTFRMB#	Ground
9	A_CTD24	A_CTD25	A_CTD26	Ground	NC	Ground
8	A_CTD21	A_CTD22	A_CTD23	LVDD	A_CTC8A	Ground
7	A_CTD19	EVDD	A_CTD20	Ground	A_CTC8B	Ground
6	A_CTD16	A_CTD17	A_CTD18	Ground	A_CTNR1	Ground
5	A_CTD13	A_CTD14	A_CTD15	LV3V	A_CTNR2	Ground
4	A_CTD11	EVDD	A_CTD12	LV3V	NC	Ground
3	A_CTD8	A_CTD9	A_CTD10	Ground	NC	Ground
2	A_CTD4	A_CTD5	A_CTD6	A_CTD7	Ground	Ground
1	A_CTD0	EV3V	A_CTD1	A_CTD2	A_CTD3	Ground

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CompactPCI J5

The CompactPCI J5 connector provides the conduit between the CPC324 and the Rear Transition Module (RTM). The RTM provides transient voltage suppression, fuses, and isolation transformers to insure galvanic isolation from harmful electrical impulses that might occur on the trunk wires under fault cases. The CPC324 provides the first eight of 24 trunk connections. Table 5-13, “CompactPCI J5 Pinout,” lists the J5 pinouts.

For more information about the RTM, see Chapter 6, “Rear Transition Module,” on page 97.

Table 5-13: CompactPCI J5 Pinout

Row Number	A	B	C	D	E	F
22	RTIP3	RRING4	RTIP4	TRING4	TTIP4	NC
21	RRING3	RRING2	RTIP2	TRING3	TTIP3	NC
20	TTIP2	TRING1	TTIP1	RRING1	RTIP1	NC
19	TRING2	RRING6	RTIP6	RRING7	RTIP7	NC
18	RTIP8	TRING8	TTIP8	RRING5	RTIP5	NC
17	RRING8	TRING6	TTIP6	TRING7	TTIP7	NC
16	RTIP12	TRING12	TTIP12	TRING5	TTIP5	NC
15	RRING12	TRING11	TTIP11	RRING11	RTIP11	NC
14	TTIP9	RRING9	RTIP9	RRING10	RTIP10	NC
13	TRING9	RRING15	RTIP15	TRING10	TTIP10	NC
12	TTIP16	RRING13	RTIP13	RRING14	RTIP14	NC
11	TRING16	TRING15	TTIP15	RRING16	RTIP16	NC
10	TTIP20	TRING14	TTIP14	TRING13	TTIP13	NC
9	TRING20	RRING19	RTIP19	RRING20	RTIP20	NC
8	RTIP17	RRING18	RTIP18	TRING19	TTIP19	NC
7	RRING17	TRING18	TTIP18	TRING17	TTIP17	NC
6	RTIP21	RRING22	RTIP22	RRING23	RTIP23	NC
5	RRING21	RRING24	RTIP24	TRING24	TTIP24	NC
4	NC	TRING22	TTIP22	TRING23	TTIP23	NC
3	NC	NC	NC	TRING21	TTIP21	NC
2	RELAY_I1 [1]	NC	GND	GND	GND	NC
1	RELAY_O1 [2]	RELAY_O2 [2]	VDD	+12V	-12V	NC

1. Input, common relay return.
2. Output, independent relay drive.

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Chapter

6

Rear Transition Module

Overview

The RTM324 Rear Transition Module (RTM) provides rear-panel I/O connectivity for the CPC324.

The following topics are covered in this chapter:

- “Feature Summary,” on page 97
- “References,” on page 99
- “Functional Description,” on page 99
- “Switches and Jumper,” on page 102
- “Connector Pinouts,” on page 106
- “Cabling Reference,” on page 111
- “19" Break Out Box (BOB),” on page 113

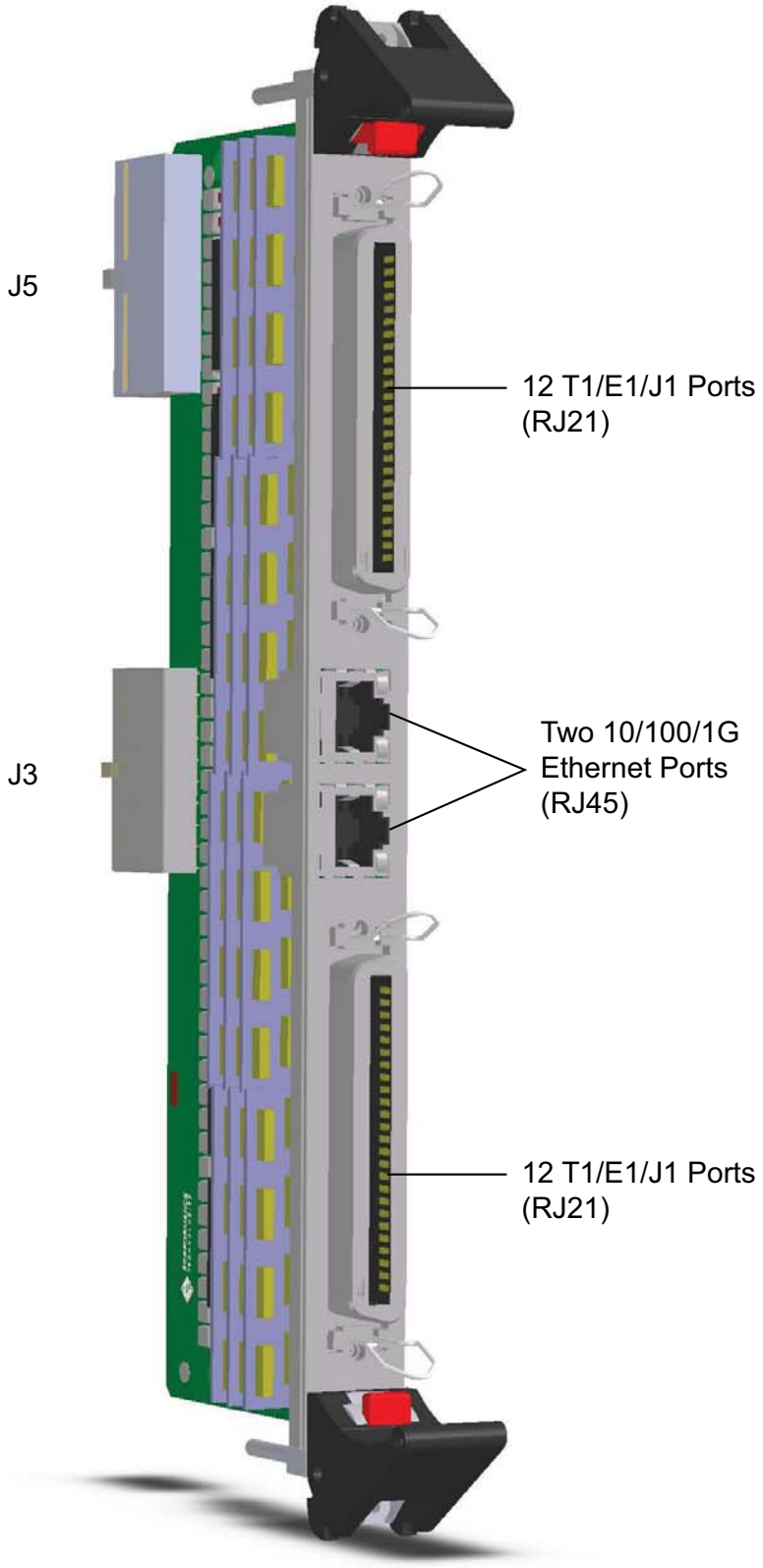
Feature Summary

The CPC324 uses the 24-port RTM324 (PT-RTM324-11965) for I/O connectivity. See Figure 6-1, “RTM324 Front Panel,” on page 98 for connector locations on the RTM324. The RTM324 contains the following features:

- 24 T1/E1/J1 port connections through two 50-pin, high density telco connectors (12 ports on each connector)
- Two 10/100/1G Ethernet node connections (configurable for PICMIG 2.16 or RJ45)
- 8-bit RTM identifier code presented to CPC324
- No active components

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Figure 6-1: RTM324 Front Panel



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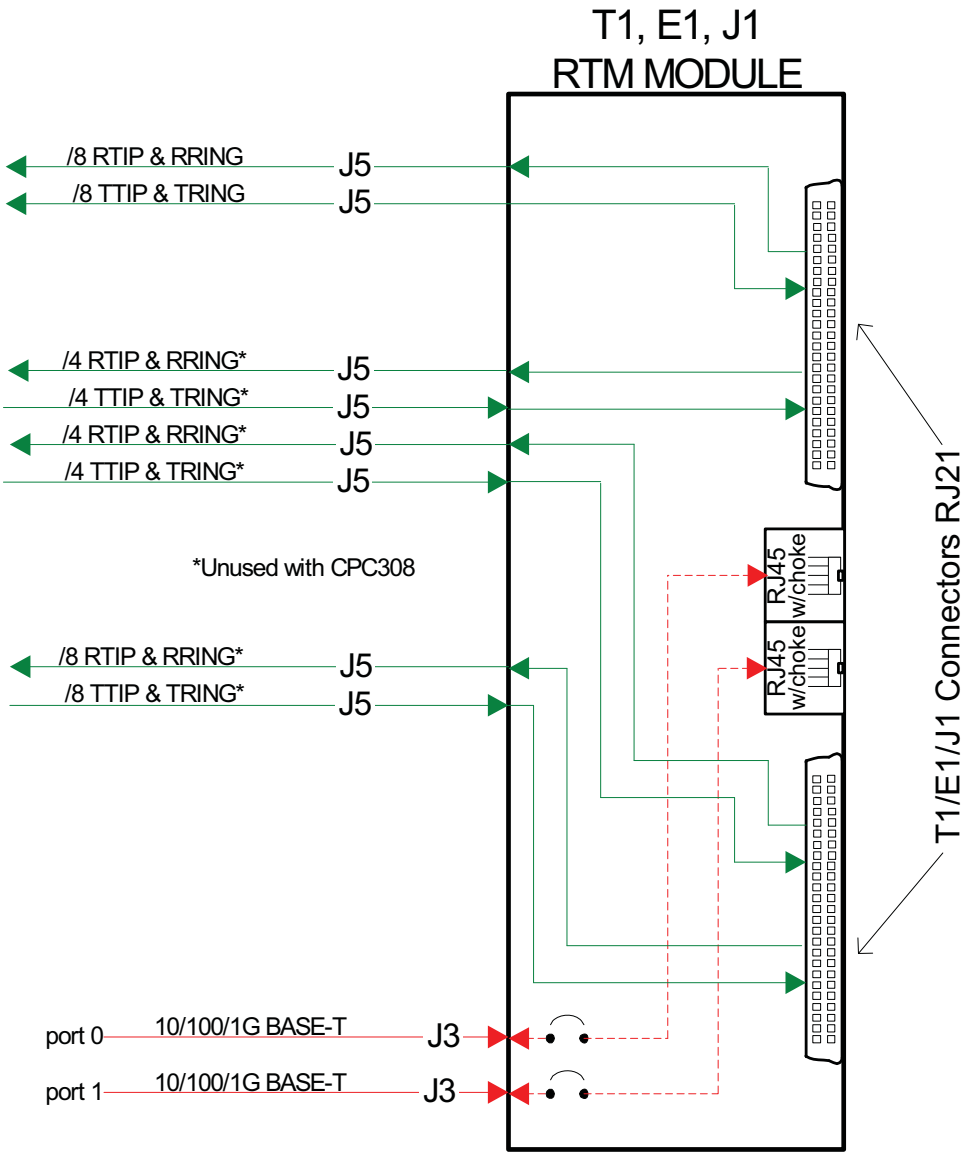
References

- PICMG 2.0 R 3.0 CompactPCI Core Specification
- PICMG 2.16 R1.0 CompactPCI Packet Switch Backplane
- IEEE Std. 802.3ab 2000 Edition CSMA/CD Access Method and Physical Layer Specification
- Teccor Electronics SIDACtor Data Book and Design Guide (http://www.teccor.com)
- IDT Reference Design “S8J Demo Schematic PCB2-28.pdf” (http://www.idt.com)

Functional Description

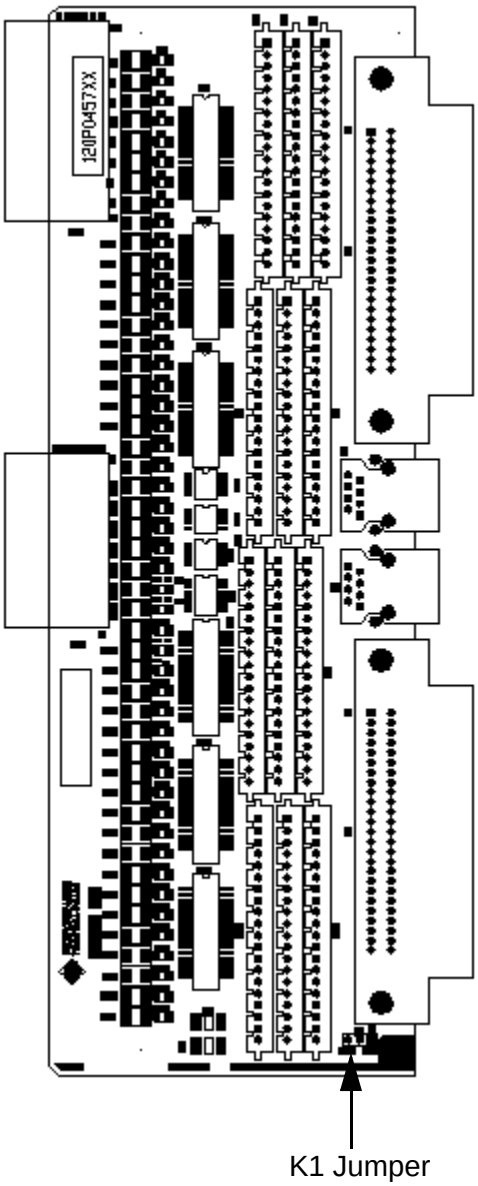
Figure 6-2, “RTM324 Block Diagram,” and Figure 6-3, “RTM324 Jumper Location,” on page 100 present diagrams of the RTM324.

Figure 6-2: RTM324 Block Diagram



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Figure 6-3: RTM324 Jumper Location



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The RTM324 provides 24 T1/E1/J1 port connections through two 50-pin high density RJ21 connectors (12 ports on each connector). These can be converted to standard RJ48 modular jacks using two RJ21 to RJ21 cables (ACC324-11968) and a rack mountable 19" break-out-box (BOB) that converts the RJ21 to RJ48. See “19" Break Out Box (BOB),” on page 113.

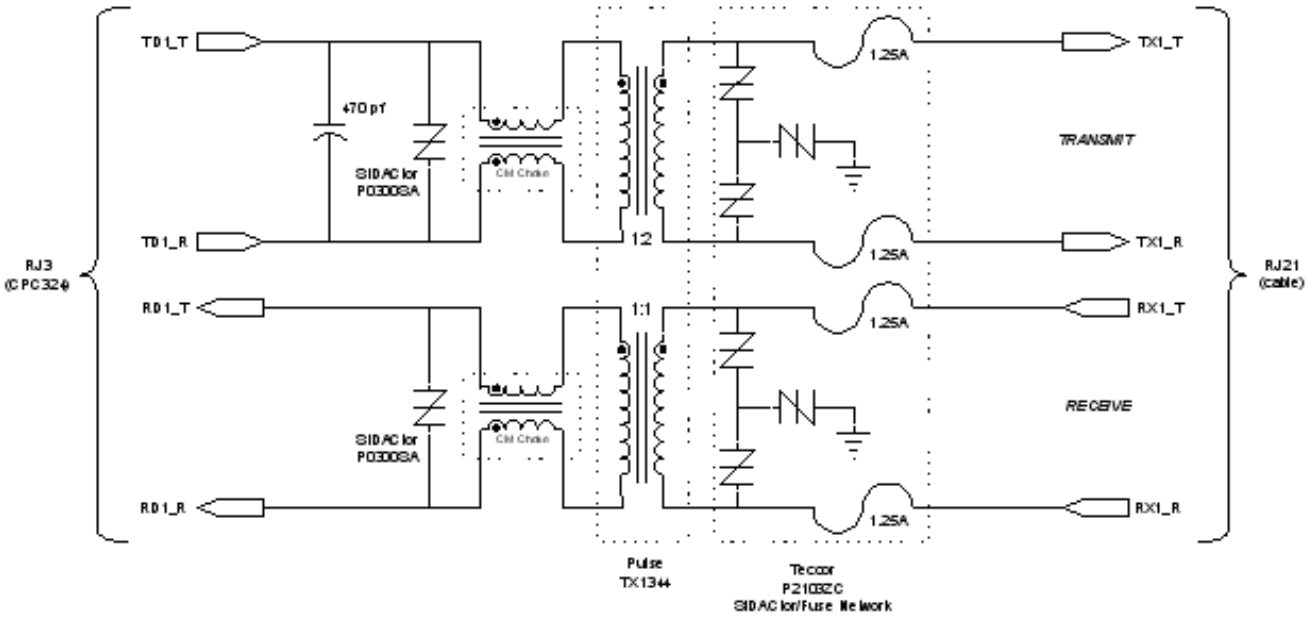
Connections to the CompactPCI backplane are provided by:

- Unshielded Type AB (with tabs) J5 connector, similar to unshielded twisted pair (UTP)
- Shielded Type AB (with tabs) RJ3 connector, for enhanced shielding of 10/100/1G Ethernet signals

The RTM324 provides magnetics and protection for the T1/E1/J1 ports. The receive terminating resistors are located on the CPC324.

One port of the circuit is shown in Figure 6-4, “Magnetics and Protection for T1/E1/J1 Ports,” below.

Figure 6-4: Magnetics and Protection for T1/E1/J1 Ports



In addition, two RJ45 connectors on the RTM faceplate provide 10/100/1G Ethernet connectivity. The magnetics for Ethernet reside on the CPC324 blade.

An 8-bit RTM identifier code is determined by factory installed zero ohm resistors and a switch for Ethernet routing. Table 6-1, “RTM Identifier,” presents the RTM Identifiers for the RTM324 configurations.

Table 6-1: RTM Identifier

# of T1/E1/J1 Ports / Ethernet Connection	RTM324 Identifier
24-port / CPSB 2.16 backplane	E0h
24-port / External	E1h
8-port / CPSB 2.16 backplane	E2h
8-port / External	E3h

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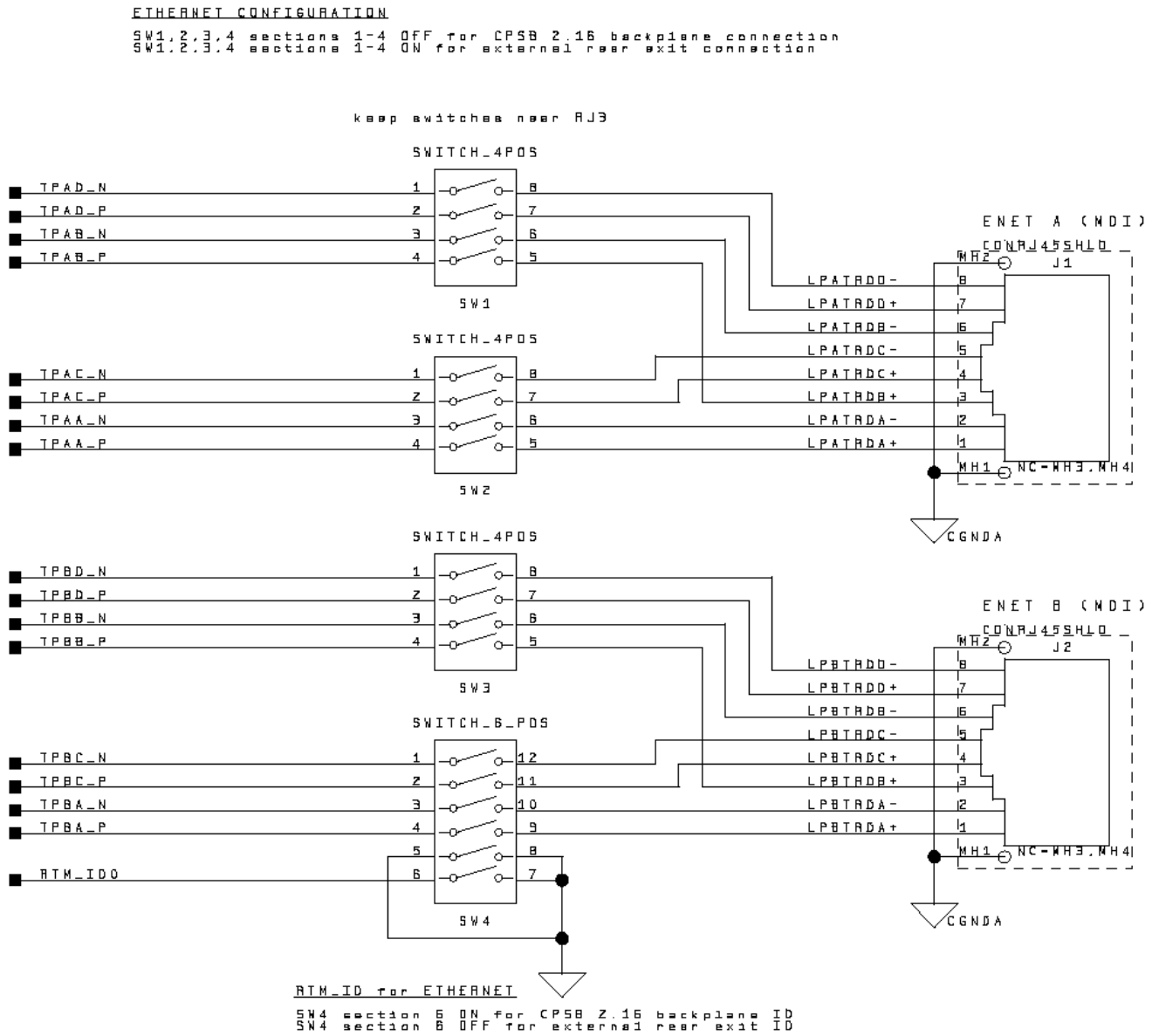
Switches and Jumper

10/100/1G BASE-T Ethernet Interface Configuration

The RTM324 has two Ethernet port connections that can be set to exit through a pair of RJ45 connectors mounted on the rear panel or through the RJ3 backplane connections. See Figure 6-5, “RTM Switch Flow Diagram,” below.

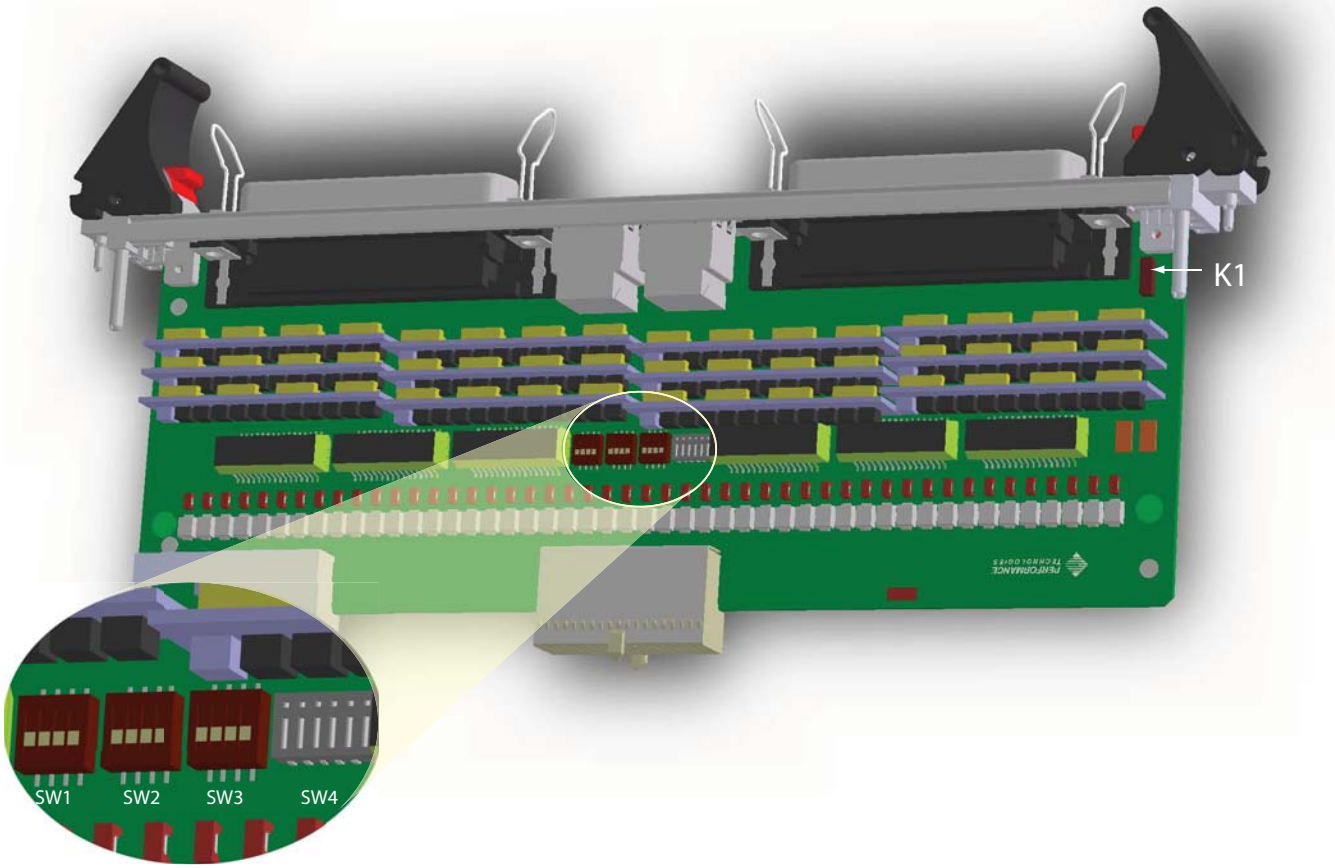
Figure 6-6, “RTM324 Switch Locations,” on page 103 shows switch and jumper locations for the RTM.

Figure 6-5: RTM Switch Flow Diagram



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Figure 6-6: RTM324 Switch Locations



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Switch Settings

The following tables (Table 6-2 and Table 6-3) show the switch settings for Port A options.

Table 6-2: SW1 for Ethernet Port A Routing

Switch Section	External (Rear Exit)[1]	CPSB 2.16 Backplane Connection
SW1-1	On	Off
SW1-2	On	Off
SW1-3	On	Off
SW1-4	On	Off

1. Factory Default

Table 6-3: SW2 for Ethernet Port A Routing

Switch Section	External (Rear Exit)[1]	CPSB 2.16 Backplane Connection
SW2-1	On	Off
SW2-2	On	Off
SW2-3	On	Off
SW2-4	On	Off

1. Factory Default

The following tables (Table 6-4 and Table 6-5) shows the switch settings for Port B options:.

Table 6-4: SW3 for Ethernet Port B Routing

Switch Section	External (Rear Exit)[1]	CPSB 2.16 Backplane Connection
SW3-1	On	Off
SW3-2	On	Off
SW3-3	On	Off
SW3-4	On	Off

1. Factory Default

Table 6-5: SW4 for Ethernet Port B Routing

Switch Section	External (Rear Exit)[1]	CPSB 2.16 Backplane Connection
SW4-1	On	Off
SW4-2	On	Off
SW4-3	On	Off
SW4-4	On	Off

1. Factory Default

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Table 6-6, “SW4 for Ethernet Configuration Identifier,” shows the switch settings for Ethernet configuration identification.

Table 6-6: SW4 for Ethernet Configuration Identifier

Switch Section	External (Rear Exit)[1]	CPSB 2.16 Backplane Connection
SW4-5	Off (not used)	On (not used)
SW4-6	Off*	On

1. Factory Default

Ground Isolation

Jumper K1 connects chassis ground to digital ground when installed across pins 1 and 2. The default condition is across pins 2 and 3, providing isolation of chassis and digital ground.

See Table 6-7, “Jumper K1 for Digital/Chassis Ground,” and Figure 6-3, “RTM324 Jumper Location,” on page 100 for jumper K1’s location.

Table 6-7: Jumper K1 for Digital/Chassis Ground

Jumper	Digital and Chassis Ground Connected	Digital and Chassis Ground Isolated [1]
K1	1-2	2-3

1. Factory Default

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Connector Pinouts

- “CompactPCI RJ3 Pinout,” on page 106
- “CompactPCI J5 Pinout,” on page 107
- “Ethernet J1 and J2 Pinout,” on page 108
- “RJ21 P1 and P2 Pinout,” on page 109

CompactPCI RJ3 Pinout

The RJ3 accepts the PICMG 2.16 dual Ethernet bus and RTM ID bits. The pinout is listed in Table 6-8, “CompactPCI RJ3 Pinout,” below.

Table 6-8: CompactPCI RJ3 Pinout

Row Number	A	B	C	D	E	F
19	GND	GND	GND	GND	GND	GND
18	LPaDA+	LPaDA-	GND	LPaDC+	LPaDC-	GND
17	LPaDB+	LPaDB-	GND	LPaDD+	LPaDD-	GND
16	LPbDA+	LPbDA-	GND	LPbDC+	LPbDC-	GND
15	LPbDB+	LPbDB-	GND	LPbDD+	LPbDD-	GND
14	NC	NC	GND	NC	NC	GND
13	NC	NC	NC	NC	NC	GND
12	NC	NC	NC	NC	NC	GND
11	NC	NC	NC	NC	NC	GND
10	NC	NC	NC	NC	NC	GND
9	NC	NC	NC	NC	NC	GND
8	NC	NC	NC	NC	NC	GND
7	NC	NC	NC	NC	NC	GND
6	NC	NC	NC	NC	NC	GND
5	NC	NC	NC	NC	NC	GND
4	RTM_ID0 [1]	RTM_ID1 [1]	NC	NC	NC	GND
3	RTM_ID2 [1]	RTM_ID3 [1]	RTM_ID4 [1]	NC	NC	GND
2	RTM_ID5 [1]	RTM_ID6 [1]	RTM_ID7 [1]	NC	NC	GND
1	NC	NC	NC	NC	NC	GND

1. RTM_ID[7:0] 8-bit rear panel RTM Identifier, zero ohm resistors to ground build option.

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CompactPCI J5 Pinout

The CompactPCI J5 connector implements the telephone I/O trunk segments per the *Compact PCI Computer Telephony Specification, PICMG 2.5 R1.0.*

Table 6-9, “CompactPCI J5 Pinout,” lists the T1/E1/J1 trunks and their pin assignments. The addition of the dark shaded cells are a trunk configuration for the CPC324, which allow J5 to carry all 24 trunks. The table cells not shaded are PICMG recommended pinouts to meet TNV1-SELV requirements.

Table 6-9: CompactPCI J5 Pinout

Row Number	A	B	C	D	E	F
22	RTIP3	RRING4	RTIP4	TRING4	TTIP4	NC
21	RRING3	RRING2	RTIP2	TRING3	TTIP3	NC
20	TTIP2	TRING1	TTIP1	RRING1	RTIP1	NC
19	TRING2	RRING6	RTIP6	RRING7	RTIP7	NC
18	RTIP8	TRING8	TTIP8	RRING5	RTIP5	NC
17	RRING8	TRING6	TTIP6	TRING7	TTIP7	NC
16	RTIP12	TRING12	TTIP12	TRING5	TTIP5	NC
15	RRING12	TRING11	TTIP11	RRING11	RTIP11	NC
14	TTIP9	RRING9	RTIP9	RRING10	RTIP10	NC
13	TRING9	RRING15	RTIP15	TRING10	TTIP10	NC
12	TTIP16	RRING13	RTIP13	RRING14	RTIP14	NC
11	TRING16	TRING15	TTIP15	RRING16	RTIP16	NC
10	TTIP20	TRING14	TTIP14	TRING13	TTIP13	NC
9	TRING20	RRING19	RTIP19	RRING20	RTIP20	NC
8	RTIP17	RRING18	RTIP18	TRING19	TTIP19	NC
7	RRING17	TRING18	TTIP18	TRING17	TTIP17	NC
6	RTIP21	RRING22	RTIP22	RRING23	RTIP23	NC
5	RRING21	RRING24	RTIP24	TRING24	TTIP24	NC
4	NC	TRING22	TTIP22	TRING23	TTIP23	NC
3	NC	NC	NC	TRING21	TTIP21	NC
2	RELAY_I1 [1]	NC	GND	GND	GND	NC
1	RELAY_O1 [2]	RELAY_O2[2]	VDD	+12V	-12V	NC

1. Input, common relay return.
2. Output, independent relay drive.

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Ethernet J1 and J2 Pinout

The RTM Ethernet port A and port A are wired as MDI. Table 6-9, “CompactPCI J5 Pinout,” and Table 6-11, “J2 Ethernet Connector Pinout,” show the pinout for these connections.

See Figure 6-1, “RTM324 Front Panel,” on page 98 for connector location information.

Table 6-10: J1 Ethernet Connector Pinout

Pin Number	Signal Name
1	LPaTRDA+
2	LPaTRDA-
3	LPaTRDB+
4	LPaTRDC+
5	LPaTRDC-
6	LPaTRDB-
7	LPaTRDD+
8	LPaTRDD-

Table 6-11: J2 Ethernet Connector Pinout

Pin Number	Signal Name
1	LPbTRDA+
2	LPbTRDA-
3	LPbTRDB+
4	LPbTRDC+
5	LPbTRDC-
6	LPbTRDB-
7	LPbTRDD+
8	LPbTRDD-

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RJ21 P1 and P2 Pinout

Applicable to the 24-port RTM324, 50-pin female RJ21 connectors P1 and P2 permit attachment to a pair of T1/E1/J1 Hydra cables, each terminating in 12 RJ48C receptacles. P1 supports ports 1-12 and P2 supports ports 13-24.

The P1 pinout is shown in Table 6-12, “RJ21 P1 Pinout,” and the P2 pinout is shown in Table 6-13, “RJ21 P2 Pinout,” on page 110.

Figure 6-1, “RTM324 Front Panel,” on page 98 provides connector location information.

Table 6-12: RJ21 P1 Pinout

Pin Number	Signal	Signal	Pin Number
1	Channel 1 TX1 Ring	Channel 1 TX1 Tip	26
2	Channel 1 RX1 Ring	Channel 1 RX1 Tip	27
3	Channel 2 TX1 Ring	Channel 2 TX1 Tip	28
4	Channel 2 RX1 Ring	Channel 2 RX1 Tip	29
5	Channel 3 TX1 Ring	Channel 3 TX1 Tip	30
6	Channel 3 RX1 Ring	Channel 3 RX1 Tip	31
7	Channel 4 TX1 Ring	Channel 4 TX1 Tip	32
8	Channel 4 RX1 Ring	Channel 4 RX1 Tip	33
9	Channel 5 TX1 Ring	Channel 5 TX1 Tip	34
10	Channel 5 RX1 Ring	Channel 5 RX1 Tip	35
11	Channel 6 TX1 Ring	Channel 6 TX1 Tip	36
12	Channel 6 RX1 Ring	Channel 6 RX1 Tip	37
13	Channel 7 TX1 Ring	Channel 7 TX1 Tip	38
14	Channel 7 RX1 Ring	Channel 7 RX1 Tip	39
15	Channel 8 TX1 Ring	Channel 8 TX1 Tip	40
16	Channel 8 RX1 Ring	Channel 8 RX1 Tip	41
17	Channel 9 TX1 Ring	Channel 9 TX1 Tip	42
18	Channel 9 RX1 Ring	Channel 9 RX1 Tip	43
19	Channel 10 TX1 Ring	Channel 10 TX1 Tip	44
20	Channel 10 RX1 Ring	Channel 10 RX1 Tip	45
21	Channel 11 TX1 Ring	Channel 11 TX1 Tip	46
22	Channel 11 RX1 Ring	Channel 11 RX1 Tip	47
23	Channel 12 TX1 Ring	Channel 12 TX1 Tip	48
24	Channel 12 RX1 Ring	Channel 12 RX1 Tip	49
25	---	---	50

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Table 6-13: RJ21 P2 Pinout

Pin Number	Signal	Signal	Pin Number
1	Channel 13 TX1 Ring	Channel 13 TX1 Tip	26
2	Channel 13 RX1 Ring	Channel 13 RX1 Tip	27
3	Channel 14 TX1 Ring	Channel 14 TX1 Tip	28
4	Channel 14 RX1 Ring	Channel 14 RX1 Tip	29
5	Channel 15 TX1 Ring	Channel 15 TX1 Tip	30
6	Channel 15 RX1 Ring	Channel 15 RX1 Tip	31
7	Channel 16 TX1 Ring	Channel 16 TX1 Tip	32
8	Channel 16 RX1 Ring	Channel 16 RX1 Tip	33
9	Channel 17 TX1 Ring	Channel 17 TX1 Tip	34
10	Channel 17 RX1 Ring	Channel 17 RX1 Tip	35
11	Channel 18 TX1 Ring	Channel 18 TX1 Tip	36
12	Channel 18 RX1 Ring	Channel 18 RX1 Tip	37
13	Channel 19 TX1 Ring	Channel 19 TX1 Tip	38
14	Channel 19 RX1 Ring	Channel 19 RX1 Tip	39
15	Channel 20 TX1 Ring	Channel 20 TX1 Tip	40
16	Channel 20 RX1 Ring	Channel 20 RX1 Tip	41
17	Channel 21 TX1 Ring	Channel 21 TX1 Tip	42
18	Channel 21 RX1 Ring	Channel 21 RX1 Tip	43
19	Channel 22 TX1 Ring	Channel 22 TX1 Tip	44
20	Channel 22 RX1 Ring	Channel 22 RX1 Tip	45
21	Channel 23 TX1 Ring	Channel 23 TX1 Tip	46
22	Channel 23 RX1 Ring	Channel 23 RX1 Tip	47
23	Channel 24 TX1 Ring	Channel 24 TX1 Tip	48
24	Channel 24 RX1 Ring	Channel 24 RX1 Tip	49
25	---	---	50

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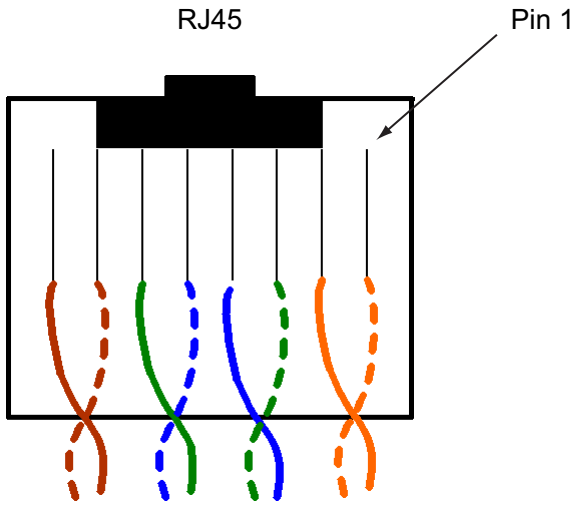
Cabling Reference

- “10/100/1G BASE-T Ethernet RJ45 Plug Pin Assignments,” on page 111
- “10/100/1G BASE-T Ethernet Loopback Plug Configuration,” on page 111
- “T1/E1/J1 Loopback Plug Configuration,” on page 112

10/100/1G BASE-T Ethernet RJ45 Plug Pin Assignments

Figure 6-7: Eight Position RJ45 Plug Pin Assignments

1 White / Orange
2 Orange
3 White /Green
4 Blue
5 White / Blue
6 Green
7 White / Brown
8 Brown



10/100/1G BASE-T Ethernet Loopback Plug Configuration

To create a loopback plug, connect the following RJ45 pins together, as shown in Table 6-14, “Ethernet RJ45 Connector,” below.

Table 6-14: Ethernet RJ45 Connector

Contact
1 to 3
2 to 6
4 to 7
5 to 8

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T1/E1/J1 Loopback Plug Configuration

To create a looback plug, connect the following RJ48C pins together.

See Figure 6-8, “RJ48C Plug Pin Assignment,” and Table 6-15, “T1/E1/J1 RJ48C Connector,” below.

Figure 6-8: RJ48C Plug Pin Assignment

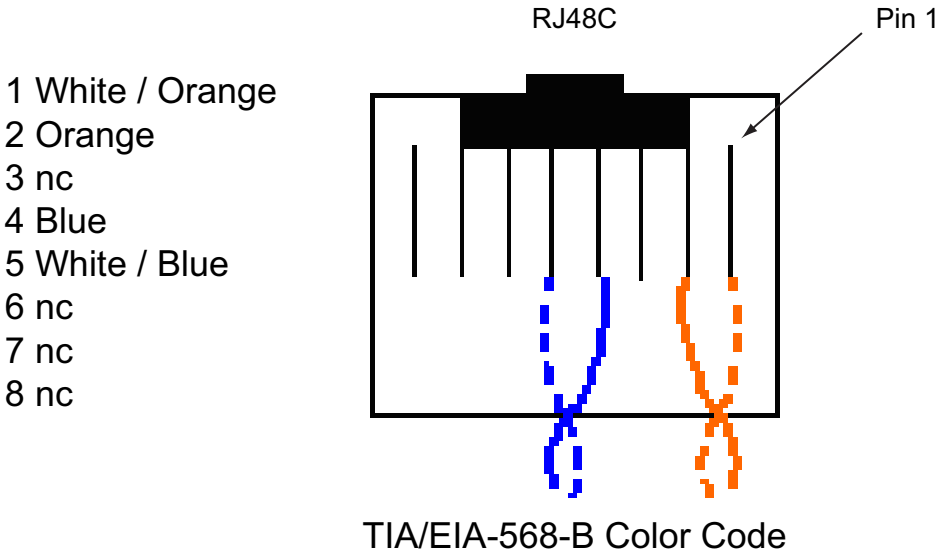


Table 6-15: T1/E1/J1 RJ48C Connector

Contact
1 to 4
2 to 5

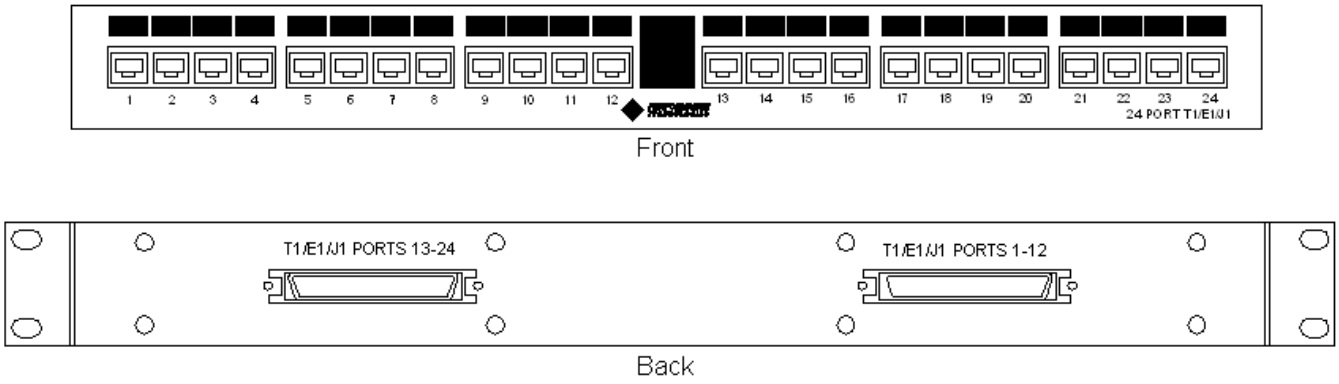
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19" Break Out Box (BOB)

The 19" Break Out Box (BOB) (ACC324-11967) is an accessory for the RTM324. The BOB attaches to the front of a system rack that connects the two RJ21 connections from the RTM324 to the two RJ21 connections on the BOB via two RJ21-to-RJ21 cables (ACC324-11968).

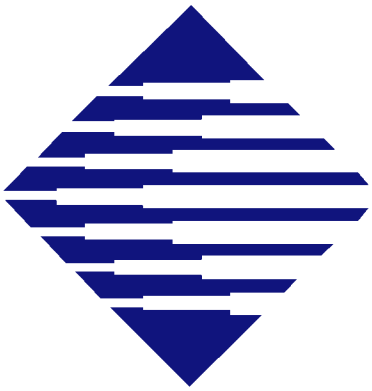
This permits the use of RJ48C jacks from the 24 ports of the CPC324. The BOB could also be used with the CPC308, if desired, utilizing the first eight ports only. The BOB is shown in Figure 6-9, “Front and Back View of 19" Break Out Box,” on page 113.

Figure 6-9: Front and Back View of 19" Break Out Box



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Chapter

7

References

Overview

The following topics are covered in this chapter:

- “Standards/Specifications,” on page 115
- “Additional Reference Documents,” on page 116

Standards/Specifications

- ECTF H.110 Hardware Compatibility Specification: CT Bus revision 1.0
- I^2C Bus Specification, Version 2.1
- IEEE P1386 2.4a March 21, 2001 Common Mezzanine Card Family
- IEEE P1386.1 Draft 2.4 Jan 12, 2001 PCI Mezzanine Cards, PMC
- IEEE Std. 802.3 2000 Edition CSMA/CD Access Method and Physical Layer Specification
- IPMI Intelligent Platform Management Specification, Version 1.5 {Intel, Hewlett-Packard, NEC, Dell}
- JEDEC JESD79C Double Data Rate (DDR) SDRAM Specification
- PCI Local Bus Specification Revision 2.2
- PICMG 2.0 R 3.0 CompactPCI Core Specification
- PICMG 2.1 R2.0 Hot Swap Specification
- PICMG 2.9 R1.0 CompactPCI System Management Specification
- PICMG 2.15 1.0 PCI Telecom Mezzanine/Carrier Card Specification
- PICMG 2.15 R1.0:ECN 2.15-1.0-001 10/100/1000 Ethernet MDI Links on PTMC
- PICMG 2.16 R1.0 CompactPCI Packet Switch Backplane
- VITA 32 -199x Processor PMC Standard Draft 0.41 Sept 8, 2000

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Additional Reference Documents

Broadcom Components

For more information about the following Broadcom components, refer to the Broadcom Web site:

- Broadcom BCM5388 Single-chip 8-port Gigabit Switch Datasheet
- Broadcom BCM5461s 10/100/1000 BASE-T Gigabit Ethernet Transceiver with SerDes
- Broadcom BCM5221 Single Port RMII 10/100 BASE-TX Transceiver

http://www.broadcom.com/

AMCC Processor

For more information about the AMCC PowerPC 440GX Embedded Processor, refer to the AMCC Web site:

- AMCC PowerPC 440GX Embedded Processor Datasheet and User's Manual

http://www.amcc.com/

Integrated Device Technology Transceiver

For more information about the Integrated Device Technology Octal T1/E1/J1 Long Haul / Short Haul Transceiver, refer to the IDT Web site:

- IDT Octal T1/E1/J1 Long Haul / Short Haul Transceiver IDT82P2288 Datasheet

http://www.idt.com/

Mindspeed Semiconductor Multichannel Synchronous Communications Controller

For more information about the Mindspeed Semiconductor Multichannel Synchronous Communications Controller, refer to the Mindspeed Web site:

- Mindspeed Semiconductor CN8478/74A/72A/71A Multichannel Synchronous Communications Controller (MUSYCC™) Datasheet

http://www.mindspeed.com/

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