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Models 1230A and 1231A VXIbus Pulsed / CW Microwave Frequency Counters

Operation Manual

1230A CCN 7818
1231A CCN 7913

Manual Assy Part Number: 5585104-02
Manual Text Part Number: 5580104-02
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Warranty

Phase Matrix, Inc. warrants this product to be free from defects in material and workmanship for one year from the date of delivery. Damage due to accident, abuse, or improper signal level is not covered by the warranty. Removal, defacement, or alteration of any serial or inspection label, marking, or seal may void the warranty. Phase Matrix, Inc. will repair or replace, at its option, any components of this product which prove to be defective during the warranty period, provided the entire unit is returned PREPAID to Phase Matrix, Inc or an authorized service facility. In-warranty units will be returned freight prepaid; out-of-warranty units will be returned freight COLLECT. No warranty other than the above is expressed or implied.

Certification

Phase Matrix, Inc. certifies this instrument to be in conformance with the specifications noted herein at time of shipment from the factory. Phase Matrix, Inc. further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology.

Manual Change Information

As Phase Matrix, Inc. continually improves and updates its products, changes to the material covered by the manual will occur. When a part or assembly in a Phase Matrix, Inc. instrument is changed to the extent that it is no longer interchangeable with the earlier part, the configuration control number (CCN) of the instrument, shown on the title page of the manual, will change, and a new edition of the manual will be published.

To maintain the technical accuracy of the manual, it may be necessary to provide new or additional information with the manual. In these cases, the manual is shipped with a Manual Update. Please be sure to incorporate the information as instructed in the Manual Update.

SAFETY

The Phase Matrix, Inc. Models 1230A & 1231A are designed and tested according to international safety requirements, but as with all electronic equipment, certain precautions must be observed. This manual contains information, cautions, and warnings that must be followed to prevent the possibility of personal injury and/or damage to the instrument.

SAFETY AND HAZARD SYMBOLS

WARNING
A WARNING denotes a hazard to personnel. It calls attention to a procedure or practice, which, if not correctly performed or adhered to, could result in personal injury.

CAUTION
A CAUTION denotes a hazard to the equipment. It calls attention to an operating procedure or practice, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.



This is a general warning that appears whenever care is necessary to prevent damage to the equipment.



Dangerous Voltage



Toxic Substance



Static-Sensitive Component



Fire Hazard

OVERALL SAFETY CONSIDERATIONS



WARNING

Before this instrument is switched on, it's protective earth terminals *must* be connected to the AC power cord's protective conductor. The main plug *must* only be inserted in a socket/outlet that has a protective earth contact. The protective action must not be negated by using an extension cord (power cable) or adapter that does not have a protective earth (grounding) conductor.



WARNING

Use only fuses of the type specified with the required current and voltage ratings. Never use repaired fuses or short-circuited fuse holders, as doing so causes shock and/or fire hazard.



WARNING

Whenever it is likely that electrical protection is impaired, the instrument *must* be made inoperative and be secured against any unintended operation.



WARNING

All protective earth terminals, extension cords, autotransformers, and other devices connected to this instrument *must* be connected to a socket/outlet that has a protective earth contact. Any interruption of the protection causes a potential shock hazard that can result in personal injury.



WARNING

The power supply is energized whenever AC power is connected to this instrument. Disconnect the AC power cord before removing the covers to prevent electrical shock. Internal adjustments or servicing that must be done with the AC power cord connected must be performed only by qualified personnel.



WARNING

Since the power supply filter capacitors may remain charged after the AC power cord is disconnected from the equipment, disconnecting the power cord does not ensure that there is no electrical shock hazard.



WARNING

Some of the components used in this instrument contain resins and other chemicals that give off toxic fumes if burned. Be sure to dispose of these items properly.



WARNING

Beryllia (beryllium oxide) is used in the construction of the YTF assembly. This material, if handled incorrectly, can pose a health hazard. *NEVER* disassemble the microwave counter assembly.



CAUTION

Static sensitive components are used in the YTF Assembly. These components can be damaged if handled incorrectly.



CAUTION

Before connecting power to the instrument, ensure that the correct fuse is installed and the voltage-selection switch on the instrument's rear panel is set properly. Refer to INSTALLATION Section 2, *Installation.*



CAUTION

Excessive signal levels can damage this instrument. To prevent damage, do not exceed the specified damage level. Refer to the instrument specifications in Section 1 of this manual.

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GENERAL INFORMATION

DESCRIPTION

The EIP Models 1230A and 1231A VXIbus Pulse/CW Microwave Frequency Counters are multifunction instruments that measure both CW and pulsed signals at microwave and millimeter-wave frequencies. They can automatically measure the frequency of repetitive pulsed signals with pulse widths as narrow as 50 ns. Both models can also automatically measure pulsed widths from 50 ns to 1 second and pulse periods from 250 ns to 1 second, to a 10 ns resolution. Additionally, through the INHIBIT IN connector, both counters can perform time gated measurements and profile modulated or chirped signals - CW or pulse - with measurement windows as narrow as 15 ns. No switching is required to measure CW or pulsed signals.

The frequency range of the EIP 1230A is 100 Hz to 26.5 GHz, and is extendible, by option, up to 170 GHz. The frequency range of the EIP 1231A is 100 Hz to 20 GHz. Band 0, 100 Hz to 250 MHz, is for CW measurements only.

Microprocessor control and the unique architecture used offer all the major counter functions, such as frequency offsets, frequency range limits, and averaging capabilities, plus a variety of special functions, including internal diagnostics, calibration and test aids, and sophisticated operational enhancements. Both counters conform to VXIbus Specification Revision 1.3/1.4 for message-based instruments. All primary and background functions are fully programmable.

OPERATING CONDITIONS

The EIP 1230A and 1231A counters are designed to operate at temperatures from 0 to 50 °C at a relative humidity not to exceed 95% (75% over 25 °C; 45% over 40 °C). These counters will perform to specifications at altitudes not exceeding 10,000 ft (3050 m) and will tolerate vibration not exceeding 2 g. They are fungus resistant. The module housing is not designed to provide protection from severe mechanical shock or liquids and is intended for normal VXIbus use in an environmentally clean area.

STORAGE

Store the instrument in an environment that is protected from moisture, dust, and other contaminants. Do not expose the instrument to temperatures below -55 °C or above 75 °C, nor to altitudes above 40,000 ft (12,000 m).

OPTIONS AND ACCESSORIES

OPTIONS	DESCRIPTION
002	Band 3 Frequency Extension. This module is available on Model 1230A only. Required for frequencies between 26.5 GHz and 170 GHz. Frequency Extension Cable Kit (890) and Remote Sensor also required.
006	SC-cut Ovenized High Stability Timebase (Aging Rate: 5 x 10^{-10}/day)
011	Extra Operation Manual (one supplied at no charge with each counter)
012	Service Manual

The following accessories are used with Option 002:

ACCESSORIES	DESCRIPTION
890	Frequency Extension Cable Kit
091	Remote Sensor 26.5 - 40 GHz (WR-28)
092	Remote Sensor 40 - 60 GHz (WR-19)
093	Remote Sensor 60 - 90 GHz (WR-12)
094	Remote Sensor 90 - 110 GHz (WR-10)
095	Remote Sensor 50 - 75 GHz (WR-15)
096	Remote Sensor 33 - 50 GHz (WR-22)
097	Remote Sensor 26.5 - 50 GHz (coaxial, K-connector ②)
098	Remote Sensor 110 - 170 GHz (WR-6)

③ K-Connector is a registered trademark of Wiltron Company.

SPECIFICATIONS

BAND 0 (CW ONLY)

Frequency Range	100 Hz to 250 MHz
Sensitivity	-15 dBm
Connector	BNC
Input Impedance	50 Ω, nominal
Maximum Input	+7 dBm
Damage Level	+20 dBm
FM Tolerance	Carrier must remain in band
Measurement Time ③	
100 Hz Resolution	200 ms
>100 Hz Resolution	$\frac{1}{RES} + 85$ ms
Accuracy ③	ACC = timebase error ±1 count

BAND 1

Frequency Range	250 MHz to 1 GHz
Sensitivity	-15 dBm
Connector	BNC
Input Impedance	50 Ω nominal
Maximum Input	+7 dBm
Damage Level	+24 dBm
Amplitude Discrimination	10 dB (>100 MHz separation)
FM Tolerance	Carrier must remain in band
Acquisition Time ③	$AC = \frac{1}{MinPRF} + 0.055$
Measurement Time ③	
Pulse	$MT = \frac{(4)(PP)}{(GW)(RES)} + 0.1$
CW	$MT = \frac{4}{(GW)(RES)} + 0.1$
Maximum Video Feedthrough ③ (signal frequency must be >250 MHz)	
Video Frequency >250 MHz	MV = SL – 20 dB
Video Frequency <250 MHz	$MV = SL - 20\text{ dB} + \left(40 \log x \frac{250\text{ MHz}}{fvideo}\right)$
Gate Error ③	$GE = \pm \frac{0.07}{GW}$

SPECIFICATIONS (Continued)

BAND 1 (Continued)

Distortion Error ③	$DE = \pm \frac{0.03}{PW - (3 \times 10^{-8})}$
Averaging Error ③	$AE = \pm 2\sqrt{\frac{RES}{(GW)(AVG)}}$
Accuracy ③	
Pulse	ACC = ±GE ±DE ±AE ± timebase error
CW	ACC = timebase error ±1 count (Based on 10 averages)

BAND 2

Frequency Range	EIP 1230A: 950 MHz to 26.5 GHz EIP 1231A: 950 MHz to 20.0 GHz
Sensitivity	950 MHz to 20 GHz: -20 dBm 20 to 26.5 GHz: -10 dBm
Input Impedance	50 Ω nominal
Connector	EIP 1230A: APC 3.5 EIP 1231A: Precision Type N
Maximum Input	+7 dBm
Damage Level	
Pulse	+53 dBm (<1 μs pulse width, 0.1% duty cycle)
CW	+45 dBm
Amplitude Discrimination	15 dB (>50 MHz separation)
Frequency Limits	Instrument will ignore signals outside of frequency limits.① Resolution: 10 MHz Accuracy: ±50 MHz
Center Frequency	Instrument will lock on signals ≤50 MHz from entered center frequency. Resolution: 10 MHz
FM Tolerance (Up to 10 MHz rate)	20 MHz (p-p)
Acquisition Time ③	
Pulse	
Frequency Limits (Default)	$AQ = 2(FH)\left[(4 \times 10^{-12}) + \frac{(4 \times 10^{-8})}{MinPRF}\right] + \frac{60}{MinPRF} + \frac{(2 \times 10^{-5})(PP)}{GW} + 0.35$
Center Frequency	$AQ = \frac{72}{MinPRF} + \frac{(2 \times 10^{-5})(PP)}{GW} + 0.2$

SPECIFICATIONS (Continued)

BAND 2 (Continued)

CW

Frequency Limits (Default) $AQ = 2(FH)\left[(4 \times 10^{-12}) + \frac{(4 \times 10^{-8})}{MinPRF}\right] + \frac{60}{MinPRF} + 0.25$

Center Frequency $AQ = \frac{72}{MinPRF} + 0.2$

Measurement Time ③

Pulse $MT = \frac{PP}{(GW)(RES)} + 0.2$

CW $MT = \frac{1}{RES} + 0.2$

Maximum Video Feedthrough 20 dB above signal level

Gate Error ③ $GE = \pm \frac{0.01}{GW}$

Distortion Error ③ $DE = \pm \frac{0.03}{PW - (3 \times 10^{-8})}$

Averaging Error ③ $AE = \pm \sqrt{\frac{RES}{(GW)(AVG)}}$

Accuracy ③

Pulse ACC = ±GE ±DE ±AE ± timebase error

CW ACC = timebase error ±1 count (Based on 10 averages)

BAND 3 (Option 002)

Frequency Range	26.5 to 170 GHz
Sensitivity	-20 dBm (-25 dBm typical) -15 dBm (110-170 GHz)
Connector	Depends on remote sensor used
Maximum Input	+5 dBm
Damage Level	+10 dBm
Amplitude Discrimination	20 dB
Center Frequency	Instrument assumes any signals present to be in the range ±2 GHz from the specified center frequency and calculates the harmonic number based on this assumption.
FM Tolerance	
Auto Mode	20 MHz p-p
Center Frequency	150 MHz p-p ②

SPECIFICATIONS (Continued)

BAND 3 (Option 002) (Continued)

Acquisition Time ③

Pulse

Auto Mode $AQ = \frac{70}{MinPRF} + \frac{(6 \times 10^{-3})(PP)}{GW} + 0.25$

Center Frequency $AQ = \frac{70}{MinPRF} + \frac{(8 \times 10^{-4})(PP)}{GW} + 0.25$

CW $AQ = \frac{70}{MinPRF} + 0.25$

Measurement Time ③

Pulse $MT = \frac{(4)(PP)}{(GW)(RES)} + 0.15$

CW $MT = \frac{4}{RES} + 0.15$

Maximum Video Feedthrough 15 mV p-p

Gate Error ③ $GE = \pm \frac{0.03}{GW}$

Distortion Error ③ $DE = \pm \frac{0.02}{PW - (3 \times 10^{-8})}$

Averaging Error ③ $AE = \pm 2\sqrt{\frac{RES}{(GW)(AVG)}}$

Accuracy ③

Pulse ACC = ±GE ±DE ±AE ± timebase error

CW ACC = timebase error ± n^2 counts

$n = \frac{\text{frequency}}{20\ \text{GHz}}$

REMOTE SENSORS

Model 1230A can have its maximum frequency extended, in bands, up to 170 GHz. This requires Option 002, a Frequency Extension Cabling Kit (EIP 890), and one or more of the following remote sensors:

Remote Sensor	Frequency Range (GHz)	Waveguide Size	Waveguide Flange
091	26.5 - 40	WR-28	UG-599/U
092	40 - 60	WR-19	UG-383/U

Remote Sensor	Frequency Range (GHz)	Waveguide Size	Waveguide Flange
094	90 - 110	WR-10	UG-387/U
095	50 - 75	WR-15	UG-385/U
096	33 - 50	WR-22	UG-383/U
097	26.5 - 50	K-Conn. ③	Coaxial
098	110 - 170	WR-6	UG-387/U

STANDARD TIMEBASE

Crystal Frequency	10 MHz (TCXO)
Stability	
Aging Rate	$<1 \times 10^{-7}$/month
Short Term	$<1 \times 10^{-9}$ RMS, 1 s average
Temperature	$<1 \times 10^{-6}$, 0 to 50 °C
Line Variation	$<1 \times 10^{-7}$, ±10% line voltage change
Warm-up Time	30 minutes
Output Frequency	10 MHz square wave, 1 V p-p minimum, into 50 Ω.
External Timebase	Requires 10 MHz square wave, 1 V p-p min., into 300 Ω.

OPTION 006 - OVENIZED HIGH STABILITY TIMEBASE (SC-CUT)

Frequency	10 MHz
Aging Rate	$<5 \times 10^{-10}$/day (after 24 hour warm-up), 1×10^{-7}/year
Short Term Stability (1 second average)	$<1 \times 10^{-10}$ rms
0 to °C Temperature Stability	$<3 \times 10^{-8}$
±10% line voltage change	$<2 \times 10^{-10}$
Warm-up time (at 25 °C)	Within 5×10^{-9} of final value 10 minutes after turn-on Within 1×10^{-9} of final value 30 minutes after turn-on
Phase Noise	-120 dBc/Hz at 10 Hz from carrier

PULSE PARAMETERS

Pulse Width	50 ns to CW
Minimum Profile Window	15 ns
Pulse Repetition Frequency	1 Hz to 4 MHz
Minimum Off Time	200 ns (will count CW)
Minimum On/Off Ratio	15 dB

SPECIFICATIONS (Continued)

PULSE WIDTH MEASUREMENT	
Range	50 ns to 1 s
Resolution	10 ns
Accuracy ③	±20 ns ± (timebase error)(PW)
Measurement Points	6 dB (±1.5 dB) below peak

PULSE PERIOD MEASUREMENT	
Range	250 ns to 1 s
Resolution	10 ns
Accuracy ③	±20 ns ± (timebase error)(PP)
Measurement Points	6 dB (±1.5 dB) below peak

GENERAL	
VXIbus Specifications	
Compatibility	Full compliance with VXIbus Specification Rev. 1.3/1.4
Device Type	Message-based instrument
Protocol	Word serial
Module Size	C-size, three slots wide
Weight	12.5 lbs (Add 1.2 lbs for Option 002 and 0.5 lbs for Option 006.)
Peak Module Current	+5 V: 1.9 A +12 V: 1.0 A - Add 0.6 A for Option 002. Add 0.7 A for Option 006. -12 V: 0.2 A - Add 0.1 A for Option 002. +24 V: 1.0 A -5.2 V: 2.0 A -2 V: 0.75 A
Dynamic Module Current	+5 V: 0.35 A +12 V: 0.08 A -12 V: 0.03 A +24 V: 0.10 A -5.2 V: 0.22 A -2 V: 0.08 A
Cooling	1 mm H_2O @ 4.7 liters/s
Resolution	1 kHz to 1 GHz (100 Hz in Band 0)
Gate Time	10 ms to 1 µs (dependent upon resolution)

NOTES

① Unwanted signals must be greater than 100 MHz from either limit.

② Measured frequency is a function of average frequency and geometric center frequency when FM is greater than 150 MHz and nonsymmetrical.

③ ACC = accuracy
AE = RMS averaging error (Hz)
AQ = acquisition time (s)
AVG = number of averages
DE = distortion error (Hz)
FH = difference between frequency limit high and frequency limit low (Hz)
GE = gate error (Hz)
GW = logical AND of inhibit input and pulse width minus 3 x 10^{-8} s
MinPRF = minimum PRF counter setting (Hz); for MinPRF >1.2 kHz, use MinPRF = 1200
MT = measurement time (s)
MV = maximum video
PP = pulse period (s)
PW = pulse width (s)
RES = counter resolution setting (Hz); for RES >1 MHz, use RES =10^6
SL = signal level

④ K-Conn is a registered trademark of Wiltron Company.

SIGNAL MEASUREMENTS

AUTOMATIC FREQUENCY MEASUREMENTS

The EIP 1230A and 1231A counters can automatically measure the frequency of both CW signals and repetitive pulse signals having pulse widths as narrow as 50 ns.

To measure the frequency of a CW signal, apply the signal to the input connector of the counter that corresponds to the frequency being measured and select the appropriate band using the BAND command. The counter will automatically find the signal and measure it.

The average frequency of repetitive pulse signals is measured in much the same way as CW signals. The only difference is that for pulse signals having pulse repetition frequencies (PRFs) of less than 2 kHz, the minimum PRF must be entered into the counter using the MINPRF function. If MINPRF is not set at or below the minimum PRF of the signal being measured, the counter will not lock onto the signal.

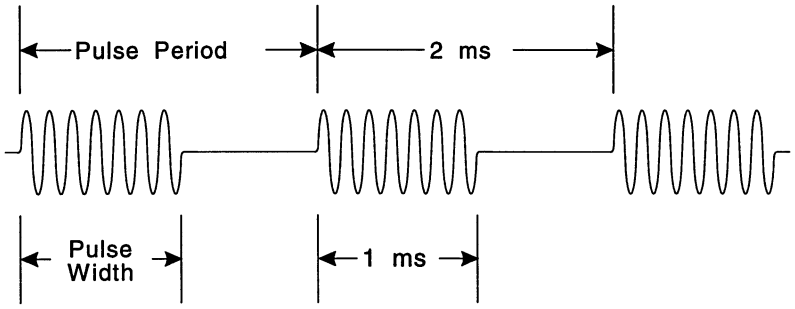


Figure 1-1. Pulsed Signals.

For example, consider the signal shown in Figure 1-1. The signal has a pulse width of 1 ms and a pulse period of 2 ms. PRF is the reciprocal of pulse period, so the PRF is 500 Hz. Since this is less than 2 kHz, it must be entered into the counter as a minimum PRF. To enter a minimum PRF of 500 Hz into the counter, issue the command MINPRF 500 HZ. At this point, if the signal were applied to the Band 2 input connector and Band 2 selected, the counter would automatically find the signal and measure its frequency.

The EIP 1230A and 1231A also automatically measure the pulse width and the pulse period of the incoming signal to a resolution of 10 ns. These measurements are enabled by issuing an OUTPUT PERIOD or OUTPUT WIDTH command.

MEASUREMENTS IN A MULTIPLE SIGNAL ENVIRONMENT

In many applications, multiple signals are present. In a multiple signal environment, the counter automatically finds and measures the highest amplitude signal, within the limits of the counter's amplitude discrimination specification. Amplitude discrimination is the ability of the counter to select, among multiple signals, the signal of highest amplitude. It specifies the minimum difference in signal amplitude required to guarantee that the counter will measure the larger signal.

In Band 2, the counter can also measure signals other than the largest signal present by setting frequency limits around the desired signal. Figure 1-2 shows an example of the Frequency Limits feature.

If the signals shown in Figure 1-2 are applied to Band 2, the counter automatically finds the signal at 6 GHz since it is the largest signal. However, if it is desired to measure the signal at 6.3 GHz, simply set the low frequency limit at 6.2 GHz and the high frequency limit to 6.4 GHz. This will prevent the counter from seeing the other higher amplitude signals.

The counter also provides a center frequency mode of operation in which it automatically sets frequency limits around the specified center frequency. Referring back to Figure 1-2, the signal at 6.3 GHz could also be measured by entering a center frequency of 6.3 GHz. In the center frequency mode, the counter locks onto signals within 50 MHz of the specified center frequency.

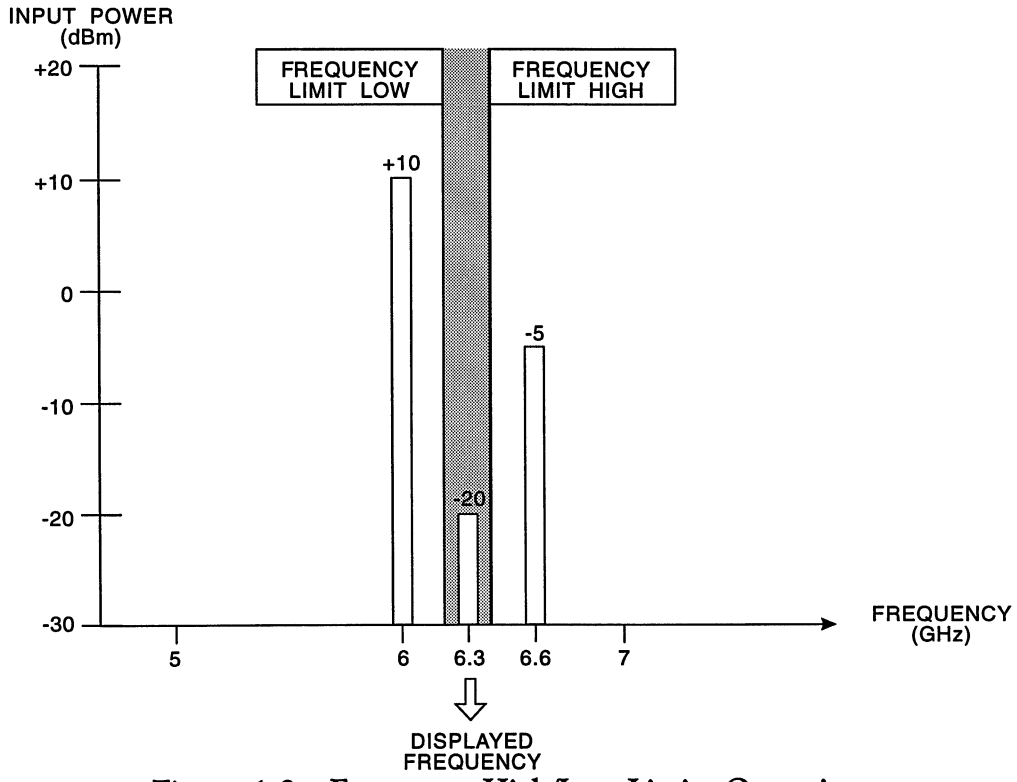


Figure 1-2. Frequency High/Low Limits Operation.

PULSE PROFILE MEASUREMENTS

Pulsed microwave frequency counters automatically measure the average frequency of a pulse. Often, however, the frequency change across the pulse is of interest as well. This frequency shift across the pulse may be intentional, as in the case of a chirp radar, or may be an undesirable concomitant. For example, a pulsed magnetron may exhibit substantial frequency shift near the leading and trailing edges of the pulse, or a pulsed Gunn diode oscillator may exhibit frequency shift during a pulse because of peak power thermal effects. Measurements of these characteristics are easily made using the pulse counter and a delaying pulse generator (see Figure 1-3).

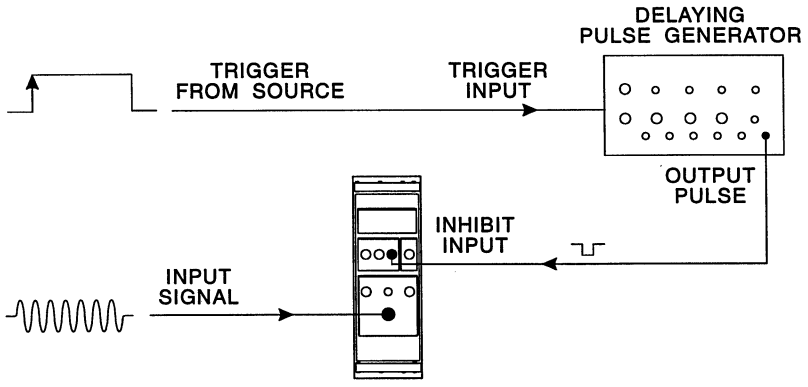


Figure 1-3. Pulse Profile Measurement Test Setup.

By triggering the pulse generator with the pulsed RF source, the generator's output pulse may be used to enable the counter at the appropriate point in time. As the pulse delay is varied, the measurement window can be "walked" through the RF pulse (see Figure 1-4) to construct a frequency versus time profile. Measurement windows as narrow as 15 ns can be used, although wider windows yield higher accuracy.

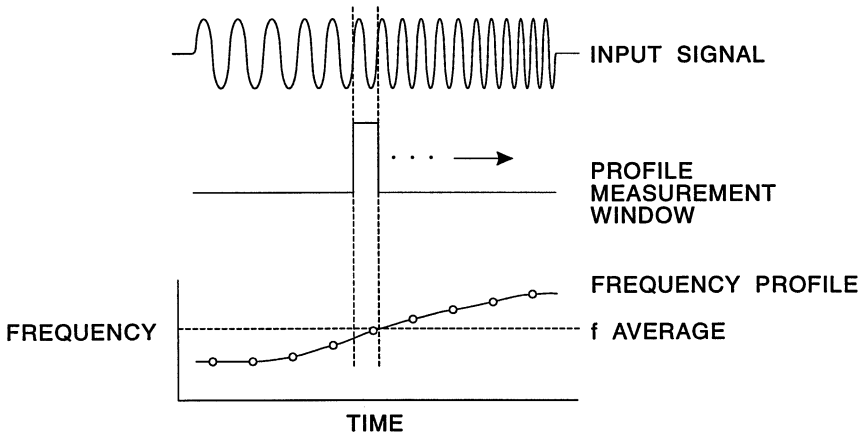


Figure 1-4. Pulse Profile Timing Sequence.

VCO SETTLING TIME MEASUREMENTS

Many complex signals are not pulses at all, but are simply CW signals whose frequencies vary with time. One example is the output of a voltage controlled oscillator (VCO). The output frequency of the VCO varies with the tuning voltage applied. When the tuning voltage is changed, the oscillator requires a finite amount of time to settle to its new frequency (see Figure 1-5). The amount of time it takes the VCO to settle within some predetermined limits is specified as VCO settling time. A typical VCO settling time specification requires that the frequency must be within ±10 MHz of the settled frequency within 1 μs after the voltage step is applied to the tuning input.

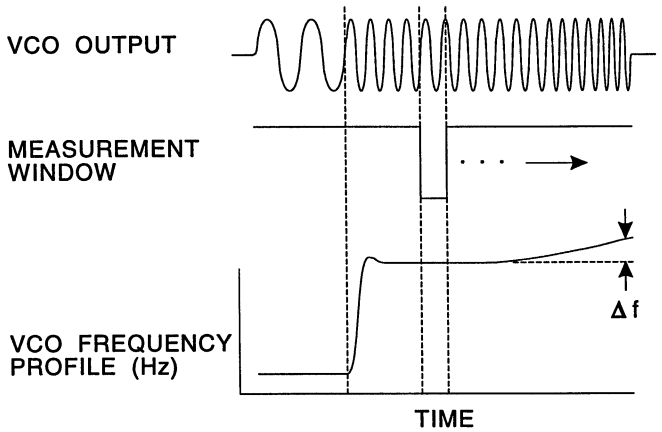


Figure 1-5. VCO Settling Time and Posttuning Drift Characteristics.

Once settled, the VCO exhibits a characteristic drift in frequency, known as posttuning drift (see Figure 1-5). This drift is typically a result of temperature effects on the semiconductor components within the oscillator, and varies as a function of the oscillator's initial and final frequencies. A square wave applied to the tuning voltage input will produce a response curve of frequency versus time, allowing measurement of settling time. A triggered or low PRF square wave may be used to measure posttuning drift. Since posttuning drift is a function of the initial and final frequencies, however, a single frequency-versus-time curve may not be adequate to completely characterize the VCO.

Both VCO settling time and posttuning drift measurements can easily be made using an EIP 1230A or 1231A counter and a delaying pulse generator as shown in Figure 1-6. The delay setting of the pulse generator corresponds to the point in time, after the VCO tuning voltage is stepped, at which the frequency measurement is made. By stepping this delay and measuring the frequency at each point, the VCO tuning characteristic may be obtained.

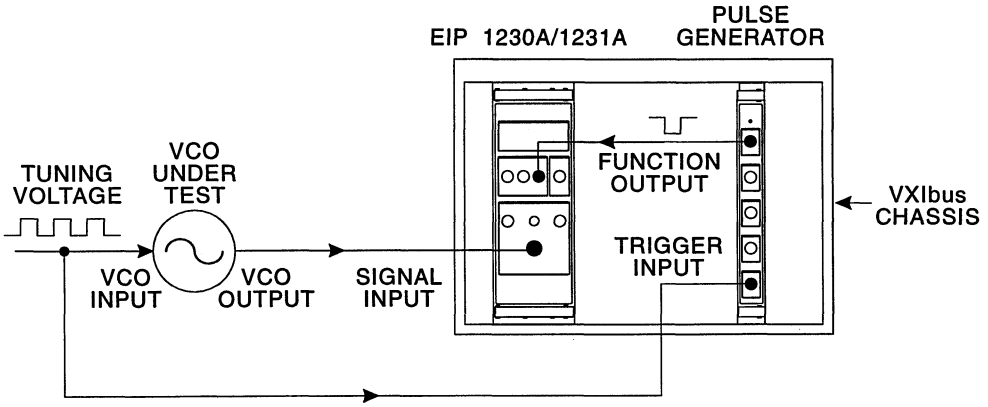


Figure 1-6. VCO Settling Time and Posttuning Drift Test Setup.

FREQUENCY AGILE SIGNAL ANALYSIS

Another application pertains to the measurement of a repetitive sequence of pulses differing in frequency, as in a frequency agile communications system. It is desired to directly measure the frequency of each pulse in the sequence. One of two methods may be used to measure multiple frequency pulse signals: time windowing, using a delaying pulse generator, or frequency windowing, using the YIG preselector.

Time Windowing

In the time windowing technique, the measurement enable input is used to discriminate between pulses. The enabling pulse can be slightly wider than the pulse to be measured. The EIP 1230A and 1231A counters automatically reduce the measurement window by approximately 15 ns on each edge to reduce distortion effects from the leading and trailing edges of pulses. By shifting the delay time of the enable pulse, each pulse in the sequence may be separately measured (see Figure 1-7). The pulses of interest must be greater than 50 ns in width for the counter to measure properly. In addition, the maximum time between the leading edges of the selected pulses must be known. The reciprocal of this time (PRF) is used to set the minimum PRF (MINPRF) setting of the counter (this prevents the counter from timing out between measurement windows).

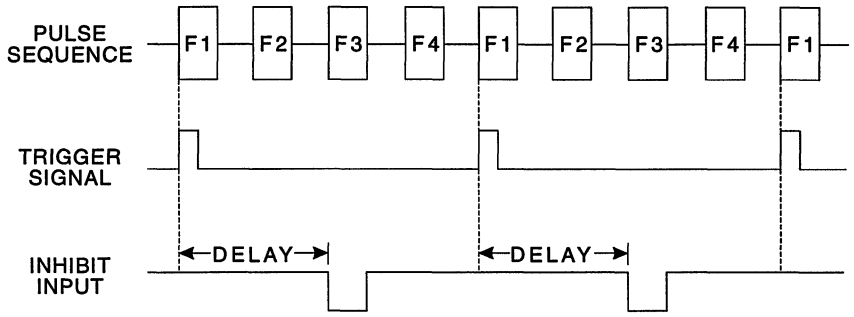


Figure 1-7. Frequency Agile Signal Measurement Using Time Windowing.

Frequency Windowing

If the approximate frequencies of the pulses are known, frequency windowing may be used. This method uses the YIG preselector in the counter to reject all frequencies not of interest. The frequency limits of the counter are adjusted so that the counter measures only one of the RF pulses in the sequence (see Figure 1-8). By moving the frequency window, each different frequency in the pattern may be measured. This method does not require a pulse generator, but can only be used in the microwave frequency range (Band 2). In addition to the pulse width and minimum PRF requirements noted above, this technique requires that the minimum frequency separation between signals be approximately 100 MHz. This separation is required to allow the YIG to selectively pass only one pulse.

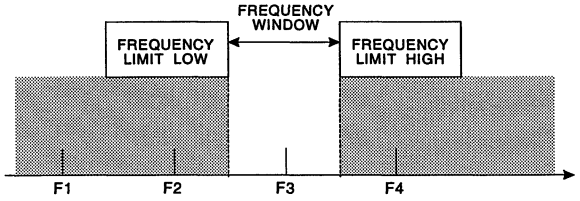


Figure 1-8. Frequency Agile Signal Measurement Using Frequency Windowing.

TIMING CONSIDERATIONS

For most frequency profiling measurements, the details of the EIP 1230A and 1231A internal timing are of little concern. However, when performing frequency profiling measurements where small frequency sampling or nanosecond accuracy is required, some details of the counter's internal operation become important, especially those concerning the counter's measurement window and internal timing delays.

Measurement Window Width

The measurement window is the period during which the gate is actually open to allow a signal to be counted. This gate width will typically be 30 ns narrower than the pulse applied to the INHIBIT IN connector, although the width will always be an integral number of clock periods (12.5 ns). Thus, to measure a 25 ns sample, a 55 ns enable pulse should be applied to the INHIBIT IN connector. For applications where the width of the measurement window must be known to an accuracy better than 20 ns, the gate output should be observed directly on a high speed oscilloscope. The desired gate width may then be set by varying the inhibit input pulse width. For accurate pulse representation, the oscilloscope input should be terminated in a 50 Ω load.

Internal Timing Delays

When it is necessary to measure signal frequency at a precise point in time, internal delays of the measuring instrument can be significant. In the EIP 1230A and 1231A counters, the total delay between the time a signal is applied to an input connector and the time it is available to be counted is nominally 60 ns. The signal threshold output typically occurs 20 ns after the signal is applied and 40 ns prior to measurement. The gate signal occurs at the measurement time with virtually no delay. In other words, when absolute time positioning of a signal is required, it is necessary to consider that the gate signal (representing the measurement period) is actually making a measurement of the signal that appeared at the input connector 60 ns earlier. Figure 1-9 shows the relative timing of these signals for a pulsed input signal. Timing is not a function of input signal characteristics.

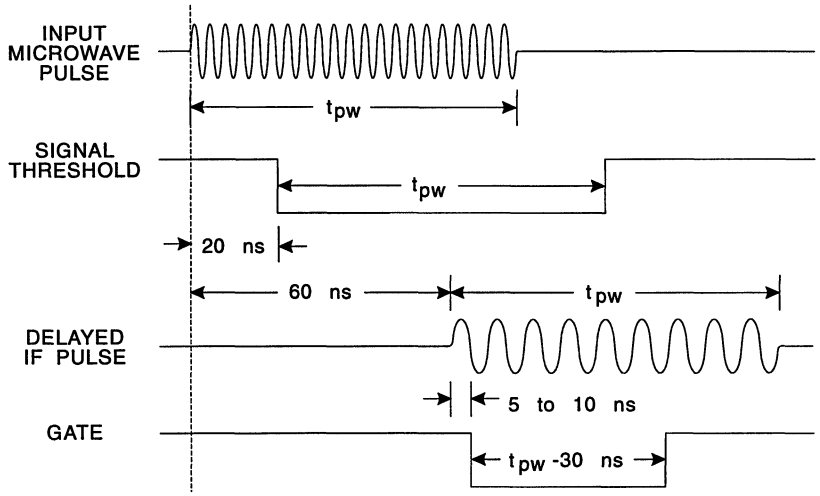


Figure 1-9. Internal Timing Delays.

MEASUREMENT ACCURACY

When making any type of measurement, some degree of measurement error exists. When measuring CW signals, these errors are limited to a combination of timebase error, gate phasing error (±1 count error), and gate width error. In making frequency measurements on pulsed RF signals, the preceding errors along with an additional distortion error, caused by distortion of the pulsed RF signal, affect measurement accuracy. To minimize these errors and to properly interpret the results of the measurements, it is necessary to know their magnitude.

CW Measurement Accuracy

When measuring CW signals the measurement accuracy is specified as:

Total error = timebase error ±1 count
(Based on measurement averaging)

Timebase error causes an error in the measured frequency proportional to the error in the timebase oscillator. For example, if the 10 MHz oscillator is off frequency by 3 Hz, the corresponding measurement error on a 1 GHz signal would be 300 Hz. For an 18 GHz signal, the same 3 Hz timebase error would cause a measurement error of 5.4 kHz. The maximum timebase error is the sum of the various error components, such as aging rate and temperature stability.

The second type of error, ±1 count, results from the lack of phase coherence between the gate and the signal. Simply stated, if an event occurs every 400 ms (F = 2.5 Hz), a counter could measure either two or three events in a one second interval. The above note "Based on measurement averaging" is included because of a random instrumentation error in the counter. This error can be virtually eliminated by averaging measurements. Following are sample calculations for determining the measurement error of the counter, based solely on the timebase aging rate.

Given: Aging rate: 1×10^{-7}/month
Calibration interval: 6 months
Frequency: 20 GHz

Calculation: Error = ± (aging rate x cal. interval x frequency)
= ± [(1×10^{-7})/mo. x 6 mo. x 20 GHz]
= ± [(6×10^{-7}) x 20 GHz]
= ± 12 kHz

Counter measurement, after a six-month calibration interval, could have an error of ±12 kHz in measuring a 20 GHz signal.

Given: Aging rate: 1×10^{-7}/month
Calibration interval: 12 months
Frequency: 20 GHz

Calculation: Error = ± (aging rate x cal. interval x frequency)
= ± [(1×10^{-7})/mo. x 12 mo. x 20 GHz]
= ± [(12×10^{-7}) x 20 GHz]
= ± 24 kHz

Counter measurement after the recommended 12-month calibration interval could have an error of ±24 kHz in measuring a 20 GHz signal just due to timebase aging.

These examples are to illustrate error due to the timebase aging rate only. Actual calculations of measurement error must include the other sources of error discussed in the following text.

Pulse Measurement Accuracy

Each of the sources of CW measurement error contribute to the overall error in pulsed frequency measurements, along with gate error and distortion error. For narrow pulses, averaging error and gate error can become the dominant sources of error.

ERROR SOURCES

The following list describes the sources of potential measurement error when using the EIP 1230A and 1231A VXIbus Pulse/CW Microwave Frequency Counters:

- Timebase Error. A frequency error in the timebase reference oscillator results in a proportional frequency measurement error. Two main sources of timebase error are aging rate and temperature stability. Aging rates of less than 1×10^{-7} parts per month and temperature stability of 1×10^{-6} over the range of 0 to 50 °C are standard in the EIP 1230A and 1231A.

- Averaging Error. Averaging error is caused by the lack of phase coherence between the gate and the incoming signal and results in an uncertainty of ±1 count, in the least significant digit, with each gate opening. If the resolution on the counter is set to 10 kHz, the potential error on each gate is ±10 kHz. On signals having pulse widths of less than the required gate time (determined by the resolution), the EIP 1230A/1231A will generate more than one gate per measurement cycle. If the counter generates n gates, then an uncertainty of ±n counts is possible, though very unlikely. The resultant averaged measurement follows the rules of statistics in that on successive gates the ±1 count error will vary randomly to a certain degree. In fact, most of the readings (63%) will fall between ± the square root of n, where n is the number of gates required to accumulate the required gate time. This is called the RMS averaging error. In the following formulas, $n = \frac{RES}{GW}$. Note that the total gate time is typically 30 ns narrower than the input pulse. The RMS averaging error, in Hz, can be calculated by using the following formulas:

  Bands 1 and 3: Averaging Error (RMS) $= \pm 2\sqrt{\frac{RES}{GW}}$

  Band 2 : Averaging Error (RMS) $= \pm\sqrt{\frac{RES}{GW}}$

  Where: RES is the specified instrument resolution in Hz, up to 1 MHz. Above 1 MHz, RES is always 1 MHz.
  GW is the logical AND of the pulse width and the inhibit signal minus 30 ns. Figure 1-10 graphically describes the logical AND function.

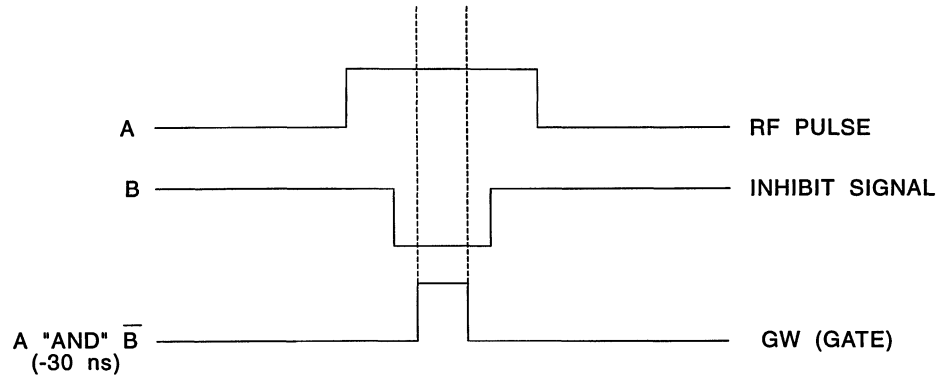


Figure 1-10. Logical "AND" Function.

- Gate Error. When narrow pulses are counted, the gate is opened and closed many times to accumulate enough gate time to provide the required resolution. Each gate opening and closing produces a small but finite error. The total error is proportional to the number of times the gate is cycled during a measurement, and is inversely proportional to the gate width. This error is also related to both temperature and input frequency. In the EIP 1230A and 1231A counters, the worst case gate error, including all variables, is specified as:

  Band 1: Gate Error $= \pm\frac{0.07}{GW}$

Band 2: Gate Error $= \pm \frac{0.01}{GW}$

Band 3: Gate Error $= \pm \frac{0.03}{GW}$

Where: GW in seconds is the logical AND of the pulse width and the inhibit signal minus 30 ns.

Unlike averaging error, which is random, gate error is systematic, and is not reduced by averaging.

- Distortion Error. During the first and last few nanoseconds of a pulse, phase distortion caused by impedance mismatches or video effects can occur, which results in shifts in time of the zero crossings. On wide pulses, distortion error is insignificant; however, on narrow pulses it may become the dominant source of error. To reduce the effect of distortion error on count accuracy, the EIP 1230A and 1231A counters automatically adjust the gate to start 15 ns after the pulse begins, and to end 15 ns before the pulse ends. The specified maximum distortion error for all three pulse bands can be calculated from the following formula:

  Maximum Distortion Error $= \pm \frac{0.03}{PW - 30\ ns}$

  Where: PW = Pulse Width (minimum pulse width is 50 ns)

TECHNIQUES FOR IMPROVING ACCURACY

In most cases, the specified counter accuracy will be more than sufficient to meet measurement requirements. If greater accuracy is required, all four sources of error can be minimized by a combination of calibration, long-term averaging, adding correction factors, and signal conditioning.

TIMEBASE CALIBRATION

A frequency error in the internal timebase oscillator results in a proportional error in the frequency reading for either CW or pulsed signals. The aging rate of the standard temperature-compensated crystal oscillator (TCXO) timebase used in the EIP 1230A and 1231A counters is specified to be less than 1×10^{-7} parts per month. This means that if the oscillator was set precisely on frequency at the beginning of the month, it could be nearly 1 Hz off at the end of the month. On a frequency measurement of 18 GHz, a 1 Hz error in the 10 MHz timebase would cause a measurement error of 1.8 kHz. Other errors can result from changes in ambient temperature. Timebase measurement errors can be reduced by calibrating the timebase at its ambient temperature using a standard of known accuracy. The timebase frequency is corrected by turning the adjustment screw on the TCXO or optional oven oscillator. Another method of improving timebase accuracy is to use an external 10 MHz timebase with a known degree of accuracy, such as a 10 MHz frequency standard.

REDUCING AVERAGING ERROR

Averaging error is reduced to ±1 count whenever the GW is greater than $\frac{1}{RES}$. Since the averaging error is random in nature, it can also be reduced by increasing the number of individual gates. This is accomplished by increasing the resolution of the counter and/or averaging a number of individual measurements. The EIP 1230A and 1231A counters allow 1 kHz maximum resolution and can automatically average up to 99 individual measurements internally. An external controller

can average a larger number of individual measurements, virtually eliminating averaging error. The following formulas can be used to determine the averaging error (RMS) when averaging a number of individual measurements.

Bands 1 and 3: Averaging Error (RMS) $= \pm 2\sqrt{\frac{RES}{(GW)(AVG)}}$

Band 2 : Averaging Error (RMS) $= \pm\sqrt{\frac{RES}{(GW)(AVG)}}$

Where: RES is the specified instrument resolution in Hz, up to 1 MHz. Above 1 MHz, RES is always 1 MHz.
GW is the logical AND of the pulse width and the inhibit signal minus 30 ns.
AVG is the number of individual measurements to be averaged.

REDUCING GATE ERROR

Gate error at any given frequency and pulse width can be virtually eliminated by comparing a CW frequency measurement to a simulated pulsed frequency measurement and computing a gate error correction factor. This correction factor can be added to, or subtracted from, the indicated pulse measurement to obtain the corrected frequency. The CW signal should be the same frequency (within 25 MHz) as that of the actual pulsed signal to be measured. To simulate a pulsed signal, apply an enable signal (of the same width as the pulse to be measured) to the INHIBIT IN connector. A single measurement will contain both averaging error and gate error. Averaging measurements will reduce averaging error by the square root of the number of measurements averaged. If 100 measurements are averaged, the averaging error will be reduced by a factor of 10. Gate error and any residual averaging error comprise the difference between the pulsed and non-pulsed measurement of the same CW signal.

To determine gate error for a 2 ms wide pulse at 2 GHz:

1. Apply a CW signal to the counter at 2 GHz ±25 MHz and record the frequency (F1).
2. Apply an ECL signal with a pulse width of 2 µs to the INHIBIT IN connector. Set the counter to average 99 readings. Record the frequency (F2).
3. Gate Error = F2 - F1.

NOTE

This procedure avoids errors associated with pulsed signal distortion and any possible pulling of the signal source. It should be noted that by using SPECIAL 92, gate error can also be automatically calibrated out of the system for a given pulse width and frequency. However, the calibrating procedure may result in additional errors for other pulse widths or frequencies.

REDUCING DISTORTION ERROR

Since distortion error is most significant on the edges of the pulse, it may be reduced by using the counter inhibit feature to measure only in the middle of the pulse; however, measuring only the middle of the pulse narrows the gate and, hence, increases gate error. For pulse widths less than 70 to 80 ns, this may add more error than it removes. Section 8 describes a method for determining the magnitude of this error, which can be used to determine the improvement in accuracy achieved by using the inhibit function.

CALCULATING MEASUREMENT ACCURACY

The following is a sample calculation for determining the maximum specified measurement error in a typical pulsed frequency measurement.

Given: Frequency: 18 GHz
Pulse Width: 530 ns
Resolution: 100 kHz

SUM INDIVIDUAL ERRORS

TIMEBASE ERROR (TBE) - ±10.8 kHz

(Based on 6 Hz error from 10 MHz Timebase)

$$TBE = \left(\frac{6\ Hz}{10\ MHz}\right) x\ 18\ GHz = 10.8\ kHz$$

NOTE

The direction of the timebase error is not specified, so it is not known whether the timebase error caused the indicated reading to be higher or lower. If the actual frequency of the timebase was 6 Hz high then its period would be reduced and the counter would indicate a lower frequency.

RMS AVERAGING ERROR - ±45 kHz

$$AE\ (RMS) = \pm\sqrt{\frac{RES}{(GW)(AVG)}}$$

Where: RES = Specified counter resolution
GW = (Pulse width "AND" Inhibit signal) - 30 ns
AVG = Number of measurements averaged

$$AE\ (RMS) = \pm\sqrt{\frac{100\ kHz}{(500\ ns)(99)}} = \pm 45\ kHz$$

NOTE

In order to reduce the averaging error for this example, the measurement averaging feature of the counter was used. If it had not been used, the averaging error would have been ±450 kHz.

GATE ERROR (Worst Case) - ±20 kHz

$$GE = \pm\frac{0.01}{GW}$$

Where: GW = (Pulse width "AND" Inhibit signal) - 30 ns

$$GE = \pm\frac{0.01}{500\text{ ns}} = \pm 20\text{ kHz}$$

DISTORTION ERROR (Worst Case) - ±60 kHz

$$DE = \pm\frac{0.03}{PW - 30\text{ ns}}$$

Where: PW = Pulse Width

$$DE = \pm\frac{0.03}{530\text{ ns} - 30\text{ ns}} = \pm 60\text{ kHz}$$

TOTAL ERROR = SUM OF INDIVIDUAL ERRORS - ±136 kHz

NOTE

The total measurement error listed above is the worst case measurement uncertainty. The errors would not normally all be in the same direction; equal errors in opposite directions would cancel and therefore the overall error would be reduced.

MEASUREMENT ACCURACY WORKSHEET

The worksheet on the following page can be used to determine the maximum specified measurement error for a particular application. To determine the specified maximum error, select the desired operating parameters and use the formulas given to determine the magnitude of each type of error.

VARIABLES: Frequency (F): _____
Pulse Width (PW): _____
Counter Resolution (RES): _____

SUM INDIVIDUAL ERRORS

TIMEBASE ERROR

This error can be determined by accurately measuring the frequency at the front panel 10 MHz IN/OUT connector. The frequency measured (F mea) is then plugged into the following formula to determine measurement error.

$$TBE = \left(\frac{10\ MHz - F\ mea}{10\ MHz}\right) x\ F$$ _____

Where: F mea = Measured Timebase Frequency
F = Input Frequency

RMS AVERAGING ERROR

$$\text{BAND 1 and 3: AE (RMS)} = \pm 2\sqrt{\frac{RES}{(GW)(AVG)}}$$ _____

$$\text{BAND 2: AE (RMS)} = \pm\sqrt{\frac{RES}{(GW)(AVG)}}$$ _____

Where: RES = Specified counter resolution in Hz up to 1 MHz. Above 1 MHz resolution, the counter's internal resolution remains at 1 MHz.
GW = (Pulse width AND" Inhibit signal) - 30 ns
AVG = Number of measurements averaged

NOTE

If GW is $> \frac{1}{RES}$ *then AE* $= \pm 1$ count.

GATE ERROR (Worst Case)

$$\text{BAND 1: GE} = \pm\frac{0.07}{GW}$$ _____

$$\text{BAND 2: GE} = \pm\frac{0.01}{GW}$$ _____

$$\text{BAND 3: GE} = \pm\frac{0.03}{GW}$$ _____

Where: GW = (Pulse width "AND" Inhibit signal) - 30 ns

DISTORTION ERROR (Worst Case)

$$DE = \pm\frac{0.03}{PW - 30\ ns}$$ _____

Where: PW = Pulse Width

TOTAL ERROR = SUM OF INDIVIDUAL ERRORS _____

DECLARATION OF CONFORMITY

Application Of Council Directive 89/336/EEC

Standards to which Conformity is Declared:

EMC: EN50011
EN50082-1

Standards to which Compliance is Declared:

Safety: IEC 1010-1 (1990)

Manufacturer's Name:	EIP Microwave, Inc.
Manufacturer's Address:	1745 McCandless Drive Milpitas, California 95035
Type of Equipment:	Frequency Counter
Model Name(s):	1230A/1231A
Tested By:	Rockford Engineering Services, Inc. 9959 Calaveras Road Sunol, CA 94586 USA
Project Engineer:	Mr. Bruce Gordon and Leo Hernandez
Reviewer:	Mr. Michael Gbadebo, P.E.

I, the undersigned, hereby declare that the equipment specified above conforms to Directives and Standards listed.

For: **EIP Microwave**

Name: Pete Pragastis
Title: Manager of Engineering

Signature: _____

Date: 4-29-96

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2

INSTALLATION

UNPACKING

The EIP 1230A and 1231A VXIbus Pulse/CW Microwave Frequency Counters arrive ready for operation. Carefully inspect the shipping carton for any sign of visible or concealed damage. If the carton or instrument is damaged, immediately notify shipper's agent.

Remove the packing carton and supports, being careful not to scar or damage the instrument. Make a complete visual inspection of the counter, checking for any damage or missing components. Report any problems to EIP immediately.

SETTING THE LOGICAL ADDRESS

Before installing the counter in the VXIbus mainframe, verify that the logical address is between 1 and 254 (decimal). The factory default setting for the logical address of the counter is 12 hexadecimal (18 decimal). The logical address of the counter can be modified by resetting the two rotary-type **hexadecimal** switches located at the top rear of the module (see Figure 2-1). The two switches represent the MSB and LSB values of the counter's logical address (the switch on the left, facing the counter, is the MSB switch). The logical address is set by dialing each switch to the hexadecimal value desired. For example, to set a logical address of 17 hexadecimal (23 decimal), use a small flathead screwdriver (or similar tool) to set the MSB switch to 1 and the LSB switch to 7. The logical address desired must be a value between decimal 1 and 254. Logical address 0 is reserved for Slot 0 devices. Logical address 255 is reserved for dynamically configured devices. The EIP 1230A and 1231A do not support dynamic configuration.

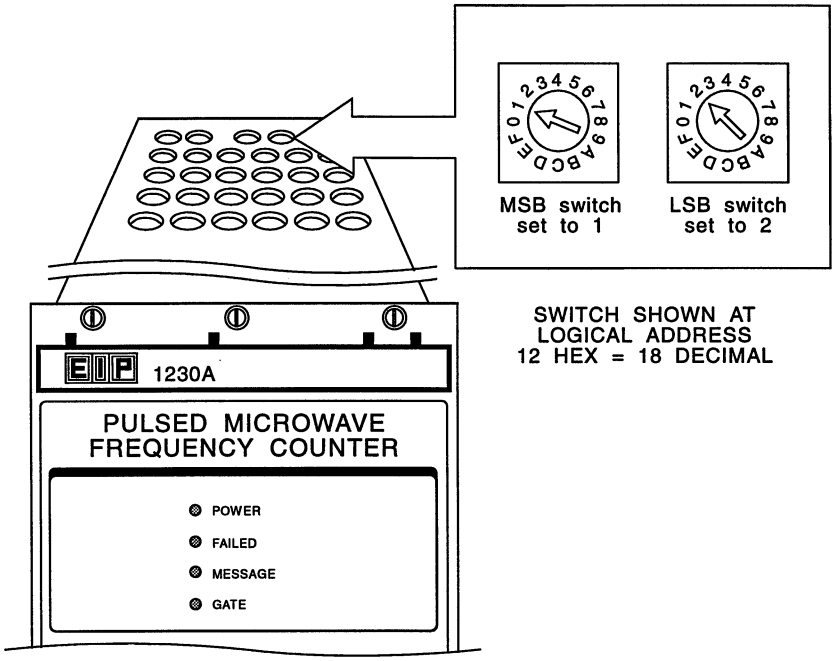


Figure 2-1. Logical Address Switch Locations.

POWER AND COOLING

When configuring your VXIbus system, make sure that the VXI chassis has sufficient power and cooling capacity to meet the requirements of the various modules in the system. The peak currant and cooling requirements of the 1230A/1231A are shown in the Specification section of this manual.

INSTALLATION

The 1230A/1231A is a VXIbus module designed to be installed in a VXIbus mainframe. Prior to installing the counter in a VXIbus mainframe, verify that all VXI defined voltages are present and within limits, and make sure the mainframe is capable of supplying the required current (see Specifications in Section 1).

CAUTION

Verify proper alignment before applying pressure and seating instrument. Failure to do so can cause damage to rear connectors.

CAUTION

Prior to installing the 1230A/1231A in a VXIbus mainframe, verify that all the VXI defined voltages are present and that the mainframe is capable of supplying the required current.



CAUTION

Do not plug counter into VXIbus mainframe with power applied.

The 1230A/1231A is a 3-slot, C-size module that can be installed into any slot of a VXIbus mainframe except slot 0. Slot 0 is reserved to the resource manager. To install the counter into the VXIbus mainframe, first turn mainframe power off. Next, place the counter card edges into the front mainframe guides (top and bottom). Gently slide the counter towards the rear of the mainframe until the connectors just mate with the backplane. Firmly seat module with backplane connectors making sure the front panel is flush with the front of the card cage. Tighten down the retaining screws to ensure the module remains fully seated.



CAUTION

Do not use retaining screws to seat module.

INCOMING OPERATIONAL CHECK

A VXIbus mainframe along with a slot 0 resource manager and an instrument controller are required to verify that the counter is operational. With the counter installed in a VXIbus mainframe, two tests are automatically performed to verify proper operation:

1. Whenever a VXIbus mainframe is energized, the resource manager queries each device checking for proper operation.
2. The counter performs an internal power-on self-test and lights the failed LED if any problems are detected. The instrument can also be commanded to perform a self-test by issuing the command SPECIAL 01 and reading the frequency. The value returned should be 100 MHz ±1 kHz.

IN CASE OF PROBLEMS

In the event that a problem does occur, there are a few things to check prior to returning the instrument for repair.

1. If the unit has never worked in the particular system, the problem may be due to the system and not an instrument fault. In this case, call EIP at the phone number listed on the cover page of the manual and ask for Customer Support.
2. Verify logical address setting on the instrument.
3. Verify that all the VXI specified voltages are present.

SERVICE INFORMATION

PERIODIC MAINTENANCE

No periodic preventive maintenance is required. However, to maintain accuracy, it is recommended that the 1230A/1231A be recalibrated every 12 months or whenever a problem is suspected. The specific calibration interval depends upon the accuracy required.

COUNTER IDENTIFICATION

This counter is identified by three sets of numbers: the model number (EIP 1230A or 1231A), serial number, and a configuration control number (CCN). These numbers are located on a label affixed to the top of the module and must be included in any correspondence regarding your counter.

FACTORY SERVICE

If the counter is being returned to EIP for service or repair, be sure to include the following information with the shipment.

- Name and address of owner.
- Model, complete serial number, and CCN of the counter.
- A complete description of the problem. The main thing is to provide enough information so that the problem can be verified, i.e., Under what conditions did the problem occur? Did the unit work and then fail? What other equipment was connected to the counter?
- Name and telephone number of someone familiar with the problem who may be contacted by EIP if any further information is required.
- Shipping address to which the counter is to be returned. Include any special shipping instructions. Pack the counter for shipping as detailed in Shipping Instructions.

SHIPPING INSTRUCTIONS

Place the counter in an antistatic bag or enclosure, wrap in heavy plastic or kraft paper, and repack in the original container, if available. If the original container cannot be used, pack in a heavy (275 pound test) double-walled carton with approximately four inches of packing material between the counter and the inner carton. Seal carton with strong filament tape or strapping. Mark the carton to indicate that it contains a fragile electronic instrument. Ship to the EIP address on the title page of the manual.

3

OPERATION

INTRODUCTION

This section provides the information needed to operate the EIP 1230A and 1231A counters to their full potential. Front panel indicators and connectors are described, instrument default settings are listed, and VXIbus mnemonics that control the counters are defined. Signal measurement procedures are explained and sample programs for user applications are included. Special functions relative to counter operation, calibration, and use enhancement are listed and described, with examples of user applications. VXIbus functions are described in terms of device-dependent messages and output messages.

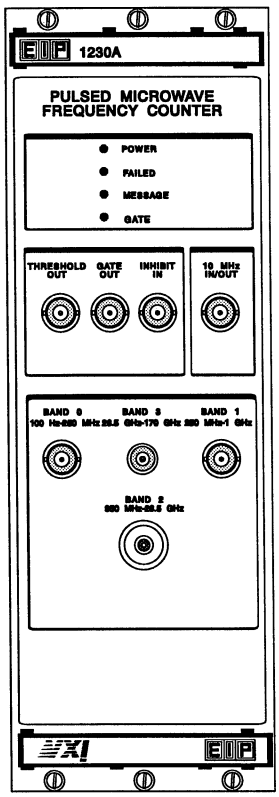


Figure 3-1. Front Panel (Model 1230A Shown).

FRONT PANEL INDICATORS

- POWER LED. When illuminated, the POWER LED indicates that power is being supplied to the counter. The counter senses the voltage on all lines that are used and checks for sufficient voltage. If the required voltages are not present, the indicator will not light.
- FAILED LED. When illuminated, the FAILED LED indicates that the counter has failed, or is in the process of executing, its self-test. Failures are typically the result of internal component failure or inadequate power supply current. The FAILED LED follows the condition of the VXIbus SYSFAIL line. If the unit has failed, the LED will remain lit even if SYSFAIL is inhibited by the commander.
- MESSAGE LED. When illuminated, the MESSAGE LED indicates that the counter is either sending or receiving messages or data over the VXIbus. The MESSAGE LED is also illuminated when a commander accesses the counter's VXIbus registers.
- GATE LED. When illuminated, the GATE LED indicates that the counter has acquired a signal and is in the process of measuring it. The GATE LED is illuminated when the counter signal gate is open.

FRONT PANEL CONNECTORS

SIGNAL INPUT CONNECTORS

Table 3-1. Signal Input Connector Characteristics.

	Band 0	Band 1	Band 2	Band 3 (Option 002)
Nominal Input Impedance (Ω)	50	50	50	50
Frequency Range	100 Hz-250 MHz (CW only)	250 MHz-1 GHz	950 MHz-20 GHz (EIP 1231A) 950MHz-26.5 GHz (EIP 1230A)	26.5-170 GHz (EIP 1230A only)
Input Level (max. dBm)	+7	+7	+7	+5
Damage Level (min. dBm)	+20	+24	+53 Pulse +45 CW	+10
Connector Type	BNC (female)	BNC (female)	APC 3.5 (female) (EIP 1230A) Precision N (female) (EIP 1231A)	Selectro Quick Connect (EIP 1230A only)

AUXILIARY CONNECTORS

- THRESHOLD OUT is the digitized pulse envelope. It is true when the counter has a converter lock and a signal is present. The output is 0 V when false, and -0.75 V into 50 Ω when true.

- GATE OUT represents the gate input to the count chain circuit. The gate output follows the actual gate, not the inhibit input. The output is 0 V when false, and -0.75 V into 50 Ω when true.
- INHIBIT IN causes the counter to perform as if the input signal were turned off. The counter ignores any signal present while inhibit is true during all phases of operation. The inhibit input impedance is 50 Ω into -2 V so that the counter can be driven by either an emitter-coupled logic (ECL) signal or a 0 to -1 V, 50 Ω source. The inhibit input can also be accepted from either of two VXIbus ECLTRG lines.

NOTE

Input inhibit is designed to be compatible with either a 50 Ω impedance pulse generator or ECL device. An internal termination of 50 Ω returned to -2 V makes this dual compatibility possible. An ECL high signal (-0.8 to -1.1 V) will inhibit measurements. ECL devices are designed to drive 50 Ω lines without reflections when the lines are terminated with 50 Ω returned to -2 V. The direct compatibility with a 50 Ω pulse generator results from the fact that 0 V from a 50 Ω source will produce -1 V at the input inhibit (inhibiting the counter), while a -1 V signal into 50 Ω will produce -2 V at the inhibit input, thus enabling the counter.

- 10 MHz IN/OUT provides a 10 MHz square wave output at 4 V p-p, ac coupled into 1.1k Ω, when the counter's internal timebase is enabled. It accepts a 10 MHz, 100 mV to 4 V p-p signal into 1.1 kΩ for external timebase operation. SPECIAL 08, 09, and 10 are used to select between the external, internal, and VXIbus CLK10 timebases, respectively.

PROGRAMMING

VXIbus CAPABILITIES

The EIP 1230A and 1231A support the following VXIbus capabilities:

Address Space	A16 only
Data Bus	D16
Device Class	Message-based instrument slave
Logical Address	Static configuration from 1 to 25
Bus Master	Not supported
Commander	Not supported
Communication	Word serial
Handshaking	Normal only
Interrupter	Dynamic Programmable Interrupter 1 to 7
Event Generation	Supported
Response Generation	Supported
Signal Register	Not supported

Shared Memory	Not supported
Trigger Lines	TTLTRG: SYNC, ASYNC protocols (the EIP 1230A and 1231A are trigger acceptors: they assert the higher numbered line of the assigned TTLTRG line pair in ASYNC mode). ECLTRG: Measurement inhibit (switchable from front panel).
Supported Word Serial Commands:	*Abort Normal Operation* *Assign Interrupter Line* *Asynchronous Mode Control* *Begin Normal Operation* *Byte Available* *Byte Request* *Clear* *Control Event* *Control Respond Normal Operation* *Read Interrupter Line* *Read Interrupters* *Read Protocol* *Read Protocol Error* *Read STB* *Trigger*

DEVICE-DEPENDENT FUNCTIONS

The EIP 1230A and 1231A counters provide the following capabilities:

1. Acceptance of device-dependent messages using the Byte Transfer Protocol to set the instrument measurement mode and parameters. The input buffer can store up to 256 characters. Execution of the device-dependent messages starts after the first message separator is accepted. Input of more characters will interrupt the execution so that the additional characters are accepted and stored for fast bus response (unless buffer is full).
2. Output of measurement results, or any parameter value or instrument mode, using the Byte Transfer Protocol on demand from the system controller.
3. Configuration of the output format in several ways to accommodate different system controllers and speed requirements.
4. Implementation of Serial Poll functions to allow the system controller to get a status byte from the instrument that gives device-dependent status information for various functions. The instrument can also be instructed to interrupt the controller on any ORed combination of the status events.

DEVICE-DEPENDENT MESSAGES

A device-dependent message generally consists of reserved words and numbers. The message structure depends on the type of message, and can be:

- Header only
- Header and argument
- Header and argument and terminator

Where the header is a reserved word, the argument is a number or a reserved word, and the terminator is a reserved word.

Messages can be concatenated with a comma or semicolon as separators. A message chain is terminated by asserting bit 8 (the END bit) of the *Byte Available* word serial command. Any device-reserved word will be recognized by at least two first characters (with the exception of RESET and INHIBIT which require the first four letters). These two characters are printed in **larger boldface** type in the following command lists to promote user familiarity with the shortened form of the command. Spelling of more characters (up to the full word) is optional for user program readability. For example:

INITIALIZE
INIT
IN are all recognized equivalently.

A <number> can be sent in any of the defined IEEE formats (NR1, NR2, NR3). For example:

12000
12000.00
001.2e4
.12000E+5 are all recognized equivalently.

The reserved word DEFAULT can replace a numeric argument for default value assignment (Default State).

The terminator in the parameter messages group is optional, and defaults to Hz or seconds.

The terminators are:

- GHZ
- MHZ
- KHZ
- HZ
- S or MS

A message with more than one word (like OUTPUT PERIOD) should have a space between the words. This is optional if the second word is a number ("OFFSET4.3e9" and "OFFSET 4.3E9" are recognized equivalently). Additional spaces in front of words, between words, or after a message are optional and will be ignored. Both upper and lower case characters are equally acceptable.

Control, mode, and parameter messages are all issued to the counter to enter instructions and data.

The following tables list the possible messages for the counters.

Control Messages

Header	Argument	Terminator	Description
CLEAR	None	None	Clears error message.
INITIALIZE	None	None	Reconfigures the device-dependent functions of the instrument to the power-on state.
RESET	None	None	Resets the converter and restarts the signal acquisition process. If a signal is found, a measurement will be taken, even if the counter is in HOLD.
TRIGGER	None	None	Triggers a new measurement cycle. If a measurement cycle is in progress, it will be aborted.

Mode Messages

Header	Argument	Terminator	Description
DYNAMIC	ON or OFF	None	Suppresses blanks and trailing zeros when counter is in output mode; results in faster free-field data transfer when DYNAMIC is ON. Default is OFF.
EXTERNAL	ON or OFF	None	Controls the INT/EXT timebase reference. (SPECIAL 08 can also be used to select the external timebase.) Default is OFF.
HEADER	ON or OFF	None	Provides an alpha header and terminator around each numeric data item for clarity when HEADER is ON. Default is OFF.
HOLD	ON or OFF	None	Holds the last result if ON. HOLD ON puts the counter into a triggered operational mode
SCIENTIFIC	ON or OFF	None	Selects engineering exponential notation when SCIENTIFIC is ON. Default is OFF.
SEPARATE	ON or OFF	None	Substitutes CR LF for the comma between multinumber results when SEPARATE is ON. Default is OFF.

Parameter Messages

Header	Argument	Terminator	Description
ASYNC	<number>	None	Selects the TTLTRG line pair to be used in the Asynchronous Trigger Protocol. The valid range is 0 to 3, corresponding to TTLTRG pairs 0 & 1, 2 & 3, 4 & 5, and 6 & 7, respectively. The ASYNC message enables the ASYNCHRONOUS TTLTRG trigger protocol. Issuing ASYNC 9 disables the protocol. Triggering Capabilities.
AVERAGE	<number>	None	This parameter controls the number of measurements to be averaged on frequency and pulse parameters. Select in the range of 1 to 99.
BAND	<number>	None	This parameter controls the frequency measurement range. Select a specific band according to the following table.

Band	Range
0	100 Hz to 250 MHz (CW only)
1	250 MHz to 1 GHz
2	950 MHz to 20 GHz (EIP 1231A) 950 MHz to 26.5 GHz (1230A)
3	26.5 GHz to 170 GHz (Optional, EIP 1230A only)

SUBBAND	<number>	None	This parameter controls the frequency measurement range of Band 3 and is set according to the remote sensor being used. Select the appropriate subband according to the following table.

Subband	Range
1	26.5 GHz to 40 GHz
2	33 GHz to 50 GHz
3	40 GHz to 60 GHz
4	50 GHz to 75 GHz
5	60 GHz to 90 GHz
6	75 GHz to 110 GHz
7	90 GHz to 140 GHz
8	110 GHz to 170 GHz

Parameter Messages (Continued)

Header	Argument	Terminator	Description
SUBBAND (Continued)			Examples: Issue BAND 3, SUBBAND 6 to select Band 3, subband 6. Issue SUBBAND 3 to select subband 3 (if counter is already in Band 3). Note: This command does not automatically set counter to Band 3.
CENTERFREQ	<number>	(Hz, kHz, MHz, or GHz)	This parameter controls the center frequency mode of operation in which the counter looks for a signal in the vicinity of the center frequency value. This mode can be used to reduce acquisition time or when measuring a particular signal in a multiple signal environment. This mode is available in either Band 2 or Band 3. Select Band 2 CENTERFREQ in the range of 900 MHz to 26.7 GHz for Model 1230A, and in the range of 900 MHz to 20.5 GHz for Model 1231A. The counter will lock on signals within ±50 MHz from the entered center frequency, depending on the power and frequency of the signal. The locking frequency is determined by the bandpass width of the YIG filter located at the input to Band 2. Select Band 3 CENTERFREQ in the range of the subband currently selected. The counter will lock on signals ±2 GHz from the entered frequency. The counter will NOT reject signals outside this range. If a signal more than 2 GHz from the entered frequency is applied, an erroneous reading may result. The value entered by the user is truncated to 10 MHz resolution. The number can be entered in any fixed-point format, with the units terminator that determines the scale of the input number. This function may be terminated by issuing CENTERFREQ DEFAULT.

Parameter Messages (Continued)

Header	Argument	Terminator	Description
FETCH	<number>	None	Recalls the counter setup stored in the storage register specified. Valid registers are 0 through 9.
HIGHLIMIT	<number>	(Hz, kHz, MHz, or GHz)	This parameter controls the high end of the frequency window that is searched for a signal in Band 2. Select the HIGHLIMIT in the range of 900 MHz to 26.7 GHz for Model 1230A and in the range of 900 MHz to 20.5 GHz for Model 1231A. The value entered by the user is truncated to 10 MHz resolution. This function is only available in Band 2. HIGHLIMIT must always be higher than LOWLIMIT. The number can be entered in any fixed-point format, with the units terminator that determines the scale of the input. This function may be deactivated by issuing HIGHLIMIT DEFAULT.
INHIBIT	<number>	None	Selects the input to be used for the measurement inhibit function. Arguments 0, 1, and 2 correspond to the VXIbus ECLTRG0 line, VXIbus ECLTRG1 line, and front panel, respectively. Note that inhibit is active high (i.e., the counter is inhibited by a logic high level and enabled by a logic low level).
IRQMASK	<number>	None	Selects the ORed combination of status events to cause an interrupt (Status Byte).
LOWLIMIT	<number>	(Hz, kHz, MHz, or GHz)	This parameter controls the low end of the frequency window that is searched in Band 2. Select LOWLIMIT in the range of 900 MHz to 26.7 GHz for Model 1230A, and in the range of 900 MHz to 20.5 GHz for Model 1231A. The value entered by the user is truncated to 10 MHz resolution. This function is only available in Band 2. LOWLIMIT must always be less than HIGHLIMIT. The number entered can be in any fixed-point format, with the units terminator determining the scale of the input number. This function may be deactivated by issuing LOWLIMIT DEFAULT.

Parameter Messages (Continued)

Header	Argument	Terminator	Description
MINPRF	<number>	(Hz, kHz, MHz, or GHz)	This parameter controls the minimum pulse repetition frequency of the pulsed signals that can be acquired and measured by the counter. For example, if a MINPRF of 500 Hz is selected, the counter will measure signals with a pulse repetition frequency of 500 Hz or greater. This parameter affects the acquisition speed indirectly via two internal processes: the waiting time for a pulse at each frequency step in the frequency range being searched, and the waiting time for a pulse when taking measurements before declaring a "signal lost" condition.
MULTIPLIER	<number>	None	This parameter controls the value of the constant M in the formula: Output frequency = (M x measured frequency) + B Where M is the frequency multiplier and B is the frequency offset. The frequency multiplier must be an integer in the range of 1 to 99.
OFFSETFREQ	<number>	(Hz, KHz, MHz, or GHz)	Allows the entry of a positive or negative frequency to 1 kHz resolution into the offset frequency register. This parameter controls the constant B in the formula: Output frequency = (M x measured frequency) + B where M is the frequency multiplier and B is the frequency offset. Select OFFSETFREQ in the range of -99.99 999 GHz to +99.999 999 GHz. The number can be entered in any fixed-point format, with the units terminator that determines the scale of the input number.

Parameter Messages (Continued)

Header	Argument	Terminator	Description
RESOLUTION	<number>	None	This parameter controls the frequency measurement resolution. Select the desired resolution according to the following table:

Resolution	Frequency	Gate Time
2	100 Hz	10 ms (Band 0 only)
3	1 kHz	1 ms
4	10 kHz	100 µs
5	100 kHz	10 µs
6	1 MHz	100 µs
7	10 MHz	1 µs
8	100 MHz	1 µs
9	1 GHz	1 µs

SAMPLERATE	<number>	(S or MS)	Sets a delay between measurement values (0 to 100 s, 10 ms resolution).
SPECIAL	<number>	None	This command activates any of the various special functions (0 to 99). Refer to the special function directory for more information.
STORE	<number>	None	Stores the current counter setup in the storage register specified. Valid registers are 0 through 9. Register 0 controls the default state of the instrument at power-on and after initialization. To restore the factory default settings to register 0, issue STORE DEFAULT.
SYNC	<number>	None	Selects the TTLTRG line to be used in the Synchronous Trigger Protocol. The valid range is 0 to 7. The SYNC message enables the SYNCHRONOUS TTLTRG trigger protocol. Issuing SYNC 9 disables the protocol.
V1FREQ	<number>	(Hz, kHz, MHz, or GHz)	Sets a start frequency for VCO sweep (SPECIAL 41 and SPECIAL 42).

Parameter Messages (Continued)

Header	Argument	Terminator	Description
V2FREQ	<number>	(Hz, kHz, MHz, or GHz)	Sets a top frequency for VCO sweep (SPECIAL 41 and SPECIAL 42).
Y1FREQ	<number>	(Hz, kHz, MHz, or GHz)	Sets a start frequency for YIG sweep (SPECIAL 40).
Y2FREQ	<number>	(Hz, kHz, MHz, or GHz)	Sets a stop frequency for YIG sweep (SPECIAL 40).
Y3FREQ	<number>	(Hz, kHz, MHz, or GHz)	Sets YIG frequency (SPECIAL 20).
MEMORY	hex_adrs	hex_data	Accesses a memory location and, if desired, alters it (SPECIAL 46).
MEMORY	INCREMENT	hex_data	Accesses the next location and, if desired, alters it (SPECIAL 46).
MEMORY	DECREMENT	hex_data	Accesses the previous location and, if desired, alters it (SPECIAL 46).

Output Control Messages

These commands are used to select data for output.

Command	Description
OUTPUT ASYNC	Outputs the current TTLTRG line pair used in the Asynchronous Trigger Protocol.
OUTPUT AVERAGE	Outputs the current averaging value.
OUTPUT BAND	Outputs the current band number.
OUTPUT CENTERFREQ	Outputs the current center frequency.
OUTPUT DATE	Outputs a 25-character string that shows the firmware revision level and date.
OUTPUT DEFAULT	Outputs frequency data.
OUTPUT ERRORNUMBER	Outputs the number of the last error. Error Messages.

Output Control Messages (Continued)

Command	Description
OUTPUT FREQUENCY (AND WIDTH) (AND PERIOD)	Controls which measurement results to output. (Note: More than one measurement result is optional. The order of the results is preserved in the output. Output frequency, width and period can be in any combination.)
OUTPUT HIGHLIMIT	Outputs the current high frequency limit.
OUTPUT IDENTIFICATION	Outputs "EIP123nA VXI ddd", where n is 0 or 1 and ddd is the revision of the VXIbus specification that the counter complies with.
OUTPUT INHIBIT	Outputs 0, 1, or 2, indicating the input used for the measurement inhibit function.
OUTPUT IRQMASK	Outputs the combination of device-dependent status events required to cause an interrupt.
OUTPUT LEVEL	Outputs the Band 2 detected RF level (SPECIAL 20).
OUTPUT LOWLIMIT	Outputs the current low frequency limit.
OUTPUT MEMORY	Outputs the content of the memory in the last accessed location.
OUTPUT MINPRF	Outputs the current MINPRF.
OUTPUT MULTIPLIER	Outputs the current multiplier value.
OUTPUT OFFSETFREQ	Outputs the current offset frequency.
OUTPUT RESOLUTION	Outputs the current frequency measurement resolution.
OUTPUT SAMPLERATE	Outputs the current delay time between measurement values.
OUTPUT SETUP	Outputs a 216-character string that describes the current setup (section on output setup command).
OUTPUT SUBBAND	Outputs the number of the current subband. OUTPUT SYNC Outputs the current TTLTRG line used in the Synchronous Trigger Protocol.
OUTPUT V1FREQ	Outputs the current start frequency for VCO sweep (SPECIAL 41).
OUTPUT V2FREQ	Outputs the current stop frequency for VCO sweep (SPECIAL 41).
OUTPUT Y1FREQ	Outputs the current start frequency for YIG sweep (SPECIAL 40).

Output Control Messages (Continued)

Command	Description
OUTPUT Y2FREQ	Outputs the current stop frequency for YIG sweep (SPECIAL 40).
OUTPUT Y3FREQ	Outputs the current YIG frequency (SPECIAL 20).

DEFAULT STATE

Default conditions are invoked by issuing the reserved word DEFAULT in place of a numeric argument. If the contents of memory register 0 are still equal to the factory-set values, then the instrument default state is achieved after power-on, self-check, and hardware initialization functions are completed.

Parameter	Default State
ASYNC	9 (disabled)
AVERAGE	01
BAND	2 (subband 1 if in Band 3)
CENTERFREQ	0 (off)
CLEAR	Activated
DYNAMIC	OFF
EXTERNAL	OFF
HEADER	OFF
HIGHLIMIT	26.7 GHz (EIP 1230A) or 20.5 GHz (EIP 1231A)
HOLD	OFF
INHIBIT	2 (front panel)
IRQMASK	000
LOWLIMIT	900 MHz
MINPRF	2 kHz
MULTIPLIER	01
OFFSETFREQ	0 MHz
RESOLUTION	3
SAMPLERATE	0 ms (maximum rate)
SCIENTIFIC	OFF
SEPARATE	OFF
SPECIAL	00 (all cleared)
SUBBAND	1 (if in Band 3)
SYNC	9 (disabled)
V1FREQ	400 MHz
V2FREQ	505 MHz

DEFAULT STATE (Continued)

Parameter	Default State
Y1FREQ	900 MHz
Y2FREQ	26700 MHz
Y3FREQ	1000 MHz
Buffer Pointers	Reset
Converter	Reset
IRQ state	Passive

OUTPUT FORMATS

After receiving a *Byte Request* word serial command, the counter outputs one byte of the current configuration, parameter value, or measurement result in accordance with the last specified output control message. (Note: Most data transfers will require multiple *Byte Available* and *Byte Request* commands.) After power-on or clear, the counter outputs frequency measurement results (as it does after the OUTPUT DEFAULT command).

The counter can be instructed to output any ordered combination of the three possible measurements.

Examples: OUTPUT FREQ AND WIDTH
OUTPUT WIDTH AND PERIOD
OUTPUT WIDTH AND FREQUENCY AND PERIOD

The format of each output message can be controlled by the following features:

DEFAULT - Outputs data in default format. The fixed fields are 16 characters long for the header and argument, and 5 characters long for the terminator. When none of the output-formatting features above are turned on, numbers are right justified, letters are left justified, and blanks are filled.

SCIENTIFIC - provides exponential notation with engineering exponents when SCIENTIFIC is ON. Default is OFF.

DYNAMIC - suppresses blanks and trailing zeros for faster data transfer when DYNAMIC is ON. Default is OFF.

SEPARATE - Substitutes CR LF for the comma between results of one measurement (e.g., freq, period) when SEPARATE is ON. Default is OFF.

HEADER - provides an alpha header and terminator around each numeric data item for clarity, when HEADER is ON. Default is OFF. Note: Terminator takes over the exponential role if both SCIENTIFIC and HEADER are ON.

Example: The counter is measuring a 12.34 GHz pulsed signal with 98 ns width and 14.567 ms period. The operator issues the following messages through the controller:
RESOLUTION 6
OUTPUT FREQ AND WIDTH AND PERIOD

The output for the following parameters will be as follows (b is for blank):

Parameter	Output
Default	bbbbb12340000000,bbbbb0.000000100,bbbbb0.000014570 CR LF
SCIENTIFIC ON	bbbbbbbb12.340E+9,bbbbbbbbbb100E-9, bbbbbbbb14.57E-6 CR LF
DYNAMIC ON	12.34E9,100E-9,14.57E-6 CR LF
SEPARATE ON	12.34E9 CR LF 100E-9 CR LF 14.57E-6 CR LF
HEADER ON	FREQUENCY 12.34 GHz CR LF WIDTH 100 NSEC CR LF PERIOD 14.57 USEC CR LF

If the counter is searching, a zero will be output to the controller (on all results) once every search loop.

If the counter has found a signal, a measurement result will be output only once; thus, when the instrument is in HOLD, the user must trigger the counter before requesting another reading or the counter will indicate a word serial protocol error (DOR Violation).

OUTPUT AND FORMAT EXAMPLES

The following programs illustrate how controllers function with the counter. These programs set the counter up in a sample configuration and program it to make a series of measurements on a 12.5 GHz pulsed signal with a 13.258 ms period. The logical address of the counter is assumed to be 18 and primary addressing is used.

- Hewlett Packard Model 320 with a Colorado Data System 73A-151 Slot-0 Resource Manager
- 10 DIM A$[36]
  20 OUTPUT 718; "INIT"
  30 WAIT 0.4
  40 OUTPUT 718; "RE 4"
  50 OUTPUT 718; "HI 17.5 GHZ,LO 1.1 GHZ"
  60 WAIT 0.1
  70 OUTPUT 718; "OUTPUT WI AND FR"
  80 WAIT 0.1
  90 ENTER 718;A$
  100 DISP A$
  110 END

This program initializes the counter, provides a resolution value, a high and low frequency limit, and instructs it to output pulse width and frequency to the controller. The controller should display something like this:

0.0000132580, 12500000000

- Hewlett Packard Model 320 with a Colorado Data System 73A-151 Slot-0 Resource Manager

- 10 OUTPUT 718; "BA 3, RE 4, OF -4.55 MHZ"
  15 WAIT 0.03
  20 ENTER 718;A$
  30 PRINT "Frequency minus offset equals",A
  40 GO TO 20

This program causes the counter to continuously make frequency measurements and prints the measurement results. To end the program, initiate a STOP command. This is accomplished on the HP 320 with the STOP key. To restart the program, enter the RUN statement followed by the line number that is printed in the interrupt message.

DATA INPUT AND OUTPUT SPEED

Input Speed

It takes a specific amount of time for the counter to process input data (error checking, formatting, changing the mode of operation, etc.). To prevent the data rate of the bus from slowing down while the counter is doing input data processing, the data is accepted as soon as it is available on the bus and is temporarily stored in a 256-character storage memory.

VXIbus users need to be aware of the difference between accepting data and complying with it. If the counter is asked to output a reading before it is finished processing the input data, the output will not reflect the newly entered data. To prevent this, sufficient programmed delays must be provided (the previous sample output program format). The user may also take advantage of the counter's interrupt capability to report when the input buffer is empty. Bit 7 in the status byte can be used to determine if the counter has completed the processing of messages. Refer to the Status Byte section.

Output Speed

Several options are available to increase the output speed of the counter. Each of the following conditions decreases the measurement cycle time. The fastest measurement cycle time is achieved with all of the following conditions set:

DYNAMIC ON	Suppresses leading blanks. Note: The controller must have free field capability.
HEADER OFF	Outputs the numeric results without header or terminator (default).
SAMPLERATE 0	Same as SPECIAL 63 (default).
SCIENTIFIC OFF	Outputs fixed point results which are shorter than exponential notations (default).
SPECIAL 61	Disables the tracking feature, thus saving the time required for YIG and VCO corrections. Note: the counter will no longer be able to track moving signals.
SPECIAL 63	Disables sample rate control, thus deleting any delay between gates.

READING MEASUREMENTS

There are two basic methods for taking readings depending on the status of the HOLD command. When HOLD is ON, the counter takes one reading and waits for a RESET or TRIGGER command. Upon receipt of one of these commands, the counter will perform another measurement and, when requested, output the new reading over the VXIbus. Note that a measurement result will be output only once; thus, when the instrument is in HOLD, the user must trigger the counter before requesting another reading or the counter will report a DOR Violation of the word serial protocol. If no signal is found, the counter will output a zero.

When the HOLD command is OFF, data is read out to the bus in the normal way. The reading is automatically updated according to the specified sample rate, and the counter can output successive readings without requiring a RESET or TRIGGER command each time.

OUTPUT SETUP COMMAND

The OUTPUT SETUP command causes the counter to output a 216-character string that corresponds to the current setup of the instrument. The string is a list of counter mnemonics and their values. The string can be modified and reissued to the counter as a simple means of reading and modifying the state of the instrument. The following sample program, for the HP Model 320 controller, can be used to obtain the setup string:

```
10 DIM A$[250]                    ! dimension a variable to hold the string
20 OUTPUT 718;"OUTPUT SETUP"      ! send command to counter
30 ENTER 718;A$                   ! get output from counter
40 DISP A$                        ! display output on HP-320
```

The following can be used to decode the returned setup string. The information contained in the parentheses will change depending upon the current state of the instrument. Once the setup string has been read by the commander, the output control reverts back to its previous setting (e.g., OU FR).

Setup string elements:

AS9,	ASYNCHRONOUS (9)
AV01,	AVERAGE (01)
BA2,	BAND (2)
CE000000MH,	CENTERFREQ (0) MHz NOT ACTIVE
DY0,	DYNAMIC (0) OFF (1) ON
HE0,	HEADER (0) OFF (1) ON
HI020500MH,	HIGHLIMIT (20500) MHz
HO0,	HOLD (0) OFF (1) ON
INHI0,	INHIBIT (0) ECLTRG0 (1) ECLTRG1 (2) FRONT PANEL

IR000,	IRQMASK (000)
LO000900MH,	LOWLIMIT (900) MHz
MI0002000,	MINPRF (2000) Hz
MU01,	MULTIPLIER (01)
OF+000000000KH,	OFFSETFREQ (0) kHz
OU FR,	OUTPUT (FR) FREQUENCY
RE3,	RESOLUTION (3)
SA000000MS,	SAMPLERATE (0) ms
SC0,	SCIENTIFIC (0) OFF (1) ON
SE0,	SEPARATE (0) OFF (1) ON
SU1,	SUBBAND (1)
SP09,	SPECIAL (09) ACTIVE
SP45,	SPECIAL (45) ACTIVE
SP62,	SPECIAL (62) ACTIVE
SP64,	SPECIAL (64) ACTIVE
SP68,	FOR EIP USE ONLY
SY9,	SYNCHRONOUS (9)
V1000400MH,	V1FREQ (400) MHz
V2000505MH,	V2FREQ (505) MHz
Y1000900MH,	Y1FREQ (900) MHz
Y2026700MH	Y2FREQ (26700) MHz
Y3001000MH	Y3FREQ (1000) MHz

STATUS BYTE

Both the EIP 1230A and 1231A maintain a one byte register that contains current information on the device-dependent status of the instrument. This register, called the status byte, can be read over the VXIbus using the *Read STB* word serial command. The counter responds to this command by returning its status byte in the lower 8 bits of the Data Low register. The status byte is structured as follows:

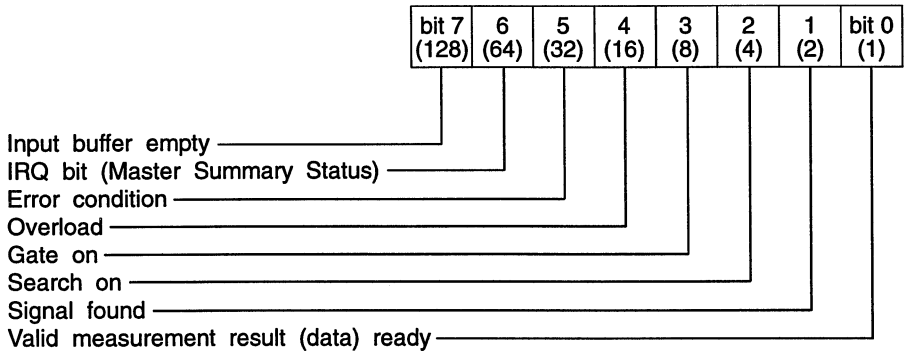


Figure 3-2. Status Byte Structure.

For example, execute the following commands using a HP Model 320.

```
10 A=SPOLL(718)
20 DISP A
30 END
```

With no signal applied to the counter, the value displayed on the HP 320 controller should be 132. Since the value is the weighted sum of all the bits set in the status byte, a value of 132 indicates that the counter's input buffer is empty and the counter is in the search mode.

INTERRUPT MASK

The counter can be instructed to send an interrupt (over an IRQ line on the VXIbus) when any ORed combination of the bits in the status byte are set. This is done by sending the counter an interrupt mask.

For example, to instruct the counter to generate an interrupt whenever it has valid data available OR an error condition exists, send the following interrupt mask:

OUTPUT 718; "IRQMASK 33"

This would tell the counter to generate an interrupt whenever bit-0 or bit-5 of the status byte are set. Since bit-0 corresponds to valid measurement result ready and bit-5 corresponds to error condition, the counter would generate an interrupt whenever either an error condition existed or a valid measurement was available.

The following items should be included in any program using the interrupt feature:

1. Tell the counter which interrupt line (IRQ 1-7) to use. This is done using the *Assign Interrupter Line* word serial command.
2. Tell the counter when to generate an interrupt. That is, tell the counter which events should generate an interrupt. This is done using the IRQMASK command.
3. Tell the controller to monitor the appropriate IRQ line on the VXIbus. This is done using the *Assign Handler Line* word serial command.
4. Tell the controller what to do when it receives an interrupt.
5. Poll the counter's status byte after an interrupt is generated to clear the interrupt. When the counter generates an interrupt it sets bit 6 in the status byte. Serial polling the instrument clears the IRQ bit and allows the instrument to generate a new interrupt upon the next occurrence of the conditions specified in the IRQMASK. Serial polling is accomplished using the *Read STB* word serial command.
6. It may also be necessary to clear the interrupt register in the controller. Consult your manual on the controller for more information on clearing the interrupt register in the controller.

The following program, written on an HP Model 320 computer, demonstrates how to use the interrupt feature to obtain a valid measurement from the counter.

```
10 ASSIGN @COUNTER TO 718          ! Assigns 718 to address variable
                                   ! The number 7 is the GPIB interface select code
                                   ! and 18 is the counters VXIbus logical address
20 REMOTE @COUNTER                 ! Place counter in Remote
30 OUTPUT @COUNTER;"IRQMASK 1"! Send IRQMASK to counter
40 ENABLE INTR 7;2                 ! Enable interrupt in controller
50 ON INTR 7 GOTO FLAG             ! Tell controller how to handle interrupt
60 WAITING:                        ! Label
70 PRINT "WAITING FOR VALID MEASUREMENT"
80 GOTO WAITING
90 FLAG: PRINT "***** INTERRUPT RECEIVED *****"
100 ENTER @COUNTER;FREQ            ! Input frequency from counter
110 PRINT "FREQ = ";FREQ           ! Print frequency
120 S2 = SPOLL(@COUNTER)           ! Clear IRQ bit in counter
130 STATUS 7,4;S                   ! Clear SRQ bit in controller
140 OUTPUT @COUNTER;"IRQMASK 00"   ! Turn off IRQMASK in counter
150 OFF INTR 7                     ! Turn off interrupt in controller
160 END                            ! Program end
```

To demonstrate this program, set up the counter with no signal applied and start the program running. The controller should continually print out "Waiting for measurement". Then apply a signal. As soon as the counter finds the signal and counts it, the controller will print out the frequency of the signal.

A NOTE ON VXIbus INTERRUPTS

There are two different types of interrupts in the VXIbus environment: event interrupts and response interrupts. An event interrupt is an instrument specific condition. Revision 1.3 of the VXIbus Specification defines four different types of events: No Cause Given, Request True, Request False, and User Defined. The EIP 1230A and 1231A generate only Request True events. These interrupts are controlled by masking certain bits of the EIP 1230A and 1231A device-dependent status byte. This status byte permits the counter to generate event interrupts on device-dependent conditions such as signal found, measurement ready, error condition, etc.

The response interrupt is generated in response to word serial commands. This interrupt indicates either handshaking-type responses or word serial protocol conformance errors. These errors include Multiple Queries, Unsupported Command, DIR and DOR violations, Read Ready and Write Ready violations, etc. Word serial protocol errors are read using the *Read Protocol Error* word serial command.

After the commander receives an IRQ, the Status/ID word will indicate whether the interrupt is an event or a response. If bit 15 of the Status/ID word is 0, then the interrupt is a response; if bit 15 is 1, then the interrupt is an event. The *Read STB* word serial command may be used to determine the cause of the event. EIP 1230A and 1231A device-dependent errors, reported via bit 5 of the status byte, may be further defined by issuing the OUTPUT ERROR command to retrieve an error code number. If the interrupt is a response, the cause of the interrupt will be reported in the Status/ID word. If the cause is a word serial protocol error, the *Read Protocol Error* word serial command will indicate the specific problem. The specific meaning of each error number is given at the end of this section.

TRIGGERING CAPABILITIES

The EIP 1230A and 1231A can accept triggers from several sources: the device-dependent mnemonic TRIGGER, the word serial command *Trigger*, or the VXIbus TTLTRG trigger lines. Both the mnemonic TRIGGER and the word serial command *Trigger* have the same effect: they trigger a new measurement cycle. Typically, these commands are used with the counter in the hold mode (i.e., HOLD ON) for control of measurement timing.

Triggers can also be issued over the VXIbus TTLTRG trigger lines. There are two types of TTLTRG trigger protocols, defined in the VXIbus specification, that the EIP 1230A and 1231A support: the synchronous (SYNC) trigger protocol and the asynchronous (ASYNC) trigger protocol.

TTLTRG SYNC Trigger Protocol

The TTLTRG SYNC trigger protocol is a single line broadcast, multiple acceptor protocol. It is used to simultaneously trigger several devices and does not require an acknowledgment from any acceptors. A trigger received using the TTLTRG SYNC trigger protocol has the same effect as the device-dependent command TRIGGER and the word serial command *Trigger*: they all trigger a new measurement cycle.

The TTLTRG SYNC trigger mode is enabled by issuing the device-dependent mnemonic SYNC n, where n is the assigned TTLTRG line (0 to 7). The TTLTRG SYNC trigger mode is disabled by issuing SYNC 9. When in the TTLTRG SYNC trigger mode, the counter will only make measurements in response to a trigger (i.e., the counter performs as if it is in hold).

TTLTRG ASYNC Trigger Protocol

The TTLTRG ASYNC trigger protocol is a two line single source, single acceptor protocol. It is used to coordinate the actions of a pair of devices. The trigger source device initiates an operation by asserting the lower numbered line of an assigned pair of TTLTRG lines. The trigger acceptor acknowledges by asserting the higher numbered line of the TTLTRG line pair. The EIP 1230A and 1231A are TTLTRG ASYNC acceptors, i.e., they assert the higher numbered line of the assigned TTLTRG line pair. The assertion time is 300 µs.

The TTLTRG line pairs are lines 0 and 1, lines 2 and 3, lines 4 and 5, and lines 6 and 7. A line pair is selected by issuing the device-dependent command ASYNC n, where n denotes the TTLTRG line pair (0 to 3). The line pairs above correspond to n values of 0, 1, 2, and 3, respectively. The ASYNC n command enables the TTLTRG ASYNC trigger mode. ASYNC 9 disables the mode. When in the TTLTRG ASYNC trigger mode, the counter will only make measurements in response to a trigger (i.e., the counter performs as if it is in hold).

A typical application of the TTLTRG ASYNC protocol is frequency profiling of voltage-controlled oscillators, pulses, etc. (VCO Settling Time Measurements and Pulse Profile Measurements.) A pulse generator, which must be an ASYNC source, initiates the measurement series by asserting the lower numbered line of the assigned TTLTRG line pair after its output is configured and settled. Either the front panel inhibit input or one of the two ECLTRG lines may be used to drive the measurement inhibit of the counter. When the counter detects the trigger on the lower numbered line, it will initiate its measurement. When the measurement is complete (i.e., a valid measurement result is ready; note this is the same as bit 0 of the status byte), the counter will assert the higher numbered line of the TTLTRG line pair. Upon receiving this acknowledgment, the pulse generator will move to its next setting and, when settled, assert the lower numbered TTLTRG line. The counter, upon detecting the trigger, will once again initiate its measurement cycle and, when complete, assert the higher numbered TTLTRG line. This process continues until the pulse generator has cycled through all of its settings.

The commander can set the counter to generate an interrupt when data are valid (bit 0 of the status byte). When interrupted, the commander should read the result from the counter. Since the counter does not have any provision to store data, any data not read by the commander before the next measurement is complete will be lost.

SPECIAL FUNCTION DIRECTORY

DEFINITION OF SPECIAL FUNCTIONS

The special functions of the EIP 1230A and 1231A counters can be divided into three categories:

- Counter operation verification - SPECIAL 01 and 06 provide the user with a means of verifying that the counter is operational.
- Calibration/troubleshooting aids - SPECIAL 20 through 49 and 90 through 99 aid the user in calibrating and/or troubleshooting the counter.
- Counter capability enhancements - SPECIAL 08, 09, 10, and 50 through 89 provide counter capability enhancements for specialized applications.

Further information about how each special function works is summarized at the end of each discussion. The summary includes the following indicators:

ONE-SHOT or CONTINUOUS ACTION FUNCTIONS

1. One-shot action functions - automatically revert the counter to its normal operation after a specific action has been taken. These special functions are designated ONE-SHOT.
2. Continuous action functions - stop all normal operations of the counter and cause it to stay in the special function mode until the user terminates the function. Most continuous action functions are terminated when a new command is received over the VXIbus. After the special function is terminated, the function corresponding to the command received will be serviced and a RESET will be generated. Exceptions to the above termination sequence will be stated in the individual special function descriptions. These functions are designated STOP/RESET or STOP/NO RESET as applicable.

ACTIVATION OF SPECIAL FUNCTIONS

CAUTION

Executing SPECIAL 46, 76, 91, and 92 can cause a loss of calibration data. To prevent this from occurring, access to these functions is blocked by an internal memory protect switch. Attempting to access these functions with the memory protect switch in the protect position will cause the counter to issue error message 53. Please refer to the service manual for information on the memory protect switch.

To activate a special function, issue "SPECIAL dd", where dd is the two-digit special function number. Activating special functions will not alter any previously entered parameters unless specifically stated. Issuing a "SPECIAL 00" will terminate all previously activated special functions.

DESCRIPTION OF SPECIAL FUNCTIONS

SPECIAL 01 - 100 MHz Self-Test ONE-SHOT

This function will terminate all previously activated special functions. This function is used to verify that the count chain, gate generator, and the VCO are operational. When this function is entered, the counter will:

1. Exit the current band.
2. Set the hardware to the self-test mode.
3. Set the VCO to 400 MHz.
4. Set the counter to take frequency measurements only.
5. Start the measurement cycle. The measurement result should be 100 MHz ±1 count.

SPECIAL 06 - PROM Check Sum Test ONE-SHOT

This function generates a check sum for the PROM in the counter and compares it with the check sum table stored in the firmware. If the check sum is incorrect, error message 61 will be issued. At the same time, the error condition status bit in the status byte will be set.

SPECIAL 08 - External Time Base Select ONE-SHOT

Selecting this function causes the counter to accept an external timebase input through the front panel.

SPECIAL 09 - Internal Time Base Select ONE-SHOT

Selecting this function causes the counter to use its internal 10 MHz timebase.

SPECIAL 10 - VXIbus CLK10 Time Base Select ONE-SHOT

Selecting this function causes the counter to use the VXIbus CLK10 as its timebase.

SPECIAL 20 - Band 2 Detected RF Level — STOP/RESET

This function outputs the relative power level of the input signal. It verifies coarse calibration of the Band 2 YIG DAC offset and YIG DAC slope adjustments.

To activate this function, first, enter the YIG frequency using the Y3FREQ command, second, issue SPECIAL 20, and third, issue OUTPUT LEVEL. The relative signal level may then be read back from the counter.

SPECIAL 40 - Sweep YIG DAC — STOP/RESET

This special function sweeps the YIG DAC continuously from F1 to F2 in 2 MHz steps until the function is terminated. The sweep rate is controlled by the sample rate. Maximum sweep rate may be obtained by disabling the sample rate (SPECIAL 63) before calling this function. If F1 and F2 are equal, the YIG DAC will be set to that particular frequency.

To activate this function, first enter the start and stop frequencies (F1 and F2, respectively). The start frequency is entered with the command Y1FREQ, and the stop frequency with Y2FREQ. SPECIAL 40 may then be activated by issuing SPECIAL 40. Note that Y1FREQ and Y2FREQ must be specified before invoking SPECIAL 40.

SPECIAL 41 - Sweep VCO With VCO Power Amplifier On — STOP/RESET

This special function sweeps the VCO continuously from F1 to F2 in 50 kHz steps until the function is terminated. The sweep rate is controlled by the sample rate. Maximum sweep rate may be obtained by disabling the sample rate (SPECIAL 63) before calling this function. If F1 and F2 are equal, the VCO will be set to that particular frequency. The VCO power amplifier is turned on during this function.

To activate this function, first enter the start and stop frequencies (F1 and F2, respectively). The start frequency is entered with the command V1FREQ, and the stop frequency with V2FREQ. SPECIAL 41 may then be activated by issuing SPECIAL 41. Note that V1FREQ and V2FREQ must be specified before invoking SPECIAL 41.

SPECIAL 42 - Sweep VCO With VCO Power Amplifier Off — STOP/RESET

This special function sweeps the VCO continuously from F1 to F2 in 50 kHz steps until the function is terminated. The sweep rate is controlled by the sample rate. Maximum sweep rate may be obtained by disabling the sample rate (SPECIAL 63) before calling this function. If F1 and F2 are equal, the VCO will be set to that particular frequency. The VCO power amplifier is turned off during this function.

To activate this function, first enter the start and stop frequencies (F1 and F2, respectively). The start frequency is entered with the command V1FREQ, and the stop frequency with V2FREQ. SPECIAL 42 may then be activated by issuing SPECIAL 42. Note that V1FREQ and V2FREQ must be specified before invoking SPECIAL 42.

SPECIAL 44 - Disable Normal Operations — STOP/RESET

This function prevents the counter from performing the normal converter lock and measurement cycles. It freezes the counter in the state it was in at the moment the function was activated. SPECIAL 44 remains activated until terminated through SPECIAL 45 or SPECIAL 00.

SPECIAL 45 - Enable Normal Operations — STOP/RESET

This function reverses the action taken with SPECIAL 44. Special 45 re-enables normal counter operation and generates a reset.

SPECIAL 46 - Display and/or Alter Memory — STOP/RESET

CAUTION



Care must be used when operating SPECIAL 46. Although the counter cannot be damaged by this function, stored calibration data can be changed. For this reason, access to this function is blocked by an internal memory protect switch. Attempting to access this function with the memory protect switch in the protect position will cause the counter to issue error message 53.

This function is used to display and/or alter memory locations. When this function is activated, the counter continues its normal operations, unless SPECIAL 44 has previously been activated. To display memory contents, the OUTPUT MEMORY command may be used. When requested for memory data, the contents of the last memory location accessed are displayed. A specific location in memory can be accessed using the MEMORY OHHHH command, where H represents a hexadecimal digit. To alter the contents of a memory location, the MEMORY OHHHH OHH command can be used. Note: SPECIAL 46 need not be activated when accessing and altering memory locations. These operations are done in the background. Refer to the service manual for information on disabling the memory protect.

SPECIAL 47 - Count Chain Test — STOP/RESET

This function causes the counter to measure the frequency of the signal present at the input of the count chain board without having the counter converter locked on the signal. The counter will not measure pulse parameters when this function is active. When SPECIAL 47 is activated, the counter stops the normal converter lock and measurement cycles. The VCO, YIG, and all the microprocessor-controlled hardware switches remain in the state they were in when the function was activated. The counter then starts measuring the frequency of the signal present at the input to the count chain board. The measurement results are available over the VXIbus. This function does not check periodically for the presence of a signal as in the normal operation of the counter.

SPECIAL 61 - Disable Input Signal Tracking — ONE-SHOT

This special function disables the counter's input signal tracking function. By disabling the signal tracking ability, the counter's measurement cycle is shortened. However, the counter is no longer able to track moving signals.

This function may be reversed by activating SPECIAL 62.

SPECIAL 62 - Enable Input Signal Tracking ONE-SHOT

This function reverses the action of SPECIAL 61.

SPECIAL 63 - Disable Sample Rate Control ONE-SHOT

This function causes the counter to ignore the sample rate control. The counter starts a new measurement cycle as soon as the last one is finished. This function shortens the measurement cycle time. It is equivalent to setting the SAMPLERATE to zero.

SPECIAL 64 - Enable Sample Rate Control ONE-SHOT

This function reverses the action of SPECIAL 63.

SPECIAL 74 - Read Relative Frequency ONE-SHOT

When this function is activated, the counter assigns a negative value to the last frequency reading and enters it into the frequency offset register (overwriting any previously entered frequency offset). The last input frequency in this case means the actual frequency of the input signal, not including the effects of a frequency multiplier or another special function. The counter outputs the relationship, i.e., the difference, between the last input frequency and the current one, subject to any other functions activated. It continues to do so until the frequency offset is reset by issuing the command OFFSET 0.

SPECIAL 75 - Display IF Readings ONE-SHOT

When this function is activated, the counter assigns a negative value to the local oscillator (LO) frequency and enters it into the frequency offset register (overwriting any previously entered frequency offset). The counter then subtracts the LO frequency from the input frequency and outputs the resulting IF. This continues until the frequency offset is reset by issuing the command OFFSET 0.

SPECIAL 76 - EEPROM Test ONE-SHOT

CAUTION



Care must be used when operating SPECIAL 76. Although the counter cannot be damaged by this function, if execution of this function is interrupted prior to completion, a loss of the data contained in the EEPROM will occur. For this reason, access to this function is blocked by an internal memory protect switch. Attempting to access this function with the memory protect switch in the protect position will cause the counter to issue error message 53.

This function allows the user to test the EEPROM by performing write and read tests on each location on the EEPROM. When SPECIAL 76 is activated, the read/write tests performed require approximately eight minutes to complete. If any location in the memory fails, error message 94 will be issued. The counter will not respond to any commands until the test is completed. Refer to the service manual for information on disabling the memory protect.

SPECIAL 91 - YIG DAC Automatic Calibration

CAUTION

Care must be used when operating SPECIAL 91. Although the counter cannot be damaged by this function, improper operation of it can affect the counter calibration. For this reason, access to this function is blocked by an internal memory protect switch. Attempting to access this function with the memory protect switch in the protect position will cause the counter to issue error message 53.

This function is used to calibrate the Band 2 input filter. Refer to the service manual for complete information.

SPECIAL 92 - Gate Accuracy Calibration

CAUTION

Care must be used when operating SPECIAL 92. Although the counter cannot be damaged by this function, improper operation of it can affect the counter calibration. For this reason, access to this function is blocked by an internal memory protect switch. Attempting to access this function with the memory protect switch in the protect position will cause the counter to issue error message 53. This function is used for calibration of the counter. Refer to the service manual for complete information.

ERROR MESSAGES

When an error occurs, an error message number will be issued. The probable cause of each error is listed below.

02 Lower limit higher than high limit
03 Frequency limits entry only in Band 2
04 Center frequency entry only in Band 2 or Band 3
05 Center frequency entry outside current band range
06 No valid data in storage registers for recall feature
07 Converter unable to lock on signal during special
09 Illegal register entry
10 Illegal band entry
11 Illegal sub-band entry
12 Illegal resolution entry
13 Illegal special function entry
14 Illegal average entry
15 illegal multiplier entry
16 Illegal offset frequency entry
17 Illegal center frequency entry

18 Illegal MINPRF entry
19 Illegal low limit entry
20 Illegal high limit entry
21 Illegal sample rate entry
22 Illegal IRQ entry
24 Illegal VCO frequency 1 entry
25 Illegal VCO frequency 2 entry
26 Illegal YIG frequency 1 entry
27 Illegal YIG frequency 2 entry
28 Illegal YIG DAC frequency entry
29 Frequency overflow due to multiplier
30 Pulse parameters measurements greater than specified MINPRF
31 VXI input message too long
32 VXI message starts with a number
33 VXI message starts with a wrong number
34 Unidentified word found
35 Word misspelled
36 Missing space
37 Wrong mode argument
40 Non-numeric parameter value
41 Wrong frequency terminator
42 Wrong time terminator
43 Wrong output argument
44 Numeric argument syntax error
45 Numeric mantissa has too many digits
46 Numeric exponent has too many digits
47 Hex data should be preceded by a zero
48 No hex memory address specified
49 Illegal hex data entry
50 Illegal hex address entry
52 Illegal entry
53 Access to this function blocked by memory protect switch
60 RAM fault
61 ROM check sum error
71 Count Chain board missing
72 Gate Generator board missing
91 Option not installed
92 Band 3 option in a 1231A unit
94 Non-volatile memory failure
99 No IF detected

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4

OPERATIONAL VERIFICATION TESTS

INTRODUCTION

This section contains information for verifying proper operation of the counter. Although these tests are not comprehensive, they do insure, to a high degree of confidence, that the instrument is operating properly. They can be useful for incoming inspection and should be performed after any servicing to insure proper operation of the counter. All tests can be performed without removing the instrument panels. A test report form is included which may be used as a test record. If the application is especially critical in nature, more extensive testing may be necessary; this is covered in the performance verification test section of the service manual.

Because of the high cost and specialized nature of frequency sources above 40 GHz, testing above 40 GHz is not covered. Also, for the purpose of operational verification tests, simulated pulsed signals will be used in Bands 1 and 3.

EQUIPMENT REQUIREMENTS

Test equipment required for the operational verification tests is listed in Table 4-1. The critical parameters are the minimum specifications required for the verification tests, and are included to assist in the selection of alternative equipment. Satisfactory performance of alternative items should be verified prior to use. All applicable test equipment must bear evidence of current calibration. For many of the following tests, an EIP 578B counter is used to source lock the microwave sweeper, thus providing a stable source for testing. This combination may be replaced with a frequency synthesizer.

Table 4-1. Equipment Requirements.

Description	Critical Parameters	Manufacturer	Model
Frequency synthesizer	100 Hz to 10 MHz	Hewlett Packard	3325A
Sweep generator	10 MHz to 40 GHz	Wiltron	6668B
Sweep generator	3 GHz to 18 GHz	Wiltron	6635B
Source locking counter	10 MHz to 26.5 GHz	EIP	578B
Spectrum analyzer	3 GHz to 18 GHz	Hewlett Packard	8566B

Description	Critical Parameters	Manufacturer	Model
Power meter	10 MHz to 60 GHz	Hewlett Packard	437B
Power sensor	10 MHz to 18 GHz (-20 to +10 dBm)	Hewlett Packard	8481A
Power sensor	50 MHz to 26.5 GHz (-20 to +10 dBm)	Hewlett Packard	8485A
Power sensor	26.5 GHz to 40 GHz (-20 to +10 dBm)	Hewlett Packard	R8486A
Oscilloscope	DC to 10 MHz	Tektronix	475
Power splitter	10 MHz to 26.5 GHz	Hewlett Packard	11667B
Directional coupler	950 MHz to 18 GHz	Narda	4226-10
Directional coupler	18 GHz to 26.5 GHz	Narda	4017C-10
Pulse generator	1 MHz	Wavetek	801
Pulse modulator	1 GHz to 2 GHz	Hewlett Packard	8731B
Pulse modulator	2 GHz to 18 GHz	Hewlett Packard	11720A
Pulse modulator	18 GHz to 26.5 GHz	Narda	S214DS
Remote sensor	26.5 GHz to 40 GHz	EIP	091
Coaxial to waveguide adapter	—	Wiltron	35WR42K
50 Ω termination	—	Pomona	4119-50
3-dB pads (2)	—	—	—

SOURCE LOCKING SETUP

DESCRIPTION

In some of the following tests, an EIP 578B counter is used to source lock the sweep generator to provide a stable frequency source for testing the EIP 1230A and 1231A counters.

The source locking setup described below is not limited to locking the Wiltron sweeper. It can be used to source lock almost any electronically tunable signal source over a frequency range from 10 MHz to 110 GHz. For more information on source locking the Wiltron 6600 series of sweep generators, request Application Bulletin 10 from the EIP sales representative in your area, or directly from EIP.

Regardless of the particular sweeper used, the procedure for source locking is basically the same. A sample of the output from the sweeper is applied to the appropriate band on the EIP 578B counter. For the setup shown in Figure 4-1, a power splitter provides the sample. The COURSE TUNE OUTPUT of the EIP 578B counter is connected to the external sweep input of the sweeper. The LOCK OUTPUT of the EIP 578B counter is connected to the FM input of the sweeper. The FM modulation on the sweeper is enabled, and the sweeper is set to the external sweep mode.

EQUIPMENT REQUIRED

Source locking counter (EIP 578B)
Sweep generator (Wiltron 6668B)
Power splitter (Hewlett Packard HP11667B)

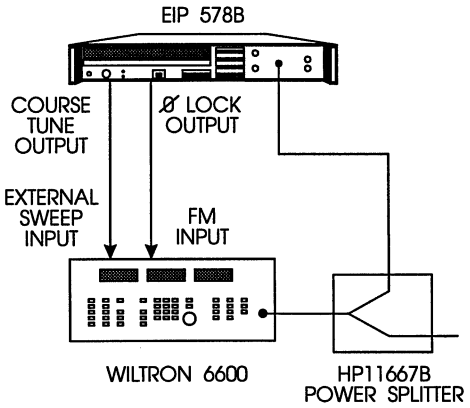


Figure 4-1. Source Locking Setup.

With the equipment setup described above, source locking over the entire range of the sweeper can be achieved by simply entering the desired frequency on the EIP 578B.

For example, to lock the sweeper at 10 GHz, set the source locking counter as follows:

PRESS: LOCK FREQ [ ] [1] [2] GHz [ ]

At this point, the sweeper should be locked to 10 GHz, the LCK annunciator on the counter should be lit, and 10 GHz should be displayed.

In the following tests, the output frequency from the sweeper is controlled directly by the EIP 578B counter, while the power is controlled at the sweeper.

OPERATIONAL VERIFICATION TEST PROCEDURES

BAND 0 FREQUENCY RANGE AND SENSITIVITY TEST (CW ONLY)

Description

This test verifies counter operation from 100 Hz to 250 MHz at -15 dBm (0.1125 V p-p into 50 Ω). The oscilloscope will be used to set up signal levels below 10 MHz. The power meter will be used to set signal levels at 10 MHz and above. Setup 1 will be used to test the counter from 100 Hz to 10 MHz and Setup 2 will be used to test the counter from 10 MHz to 250 MHz.

Equipment

Frequency synthesizer (Hewlett Packard 3325A)
Sweep generator (Wiltron 6668B)
Source locking counter (EIP 578B)
Power meter (Hewlett Packard 437B)
Power sensor (Hewlett Packard 8481A)
Power splitter (Hewlett Packard 11687B)
Oscilloscope (Tektronix 475)
50 Ω termination (Pomona 4119-50)

Setup 1

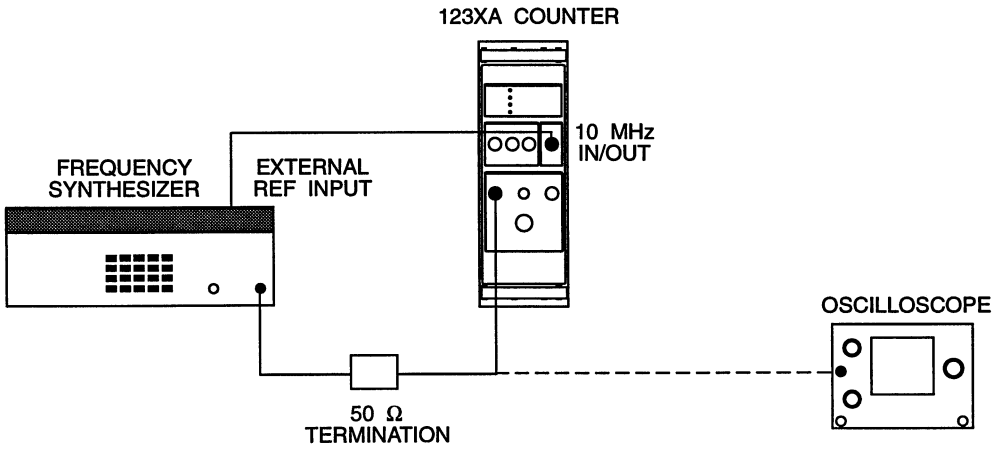


Figure 4-2. Band 0 Test Setup (100 Hz to 10 MHz).

Procedure

1. Connect equipment as shown in Figure 4-2.
2. Set the counter to Band 0 and select resolution 2.
3. Set the output frequency of the synthesizer to 100 Hz.
4. Using the oscilloscope, set the output signal level from the synthesizer to -15 dBm (0.11 V p-p into 50 Ω).
5. Apply 100 Hz signal to the counter, verify proper reading, and record results.
6. Repeat steps 3, 4, and 5 at 1 kHz, 10 kHz, 100 kHz, 1 MHz, and 10 MHz.

Setup 2

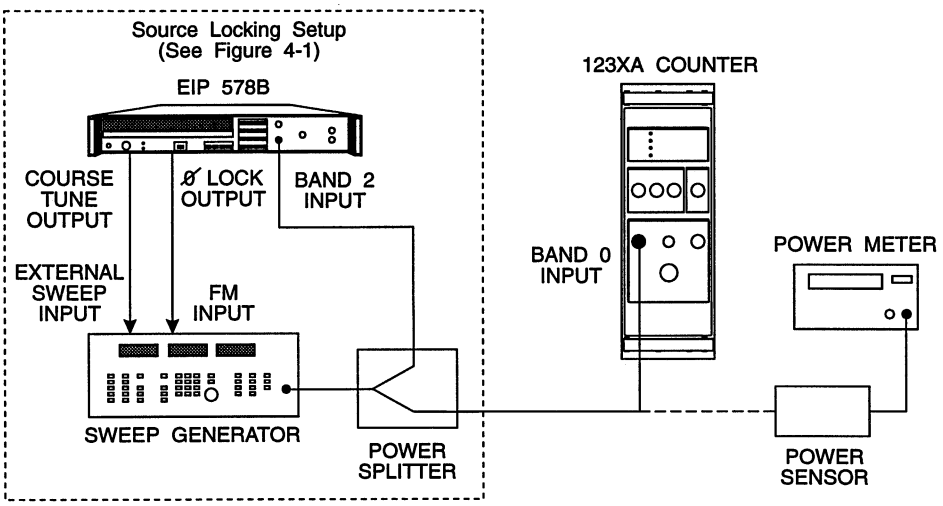


Figure 4-3. Band 0 Test Setup (10 MHz to 250 MHz).

Procedure

1. Connect equipment as shown in Figure 4-3.
2. Set the counter to Band 0 and select resolution 3.
3. Using the EIP 578B, source lock the sweeper at 100 MHz.
4. Using the power meter, set the output signal level from the sweeper to -15 dBm.
5. Apply the signal to the counter under test, verify proper reading and record the results.
6. Repeat steps 3, 4, and 5 at 200 MHz and 250 MHz.

BAND 1 FREQUENCY RANGE AND SENSITIVITY TEST

Description

This test verifies counter operation from 250 MHz to 1 GHz at -15 dBm for both CW and simulated pulsed signals. The pulse generator will be used to simulate a pulsed signal. This is accomplished by applying a 50 ns ECL low, with a 1 MHz repetition rate to the INHIBIT IN connector on the front panel of the counter. The power meter will be used to set signal levels.

Equipment

Sweep generator (Wiltron 6668B)
Source locking counter (EIP 578B)
Power meter (Hewlett Packard 437B)
Power sensor (Hewlett Packard 8481A)
Pulse generator (Wavetek 801)
Power splitter (Hewlett Packard 11667B)
Oscilloscope (Tektronix 475)
50 Ω termination (Pomona 4119-50)

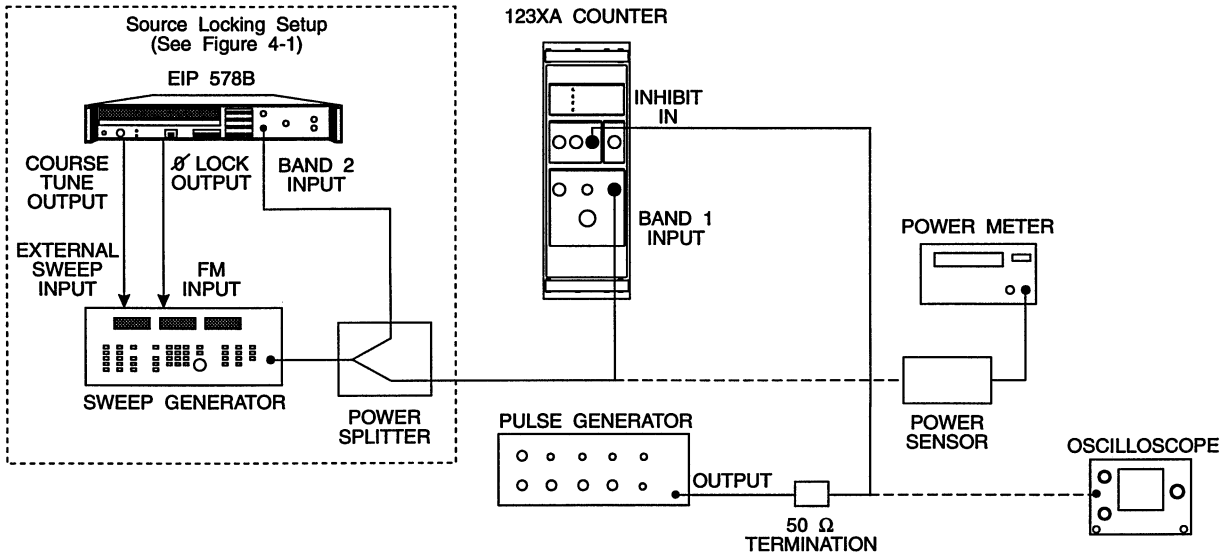


Figure 4-4. Band 1 Frequency Range and Sensitivity Test Setup.

Procedure

1. Connect equipment as shown in Figure 4-4.
2. Set the counter to Band 1 and select resolution 3.
3. Using the 578B, source lock the sweeper at 250 MHz.
4. Using the power meter, set the output signal level from the sweeper to -15 dBm.
5. Apply the signal to the counter, verify proper reading and record the results.
6. Repeat steps 3, 4, and 5 at 300 MHz, 400 MHz, 500 MHz, 600 MHz, 700 MHz, 800 MHz, 900 MHz, and 1 GHz.
7. Using the oscilloscope, set up the pulse generator to output a 50 ns wide ECL low signal with a 1 MHz repetition rate and apply the signal to the INHIBIT IN connector on the front panel of the counter. This signal gates signal threshold inside the counter and is used to simulate a pulsed signal.
8. Repeat steps 3, 4, 5, and 6 for the simulated pulsed signal and record the results.

BAND 2 FREQUENCY RANGE AND SENSITIVITY TEST

Description

This test verifies counter operation from 950 MHz to 20 GHz (26.5 GHz for 1230A). The first part of the test verifies operation in the CW mode. Next, the counter is tested in the pulse mode using the pulse modulators to modulate the microwave source. Attenuators are necessary on the input and output from the pulse modulators to reduce frequency pulling of the microwave source. To be able to accurately set the power level of the pulsed signal, it is necessary to compensate for the insertion loss of the pulse modulators. This is accomplished by applying a constant enable signal to the pulse modulator and adjusting the sweeper, at each test frequency, until the output power from the modulator is at the required level.

Equipment

Sweep generator (Wiltron 6668B)
Source locking counter (EIP 578B)
Power meter (Hewlett Packard 437B)
Power sensor (Hewlett Packard 8485A)
Pulse generator (Wavetek 801)
Pulse modulator (Hewlett Packard 8731B)
Pulse modulator (Hewlett Packard 11720A)
Pulse modulator (Narda S214DS)
Power splitter (Hewlett Packard 11667B)
Oscilloscope (Tektronix 475)
50 Ω termination (Pomona 4119-50)
3 dB pads (2)

Setup 1

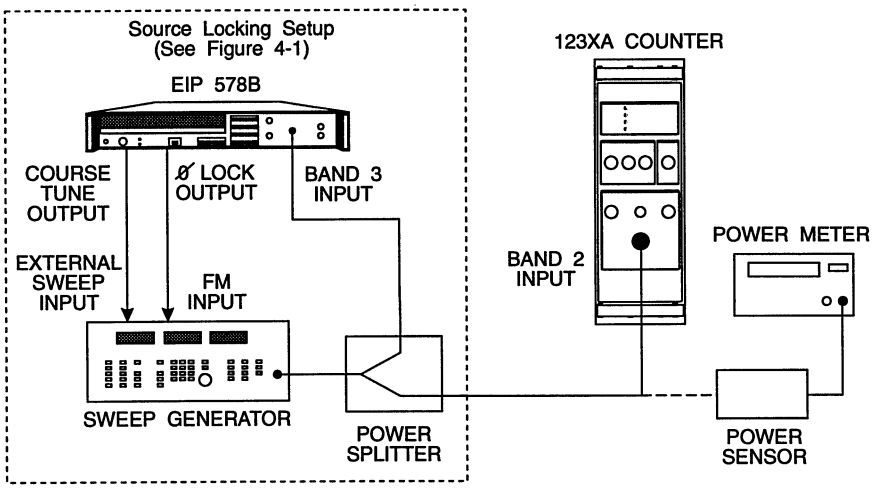


Figure 4-5. Band 2 Frequency Range and Sensitivity Test Setup (CW Mode).

Procedure

1. Connect equipment as shown in Figure 4-5.
2. Set the counter to Band 2 and select resolution 3.
3. Using the 578B, source lock the sweeper at 950 MHz.
4. Using the power meter, set the output signal level from the sweeper to -20 dBm.
5. Apply the signal to the counter, verify proper reading, and record the results.
6. Repeat steps 3, 4, and 5 at 1 GHz, 3 GHz, 6 GHz, 10 GHz, 12.4 GHz, 15 GHz, 18 GHz, and 20 GHz. For EIP 1230A counters, also test at 22 GHz, 24 GHz, and 26.5 GHz at a power level of -10 dBm. Record the results.

Setup 2

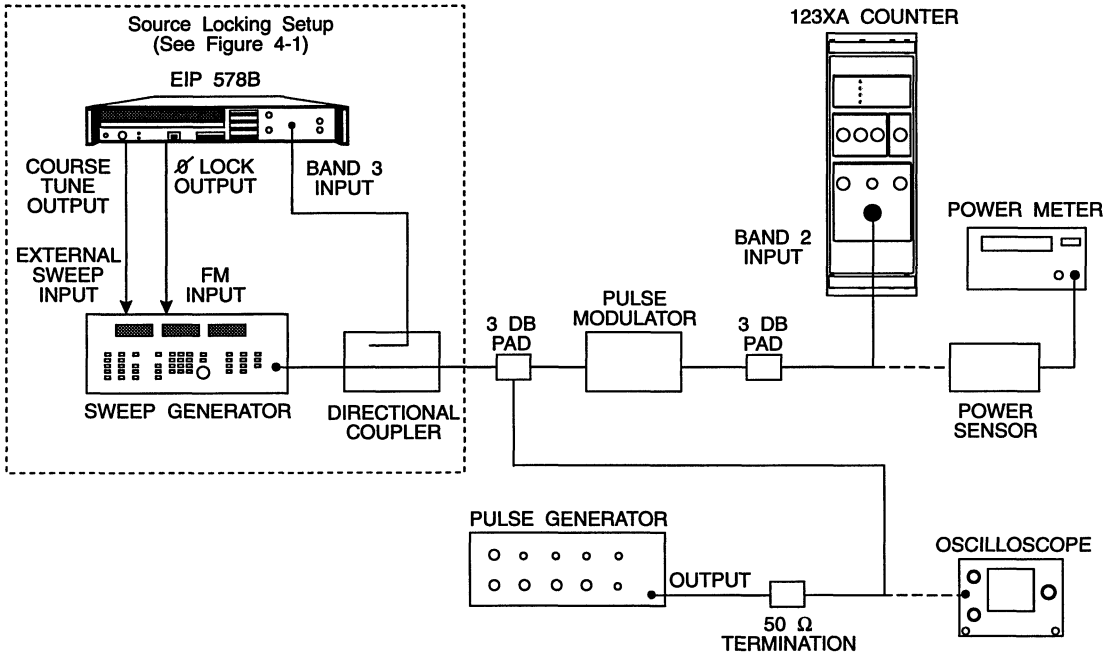


Figure 4-6. Band 2 Frequency Range and Sensitivity Test Setup (Pulse Mode).

Procedure

For this test, three pulse modulators and two directional couplers are used. Use the appropriate device corresponding to the frequency. Refer to Table 4-1 for a listing of frequency ranges of the pulse modulators and directional couplers.

1. Connect equipment as shown in Figure 4-6.
2. Set the counter to Band 2 and select resolution 3.
3. Set up the pulse generator to output a 100 ns wide TTL signal with a 1 MHz repetition rate. This signal will be used to drive the pulse modulators.
4. Using the 578B, source lock the sweeper at 950 MHz.
5. Apply a constant enable signal to the pulse modulator. Adjust the output power on the sweep generator until the power meter indicates the specified sensitivity level for the counter.
6. Apply the modulation drive to the appropriate pulse modulator and connect the pulse modulated signal to the counter.
7. Verify that the counter counts the pulsed signal properly and record the results.
8. Repeat steps 4, 5, 6, and 7 at 1 GHz, 3 GHz, 6 GHz, 10 GHz, 12.4 GHz, 15 GHz, 18 GHz and 20 GHz. For EIP 1230A counters, change the pulse width from the modulator to 500 ns and test at 22 GHz, 24 GHz, and 26.5 GHz.

BAND 3-1 FREQUENCY RANGE AND SENSITIVITY TEST (EIP 1230A with Option 002 Only)

Description

This test verifies counter operation from 26.5 GHz to 40 GHz at -20 dBm for both CW and simulated pulsed signals. The pulse generator will be used to simulate a pulsed signal. This is accomplished by applying a 50 ns ECL low, with a 1 MHz repetition rate to the INHIBIT IN connector on the front panel of the counter. The power meter will be used to set signal levels.

Equipment

Sweep generator (Wiltron 6668B)
Power meter (Hewlett Packard 437B)
Power sensor (Hewlett Packard R8486A)
Pulse generator (Wavetek 801)
Oscilloscope (Tektronix 475)
50 Ω termination (Pomona 4119-50)
Remote sensor (EIP 091)
Coaxial to waveguide adapter (Wiltron 35WR42K)

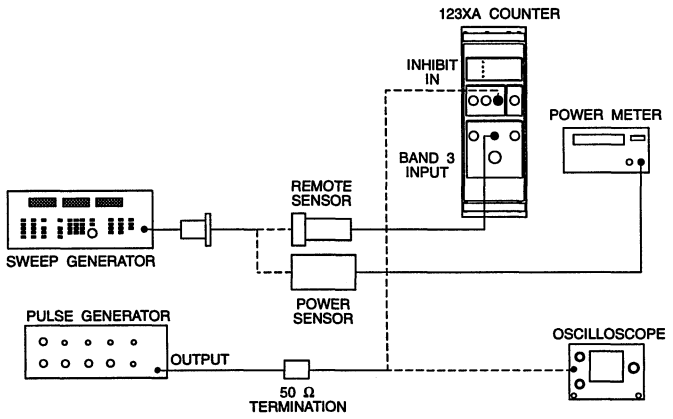


Figure 4-7. Band 3-1 Frequency Range and Sensitivity Test Setup.

Procedure

1. Connect equipment as shown in Figure 4-7.
2. Set the counter to Band 3-1 and select resolution 3.
3. Set the output frequency from the sweeper at 26.5 GHz.
4. Using the power meter, set the output signal level from the sweeper to -20 dBm.
5. Apply the signal to the remote sensor, verify proper reading, and record the results.
6. Repeat steps 3, 4, and 5 at 30 GHz, 35 GHz, and 40 GHz.
7. Set up the pulse generator to output a 50 ns wide ECL low signal with a 1 MHz repetition rate and apply the signal to the INHIBIT IN connector on the front panel of the counter. This signal gates signal threshold inside the counter and is used to simulate a pulsed signal.
8. Repeat steps 3, 4, 5, and 6 for the simulated pulsed signal and record the results.

BAND 2 AMPLITUDE DISCRIMINATION TEST

Description

This test verifies that the counter will measure accurately the larger of two signals differing in amplitude by 15 dB or more.

Equipment

Sweep generator (Wiltron 6668B)
Sweep generator (Wiltron 6635B)
Spectrum analyzer (Hewlett Packard 8566B)
Power splitter (Hewlett Packard 11667B)

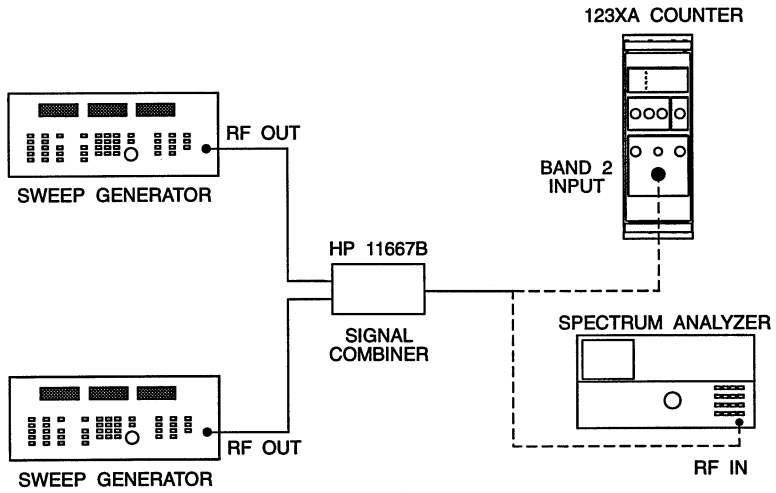


Figure 4-8. Band 2 Amplitude Discrimination Test Setup.

Procedure

1. Connect equipment as shown in Figure 4-8.
2. Set first signal generator to 3.000 GHz at 0 dBm and second signal generator to 3.2 GHz at +6 dBm.
3. Using the spectrum analyzer, adjust the power level so that the power level difference between the two signals is 15 dB.
4. Verify that the counter correctly measures the frequency from the higher power signal source.
5. Repeat steps 2, 3, and 4 at 6 and 6.2 GHz, at 12 and 12.2 GHz, and at 17.8 and 18 GHz.

OPERATIONAL TEST RECORD

MODEL _____ SERIAL NO._____ DATE _____

BAND 0 FREQUENCY RANGE AND SENSITIVITY TEST
(100 Hz TO 250 MHz CW ONLY)

INPUT	CW READINGS	INPUT	CW READINGS	SPECIFICATIONS
100 Hz	_____	10 MHz	_____	-15 dBm
1 kHz	_____	100 MHz	_____	
10 kHz	_____	200 MHz	_____	
100 kHz	_____	250 MHz	_____	
1 MHz	_____			

BAND 1 FREQUENCY RANGE AND SENSITIVITY TEST
(250 MHz TO 1 GHz)

INPUT	CW READINGS	PULSE READINGS	INPUT	CW READINGS	PULSE READINGS	SPECIFICATIONS
250 MHz	_____	_____	700 MHz	_____	_____	-15 dBm
300 MHz	_____	_____	800 MHz	_____	_____	
400 MHz	_____	_____	900 MHz	_____	_____	
500 MHz	_____	_____	1 GHz	_____	_____	
600 MHz	_____	_____				

BAND 2 FREQUENCY RANGE AND SENSITIVITY TEST
(950 MHz TO 20 GHz/26.5 GHz)

INPUT	CW READINGS	PULSE READINGS	INPUT	CW READINGS	PULSE READINGS	SPECIFICATIONS
950 MHz	_____	_____	12.4 GHz	_____	_____	-15 dBm
1 GHz	_____	_____	15 GHz	_____	_____	
3 GHz	_____	_____	18 GHz	_____	_____	
6 GHz	_____	_____	20 GHz	_____	_____	
10 GHz	_____	_____				
		1230A ONLY	22 GHz	_____	_____	-10 dBm
			24 GHz	_____	_____	
			26.5 GHz	_____	_____	

BAND 3-1 FREQUENCY RANGE AND SENSITIVITY TEST
(26.5 GHz TO 40 GHz)
1230A WITH OPTION 002 ONLY

INPUT	CW READINGS	PULSE READINGS	INPUT	CW READINGS	PULSE READINGS	SPECIFICATIONS
26.5 GHz	_____	_____	35 GHz	_____	_____	-20 dBm
30 GHz	_____	_____	40 GHz	_____	_____	

BAND 2 AMPLITUDE DISCRIMINATION TEST
(CONDITIONS: F1 > F2 BY 15 dB OR MORE)

F1	F2	PASS	FAIL	SPECIFICATIONS
3 GHz	3.2 GHz	_____	_____	15 dBm
6 GHz	6.2 GHz	_____	_____	
12 GHz	12.2 GHz	_____	_____	
17.8 GHz	18 GHz	_____	_____	

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APPENDIX A
VXIbus OVERVIEW

This VXIbus overview is from the VXIbus Specification, revision 1.3.

INTRODUCTION

The goal of the VXIbus is to define a technically sound modular instrument standard based on the VMEbus that is open to all manufacturers and is compatible with present industry standards.

VXIbus is an acronym for VMEbus extensions for Instrumentation. The VXIbus specification details the technical requirements of VXIbus compatible components, such as mainframes, backplanes, power supplies, and modules. Before studying the VXIbus architecture, one should become familiar with the VMEbus and its specifications.

VMEbus BACKGROUND

The VMEbus is an open system architecture primarily focused at computer systems, though there presently is a limited offering of instrumentation. VMEbus modules are approximately six inches deep and come in two heights, about four and nine inches. The VXIbus specification refers to these as the A and B sizes, respectively. The precise dimensions are specified by the Eurocard standard, which describes a family of printed circuit boards and their associated DIN connector locations. VMEbus modules are designed for 0.8 inch slot to slot spacing. The A size board has a single 96 pin connector known as P1, while the B size may include a P1 and P2 connector. Each of these DIN connectors consists of three rows of 32 pins apiece on 0.1 inch centers. Typically, these boards are positioned vertically in a frame with the P1 connector closest to the top. Neither the VMEbus nor the VXIbus mandates a physical orientation, since orientation is only an implementation issue not needed for compatibility. Many VMEbus systems are designed to accept boards horizontally.

The VMEbus specification allows a maximum of 21 modules. However, if installed vertically in a mainframe intended for mounting in a standard 19 inch rack, 20 is the practical maximum. VMEbus makes no particular provision for an extension chassis or frame to frame communication. Multiple frame systems can be created by electrically buffering the VMEbus (at the loss of some bandwidth between cages) or by using standard data communication links that disguise the underlying VMEbus architecture. There are no EMC (electromagnetic compatibility) requirements dictated by VMEbus, either conducted or radiated, nor are there power dissipation limits or chassis cooling requirements. VMEbus has left these issues to the system integrator, while VXIbus addresses these issues more rigorously.

Although electrically and logically similar to the 68000 microprocessor architecture, the VMEbus interface has been specified broadly enough that it is not dependent on any particular processor, and many processors are already supported on VMEbus, including the 80386. Many of the simpler VMEbus boards do not have processors at all.

A minimum VMEbus system requires only the P1 connector. All handshaking, arbitration, and interrupt support exists on P1, with P2 used to expand the system to 32 bits of address and data (A32 and D32). P1 will support 16 bit and 24 bit addressing (A16 and A24), as well as 8 and 16 bit data paths (D08 and D16). The extra lines needed for A32 and D32 are contained on the center row of P2, while the outer rows are user defined. These undefined pins are typically used for interface connections, such as allowing a module to drive a chassis mounted connector, access an internal disk drive, or provide for module to module communication. VSB (VMEbus Subsystem Bus) is a standard "subsystem bus" that has defined P2 as an additional communication path for up to six modules. Multiple VSBs may exist within any one VMEbus system. This is important to note, because VXIbus defines a subsystem of up to 13 modules and, like VSB, multiple VXIbus subsystems may exist within any one VXIbus system.

THE VXIbus EXTENSIONS

VXIbus retains P1 and the center row of P2 exactly as defined by VMEbus. This includes the 5 volt and ±12 volt power pins on P1, and the additional 5 volt pins on P2. VXIbus includes the A and B card sizes, and these modules remain totally VMEbus compatible. However, VXIbus has made substantial additions to the VMEbus specification oriented towards instrumentation that can best be described as an electromechanical superset and a logical subset.

VXIbus Modules

VXIbus has added two Eurocard module sizes of about 13 inch depth referred to as the C and D sizes. These modules are 9 and 14 inches high respectively, and are placed on 1.2 inch centers. The C Eurocard is the same height as the VMEbus B size board, and may sport both the P1 and P2 connectors. The D size module is a triple high Eurocard that may include a P3 connector in addition to P1 and P2. The 1.2 inch module width allows feasible implementation of high density instrumentation modules while allowing enough space for shielding both sides of a module and inserting an optional chassis shield. It also has the added benefit of allowing a high degree of compatibility with the shorter and narrower A and B sizes by allowing them to be mounted on full length board carriers or adapters. These carriers/adapters may also shield the sides of standard VMEbus cards, giving them a high degree of electromagnetic compatibility with VXIbus systems.

VXIbus Subsystems

A VXIbus system may have up to 256 devices, including one or more VXIbus subsystems. A VXIbus subsystem consists of a central timing module referred to as Slot 0 with up to 12 additional instrument modules. P2 and P3 are completely defined in a VXIbus subsystem. These 13 modules conveniently fill a standard 19 inch cabinet when mounted vertically on 1.2 inch centers. Many VXIbus systems will consist only of a single frame with these 13 modules. A common configuration will load the Slot 0 module with system resources such as the VXIbus mandated timing generation, the VMEbus required system controller functions, and a data communication port such as IEEE 488 or RS-232. Slot 0 may also include optional instrumentation. The other positions are general purpose slots for the user to mix and match modules. A single VXIbus subsystem may have less than 12 additional slots, but may not have more. Any combination of VXIbus subsystems may exist within a VXIbus system. For instance, one VXIbus system may consist of a frame with one Slot 0 and 12 VXIbus modules extended to another frame that has a Slot 0 adjacent to three instrument slots, another Slot 0 with five instrument slots, and four standard VMEbus slots of undefined P2.

P2 CONNECTOR DEFINITION

As mentioned previously, a VXIbus subsystem defines all P2 and P3 pins. The VXIbus P2 adds a 10 MHz ECL clock, ECL and analog supply voltages, ECL and TTL trigger lines, an analog summing bus, a module identification line, and a daisy chain structure known as the local bus. The trigger lines serve primarily as resources for signaling between instruments in a VXIbus subsystem, while the local bus lines are preferred for use within a multiple module instrument set (adjacent slots). The daisy chain local bus use is left to the module manufacturer to define, and several classes of electrical signals are permitted. Allowed signals are TTL, ECL, low voltage analog, and analog up to 42 volts. A keying mechanism near the faceplate indicating that module's local bus class prevents incompatible classes from accidentally being placed adjacently and potentially causing a destructive condition. Typical uses of the local bus include creating an internal analog bus or a chain of serial digital signal processors. There are a total of 24 local bus pins on P2, 12 lines in and 12 lines out for each slot; thus creating a 12 line bus that may or may not be passed on to adjacent slots.

P3 CONNECTOR DEFINITION

The VXIbus P3 connector adds many of the same resource types as described for P2, but is aimed at higher performance instrumentation. Included on P3 is a 100 MHz clock and sync signal, additional power pins of the same supply voltages, more ECL trigger lines, and 24 additional lines (48 pins) of daisy chain local bus. Also defined on P3 is a "star" trigger system where precision ECL trigger signals are routed through Slot 0 acting as a cross point switch. This allows very precisely matched trigger timing between modules regardless of module position.

VXIbus System Architecture

The VXIbus device protocols define how modules are granted non-conflicting portions of the VMEbus address space. A device is typically a single module, but this is not required. Several devices may exist on a single module, and a single device may consist of multiple modules. 256 devices may exist in any one VXIbus system, and are referred to by logical device address ranging from 0 to 255. A VXIbus system configuration space is defined in the upper 16K of the 64K A16 address space. Each device is granted a total of 64 bytes in this space, which is sufficient for many of the simpler devices. Devices requiring additional address space have their address requirements readable in a defined register in the A16 address space. A "resource manager" reads this value shortly after power-on, and then assigns the requested memory space by writing the module's new VMEbus address into the device's offset register. This method positions a device's additional memory space in the A24 (16 Mbyte) or A32 (4 Gbyte) address space. If present day VMEbus cards are used in a system, the resource manager must position the VXIbus devices around the space taken by the standard VMEbus cards.

Higher level communication protocols are defined to allow sharing of interface modules and other devices by multiple manufacturers.

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