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Find the *Philips 4400–VF10* at our website: *Click HERE*

4400 - VF10



4400 – VF10
PCM Bit Synchronizer

Features

- Supports input PCM Data rates up to 10 Mbps
- K^2 Filter & Filter Sample Detection Modes
- All PCM Codes Including DM, Miller^2, & RNRZ
- Three Software Selectable Input Sources
- Selectable Loop Bandwidth from (0.1% to 1.5%)
- Options
  Bi-polar Tape Driver Output
  Conventional Encoder/Viterbi Decoder, Soft Bit Decision Output

Phillips Aerospace
16125 East Gale Ave.
Industry Ca 91745
www.paero.com • info@paero.com
(626) 855-4600

Summary

4400-VF10 is a tunable, high performance PCM bit synchronizer module. The bit synchronizer supports input data rates up to 10 Mbps. Phillips Designed the 4400-VF10 to operate in a stand-alone mode or as a daughter card for 4422 Series Decommutators. In spite of its small size, the Mode 4400-VF10's performance can rival most stand-alone bit synchronizer.

With Phillips' exclusive K^2 Filter-Sample detection modes, users can optimize bit synchronizer performance. The 4400-VF10 features an implementation loss that is typically less than 1bB from the theoretical Bit Error Performance Curve.

The bit synchronizer offers several user-selectable features. These features include input source, input PMC data rate, loop bandwidth and derandomizer (on/off).

The 4400-VF10 has the following advanced options available: bi-polar tape driver output, 3-bit soft decision output and Convolutional Encode/Viterbi Decoder.

You program the 4400-VF10 Bit Synchronizer via the VMEbus. Bit synchronizer readback (status) is available on the same bus. LED indicator located on the module's front panel indicate signal presence and bit sync lock.

Specifications

Performance:

Input data rate:	250 bps to 10.0 Mbps (NRZ codes) 250 bps to 5.0 Mbps (all other codes)
Input PCM code:	NRZ-L/M/S BIØ-L/M/S DM-M/S M2 RZ RNRZ-L (211-1 & 215-1)

Inputs:

Input signal amplitude:	0.4 V 10 V (peak-to-peak
Input signal offset:	Two times the peak-to-peak value (within 20 V window)
Input signal impedance:	75 ohms (or 50ohms) or 10 kohms (selectable)
Loop bandwidth:	0.1% to 1.5% of bit rate (selectable)
Bit Error Probability:	Within 1dB from theoretical BER curve (NRZ-L & BIØ-L typically 0.5 dB)

Outputs-(buffered TTL & RS-422):

Data:	NRZ-L & BIØ-L Clock 0° & 90°
Programming:	Via the VME bus including Input source, bit rate, PMC Code, loop bandwidth, detection method, derandomizer & output PCM Code

Specifications Continued

Soft Readback:
Via the VME bus including:
Signal resence, loop stress, bit sync lock, bit rate setting, PMC Code setting, loop bandwidth setting
Status indicators: Signal Present , Bit Sync Lock Status, Self Test, & Viterbi Decoder (sync)
Conventional Encoder/Vierbi Decoder (Optional):

Input symbol rate:	Up to 10 Mbps (RNZ Codes) Up to 5 Mbps (all other PCM Codes)
FEC:	Rate ½ & 1/3, constraint length (K)=7
Soft decision input:	Sign magnitude or offset binary
Coding gain:	5.2 dB (R=1/2) & 5.5 dB (R=1/3) @ 10-5 (BER)
Scrambling/Descrambling:	V.35 (CCITT or Intelsat Version)
Data Modes:	Serial (BPSK, FWD or Rev, Parallel (OPSK or QPSK), Differential (ENC/DEC), Invert G1 weighted bits (alternate symbol inversion
Inputs:	Encoder (data & clock), Q (soft bits) & External (soft bits) Outputs Soft bit, FEC sync, symbol error clock, encoder clock, encoder (I & O) and decoder (data & clock)

Mechanical:

Dimensions:	9.187”H x 6.299”W
Form Factor:	Single, 6U VME module
Connectors:	VMEbus (P1 & P2) plus D-Shell & BNCs at top plate
Manufacturing:	Hybrid of standard components & Surface Mount Technology (SMT)

Environmental:

Operating:	Temperature: 0° to 50°C Humidity: 0 to 90% (non-condensing)
Non-operating:	(in proper packaging) Temperature: -25° to +70°C Humidity: Must prevent contact with moisture & contaminants
Special handling:	Standard ESD handling methods recommended

Ordering Information

Part Number: 4400–VF10

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