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PCI-X SYS Board

Reference Manual

Version 1.1 May 2004
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PCI-X SYS Board

Reference Manual

Change History

Date	Version Number	Change
May 2004	1.1	● Rewrite and update of content ● Update of formatting
May 2003	1.0	● First release

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Product Status

The information in this document is final content pertaining to the PLDA PCI-X SYS board.

Web Address

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Preface

The preface describes the contents of this document and suggests additional reading. It contains the following sections:

- About this document
- Additional Reading
- Feedback and contact information

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About this document

Intended audience

This document has been written for design managers, system engineers, and designers of ASICs and FPGAs who are evaluating or using the PLDA PCI-X SYS board. Prior knowledge of PCI and PCI-X is assumed.

Scope

This document provides the complete functional description of the PLDA PCI-X SYS board.

Using this manual

This document includes the following chapters:

Chapter 1: Introduction

Chapter one includes system requirements and a broad description of the board's purpose.

Chapter 2: Exploring the PCI-X SYS architecture

Chapter two includes photographs and a block diagram of the board, and a table describing each feature of the board.

Chapter 3: PCI-X SYS Resources

Chapter three describes each resource that connects with the PCI-X SYS board.

Chapter 4: PCI-X SYS CPLD Configuration

Chapter four describes how to configure programmable devices on the board.

Chapter 5: Getting Started with the PCI-X SYS board

Chapter five provides a brief description of the two reference designs that are included with the board.

Typographical conventions

italic	Highlights important notes or publications
bold	**Highlights interface elements.**
Times New Roman	Denotes text used in a code example.
COURIER NEW	DENOTES A SIGNAL.

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Additional Reading

This section lists additional resources from PLDA and third-parties.

PLDA periodically updates its documentation. Please contact PLDA at support@plda.com or check the Web site at http://www.plda.com for current versions.

PLDA publications

Please refer to the following documents for further information:

- PCI / PCI-X Core User's Guide
- Build History: The Build History lists changes made in each version of the PCI-X SYS board.

Other publications

Please refer to the following documents for further information:

- PCI Local Bus Specification, Rev. 2.1, June 11, 1995.
- PCI Specification, Rev. 2.2.
- PCI-X addendum V1.0a
- PCI System Architecture, 3rd edition, September 1995.
- PCI Hardware and Software architecture & design, 2nd edition, March 1995
- Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC, P1386.1/Draft 2.4 - January 12, 2001

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Feedback and contact information

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- the title of the document
- the page number to which your comments refer
- a description of your comments

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Chapter 1 Introduction

1.1 System Requirements

To install and use the PCI-X SYS board, you need:

- PLDA's **PCI-X SYS board**
- a **PC with a 66 MHz 3.3V bus**
- In order to program board features, you also need **Quartus® II** and one of the following:
  - **ByteBlaster™** and a **parallel port**
  - **MasterBlaster™** and a **USB 2.0 port**

1.2 Purpose of the board

The PCI-X SYS board provides a rapid and high-bandwidth prototyping platform for FPGA and ASIC designers. It can also be used in applications at the system-level for such tasks as digital signal processing (DSP), test & measurement, and data acquisition. It is based on FPGA technology, which is used as a single point of data acquisition and processing on the board.

All data goes through the Altera FPGA, allowing maximum speed for all application processes, such as:

- data acquisition
- multi channel processing
- PCI transfer of up to 64 bits / 66MHz
- PCI-X transfer up to 1 Gbytes (64bits / 133MHz).

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Chapter 2 Exploring the PCI-X SYS architecture

2.1 Introduction

Featuring a PCI-X bus and PLDA's 64-bit 133 MHz PCI-X Core, the PCI-X SYS can be mounted with any of four Stratix devices (see Section 3.1) and features two fully independent banks of 4M x 32-bit words of Double Data Rate (DDR) SDRAM.

Figure 1 is a photograph of the component side of the PCI-X SYS board (note that CameraLink component is not mounted in this picture).

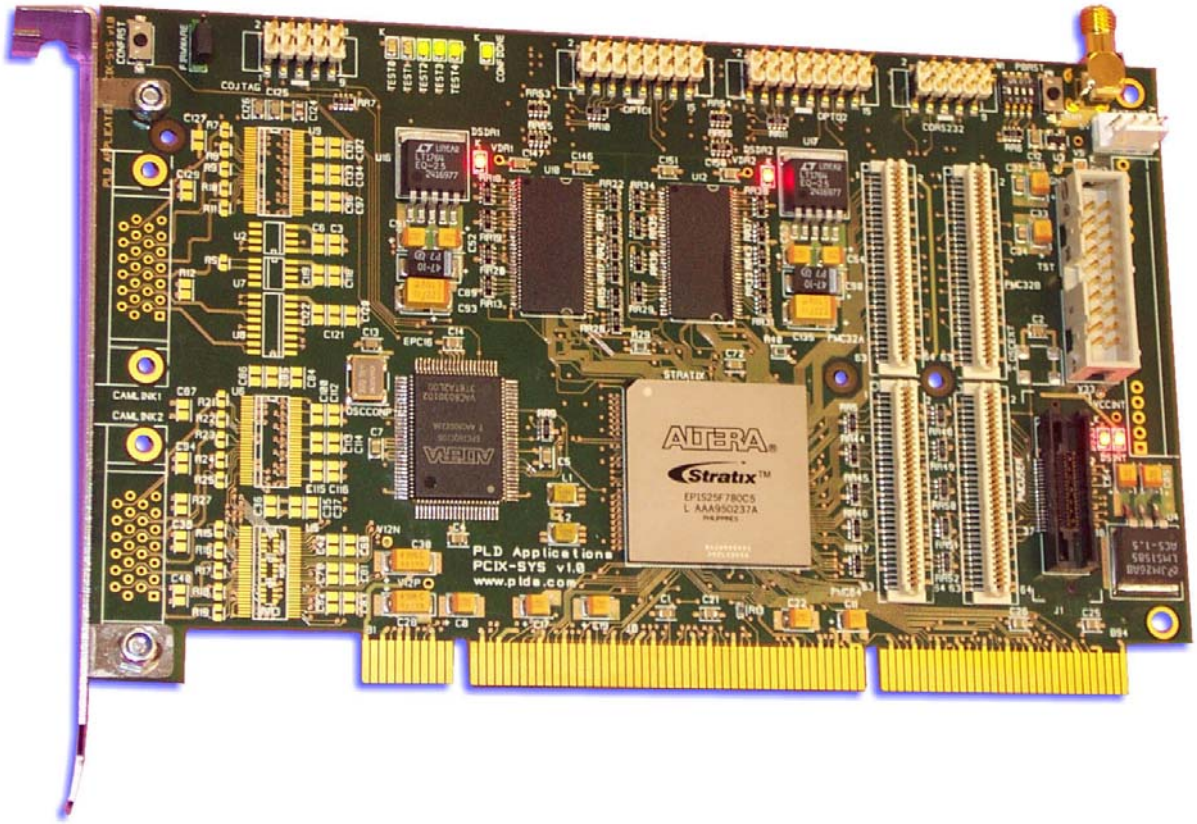


Figure 1: Photograph: PCI-X SYS board (component side)

Figure 2 shows the architecture of the component side of the PCI-X SYS board. Numbered components correspond to descriptions in Table 1.

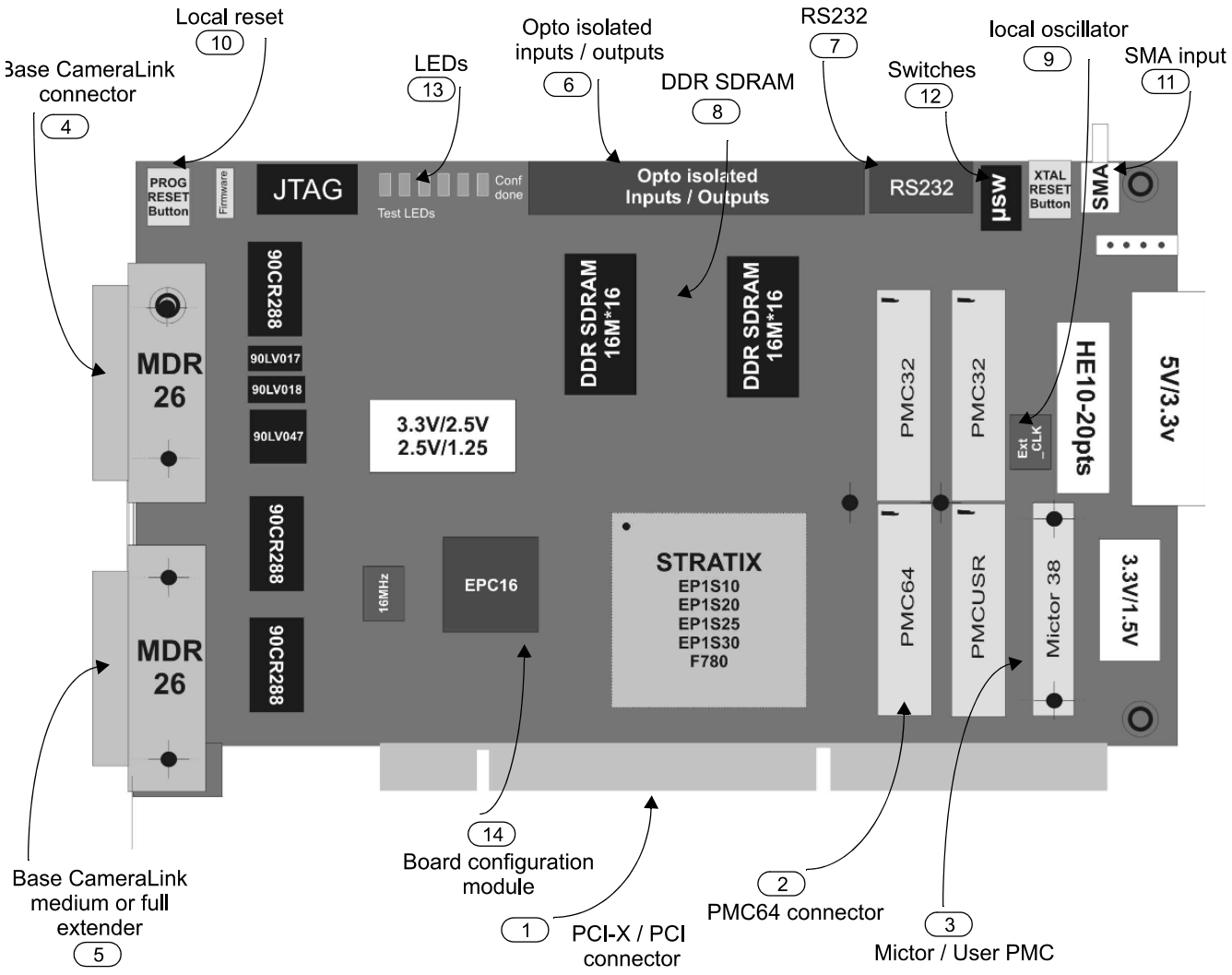


Figure 2: Block diagram: PCI-X SYS layout (component side)

Figure 3 shows the solder side of the PCI-X SYS board. Numbered components correspond to descriptions in Table 1.

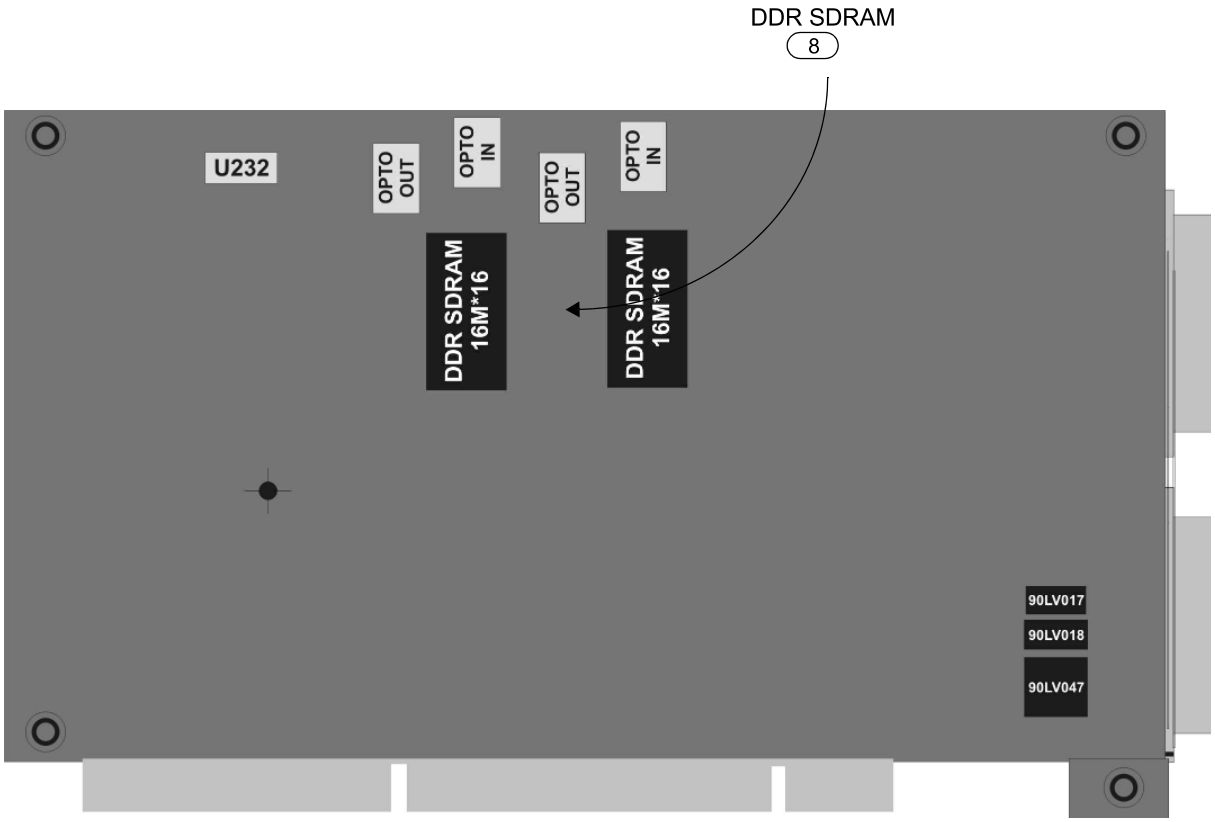


Figure 3: Block diagram: PCI-X SYS layout (solder side)

2.2 Block diagram of the PCI-X SYS

Numbered components in Figure 4 correspond to descriptions in Table 1.

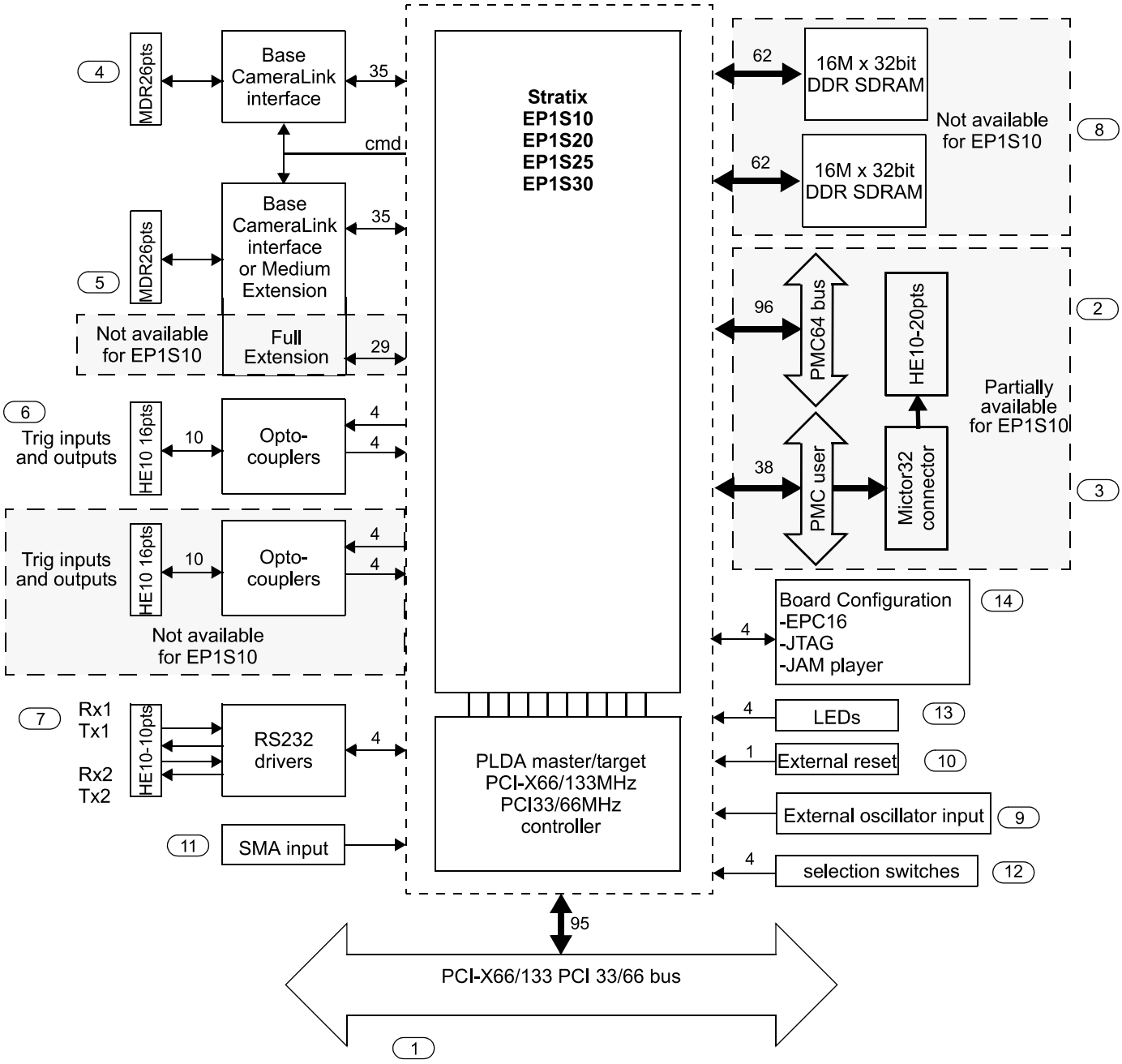


Figure 4: PCI-X SYS block diagram

2.3 Feature descriptions of the board

Table 1 describes PXI-X SYS board features. The feature number corresponds with the numbers in Figure 2,

Figure 3, and Figure 4.

Table 1: Features description

Feature number	Feature name	Signals	Description
1	PCI / PCI-X connector	95	The PCI-X SYS board is a 3.3V / 64-bit short form PCI card designed to be plugged into either a 32 / 64-bit, 33 / 66MHz PCI bus or into a PCI-X bus (up to 133MHz).
2	PMC64 connector	96	This 32 / 64-bit, 33 / 66-MHz PCI Mezzanine Card connector allows you to plug standard PMC or custom daughter cards into the board (96 I/Os available). Note that this feature is only partially available when the board is mounted with the EP1S10 component.
3	PMC / Mictor / 20-pin IDC header	38	You can use these connectors for a variety of purposes: ● Mictor 38-bit connector (AMP 2-767004-2): probing with an HP logic analyzer ● IDC header: probing and external connections ● PMC user Note that this feature is only partially available when the board is mounted with the EP1S10 component.
4	Base CameraLink 1	36	This interface permits you to connect components that have a CameraLink interface to the PCI / PCI-X bus.
5	Base CameraLink 2 / medium or full extension	64	This interface permits you to connect a second component that has a CameraLink interface to the PCI / PCI-X bus or to extend the first CameraLink interface to a medium or a full CameraLink interface. Note that this feature is not available when the board is mounted with the EP1S10 component.
6	Opto isolated inputs / outputs	16	8 opto-isolated inputs and 8 opto-isolated outputs. Note that only four inputs and four outputs are available when the board is mounted with the EP1S10 component.
7	RS232 channels (two)	4	The RS232 channels include two inputs and two outputs and allow: ● two simple serial links (Tx / Rx) ● one extended serial link (Tx / Rx / CTS / RTS)
8	DDR SDRAM (two)	124	The board supports two fully independent banks of 16M x 32-bit Words of DDR SDRAM. Note that this feature is not available when the board is mounted with the EP1S10 component.
9	Local oscillator	1	A local oscillator is available for custom applications.
10	Local reset	1	A local push button allows you to reset internal logic.
11	SMA input	1	The SMA connector can be used as a clock/trigger signal.
12	Microswitches (four)	4	Four micro switches are available (0 or 1 logic level).
13	LEDs (four)	4	Four LEDs can display system information, such as state machines and clock detection.

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Table 1: Features description

Feature number	Feature name	Signals	Description
(14)	Board configuration module	4	The Altera EPC16 is programmable via: ● a JTAG connector ● Jam Player: Allows you to configure the EPC16 or daughter card's CPLDs through the PCI / PCI-X bus and the JAM PCI software (no external cable needed). ● Two different configurations can be written on the EPC16.
(15)	Support for stand-alone operations		● 5V stand-alone power supply ● All resources are available in stand-alone mode ● External reset button for Stratix device reconfiguration ● External reset button for Stratix logic resources initialization ● Local oscillator (optional, please see Section 3.6.4 for details)

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Chapter 3 PCI-X SYS Resources

This section describes PCI-X SYS resources, which are all connected to the Stratix device.

3.1 Stratix device

The PCI-X SYS board supports four Stratix devices in the FPGA 780-pin package:

- EP1S10F780[1]
- EP1S20F780
- EP1S25F780
- EP1S30F780

C5-speed Stratix devices (for example, EP1S20F780C5) are required for maximum performance (133 MHz PCI-X and 400 MHz DDR SDRAM).

C6-speed Stratix devices can be used for PCI 66 MHz and 333 MHz DDR SDRAM environments.

The Stratix device is divided into eight I/O banks:

- Six banks are devoted to the PCI / PCI-X connector and are supplied with 3.3V.
- Two banks are used for DDR SDRAM (SSTL2) and are supplied with 2.5V (plus a 1.25V reference voltage; see Section 3.5 for more details).

1. The EP1S10 device permits most (but not all) functionality of the PCI-X SYS board.

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3.1.1 Block diagram of clock organization

Figure 5 illustrates clock signals on the board.

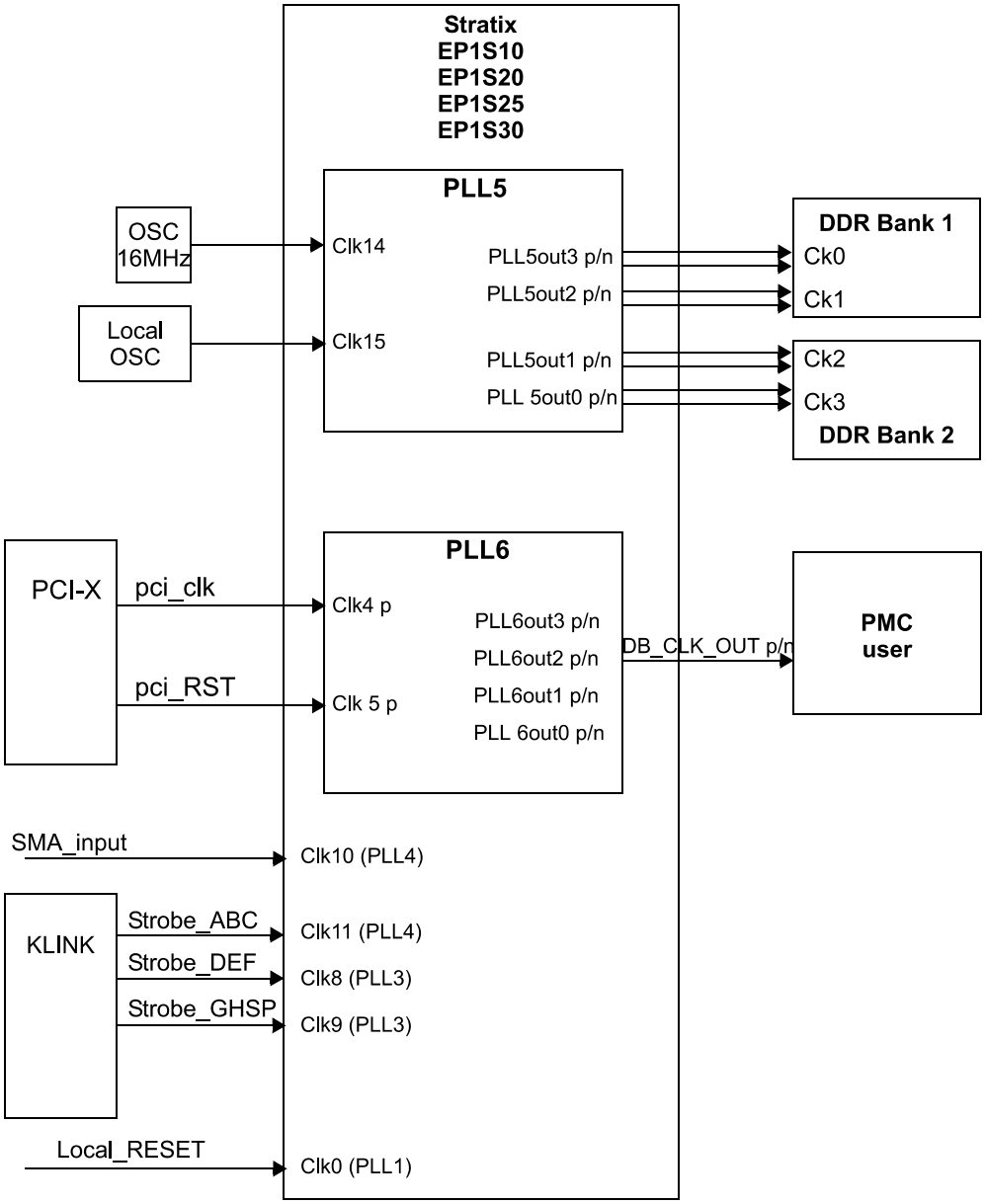


Figure 5: Clock organization

3.1.2 Signal / pin assignments for clock inputs, outputs, and I/Os

Table 2 and Table 3 describe PLL, CLK, and pin assignments for the Stratix device. Note that “p” (positive) and “n” (negative) imply that a particular signal can be used as a differential signal.

Table 2: Signal / pin assignments for Clock input signals

Bank	PLL	CLK p/n	Pin (p)	Pin (n)	Signal	Description
1	PLL 2	CLK 2	**R27**	**T27**	DB_CLK_IN(p/n)	incoming clock from the PMC user
1	PLL 2	CLK 3	R25	R26	--	**Not used.**
2	PLL 1	CLK 0	**P27**	N27	EXT_RST	Local reset button
2	PLL 1	CLK 1	P25	P26	--	**Not used.**

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Table 2: Signal / pin assignments for Clock input signals

Bank	PLL	CLK p/n	Pin (p)	Pin (n)	Signal	Description
3	PLL 5	CLK 14	**K17**	J17	conf_CLK	16Mhz from the configuration module
3	PLL 5	CLK 15	**M17**	**L17**	ext_OSC	optional oscillator clock
4	PLL 11	CLK 12	**K13**	J13	**--**	**Not Used.**
4	PLL 11	CLK 13	M13	L13	**--**	**Not Used.**
5	PLL 4	CLK10	**P4**	P3	**SMA_INPUT**	external clock input
5	PLL 4	CLK 11	**P2**	N2	strobe_abc	devoted to CameraLink
6	PLL 3	CLK 8	**R4**	R3	strobe_def	devoted to CameraLink
6	PLL 3	CLK 9	**R2**	T2	strobe_ghsp	devoted to CameraLink
7	PLL12	CLK 6	**AJ16**	AK16	**--**	**Not Used.**
7	PLL12	CLK 7	AG16	AH16	--	**Not used.**
8	PLL 6	CLK 4	**AL18**	AM18	pci_RST	--
8	PLL 6	CLK 5	**AK19**	AL19	PCI_CLK	--

Table 3: Signal / pin assignments for Clock output signals

Bank	PLL output	Pin (p)	Pin (n)	Signal	Description
9	PLL5out 0	**E15**	**D15**	DDR_BANK1_CK0(p/n)	Differential SSTL2 clocks feeding DDR SDRAM
9	PLL5out 1	**K14**	**K15**	DDR_BANK1_CK1(p/n)	Differential SSTL2 clocks feeding DDR SDRAM
10	PLL5out 2	**B17**	**A17**	DDR_BANK2_CK2(p/n)	Differential SSTL2 clocks feeding DDR SDRAM
10	PLL5out 3	**D18**	**C18**	DDR_BANK2_CK3(p/n)	Differential SSTL2 clocks feeding DDR SDRAM
11	PLL6out 0	**AL17**	**AM17**	--	--
11	PLL6out 1	AJ17	AK17	DB_CLK_OUT(p/n)	Clock going to the PMC user connector
12	PLL6out 2	**AJ18**	AK18	--	Not Used.
12	PLL6out 3	**AG18**	AH18	--	Not Used.

3.2 PCI / PCI-X Connector

3.2.1 Introduction

The PCI / PCI-X connector can act either as a PCI connector or as a PCI-X connector, depending on how the PCIXCAP is set (see Section 3.2.2 for details). The 5V key is not implemented on this connector because it can only be plugged into 3.3V busses (33 MHz or 66 MHz).

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3.2.2 PCIXCAP pin

The PCI-X SYS supports a 32/64-bit PCI/PCI-X connector that can only be plugged into 3.3V busses (33MHz or 66MHz).

A PCI-X bus is electrically equivalent to a regular PCI bus; the only difference is the PCIXCAP connection on the B-38 pin of the PCI connector. Figure 6 shows the structure of the PCIXCAP.

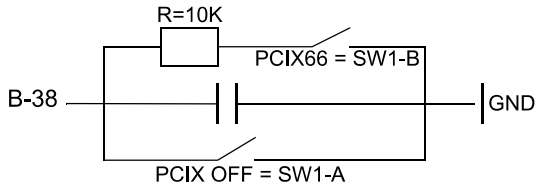


Figure 6: Structure of the PCIXCAP

You can configure the SW1 microswitches in the following ways:

Table 4: SW1 microswitch configurations

SW1-A	SW1-B	Board status
off	off	PCI-X 133 MHz board (default configuration)
off	on	PCI-X 66MHz board
on	off or on	PCI board

3.2.3 Signal / pin assignments for the PCI / PCI-X connector

Table 5 shows signal / pin assignments for the PCI / PCI-X connector. Note that all PCI interface signals are connected to bank 7 and bank 8 of the Stratix device.

Table 5: Pin assignments for main signals of the PCI / PCI-X connector

PCI / PCI-X pin	Stratix pin	Signal	PCI / PCI-X Pin	Stratix pin	Signal
B-48	V18	ad_pci[0]	B-80	AG20	ad_pci[47]
B-58	W18	ad_pci[1]	A-79	AE21	ad_pci[48]
A-57	AA18	ad_pci[2]	B-78	AH19	ad_pci[49]
A-56	Y9	ad_pci[3]	A-77	AF20	ad_pci[50]
A-55	AB7	ad_pci[4]	B-77	AG19	ad_pci[51]
B-55	AH9	ad_pci[5]	A-76	AG18	ad_pci[52]
A-54	AE9	ad_pci[6]	B-75	AE20	ad_pci[53]
B-53	AD8	ad_pci[7]	A-74	AF19	ad_pci[54]
B-52	AE8	ad_pci[8]	B-74	AF18	ad_pci[55]
A-49	AF9	ad_pci[9]	A-73	AE19	ad_pci[56]
B-48	AE7	ad_pci[10]	B-72	AE18	ad_pci[57]
A-47	AF8	ad_pci[11]	A-71	AD21	ad_pci[58]
B-47	AD6	ad_pci[12]	B-71	AB18	ad_pci[59]
A-46	AE6	ad_pci[13]	A-70	AD19	ad_pci[60]
B-45	AE5	ad_pci[14]	B-69	AB19	ad_pci[61]
A-44	AE4	ad_pci[15]	A-68	AD18	ad_pci[62]

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Table 5: Pin assignments for main signals of the PCI / PCI-X connector

PCI / PCI-X pin	Stratix pin	Signal	PCI / PCI-X Pin	Stratix pin	Signal
A-32	AF7	ad_pci[16]	B-68	AA20	ad_pci[63]
B-32	AG8	ad_pci[17]	B-60	W11	ack64_pci
A-31	AF6	ad_pci[18]	A-52	AF11	cbe_pci[0]
B-30	AG7	ad_pci[19]	B-44	AE11	cbe_pci[1]
A-29	AH8	ad_pci[20]	B-33	AC10	cbe_pci[2]
B-29	AF5	ad_pci[21]	B-26	AA11	cbe_pci[3]
A-28	AG6	ad_pci[22]	B-66	AF10	cbe_pci[4]
B-27	AH7	ad_pci[23]	A-65	AG10	cbe_pci[5]
A-25	AF4	ad_pci[24]	B-65	AG11	cbe_pci[6]
B-24	AH6	ad_pci[25]	A-64	AH11	cbe_pci[7]
A-23	AG5	ad_pci[26]	B-16	AA17	clk_pci
B-23	AH5	ad_pci[27]	B-37	V11	devsel_pci
A-22	AG4	ad_pci[28]	A-34	Y11	frame_pci
B-21	AH4	ad_pci[29]	A-17	AD10	gnt_pci
A-20	AG3	ad_pci[30]	A-26	AC8	idsel_pci
B-20	AH3	ad_pci[31]	A-6	AC21	inta_pci
A-91	AH24	ad_pci[32]	B-7	W19	intb_pci
B-90	AE24	ad_pci[33]	A-7	AB17	intc_pci
A-89	AH23	ad_pci[34]	B-8	Y17	intd_pci
B-89	AG23	ad_pci[35]	B-35	W12	irdy_pci
A-88	AF23	ad_pci[36]	B-39	Y19	lock_pci
B-87	AH22	ad_pci[37]	A-67	AH10	par64_pci
A-86	AG22	ad_pci[38]	A-43	AB11	par_pci
B-86	AE23	ad_pci[39]	B-40	AC9	perr_pci
A-85	AH21	ad_pci[40]	A-60	AG9	req64_pci
B-84	AF22	ad_pci[41]	B-18	AB10	req_pci
A-83	AG21	ad_pci[42]	A-15	AC17	rst_pci
B-83	AD23	ad_pci[43]	B-42	AE10	serr_pci
A-82	AH20	ad_pci[44]	A-38	AC11	stop_pci
B-81	AE22	ad_pci[45]	A-36	W10	trdy_pci
A-80	AF21	ad_pci[46]	B-49	AE14	m66_en

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3.3 PMC interface

3.3.1 PMC32 and PMC64

3.3.1.1 Introduction

The PCI-X SYS board implements a standard PCI Mezzanine Card (PMC) interface on the component side of the board. Assuming the Stratix device implements a PCI host Core, you can plug standard PMC daughter cards into this interface (see Section 3.3.4 for more details). You can also plug custom daughter cards into the PMC connector (see Section 3.3.1.2 for pin assignments).

3.3.1.2 Signal / pin assignments for the PMC32 and PMC64 interfaces

All PMC signals are connected to banks 1 and 2 of the Stratix device. Table 6, Figure 7, and Figure 8 describe signal / pin assignments for the three PMC connectors.

Table 6: signal / pin assignments for the PMC 32A connector

PMC 32A pin	Stratix pin	Signal	PMC 32A pin	Stratix pin	Signal
1	K12	TCK	2		-12V
3		GND	4	F25	Pmc_INTA
5	C27	pmc_INTB	6	F26	Pmc_INTC
7	C28	BUSMODE1	8		+5V
9	D27	Pmc_INTD	10		NC
11		GND	12		NC
13	D28	Pmc_CLK	14		GND
15		GND	16	H21	Pmc_GNT
17	E27	Pmc_REQ	18		+5V
19		+3,3V	20	H24	Pmc_AD31
21	E28	Pmc_AD28	22	H26	Pmc_AD27
23	F27	Pmc_AD25	24		GND
25		GND	26	J24	Pmc_CBE3
27	F28	Pmc_AD22	28	J26	Pmc_AD21
29	G27	Pmc_AD19	30		+5V
31		+3,3V	32	K24	Pmc_AD17
33	G28	Pmc_FRAME	34		GND
35		GND	36	K26	Pmc_IRDY
37	H27	Pmc_DEVSEL	38		+5V
39		GND	40	L21	Pmc_LOCK
41		NC	42		NC
43	H28	Pmc_PAR	44		GND
45		+3,3V	46	L26	Pmc_AD15
47	J27	Pmc_AD12	48	M20	Pmc_AD11
49	J28	Pmc_AD09	50		+5V

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Table 6: signal / pin assignments for the PMC 32A connector

PMC 32A pin	Stratix pin	Signal	PMC 32A pin	Stratix pin	Signal
51		GND	52	M23	Pmc_CBE0
53	K27	Pmc_AD06	54	M24	Pmc_AD05
55	K28	Pmc_AD04	56		GND
57		+3,3V	58	M25	Pmc_AD03
59	L27	Pmc_AD02	60	M26	Pmc_AD01
61	L28	PMC_AD0	62		+5V
63		GND	64	N20	Pmc_REQ64

Table 7: signal / pin assignments for the PMC 32B connector

PMC 32B pin	Stratix pin	Signal	PMC 32B pin	Stratix pin	Signal
1		+12V	2		NC
3	F13	Pmc_TMS	4	G13	Pmc_TDO
5		Pmc_TDI	6		GND
7		GND	8		NC
9		NC	10		NC
11	G23	BUSMODE2	12		+3,3V
13	G25	Pmc_RESET	14	G24	BUSMODE3
15		+3,3V	16	G26	BUSMODE4
17		NC	18		GND
19	H23	Pmc_AD30	20	H22	Pmc_AD29
21		GND	22	H25	Pmc_AD26
23	J21	Pmc_AD24	24		+3,3V
25	J23	Pmc_IDSEL	26	J22	Pmc_AD23
27		+3 ,3V	28	J25	Pmc_AD20
29	K21	Pmc_AD18	30		GND
31	K23	Pmc_AD16	32	K22	Pmc_CBE2
33		GND	34		NC
35	K25	Pmc_TRDY	36		+3,3V
37		GND	38	L19	Pmc_STOP
39	L20	Pmc_PERR	40		GND
41		+3,3V	42	L22	Pmc_SERR
43	L23	Pmc_CBE1	44		GND
45	L25	Pmc_AD14	46	L24	Pmc_AD13
47		GND	48	M19	Pmc_AD10

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Table 7: signal / pin assignments for the PMC 32B connector

PMC 32B pin	Stratix pin	Signal	PMC 32B pin	Stratix pin	Signal
49	M21	Pmc_AD08	50		+3,3V
51	M22	Pmc_AD07	52		NC
53		+3,3V	54		NC
55		NC	56		GND
57		NC	58		NC
59		GND	60		NC
61	N19	Pmc_ACK64	62		+3,3V
63		GND	64		NC

Note that all PMC64 signals are pulled up to 3.3V through 10KΩ.

Table 8: Signal / pin assignments for the PMC64 connector

PMC 64pin	Stratix pin	Signal	PMC 64 pin	Stratix pin	Signal
1	NC		2	GND	
3	GND		4	Pmc_CBE7	N21
5	Pmc_CBE6	M27	6	Pmc_CBE5	N22
7	Pmc_CBE4	N28	8	GND	
9	+3,3V		10	Pmc_PAR64	AF25
11	Pmc_AD63	T28	12	Pmc_AD62	N24
13	Pmc_AD61	U27	14	GND	
15	GND		16	Pmc_AD60	N26
17	Pmc_AD59	V28	18	Pmc_AD58	T20
19	Pmc_AD57	V27	20	GND	
21	+3,3V		22	Pmc_AD56	U20
23	Pmc_AD55	W28	24	Pmc_AD54	U21
25	Pmc_AD53	W27	26	GND	
27	GND		28	Pmc_AD52	U22
29	Pmc_AD51	Y28	30	Pmc_AD50	U23
31	Pmc_AD49	Y27	32	GND	
33	GND		34	Pmc_AD48	U26
35	Pmc_AD47	AA28	36	Pmc_AD46	V21
37	Pmc_AD45	AA27	38	GND	
39	+3,3V		40	Pmc_AD44	V24
41	Pmc_AD43	AB28	42	Pmc_AD42	W21
43	Pmc_AD41	AB27	44	GND	
45	GND		46	Pmc_AD40	W26

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Table 8: Signal / pin assignments for the PMC64 connector

PMC 64pin	Stratix pin	Signal	PMC 64 pin	Stratix pin	Signal
47	Pmc_AD39	AC28	48	Pmc_AD38	Y25
49	Pmc_AD37	AC27	50	GND	
51	GND		52	Pmc_AD36	AA25
53	Pmc_AD35	AD28	54	Pmc_AD34	AA22
55	Pmc_AD33	AD27	56	GND	
57	+3.3V		58	Pmc_AD32	AB25
59	NC		60	NC	
61	NC		62	GND	
63	GND		64	NC	

3.3.2 PMC user extension

3.3.2.1 Introduction

The following signals are available on the PMC user connector:

- **PMC_USR[37..0]**: General purpose 38-bit data path
- **DB_CLK_IN (p/n)**: Clock that comes from a daughter card
- **DB_CLK_OUT (p/n)**: Clock that goes to a daughter card
- **EXT_OSC**: Local oscillator that feeds the Stratix and the daughter card
- **EXT_RST**: Reset Button that feeds the Stratix device and the daughter card

3.3.2.2 Signal / pin assignments for the PMC user connector

Table 9 describes signal / pin assignments for the PMC user connector.

Table 9: Signal / pin assignments for the PMC user connector

PMC user pin	Stratix pin	Signal	PMC user pin	Stratix pin	Signal
1	--	+12V	2	--	+12V
3	--	GND	4	--	GND
5	P27	EXT_RST	6	M17	EXT_OSC
7	W14	DB_CLK_OUTp	8	R27	DB_CLK_INp
9	W15	DB_CLK_OUTn	10	T27	DB_CLK_INn
11	N23	Pmc_usr00	12	N25	Pmc_usr01
13	--	+5V	14	–	+5V
15	P26	Pmc_usr02	16	R26	Pmc_usr03
17	T19	Pmc_usr04	18	T21	Pmc_usr05
19	T22	Pmc_usr06	20	T23	Pmc_usr07
21	T24	Pmc_usr08	22	T25	Pmc_usr09
23	T26	Pmc_usr10	24	U19	Pmc_usr11
25	--	+3.3V	26	--	+3.3V

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Table 9: Signal / pin assignments for the PMC user connector

PMC user pin	Stratix pin	Signal	PMC user pin	Stratix pin	Signal
27	--	+3.3V	28	--	+3.3V
29	U24	Pmc_usr12	30	U25	Pmc_usr13
31	V19	Pmc_usr14	32	V20	Pmc_usr15
33	V23	Pmc_usr16	34	V22	Pmc_usr17
35	V26	Pmc_usr18	36	V25	Pmc_usr19
37	--	GND	38	--	GND
39	--	GND	40	--	GND
41	W23	Pmc_usr20	42	W22	Pmc_usr21
43	W25	Pmc_usr22	44	W24	Pmc_usr23
45	Y22	Pmc_usr24	46	Y21	Pmc_usr25
47	Y26	Pmc_usr26	48	Y23	Pmc_usr27
49	AA23	Pmc_usr28	50	Y24	Pmc_usr29
51	--	+5V	52	–	+5V
53	AA26	Pmc_usr30	54	AA21	Pmc_usr31
55	AB26	Pmc_usr32	56	AA24	Pmc_usr33
57	AE28	Pmc_usr34	58	AE27	Pmc_usr35
59	AF28	Pmc_usr36	60	AF27	Pmc_usr37
61	--	GND	62	--	GND
63	--	-12V	64	--	-12V

3.3.3 Mictor 38-point test / 20-pin IDC header

3.3.3.1 Introduction

The Mictor connector shares 17 pins with the PMC user connector and 19 pins with a 20-pin IDC header (marked TST on the board). You can use the Mictor connector with an HP logic analyzer for medium-speed (up to 250 MHz) signal probing.

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3.3.3.2 Signal / pin assignments for the Mictor connectors

Table 10: Signal / pin assignments for the Mictor connector

Mictor pin	Stratix pin	PMC USR	Signal	Mictor pin	Stratix pin	PMC USR	Signal
						20	GND
1 (5VDC)		14	+5V	2 (SCL)	AB22	19	Mic_SCLodd
3 (GND)		4	GND	4 (SDA)	Y20	18	Mic_SDAodd
5 (CLK even)	M17	6	EXT_OSC	6 (CLK odd)	AB20	17	Mic_CLKodd
7 (D15 even)	R27	8	DB_CLK_INp	8 (D15 odd)	AE25	16	Mic_D15odd
9 (D14 even)	T27	10	DB_CLK_INn	10 (D14 odd)	AC22	15	Mic_D14odd
11 (D13 even)	N25	12	Pmc_usr01	12 (D13 odd)	AC23	14	Mic_D13odd
13 (D12 even)	R26	16	Pmc_usr03	14 (D12 odd)	AF17	13	Mic_D12odd
15 (D11 even)	T21	18	Pmc_usr05	16 (D11 odd)	AC20	12	Mic_D11odd
17 (D10 even)	T23	20	Pmc_usr07	18 (D10 odd)	AE17	11	Mic_D10odd
19 (D09 even)	T25	22	Pmc_usr09	20 (D09 odd)	AD24	10	Mic_D09odd
21 (D08 even)	U19	24	Pmc_usr11	22 (D08 odd)	AD17	9	Mic_D08odd
23 (D07 even)	U25	30	Pmc_usr13	24 (D07 odd)	AD16	8	Mic_D07odd
25 (D06 even)	V20	32	Pmc_usr15	26 (D06 odd)	AE16	7	Mic_D06odd
27 (D05 even)	V22	34	Pmc_usr17	28 (D05 odd)	AD13	6	Mic_D05odd
29 (D04 even)	V25	36	Pmc_usr19	30 (D04 odd)	AE13	5	Mic_D04odd
31 (D03 even)	W22	42	Pmc_usr21	32 (D03 odd)	AD12	4	Mic_D03odd
33 (D02 even)	W24	44	Pmc_usr23	34 (D02 odd)	AB21	3	Mic_D02odd
35 (D01 even)	Y21	46	Pmc_usr25	36 (D01 odd)	AF16	2	Mic_D01odd
37 (D00 even)	Y23	48	Pmc_usr27	38 (D00 odd)	AE12	1	Mic_D00odd

3.3.4 Daughter boards

3.3.4.1 Introduction

You can extend the features of the PCI-X SYS board by adding daughter boards in order to meet additional A/D processes or memory storage requirements. You can design your own daughter board, or PLDA can build a custom daughter board for you. PLDA designs boards for industrial and semi-industrial applications, including Bread boards, optical fiber boards, and LVTTL boards. Please contact PLDA for more details.

3.3.4.2 Mechanical specifications

If you design your own daughter board, you will need the following information:

Table 11: PMC connector part numbers for the Mezzanine IEEE 1386

	MOLEX reference	AMP reference
male connector (mounted on PCI-X SYS)	71436-2864	0-0120527-1
female connector (mounted on daughter board)	71439-0864	0-0120521-1

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In order to work properly, PMC connectors and hole placements must conform with Figure 7.

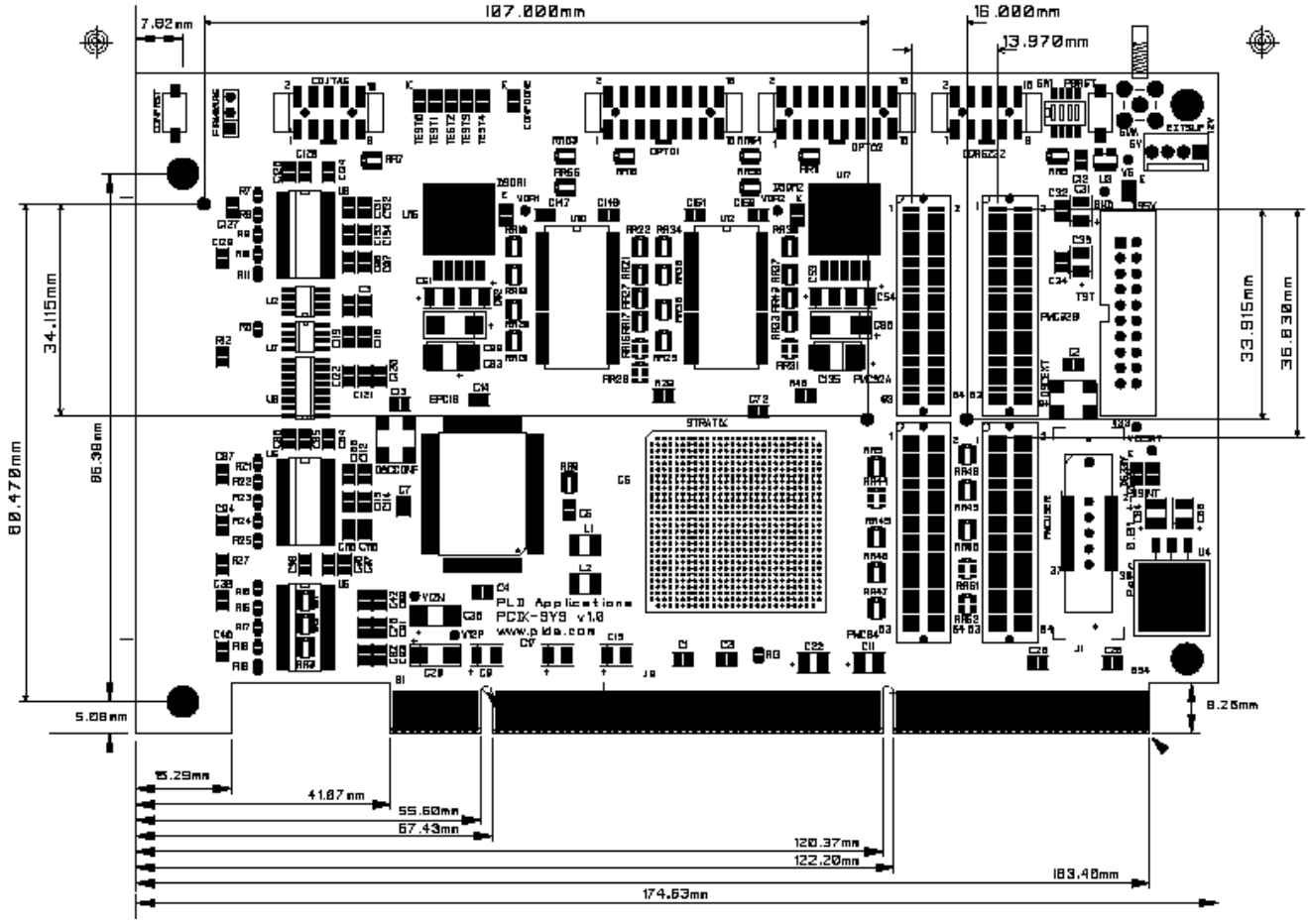


Figure 7: Dimensions of the PCI-X SYS board

3.4 Base CameraLink interface

3.4.1 Introduction

CameraLink is a standard interface primarily used for connecting digital cameras and other frame-grabbing applications. At the time of purchase, you decide how you wish PLDA to manufacture the CameraLink interfaces, either as a single 80-pin data link (full CameraLink) or as two independent 24-pin data links (dual-base CameraLink).

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Figure 8 illustrates all potential configurations of the CameraLink interface.

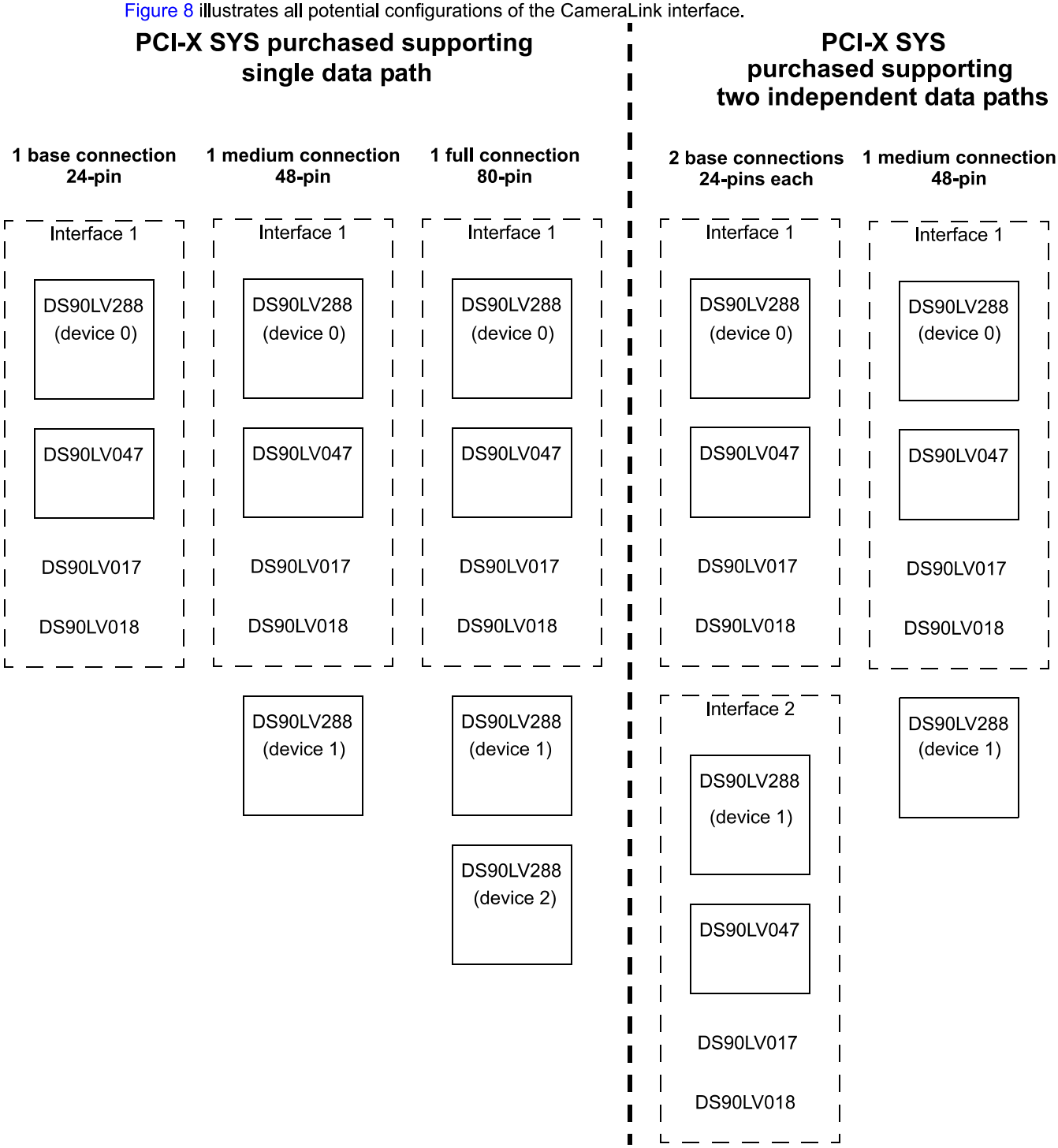


Figure 8: All possible configurations of the CameraLink interfaces

3.4.1.1 Two independent data paths

If you choose to purchase the PCI-X SYS with two independent data paths, each path includes:

- 24-bit data path
- 4 synchronization signals
- 4 command signals
- strobe signal routed to a dedicated clock input
- serial link (Rx/Tx)

Figure 9 illustrates two distinct data paths for the CameraLink connector.

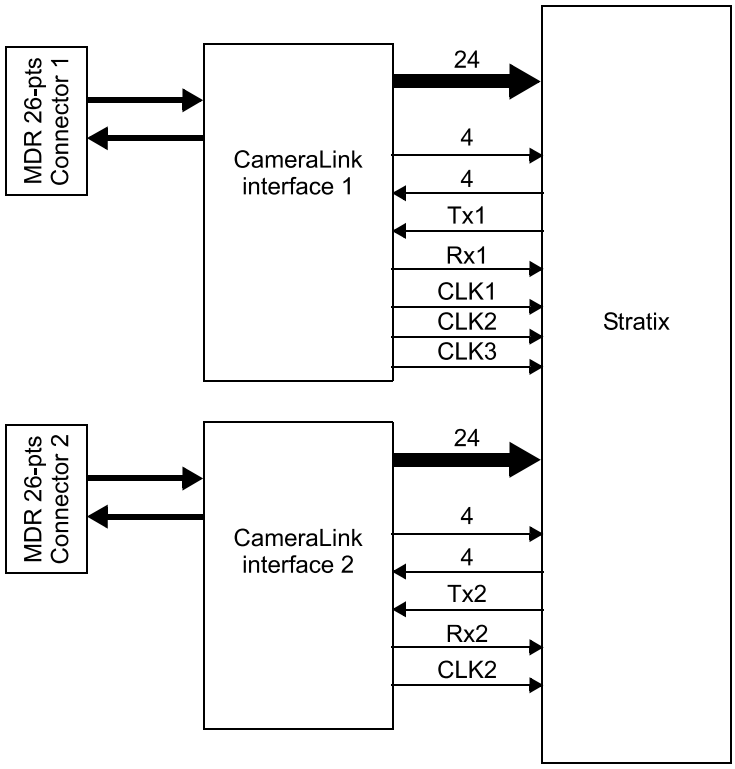


Figure 9: CameraLink connector: 2 distinct data paths

All signals of the two-data-path model connect to Banks 5 and 6 of the Stratix device.

3.4.1.2 Single data path

The other possibility is to purchase the PCI-X SYS with one common CameraLink data path, in which case the interface includes:

- up to 80-bit data path
- 4 synchronization signals
- 4 command signals
- 3 strobe signals routed to dedicated clock inputs
- 1 serial link (Rx/Tx)

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Figure 10 illustrates a single data path for the CameraLink connector.

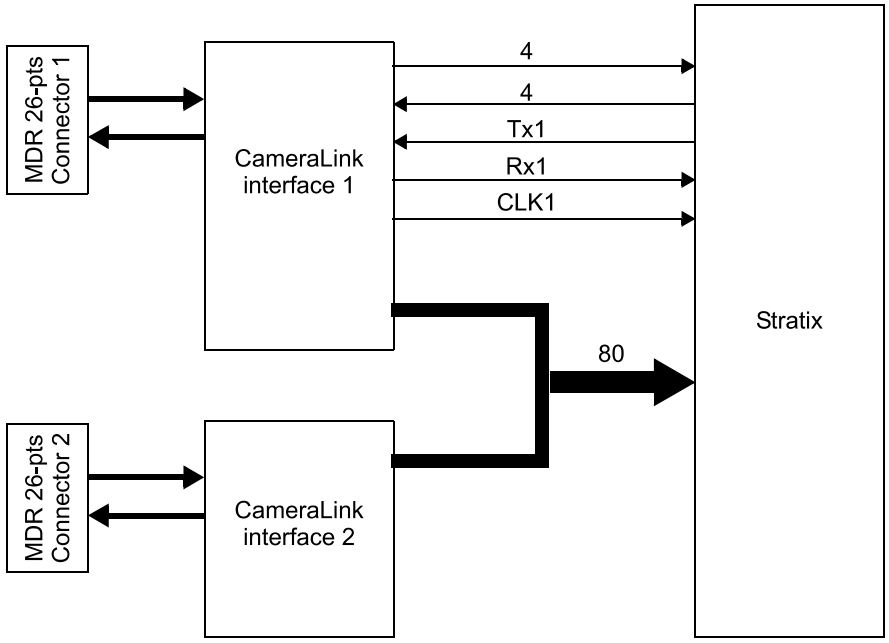


Figure 10: CameraLink connector: full interface

All signals of the shared data-path model connect to Bank 5 of the Stratix device.

3.4.2 Interface 1

3.4.2.1 Block diagram of the Base CameraLink interface 1

Figure 11 illustrates the architecture of interface 1 of the base CameraLink connector.

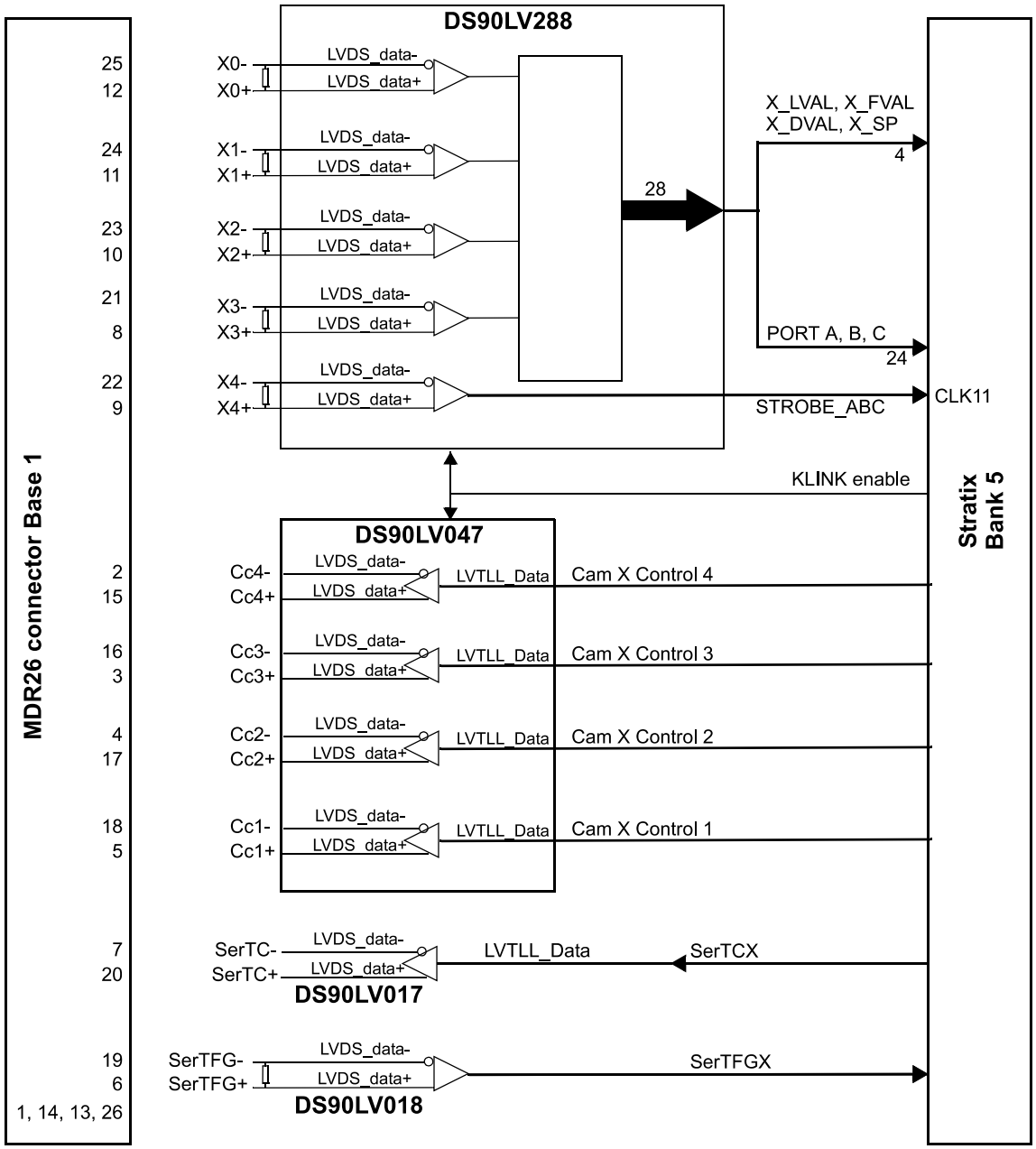


Figure 11: Block diagram of the base CameraLink Interface: two-data-path model

3.4.2.2 Signal / pin assignments for interface 1

Table 12, Table 13, and Table 14 describe signal / pin assignments interface 1 of the Base CameraLink connector.

Table 12: Signal / pin assignments for data-related signals of the CameraLink connector interface 1

Signal	Stratix pin	Signal	Stratix pin
Port_a		Port_a	
Port_a0	N1	Port_a4	M2
Port_a1	N5	Port_a5	M4

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Table 12: Signal / pin assignments for data-related signals of the CameraLink connector interface 1

Signal	Stratix pin	Signal	Stratix pin
Port_a2	N4	Port_a6	J3
Port_a3	N3	Port_a7	M3
Port_b		Port_b	
Port_b0	L5	Port_b4	K1
Port_b1	L3	Port_b5	K3
Port_b2	L4	Port_b6	L2
Port_b3	K8	Port_b7	L1
Port_c		Port_c	
Port_c0	K4	Port_c4	G1
Port_c1	H3	Port_c5	K7
Port_c2	H1	Port_c6	K2
Port_c3	G2	Port_c7	J4

Synchronization signals, described in Table 13, are sent from the CameraLink connector to the Stratix device.

Table 13: Signal / pin assignments for synchronization signals of the CameraLink connector

Stratix pin	Signal
P2	Strobe_abc
H4	X_LVAL
J1	X_FVAL
J2	X_DVAL
H2	X_SP
M5	KLINK_EN[a]

a. Active high allows CameraLink function.

Control signals, listed in Table 14, are sent from the Stratix device to the CameraLink connector.

Table 14: Signal / pin assignments for control signals of the CameraLink connector

Stratix pin	Signal
T6	CxC4
R3	CxC3
T5	CxC2
T4	CxC1
N6	SerTC_X
P3	SerTFG_X

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3.4.3 Interface 2

3.4.3.1 Block diagram of interface 2

Figure 12 illustrates the architecture of the second interface of the base CameraLink connector with a second DS90LV288 component (device 1), which makes a medium CameraLink connector.

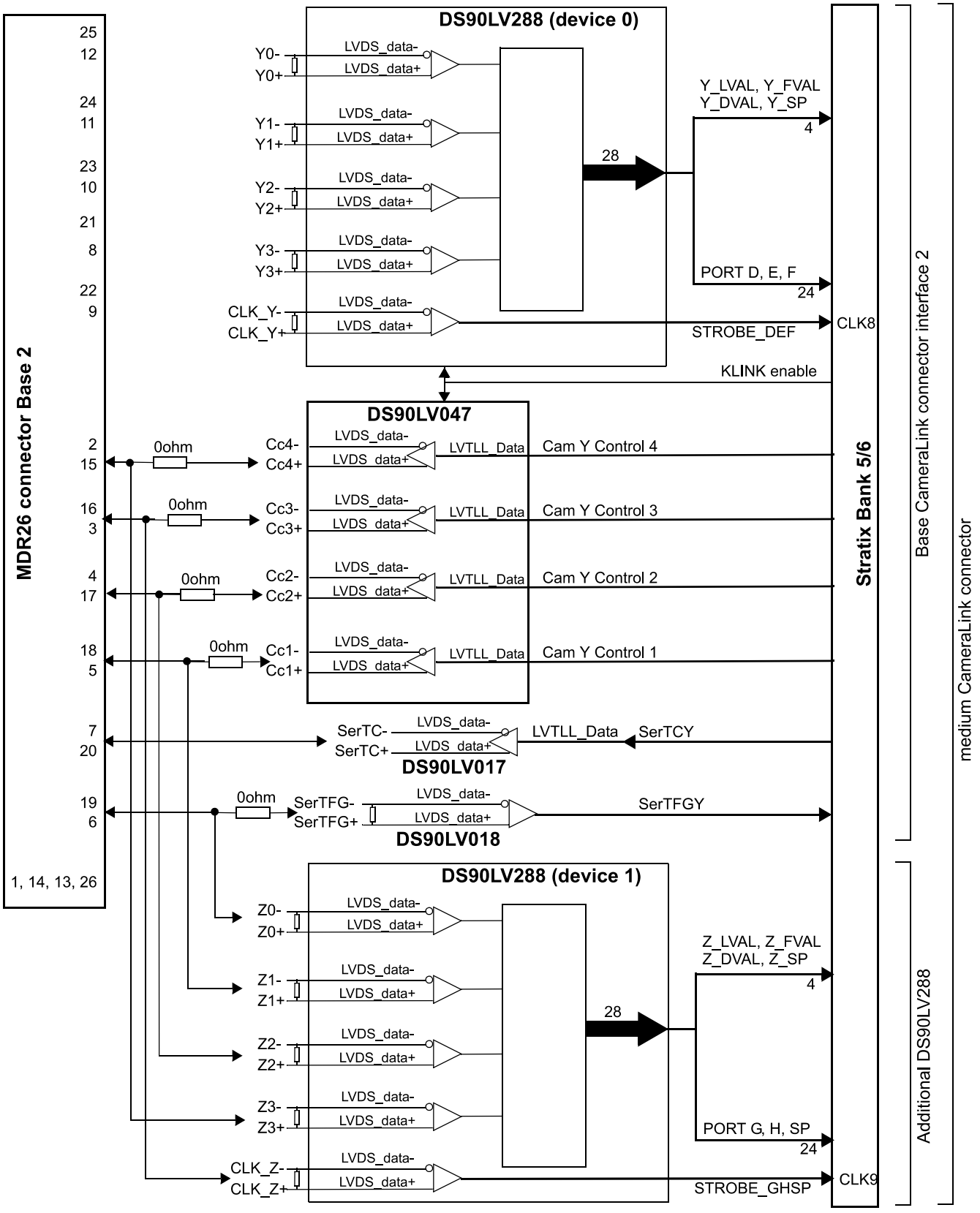


Figure 12: Block diagram of the CameraLink Interface

3.4.3.2 Signal / pin assignments for interface 2

Table 15, Table 16, and Table 17 describe signal / pin assignments for interface 2.

Table 15: Signal / pin assignments for data-related signals of the CameraLink connector interface 1

Signal	Stratix pin	Signal	Stratix pin
Port_d		Port_d	
Port_d0	U10	Port_d4	V7
Port_d1	V9	Port_d5	W5
Port_d2	V10	Port_d6	W2
Port_d3	V8	Port_d7	W6
Port_e		Port_e	
Port_e0	Y4	Port_e4	V1
Port_e1	Y3	Port_e5	V2
Port_e2	W4	Port_e6	Y1
Port_e3	W1	Port_e7	Y2
Port_f		Port_f	
Port_f0	W3	Port_f4	U6
Port_f1	U3	Port_f5	U8
Port_f2	V5	Port_f6	V3
Port_f3	U7	Port_f7	U4
Port_g		Port_g	
Port_g0	AA6	Port_g4	AB4
Port_g1	AA8	Port_g5	AF1
Port_g2	AA7	Port_g6	H6
Port_g3	AF2	Port_g7	AE2
Port_h		Port_h	
Port_h0	AE1	Port_h4	AA5
Port_h1	AD2	Port_h5	Y6
Port_h2	AD1	Port_h6	AC2
Port_h3	AB3	Port_h7	AC1
Port_sp		Port_sp	
Port_sp0	Y5	Port_sp4	J6
Port_sp1	W8	Port_sp5	J5
Port_sp2	Y8	Port_sp6	Y7
Port_sp3	J7	Port_sp7	W7

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Synchronization signals, described in Table 16, are sent from the CameraLink connector to the Stratix device.

Table 16: Signal / pin assignments for synchronization signals of the CameraLink connector

Stratix pin	Signal
Y channel	
R4	Strobe_def
U5	Y_LVAL
V6	Y_FVAL
V4	Y_DVAL
U9	Y_SP
Z channel	
R2	Strobe_ghsp
K6	Z_LVAL
H7	Z_FVAL
H5	Z_DVAL
K5	Z_SP

Control signals, listed in Table 17, are sent from the Stratix device to the CameraLink connector.

Table 17: Signal / pin assignments for control signals of the CameraLink connector

Stratix pin	Signal
AB2	CyC4
AB1	CyC3
AA4	CyC2
AA1	CyC1
AA3	SerTC_Y
AA2	SerTFG_Y

3.5 DDR SDRAM

3.5.1 Introduction

The DDR SDRAM module includes two identical independent 64MB banks (organized into 16M*32 bit Words). Each bank is built with 2 Micron devices (part: MT46V16M16 or cross reference).

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3.5.2 Block diagram of the DDR SDRAM

Figure 13 illustrates the structure of the DDR SDRAM.

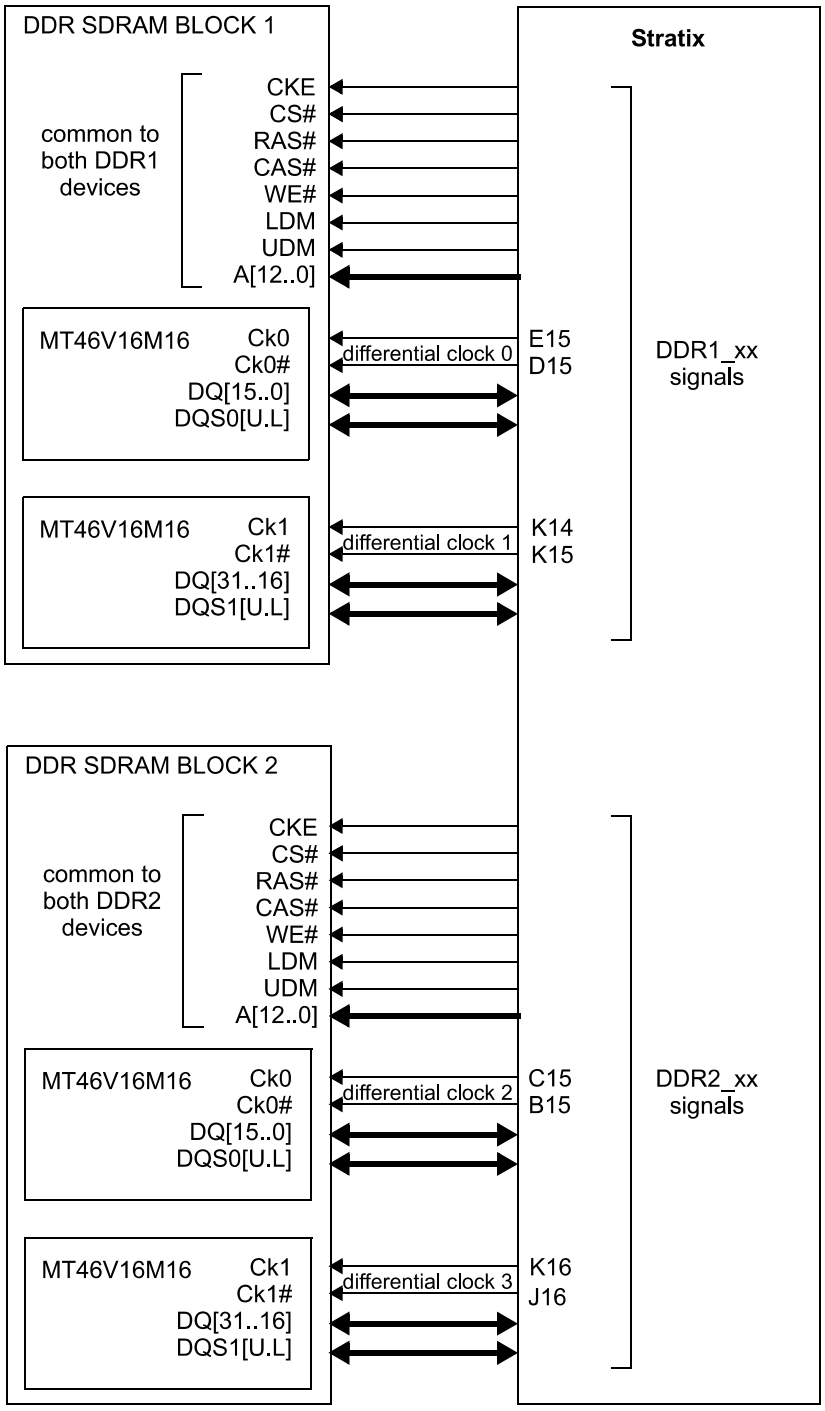


Figure 13: Block diagram of DDR SDRAM

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3.5.3 I/O electrical constraints

3.5.3.1 SSTL2 class 1 I/Os

The I/O standard for the DDR SDRAM is 2.5V SSTL_2 (VDD / VDDQ = 2.5V), as illustrated in Figure 14.

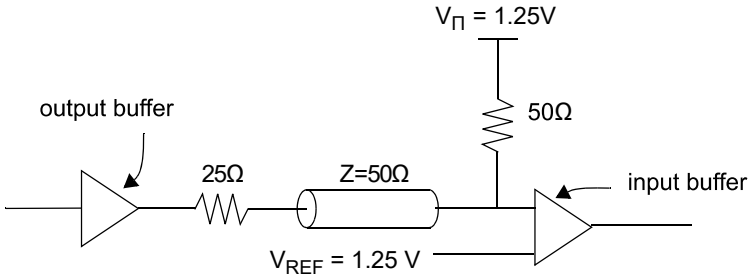


Figure 14: SSTL2 implementation

The standard requires SSTL_2 VTT (VREF = 1.25V = center rail Voltage termination). Power is supplied (VTT, VREF) to the Stratix device and to the DRR SDRAM chips by an LP2995.

3.5.3.2 Terminator technology

The Stratix device features Altera's Terminator technology, which shifts signal termination circuitry on chip, thereby saving space and simplifying board design. Keep in mind the following design rules in order to implement the technology:

- Altera recommends using on-chip series termination and parallel external pull-up resistors, for which each signal is tied to VTT through 50Ω.
- Differential termination is not supported on the top banks. Each clock signal (p and n) has a 25Ω series termination resistor and is tied to VTT through 50Ω.
- Each I/O pin has two dual-purpose reference pins to which two external reference resistors need to be connected:
  - Signal RUP4 (Stratix pin: H11) is tied to 2.5V through 500Ω
  - Signal RDN4 (Stratix pin: G11) is tied to GND through 500Ω
  - Signal RUP3 (Stratix pin: J18) is tied to 2.5V through 500Ω
  - Signal RDN3 (Stratix pin: K19) is tied to GND through 500Ω

3.5.4 Signal / pin assignments for the DDR SDRAM

Table 18 and Table 19 describe signal / pin assignments for the DDR SDRAM.

Table 18: Signal / pin assignments for the DDR SDRAM banks 0 and 1

Signal	Stratix pin	Signal	Stratix pin
Control Signals		Control Signals	
DDR1_CKE	E12	DDR1_A13	--
DDR1_CS#	F9	DDR1_A12	D12
DDR1_RAS#	G9	DDR1_A11	C12
DDR1_CAS#	F10	DDR1_A10	H10
DDR1_WE#	G12	DDR1_A09	G10
DDR1_LDM	E13	DDR1_A08	F11
DDR1_UDM	D13	DDR1_A07	B12
DDR1_CK0	E15	DDR1_A06	B13
DDR1_CK0#	D15	DDR1_A05	A13

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Table 18: Signal / pin assignments for the DDR SDRAM banks 0 and 1

Signal	Stratix pin	Signal	Stratix pin
DDR1_CK1	K14	DDR1_A04	C13
DDR1_CK1#	K15	DDR1_A03	J11
DDR1_DQS1U	D10	DDR1_A02	J9
DDR1_DQS1L	C9	DDR1_A01	H9
DDR1_DQS0U	B6	DDR1_A00	G7
DDR1_DQS0L	D5	DDR1_BA1	G8
		DDR1_BA0	F8
Bank 1		Bank 0	
DDR1_DQ31	B11	DDR1_DQ15	D6
DDR1_DQ30	C11	DDR1_DQ14	D7
DDR1_DQ29	D11	DDR1_DQ13	C7
DDR1_DQ28	B10	DDR1_DQ12	A6
DDR1_DQ27	A11	DDR1_DQ11	C6
DDR1_DQ26	C10	DDR1_DQ10	B7
DDR1_DQ25	A10	DDR1_DQ09	A7
DDR1_DQ24	E10	DDR1_DQ08	E6
DDR1_DQ23	A9	DDR1_DQ07	C5
DDR1_DQ22	B9	DDR1_DQ06	A3
DDR1_DQ21	A8	DDR1_DQ05	C4
DDR1_DQ20	B8	DDR1_DQ04	B4
DDR1_DQ19	D9	DDR1_DQ03	B5
DDR1_DQ18	E8	DDR1_DQ02	B3
DDR1_DQ17	C8	DDR1_DQ01	A4
DDR1_DQ16	D8	DDR1_DQ00	A5

Table 19: Signal / pin assignments for the DDR SDRAM banks 2 and 3

Signal	Stratix pin	Signal	Stratix pin
Control Signals		Control Signals	
DDR2_CKE	C25	DDR2_A13	

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Table 19: Signal / pin assignments for the DDR SDRAM banks 2 and 3

Signal	Stratix pin	Signal	Stratix pin
DDR2_CS#	J20	DDR2_A12	D24
DDR2_RAS#	H20	DDR2_A11	C24
DDR2_CAS#	F21	DDR2_A10	F18
DDR2_WE#	G21	DDR2_A09	A24
DDR2_LDM	F22	DDR2_A08	B26
DDR2_UDM	G22	DDR2_A07	A26
DDR2_CK2	C15	DDR2_A06	B24
DDR2_CK2#	B15	DDR2_A05	A25
DDR2_CK3	K16	DDR2_A04	B25
DDR2_CK3#	J16	DDR2_A03	J17
DDR2_DQS1U	D23	DDR2_A02	H19
DDR2_DQS1L	D20	DDR2_A01	G19
DDR2_DQS0U	B18	DDR2_A00	F17
DDR2_DQS0L	A16	DDR2_BA1	F19
		DDR2_BA0	F20
Bank 3		Bank 2	
DDR2_DQ31	B23	DDR2_DQ15	D18
DDR2_DQ30	E23	DDR2_DQ14	C18
DDR2_DQ29	C23	DDR2_DQ13	D19
DDR2_DQ28	A23	DDR2_DQ12	A19
DDR2_DQ27	D22	DDR2_DQ11	B19
DDR2_DQ26	C22	DDR2_DQ10	C19
DDR2_DQ25	B22	DDR2_DQ09	E19
DDR2_DQ24	A22	DDR2_DQ08	A18
DDR2_DQ23	E21	DDR2_DQ07	D17
DDR2_DQ22	C20	DDR2_DQ06	B16
DDR2_DQ21	D21	DDR2_DQ05	C17
DDR2_DQ20	B21	DDR2_DQ04	E17
DDR2_DQ19	A21	DDR2_DQ03	B17
DDR2_DQ18	C21	DDR2_DQ02	C16
DDR2_DQ17	B20	DDR2_DQ01	D16
DDR2_DQ16	A20	DDR2_DQ00	E16

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3.6 Miscellaneous features

3.6.1 Opto-coupled inputs and outputs

The PCI-X SYS supports eight opto-isolated inputs and eight opto-isolated outputs (the OPTO2 connector is not available on boards mounted with the EP1S10).

3.6.1.1 Setting the power of the opto-coupled outputs

Two pairs of jumpers found on the solder side of the board (shown in Figure 15) allow you to drive the opto-coupled outputs at either 5V or 12V.



Figure 15: photograph: jumpers used to drive the opto outputs at either 5V or 12V (solder side of board)

Table 20 describes jumper / voltage settings for the two connectors.

Table 20: Jumpers used to determine voltage for the Opto-coupled outputs

Connector	Volts	Solder jumper...
OPTO1	5	OPTO5A
	12	OPTO12A
OPTO2	5	OPTO5B
	12	OPTO12B

WARNING: Soldering the following combinations of jumpers simultaneously will damage the board:

- OPTO5A and OPTO12A
- OPTO5B and OPTO12B

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3.6.1.2 Electrical schematics of the opto-isolated connector

Figure 16 illustrates the architecture of the opto-isolated connector.

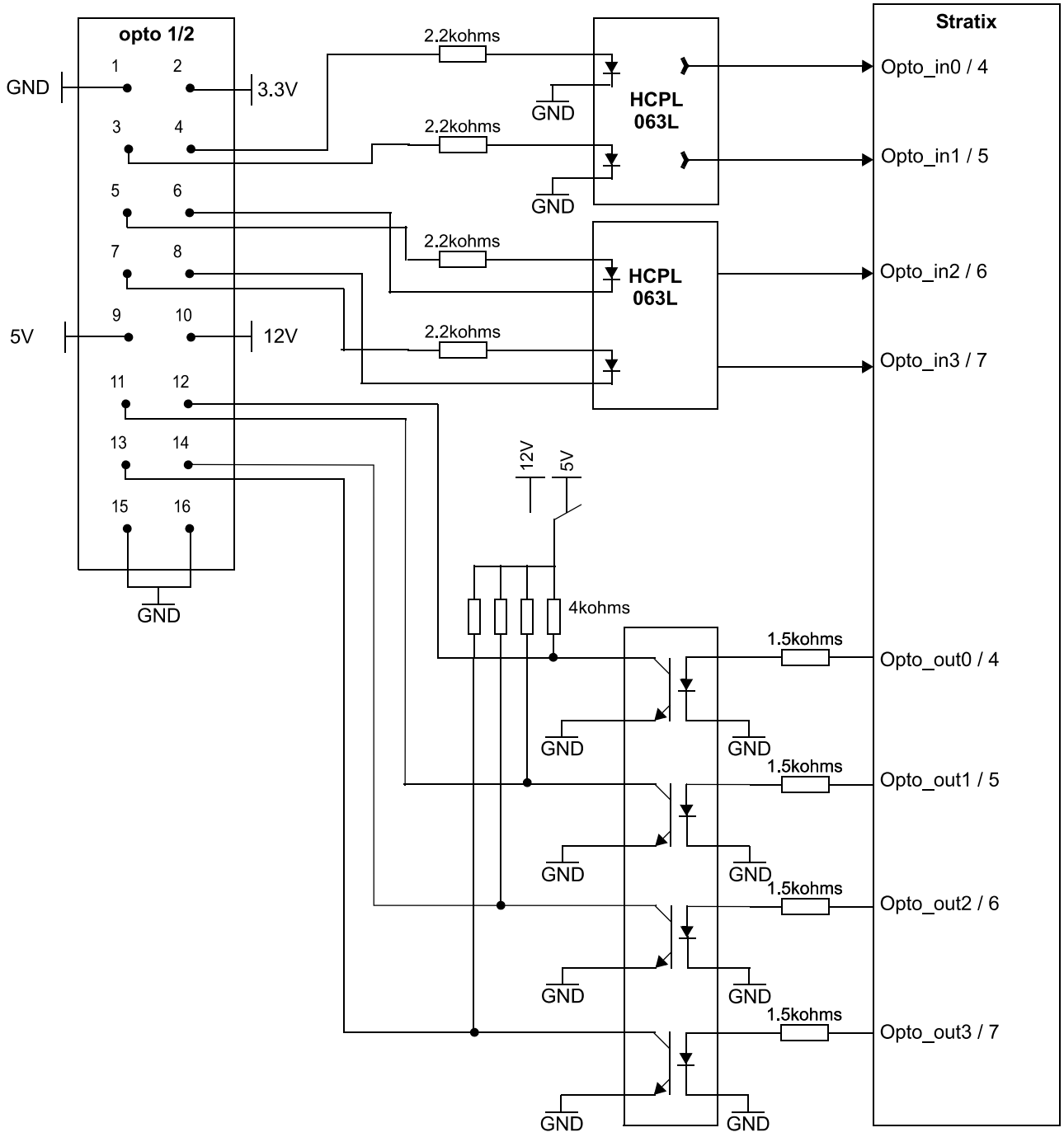


Figure 16: Block diagram of the opto-isolated connector

3.6.1.3 Signal / pin assignments for the opto-isolated connector

Table 21: Signal / pin assignments for the opti-isolated connector

opto-isolated pin	Stratix pin	Signal	opto-isolated pin	Stratix pin	Signal
inputs			outputs		
4 (anode)	C1	OPTO_IN0	12	E1	OPTO_OUT0
3 (annode)	C2	OPTO_IN1	11	E2	OPTO_OUT1
5 (anode) and 6 (cathode)	D1	OPTO_IN2	14	F1	OPTO_OUT2
7 (anode) and 8 (cathode)	D2	OPTO_IN3	13	F2	OPTO_OUT3
4	L7	OPTO_IN4	12	L9	OPTO_OUT4
3	N7	OPTO_IN5	11	L10	OPTO_OUT5
5 and 6	L8	OPTO_IN6	14	M9	OPTO_OUT6
7 and 8	M8	OPTO_IN7	13	M10	OPTO_OUT7

3.6.2 User LEDs

The PCI-X SYS includes four LEDs.

Table 22: LED signals

LED	Stratix pin	Signal	LED	Stratix pin	Signal
0	N8	USR_LED0	2	M7	USR_LED2
1	M6	USR_LED1	3	L6	USR_LED3

3.6.3 RS232 Interface

The PCI-X SYS includes two RS232 channels that are implemented on a single 10-pin IDC header. The RS232 connector includes two inputs and two outputs and allow two simple serial links (Tx / RX) or one extended serial link (Tx / Rx / CTS / RTS). Figure 17 illustrates signal / pin assignments for the RS232 connector.

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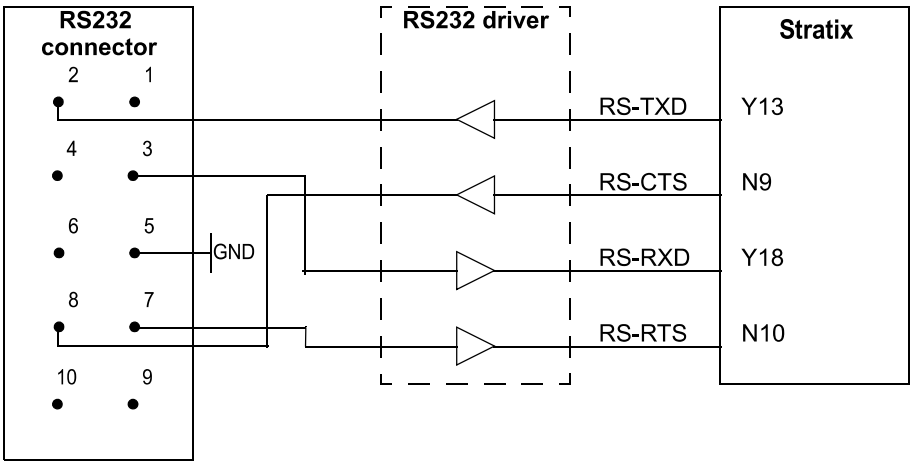


Figure 17: RS232 serial links

3.6.4 Local oscillator (optional)

Figure 18 shows the local oscillator print.

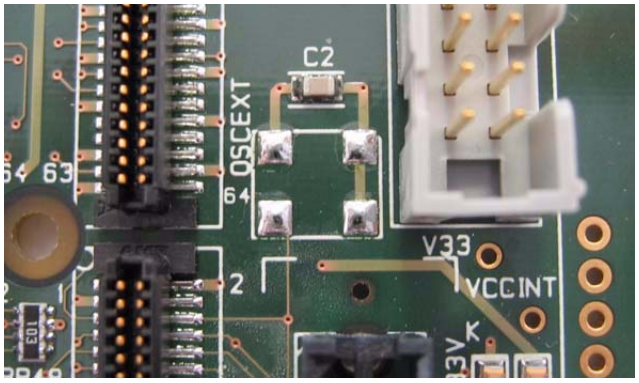


Figure 18: Photograph: Local oscillator print

A local oscillator can be mounted (on request) on the PCI-X SYS. Its output clock signal (EXT_OSC) connects to dedicated pin M17 of the Stratix device.

Available Oscillator frequencies vary between 1.84 MHz and 125 MHz. The PCI-X SYS board uses a Jauch oscillator, part number VX3J.

3.6.5 SMA inputs

Figure 19 shows the SMA input, the local reset button, and the microswitches.

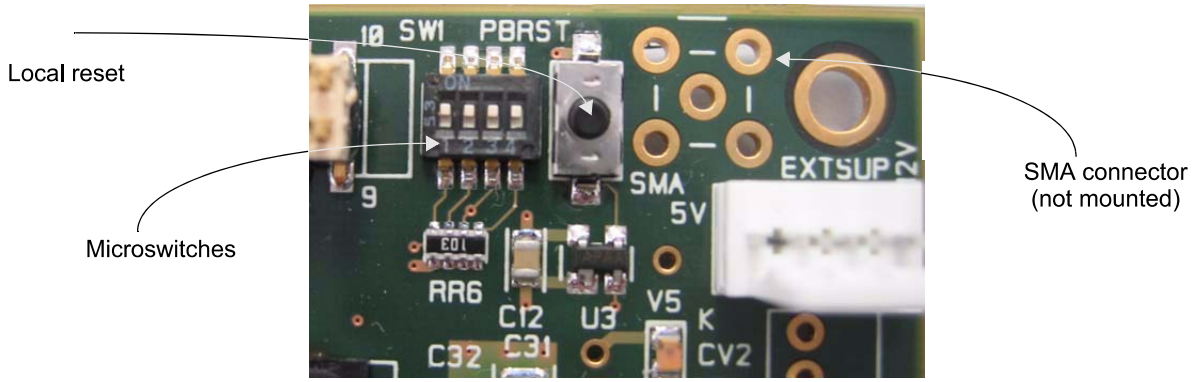


Figure 19: Photograph: SMA input, local reset button, and miscroswitches

The SMA connector permits an external signal, for example a clock, to connect to dedicated pin P4 of the Stratix device.

3.6.6 Local Reset

The PCI-X SYS includes a reset push button (Stratix pin P27) that allows you to reset internal Stratix logic. Please see Figure 19 for an image of the Local Reset button.

WARNING: Do not confuse this button with the CONF_RST button, which is used to reconfigure the CPLD (see Chapter 4 on page 47 for more information).

3.6.7 Mechanical switches

Figure 20 illustrates the architecture of the four mechanical switches available on the board. (Please see Figure 19 for an image of the microswitches.)

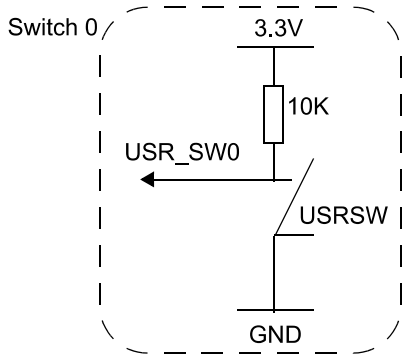


Figure 20: Architecture of the mechanical switches

Table 23 describes switch / signal assignments.

Table 23: Mechanical switches

Switch	Stratix pin	Signal
0	AF24	USR_SW0
1	AG24	USR_SW1
2	AG25	USR_SW2
3	AG26	USR_SW3

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Chapter 4 PCI-X SYS CPLD Configuration

4.1 Introduction

You can configure the Stratix device via the JTAG chain or in Fast Passive Parallel mode using the EPC16.

4.2 JTAG

The PCI-X SYS JTAG chain is comprised of 3 devices, as shown in Figure 21.

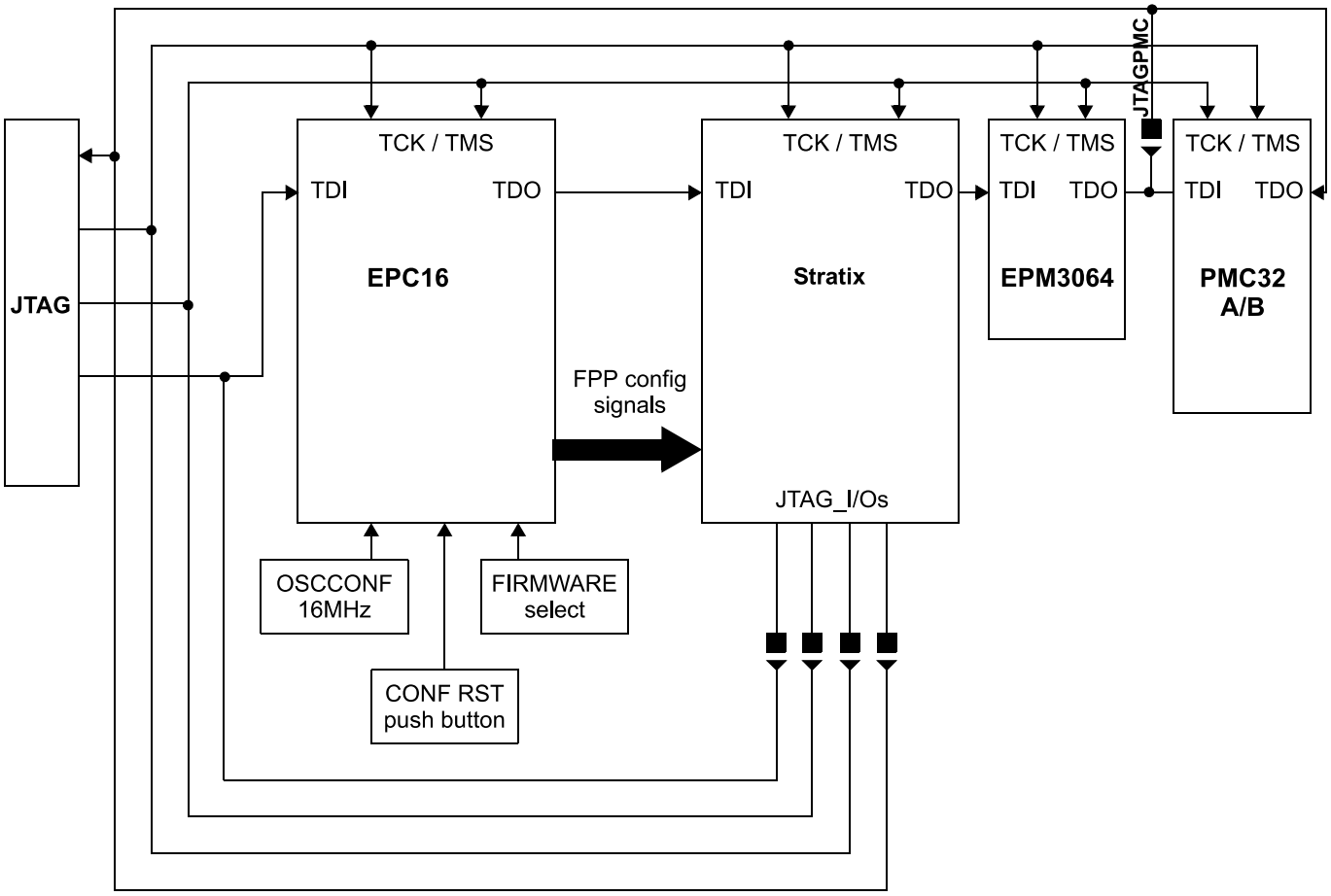


Figure 21: JTAG chain structure

The JTAG chain allows you to configure the Stratix device or the EPC16. To do so, use Altera's ByteBlaster™ or MasterBlaster™ and Altera Quartus® II software (please see www.altera.com for more details).

The JTAG signals are available on the PMC32A and PMC32B connectors, which makes possible an optional JTAG-compliant device mounted onto an optional daughter card. If there is no daughter card on the PMC connector, the JTAGPMC jumper must be soldered.

The JTAG chain can be driven via the Quartus II software or via the JAMPCI software, as described in the following section.

4.2.1 Configuring programmable devices with Quartus II

4.2.1.1 Configuring board devices

The following instructions describe how to program board devices with the ByteBlaster.

WARNING: Do not modify the EMP3064 device. Doing so will cause the board to stop functioning.

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1. Plug the ByteBlaster to the JTAG connector (the serigraphy key must match the ByteBlaster key—pin 1 to pin 1).
2. Launch Quartus II.
3. Choose **Programmer** from the **Tools** menu. The **Chain1.cdf** window appears.
4. Choose **Auto-detect** from the **Processing** menu. A list of detected devices appears, as shown in Figure 22.

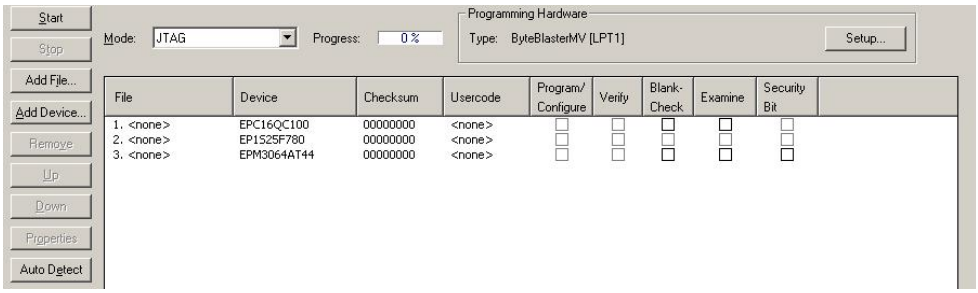


Figure 22: Screenshot: Chain1.cdf window

5. Double click the "<none>" file corresponding to the device you with to configure. The **Select New Programming File** window appears, as shown in Figure 23.
6. Select the file with which you wish to configure your device and click **Open** (the Stratix device is configured with a .sof file— tutorial1_pcixsys_v10.sof, in this example— and the EPC16 is configured with a .pof file).

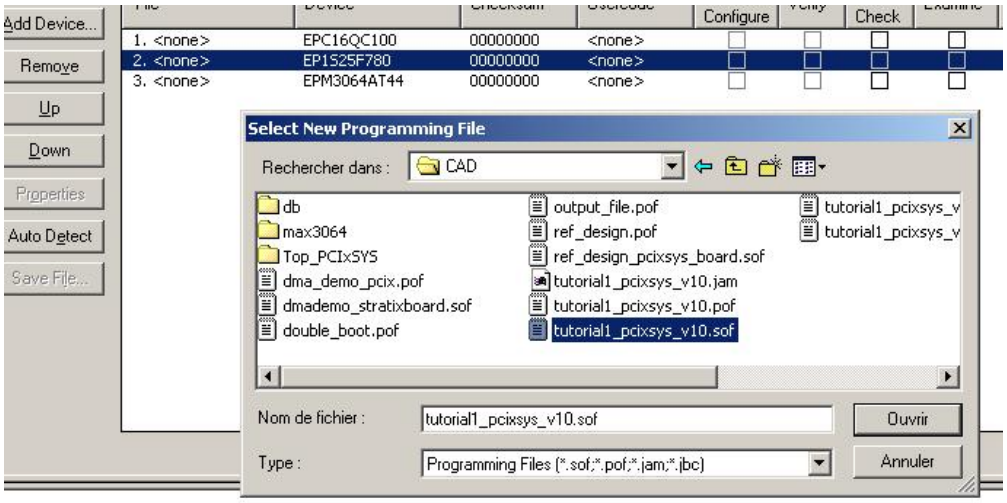


Figure 23: Screenshot: Select New Programming File

7. In the **Chain1.cdf** window, select the file you wish to use by checking the corresponding **Program/Configure** checkbox.
8. Choose **Start** from the **Processing** menu. Quartus II begins configuration of the selected device.

4.2.1.2 POF generation

If you wish to configure the EPC16, you must first generate a .pof file from the .sof file generated by Quartus II. Note that the default .pof file generated by Quartus II can not be used to program the EPC16.

The following instructions describe how to generate a .pof file for the PCI-X SYS EPC16.

1. Launch Quartus II, if it is not already running.
2. Choose **Convert Programming Files** from the **File** menu. The **Convert Programming Files** window appears.

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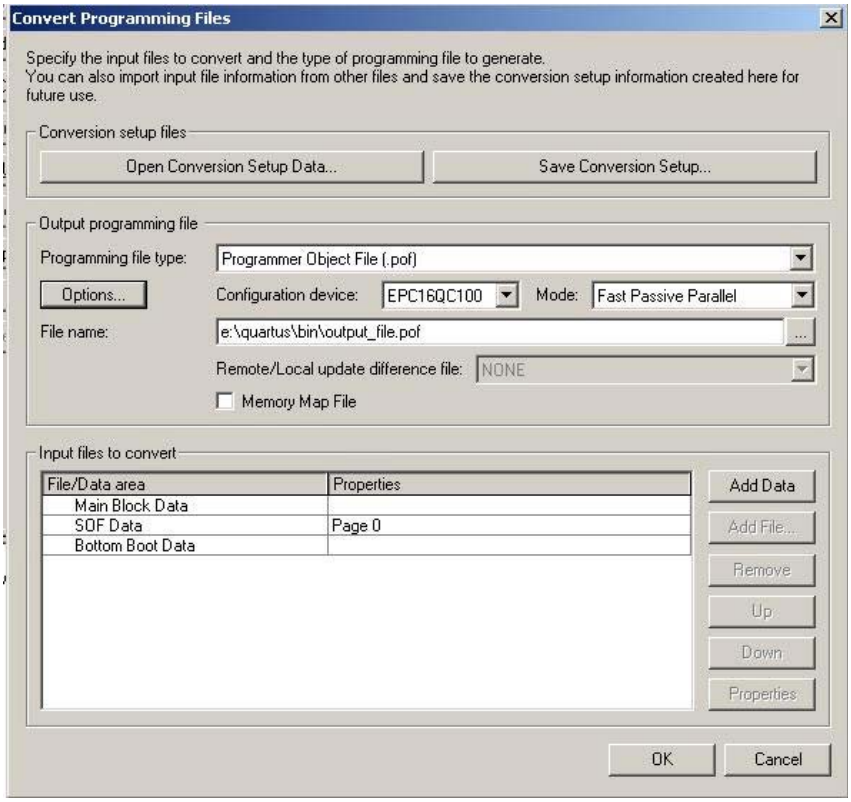


Figure 24: Screenshot: Convert Programming Files window

3. Select **Programmer Object File (.pof)** from the **Programming file type** dropdown list (as shown in Figure 24).
4. Select **EPC16QC100** from the **Configuration device** dropdown list (as shown in Figure 24).
5. Select **Fast Passive Parallel** from the **Mode** dropdown list (as shown in Figure 24).
6. Type a file name and destination in the **File Name** text box (as shown in Figure 24).
7. Select the **SOF Data** line of the **Input files to convert** menu.
8. Click **Add File**. The **Select Input File** window appears.
9. Select the desired file and click **Open**.

   Note: While not necessary, we recommend that you add a second boot sector to the EPC16 (see Section 4.3.3 for details). If you wish to ignore this recommendation, please skip to step 12.

10. Click **Add Data** to add a second Boot sector to the EPC16. A second **SOF Data** line appears in the **Input files to convert** field.
11. Repeat steps 7, 8, and 9.

    Note: A bug exists in Quartus II 3.0 or less that labels all page numbers as page 0. In order for page numbers to follow sequentially, do the following:

    - Select the second SOF data line and click **Properties**. The **SOF Data Properties** window appears.
    - Change the page number to 1 in the **Pages** field, and click **OK**.

12. Click **OK** in the main window. Quartus II generates the .pof file.

The PCI-X SYS EPC16 can now be programmed using the generated .pof file.

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4.3 Fast Passive Parallel (FPP) Stratix Configuration

4.3.1 Introduction

The EPC16 configures the Stratix device automatically when you start the system, or on command when you push the Configuration Reset (CONFRST) button (shown in Figure 25).

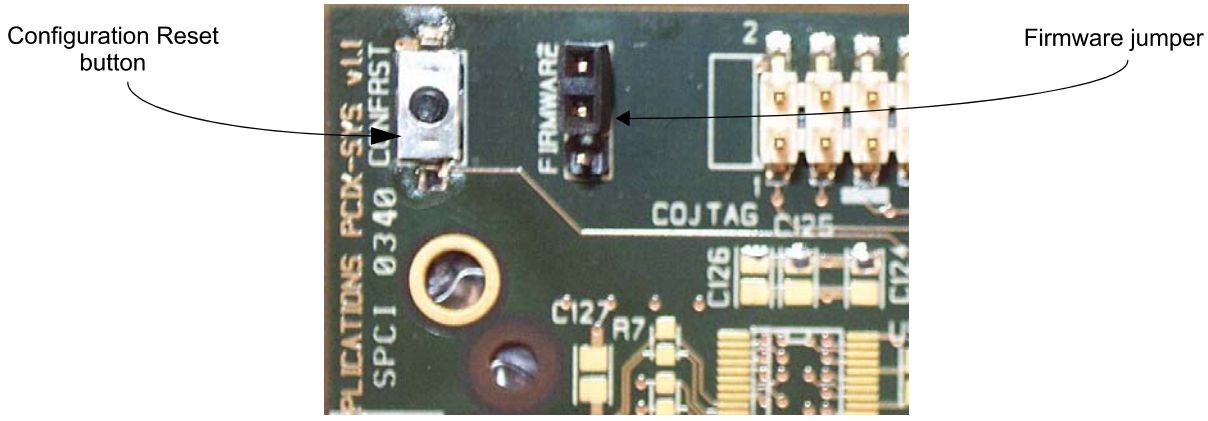


Figure 25: Photograph: Board configuration module

In FPP mode, the Stratix device receives byte-wide configuration data with each clock cycle, as determined by the PCI-X specification, which requires configuration within 100ms after power up.

4.3.2 Configuration Clock selection

You can modify the clock frequency with which the Stratix device is configured when you create the .pof file (see Section 4.2.1.2 for details). The default frequency is 10MHz, but other choices include:

- internal EPC16 clock frequencies (10 / 33 / 50 / 66MHz)
- multiples of the external 16MHz configuration clock

To change the default clock frequency, do the following:

1. Open your project in Quartus II.
2. Choose **Convert Programming Files** from the **File** menu. The **Convert Programming Files** window appears.
3. Click **Options**. The **Configuration Device Options** window appears.
4. Select a clock source from the **Clock Source** dropdown menu.
5. Select a clock frequency from the **Clock frequency** dropdown menu.
6. Click **OK**.

4.3.3 Boot sector selection

The EPC16 has enough memory to support two configuration files. The firmware jumper allows you to determine which configuration file is loaded to the Stratix device:

- To boot from sector 1, set the firmware jumper to 1.
- To boot from sector 0, set the firmware jumper to 2.

We recommend writing to both boot sectors of the EPC16 because if you accidentally boot the EPC16 from an empty sector it will stop operating, and you will need to reboot your system.

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Chapter 5 Getting Started with the PCI-X SYS board

The PCI-X SYS board comes with two reference designs that are intended to illustrate the capabilities of the board and to help you get started with your own design. Each reference design performs the following tasks:

- in Master mode, DMA shots in Direct and Scatter / Gather mode
- in Target mode, Write and Read requests made to internal SRAM
- in Target mode, access to an internal register (blinking LEDs)

5.1 Selecting a Reference Design

You can choose which design to load with the firmware jumpers, shown in Figure 25.

- **Boot sector 0**: PCI-X 66/100/133MHz and PCI-33MHz compatible
- **Boot sector 1**: PCI-33/66MHz compatible

Note that the selected reference design may not function properly if you haven't established the proper type of board (either as a PCI-X 133MHz, a PCI-X 66MHz, or a PCI board). Please see Section 3.2.2 for more details.

5.2 Testing the Reference Design

The following instructions assume that you have already installed the PCI-X / PCI Core.

In order to test the reference design, do the following:

1. Choose **Start -> Programs -> pcix_pci_core -> PCI Tools**. The PLDA PCI Tools icon appears in the Windows system tray.
2. Right-click the Tools icon and choose **Reference Design** from the menu. The **Reference Design** window appears, as shown in Figure 26.

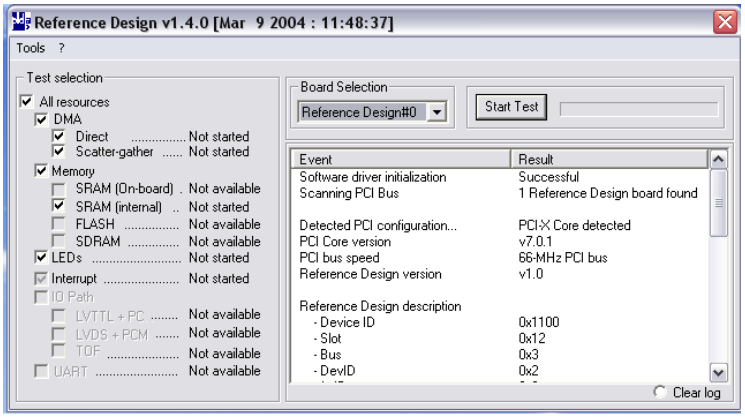


Figure 26: Screenshot: Reference Design window

3. Select the resources you would like to test.
4. Click **Start Test**.
5. Click **Yes** or **No** when prompted to confirm whether the board's LEDs indicate a successful test. Results of the test are displayed in the **Reference Design** window.

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