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IPnexus™

CPC395

CompactPCI® Dual T3/H.110 TDM Communications Controller

Hardware Guide



innovative IP communications

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CPC395 Hardware Manual part no. 126P0372

Revision History

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11	Update address and area code.		04/26/02

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Notice

This document presents information for users of Performance Technologies' CPC395 CompactPCI Dual T3/H.110 TDM Communications Controller.

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Safety Precautions

This section is provided as a summary of the safety recommendations throughout this manual. Performance Technologies, Inc., recommends that all safety precautions are followed to prevent harm to yourself or to the equipment.

- Follow all warnings and instructions marked on the equipment.
- Ensure that the voltage and frequency of your power source matches the voltage and frequency inscribed on the equipment's electrical rating label.
- Never push objects of any kind through the openings in the equipment. Dangerous voltages may be present. Conductive foreign objects could produce a short circuit that could cause fire, electrical shock, or damage the equipment.

This equipment contains a replaceable lithium SNAPHAT battery as part of the Time of Day clock device. It is located at U20.



CAUTION: To avoid draining battery, do not place SNAPHAT pins in a conductive foam.

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Symbols and Conventions in this Manual

An overbar indicates the signal is an Active Low signal.

Example: $\overline{\text{ENUM}}$

The following symbols appear in this document.



CAUTION: There is risk of personal injury or equipment damage. Follow the instructions.



WARNING: Hazardous voltages are present. To reduce the risk of electrical shock and danger to personal health, follow the instructions.

Electrostatic Discharge



CAUTION: Electronic components on printed circuit boards are extremely sensitive to static electricity. Ordinary amounts of static electricity generated by your clothing or work environment can damage the electronic equipment. It is recommended that anti-static ground straps and anti-static mats are used when installing the board in a system to help prevent damage due to electrostatic discharge.

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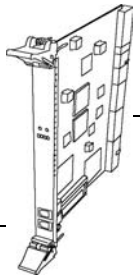
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Section

1



Introduction

This manual describes the CPC395 Dual T3/H.110 TDM Circuit Switch, which provides telecom equipment manufacturers and integrators with full switching of two DS-3 communications interfaces (1344 DS-0s) on one single or two independent H.110 buses. This chapter contains a product description, model definitions and typical applications of the CPC395.

1.1 Product Description

The CPC395 is a CompactPCI form-factor ECTF CT Bus (H.110) Interface card with dual T3 Media and dual Ethernet Control Interfaces. The CPC395 supports Hot Swap and passive rear I/O, is fully channelized, and supports full DS-0 to DS-3 multiplexing.

The CPC395 is designed to be an integral component in a wide array of Computer Telephony applications, including VoIP Gateways, Interactive Voice Response Systems, Internet Intercept Systems, Fax Servers, Automatic Call Distributors, Predictive Dialers, E-mail Voice Gateways, Signalling Gateways, etc. These applications and many others must provide an interface between the PSTN and the ECTF (Enterprise Computer Telephony Forum) Computer Telephony Bus (CT Bus).

The CT Bus provides users with a standard interface that enables inter-operability between telecom equipment vendors. This allows the user to construct a variety of telecom application solutions using off-the-shelf components. The CPC395 provides termination of two full DS-3 links to two CT bus interfaces for those applications that need to process high volumes of call traffic in as small a footprint as possible.

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Model Numbers

- PT-CPC395-11353 is configured to switch all of the 672 DS-0s on each T3 to separate H.110 buses.
- PT-CPC395-11354 is configured to switch all 1344 DS-0s from two T3 links to one H.110 CT bus.
- PT-CPC395C-11360 has a single H.110 bus and includes circuit switching software.
- PT-CPC395N-11462 has a single H.110 bus and includes NexusWare®, Performance Technologies' Linux-based development environment.

Unless otherwise indicated, use of the term CPC395 in this document refers to all available models.

There are two Line Interface Modules (LIMs) available:

- PT-LIM395-11218 has an Ethernet connection through the midplane.
- PT-LIM395-11219 has an Ethernet connection through the rear panel.

The CPC395 is shown in Figure 1.

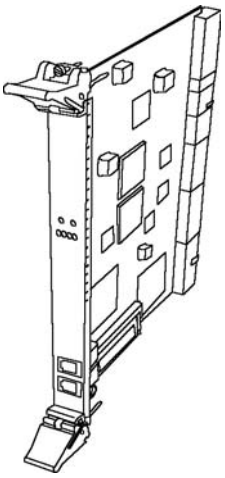


Figure 1. CPC395

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Figure 2 is a basic block diagram of the CPC395.

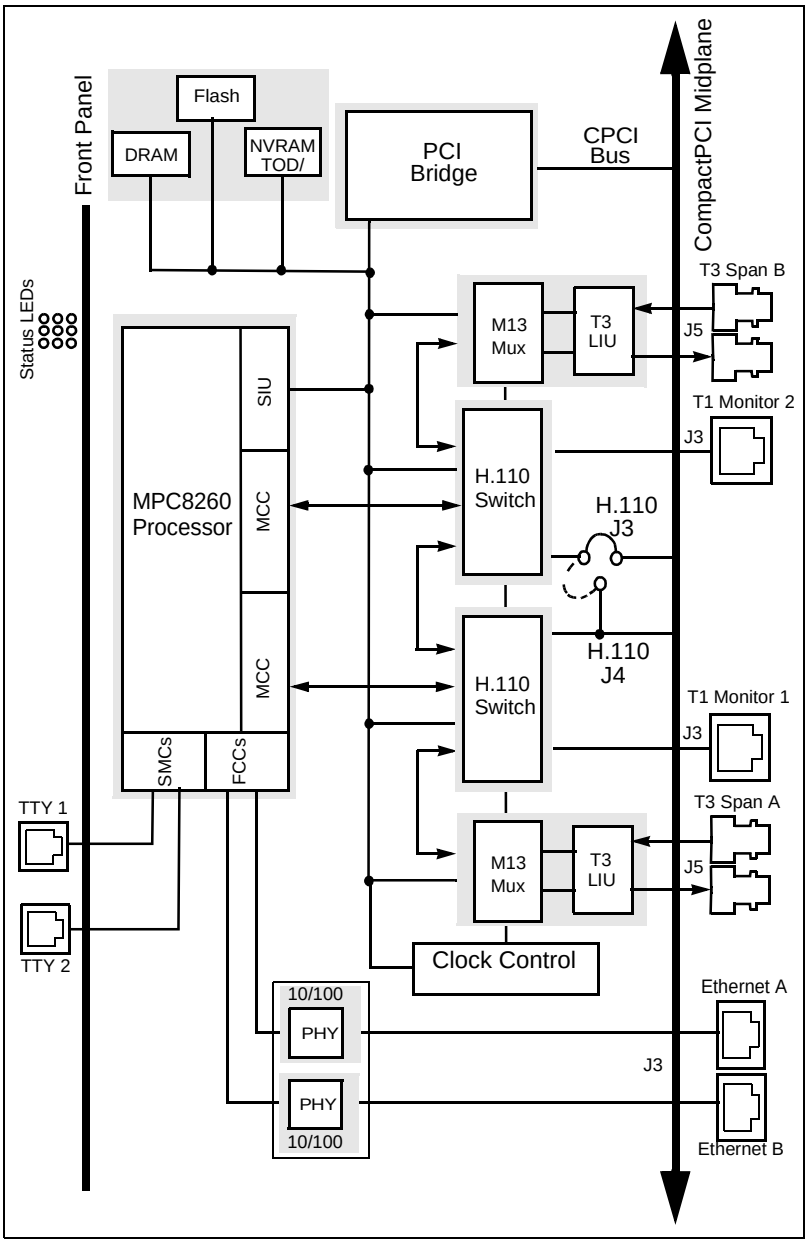


Figure 2. CPC395 Basic Block Diagram

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1.2 Feature Summary

The major features of the CPC395 include:

- Hot Swap CompactPCI 32/64 bit 33 MHz Interface
- Dual T3 LIUs and framers
- Dual ECTF H.110 controllers
- 58 T1 Framing Channels (28 per T3 plus 2 Monitors)
- Direct DS-3 to DS-0 conversion
- Dual 10/100 Base-T Ethernet ports
- Dual Serial Management Controllers
- Extensive Clocking Options
- Transport of Channel Associated Signalling

1.3 Architecture

An overview of the major functional blocks is provided here. Subsequent sections provide more detail.

Processor

The CPC395 may be used as a standalone device. All of the functionality required for the CPC395 to operate as a TDM switch is included onboard. An onboard communication processor oversees all of the functions of the CPC395. The processor used is the MPC8260 PowerQUICC II. The PowerQUICC II is a versatile communications processor that integrates, on one chip, a high performance PowerPC™ RISC microprocessor and a variety of communications peripheral controllers. The CPC395 utilizes the onchip communications peripherals for Ethernet (FCCs), Console ports (SCCs), and the Multi-channel Communication Controllers (MCCs).

MultiChannel Communication Controllers

The MCCs support processor access to up to 256 Full Duplex DS-0 channels switched via the H.110 controllers. Any set of DS-0s can be terminated from the T1 Monitor ports, T3 Trunks, or H.110 buses. The processor performs protocol processing at the DS-0, fractional T1, or full T1 level.

Serial Ports

Two serial ports are present on the CPC395. though only one is currently enabled. The second port is provided for future use. The topmost serial port on the front panel, labelled “Console,” provides for local access to the card from a VT-100-compatible ASCII terminal. This port provides access to an available Command Line Interface (CLI), giving the user access to the CPC395 functions and status.

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T3 Trunks

Two onboard T3 transceivers, composed of individual LIUs and framers, send and receive framed serialized DS-3 bit streams, recover timing information, and demultiplex DS-3 data directly to the DS-0 level. The result is dual independent sets of 672 DS-0 channels that are terminated to the two onboard H.110 controllers. The individual DS-0s of each T1 bit stream can be randomly assigned to or from any of the switched timeslots.

The CPC395 provides two T3 LIU transceivers which perform clock synchronization and data encoding and recovery for transmission over 75 ohm coaxial cable. The T3 LIUs contain a programmable “Line-Buildout” circuit and equalizer to reduce the effects of cable distortion.

The LIM card provides secondary protection circuitry against electrical hazard for the T3 trunks.

H.110 Controllers

The H.110 controllers provide switching between one or two ECTF H.110 interfaces and the local resources. The local resources include: the T3/M13 Framers, a multi-channel communication controller within the processor, the T1 Monitor ports, Channel Associated Signalling (CAS) bits, and an inter-switch link used for switching between the two H.110 controllers. Each H.110 controller can support 4096x2342 H.110 bus to local resource timeslots, 2342x2342 local resource to local resource timeslots, or 2048x2048 H.110 to H.110 timeslots.

T1 Monitor Ports

Two T1 Monitor ports, located on the rear panel Line Interface Module (LIM), provide monitoring of up to 24 DS-0s each. The T1 Monitor transceivers and line interface units provide all of the necessary functions to generate ANSI T1.403 compliant T1 bit streams. The T1 bit streams are brought out to RJ-48C connectors on the LIM. The T1 Monitor transceivers’ TDM system interfaces are connected to the local sides of the H.110 switches. The individual DS-0s of each T1 bit stream can be randomly assigned from any of the switched timeslots. Besides offering the ability to monitor timeslots, the T1 Monitor ports also provide a convenient connection point to a network timing reference that may be used to clock the H.110 buses.

Clock Control

The CPC395 supports extensive clock synchronization control, maintained by digital phase locked loop (DPLL) circuitry.

The CPC395 reference clock can be selected from any one of seven sources, including an onboard reference clock, either of the H.110 buses, clock recovered from either of the T3 interfaces, or either of the T1 Monitor ports. The Monitor ports provide a convenient interface to a local BITS (Building Integrated Timing Supply) clock source.

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The CPC395 can be configured as an H.110 clock Master or Slave, and supports all clock fallback features defined in the ECTF H.110 specification. Any of the network interfaces may be configured to provide a network reference, including the T1 Monitor ports.

CompactPCI Interface

The CPC395 supports a fully compliant 33MHz 32/64 bit CompactPCI bus interface for local bus-based management and/or high speed data movement applications.

Ethernet Ports

Two Ethernet ports are provided on the CPC395 for management purposes. The CPC395 supports mid-plane Ethernet wiring, allowing for the cablefree interconnect between the CPC395 and other CompactPCI-based Ethernet components such as the CPC4400 Ethernet switch.

Two modes of operation are supported by the Ethernet subsystem: dual independent subnet and dual-homed shared subnet. In the dual subnet configuration, each port provides access to a separate subnet. In this mode, the CPC395 is configured with two IP addresses and two Ethernet MAC Addresses. The CPC395 can be configured as a gateway in dual subnet mode.

In single-subnet, dual-homing mode, the CPC395 is configured with one IP address and one MAC Address. The CPC395 will use only one of the ports at a time. Port 1 is the primary port and the CPC395 will always use that port if it is available. If port 1 loses link, the CPC395 will automatically switch to port 2 within 500ms. While the secondary port is in stand-by mode, it will not establish a link with its peer.

1.4 Diagnostics

The diagnostic facilities of the CPC395 support a Power On Confidence test suite (POC), continuous network validation through detection of alarms and faults, and a set of online utilities that provide for extensive network level diagnostics.

Power-On Confidence (POC)

POC tests are a diagnostic suite that is run whenever the CPC395 is booted. POC tests are enabled by default, but the CPC395 also provides a method to disable them. The POC test suite includes only those diagnostic tests that do not affect externally attached devices. The CPC395 becomes available to the user within 30 seconds of a power-on or reset.

Watchdog Timer

The CPC395 includes a hardware Watchdog timer that must be refreshed by the processor at a preset frequency. If the processor is unable to service the watchdog, this indicates that the CPC395 has become unreliable and is reset. The user may elect to force a reboot upon this event or take the board out of service.

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1.5 Available Management and Development Software

The CPC395C and CPC395N provide a variety of software management and development options.

TDM Circuit Switch Software (CPC395C)

Command Line Interface (CLI)

The CPC395C provides a Command Line Interface (CLI) via either RS-232 TTY port or via Telnet over the Ethernet ports. The CLI provides the following:

- An initial configuration interface
- A simple and efficient management user interface
- Access to diagnostic utilities

The command list and user information is provided in the User's and System Integrator's Guide.

CompactPCI Device Drivers

Local CompactPCI-based hosts may manage the CPC395C through a standardized API interface. Host-resident applications wishing to access features on the CPC395C can link with the appropriate API library. Device drivers for Windows NT, Solaris, and Linux will be available.

Remote TCP/IP-Based API

The CPC395C supports a remote TCP/IP-based API interface for Windows NT, Solaris, and Linux. Using this API, the user may create a remote application allowing management of the CPC395C hardware. See "Application Programming Interface" in the User's and System Integrator's Guide.

SNMP

The CPC395C SNMP agent is a version 1/2C/3 implementation. The agent responds to a defined set of SNMP client requests and generates the appropriate traps to respond to events. All mandatory parameters for the following MIBs are provided:

- MIB II (RFC 1213)
- DS-1 MIB (RFC 2495)
- DS-3 MIB (RFC 2496)
- Performance Technologies Enterprise MIB for extended monitoring, configuration, and H.110 circuit setup.

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NexusWare® (CPC395N)

NexusWare is a Linux-based development, integration, and management environment. It features an integrated suite of carrier-grade device drivers for full access to onboard resources (H.110, Ethernet, PCI, T3, T1/E1/J1) as well as a powerful NexusWare API. The NexusWare API provides a common interface for application development and allows system integration using either the PCI bus or the PICMG 2.16 CompactPCI/PSB architecture.

1.6 Additional Documentation

This manual is not intended to be a stand-alone document. Following are additional sources of information which can provide a complete understanding of all the features and functions of the CPC395 hardware:

SODIMM Memory 128 MByte 100 MHz Datasheet

SL64G6F16M8G - A10DV Silicon Tech, 3009 Daimler St.,
Santa Ana, CA 92705, U.S.A. Tel: 949-476-1130
More information at:
http://www.silicontech.com/pdf/611033c2.pdf

PEB2256 FALC, QFP80 Datasheet

PEB2256 Infineon Technologies, 79 T.W. Alexander Drive, 4101 Research Commons Suite 200, Research Triangle Park, NC 27709-0006, U.S.A.,
Tel: 208-368-3900
More information at:
http://www.infineon.com/cgi/ecrm.dll/ecrm/scripts/prod_ov.jsp?oid=13588

XPC8260 PowerQUICC II, MPC8260 POWERQUICC II User's Manual

MPC8260UM/D, Rev 0, Motorola Incorporated, Motorola Literature
Distribution Center, P.O.Box 5405, Denver, Colorado 80217, U.S.A.Tel: (800) 441-2447
More information at:
http://merchant.hibbertco.com/servlet/mtrlext.MtrlExtServlet?tp=pdf&cpn=MPC8260UM/D

CA91L8200 Tundra Power Span Datasheet

CA91L8200-100CEZ Tundra Semiconductor Corporation, 603 March Road, Kanata, Ontario, Canada, K2K 2M5,Tel: 613 592 0714
More information at:
http://www.tundra.com/page.cfm?tree_id=100008

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MT90866 H.110 Switch LQFP Data Sheet

MT-90866 Mitel Semiconductor, 360 Legget Drive, Kanata, ON K2K 2W7, Canada, Tel: (613) 592-2122
More information at:
http://www.mitelsemi.com/index.htm

Specifications

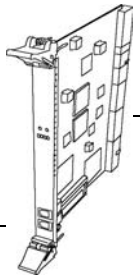
- CompactPCI Specification, PICMG 2.0 R3.0
- CompactPCI Computer Telephony Specification, PICMG 2.5 R1.0 Oct 25, 1999.
- ECTF H.110 Hardware Compatibility Specification revision 1.0.

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Section

2



Installation

This section describes the installation and initial setup of the CPC395.

Electrostatic Discharge

CAUTION: Electronic components on printed circuit boards are extremely sensitive to static electricity. Ordinary amounts of static electricity generated by your clothing or work environment can damage the electronic equipment. When installing the board in a system, anti-static grounding straps and anti-static mats must be used in order to prevent damage due to electrostatic discharge.

2.1 Board Jumpers

There are several jumpers on the board. Refer to the following sections to determine jumper functions and appropriate settings.

NOTE: To prevent losing the jumper when it is not required on a particular header, hang the jumper off one of the pins, as shown:



Jumper Settings

Refer to Table 1 for a summary of board jumper options.

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Table 1. Jumper Options

Jumper	Description	Factory Setting
K1[1]	RESERVED	OUT
K2	USE COMPUTER TELEPHONY RESET (CT_RESET) IN = The CT_RESET signal will reset the board OUT = The CT_RESET signal will not reset the board	IN
K3[1]	RESERVED	IN
K4[1]	RESERVED	OUT
K5[2]	BDSEL POWER CONTROLLER ENABLE: IN = CPCI Board Select signal enables Hot Swap Power Controller OUT = Hot Swap Power Controller not under CPCI Board Select control.	IN
K6[2]	CTBUS POWER CONTROLLER ENABLE: IN = A side CT Bus Enable (CT_EN) controls Hot Swap Power Controller OUT = Hot Swap Power Controller not under CPCI A side CT Bus Enable (CT_EN) control.	OUT
K7[2]	STANDALONE POWER CONTROLLER: IN = Hot Swap Power Controller enabled on presence of CompactPCI power OUT = Hot Swap Power Controller not in Standalone mode	OUT
K8[1]	RESERVED	IN
K9	CT BUS RESET MASTER: IN = The CPC395 drives CT_RESET when it detects PCI RESET OUT = The CPC395 does not drive CT_RESET	IN
K10	BREAK DETECT: IN = Break Detect on Serial Port causes board reset. Used for Debugging only. OUT = Break Detect Reset is disabled..	OUT
K11	AUTO FUNCTION JUMPER: IN = Application Flash Boot OUT = Diagnostic Boot	OUT
K12	PQRESET - POWER QUICK 2 RESET: IN = Manually holds the MPC8260 processor in reset OUT = MPC8260 processor is not held in reset	OUT
K13	STANDALONE 33 MHz CLOCK ENABLE: IN = Enable Standalone Clock circuit (K18 must be 1-2) OUT = Disable Standalone Clock circuit	IN

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Table 1. Jumper Options *(Continued)*

Jumper	Description	Factory Setting
K14	ABORT: IN = Manual generation of ABORT - used for debugging only OUT = Negate manual generation of ABORT	OUT
K15	CPCI CONTROLLER PRECHARGE ENABLE 0.9 Volts: IN = enable precharge of PCI bus OUT = disable precharge of PCI bus	IN
K16	CT BUS I/O LOGIC PRECHARGE ENABLE 0.7 Volts: IN = enable precharge of CT bus OUT = disable precharge of CT bus	IN
K17	M66EN OVERRIDE: IN = Force 66 MHz operation - Connects CPCI /M66EN to Ground onnboard. The CPCI /M66EN signal is also driven low to the CPCI bus. OUT = Select speed according to the /M66EN signal received from the CPCI bus	OUT
K18	CPCI CLOCK SELECT: Pins 1-2 IN = Use Onboard 33 MHz standalone clocking. (K13 must be IN) Pins 2-3 IN = Use CPCI system bus clock	2-3
P4	BOOT PROM ENABLE: Pins 1 to 2 IN = MPC8260 loads default Reset Configuration Word. Used for factory configuration only. Pins 2 to 3 IN = MPC8260 loads Reset Configuration Word from Boot PROM.	2-3

1. These jumper options are Reserved and should not be modified.
2. Select one Power Control Enable (K5-K7) setting only.

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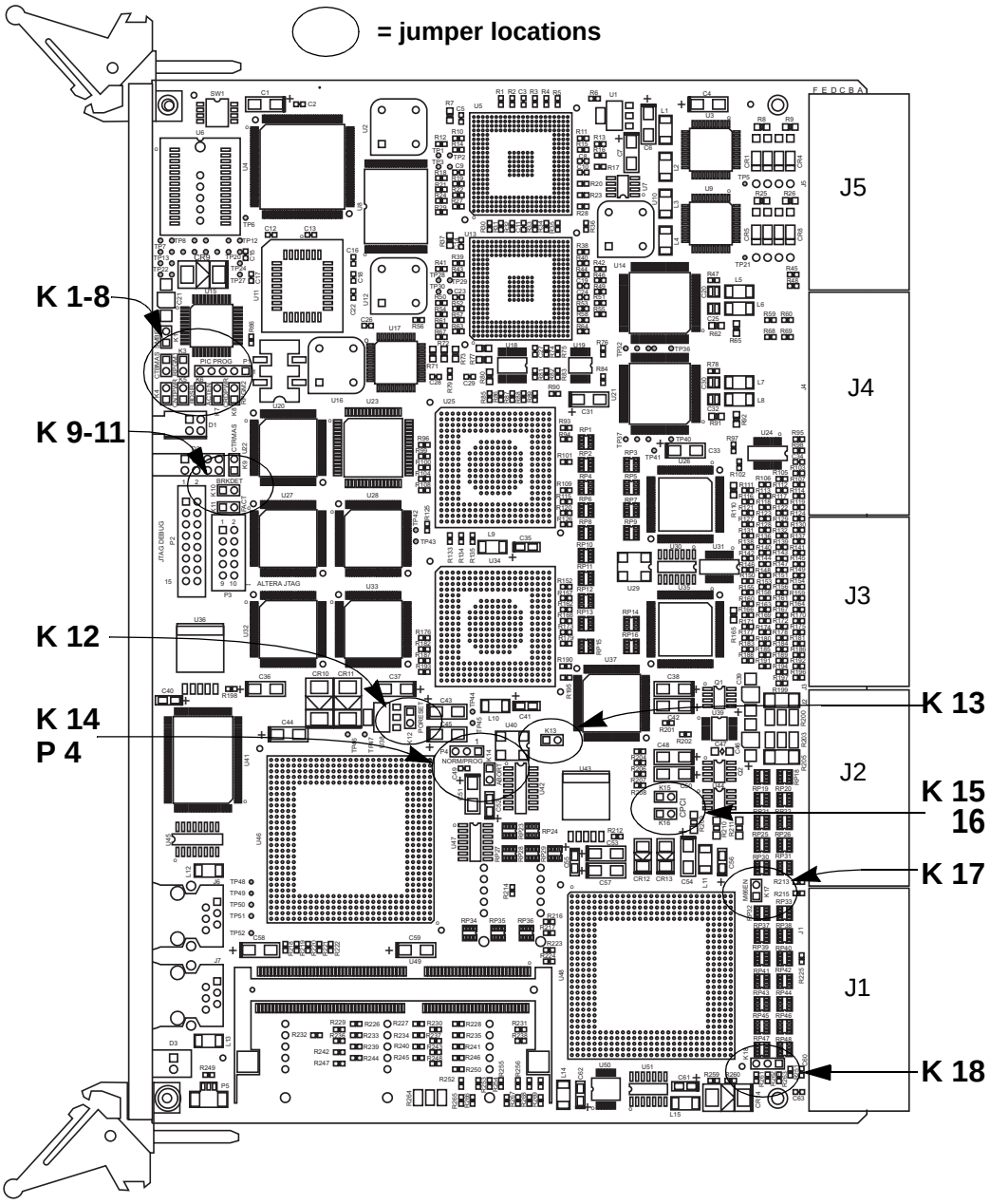


Figure 3. CPC395 Board Layout

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Board Status LEDs (page 16)

T3 A and B Trunk Port LEDs (page 17)

Console Port (page 23)

Serial 2 Port

Hot-Swap LED (pages 17 and 21)

Figure 4. CPC395 Front Panel

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2.2 Front Panel LEDs

The LEDs on the front panel include:

- Board Status LEDs
- T3 Trunk Port LEDs
- Hot Swap LED

See Figure 4 on page 15.

Board Status LEDs

Two LEDs provide board level status information.

- A bi-color (green-yellow) LED provides *System* status on the front panel.
- A red LED provides *Fault* status on the front panel.

On power-up, the System LED is yellow. After the basic board integrity checks are complete the System LED changes to green.

The System LED normally remains green unless a board failure is detected that turns the LED OFF, or the board is in a boot-up state. See Table 2.

Table 2. Board Status System LED

LED State or Color	State Indication
Green	Board is alive
Yellow	Board is Booting
OFF	No Power or Serious Fault

The Fault LED is OFF unless a serious internal error is detected, when it is RED. See Table 3.

Table 3. Board Status Fault LED

LED State or Color	State Indication
Red	Fault
OFF	No fault or no power

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T3 Trunk Port LEDs

The status of each T3 Interface is indicated by LEDs visible from the front panel. Refer to Table 4

Table 4. T3 Trunk Link/Activity LED

LED State	PortIndication
Green ON	Framed
Flashing Green	Activity
OFF	No Link

Hot Swap LED

The blue Hot Swap LED is used to signal that the board has been partially inserted or removed from the chassis. When the blue Hot Swap LED is ON, the electrical separation is currently in process.

Refer to “Hot Swap Chassis Install and Replacement” on page 21 for board removal and insertion instructions.

2.3 LIM Front Panel LEDs

The LEDs on the front panel of both LIMs include:

- Ethernet Port LEDs

For diagrams of the LIM front panels, see pages 18 and 19.

Ethernet Port LEDs

The status of each Ethernet interface is indicated by LEDs visible from the rear panel, as shown in Table 5.

Table 5. Ethernet Port Link/Activity LED

LED State	PortIndication
Green ON	Framed
Flashing Green	Activity
OFF	No Link

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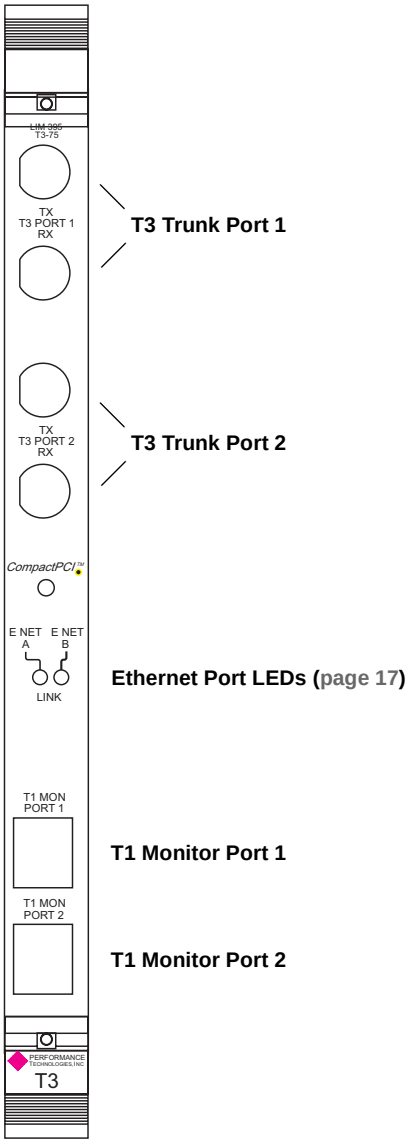


Figure 5. CPC395 Internal Ethernet LIM Panel

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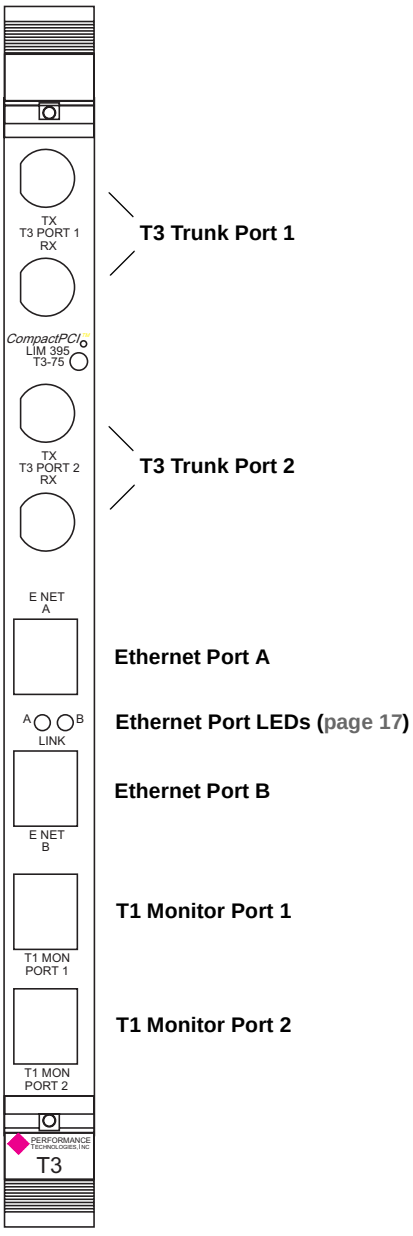


Figure 6. CPC395 External Ethernet LIM Panel

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2.4 Physical Installation

A typical CompactPCI chassis is shown in Figure 7

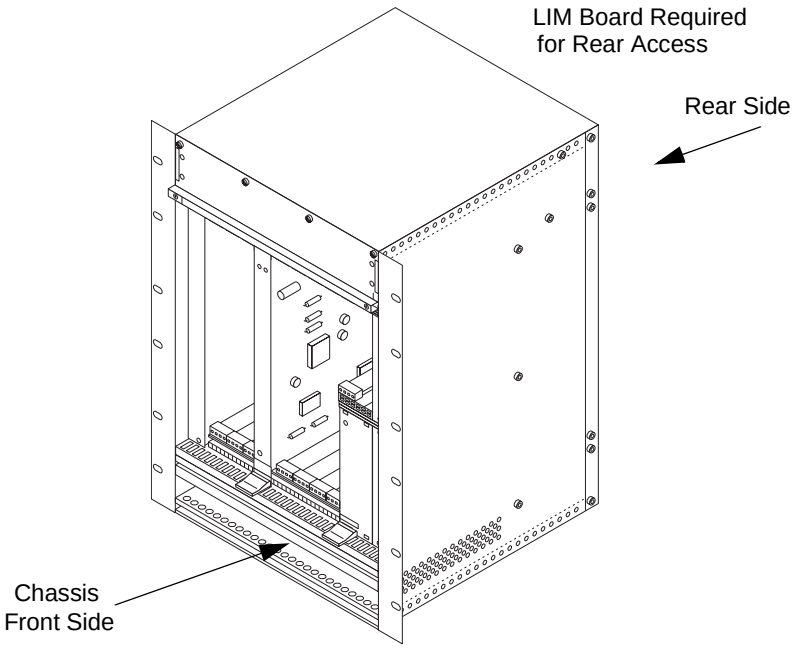


Figure 7. Typical CompactPCI Chassis

Non-Hot-Swap Chassis Install

1. Quit all applications. Power down the CompactPCI chassis and any attached peripherals.
2. Configure the CPC395 hardware. See "Board Jumpers" on page 11 for a description of setup issues and jumper configuration procedures.

   Ensure that if BDSEL# is not supported on the backplane, Jumper K5 is OUT and that either K6 or K7 is IN.
3. Select an available 6U, 32-bit (or 64-bit) CompactPCI slot.
4. Cock the ejector handles into the open position and slide the CPC395 into the chassis. Make sure the front plate on the board mounts flush with the chassis panel opening by using the ejector/injector handle to firmly seat the card by locking the ejectors into the latched position.
5. Secure the front plate screws (one at the top of the card and another under the ejector/injector handle) to secure the card into the chassis. This also provides a chassis ground connection to the CPC395.

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6. Install the appropriate LIM rear access board into the chassis in the rear I/O slot associated with the board slot, if required.
7. Re-connect any cables from the peripheral devices.
8. This completes the hardware installation. At this point, turn power back on to the CompactPCI chassis and proceed to any software installation instructions that may have been provided.

Hot Swap Chassis Install and Replacement

The following procedure assumes the chassis power is on and the host supports Hot Swap capabilities.

NOTE: If a LIM rear access board is used, the chassis must be powered down to install the LIM board. There is not sufficient card guidance on the rear panel slots to prevent mis-alignment.

Installation

1. Configure the CPC395 hardware. See "Board Jumpers" on page 11 for a description of setup issues and jumper configuration procedures.

   Ensure that if BDSEL# is not supported on the backplane, jumper K5 is OUT and one of K6, or K7 is IN. If the backplane drives BDSEL#, then install jumper K5.
2. Select an available 6U, 32-bit (or 64-bit) CompactPCI slot.
3. Cock the ejector handles into the open position and slide the board into the chassis. Ensure the front plate on the board mounts flush with the chassis panel opening by using the ejector/injector handle to firmly seat the card by locking the ejector/injector into the latched position.

   When the board makes contact with the CompactPCI backplane, the blue Hot Swap LED turns ON and the hardware connection process begins. When the hardware connection process is complete the blue Hot Swap LED turns OFF.
4. Tighten the front plate screws to secure the board to the chassis. The screws also provide an electrical ground function.
5. Install the appropriate LIM rear access board into the chassis in the rear I/O slot associated with the board just installed.
6. Install the port cables to the LIM board connectors.
7. Reconnect any cables from the peripheral devices.

Extraction

1. Unscrew the front plate screws.
2. Open the ejector/injector handle just enough to unlock the handle but not enough to actually remove the board. This closes the ejector/injector handle switch causing assertion of the interrupt to the host and sets the Status Indicator and the blue Hot Swap LED turns ON.
3. After the blue Hot Swap LED is ON, open the ejector/injector handle fully to unseat the card and remove it from the chassis.

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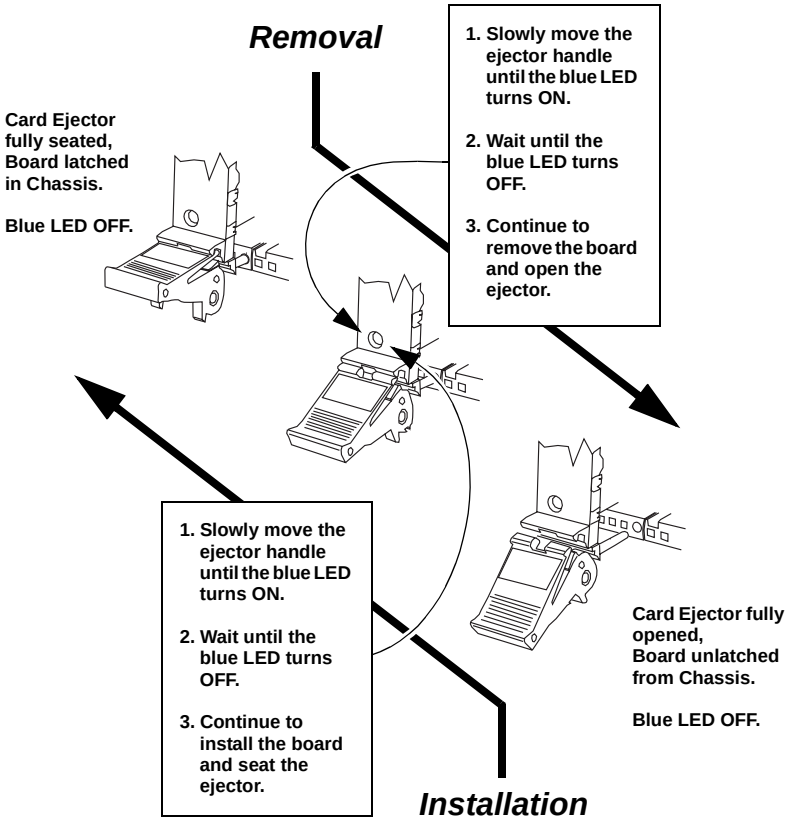


Figure 8. Hot Swap Installation and Removal Sequence

2.5 MAC Address Identification

The CPC395 has a unique MAC Address on each of its Ethernet ports. There are 2 addresses allocated to each board. These addresses are *not* sequential when viewed in Ethernet bit order. They are derived from a sequential list of Token-Ring format MAC addresses (this is due to company history and the manufacturing process). Token Ring format MAC Addresses are formed from Ethernet addresses by swapping the order of the bits within each byte of the address (bit 0 becomes bit 7, bit 1 becomes bit 6, etc).

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The MAC addresses are printed on a label located on the underside of the CPC395. If you know the MAC address of one port, you can derive the MAC Address of the other. To calculate the MAC Address of Ethernet B, you need to convert the address of Ethernet A to Token-Ring format, add 1, and convert it back to Ethernet order. Ethernet A's MAC Address can be derived by subtracting one from B's Token-Ring format.

For example, if the address of Ethernet A is 00 c0 8c 01 10 00, then the following table shows the addresses assigned to each port.

Table 6. Example of MAC Address Identification

Port Number	Token Ring Format	Ethernet Format
ENET A	00 03 31 80 08 00	00 c0 8c 01 10 00
ENET B	00 03 31 80 08 01	00 c0 8c 01 10 80

2.6 Initial Setup

Prior to connecting the CPC395 to your network, you should establish a compatible configuration. If network management is desired, this configuration must include, at a minimum, setting up the IP Address of the Ethernet interface(s). This may be done automatically through DHCP. The CPC395 is shipped with DHCP enabled.

If you do not wish to use DHCP, you must configure the network manually. Since the board is not yet attached to the network, this initial setup must be done through the console port. Refer to the following sections.

Console Port Connection

Connection to the console port is used for direct local management.The Console port uses RS-232 compatible signal levels. The terminal (or terminal emulator) connected to the console port must be configured as follows:

- Baud rate — 9600
- Data bits — 8
- Stop bit — 1
- Parity — None
- Flow control — XON/XOFF
- VT-100 Terminal Compatible

The Console port pinout is shown in "RS-232 Console Port" on page 170.

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Boot Process

The boot process is composed of the following steps:

- Power On Confidence (POC)
- Board Initialization

Power-On Confidence

After applying power to the CPC395, the switch executes the suite of Power On Confidence (POC) diagnostic tests. During the POC, all ports are temporarily disabled.

CPC395 Initialization

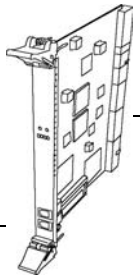
After completion of the POC tests, the CPC395 undergoes initialization.

- If no boot script has been configured, the management interface will display the default Forth prompt: OK.
- If the CPC395 has been configured to run a boot script, the application will load and display an appropriate login prompt.

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Section

3



Functional Description

This chapter provides detailed descriptions of the various functions available on the CPC395. Following the Overview, Table 7 lists the individual topics and the page number for each.

3.1 Overview

The CPC395 is a universal I/O board (i.e., there is no key on the J1 connector), and accepts either 5.0 vdc or 3.3 vdc for the PCI I/O signals.

Physically, the CPC395 is composed of a CompactPCI main card and a rear Line Interface Module (LIM). T3 digital bit streams enter and exit through the LIM. The LIM provides connectivity and line protection between the main card and the receive/transmit metallic BNC connectors. The LIM contains only passive components, including the receive/transmit galvanic isolation and line-side lightning protection.

The main card contains all of the active components:

- T3 LIUs (line interface units)
- framers
- ECTF H.110 controllers
- CompactPCI Hot Swap bus interface
- MPC8260 processor
- memory

Because the current Computer Telephony CompactPCI specification defines support for only a single H.110 presence on J4/P4, a second independent H.110 interface is implemented on J3/P3 with a pinout that is a subset of the J4/P4 H.110 signals.

Two onboard T3 transceivers, composed of individual LIUs and framers, receive and transmit framed, serialized DS-3 bit streams, recover timing information, and demultiplex DS-3 data directly to the DS-0 level. The result is dual independent sets of 672 DS-0 timeslots that may be sourced from or terminated to the H.110 bus.

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In the receive direction, the LIUs accept T3 bipolar signals, perform equalization, and convert the signals into binary digital data streams. The framers perform receive-frame synchronization, data recovery, frame overhead extraction, and provide data connection paths to the H.110 controllers.

In the transmit direction, the framers accept digital data from the H.110 controllers. The framers perform frame generation overhead insertion, and create binary digital data streams that are passed to the LIUs. The LIUs convert digital clock signals and data received from the framers to the appropriate wave shapes for transmission as bipolar T3 streams.

The H.110 controllers provide two fully compliant ECTF H.110 interfaces. Each controller can assign up to 2432 unidirectional local-to-local timeslots, or 2432 unidirectional local-to-4096 H.110 external timeslots. Each H.110 controller interfaces 18 local I/O lines, with a throughput of up to 8.192 Mbps per line, to the T3 framer, the T1 monitor port, or the other H.110 controller. Because the H.110 controller's switching capacity is fixed at 2432 timeslots, the switch connections in the accompanying block diagram represent the maximum number of connections that can be made to each specific block, and not the total number of connections that can be made on the entire card. For example, if 672 bi-directional timeslots (1344 connections) were allocated to and from a T3 framer as a local-to-local connection, then 1088 (2432 minus 1344) connections would still be available for other local resources, such as the local side connection to the other H.110 controller.

Two T1 monitor ports, located on the LIM, are switch-accessed and provide monitoring of up to 24 DS-0s each. The T1 monitor transceivers and line interface units provide all of the necessary functions to generate ANSI T1.403-compliant T1 bit streams. The T1 bit streams are brought out to RJ-48C connectors on the CPC395 front panel. The local sides of the T1 monitor transceivers are connected to the local sides of the H.110 switches. The individual DS-0s of each T1 bit stream can be randomly assigned from any of the internally or externally switched timeslots.

Clock synchronization is maintained by circuitry that contains a digital phase locked loop (DPLL), which provides timing and synchronization signals for the T3 interfaces and the H.110 controllers. The CPC395 reference clock can be selected from any one of seven sources: an onboard reference clock, either of the H.110 buses, clock recovered from either of the T3 interfaces, or either of the T1 Monitor ports. Additionally the clock source can be generated internally and can provide clocking for the entire card cage via the H.110 controller in master clock mode.

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Table 7. Topic List

Topic	Page	Topic	Page
Power Distribution	pg. 27	TDM Clock Distribution and Control	pg. 74
Reset Logic	pg. 29	H.110 Buses and Local TDM Switches	pg. 80
General CPU Section	pg. 32	Interswitch Elastic Store	pg. 91
SDRAM	pg. 47	MPC8260 TDM Multiplexer	pg. 93
Boot Flash Memory	pg. 56	T3/M13 Multiplexer Framers and Line Interface Units (LIUs)	pg. 94
Application Flash Memory	pg. 59	T3/T1 Synchronization and Clock Recovery	pg. 96
Time of Day Timer	pg. 62	TEMUX T3 Framer / M13 Multiplexer	pg. 97
Communications Buffer Memory	pg. 64	T1 28 Channel Framer	pg. 101
CompactPCI Interface	pg. 67	T1 A/B FALC Monitor Ports	pg. 102
Fast Ethernet Controller	pg. 71	General Purpose Status and Control Registers	pg. 111

3.2 Power Distribution

The power distribution network on the CPC395 starts with the contact pins on the CompactPCI backplane. The power pins are connected per the CompactPCI Specification (PICMG 2.0 R3.0) recommendation. The pins are staged per the CompactPCI Hot Swap Specification (PICMG 2.1 R1.0) so that Ground makes first and then the various voltages. Among them are 3.3V, 5V, +12 and -12V.

The power control is accomplished using the LTC1643L Hot Swap controller. The LTC1643 allows the board to be safely inserted and removed from a live PCI-Bus slot. The LTC1643 controls external N-channel transistors to provide the high current control for the 3.3V and 5V supplies while on-chip switches control the -12V and +12V supplies. All supply voltages can be ramped up at a programmable rate. An electronic circuit breaker protects all four supplies against overcurrent faults. A foldback current limit feature limits current spikes and power dissipation when shorts occur and allows the board's large capacitances to be powered up without tripping the circuit breaker. The PWRGD output indicates when all of the supply voltages are within tolerance and the FAULT output indicates an overcurrent condition.

The $\overline{\text{ON}}$ pin is used to cycle the board power or reset the circuit breaker. The $\overline{\text{ON}}$ pin is controlled by one of several startup control signals. The sources are outlined in the following table.

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Table 8. Startup Control Signals

Signal Name	Function
$\overline{\text{CNT_PWR}}$	This input is selected by jumpering K4-1 to 2. This signal is generated by the SMB controller and should only be selected if the SMB bus is configured and active.
$\overline{\text{P1_BD_SEL}}$	This input is selected by jumpering K5-1 to 2. This signal is generated by the CompactPCI backplane Hot Swap controller. It is used when this device is to be controlled by the CompactPCI bus Host.
$\overline{\text{CT_EN}}$	This input is selected by jumpering K6-1 to 2. It is used when there is no CompactPCI bus in the system and the Computer Telephony bus is the master of the backplane.
LOCAL	This setting is selected by jumpering K7-1 to 2. This setting turns the board power on as soon as the board is plugged into a powered backplane. It is used to bypass all of the above modes.

The power distribution system has bypass capacitance at several points in the system. The un-switched portion of the distribution circuit, connected directly to the CompactPCI, has a limited amount of bulk and high frequency bypass as directed by the CompactPCI specification. The switched portion of the board, or "back end," has much more distributed capacitance. As a rule, a .1uf cap is used for every +5V and 3.3V power pin to each IC. This rule is observed unless there is a placement or routing conflict that demands otherwise. There is sufficient bulk capacitance distributed about the board on each of the power planes, (+5, +3.3, +12 and –12).

There are also some chip-specific voltages generated on the board. These voltages were created for various reasons: either they weren't available on the backplane, or the chips may require them to be changed to lower values in the future, or isolated voltages are required to maintain a "noise free" supply to transceiver chips, PLLs, etc.

Table 9. Local Voltages

Signal Name	Function
VCORE_PQ	This is the voltage required by the MPC8260 core. This voltage is 2.5 volts for the A and B.X revisions of the part. It is distributed on a sub-plane.
VCORE_PCI	This is the voltage required by the Tundra PCI bridge. This voltage is 2.5 volts for the A revision of the part. It is distributed on a sub-plane

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Table 9. Local Voltages *(Continued)*

Signal Name	Function
.9V Precharge	This voltage is used to precharge the CompactPCI interface for hot plug in and hot swapping. The precharge voltage is .9V, ±.1V per the Tundra specification. Jumper K38-1 to K38-2 when installed, directs an LMC6582 OP-AMP to create the voltage via a resistor chain. The jumper may be removed if there is no CompactPCI bus in the system. This allows the precharge voltage to be driven high causing the CompactPCI inputs on the Tundra chip to be driven false. This voltage is distributed on a sub-plane.
.7V Precharge	This voltage is used to precharge the CT bus interface for hot plug in and hot swapping. The precharge voltage is .7V, ±.1V per the Computer Telephony and CompactPCI specifications. Jumper K39-3 to K39-4 when installed, directs an LMC6582 OP-AMP to create the voltage via a resistor chain. The jumper may be removed if there is no CT bus in the system. This allows the precharge voltage to be driven high causing the CT bus inputs on the H.110 switch chip to be driven false. This voltage is distributed on a sub-plane

3.3 Reset Logic

The reset logic for the board has many components. There are power-on, hard, and soft resets. There are resets caused by the external buses, time of day timer/watchdog and the System Management Bus. Each of these will be discussed in the following sections.

Power-On Reset

A Dallas DS1233A initiates the power-on reset sequence for the board. The device senses the 3.3V backend power and issues a $\overline{\text{PORESET}}$ to the MPC8260 and the Tundra PCI bridge. The DS1233A provides a 350ms reset pulse after the 3.3V power settles to an intolerance condition. It will also signal $\overline{\text{PORESET}}$ if there is a brownout condition. In addition to the CPU and bridge, the signal is provided to all of the FALC JTAG resets, the PSM502 PAL for the PAL reset logic and it has a pin on the J10 Mictor for connection to an analyzer.

The device also will de-bounce a pushbutton or jumper on its output. This feature is supported in the design with jumper K12. Shorting K12-1 to K12-2 will cause a debounced $\overline{\text{PORESET}}$ to be issued from the part.

Hard Reset

The hard reset signal, $\overline{\text{PQ_HRESET}}$, is generated by the MPC6820 and the PSM502 PAL Logic. The MPC8260 generates $\overline{\text{PQ_HRESET}}$ in response to a power-on reset, a software watchdog reset (if enabled), a bus monitor reset (if enabled), or a checkstop reset (if enabled).

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The PSM502 PAL will generate a PQ_HRESET under several conditions. The configuration of a few jumpers that feed into the PSM502 PAL regulate which signals generate PQ_HRESET. The following chart shows the signals involved and the jumper settings required to produce the desired action.

Table 10. !PQ_HRESET Control Signals and Select Jumpers

Signal Name	Function
CARD_RST	This input is enabled by jumpering K1-1 to K1-2, SMBEN true. This signal indicates to the PAL logic that the SMB controller is active and that it is configured to issue a hard reset to the board by asserting its CARD_RST signal. The logic will continue to issue PQ_HRESET as long as CARD_RST is asserted. As long as the jumper is in, the logic will drive PQ_HRESET in response to the CARD_RST signal no matter what the other jumper options are set to. If K1-1 to K1-2 is open, the CARD_RST signal will be ignored by the PAL Logic.
P1_RST_IN	This signal is generated by the CompactPCI bus and is the CompactPCI reset. The signal is buffered and fed to the PAL logic and the CompactPCI side of the Tundra chip as P1_RST_IN. The signal will always drive a PQ_HRESET unless the CT_BMASTER signal is active (controlled by jumper K2-1 to K2-2). If CT_BMASTER is active, it means that there is no CompactPCI system master and that the CT bus has control of the subsystem. The PQ_HRESET signal is generated when the falling edge of P1_RST_IN is detected and held low for approximately 11.50 ns. clock cycles. The PQ_HRESET will then be negated and not reasserted until the P1_RST_IN has been negated for at least 50ns.
CT_RESET (Input)	The CT_RESET signal is used to generate the PQ_HRESET, only when the CT_BMASTER signal is active. The CT_BMASTER indicates to the logic that there is no CompactPCI bus in the system and that the CT is the controlling element for the board. When Jumper K2-1 to K2-2 is in place, the CT_BMASTER signal is driven true. If the jumper is left open the reception of CT_RESET will be ignored by the logic.

Soft Reset

The soft reset for the board is accomplished by asserting the PQ_SRESET signal. The signal is distributed to the MPC8260, PSM502 Registers PAL, PSM503 Clock Controller PAL, PSM499 Clock Mux PAL, PSM500 General I/O Ports PAL, PSM501 Interrupt Controller PAL, PSM505 CT bus Clock Adjustment PAL, the J10 Mictor and the COP8 JTAG header for the debug port. The signal sources for PQ_SRESET include the MPC8260 and the PSM502 PAL logic.

The MPC8260 will assert this signal in response to any power-on reset or hard reset condition. The effect of soft reset on the processor is different than power-on reset or hard reset, and is outlined in the Motorola MPC8260 User's Manual.

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Logic inside the PSM502 PAL will also assert the PQ_SRESET signal when some on board signals are true. One of the signal sources is the Tundra PowerSpan chip level 5 interrupt. The interrupt is routed to the PSM502 logic and is used to let the system host cause a soft reset to the board under the control of the system software. This feature is only active when the PQ_HRESET signal is inactive and the Reset Configuration jumper P4, is in the Normal Position P4-2 to P4-3.

The other source of PQ_SRESET in the PSM502 PAL is the TOD_RST_OUT signal. The TOD_RST_OUT signal is a watchdog timer timeout signal that is part of the functionality of the Time Of Day timer (M48T59Y). If the watchdog timer is activated in the part and set to cause a pulse on the RST output, the TOD_RST_OUT signal will be generated if the watchdog expires.

Tundra PowerSpan Resets

The Tundra PowerSpan has three sources of Reset. It can both receive and source reset on the Primary PCI bus 1, the secondary PCI bus 2 and the local processor or PB bus. The setup on each source is as follows:

Primary PCI Reset

In the CPC395 implementation, the chip is set to receive a reset on the primary PCI 1 bus and to not be a source. This is accomplished by setting the P1_RST_DIR pin low. The P1_RST_IN input signal from the PCI bus is buffered and routed to the PSM502 logic and the Tundra P1_RST input. The signal will cause logic within the chip to be reset as outlined in the Tundra users manual. The P1_RST_IN also causes a PQ_HRESET to the board as described in the Hard Reset section.

Processor Bus Reset

The PowerSpan processor bus reset pin PB_RST is configured to be an input. This is accomplished by setting the PB_RST_DIR pin low. The source of the signal is the PSM502 logic. The logic drives the PB_RST pin with a standard driver output and it drives the signal true when PQ_HRESET is true or whenever the Reset Configuration jumper P4, is in the PROM Programming Position P4-1 to P4-2.

Secondary PCI Reset

The Secondary PCI Reset is not implemented in this design.

Peripheral Resets

Each peripheral chip on the CPC395 has an individual reset line. The peripheral resets are driven by the PSM50 PAL logic. The resets are all set to a reset state by anything that creates a PQ_SRESET on the board. The devices will be held in reset until the appropriate bit in the general purpose registers is set. The following table describes the individual peripheral reset signals, the power up reset state and the bit that controls the device in the general purpose registers.

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Table 11. Peripheral Resets

Peripheral	Reset Signal Name	!PQ_SRESET State	Register Bit Name
H.110 A Side Switch	$\overline{\text{A_H110_RST}}$	0	A_H110_RST
H.110 B Side Switch	$\overline{\text{B_H110_RST}}$	0	B_H110_RST
Ethernet PHY 1	PHY1_RESET	1	phy_rst1
Ethernet PHY 2	PHY2_RESET	1	phy_rst2
A Side T3 MUX 1	$\overline{\text{A_TMUX_RST}}$	0	A_TMUX_RST
B Side T3 MUX 1	$\overline{\text{B_TMUX_RST}}$	0	B_TMUX_RST
A side Monitor FALC	$\overline{\text{A_FALC_RST}}$	0	A_FALC_RST
B side Monitor FALC	$\overline{\text{B_FALC_RST}}$	0	B_FALC_RST
Elastic Store	$\overline{\text{ESRESET}}$	0	ESRESET

The bit actions are described further in the General Purpose Registers Section.

CT Bus Resets

The PSM502 logic can also generate CT Bus resets on the A and B CT buses. The conditions that must be met to allow this to happen are that the CT Bus is the master of the cardfile. Having Jumper K2-1 to K2-2 inserted sets this condition. A second Jumper, K9-1 to K9-2 must be in to enable the PSM502 logic to respond to CT_RESET bit in the general purpose register bits. See “General Purpose Status and Control Registers” on page 111.

3.4 General CPU Section

The CPU that is used on the board is a Motorola MPC8260. For information on the internal portions of the chip, see the Motorola website: www.mot.com.

The MPC8260 is the primary controller on the CPC395. It supplies the PowerPC CPU core, the Communications Processor Module (CPM), and the 60X bus processor bus controller. It has direct connections to, and is the controller for the Synchronous DRAM (SDRAM), the local bus Synchronous Static RAM (SSRAM), and the TUNDRA PowerSPAN Dual PCI bridge. It also controls all of the onboard peripheral chips via a buffered data and address bus.

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MPC8260 Initial Configuration

A great deal of the initialization of the MPC8260 occurs during the hard reset process. When the $\overline{\text{PQ_HRESET}}$ signal is active the CPU selects its CPU PLL settings and several other initial configuration settings. The following sections describe these settings.

Core Clock and PLL

The board has a 200 MHz Power PC Core (PPC), a 133 MHz CPM and a 66 MHz external 60x, multi-master bus. The chip is supplied with a 66 MHz primary clock input (CLK1) on the CLKIN input. The clock PLL settings to select the core speed are driven into the part by the MODCLOCK lines from the PAL logic while the $\overline{\text{PQ_HRESET}}$ signal is active. The clock settings are as follows:

- 200MHz core/133Mhz CPM/66Mhz 60x Bus (Initial Release Product)
- MODCLOCK[2:0] 111

The following core clock configurations settings are suggested for operation with the Performance Technologies default software settings for system clocks, refresh timers and baud rate generators.

Table 12. System Clock Control Register Bit Field Definitions

Bits	Name	Description
29	CLPD	0-CPM does not enter low power mode when the core enters low power mode.
30-31	DFBRG	01-Division factor of BRGCLK relative to VCO_OUT (twice the CPM clock). Defines the BRGCLK frequency. The BRGCLK is divided from the CPM clock. 01 set the divisor to 16.

NOTE: When the MPC8260 has the RSTCONF jumper in the Boot PROM program mode, K4 –1 to K4-2, the clock default modes for the PLL are invoked. The MPC8260 will function in this mode, it will be able to use the SDRAM and program the Boot FLASH PROM but no other operations, CPM or peripherals are guaranteed or supported.

Reset Configuration

The reset configuration has two modes. If the RSTCONF is high (jumpered in the P4-1to P4-2 Boot FLASH programming mode) the MPC8260 will take the default settings and there will be no Reset Configuration cycles on the Bus because the MPC8260 will be set to be a RESET Slave and the PowerSpan will be held in reset.

If the RSTCONT jumper is in the Normal mode (K4-2 to K4-3) the MPC8260 will be setup as the Reset Configuration Master. The PowerSpan device will be the 3rd configuration slave.

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The MPC8260 will read its configuration from the Boot FLASH device beginning at location 0. The format of the boot words is listed in the MPC8260's user manual. The information read from the PROM is loaded into the Hard Reset Configuration Word Register. The address for this device is located in the memory map in the MPC8260's user manual. The standard configuration supplied with the Boot FLASH is:

- No External Arbitration.
- Internal Memory Controller Selected for the FLASH.
- Core is Active
- External Bus Mode is 60X compatible.
- Boot port size is 8 bit.
- Core initial exception prefix is zero. Exceptions are vectored to Physical address 0xFFFn_nnnn.
- Internal Space port size is set to 32 bit.
- Bus address pins selected for layer 2 cache pin configuration. (BADDR Pins selected)
- No data bus parity, IRQ pins selected for the multifunction pins.
- Base address of the Internal Memory space is 0xFF00_0000.
- Boot memory space 0xFE00_0000 to 0xFFFF_FFFF.
- Address Bus Busy and Data Bus Busy selected on multifunction pins.
- MMR Register initial value is no masking on Bus Request lines.
- Local Bus Pin Configuration (LBPC), pins function as a local bus.
- Address Parity Pin configuration, no address parity, Bank Select Function Selected on Multifunction pins.
- CS10 pin configuration is set to be $\overline{\text{BCTL1}}$, Buffer control for byte lane 1.
- MODCK_H Clock Reset Configuration high order bits set to 0101.

Internal Initial Configuration

The internal initial configuration is obtained from the Boot Code running out of the FLASH PROM. The configuration information includes the initial settings for the System Integration Unit module configuration register (SIUMCR).

Table 13. SIUMCR Register Settings

Field	Recommended Setting	Description
BBD	0	$\overline{\text{ABB}}/\overline{\text{IRQ2}}$ pin is $\overline{\text{ABB}}$, $\overline{\text{DBB}}/\overline{\text{IRQ3}}$ pin is $\overline{\text{DBB}}$
ESE	1	External Snooping is enabled, $\overline{\text{GBL}}/\overline{\text{IRQ1}}$ pin is $\overline{\text{GBL}}$.
PBSE	0	Parity byte select is disabled, GPL4 is available for UPM use.

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Table 13. SIUMCR Register Settings *(Continued)*

Field	Recommended Setting	Description
CDIS	0	MPC8260 core is enabled.
DPPC	00	Pins set to $\overline{IRQx}$
L2CPC	10	Level 2 cache pins set to BADDR[29-31]
LBPC	00	Local Bus pins function as local bus
APPC	10	MODCLK Pins function as BNKSEL[0-2] and $\overline{IRQ7}$ out and $\overline{CS11}$
CS10PC	01	$\overline{CS10}$ is $\overline{BCTL1}$
BCYLC	00	$\overline{BCTL0}$ is used as W/$\overline{R}$, $\overline{BCTL1}$ is $\overline{OE}$ control.
MMR	00	No masking on bus request lines.
LPBSE	0	Parity Byte disabled. LGPL4 output of UPM is available for memory control.

Memory Map

The memory map is defined by the CPC395 Address Decode Scheme. There are different levels of Address Decode built into the CPC395. The first level and primary decode is done by the MPC8260's System Interface Unit (SIU). One of the SIU's subsections is the Memory controller. The memory controller is responsible for controlling a maximum of twelve memory banks shared by a high performance SDRAM machine, a general-purpose chip-select machine (GPCM), and three user-programmable machines (UPMs). It supports a glueless interface to synchronous DRAM (SDRAM), SRAM, EPROM, FLASH EPROM, burstable RAM, regular DRAM devices, extended data output DRAM devices, and other peripherals. This flexible memory controller allows the implementation of memory systems with very specific timing requirements:

- .The SDRAM machine provides an interface to synchronous DRAMs, using SDRAM pipelining, bank interleaving, and back-to-back page mode to achieve the highest performance.
- The GPCM provides interfacing for simpler, lower-performance memory resources and memory-mapped devices. The GPCM has inherently lower performance because it does not support bursting. For this reason, GPCM-controlled banks are used primarily for boot-loading and access to low-performance memory-mapped peripherals.
- The UPM supports address multiplexing of the external bus, refresh timers, and generation of programmable control signals for row address and column address strobes to allow for a glueless interface to DRAMs, burstable SRAMs, and almost any other kind of peripheral. The refresh timers allow refresh cycles to be initiated. The UPM can be used to generate different timing patterns for the control signals that govern a memory device. These patterns define how the external control signals behave during a read, write, burst-read, or burst-write access request. Refresh timers are also available to periodically generate user-defined refresh cycles.

The primary control of the devices served by the memory controller machines is through the MPC8260's external Chip select lines. The specific memory controller setups will be defined for each type of device in the section of the specification that describes the device. The following table represents the primary address decode of the External chip select lines.

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Table 14. MPC8260 Chip Select Assignments

Chip Select Line	Controlled Device	Address Range
$\overline{CS0}$	FLASH Boot PROM	FFF0_0000 to FFF7_FFFF h
$\overline{CS1}$	SDRAM	0000_0000 to 01FF_FFFF h
$\overline{CS2}$	Local Bus SSRAM	2080_0000 to 2083_FFFF h
$\overline{CS3}$	Application FLASH	1000_0000 to 10FF_FFFF h
$\overline{CS4}$	General Purpose Registers	2000_0000 to 2000_00ff h
$\overline{CS5}$	Communications Devices	2010_0000 to 2010_7FFF h
$\overline{CS6}$	H.110 A Side Switch	2020_0000 to 2020_7FFF h
$\overline{CS7}$	H.110 B Side Switch	2020_8000 to 2020_FFFF h
$\overline{CS8}$	Time of Day Chip	2030_0000 to 2030_7FFF h
$\overline{CS9}$	Reserved	2040_0000 to 2040_7FFF h
$\overline{CS11}$	Not Used	
None	Power Span mapped space	3000_0000 to 3000_0fff

60x Bus Connections

The MPC8260 has its external bus configured in the PowerPC 60x mode. The bus features a 32-bit non-parity address bus. The address bus is pulled up by 20K resistor packs to V3V to prevent unknown bus conditions during no-drive periods on the bus. The 64-bit non-parity data bus is also pulled up to V3V with 20K resistor packs to prevent unknown bus conditions during no-drive periods on the bus. Because the bus runs at a 66 MHz clock rate, the length of the bus is restricted to 6in. or less with a very limited number of peripheral connections.

There are some multifunction pins that are used for bus control. These assignments have been made as follows:

- For multiple beat transfers, the MPC8260 is configured to supply the BADDRXX lines as the lower order address bits.
- The PBSx/$\overline{PSDDQMx}$/$\overline{PWEx}$ lines are configured as PSDDQMx.
- PGPL5/PSDAMUX is configured as PSDAMUX for SDRAM control.
- MODCLKx/Apx/TCx/BANKSELx are used as the MODCLKx inputs during hard reset and as BNKSELx for the SDRAM module.
- PGPL3/$\overline{PSDCAS}$ is used as the $\overline{PSDCAS}$ for the SDRAM module.
- PGPL2/$\overline{PSDRAS}$/$\overline{POE}$ is used as the $\overline{PSDRAS}$ for the SDRAM module.
- PGPL1/$\overline{PSDWE}$ is used as the $\overline{PSDWE}$ for the SDRAM module.

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- PGPL0/PSDA10 is used as PSDA10 for the SDRAM module.

The external cache lines are not used and are therefore not connected. The internal CPU arbiter is used as the bus arbiter. All of the normal 60x bus transfer size (TSIZE0-3) and transfer type (TT0-4) lines are supported. The rest of the transfer control signals are used in their normal mode. All of the control signals are pulled to V3V with 10K resistors to prevent accidental activation during no-drive periods on the bus.

MPC8260 Interrupt Sources

Several multifunction pins are used to supply the MPC8260 with interrupts from the various board peripherals. The $\overline{IRQ0}$ to $\overline{IRQ7}$ lines are used along with some of the PORT C interrupt capable pins. The interrupt sources, for the most part, have multiple interrupt conditions. The PSM501 PAL contains actual interrupt input signals and supplies the various enable and masking conditions used in the interrupt scheme. The PSM501 PAL is connected directly to the MPC8260's interrupt inputs. Refer to the individual component subsections or the component's user manual for the complete breakdown of interrupt causes. The following table defines the interrupt levels used and what the source device(s) of each level is:

Table 15. MPC8260 Interrupt Sources

IRQ Level	Pin Number	Controlled Device
$\overline{IRQ0}$	T1	NMI Interrupt from the Abort Jumper K14-1 to K14-2
$\overline{IRQ1}$	A22	A Side H.110 Clock Failure Interrupts
$\overline{IRQ2}$	E21	B Side H.110 Clock Failure Interrupts
$\overline{IRQ3}$	D21	A Side TMUX and LIU Interrupts
$\overline{IRQ4}$	C21	B Side TMUX and LIU Interrupts
$\overline{IRQ5}$	B21	Monitor FALC A General Interrupt
$\overline{IRQ6}$	A21	Monitor FALC B General Interrupt
$\overline{IRQ7}$	E20	PowerSpan PCI Bridge input Interrupt
PC0	AB26	System Management Controller Chip Interrupt
PC1	AD29	Time of Day Interrupt
PC2	AE29	Ethernet PHY 1 Interrupt
PC3	AE27	Ethernet PHY 2 Interrupt

Local Bus Connections

The MPC8260 Local Bus is configurable to be a PCI interface or a slave device, local memory bus. This bus is closely coupled to the MPC8260's CPM processor, and its most effective use is as memory for the CPM. In the CPC395 implementation, the bus is configured as a slave device, local memory bus for a bank of

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Synchronous Static RAM (SSRAM). The local bus provides address, data and control for the SSRAM. The cycle control for the SSRAM is provided by the UMPB and the $\overline{CS2}$'s address space decode. The Local Bus multifunction pins are configured for the SSRAM as follows:

- LGPL0/LSDA10 is configured as LGPL0 and controls the SSRAM output enable signal ($\overline{LCL_OE}$).
- LGPL1/$\overline{LSDWE}$ is configured as LGPL1 and controls the SSRAM Address Control Strobe signal ($\overline{LCL_ADSC}$).
- LGPL2/$\overline{LSDRAS}$/$\overline{LOE}$ is configured as LGPL2 and controls the SSRAM Address Advance Strobe signal ($\overline{LCL_ADV}$).
- LGPL3/LSDCAS is configured as LGPL3 and controls the SSRAM Chip Enable signal ($\overline{LCL_CE}$).
- The $\overline{LBSx}$/$\overline{LSDDQMx}$/$\overline{LWEx}$ are configured as $\overline{LBSx}$ and control the SSRAM byte strobes ($\overline{LCL_LBSx}$).
- The $\overline{PCI_C}$/BEx/LCL_DPx are configured as DPX and control the SSRAM data parity bits (LCL_DPx).
- LPL5 and $\overline{LWR}$ are not used in this design.

MPC8260 Parallel I/O Ports

The CPM supports four general-purpose I/O ports: A, B, C, and D. Each pin in the I/O ports can be configured as a general-purpose I/O signal or as a dedicated peripheral interface signal. Port C is unique in that 16 of its pins can generate interrupts to the internal interrupt controller.

Each pin can be configured as an input or output and has a latch for data output, read or written at any time, and configured as general-purpose I/O or a dedicated peripheral pin. Some of the pins can be configured as open-drain (the pin can be configured in a wired-OR configuration on the board). The pin drives a zero voltage but three-states when driving a high voltage. Note that port pins do not have internal pull-up resistors. Due to the CPM's significant flexibility, many dedicated peripheral functions are multiplexed onto the ports. The functions are grouped to maximize the pins' usefulness in the greatest number of MPC8260 applications. Refer to the MPC8260 user's manual for more information on the various peripheral setups.

Serial Management Controllers SMC 1 and SMC 2

The MPC8260 features two, general-purpose serial management controllers (SMCs), that may be used as general purpose RS232 communications interfaces. The two SMCs are full-duplex ports that can be configured independently to support one of three operating or modes:

- UART
- Transparent
- General Circuit Interface (GCI)

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The CPC395 is designed to support UART operation on both ports. Two RJ11 connectors located on the CPC395 faceplate provide connectivity to the SMCs. RJ11 connector J6 is configured to be the Console port and RJ11; J7 is designated as the secondary serial port. The console port can be used to provide a debug, monitor or download function. The console port also has the ability to generate a $\overline{\text{PQ_HRESET}}$ if it receives a RS232 break signal that lasts for longer than 3.2ms. The logic that watches the console receive line is located in the PSM502 PAL. The reset on break detect can be enabled by setting jumper K10-1to K10-2. Removing the jumper will disable the reset action.

The secondary Serial I/O channel can be configured for any purpose that the SMC will support. Both ports feature a MAX202E RS232 transceiver with integral ESD protection. A set of external transient protection diodes and high frequency shunt capacitors also augment the inherent ESD protection on the transmit and receive lines. Both received signals from the MAX202E are buffered through the PSM494 PAL logic to convert them from 5V output logic to 3V compatible logic for the MPC8260 inputs.

On the CPC395 TDM for T1/E1 Channels on TDM_B1 and TDM_B2

In general, the MPC8260 can support 8 full duplex TDMs on two SIs (1, 2). Each SI supports 4 TDMs (A, B, C, D). Each SI has an SIRAM with 256 entries for Transmit, and 256 entries for Receive. Each of these 256 entries is divided into 4 banks of 64 entries each. Only one entry is needed to route a timeslot to a particular MCC channel. Allocation of the SIRAM for each TDM is done in 32-entry segments. The user can define the size of each SIRAM that is related to a certain TDM channel by programming the starting bank of that TDM.

On the CPC395 both Serial Interfaces (SI) in the MPC8260 are configured to support up to 256 data or voice channels on TDM_ B1 and TDM_B2.

Fast Ethernet 10/100 Base T on FCC1 and FCC3

The CPC395 uses two of the MPC8260's FCC controllers to function as 10/100 Base T Ethernet MACs. FCC1 and FCC 3 are used for this function. Each FCC connection supports an independent Physical Layer (PHY) 10/100 Base T Fast Ethernet connection through its MII (Media-Independent Interface). A Cirrus Logic CS8952 is the PHY interface device. The Ethernet I/O signal lines and the Link/Activity LED status indicator lines are brought out to rear panel CompactPCI on connector J3. The CPC395 Ethernet interface implements the full set of IEEE 802.3/Ethernet CSMA/CD media access control (MAC) and channel interface functions. The FCC configuration is set in MPC8260 GFMRx[MODE] register of each active FCC. The MPC8260 CPM pin assignments for Fast Ethernet devices can be found in "MPC8260 Parallel Port Pin Assignments" on page 40.

The IEEE 802.3 management interface MDIO and MDC are supported via general-purpose I/O pins PB19 and PB18 respectively. Since there is no MPC8260 hardware controller, the management interface function is implemented in software via these general purpose bits.

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The MPC8260 PB21 and PB22 bits are used to provide an MII isolate signal to each PHY (1 and 2 respectively). These bits are programmed as general purpose I/O bits in the MPC8260 and are under software control.

Each CS8952 Ethernet PHY provides an MII_IRQ interrupt signal line to the PSM501 PAL logic, which maps it to the appropriate interrupt on the MPC8260.

I^2C Bus

There is an I^2C Bus implemented on pins PA0 and PA1. They are connected to the I^2C pins on the SODIMM connector that houses the SDRAM module. This bus can be used to retrieve SDRAM setup parameters for memory controller operation. The I^2C bus is implemented in software as these two pins are programmed as general purpose I/O pins on the MPC8260.

MPC8260 Parallel Port Pin Assignments

The following table shows the MPC8260 Port A pin assignments:

Table 16. MPC8260 Port A Pin Assignments

Pin	Pin Function					
	PSORA = 0			PSORA = 1		
	PDIRA =1 Out	PDIRA = 0 In	Default	PDIRA = 1 Out	PDIRA = 0 In	Default
PA31					FCC1: COL MII	
PA30					FCC1: CRS MII	
PA29				FCC1: TX_ER MII		
PA28				FCC1: TX_EN MII		
PA27					FCC1: RX_DV MII	
PA26					FCC1: RX_ER MII	
PA25			Unassigned			Unassigned
PA24			Unassigned			Unassigned
PA23			Unassigned			Unassigned
PA22			Unassigned			Unassigned

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Table 16. MPC8260 Port A Pin Assignments *(Continued)*

Pin	Pin Function					
	PSORA = 0			PSORA = 1		
	PDIRA =1 Out	PDIRA = 0 In	Default	PDIRA = 1 Out	PDIRA = 0 In	Default
PA21	FCC1: TXD3 MII					
PA20	FCC1: TXD2 MII					
PA19	FCC1: TXD1 MII					
PA18	FCC1: TXD0 MII					
PA17		FCC1: RXD0 MII				
PA16		FCC1: RXD1 MII				
PA15		FCC1: RXD2 MII				
PA14		FCC1: RXD3 MII				
PA13			Unassigned			Unassigned
PA12			Unassigned			Unassigned
PA11			Unassigned			Unassigned
PA10			Unassigned			Unassigned
PA9	SMC2: SMTXD					
PA8		SMC2: SMRXD				
PA7			Unassigned			Unassigned
PA6			Unassigned			Unassigned
PA5			Unassigned			Unassigned
PA4			Unassigned			Unassigned
PA3			Unassigned			Unassigned
PA2			Unassigned			Unassigned
PA1			PQ_I2CSDA			Unassigned
PA0			PQ_I2CSCL			Unassigned

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The following table shows the MPC8260 Port B pin assignments:

Table 17. MPC8260 Port B Pin Assignments

Pin	Pin Function					
	PSORB = 0			PSORB = 1		
	PDIRB = 1 Out	PDIRB = 0 In	Default	PDIRB = 1 Out	PDIRB = 0 In	Default
PB31					TDM_B2: L1TXD	
PB30					TDM_B2: L1RXD	
PB29					TDM_B2: L1RSYNC	
PB28					TDM_B2: L1TSYNC	
PB27			Unassigned			Unassigned
PB26			Unassigned			Unassigned
PB25			Unassigned			Unassigned
PB24			Unassigned			Unassigned
PB23			Unassigned			Unassigned
PB22			ISOLATE_MII2			Unassigned
PB21			ISOLATE_MII1			Unassigned
PB20			Unassigned			Unassigned
PB19			PB19_MDIO			Unassigned
PB18			PB18_MDC			Unassigned
PB17		FCC 3:RX_DV MII				
PB16		FCC 3:RX_ER MII	.			
PB15	FCC 3:TX_ER MII					
PB14	FCC 3:TX_EN MII					
PB27			Unassigned			Unassigned
PB26			Unassigned			Unassigned
PB25			Unassigned			Unassigned

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Table 17. MPC8260 Port B Pin Assignments *(Continued)*

Pin	Pin Function					
	PSORB = 0			PSORB = 1		
	PDIRB = 1 Out	PDIRB = 0 In	Default	PDIRB = 1 Out	PDIRB = 0 In	Default
PB24			Unassigned			Unassigned
PB23			Unassigned			Unassigned
PB22			ISOLATE_MII2			Unassigned
PB21			ISOLATE_MII1			Unassigned
PB20			Unassigned			Unassigned
PB19			PB19_MDIO			Unassigned
PB18			PB18_MDC			Unassigned
PB17		FCC3:RX_DV MII				
PB16		FCC3:RX_ER MII				
PB15	FCC3:TX_ER MII					
PB14	FCC3:TX_EN MII					

The following table shows the MPC8260 Port C pin assignments:

Table 18. MPC8260 Port C Pin Assignments

Pin	Pin Function					
	PSORC = 0			PSORC = 1		
	PDIRC =1 Out	PDIRC = 0 In	Default	PDIRC = 1 Out	PDIRC = 0 In	Default
PC31			Unassigned			Unassigned
PC30			Unassigned			Unassigned
PC29		Assign CLK3 to TDMB1 RxCLK				

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Table 18. MPC8260 Port C Pin Assignments *(Continued)*

Pin	Pin Function					
	PSORC = 0			PSORC = 1		
	PDIRC =1 Out	PDIRC = 0 In	Default	PDIRC = 1 Out	PDIRC = 0 In	Default
PC28		Assign CLK4 to TDMB1 TxCLK				
PC27			Unassigned			Unassigned
PC26			Unassigned			Unassigned
PC25			Unassigned			Unassigned
PC24			Unassigned			Unassigned
PC23			Unassigned			Unassigned
PC22			Unassigned			Unassigned
PC21		Assign CLK11 to FCC 1 MII Tx_CLK				
PC20		Assign CLK12 to FCC 1 MII Rx_CLK				
PC19		Assign CLK13 to FCC 3 MII Tx_CLK				Unassigned
PC18		Assign CLK14 to FCC 3 MII Rx_CLK				Unassigned
PC17		Assign CLK15 to TDMB2 RxCLK				
PC16		Assign CLK16 to TDMB2 TxCLK				
PC15			Unassigned			Unassigned
PC14			Unassigned			Unassigned
PC13			Unassigned			Unassigned
PC12			Unassigned			Unassigned
PC11			Unassigned			Unassigned
PC10			Unassigned			Unassigned
PC9			Unassigned			Unassigned

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Table 18. MPC8260 Port C Pin Assignments *(Continued)*

Pin	Pin Function					
	PSORC = 0			PSORC = 1		
	PDIRC =1 Out	PDIRC = 0 In	Default	PDIRC = 1 Out	PDIRC = 0 In	Default
PC8			Unassigned			Unassigned
PC7			Unassigned			Unassigned
PC6			Unassigned			Unassigned
PC5			Unassigned			Unassigned
PC4			Unassigned			Unassigned
PC3			PHY2_INT			
PC2			PHY2_INT			
PC1			TOD_INT			
PC0			SMB_INT			

The following table shows the MPC8260 Port D pin assignments:

Table 19. MPC8260 Port D Pin Assignments

Pin	Pin Function					
	PSORD = 0			PSORD = 1		
	PDIRD =1 Out	PDIRD = 0 In	Default	PDIRD = 1 Out	PDIRD = 0 In	Default
PD31			Unassigned			Unassigned
PD30			Unassigned			Unassigned
PD29			Unassigned			Unassigned
PD28			Unassigned			Unassigned
PD27			Unassigned			Unassigned
PD26			Unassigned			Unassigned
PD25			Unassigned			Unassigned
PD24			Unassigned			Unassigned
PD23			Unassigned			Unassigned
PD22			Unassigned			Unassigned
PD21			Unassigned			Unassigned
PD20			Unassigned			Unassigned

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Table 19. MPC8260 Port D Pin Assignments *(Continued)*

Pin	Pin Function					
	PSORD = 0			PSORD = 1		
	PDIRD =1 Out	PDIRD = 0 In	Default	PDIRD = 1 Out	PDIRD = 0 In	Default
PD19			Unassigned			Unassigned
PD18			Unassigned			Unassigned
PD17			Unassigned			Unassigned
PD16			Unassigned			Unassigned
PD15			Unassigned			Unassigned
PD14			Unassigned			Unassigned
PD13					TDM_B1: L1TXD	
PD12					TDM_B1: L1RXD	
PD11					TDM_B1: L1TSYNC	
PD10					TDM_B1: L1RSYNC	
PD9	SMC1: SMTXD					
PD8		SMC1: SMRXD				
PD7						
PD6			Unassigned			Unassigned
PD5			Unassigned			Unassigned
PD4			Unassigned			Unassigned

JTAG Support

The JTAG testing port on the MPC8260 is used to support the EST COP debugger on the P2 connector. The connector is set up to support the extended 16-pin COP debugger signaling, but the basic 10 pin signaling devices may be used with an interposing adapter. The P2 pinout is found in the following Table:

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Table 20. JTAG Pinout

Pin Number	Signal Name
1	PQ_TDO – JTAG Test Data Out signal
2	$\overline{\text{PQ_QACK}}$- Quiescent State Acknowledge, not supported
3	PQ_TDI- JTAG Test Data In signal
4	$\overline{\text{PQ_TRST}}$- JTAG Reset and Tri-state signal
5	$\overline{\text{PQ_QREQ}}$- Quiescent State Request-
6	V3V
7	PQ_TCK- JTAG Test Clock
8	No Connection
9	PQ_TMS-JTAG Test Mode Select
10	No Connection
11	$\overline{\text{PQ_SRESET}}$- MPC8260 Soft Reset
12	Ground
13	$\overline{\text{PQ_HRESET}}$- MPC8260 Hard Reset
14	No Connection
15	$\overline{\text{CHKSTPO}}$-Checkstop output, Not supported
16	Ground

All of the control signals are pulled to V3V with a 10K resistor to prevent false actuation when no JTAG controller is connected.

3.5 SDRAM

SDRAM architecture provides the ability to synchronously burst data at a high data rate with automatic column address generation, the ability to interleave between internal banks in order to hide PRECHARGE time, and the capability to randomly change column addresses on each clock cycle during a burst access. See Figure 9 on page 48.

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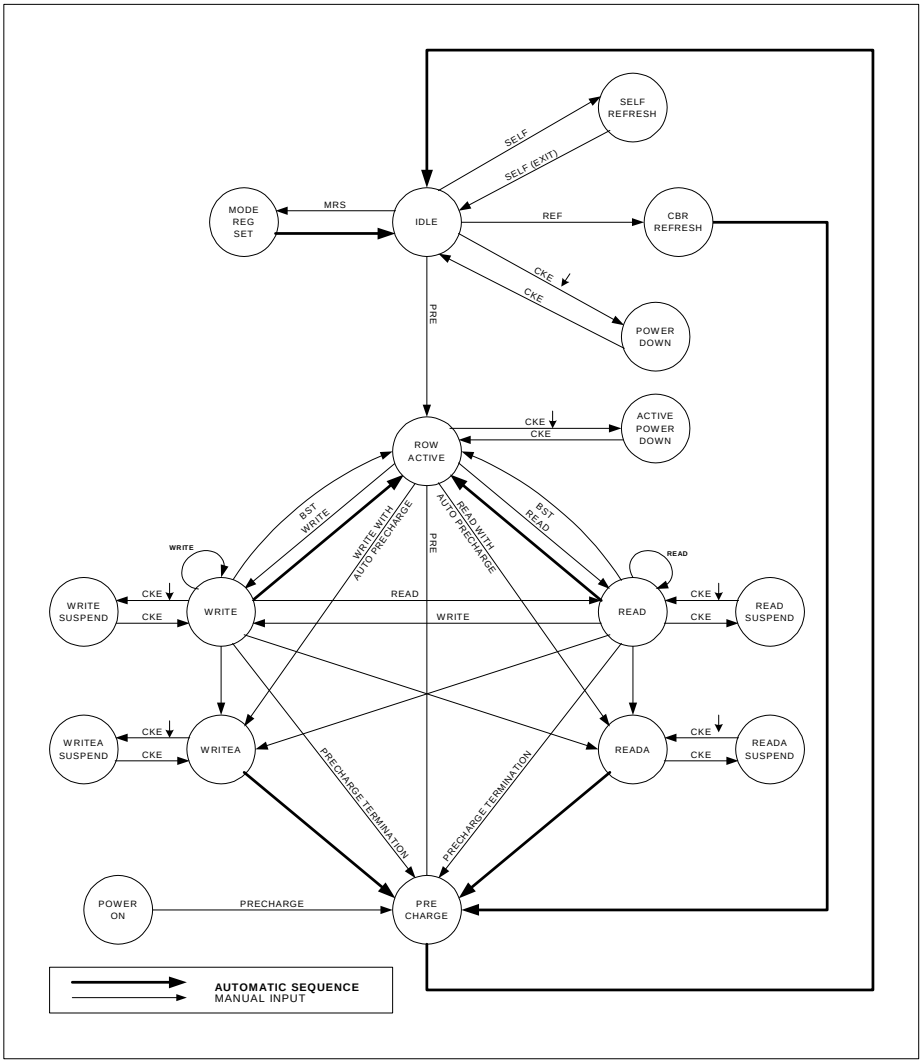


Figure 9. Partial SDRAM State Diagram

This synchronous DRAM design provides support for a 144-pin SODIMM module at 3.3V. The I2C interface of the SODIMM module is not supported. A density of 32MB or 64MB is supported at 66MHz.

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The data port size is 64-bits. Clock drive to the module is provided from the same low-skew clock driver that provides 66MHz to the MPC8260. The clock enable signals (CKE0 and CKE1) are permanently enabled, thus the SELF-REFRESH command and operation are unavailable. The MPC8260 can be programmed to provide refresh as needed. The 64-bit data bus, eight data read/write mask signals, and the three command signals (WE#, CAS#, and RAS#), and the two chip selects (S0 and S1) are provided to the module directly from the MPC8260. The MPC8260 will automatically assert S0, then S1, during refresh cycles. Multiplexed row/column address bits (MA0 thru MA12) and bank select signals (BA0 and BA1) are driven to the module from PSM496. The PSM496 PLD creates these from the MPC8260 address and bank select bits that have been latched with the processors ALE signal and multiplexed with the processors SDAMUX signal. Burst address bits (BADDR27 and BADDR28) are utilized directly to provide the least significant bits to the SODIMM during column address presentation. The least significant three address lines 29-31 are unused due to the 8 byte wide data path. The SODIMM module uses BADDR27 and BADDR28 to select one of four sequential locations as the first to be burst. Bursts occur up to a maximum of four transfers. The remaining three locations are addressed sequentially, after a mod 4 operation is applied to BADDR27 and BADDR28. SDA10 passes through PSM496 and always drives MA10 on the SODIMM. During the activate command, this pin provides the row address for A10. During a PRECHARGE command this pin selects PRECHARGE all-banks (PSDA10 = 1), or PRECHARGE-SELECTED-BANK (PSDA10 = 0) using BANKSEL[1-2]. Four banks are supported and BANKSEL[0] is unused. During READ and WRITE commands this pin selects AUTO-PRECHARGE (PSDA10 = 1) or no AUTO-PRECHARGE (PSDA10 = 0). Address bit ordering conventions are opposite between the MPC8260 (A0 is most significant bit) and the SODIMM (A0 is least significant bit) these are resolved within PSM496.

Memory Organization

The MPC8260 SDRAM register programming, described in subsequent sections, is in reference to a 32MB memory organized as 4 banks x 4096 rows x 256 columns x 16 data bits x 4 words, or a 64MB memory organized as 4 banks x 4096 rows x 512 columns x 16 data bits x 4 words. 32MB and 64MB memory is accessible using the S0 SDRAM input signal only. The 60x address bus is programmed to utilize page-based interleaving and is partitioned as shown in Table 21.

Table 21. 60x Address Bus Partitioning

	MSB of Start Address	Row	Bank Select	Column	LSB
64MB	A0-A5	A6-A17	A18-A19	A20-A28	A29-A31
32MB	A0-A6	A7-A18	A19-A20	A21-A28	A29-A31

Following initialization, access to the SODIMM is composed of an ACTIVATE and READ/WRITE command. During the ACTIVATE command the bank select and row selection are provided by PSM496 on the SODIMM address lines as shown in Table 22.

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Table 22. SODIMM Address Port During Activate Command

	SODIMM pins	na	BA1-BA0	MA12-MA2	MA1-MA0	na
	mpc8260 pins	A0-A14	bnksel[1-2]	A16-A26	baddr27-baddr28	A29-A31
64MB	physical address	na	A18-A19	row (A6-A15)	A16-A17	na
32MB	physical address	na	A19-A20	row (A7-A16)	A17-A18	na

During the row-addressing phase of SDRAM access, PSM496 provides bank select and address to the SODIMM as shown in Table 23.

Table 23. SODIMM Address Port During Row Addressing

	SODIMM pins	BA1-BA0	MA12	MA11	MA10	MA9-MA2	MA1-MA0
64MB	mpc8260 pins	bnksel[1-2]	-	A6	SDA10	A8-A15	A16-A17
32MB	mpc8260 pins	bnksel[1-2]	-	A7	SDA10	A9-A16	A17-A18
64MB	physical address	A18-A19	-	A6	A7	A8-A15	A16-A17
32MB	physical address	A19-A20	-	A7	A8	A9-A16	A17-A18

During the READ/WRITE command the bank select and column selection are provided by PSM496 on the SODIMM address lines as shown in Table 24.

Table 24. SODIMM Address Port during Read/Write Command

	SODIMM pins	BA1-BA0	MA12	MA11	MA10	MA9	MA8	MA7-MA2	MA1-MA0
	mpc8260 pins	bnksel[1-2]	0	0	SDA10	A19	A20	A21-A26	baddr27-baddr28
64MB	physical address	A18-A19	-	-	AP	-	column (A20)	column (A21-A26)	column (A27-A28)
32MB	physical address	A19-A20	-	-	AP	-	-	column (A21-A26)	column (A27-A28)

During the column-addressing phase of SDRAM access, PSM496 provides bank select and address to the SODIMM as shown in Table 25.

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Table 25. SODIMM Address Port during Column Addressing

	sodimm pins	BA1-BA0	MA12	MA11	MA10	MA9	MA8	MA7-MA2	MA1-MA0
	mpc8260 pins	bnksel[1-2]	0	0	SDA10	0	A20	A21 A26	baddr27-baddr28
64MB	physical address	a18-a19	-	-	AP	-	A20	A21-A26	A27-A28
32MB	physical address	a19-a20	-	-	AP	-	0	A21-A26	A27-A28

External Master Support

When the MPC8260 is placed in 60x compatible mode, external masters can access the SODIMM SDRAM as shown in Figure 10. External masters will not necessarily multiplex row and column addresses for the SDRAM. Therefore, an SODIMM SDRAM interface (PSM496) has been located between the 60x address bus and SODIMM address bus. 60x addresses are latched with ALE at the start of each memory cycle. The MPC8260 SDAMUX signal is used to multiplex address bits during row and column address presentation to the SDRAM. The MPC8260 monitors the 60x address bus and asserts ALE, SDAMUX, BADDR, and SDA10 appropriately for external masters.

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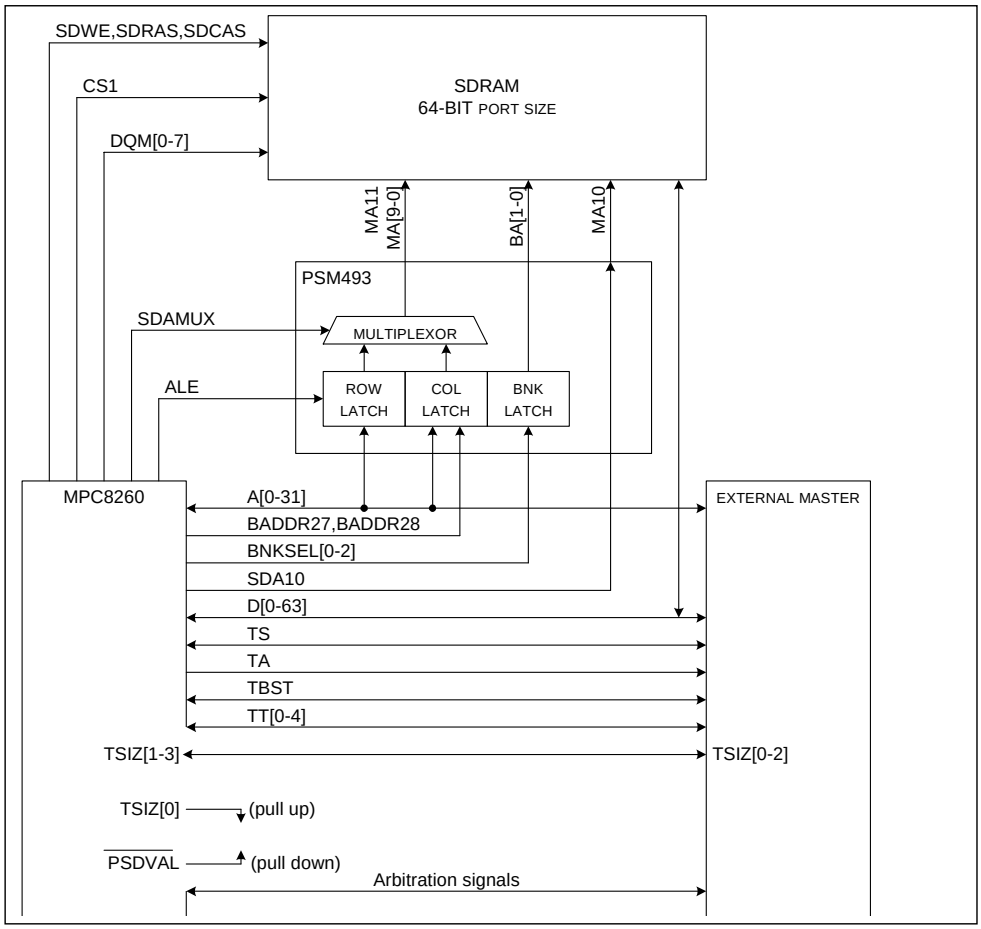


Figure 10. External Master SDRAM Configuration

SDRAM Controller Initialization

Prior to SDRAM Controller Initialization the SCMR, BSR, SIUMCR, and SWSR registers are initialized. The MPC8260 documentation recommends the following register order for SDRAM controller initialization: MPTPR, PSRT, PSDMR, OR, BR. A PRECHARGE-ALL-BANKS command is issued next, followed by eight CBR REFRESH commands and the SDRAM load mode register command. The SDRAM and MPC8260 SDRAM Controller will now be completely initialized. The SDRAM Controller can now be placed in normal operating mode by setting the PSDMR[OP] field to 000.

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MPC8260 MPTPR and PSRT Register Configuration

The SDRAM must receive 4096 refresh cycles in 64 mS, or a periodic refresh rate of 15.625 uS. The Memory Periodic Timer Prescaler Register (MPTPR) and SDRAM Refresh Timer (PSRT) together configure the refresh rate for SDRAM on the 60x bus. Each time the MPC8260 SDRAM refresh timer expires, all banks that qualify (e.g., CS1#) generate a bank staggering auto-refresh request using the SDRAM machine. Memory banks internal to SDRAM devices and modules have common row addresses and are refreshed simultaneously. The product of PSRT and MPTPR must be less than the product of the refresh rate and the BUS clock frequency (66.6 MHz). Therefore, the product of MPTPR and PSRT must be less than 15.625 uS x 66.6 MHz = 1041. MPTPR is programmed to 0x32 = 50 and PSRT is programmed to 0xE = 14 to produce a product of 700.

MPC8260 PSDMR Register Configuration

The 60x SDRAM Mode Register (PSDMR) contains PBI, RFEN, OP, SDAM, BSMA, SDA10, RFRC, PRETOACT, ACTTORW, BL, LDOTOPRE, WRC, EAMUX, BUFCMD, and CL fields.

Table 26. PSDMR Register Configuration

FIELD	32MB	64MB
PBI	1	1
RFEN	1	1
SDAM	010	011
BSMA	010	010
SDA10	010	011
RFRC	100	100
PRETOACT	010	010
ACTTORW	010	010
BL	0	0
LDOTOPRE	10	10
WRC	10	10
EAMUX	1	1
BUFCMD	1	1
CL	10	10

PBI is set to 1 to enable page-based interleaving. RFEN is set to 1 to enable refresh services in the MPC8260. OP defines the command presented to the SODIMM. SDAM is set to 010 to specify that external bus address pins A[15-31] will present address signals A[5-21] during SDRAM accesses. The value of BSMA is irrelevant when the SODIMM interface utilizes bank select signaling that is presented on the BANKSEL[0-2] pins, as is done here. BSMA is set to 010 to select A[14-16] as internal bank select. SDA10 is set to 010 to select

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A8 to be presented on the SDA10 pin during an ACTIVATE command to the SDRAM. The value of SDMR[PBI] does not need to be programmed prior to programming PSDMR[SDA10]. RFRC is set to 100 to select 6 clocks for the refresh recovery time after an ACTIVATE command and before a REFRESH command. PRETOACT is set to 010 to set the minimum interval (following a PRECHARGE command and preceding an activate/refresh command) to 2 clocks. This should be 2 for the MICRON tRP of 20nS and clock frequency of 66.6 MHz. ACTTORW is set to 010 to set the minimum interval (following an activate command and preceding a read/write command) to 2 clocks. This should be 2 for the MICRON tRCD of 20nS and clock frequency of 66.6 MHz. BL is set to 0 to select a burst length of 4, which is required for a port size of 64 bits. LDOTOPRE is set to 10 to set the minimum interval (following the last data READ and preceding a PRECHARGE command) to 1 clock. This is less than the ap-note recommended value of tDPL, but consistent with the SDRAM datasheet recommendation of CAS-latency – 1 = 1. WRC is set to 10 to set the minimum interval (following the last data WRITE and preceding a PRECHARGE command) to 2 clocks. This is greater than the ap-note recommended, MICRON tCDL value of 1, but consistent with the WRITE recovery specification of 1CLK + 7nS. EAMUX is set to 1 to cause the memory controller to add another cycle for each address phase. This compensates for delays through the external address multiplexing circuitry. BUFCMD is set to 1 to select relaxed timing, which is recommended when address or command lines are buffered. CL is set to 10 to select a CAS latency of 2. This matches the SDRAM mode configuration word setting of CAS latency.

MPC8260 OR Register Configuration

The Option Register (OR) contains SDAM, LSDAM, BPD, ROWST, NUMR, PMSEL, and IBID fields.

Table 27. Option Register Configuration

FIELD	32MB	64MB
SDAM	1111_1110_0000_0000_0	1111_1100_0000_0000_0
BPD	01	01
ROWST	0111	0110
NUMR	011	011
PMSEL	0	0
IBID	1	1

SDAM is set to 1111_1100_0000_0000_0 to specify a 128MB address range. BPD is set to 01 to specify four internal banks per device. ROWST is set to 0101 to select A5 as the demultiplexed row start address bit. NUMR is set to 100 to select 13 address lines to be used for row addressing (i.e., A5-A17). PMSEL is set to 0 to select the back-to-back page mode (normal operation). IBID is set to 1 to disable bank interleaving between internal banks of an SDRAM device connected to the chip-select line.

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MPC8260 BR Register Configuration

The Base Register (BR) contains the BA, PS, DECC, WP, MS, EMEMC, ATOM, DR, and V fields.

Table 28. Base Register Configuration

Field	32MB	64MB
BA	0000_0000_0	0000_0000_0
PS	00	00
DECC	00	00
WP	0	0
MS	010	010
EMEMC	0	0
ATOM	00	00
DR	0	0
V	1	1

BA is set to 0000_0000_0 to specify a base address of 0 for SDRAM memory. PS is set to 00 to specify a data port size of 64 bits. DECC is set to 00 to disable data error checking and correction. WP is set to 0 in order to enable read and write accesses. MS is set to 010 in order specify that SDRAM is located on the 60x bus, as opposed to the local bus. EMEMC is set to 0 to specify that accesses will be handled according to MSEL, as opposed to an external memory controller. ATOM is set to 00 to indicate that the SDRAM memory space is not used for atomic operations. DR is set to 0 to specify that no data pipelining will be performed. V is set to 1 to indicate that this memory bank is valid, which allows the chip select to be asserted.

SDRAM Initialization Requirements

The SODIMM SDRAM must be powered up and initialized in a predefined manner. After a stable clock and power are provided to the device, a 100 uS period must elapse before a command is issued (other than COMMAND INHIBIT or NOP). COMMAND INHIBIT or NOP should be applied during this 100 uS period until the end of the period. Once the 100 uS period has been satisfied with COMMAND INHIBIT or NOP, a PRECHARGE command should be applied to PRECHARGE all banks and transition to the IDLE state. Once in the IDLE state, two AUTO REFRESH cycles must be performed. The mode register powers up in an undefined state and must now be loaded prior to applying any operational command. Assuming the refresh rate has been programmed in the MPC8260 refresh controller, refresh may now be enabled.

COMMAND INHIBIT

After power-up, a 66MHz clock is driven to the SODIMM. Chip select from the processor is inactive and thus provides the COMMAND INHIBIT command.

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PRECHARGE

Precharging all banks will place the SODIMM into the IDLE state. In order to precharge all banks the MPC8260 requires the PSDMR[OP] field be set to 101. The SODIMM SDRAM requires A10 to be high in order to precharge all banks. This is accomplished by connecting SDA10 from the MPC8260 to A10 of the SODIMM during row-address presentation. PRECHARGE of individual banks is supported in the same way. SDA10 from the MPC8260 is provided to A10 of the SODIMM during column-address presentation to support the AUTO-PRECHARGE command.

AUTO REFRESH

The AUTO REFRESH access occurs when the MPC8260 PSDMR register is accessed at 0xFF01_0190 with the OP field set to 001. This causes a CAS# before RAS# (CBR) refresh command to be presented to the SODIMM.

SODIMM Mode Register Configuration

The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. The mode register is used to define the specific mode of operation of the SODIMM SDRAM. This definition includes the selection of a burst length, a burst type, CAS latency, an operating mode and a write burst mode. The LOAD MODE REGISTER command is selected when CS#, RAS#, CAS#, and WE# are low. This access occurs when the MPC8260 PSDMR register is accessed at 0xFF01_0190 with the OP field set to 011. The SDRAM initialization routine sets burst length to 4, burst type to SEQUENTIAL, CAS latency to 2, operating mode to standard, and the write burst mode to PROGRAMMED. A burst length of 4 is required by the MPC8260 for 64-bit port size. A burst type of SEQUENTIAL is required for 60x-cash-wrap compatibility.

3.6 Boot Flash Memory

The boot flash EPROM is used to store the initial startup code for the CPC395's MPC8260 CPU. The device is socketed on the board at position U11. The boot flash is a non-volatile memory that has the following general characteristics:

- The flash is a single power supply, 4 Mbit, 3.0 volt-only flash memory device organized as 524,288bytes. The data appears on DQ0-DQ7.
- The device is in a 32-pin PLCC package.
- All read, erase, and program operations are accomplished using only a single power supply. Internally generated and regulated voltages are provided for the program and erase operations.
- The device is entirely command set compatible with the JEDEC single-power-supply flash standard.

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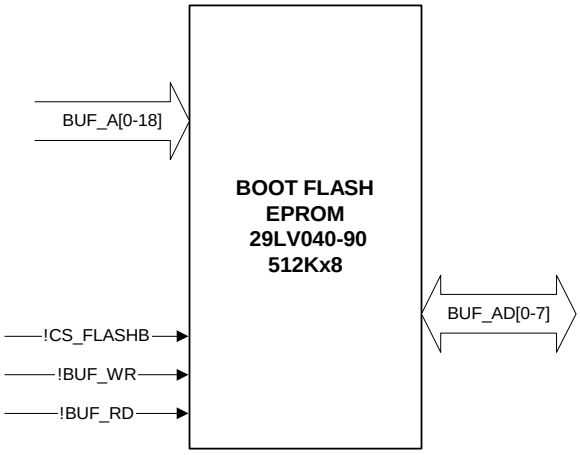


Figure 11. Boot Flash Block Diagram

The device is accessed by the MPC8260 through the Buffered Data bus. The Buffered data bus supplies a buffered MPC8260 address and a bi-directional 8 or 16 bit data bus. The $\overline{\text{CS_FLASHB}}$ supplied by the MPC8360, acts as the device chip enable. The $\overline{\text{BUF_RD}}$ supplied by PSM497PAL logic acts as the device output enable and $\overline{\text{BUF_WR}}$ again supplied by the PSM497 logic is the write enable.

NOTE: The CPC395 has a write protect feature that will not allow the $\overline{\text{BUF_WR}}$ signal to activate unless the FLASH_WP bit is set in the General Purpose registers.

The default after reset is to disable writing to the flash. The read and write cycle is timed by the GCPM's wait state programming. There is no cycle termination signal generated by the device.

MPC8260 Related Flash Settings

The MPC8260 uses its chip select 0 (CS0) as the $\overline{\text{CS_FLASHB}}$ signal. The CS0 Base Register is set to define the address space as FFF0_0000h to FFF7_FFFF H. The following is a list of recommended Base and Option Register field settings other than the base address and address masks:

Table 29. CS0 Base Register Settings

Field	Recommended Setting	Description
PS	01	8-bit
DECC	00	Data Errors checking disabled
WP	0	Read and write accesses are allowed
MSEL	000	Machine Select GPCM-60x bus

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Table 29. CS0 Base Register Settings *(Continued)*

Field	Recommended Setting	Description
EMEMC	0	Accesses are handled by the MSEL selected controller. No external memory controller allowed in this space.
ATOM	00	The address space is controlled by the memory controller bank and is not used for atomic operations
DR	0	No data pipelining is done.
V	1	This bank is valid

The Option Register Settings follow the form outlined for the GPCM Machine:

Table 30. CS0 Option Register Settings

Field	Recommended Setting	Description
BCTLD	0	$\overline{\text{BCTLx}}$ is asserted upon access to the current memory bank
CSNT	1	$\overline{\text{CS}}$/WE is negated a quarter of a clock early.
ACS	11	$\overline{\text{CS}}$ is output half a clock after the address lines.
SCY	6	Clock Wait states
SETA	0	$\overline{\text{PSDVAL}}$ is generated by the GCPM.
TRLX	1	Relaxed timing is generated by the GCPM for this memory region.
EHTR	00	Normal Idle Timing

General Flash Information

Flash access in the read mode is done as any normal PROM device. The programming or write operations are entirely command set compatible with the JEDEC single-power-supply flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Device programming occurs by executing the program command sequence. This initiates the Embedded Program algorithm, an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

Device erasure occurs by executing the erase command sequence. This initiates the Embedded Erase algorithm, an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin. The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data/Polling) and DQ6 (toggle) status bits. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

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The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. Device hardware data protection measures include a low VCC detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both the program and erase operations in any combination of the sectors of memory. This is achieved via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

3.7 Application Flash Memory

The Application Flash PROM is used to store application code that will not be executed at boot up time. The device is permanently mounted to the PCB at position U4. The Application flash is a non-volatile memory that has the following general characteristics:

- The flash is a single power supply, 16 Mbyte, 3.0 volt-only flash memory device.
- Read accesses to the device are the same as any EPROM. The data appears on DQ0-DQ7 on the buffered data bus.
- For writing purposes, the device has 127 blocks of byte-wide data storage. The storage blocks have 128Kbytes of storage each.
- Selecting, writing and erasing the blocks is done by using a Common Flash Interface (CFI) and a Scaleable Command Set (SCS).
- All read, erase, and program operations are accomplished using only a single power supply. Internally generated and regulated voltages are provided for the program and erase operations.
- The device package is a 56-pin TSOP.

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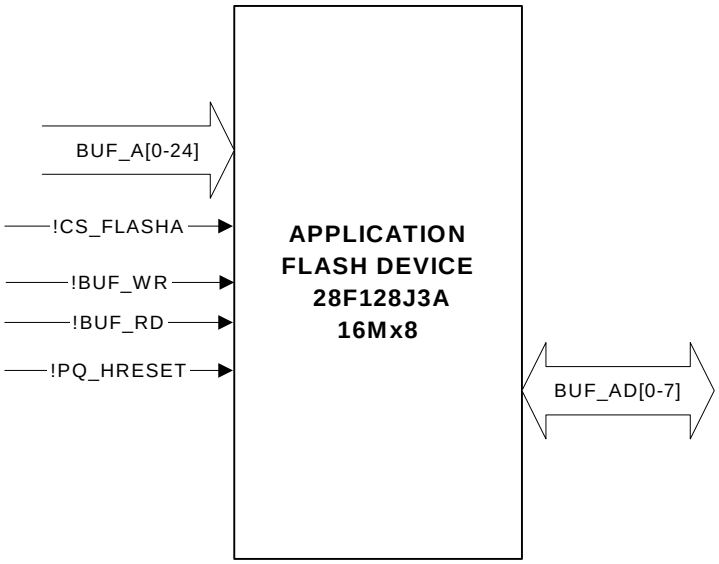


Figure 12. Application Flash Block Diagram

The device is accessed by the MPC8260 through the Buffered Data Bus. The Buffered Data Bus supplies a buffered MPC8260 address and a bi-directional 8 or 16 bit data bus. The $\overline{\text{CS_FLASHA}}$ is supplied by the PMC8260 and acts as the device chip enable. The $\overline{\text{BUF_RD}}$ is supplied by the PSM497 PAL logic and acts as the device output enable. The PSM497 also supplies the $\overline{\text{BUF_WR}}$ strobe which is the write enable.

Note: The CPC395 has a write protect feature that will not allow the $\overline{\text{BUF_WR}}$ signal to activate unless the FLASH_WP bit is set in the General Purpose registers.

The default after reset is to disable writing to the flash. The read and write cycle is timed by the GCPM's wait state programming. There is no cycle termination signal generated by the device.

MPC8260 Related FLASH Settings

The MPC8260 uses its chip select 3 (CS3) as the $\overline{\text{CS_FLASHA}}$ signal. The CS3 Base Register is set to define the address space as 1000_0000h to 10FF_FFFF H. The following is a list of recommended Base and Option Register field settings other than the base address and address masks:

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Table 31. CS3 Base Register Settings

Field	Recommended Setting	Description
PS	01	8-bit
DECC	00	Data Errors checking disabled
WP	0	Read and write accesses are allowed
MSEL	000	Machine Select GPCM-60x bus
EMEMC	0	Accesses are handled by the MSEL selected controller. No external memory controller allowed in this space.
ATOM	00	The address space is controlled by the memory controller bank and is not used for atomic operations
DR	0	No data pipelining is done.
V	1	This bank is valid

The Option Register Settings follow the form outlined for the GPCM Machine:

Table 32. CS3 Option Register Settings

Field	Recommended Setting	Description
BCTLD	0	$\overline{\text{BCTLx}}$ is asserted upon access to the current memory bank
CSNT	1	$\overline{\text{CS}}$/WE is negated a quarter of a clock early.
ACS	11	$\overline{\text{CS}}$ is output half a clock after the address lines.
SCY	6	Clock Wait states
SETA	0	$\overline{\text{PSDVAL}}$ is generated by the GCPM.
TRLX	1	Relaxed timing is generated by the GCPM for this memory region.
EHTR	00	Normal Idle Timing

General Application Flash Information

Flash access in the read mode is done as with any normal PROM device. Selecting, writing and erasing the blocks is done by using a Common Flash Interface (CFI) and a Scaleable Command Set (SCS). Please refer to “3-Volt Intel STRATAFlash^{tm} Memory Datasheet” for the command set and the programming strategy.

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3.8 Time of Day Timer

The Time of Day (TOD) Timer is an integrated ultra low power SRAM, real time clock, power fail-control circuit with a top mounted “SNAPHAT” battery. The device is available to be used as scratch SRAM, a real time clock or a watchdog timer.

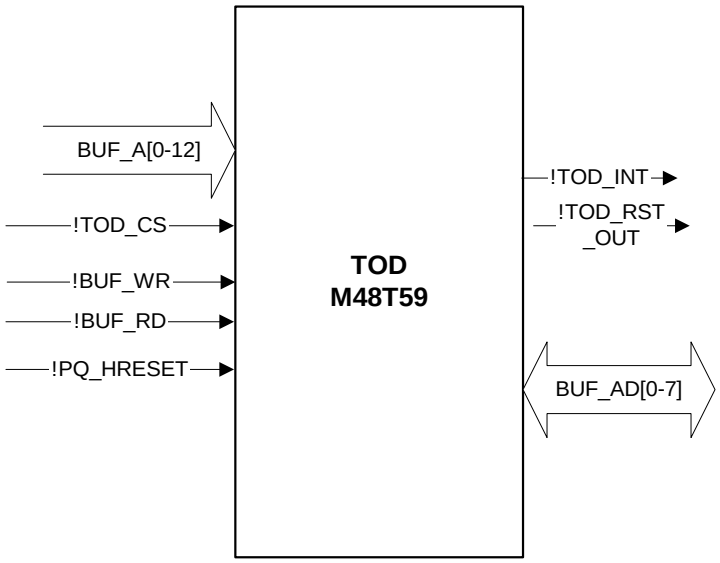


Figure 13. TOD Block Diagram

The device is accessed by the MPC8260 through the buffered data bus. The buffered data bus supplies a buffered MPC8260 address and a bi-directional 8 or 16-bit data bus. The $\overline{\text{TOD_CS}}$ is supplied by the MPC8260 and acts as the device chip enable. The $\overline{\text{BUF_RD}}$ is supplied by the PSM497 PAL logic and acts as the device output enable. The PSM492 also supplies the $\overline{\text{BUF_WR}}$ strobe which is the write enable. The read and write cycle is timed by the GCPM’s wait state programming. There is no cycle termination signal generated by the device. This particular device has 5 volt I/O and passes through an extra 74LVC245A data buffer to connect to the 3.3 volt buffered data bus.

MPC8260 Related TOD Settings

The MPC8260 uses its chip select 8 (CS8) as the $\overline{\text{TOD_CS}}$ signal. The CS8 Base Register is set to define the address space as 2030_0000h to 2030_7FFF H. The following is a list of recommended Base and Option Register field settings other than the base address and address masks:

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Table 33. CS8 Base Register Settings

Field	Recommended Setting	Description
PS	01	8-bit
DECC	00	Data Errors checking disabled
WP	0	Read and write accesses are allowed
MSEL	000	Machine Select GPCM-60x bus
EMEMC	0	Accesses are handled by the MSEL selected controller. No external Memory controller allowed in this space.
ATOM	00	The address space is controlled by the memory controller bank and is not used for atomic operations
DR	0	No data pipelining is done.
V	1	This bank is valid

The Option Register Settings follow the form outlined for the GPCM Machine:

Table 34. CS8 Option Register Settings

Field	Recommended Setting	Description
BCTLD	0	$\overline{\text{BCTLx}}$ is asserted upon access to the current memory bank
CSNT	1	$\overline{\text{CS}}$/WE is negated a quarter of a clock early.
ACS	11	$\overline{\text{CS}}$ is output half a clock after the address lines.
SCY	5	Clock Wait states
SETA	0	$\overline{\text{PSDVAL}}$ is generated by the GCPM.
TRLX	1	Relaxed timing is generated by the GCPM for this memory region.
EHTR	00	Normal Idle Timing

General TOD Information

The M48T59vTIMEKEEPER® RAM is an 8Kb x8 non-volatile static RAM and real time clock. The monolithic chip is a highly integrated battery backed-up memory and real time clock solution.

The M48T59 is a non-volatile pin and function equivalent to any JEDEC standard 8Kb x8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of ROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

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The 28-pin 600mil DIP SNAPHAT battery houses the M48T59/59Y silicon with a quartz crystal and a long life lithium button cell in a single package. The unique design allows the SNAPHAT battery package to be mounted on top of the package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The Watchdog and Real Time functions embedded in the part can be connected internally to either the $\overline{\text{TOD_RST_OUT}}$ reset line or the $\overline{\text{TOD_INT}}$ interrupt lines. Activation of the reset lines causes an MPC8260 soft reset. The interrupt will cause an MPC8260 interrupt on the Port C1 line.

For information on how to set up the clock and watchdog timer, please refer to the “ST Micro MT48T59 64Kbit (8Kb x8) TIMEKEEPER® SRAM” datasheet.

3.9 Communications Buffer Memory

The Communications Buffer Memory is used by the Communications Processor Module (CPM) in the MPC8260. The memory array is interfaced directly to the 8260’s local bus connection. The local bus interface is tightly coupled to the CPM inside the part making it an ideal resource for use as a high-speed buffer memory for data and commands.

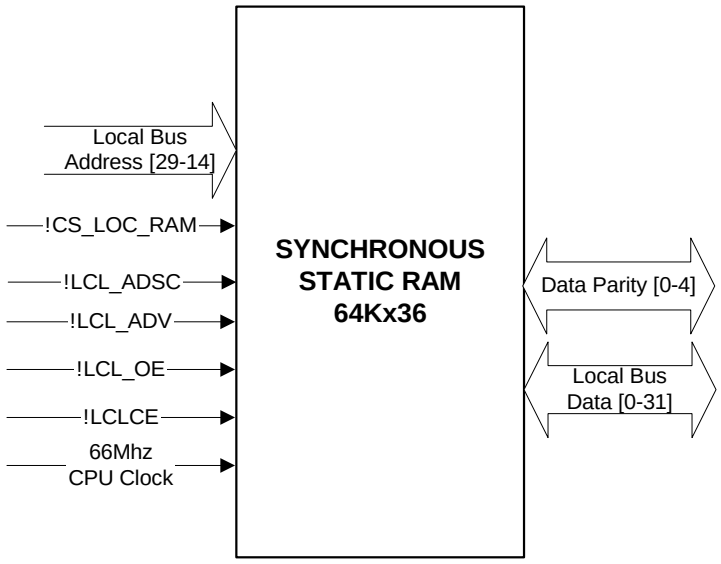


Figure 14. Communications Buffer Memory Block Diagram

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The Communications Memory Buffer is implemented with synchronous static random access memory (SSRAM) operating at 3.3V. 256KB of data are available and organized as 64K x 32-bits of data. The flow-through device is supported, as opposed to the pipelined device. Individual parity for each byte lane is provided in 64K x 4-bits of memory (the default controller setting is parity disabled). Both data and parity are implemented in a monolithic component that is wired directly to the MPC8260 local bus.

The device is controlled by the MPC8260's Universal Programmable Memory (UPMB) controller. A 66MHz clock is provided to the memory from the same low-skew clock driver that provides 66MHz to the MPC8260. The active-high and active low chip selects are permanently enabled via external resistors. Global Write Enable (GWE#) is pulled-up to permanently disable the global override of byte-write enable. Address Status Processor (ADSP#) is pulled-up to permanently disable burst abort with READ override. Snooze (ZZ) is grounded to permanently disable snooze. Burst mode (LBO#) is grounded to permanently select linear burst. FT#/Vss is a ground pin on this device.

The memory interface consists of 32 data (LCL_D[0-31]), 4 byte-parity (LCL_DP[0-4]), 4 byte-write selects (LCL_LBS[0-3]), 1 write enable ($\overline{\text{CS_LOC_RAM}}$), 1 Address Status Controller ($\overline{\text{LCL_ADSC}}$), 1 Address Advance ($\overline{\text{LCL_ADV}}$), 1 output enable ($\overline{\text{LCL_OE}}$), 1 chip enable ($\overline{\text{LCL_CE}}$), and 16 address (LCL_A29-A14). The seventeenth address connection to memory is grounded. $\overline{\text{LCL_OE}}$, $\overline{\text{LCL_ADSC}}$, $\overline{\text{LCL_ADV}}$, and $\overline{\text{LCL_CE}}$ are driven from the MPC8260s LGPL[0-3] pins, respectively.

MPC8260 Related Communications Buffer Memory Settings

The MPC8260 uses its chip select 2 (CS2) as the $\overline{\text{CS_LOC_RAM}}$ signal. The CS2 Base Register is set to define the address space as 20800_0000h to 2083_FFFF H. The following is a list of recommended Base and Option Register field settings other than the base address and address masks:

Table 35. CS2 Base Register Settings

Field	Recommended Setting	Description
PS	11	32-bit
DECC	00	Data Errors checking disabled (default)
WP	0	Read and write accesses are allowed
MSEL	101	Machine Select UPMB for Local Bus
EMEMC	0	Accesses are handled by the MSEL selected controller. No external Memory controller allowed in this space.
ATOM	00	The address space is controlled by the memory controller bank and is not used for atomic operations
DR	0	No data pipelining is done.
V	1	This bank is valid

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The Option Register Settings follow the form outlined for the UPMB Machine:

Table 36. CS2 Option Register Settings

Field	Recommended Setting	Description
BCTLD	1	$\overline{\text{BCTLx}}$ is not asserted upon access to the current memory bank
BI	0	This Bank of memory supports bursting
EHTR	00	Normal Idle Timing

UPMB Table Settings

The UPMB Table settings are as follows:

```
; single read   (offset 0x00 in upm ram)
            .long     0xffe33000    0xffaff005    0xfffff000    0xfffff000
            .long     0xfffff000    0xfffff000    0xfffff000    0xfffff000
; burst read    (offset 0x08 in upm ram)
            .long     0xffe33008    0xffacf00c    0xffacf00c    0xffacf00c
            .long     0xffa33004    0xffacf004    0xffacf004    0xffacf004
            .long     0xffaff005    0xfffff000    0xfffff000    0xfffff000
            .long     0xfffff000    0xfffff000    0xfffff000    0xfffff000
; single write  (offset 0x18 in upm ram)
            .long     0x00f33005    0xfffff000    0xfffff000    0xfffff000
            .long     0xfffff000    0xfffff000    0xfffff000    0xfffff000
; burst write   (offset 0x20 in upm ram)
            .long     0x00f3300c    0x00fcf00c    0x00fcf00c    0x00fcf00c
            .long     0x00f33004    0x00fcf004    0x00fcf004    0x00fcf005
            .long     0xfffff000    0xfffff000    0xfffff000    0xfffff000
            .long     0xfffff000    0xfffff000    0xfffff000    0xfffff000
; refresh       (offset 0x30 in upm ram)
            .long     0xfffff005    0xfffff000    0xfffff000    0xfffff000
            .long     0xfffff000    0xfffff000    0xfffff000    0xfffff000
            .long     0xfffff000    0xfffff000    0xfffff000    0xfffff000
; exception     (offset 0x3C in upm ram)
            .long     0xfffff005    0xfffff000    0xfffff000    0xfffff000

UPMBTableEnd:
```


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3.10 CompactPCI Interface

The Dual PCI PowerSpan, part number CA91L8200, is a three port device which has two PCI interfaces and a PowerPC processor bus interface. The PowerSpan operates as a non-transparent PCI-to-PCI bridge in which the primary and the secondary address spaces are independent. The PowerSpan also offers address translation between the primary and the secondary buses. Each PCI interface has its own configuration space. This configuration space cannot be accessed by Type 0 configuration cycles initiated from the opposite PCI interface. Also, the PowerSpan does not accept Type 1 configuration cycles. These features allow the local processor to have complete PCI configuration control of subsystem devices, without interference from the host. In the CPC395 implementation, the secondary PCI bus is not used. The primary PCI bus and the PowerPC buses are used.

PowerSpan Signal Connections and Hardware Configuration

The bus interface signals between PowerSpan and the MPC8260 are directly connected. External pull-up resistors are connected to all bus control signals to ensure that they are held in an inactive state when not accessed. In addition, pull-up resistors are provided on the address and data bus interfaces to minimize current consumption of the buffers when tri-stated.

No provision has been made for parity checking on either the address or data presented to the Tundra. This choice was made due to the multiplexed nature of the MPC8260 pins being used for interrupts and bank selection of the SDRAM memory.

Since either the MPC8260 or the PowerSpan can be bus masters of the 60x bus, and both have internal arbiters, one part must be selected as the master. The MPC8260 is selected as the master and uses its internal arbiter. The PowerSpan connections for address bus or data bus requests are programmed to be outputs, and are therefore inputs to the MPC8260 arbiter.

The MPC8260 sees the Tundra 60x bus registers at 3000_0000 to 3000_0fff H, which is the default 60x bus address decode for the Tundra device.

The CompactPCI P1 connection is designed to be a 64-bit interface that can be either 33 Mhz or 66 Mhz, configurable by jumper K17. On the CPC395, the secondary PCI port is not used.

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Additional Documentation

For further information on circuit connection, description, and operation, refer to the following documents available in the PowerSpan Design Support Tools section of the Tundra web site, www.tundra.com:

- 80A1000_FB001_04.pdf: PowerSpan Feature Brief
- 80A100B_AN001_01.pdf: PowerSpan (CA91L8200) as a PCI-to-PCI Bridge
- 80A100A_AN001_01.pdf: PowerSpan (CA91L8200) MPC8260 Connection Application Note
- 80A1000_ER001_06.pdf: PowerSpan (CA91L8200/CA91L8260) Device Errata and Design Notes
- 80A1000_MA001_08.pdf: PowerSpan (CA91L8260, CA91L8200) PowerPC-to-PCI Bus Switch Manual

Due to a Tundra component problem, a circuit modification was included which adds an additional load on the P1-IDSEL line. Also, the present parts have timing issues with the PCI bus running at 66 Mhz. Refer to the following document for an explanation from Tundra:

80A1000_ER001_06.pdf – PowerSpan (CA91L8200/CA91L8260) Device Errata and Design Notes

PowerSpan Reset Configuration Word

The MPC8260 system provides support for a single configuration master and up to seven configuration slaves. In the CPC395, the MPC8260 is set up to be the configuration master. During the assertion of HRESET, the configuration master (MPC8260) reads configuration words from memory and writes them to the configuration slaves. A total of seven 64-bit words are transferred over the data bus. One of Address[0:6] lines is strobed to transfer each word.

The PowerSpan acts as a configuration slave because the following conditions have been preset:

- PB_RSTCONF connected to one of MPC8260 Address[0:6]
- PB_RST connected to MPC8260 HRESET
- PB_D[0-31] connected to MPC8260 D[0-31]

The reset configuration word consists of eight bits set on the PB_D[0-7] bits:

bit 0 - 0 - disable PB arbiter - PowerSpan is not the 60X arbiter
bit 1 - 0 - disable PCI-1 arbiter - PowerSpan is not the PCI-1 arbiter
bit 2 - 1 - enable PCI-2 arbiter - PowerSpan is the PCI-2 arbiter
bit 3 - 0 - PCI-1 is primary PCI
bit 4 - 1 - disable PCI-1 REQ64
bit 5 - 0 - PB Boot - get local configuration from the processor bus.
bit 6 - 0 - disable debug mode
bit 7 - 0 - disable PLL bypass mode

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Local Processor Connections Between MPC8260 and PowerSpan

The design is similar to the referenced Tundra documentation with the exception of signals described below in Table 37. The variation is in the selection of the MPC8260 as the bus arbiter and the inability to select the pin modes due to the multiplexed pins on the MPC8260. Also, a different means of controlling the board reset is done either by the MPC8260 processor or CompactPCI bus.

Table 37. Signal Variations Between PowerSpan and the MPC8260

Power Span Signal	MPC8260 Signal	Description or comments
$\overline{\text{PB_BR}}$[1]	$\overline{\text{BR}}$	Address Bus Request – 8260 arbitration
$\overline{\text{PB_BG}}$[1]	$\overline{\text{BG}}$	Address Bus Grant – 8260 arbitration
$\overline{\text{PB_DBG}}$[1]	$\overline{\text{DBG}}$	Data Bus Grant – 8260 arbitration
$\overline{\text{PB_DBB}}$	$\overline{\text{DBB}}$	Data Bus Busy – 8260 arbitration
PB_AP[0:3]	AP[0:3]	Address bus parity - not used
PB_DP[0:7]	DP[0:7]	Data bus parity - not used
$\overline{\text{PB_CI}}$	$\overline{\text{CI}}$	Cache Inhibit – not used

The following table itemizes the Reset operation of the CPC395 PCI ports.

Table 38. PowerSpan Reset Pins

Pin Name	Direction	Description	Comments
PO_RST	Input	Power-On Reset	Voltage Level Sense
HEALTHY	Input	Board Status	Power Good Asserts Signal
PB_RST	Input	Processor Bus Hard Reset	PB_RST_DIR = 0 (Input) HRESET generated
P1_RST#	Input	PCI-1 Bus Reset	P1_RST_DIR = 0 (Input) CPCI bus generated
P2_RST#	Output	PCI-2 Bus Reset	P2_RST_DIR = 1 (Output) CPCI or register controlled
TRST	Input	JTAG Reset	Voltage Level Sense

PowerSpan Interrupts

The following table documents the interrupt connections from the PowerSpan.

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Table 39. PowerSpan Interrupt Connections

Power Span Signal	MPC8260 Signal	Description or comments
$\overline{\text{INT_3}}$	$\overline{\text{PQ_IRQ4}}$	Address Bus Request – 8260 arbitration
$\overline{\text{INT_4}}$	$\overline{\text{PQ_IRQ3}}$	Address Bus Grant – 8260 arbitration
$\overline{\text{INT_5}}$	$\overline{\text{PQ_SRESET}}$ (via PAL logic)	Mailbox generates SRESET To MPC8260

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3.11 Fast Ethernet Controller

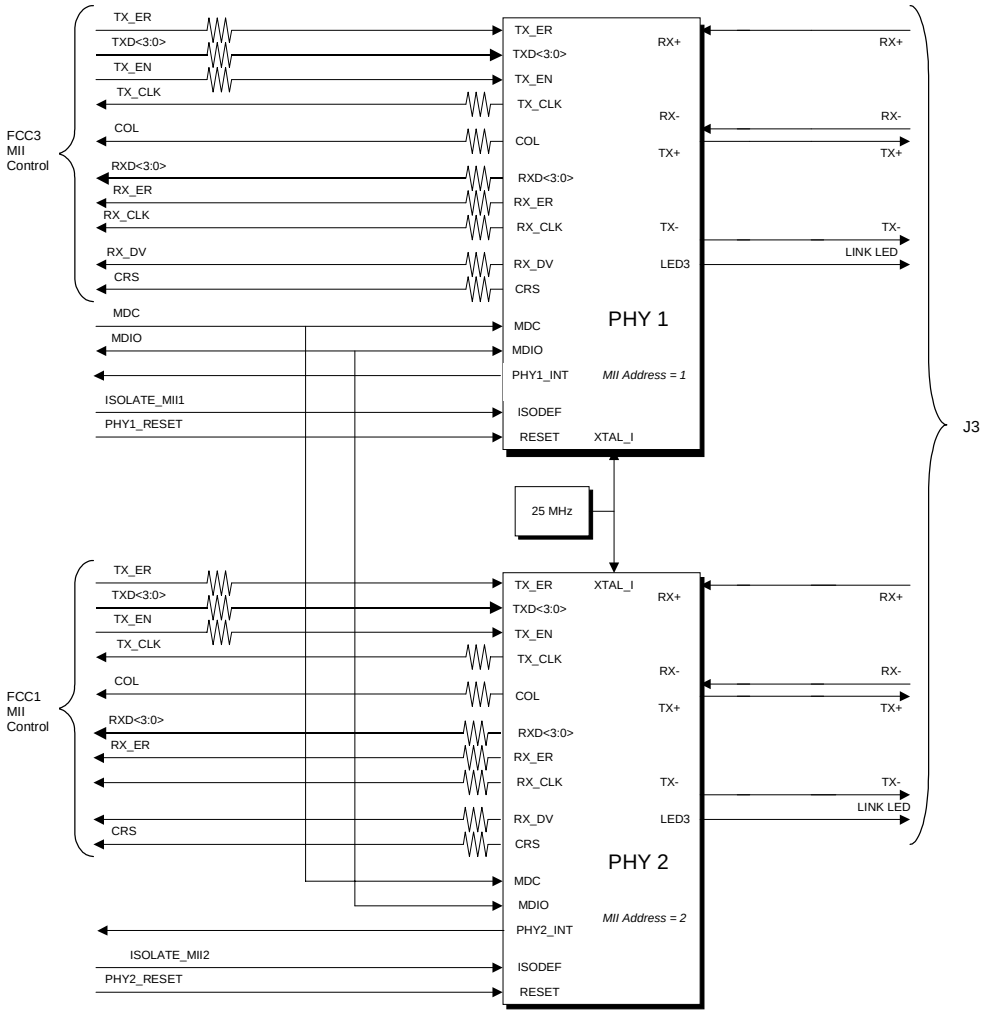


Figure 15. Fast Ethernet Controllers Block Diagram

There are two independent Fast Ethernet Controller channels on the CPC395 board. Each is composed of a Cirrus Logic CS8952 Transceiver (PHY) and an MII bus connection to a MPC8260 PowerQUICC II Fast Communication Controller (FCC). The FCC1 and FCC3 controllers are used for the individual channels. The

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isolation magnetics and terminations for each channel are located on the Rear Transition Module (RTM). The signals for each channel can be routed out an RJ45 connector on the RTM or turned back into the midplane for a cable-less connection to the switch fabric.

A 25MHz shielded surface mount oscillator (+/- 100 ppm) supplies the clock to both PHYs.

The MII bus of the CS8952 operates at +3.3V (separate power supply pins for the MII, core of the part needs +5V). Series resistors are provided to reduce the rise/fall times for EMI considerations.

For management communication with both PHYs, the MPC8260 PowerQUICC II uses a serial management interface using the MDIO and MDC signals programmed on General Purpose I/O pins on port B. The MDIO is on Port B-19 and the MDC is on Port B-18. The PHY that is connected to FCC3 has address 1 and the PHY that is connected to FCC1 has address 2. MII bus signals have pull-up/pull-down resistors that are read at reset to obtain these addresses.

Each CS8952 PHY has configuration pins that determine its mode of operation at reset. These can be over-ridden using the serial management interface. The following table lists those pins and their settings as implemented on the CPC395:

Table 40. 10/100 Base-T Ethernet PHY Reset Settings

Signal Name	Description	Reset Setting
RX_EN	Receive Enable	Pulled high internally to enable MII bus receive signals
10BT_SER	10Mb/s Serial Mode Select	Pulled down internally to select 4-bit parallel MII bus data
AN0	Auto-Negotiate Control 0	This is left floating to select the maximum capability of 100 or 10 Mb/s, Auto-Negotiation enabled, full or half duplex
AN1	Auto-Negotiate Control 1	This is left floating to select the maximum capability of 100 or 10 Mb/s, Auto-Negotiation enabled, full or half duplex
BP4B5B	Bypass 4B5B Coders	Pulled down internally so that 4B5B coding is NOT bypassed. Some repeaters use a five bit mode (faster). Most network interface cards use four bit encoded data.
BPALIGN	Bypass Alignment	Pulled down internally so that alignment is NOT bypassed
BPSCR	Bypass Scrambler	Pulled down internally so that scrambler is NOT bypassed. The scrambler is bypassed for 100BASE-FX (fiber optic) only.
ISODEF	Isolate Default	This is a programmable bit from the MISC register. Set high to isolate MII bus. Clear low to enable MII bus.
LPBK	Loopback Enable	Grounded externally to disable local loopback
/LPSTRT	Low Power Start	Pulled up externally so that PHY powers up immediately
PWRDN	Power Down	Grounded externally so that PHY is not powered down

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Table 40. 10/100 Base-T Ethernet PHY Reset Settings *(Continued)*

Signal Name	Description	Reset Setting
REPEATER	Repeater Mode	Pulled down internally so that the Carrier Sense operates normally (in a non-repeater mode)
TCM	Transmit Clock Mode	Grounded externally so that TX_CLK is output and CLK25 disabled
TEST0	Factory Test 0	Tied directly to VSS (Ground) for normal operation
TEST1	Factory Test 1	Tied directly to VSS (Ground) for normal operation
TXSLEW0	Transmit Slew Rate Control 0	Left floating for 2.5 ns rise/fall time (the value from the ANSI standard)
TXSLEW1	Transmit Slew Rate Control 1	Left floating for 2.5 ns rise/fall time (the value from the ANSI standard)

The Link LED control signal (/LED3) and the Activity LED control signal (/LED2) for each PHY is brought to the PSM502 PAL. Each pair is logically combined within the PAL to provide a combination signal $\overline{\text{LINK1}}$ (PHY1) and $\overline{\text{LINK2}}$ (PHY2) that is brought out the J3 connector to the RTM. Each signal can indicate a LINK condition by a steady true condition and Link + Activity by a True/False blinking mode. The remaining LED lines, LED1 – Transmit Activity (active low), LED2 – Receive Activity (active low), LED4 – Polarity/Full Duplex (active low), LED5 – Collision/Descrambler Lock (active low), SPD10 – 10Mb/s Speed Indication (active high) and SPD100 - 100Mb/s Speed Indication (active high) are not supported.

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Each PHY has an individual Interrupt line that is passed through the PSM501PAL logic and then on to the MPC8260. The sources of the MII_INT assertion is selected through the Interrupt Mask Register 10h. The possible selections are:

- Carrier Integrity Monitor Link Unstable
- Link Status Change
- Descrambler Lock Change
- Premature End Error
- DCR Rollover
- FCCR Rollover
- RECR Rollover
- Remote Loopback Fault
- Reset Complete
- Jabber Detect
- Auto-Neg Complete
- Parallel Detection Fault
- Parallel Fail
- Remote Fault
- Page Received

Each PHY can be electrically isolated on its MII bus ISODEF pin at RESET or by bit 10 (Isolate) of the Basic Mode Control Register (00h), which is programmable by the MII Serial Management Interface. The MPC8260 supplies the ISODEF signal to each PHY on a general purpose I/O pin on port B21 (PB21_ISOLATE_MII1) and B22 (PB22_ISOLATE_MII2) of the MPC8260. The signals are pulled high on power up allowing the isolation condition to exist until the port can be programmed as an output.

There is an individual reset line to each PHY. PHY1_RESET and PHY2_RESET both originate from the PMS502 logic. They both default to true on power up or a hard or soft reset. The bit must be cleared by writing to the appropriate general purpose register. (See “General Purpose Status and Control Registers” on page 111.) The active high PHY_RESET bit should only be cleared after the isolate signals have been set up and programmed correctly on the MPC8260 ports.

3.12 TDM Clock Distribution and Control

The TDM clock distribution is centralized about a pair of Mitel MT90866 H.110 TDM switches. These devices generate all of the local TDM Frame Pulses and data clocks. They use a variety of clock sources to lockup their internal digital phase locked loops (DPLL) to a system reference. This connectivity ensures that

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the data transferred on the board stays in synchronization with the system and that no timing slips occur. Refer to Figure 16 on page 79 for a visual representation of the circuit. The following sections describe the general features of a single switch. Where appropriate, distinction will be made between the two switches on the board.

H.110 Switch DPLL

The core of the part is the Digital Phase Locked Loop (DPLL). The DPLL has a 20MHz 25ppm signal source as its primary clock input. This clock directly drives the DPLL. The DPLL accuracy and the 25ppm input clock, allows each H.110 switch to function as a Stratum 4 Enhanced clock source when it runs in a free run mode. In a normal integration into a Telephony system, synchronized timing is maintained by locking the PLL to a system-supplied reference. Some of the important PLL specifications are listed in Table 41.

Table 41. H.110 DPLL Operating Specifications

Parameter	Value
Acceptable Reference Clock Input Frequencies	1.544MHz , 2.048MHz or 8kHz.
Skew Control	8 taps @ 1.9ns each, allows 0 to13.3ns total skew adjustment between reference input and clock outputs. This translates to static phase offset of 1.28us to 1.293us for reference clock input of 1.544Mhz. For a reference clock input of 8kHz or 2.048Mhz, the static phase offset is 960ns to 973ns.
Phase Offset, dependent on reference clock frequency	For 1.544Mhz reference clock, maximum phase offset +/- 1.28 us, minimum phase adjustment 10ns. For 8kHz or 2.048Mhz reference clock, maximum phase offset +/- 0.96us, minimum phase adjustment 7.5ns.
Phase Slope Limiter	Maximum phase slope response for input transient 4.6ns per 125us.
Loop Filter	Equivalent to a first order low pass filter with 1.52 Hz cutoff.
Intrinsic Jitter	6.25nspp for the 80MHz Master clock.
Jitter Transfer	Rate limited by Phase Slope Limiter to 4.6ns/125us. Jitter Transfer Function Cutoff frequency 1.52Hz with slope of 20db/decade. Please refer to the datasheet for the actual curves and the UI calculations.
Frequency Accuracy	Master Clock/ppm + DPLL/ppm= 25+.03=25.03ppm of selected frequency.
Holdover accuracy	Same as above calculation
Locking Range	+/- 273ppm
Maximum Time Interval Error (MTIE)	21ns for every reference switch.
Phase Continuity	Maintained to within 4.6ns at the instance (over one frame) of all reference switches.
Phase Lock Time	Less than 25 seconds

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As mentioned above, the DPLL can choose from several input sources to obtain the signal it needs to lock to. This mechanism is what supplies the system synchronization. These clock sources can be selected either internally via the reference mux internal to the part or externally by the PSM499 PAL logic. Please refer to the “Mitel MT9088 WAN Access Switch Data Sheet” for further information on internal clock selections.

Internal Reference Clock Sources

The internal reference selector mux for the DPLL has a redundant configuration. The primary and secondary muxes both have access to the same set of clock sources. These sources include any of the 8 local reference inputs: the A and B CT bus clocks or the CT Netreferences from the CT bus.

Internal Reference Monitors

There are two Reference Monitor Circuits: one for the primary reference (PRI_REF) and one for the secondary reference (SEC_REF). These two circuits monitor the selected input reference signals and detect failures by setting up the adequate internal fail outputs (FAIL_PRI and FAIL_SEC). These fail signals are used in the Autodetect mode as the internal LOS_PRI and LOS_SEC signals to indicate when the reference is failed. Method of generating failure depends on the selected reference:

- For all references, the “minimum 90ns” check is done. This is the requirement by the H.110 specifications. Both low level and high level of the reference must last for minimum 90ns each.
- The “period in the specified range” check is done for all references. The length of the period of the selected input reference is checked if it is in the specified range. For the E1 (2.048 MHz clock) or the T1 (1.544 MHz clock) reference, the period of the clock can vary within the range of 1 +/- 1/4 of the defined clock period which is 488ns for the E1 clock and 648ns for T1 clock. For the 8KHz reference, the variation is from 1 +/- 1/32 period.
- If the selected reference is E1 or T1, “64 periods in the specified range” check is done. The selected reference is observed for long period (64 reference clock cycles) and checked if it is within the specified range - from 62 to 66 clock periods.

These reference signal verifications include a complete loss or a large frequency shift of the selected reference signal. When the reference signal returns to normal, the LOS_PRI and LOS_SEC signals will return to logic low.

CT Clock and Frame Monitor Circuits

These monitor circuits check the period of the C8_A and the C8_B clocks and the FRAME_A and FRAME_B frame pulses. According to the H.110 signal specification, the C8 period is 122 ns with a tolerance of +/-35 ns measured between rising edges. If C8 falls outside the range of [87ns,157ns], the clock is rejected and the fail signal (FAIL_A or FAIL_B) becomes high. The Frame pulse period is measured with respect to the C8 clock. The frame pulse period must have exactly 1024 C8 cycles. Otherwise, the fail signal (FAIL_A or FAIL_B) becomes high. This pair of signals, a set from each switch, are connected to the PSM501 PAL logic. The PAL groups the signals and transforms them into the H.110 interrupt for each switch

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to the MPC8260. The PAL also has logic that can disable, enable, mask and unmask the interrupt conditions. Details surrounding their function are outlined in “PSM501 Interrupt Mask and Control Registers” on page 120.

External Reference Clock Sources

These sources include any of the recovered clocks from the TEMUX A or B T1 recovered clock output, the Monitor FALC’s receivers, the A or B H.110 switch’s 1.544 MHz clock output or a 25 ppm 1,544 MHz on board clock reference. The clock sources are connected to the PSM499 PAL logic, which is internally programmed to select one of 9 source inputs. There are six of these selectors and they feed the A_PRI, A_SEC, A_TER, B_PRI, B_SEC, B_TER on the A and B H.110 chip local primary, secondary and tertiary local reference inputs. Refer to “PSM499 Clock Multiplexer Registers” on page 144.

External Reference Clock Source Monitor

There is a set of clock monitors in the PSM499 logic that will check the external clock sources for the selector muxes for validity. The A and B side primary and secondary clocks are monitored. There is a Clock Timer Timeout Period Register for each of the A and B primary and secondary clocks. Each register contains a clock count value that is used to check for a valid time period for the local reference clocks fed from the PSM499 select multiplexer to the respective H.110 Switch chip. The timer value is the maximum number of 20 MHz clocks that are allowed to elapse during the reference clock period. If the 20 MHz count is exceeded without seeing at least one valid local reference clock, an interrupt status indicator signal is set. The four possible output signals are, A_PRI_INT, A_SEC_INT, B_PRI_INT, and B_SEC_INT. The signals are all routed to the PSM501 Interrupt PAL logic for inclusion as either the A side or B side H.110 interrupt. Please see “PSM501 Interrupt Mask and Control Registers” on page 120 for the timer value registers and their appropriate settings.

H.110 Clock Operating Modes

The H.110 switches have several functions with respect to the various clocks generated by and distributed on the CPC395. On the H.110 side, Internal and External clock distribution and control circuitry within the H.110 switches support both master and slave modes of H.110 operation. The H.110 switches also source all of the local TDM clocks, locked to the appropriate master source.

In the H.110 master mode, each switch accepts two of several local clock references that may be recovered by the TEMUX T1 framers, one of the Monitor FALCs or by an optional local precision oscillator. These clocks are supplied by the A and B-side Clock multiplexer PAL logic located in the PSM499 PAL logic. The signals are phase lock the internal switch DPLL and are used to generate the various clock output signals. For the H.110 bus, the H.110 backplane clocks CT_C8_A and CT_C8_B are generated. CT Bus clocking is at 8MHz exclusively. In addition, the DPLL generates and drives the CT_FRAME_A or CT_FRAME_B 8KHz synchronization pulses for the backplane. The selected local reference clocks are monitored and cause an interrupt upon failure. Local status and masking is provided for these interrupt sources.

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While in Master Mode, each CT bus, A and B side clock and frame synchronization are monitored by the H.110 switch and failure causes the corresponding A or B, FAIL_A or FAIL_B signal to be asserted. This signal is intercepted and provided as an interrupt to the MPC8260 through the PSM501 PAL logic. Local status and masking is provided for this interrupt source.

When either switch is the CT Bus clock master, support is included to allow A-side and B-side source termination resistors on CT_C8_A/B and CT_FRAME_A/B to be bypassed. See "Telecom Control Register 7" on page 142 for the appropriate bit settings for these signals.

In slave mode, the H.110 switch accepts CTREF1, CTREF2, CT_C8_A and CT_C8_B clocks. One CTREF and one CT_C8 clock are selected for primary operation, while the alternate pair can stand-by as secondary clocks.

There is a tertiary clock output from the clock multiplexer that is sourced on the local reference inputs as well. This input is intended to be divided down into an 8 KHz reference signal within each H.110 switch and then used to source the CTREF1 or CTREF2 signal on each switch's H.110 backplane for primary or secondary master operation.

For more information on the Switch setup and control please refer to the "Mitel MT9088 WAN Access Switch Data Sheet."

Local TDM Clocking

Each H.110 switch provides clock and frame synchronization sources for the local TDM streams. These are distributed to the MPC8260, A and B side TEMUX framers, the interswitch elastic store, clock monitoring circuitry and the A and B side Monitor FALCS. The local TDM clock is generated by the switch at 16.384MHz operation exclusively. However 8.192MHz and 4.096Mhz are also generated by the local clock distribution logic found in the PSM503 PAL for use by the devices that require them.

A 20MHz crystal oscillator is distributed on the CPC395 to provide a 20MHz clock for each of the H.110 switches, the monitor FALCs, and general-purpose logic components. These are dedicated clocks without control options.

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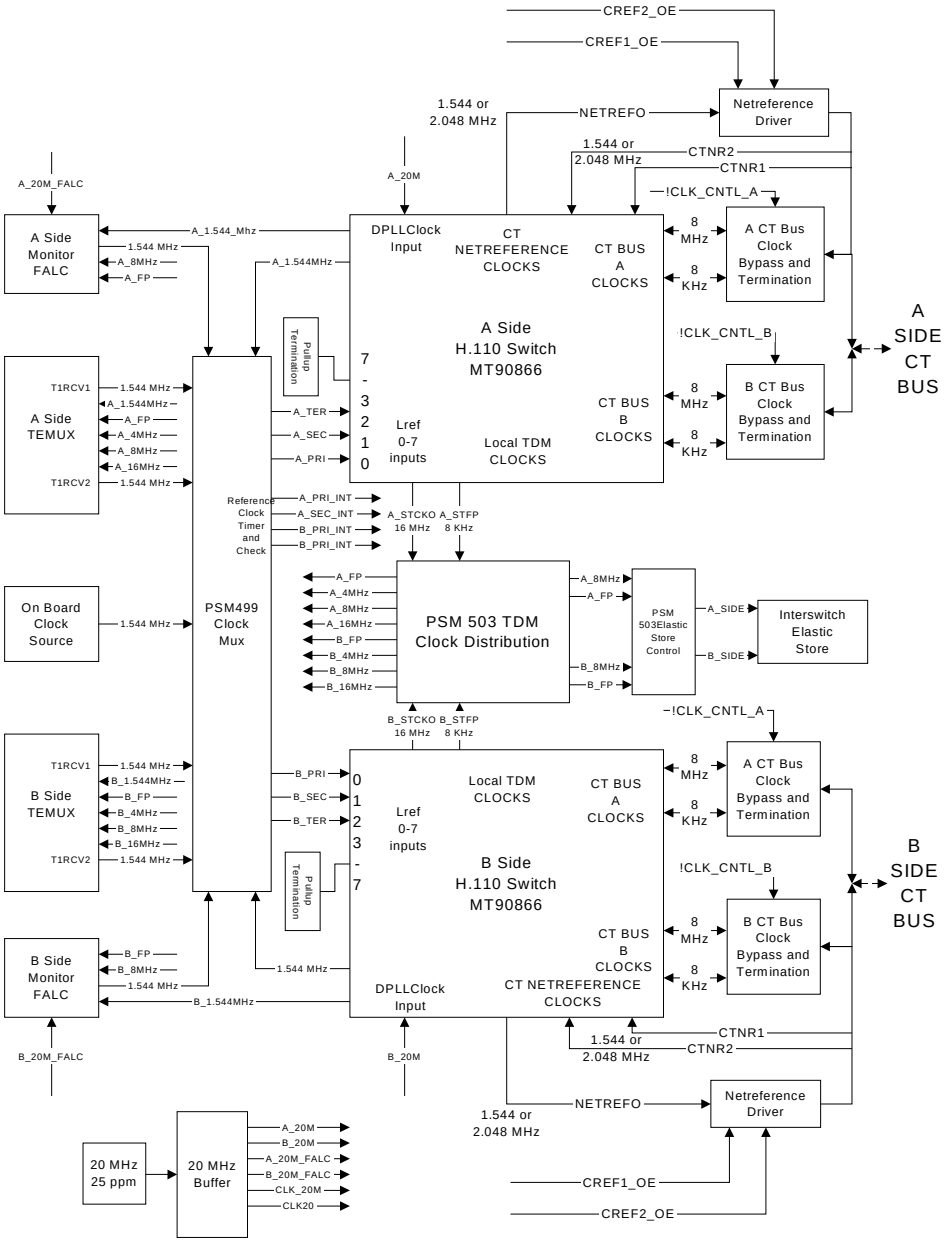


Figure 16. CPC395 TDM Clock Tree

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3.13 H.110 Buses and Local TDM Switches

The CPC395 uses a pair of Mitel MT90866 WAN switches to connect the various Time Division Multiplexed (TDM) interface streams together and provide a connection to a conventional J4 midplane H.110 CT bus and an optional J3 midplane H.110 CT bus. The local side TDM connections include the MPC8260's TDM I/O, ports B1 and B2, both T3 framers' 28 T1s, the dual T1Monitor FALCs and an Inter-Switch Elastic Store. See "Figure 17. H.110 Data and Control" on page 82.

The switches themselves feature:

- 3.3V operation with 5V tolerant inputs and I/O's
- 5V tolerant PCI driver on CT-Bus I/O's
- 2,432 x 2,432 non-blocking switching among local streams
- 4,096 x 2,432 blocking switching between backplane and local streams
- 2,048 x 2,048 non-blocking switching among backplane streams
- Rate conversion between backplane and local streams
- Rate conversion among local streams
- Backplane interface accepts data rate of 8.192Mb/s
- Local interface accepts data rates of 2.048Mb/s, 4.096Mb/s or 8.192Mb/s
- Sub-rate switching (2 or 4 bits) configuration for local streams at a data rate of 2.048Mb/s
- Per-channel variable or constant throughput delay
- Fully compliant to H.110 timing specification
- Per-stream input delay, programmable for local streams on a per bit basis
- Per-stream output advancement, programmable for backplane and local streams
- Per-channel direction control for backplane streams
- Per-channel message mode for backplane and local streams
- Compatible to Stratum 4 Enhanced clock switching standard
- Integrated PLL conforms to Bellcore Stratum 4 Enhanced switching standard
- Holdover mode with hold over frequency of 0.07ppm
- Wander attenuation from 1.5Hz.
- Time interval error (TIE) correction
- H.110 Bus Master and Slave mode operation
- Connection memory block programming for fast device initialization
- Tristate-control outputs for external drivers

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- Pseudo-Random Binary Sequence (PRBS) pattern generation and testing for backplane and local streams

General Description

Each MT90866 Digital Switch provides switching capacities of 4,096 x 2,432 channels between backplane and local streams, 2,432 x 2,432 channels among local streams and 2,048 x 2,048 channels among backplane streams. The local connected serial inputs and outputs can support 32, 64 and 128 64kb/s channels per frame with data rates of 2.048, 4.096 and 8.192Mb/s respectively. The backplane connected serial inputs and outputs have 128 64kb/s channels per frame with data rate of 8.192 Mb/s. The device has features that are programmable on a per-stream or per-channel basis including message mode, input delay offset, output advancement offset, direction control and high impedance output control.

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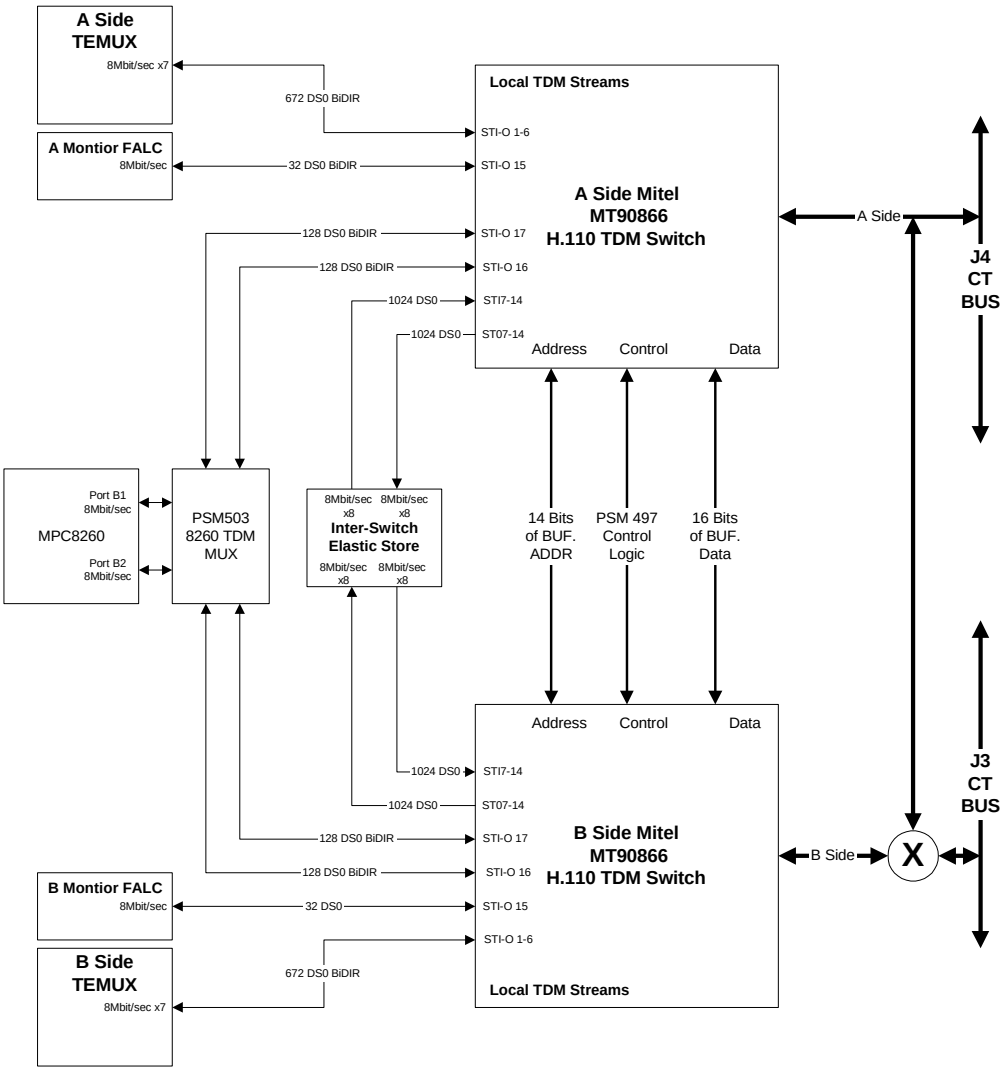


Figure 17. H.110 Data and Control

The devices CPU interface is accessed by the MPC8260 for setup and control purposes through the Buffered Data bus. The Buffered data bus supplies a buffered MPC8260 address and a bi-directional 16 bit data bus. There is a chip select assigned to each device. The chip select for the A side switch, $\overline{\text{CS_H110_A}}$, is supplied

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by the MPC8260 on $\overline{CS6}$. The chip select for the B side switch, $\overline{CS_H110_B}$ is supplied by the MPC8260 on $\overline{CS7}$. The $\overline{BUF_DS}$ is supplied by the PSM497 PAL logic and acts as the device data strobe in Motorola signaling mode. The PSM497 also supplies the BUF_RW# strobe, which is the read/write, enable.

Each H.110 device uses a transfer acknowledge signal, ($\overline{DTA_H110}$) to signal completion of data transfers on the Buffered Data Bus. This signal is synchronized to the MPC8260 clock in the PSM497 PAL and reissued as $\overline{PQ_PGTA}$ to the MPC8260. This signal is used by the GCPM to recognize the completion of the access and either terminates the cycle in the case of a write, or latch the data on the 60x bus in the case of a read.

NOTE: Data transfers for this device are 16 bit in nature. The device does not support 8 bit transfers, even though the Buffered Data Bus does support them. Therefore sequential addresses in the device are all offset by 2 Hex, 0000, 0002, 0004, etc. Be aware that an 8 bit write is still allowed to happen but any byte write will still cause a 16 bit write to the device.

MPC8260 Related H.110 Settings

The A side switch uses the MPC8260's Chip Select 6 for CPU accesses. The GPCM is used to control the cycles.

Table 42. CS6 Base Register Settings

Field	Recommended Setting
PS	10 16-bit
DECC	00 Data Errors checking disabled
WP	0 Read and write accesses are allowed
MSEL	000 Machine Select GPCM-60x bus
EMEMC	0 Accesses are handled by the MSEL selected controller. No external memory controller allowed in this space.
ATOM	00 The address space is controlled by the memory controller bank and is not used for atomic operations
DR	0 No data pipelining is done.
V	1 This bank is valid

The Option Register Settings follow the form outlined for the GPCM Machine:

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Table 43. CS6 Option Register Settings

Field	Recommended Setting
BCTLD	0 $\overline{\text{BCTLx}}$ is asserted upon access to the current memory bank
CSNT	1 $\overline{\text{CS}}$/WE is negated a quarter of a clock early.
ACS	11 $\overline{\text{CS}}$ is output half a clock after the address lines.
SCY	6 Clock Wait states
SETA	1 $\overline{\text{PSDVAL}}$ is generated after external logic asserts $\overline{\text{GTA}}$
TRLX	1 Relaxed timing is generated by the GCPM for this memory region.
EHTR	00 Normal Idle Timing

The B side switch uses the MPC8260's Chip Select 7 for CPU accesses. The GPCM is used to control the cycles.

Table 44. CS7 Base Register Settings

Field	Recommended Setting
PS	10 16-bit
DECC	00 Data Errors checking disabled
WP	0 Read and write accesses are allowed
MSEL	000 Machine Select GPCM-60x bus
EMEMC	0 Accesses are handled by the MSEL selected controller. No external memory controller allowed in this space.
ATOM	00 The address space is controlled by the memory controller bank and is not used for atomic operations
DR	0 No data pipelining is done.
V	1 This bank is valid

The Option Register Settings follow the form outlined for the GPCM Machine:

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Table 45. CS7 Option Register Settings

Field	Recommended Setting
BCTLD	0 $\overline{\text{BCTLx}}$ is asserted upon access to the current memory bank
CSNT	1 $\overline{\text{CS}}$/WE is negated a quarter of a clock early.
ACS	11 $\overline{\text{CS}}$ is output half a clock after the address lines.
SCY	6 Clock Wait states
SETA	1 $\overline{\text{PSDVAL}}$ is generated after external logic asserts $\overline{\text{GTA}}$
TRLX	1 Relaxed timing is generated by the GCPM for this memory region.
EHTR	00 Normal Idle Timing

The address range for the different internal sections of the part is as follows:

Table 46. H.110 Digital Switch Register Map

Address	Register	Function	Type	Initial Value
CS6(7)+0000h	CR	Control Register	Read/Write, 16 Bit	0x0000
CS6(7)+0002h	DMS	Device Mode Selection Register	Read/Write, 16 Bit	0x0000
CS6(7)+0004h	BPM	Block Programming Mode Register	Read/Write, 16 Bit	0x0000
CS6(7)+0008h	LIDR0	Local Input Delay Register 0	Read/Write, 16 Bit	0x0000
CS6(7)+000Ah	LIDR1	Local Input Delay Register 1	Read/Write, 16 Bit	0x0000
CS6(7)+000Ch	LIDR2	Local Input Delay Register 2	Read/Write, 16 Bit	0x0000
CS6(7)+000Eh	LIDR3	Local Input Delay Register 3	Read/Write, 16 Bit	0x0000
CS6(7)+0010h	LIDR4	Local Input Delay Register 4	Read/Write, 16 Bit	0x0000
CS6(7)+0012h	LIDR5	Local Input Delay Register 5	Read/Write, 16 Bit	0x0000
CS6(7)+0014h	LIDR6	Local Input Delay Register 6	Read/Write, 16 Bit	0x0000
CS6(7)+0018h	LIDR7	Local Input Delay Register 7	Read/Write, 16 Bit	0x0000
CS6(7)+001Ah	LIDR8	Local Input Delay Register 8	Read/Write, 16 Bit	0x0000
CS6(7)+001Ch	LIDR9	Local Input Delay Register 90	Read/Write, 16 Bit	0x0000
CS6(7)+0038h	BOAR0	Backplane Output Advancement Register 0	Read/Write, 16 Bit	0x0000
CS6(7)+003Ah	BOAR1	Backplane Output Advancement Register 1	Read/Write, 16 Bit	0x0000
CS6(7)+003Ch	BOAR2	Backplane Output Advancement Register 2	Read/Write, 16 Bit	0x0000

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Table 46. H.110 Digital Switch Register Map *(Continued)*

Address	Register	Function	Type	Initial Value
CS6(7)+003Eh	BOAR3	Backplane Output Advancement Register 3	Read/Write, 16 Bit	0x0000
CS6(7)+0040h	LOAR0	Local Output Advancement Register 0	Read/Write, 16 Bit	0x0000
CS6(7)+0042h	LOAR1	Local Output Advancement Register 1	Read/Write, 16 Bit	0x0000
CS6(7)+0044h	LOAR2	Local Output Advancement Register 2	Read/Write, 16 Bit	0x0000
CS6(7)+0046h	LOAR3	Local Output Advancement Register 3	Read/Write, 16 Bit	0x0000
CS6(7)+004Eh	LBIS	Local Bit Error Rate Input Selection Register	Read/Write, 16 Bit	0x0000
CS6(7)+0050h	LBERR	Local Bit Error Rate Register	Read/Write, 16 Bit	0x0000
CS6(7)+0052h	BBIS	Backplane Bit Error Rate Input Selection Register	Read/Write, 16 Bit	0x0000
CS6(7)+0054h	BBERR	Backplane Bit Error Rate Register	Read/Write, 16 Bit	0x0000
CS6(7)+0056h	DOM1	DPLL Operation Mode 1 Register	Read/Write, 16 Bit	0x0000
CS6(7)+0058h	DOM2	DPLL Operation Mode 2 Register	Read/Write, 16 Bit	0x0000
CS6(7)+005Ah	DPOA	DPLL Output Adjustment Register	Read/Write, 16 Bit	0x0000
CS6(7)+005Ch	DHKR	DPLL House Keeping Register	Read/Write, 16 Bit	0x0000
CS6(7)+0400h to 7FFFh		Connection Memory Setup and Connection Memory Data depending on Memory Selection Bits in Control Register		
CS6(7)+0400h to 16FEh		MS=0 Local Connection Memory Low Bits	Read/Write, 16 Bit	Undefined
CS6(7)+040h0 to 16FEh		MS=1 Local Connection Memory High Bits	Read/Write, 16 Bit	Undefined
CS6(7)+0400h to 23FEh		MS=2 Backplane Connection Memory	Read/Write, 16 Bit	Undefined
CS6(7)+0400h to 16FEh		MS=3 Local Data Memory Read Bits	Read/Write, 16 Bit	Undefined
CS6(7)+0400h to 23FEh		MS=4 Backplane Data Memory Read	Read/Write, 16 Bit	Undefined

For information on how to use the registers in the H.110 TDM Switch, please refer to the “Mitel Semiconductor MT9866 WAN Access Switch Datasheet.”

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Digital Switch Local TDM Streams Connection

The H.110 switches serve as the focal point for all of the TDM streams from the various onboard peripherals. Refer to "Figure 17. H.110 Data and Control" on page 82 for a complete view of the peripheral connections. Each switch's local I/O connections are grouped as inputs and outputs. The inputs and outputs are also sub-grouped in fours. This allows each sub-group to be run at one of the available data rates: 2.048, 4.096 or 8.192 Mbits/sec. Some of the sub-groups will also support 2 and 4-bit sub-rate switching when the group is run at the 2.048Mbits/sec data rate. The Local TDM clock for each of the A and B side devices is sourced from the respective switch's DPLL and is fixed at 16.384 MHz. The DPLL is locked to a system reference, which is programmable and chosen by the system architect. The Local Frame Pulse signal is 8KHz and is also supplied by the DPLL locked to the system reference. The following tables list the peripheral connections for each of the A and B side devices for the CPC395 and the data rate at which the link operates.

Table 47. A-Side Digital Switch Local TDM Streams Connection

Group	Device	Switch Connection	TDM Data Rate	Interleaving Format/DS-0 Mapping
Group 0	A side TEMUX D1 TDM Stream	Sti0/Sto0	8.192 Mbits/sec	4 Streams x 24 DS-0s stream with byte interleave and unused DS-0 byte stuffing. Defined by TEMUX.
	A side TEMUX D2 TDM Stream	Sti1/Sto1	8.192 Mbits/sec	4 Streams x 24 DS-0s/stream with byte interleave and unused DS-0 byte stuffing. Defined by TEMUX.
	A side TEMUX D3 TDM Stream	Sti2/Sto2	8.192 Mbits/sec	4 Streams x 24 DS-0s/stream with byte interleave and unused DS-0 byte stuffing. Defined by TEMUX.
	A side TEMUX D4 TDM Stream	Sti3/Sto3	8.192 Mbits/sec	4 Streams x 24 DS-0s/stream with byte interleave and unused DS-0 byte stuffing. Defined by TEMUX.
Group 1	A side TEMUX D5 TDM Stream	Sti4/Sto4	8.192 Mbits/sec	4 Streams x 24 DS-0s/stream with byte interleave and unused DS-0 byte stuffing. Defined by TEMUX.
	A side TEMUX D6 TDM Stream	Sti5/Sto5	8.192 Mbits/sec	4 Streams x 24 DS-0s/stream with byte interleave and unused DS-0 byte stuffing. Defined by TEMUX.

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Table 47. A-Side Digital Switch Local TDM Streams Connection *(Continued)*

Group	Device	Switch Connection	TDM Data Rate	Interleaving Format/DS-0 Mapping
	A side TEMUX D7 TDM Stream	Sti6/Sto6	8.192 Mbits/sec	4 Streams x 24 DS-0s/stream with byte interleave and unused DS-0 byte stuffing. Defined by TEMUX.
	Elastic Store Stream 0	Sti7/Sto7	8.192 Mbits/sec	Configured by Connection Memories
Group 2	Elastic Store Stream 1	Sti8/Sto8	8.192 Mbits/sec	Configured by Connection Memories
	Elastic Store Stream 2	Sti9/Sto9	8.192 Mbits/sec	Configured by Connection Memories
	Elastic Store Stream 3	Sti10/Sto10	8.192 Mbits/sec	Configured by Connection Memories
	Elastic Store Stream 4	Sti11/Sto11	8.192 Mbits/sec	Configured by Connection Memories
Group 3	Elastic Store Stream 5	Sti12/Sto12	8.192 Mbits/sec	Configured by Connection Memories
	Elastic Store Stream 6	Sti13/Sto13	8.192 Mbits/sec	Configured by Connection Memories
	Elastic Store Stream 7	Sti14/Sto14	8.192 Mbits/sec	Configured by Connection Memories
	A_MONITOR_RDO/ A_MONITOR_XDI	Sti15/Sto15	8.192 Mbits/sec	For T1, 24 DS-0s with idle channel insertion every 4th channel. Phase channel transmission using 1 of four 2Mbit phases available on 8 Mbit connection.
Group 4	A_TDM_MUX_IN1 A_TDM_MUX_OUT1	Sti16/Sto16	8.192 Mbits/sec	Input side from MPC8260 connection memory, output side from Switch connection memory.
	A_TDM_MUX_IN2 A_TDM_MUX_OUT2	Sti17/Sto17	8.192 Mbits/sec	Input side from MPC8260 connection memory, output side from Switch connection memory.
	Pulled Up	Sti18/Sto18	8.192 Mbits/sec	None
	Pulled Up	Sti19/Sto19	8.192 Mbits/sec	None
	Pulled Up	Sti20/Sto20	8.192 Mbits/sec	None
	Pulled Up	Sti21/Sto21	8.192 Mbits/sec	None
	Pulled Up	Sti22/Sto22	8.192 Mbits/sec	None

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Table 47. A-Side Digital Switch Local TDM Streams Connection *(Continued)*

Group	Device	Switch Connection	TDM Data Rate	Interleaving Format/DS-0 Mapping
	Pulled Up	Sti23/Sto23	8.192 Mbits/sec	None
	Pulled Up	Sti24/Sto24	8.192 Mbits/sec	None
	Pulled Up	Sti25/Sto25	8.192 Mbits/sec	None
	Pulled Up	Sti26/Sto26	8.192 Mbits/sec	None
	Pulled Up	Sti27/Sto27	8.192 Mbits/sec	None

Table 48. B-Side Digital Switch Local TDM Streams Connection

Group	Device	Switch Connection	TDM Data Rate	Interleaving Format/ DS-0 Mapping
Group 0	B side TEMUX D1 TDM Stream	Sti0/Sto0	8.192 Mbits/sec	4 Streams x 24 DS-0s stream with byte interleave and unused DS-0 byte stuffing. Defined by TEMUX.
	B side TEMUX D2 TDM Stream	Sti1/Sto1	8.192 Mbits/sec	4 Streams x 24 DS-0s/stream with byte interleave and unused DS-0 byte stuffing. Defined by TEMUX.
	B side TEMUX D3 TDM Stream	Sti2/Sto2	8.192 Mbits/sec	4 Streams x 24 DS-0s/stream with byte interleave and unused DS-0 byte stuffing. Defined by TEMUX.
	B side TEMUX D4 TDM Stream	Sti3/Sto3	8.192 Mbits/sec	4 Streams x 24 DS-0s/stream with byte interleave and unused DS-0 byte stuffing. Defined by TEMUX.
Group 1	B side TEMUX D5 TDM Stream	Sti4/Sto4	8.192 Mbits/sec	4 Streams x 24 DS-0s/stream with byte interleave and unused DS-0 byte stuffing. Defined by TEMUX.
	B side TEMUX D6 TDM Stream	Sti5/Sto5	8.192 Mbits/sec	4 Streams x 24 DS-0s/stream with byte interleave and unused DS-0 byte stuffing. Defined by TEMUX.
	B side TEMUX D7 TDM Stream	Sti6/Sto6	8.192 Mbits/sec	4 Streams x 24 DS-0s/stream with byte interleave and unused DS-0 byte stuffing. Defined by TEMUX.

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Table 48. B-Side Digital Switch Local TDM Streams Connection *(Continued)*

Group	Device	Switch Connection	TDM Data Rate	Interleaving Format/ DS-0 Mapping
	Elastic Store Stream 0	Sti7/Sto7	8.192 Mbits/sec	Configured by Connection Memories
Group 2	Elastic Store Stream 1	Sti8/Sto8	8.192 Mbits/sec	Configured by Connection Memories
	Elastic Store Stream 2	Sti9/Sto9	8.192 Mbits/sec	Configured by Connection Memories
	Elastic Store Stream 3	Sti10/Sto10	8.192 Mbits/sec	Configured by Connection Memories
	Elastic Store Stream 4	Sti11/Sto11	8.192 Mbits/sec	Configured by Connection Memories
Group 3	Elastic Store Stream 5	Sti12/Sto12	8.192 Mbits/sec	Configured by Connection Memories
	Elastic Store Stream 6	Sti13/Sto13	8.192 Mbits/sec	Configured by Connection Memories
	Elastic Store Stream 7	Sti14/Sto14	8.192 Mbits/sec	Configured by Connection Memories
	B_MONITOR_RDO/ B_MONITOR_XDI	Sti15/Sto15	8.192 Mbits/sec	For T1, 24 DS-0s with idle channel insertion every 4th channel. Phase channel transmission using 1 of four 2Mbit phases available on 8 Mbit connection.
Group 4	B_TDM_MUX_IN1 B_TDM_MUX_OUT 1	Sti16/Sto16	8.192 Mbits/sec	Input side from MPC8260 connection memory, output side from Switch connection memory.
	B_TDM_MUX_IN2 B_TDM_MUX_OUT 2	Sti17/Sto17	8.192 Mbits/sec	Input side from MPC8260 connection memory, output side from Switch connection memory.
	Pulled Up	Sti18/Sto18	8.192 Mbits/sec	None
	Pulled Up	Sti19/Sto19	8.192 Mbits/sec	None
	Pulled Up	Sti20/Sto20	8.192 Mbits/sec	None
	Pulled Up	Sti21/Sto21	8.192 Mbits/sec	None
	Pulled Up	Sti22/Sto22	8.192 Mbits/sec	None
	Pulled Up	Sti23/Sto23	8.192 Mbits/sec	None
	Pulled Up	Sti24/Sto24	8.192 Mbits/sec	None
	Pulled Up	Sti25/Sto25	8.192 Mbits/sec	None

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Table 48. B-Side Digital Switch Local TDM Streams Connection *(Continued)*

Group	Device	Switch Connection	TDM Data Rate	Interleaving Format/ DS-0 Mapping
	Pulled Up	Sti26/Sto26	8.192 Mbits/sec	None
	Pulled Up	Sti27/Sto27	8.192 Mbits/sec	None

3.14 Interswitch Elastic Store

The interswitch elastic store is used to couple the two MT90866 TDM switches together. This is done by cross-connecting 8 of the local input and output lines on each switch, as indicated in Figure 18.

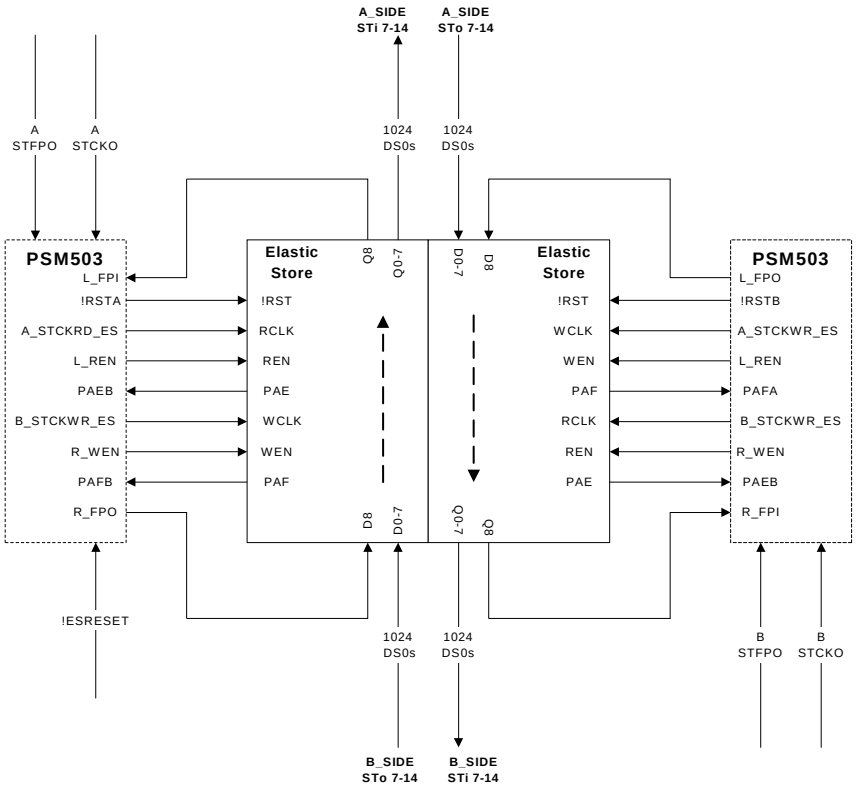


Figure 18. Interswitch Elastic Store Block Diagram

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The cross-connection is done through the Elastic Store device itself, which is a pair of large Dual Port RAMs that can hold more than an entire frame's worth of data (128 DS-0s) for each Sti/o line from each switch. Logic in the PSM503 PAL controls the synchronization to each of the A and B side TDM streams and the control of the reading and writing of the data to the RAM.

The Elastic Store can only be used when both T3 interfaces' time domains are synchronized to a common clock reference. When this requirement is met the local TDM clocks, A/B_STCKO (16.384 Mhz bit rate clock) and A/B_STFPO (8Khz Frame Pulse) will not slip against one another. However each pair of signals is not phase locked to the pair on the other side. This fact requires that the clocking in of the TDM data to the RAM follow the data source's clocking and clocking out of the data from the RAM follows the destination's clocking. The device functionality is described in detail in the following sections.

Elastic Store Initialization

The Elastic store is initialized by two signals. The first is the MPC8260's soft reset. Any time this signal is true, the PSM503 control logic will clear all of its state machines and counters and assert the reset signal to each of the RAMs to clear them out. The $\overline{\text{ESRESET}}$ signal when asserted has the same effect on the logic. The $\overline{\text{ESRESET}}$ signal is controlled by the esreset bit in the telecom control register (see Table 90 on page 135). This bit is controllable by the MPC8260. It is also asserted true by an MPC8260 soft reset. The power-on state of the Elastic store is initialized.

Enabling the Elastic Store

When the $\overline{\text{ESREST}}$ is driven false by setting the esreset bit in the telecom control register, the Elastic store is enabled. Before enabling the elastic store it is recommended that both switches be configured so that all of the TDM clocks are present as the device starts up. Although this is not a requirement, it cuts down on the time needed to get the A and B sides synchronized to their respective clocks and allows the data to flow through the part sooner. This is especially true in a situation where the part is being used in a test mode.

Elastic Store Fill

When the elastic store is enabled, a pair of state machines (b2ainctl and a2binctl) that controls each sides' input (write) to the RAM begins to operate. The state machines look for the frame pulse from its' respective TDM data source and then allows the RAM to be filled. The first write to each RAM after a reset will go to memory location 0 in the RAM. The subsequent writes will be put in the RAM in numeric order until the RAM is full. The RAM addressing will then wrap back around to the 0 location. Therefore, the first write to the RAM is synchronized to the data source side's frame pulse, and represents time slot 0 on all of the source streams.

In addition to the data streams being written, whenever the frame pulse is detected, a 0 is written to the ninth data input stream of each RAM on the L/R_FPO signals. At all other times the data written on this stream is a one. The data is used on the output side to confirm the DS-0 time slot 0 memory location of the RAM. It is also used to detect slippage of the clocks on the output side.

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As the Ram begins to fill, a part of the input control state machines checks for two conditions on the RAM fill operation. The first is the detection of the RAM almost empty (PAE) signal being negated. This signal is generated by the RAM device itself and indicates that some minimum number of locations have been written to in the RAM. The second condition that the state machine checks for is the ¼ of a frame mark indicated by an internal counter value. This condition is used to let the RAM fill up to an optimal value so that the greatest slippage compensation can take place between the two local side clock domains without causing an error. The ¼ frame value was chosen to allow the most slippage in the clocks and still allow for full frame buffering on startup.

After this ram fill condition has been detected, the state machine issues a signal to the output side state machine to allow the RAM to drain (empty). At this point the state machine will stay in this fill/empty mode unless one of the following happens, the RAM almost full signal is detected ($\overline{\text{PAFA}}$/B) or the part is initialized by a reset. If the overflow condition occurs the logic will force the state machine into the initialization state and clears the SRAM on its' side (A or B) only. It then resumes the normal startup procedure, looking for the frame pulse and starting up the fill operation.

Elastic Store Drain

There are two state machines in the PSM503 PAL logic (b2aoutctl and a2boutctl) that control emptying or draining the Elastic Store part. The two machines are reset whenever the MPC8260 soft reset is true, the reset to the RAM is asserted or the drain signal from the input state machine controller is false.

The machines begin the data drain operation when the resets are removed and the drain signal from the fill controller is true. The drain controller then starts looking for the output side frame sync pulse. When it sees the pulse, it starts to clock out the RAM data onto the destination TDM streams. It also checks that the Ninth data bit clocked out of the RAM is a logic 0 whenever the Sync pulse is true and a logic 1 at all other times. This ensures that once the drain process begins, the data is checked once a frame to see that it has not slipped against the input side. If for some reason there is a miscompare, the drain controller signals the fill controller to reset.

3.15 MPC8260 TDM Multiplexer

The MPC8260 can terminate TDM data that consist of two 8.192 Mbits/sec, full duplex streams each containing up to 128 DS-0s. The PSM503 PAL logic has a multiplexer that connects the MPC8260 B1 and B2 TDM I/O to the MT90866 switches. The multiplexer can be configured so that either switch can feed all of the 8260's available time slots. It can also be programmed to allow each switch to have access to one of the 8260's TDM channels.

The stream selection is done by the B1_CNTL and B2_CNTL control bits that are set by the b1tdmctl and b2tdmctl bits in the Telecom Control Register 1 (see "Telecom Control Register 1" on page 130). The multiplexer connects to the A and B Local side of the MT90866s on TDM streams 16 and 17.

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3.16 T3/M13 Multiplexer Framers and Line Interface Units (LIUs)

There are two independent T3 interfaces on the CPC395. They are designated T3 A and T3 B. Each T3 interface is composed of a T3 Line Interface Unit (LIU), and a T3 Framer/M13 Multiplexer.

T3 A/B Line Interface Units

The two T3 LIUs are composed of Exar XRT7300 T3 Line Transceivers. The LIUs interface to the T3 framers. When transmitting, the T3 framers provide the LIUs with dual-rail data which is converted into appropriate pulse shapes for transmission over 75 ohm coaxial cable. When receiving, the LIUs perform clock recovery and accept bipolar line signals from the incoming external T3 lines. Optionally, the LIUs can perform receiver equalization on the incoming line signal.

The LIU transmitter accepts TTL or CMOS-level signals from the T3 Framer/M13 Mux on its inputs in dual-rail format. The LIU transmit section will then take this data and encode it into the B3ZS format. However because the T3 Framer/M13 Mux is also capable of B3ZS encoding it is recommended that the LIU encoding be turned off. The LIU pulse shaper will convert the B3ZS encoded data into pulses with shapes that are compliant with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993.

The LIU receive section receives bipolar signal from the Line Interface Module (LIM) via 1:1 transformer. As the receive section receives the line signal, it will adjust the signal level through an AGC circuit and then optionally equalize this signal for cable loss.

LIU Equalization and Line Build-Out

The purpose of receiver equalization is to equalize the distortion of the incoming signal, due to cable loss. For normal operation it is recommended that the receiver equalizer always be enabled. This is controlled by the *areqdis* and *breqdis* bit fields in the telecom control registers 2 and 4. The user should only disable the receive equalizer in applications where the receiver is monitoring the transmit output signal directly.

In typical installations where the CPC395's DS-3 lines interface to a Digital Cross-Connect System the "Transmit Line Build-Out" circuit is set so that the transmit output pulse is compliant with the "Isolated DSX-3 Pulse Template" per the requirements of Bellcore GR-499-CORE. Transmit Line Build-Out for the LIUs are controlled by the *atxlev* and *btxlev* bit fields in the telecom control registers 1 and 3.

LIU Loss of Signal and Loss of Lock

The LIUs will monitor the following two parameters associated with the incoming line signals to determine loss of signal or loss of lock:

- The amplitude of the incoming line signal via the RTIP and RRING inputs;
- The number of pulses, detected (in the incoming line signal) within a certain amount of time.

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If an LIU determines that the incoming line signal is missing, either due to insufficient amplitude or a lack of pulses, then it will declare a “Loss of Signal” (LOS) condition. The LIU declares the LOS condition by toggling the RLOS output pin “high” which sets an interrupt $\overline{\text{PQ_IRQ}}$ 3 for the A side or $\overline{\text{PQ_IRQ}}$ 4 for the B side.

Conversely, if the LIU determines that the incoming line signal has been restored (e.g., there is sufficient amplitude and pulses in the incoming line signal); then it will clear the LOS condition by toggling the RLOS output pin “low”.

The LOS Declaration/Clearance scheme that is employed within the LIU is based on ITU-T Recommendation G.775 for DS-3 applications. The LOS output (RLOS) is simply the logical “OR” of the Analog LOS (ALOS) and the Digital LOS (DLOS) states.

The LIU will declare ALOS whenever the input signal amplitude falls below the pre-declared threshold signal level. The LIU will clear ALOS whenever the input signal rises above a pre-declared threshold. The LIU will declare a DLOS if the LIU detects 160±32 or more consecutive “0s” in the incoming data. The LIU will clear DLOS if it detects four consecutive sets of 32 bit-periods, each of which containing at least 10 “1s” (e.g., average pulse density of greater than 33%).

Table 49. LOS Level

LOSTHR	SIGNAL LEVEL TO DECLARE ALOS	SIGNAL LEVEL TO CLEAR ALOS	EQUALIZER
0	$\leq$55 mv	$\geq$ 220 mv	Enabled
1	$\leq$22 mv	$\geq$ 70 mv	Enabled
0	$\leq$35 mv	$\geq$ 155 mv	Disabled
1	$\leq$17 mv	$\geq$ 70 mv	Disabled

If the LIU is not receiving a line signal or if the frequency difference between the line signal and that applied via the local on board 44.736 MHz clock reference exceeds 0.5%, then the LIU will be operating in “Training Mode”. When the LIU is operating in the “Training Mode”, it will do the following:

- Declare a “Loss of Lock” indication, by setting the *RLOL* bit to 1 in Command/Status Register 2.
- Output a clock signal (via the RCLK1 and RCLK2 output pins) that is derived from the local on board 44.736 MHz clock reference.

If the frequency difference between the line signal and that applied via the on board 44.736 MHz clock reference is less than 0.5%, then the LIU will be operating in the “Data/Clock Recovery” mode. In this mode, the “Clock Recovery” PLL will be “locked” onto the T3 line signal.

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T3 LIU A/B Control Bits

On the CPC395 the LIUs are designed to operate in “Hardware Mode.” The LIU “Host/HW*” input pin (pin 18) is tied to GND. Because the LIUs operate in “Hardware Mode,” the Microprocessor Serial Interface block is disabled and the LIUs are configured via the following input pin settings which are accessed through the Telecom Control Registers (starting on page 130):

- Pin 1 - TxLEV, Transmit Line Build-Out Enable/Disable Select
- Pin 2 - TAOS, Transmit All Ones Select
- Pin 12 - REQDIS, Receive Equalization Disable Input
- Pin 13 - LOSTHR, Loss of Signal Threshold Control
- Pin 14 - LLB, Local Loopback Select
- Pin 15 - RLB, Remote Loopback Select
- Pin 35 - TxOFF, Transmitter Off Input
- Pin 19 - LOSMUTEN, Mute upon Loss of Signal Enable Input
- Pin 21 - ENCODIS, B3ZS/HDB3 Encoder Disable
- Pin 22 - DECODIS, B3ZS/HDB3 Decoder Disable

Setting the Transmit Line Build-Out Circuit

The CPC395 is capable of operating on maximum cable length of 450 ft. from a DSX-3.

The TxLEV input pin or bit-field should be set based upon the overall cable length between the CPC395 and the Digital Cross Connect system (where the pulse template measurements are typically made). If the cable length between CPC395 and the DSX-3 or STSX-1 is less than 225 feet, the user is advised to enable the Transmit Line Build-Out circuit by setting the TxLEV input pin or bit-field to "0".

If the cable length between the CPC395 and the DSX-3 or STSX-1 is greater than 225 feet, the user is advised to disable the “Transmit Line Build-Out circuit” by setting the “TxLEV” input pin or bit-field to "1".

3.17 T3/T1 Synchronization and Clock Recovery

The multiplexing of DS-1 to DS-3 is referred to as M13 multiplexing. A single DS-3 contains 28 DS-1. The process of M13 multiplexing is a two stage operation that first multiplexes 4 DS-1 into a single DS-2 stream at a 6.312 Mbps rate, and then multiplexes 7 DS-2 to a single DS-3 at 44.736 Mbps rate. Therefore, 4 DS-1 in 7 DS-2 is the equivalent of 28 DS-1 in one DS-3. However, 7 times 6.132 Mbps is only 44.184 Mbps, which is 552 Kbits less than 44.736 Mbps. The T3 framer M13 multiplexer adds extra bits, “bit stuffs,” to make up the rate difference of DS-3. M13 multiplexing allows for some variation in bit rate between each of

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the 28 T1 ports and accommodates these variations in bit rate as long as they fall within the M13 capabilities. Accurate, precise network timing synchronous at the DS-1 and DS-3 levels will results in consistent bit stuffing and during the T1 multiplexing process and help eliminate irregularities that cause jitter and wander.

It is the responsibility of the user to insure that the system clock reference of the T1 network is within the required 32 ppm clock rate of T1.

3.18 TEMUX T3 Framer / M13 Multiplexer

The A and B side T3 Framers / M13 Multiplexers are composed of individual PMC 8315 TEMUXs. Each TEMUX is programmed in software to be configured as a T3 Framer and M13 multiplexer. The TEMUXs are physically connected on the system side via their local H-MVIP to the local side of the H.110 switch. On the network side the TEMUXs connect to the receive and transmit interfaces of the T3 LIUs. Each TEMUX supports asynchronous multiplexing and demultiplexing of 672 DS-0s into 28 DS-1s, and 28 DS-1s into a DS-3 signal as specified by ANSI T1.107 and Bell Communications Research TR-TSY-000009.

The TEMUXs are accessed by the MPC8260 for setup and control purposes through the buffered data bus. The buffered data bus supplies a buffered MPC8260 address and a bi-directional 16 bit data bus. The TEMUXs are set up as 8 bit devices on the bus. The chip selects for the TEMUXs are sub-decoded from the MPC8260 CS5 ($\overline{\text{CS_INTERFACE}}$) in PLD PSM499 PAL logic. The sub-decoded signals come out as $\overline{\text{CS_TEMUX_A}}$ and $\overline{\text{CS_TEMUX_B}}$ chip selects. The following table shows the primary chip select address and the PSM499 sub-decode chip selects for the TEMUXs:

Table 50. CS5 Address Decode and Sub-decode

Address	Device
For Base Address, see section	$\overline{\text{CS_INTERFACE}}$
$\overline{\text{CS_INTERFACE}}$+0_0000h $\overline{\text{CS_INTERFACE}}$+0_3FFFh	$\overline{\text{CS_TEMUX_A}}$
$\overline{\text{CS_INTERFACE}}$+0_4000h $\overline{\text{CS_INTERFACE}}$+0_7FFFh	$\overline{\text{CS_TEMUX_B}}$

The cycle control portion of the buffered data bus for this device is supplied by the $\overline{\text{BUF_DS}}$ and BUF_RW# signals. The $\overline{\text{BUF_DS}}$ is supplied by PSM497 PLD logic and acts as the device data strobe in Motorola signaling mode. The PSM497 also supplies the BUF_RW# strobe, which is the read/write, enable. The cycle timing including the cycle termination is handled by the GCPM in the MPC8260. The settings for the $\overline{\text{CS5}}$ ($\overline{\text{CS_INTERFACE}}$) address space and the GPCM are as follows:

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MPC8260 Related TEMUX Settings

Table 51. CS5 Base Register Settings

Field	Recommended Setting	Description
PS	01	8-bit
DECC	00	Data Errors checking disabled
WP	0	Read and write accesses are allowed
MSEL	000	Machine Select GPCM-60x bus
EMEMC	0	Accesses are handled by the MSEL selected controller. No external memory controller allowed in this space.
ATOM	00	The address space is controlled by the memory controller bank and is not used for atomic operations
DR	0	No data pipelining is done.
V	1	This bank is valid

The Option Register Settings follow the form outlined for the GPCM Machine:

Table 52. CS5 Option Register Settings

Field	Recommended Setting	Description
BCTLD	0	$\overline{\text{BCTLx}}$ is asserted upon access to the current memory bank
CSNT	1	$\overline{\text{CS}}$/WE is negated a quarter of a clock early.
ACS	11	$\overline{\text{CS}}$ is output half a clock after the address lines.
SCY	5	Clock Wait states
SETA	0	$\overline{\text{PSDVAL}}$ is generated internally.
TRLX	1	Relaxed timing is generated by the GCPM for this memory region.
EHTR	00	Normal Idle Timing

The address range for the different internal sections of the part can be found in the TEMUX users manual.

TEMUX Operation

In the DS-3 receive direction, the TEMUX frames to DS-3 signals with a maximum average reframe time of 1.5 ms in the presence of 10 -3 bit error rate and detects line code violations, loss of signal, framing bit errors, parity errors, C-bit parity errors, far end block errors, AIS, far end receive failure and idle code. The DS-3 framer is an off-line framer, indicating both out of frame (OOF) and change of frame alignment (COFA)

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events. The error events (C-BIT, FEBE, etc.) are still indicated while the framer is OOF, based on the previous frame alignment. When in C-bit parity mode, the Path Maintenance Data Link and the Far End Alarm and Control (FEAC) channels are extracted. HDLC receivers are provided for Path Maintenance Data Link support. In addition, valid bit-oriented codes in the FEAC channels are detected and are available through the microprocessor port.

TEMUX T1 Synchronization and Clock Recovery

The TEMUXs are required to run in H-MVIP slave mode. The serial clock and data clocking modes are selected via the TEMUX IMODE [1:0] bits in the T1/E1 Ingress Serial Interface Mode Select register. Clock Master mode NxChannel and Clock Master mode Full T1 use the same IMODE [1:0] selection but are differentiated by the TEMUX INXCHAN [1:0] bits in the same register as IMODE [1:0].

When clock slave H-MVIP mode is enabled an 8.192Mb/s H-MVIP egress interface multiplexes up to 672 channels from 28 T1s. The H-MVIP interfaces use common clocks:

- CMV8CLK, 16.384 MHz;
- CMVFPC, 4.096 MHz;
- CMVFPB, 8 KHz frame pulse;
- CT_CLK 1.544 MHz.

These clocks are derived from the H.110 switch and adjusted in PLD PSM503 to match the H.110 switch timing to the requirements of the TEMUX H-MVIP bus.

The receive input clock (RCLK) provides the receive direction timing. RCLK is the DS-3 recovered clock from the LIU. It is a 44.736 MHz with a 50% duty cycle. The transmit output clock (TCLK) provides the transmit direction timing to the DS-3 LIU. It is 44.736 MHz with a 50% duty cycle.

The TEMUXs require two external clocks which are supplied by two crystal clock oscillators. The first, XCLK, is nominally a 37.056 MHz ± 25ppm, 45-55 % duty cycle clock when configured for T1 modes. This clock is required for all operating modes of the TEMUX. It is enabled via the control signal *en44mosc* of “Telecom Control Register 1” on page 130. The second, transmit input clock TICLK provides the transmit direction timing. TICLK is nominally a 44.736 MHz ± 20ppm 40-60 % duty cycle clock. This clock is required by the TEMUX DS-3 transmitter and is used for the DS-3 line side interface and the DS-3 mapper. It is enabled via the control signal *en_37m_osc*. The *en_37_mn* bitfield of telecom control register 1 controls this signal.

Each TEMUX produces two recovered and de-jittered clocks from any two of the 28 T1 framers on clock output lines A_RECVCLK1, A_RECVCLK2, B_RECVCLK1, and B_RECVCLK2. These clocks are fed forward to PLD PSM499 the clock multiplexer where they are used as possible sources for primary, secondary, or tertiary system level synchronization.

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TEMUX Data Connections

The PMC8315 TEMUX manual refers to data path directions as “egress” and “ingress.” “Egress” refers to data traveling from the CPC395 to the T3 network connections, and “ingress” refers to data traveling from the T3 networks into the CPC395. Each TEMUX has seven H-MVIP egress data lines, MVED[1:7] which are connected to an H.110 switch on the local side on output lines STO [0:6]. These connections allow each TEMUX H-MVIP interface to access 672 data channels from its respective H.110 switch. There are 4 T1s worth of data on each egress H-MVIP data line.

Conversely, each TEMUX also has seven H-MVIP ingress data lines, MVID[1:7] which are connected to an H.110 switch on the local side input lines STI [0:6]. These connections allow each TEMUX H-MVIP ingress interface to distribute 672 data channels to its respective H.110 switch. There are 4 T1s worth of data on each ingress H-MVIP data line.

The H-MVIP mapping is fixed such that each group of four nearest neighbor T1 links make up the individual 8.192Mb/s H-MVIP signal. The multiplexed data input is shared with the lowest numbered T1 PCM link in the bundle, for example MVED[2] combines the DS-0s or timeslots of ED [5,6,7,8] and is pin multiplexed with ED [5]. This mode is selected when the SYSOPT [2:0] bits in the TEMUX Global Configuration register are set to H-MVIP.

The TEMUX transmit data interfaces to the T3 LIUs are on signal lines TPOS and TNEG. TPOS carries the positive pulses transmitted on the B3ZS-encoded DS-3 line for dual-rail outputs. While TNEG carries the negative pulses transmitted on the B3ZS-encoded DS-3 line for dual-rail outputs.

Conversely, the TEMUX receive data interfaces from the T3 LIUs are on signal lines RPOS and RNEG. RPOS carries the positive pulses transmitted on the dual-rail inputs. While RNEG carries the negative pulses transmitted on the dual-rail inputs.

T3 Framer Line Loopback

The Line Loopback loops the incoming network side T3 data (the HRCLK, HRPOS, and HRNEG inputs) directly back to the network transmit side (the HTCLK, HTPOS, and HTNEG outputs). When this loopback is enabled, the incoming network receive data continues to pass through the device but the data output from the T3 formatter is replaced with the data being input to the device.

Diagnostic Loopback

The Diagnostic Loopback loops the outgoing T3 data from the T3 formatter toward the network back to receive side framer. When this loopback is enabled, the incoming network receiver data at HRCLK, HRPOS, and HRNEG is ignored. See the Block Diagrams in Section XX for a visual description of this loopback. Please note that the device can still generate AIS at the HTCLK, HTPOS, and HTNEG outputs when this loopback is invoked. This is important to keep the data that is being looped back from disturbing downstream equipment.

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Payload Loopback

The Payload Loopback loops the framed T3 data from the receive side framer back to the transmit side formatter. When this loopback is enabled, the incoming receive data continues to pass through the device but the data normally being input to the T3.

3.19 T1 28 Channel Framer

The CPC395 uses a PMC8315 High Density T1/E1 Framer with M13 Multiplexer (TEMUX). This device is able to operate in T1 mode or E1 mode, but not a mix of T1 and E1 modes.

In the ingress direction, each of the 28 T1 framers is demultiplexed from a channelized DS-3. Each T1 framer can be configured to frame to either of the common DS-1 signal formats (SF or ESF), or to be bypassed (unframed mode). Each T1 framer detects and indicates the presence of Yellow and AIS patterns and also integrates Yellow, Red, and AIS alarms.

T1 performance monitoring is provided, including accumulation of CRTC-6 errors, framing bit errors, out-of-frame events, and changes of frame alignment. The TEMUX also detects the presence of ESF bit-oriented codes, and detects and terminatees HDLC messages on the ESF data link. The HDLC messages are terminated in a 128-byte FIFO. An elastic store that optionally supports slip buffering and adaptation to backplane timing is provided, as is a signaling extractor that supports signaling debounce, signaling freezing, and interrupt on signaling state change on a per-DS-0 basis. The TEMUX also supports idle code substitution and detection, digital milliwatt code insertion, data extraction, trunk conditioning, data sign and magnitude inversion, and pattern generation or detection on a per-DS-0 bases.

In the egress direction, framing is generated for 28 T1s into either a DS-3 ultiplex or a SONET/SDH mapped add bus. Each T1 transmitter frames to SF or ESF DS-1 formats, or framing can be optionally disabled. The TEMUX supports signaling insertion, idle code substitution, data insertion, line loopback, data inversion and zero-code suppression on a per-DS-0 basis. PRBS generation or detection is supported on a framed and unframed T1 basis.

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3.20 T1 A/B FALC Monitor Ports

The CPC395 has two T1 framers with built-in integral line interface units that can be used as a Trunk line monitor or a clock reference input from a master T1. The CPC395 uses the Infineon (Siemens) PEB2256 (FALC) device for this purpose. The FALCs support a multitude of features. Among them are:

- Generic interface for all T1 applications
- Analog receive and transmit circuit for long/short haul applications
- Software selectable T1 mode
- Data and clock recovery using an integrated digital phase locked loop
- Maximum line attenuation up to -43 dB at 1024 kHz (E1) and up to -36 dB at 772 kHz (T1/J1)
- Programmable transmit pulse shapes for T1 pulse masks
- Programmable Line Build-Out for CSU signals according to ANSI T1. 403 and FCC68: 0dB, -7.5dB, -15dB, -22.5 dB (T1)
- Low transmitter output impedances for high transmit return loss
- Tristate function of the analog transmit line outputs
- Transmit line monitor protecting the device from damage
- Receive line monitor mode
- Crystal-less wander and jitter attenuation/compensation
- Common master clock reference for and T1 (any frequency within 1.02 and 20 MHz)
- Support of automatic protection switching
- Selectable line codes (AMI/T1: B8ZS, AMI with ZCS)
- Loss of signal indication with programmable thresholds according to ITU-T G.775, and ANSI T1.403 (T1)
- Optional data stream muting upon LOS detection
- Programmable receive slicer threshold
- Clock generator for jitter free system/transmit clocks per channel
- Local loop and remote loop for diagnostic purposes
- Low power device, single power supply: 3.3 V with 5 V tolerant digital inputs

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Frame Aligner Features:

- Frame alignment/synthesis for 1544 kbit/s according to ITU-T G.704
- Programmable frame formats: T1 4-Frame Multiframe (F4,FT), 12-Frame Multiframe (F12, D3/4), Extended Superframe (F24, ESF), Remote Switch Mode (F72, SLC96)
- Selectable conditions for recover/loss of frame alignment
- Error checking via CRC6 procedures according to ITU-T G. 706 (T1)
- Insertion and extraction of alarm indication signals (AIS, remote/yellow alarm,…)
- Remote Alarm generation/checking according to ITU G.704 in ESF-format
- IDLE code insertion for selectable channels
- Single bit defect insertion
- Flexible system clock frequency for receiver and transmitter
- Supports programmable system data rates with independent receive/transmit shifts: E1: 2.048, 4.096, 8.192 and 16.384 Mbit/s (according to H.100 bus). T1: 2.048, 4.096, 8.192, 16.384 MBit/s and 1.544, 3.088, 6.176, 12.352 Mbit/s
- Elastic store for receive and transmit route clock wander and jitter compensation; controlled slip capability and slip indication
- Programmable elastic buffer size: 2 frames/1 frame/short buffer/bypass
- Provides different time slot mapping modes
- Supports fractional or T1 access
- Flexible transparent modes
- Programmable In-Band Loop Code detection and generation
- Channel loop back, line loop back or payload loop back capabilities (TR54016)
- Pseudo Random Bit Sequence (PRBS) generator and monitor (framed or unframed)
- Clear channel capabilities (T1)
- Loop-timed mode

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Signaling Controller Features

- HDLC controller bit stuffing, CRC check and generation, flag generation, flag and address recognition, handling of bit oriented functions
- Supports Signaling System #7 delimitation, alignment and error detection according to ITU-Q.703 processing of fill in signaling units, processing of errored signaling units
- CAS/CAS-BR controller with last look capability, enhanced CAS- register access and freeze signaling indication
- DL-channel protocol for ESF format according to ANSI T1.403 specification or according to AT&T TR54016 (T1)
- DL-bit access for F72 (SLC96) format (T1)
- Generates periodic performance report according to ANSI T1. 403
- Provides access to serial signaling data streams
- Multiframe synchronization and synthesis according to ITU-T G.732
- Alarm insertion and detection (AIS and LOS in time slot 16)
- Transparent Mode
- FIFO buffers (64 bytes deep) for efficient transfer of data packets
- Time slot assignment: Any combination of time slots selectable for data transfer independent of signaling mode (useful for fractional T1 applications)

General Features:

- Extended interrupt capabilities
- One-second timer (internal or external timing reference)

FALC General Description

The CPC395 utilizes two Infineon PEB2256 FALC framers with integrated LIUs as monitor ports. The FALCs are designated in the schematic as A-side Monitor Port and B-side Monitor Port. The FALC is a multi-function device designed to fulfill a multitude of interfacing requirements between a variety of analog E1/T1/J1 lines and digital PCM system highways of H.100 or H-MVIP type buses. However, on the CPC395 the function of the two FALCs will be limited to that of a T1 line interface only.

The Monitor FALCs are accessed by the MPC8260 for setup and control purposes through the buffered data bus. The buffered data bus supplies a buffered MPC8260 address and a bi-directional 16 bit data bus. The Monitor FALCs are set up as 8 bit devices on the bus. The chip selects for the FALCs are sub-decoded from the MPC8260 CS5 ($\overline{\text{CS_INTERFACE}}$) in PLD PSM499 PAL logic. The sub decoded signals come out as $\overline{\text{CS_FALC_A}}$ and $\overline{\text{CS_FALC_B}}$ chip selects. The following table shows the primary chip select address and the PSM499 sub-decode chip selects for the Monitor FALCs:

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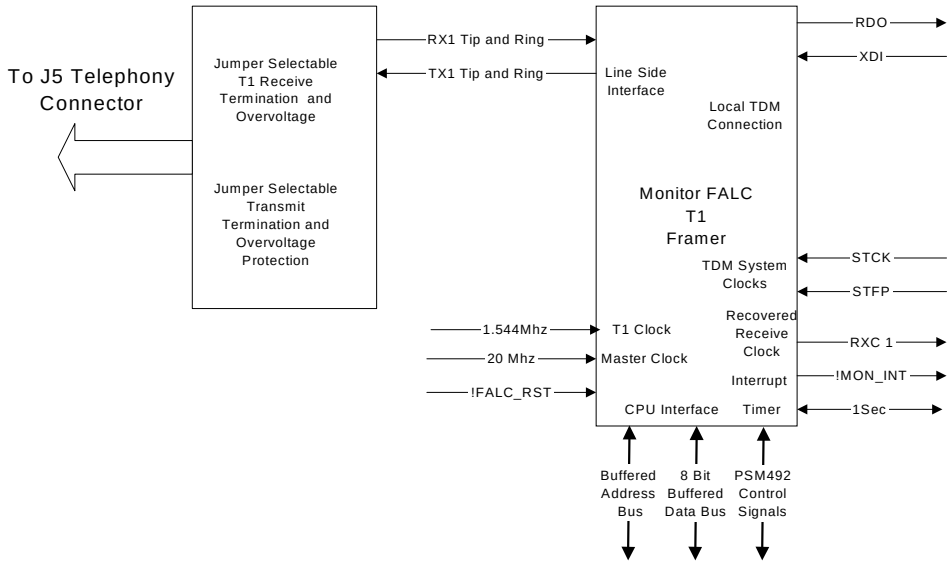


Figure 19. Monitor Framer Block Diagram

Table 53. CS5 Address Decode and Sub-decode

Address	Device
For Base Address, see Memory Map	$\overline{\text{CS_INTERFACE}}$
$\overline{\text{CS_INTERFACE}}$+08000h $\overline{\text{CS_INTERFACE}}$+080ffh	$\overline{\text{CS_FALC_A}}$
$\overline{\text{CS_INTERFACE}}$+08100h $\overline{\text{CS_INTERFACE}}$+081ffh	$\overline{\text{CS_FALC_B}}$

The cycle control portion of the buffered data bus for this device is supplied by the $\overline{\text{BUF_DS}}$ and BUF_RW# signals. The $\overline{\text{BUF_DS}}$ is supplied by PSM497 PLD logic and acts as the device data strobe in Motorola signaling mode. The PSM497 also supplies the BUF_RW# strobe, which is the read/write, enable. The cycle timing including the cycle termination is handled by the GCPM in the MPC8260. The settings for the $\overline{\text{CS5}}$ ($\overline{\text{CS_INTERFACE}}$) address space and the GPCM are as follows:

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MPC8260 Related FALC Settings

Table 54. CS5 Base Register Settings

Field	Recommended Setting	Description
PS	01	8-bit
DECC	00	Data Errors checking disabled
WP	0	Read and write accesses are allowed
MSEL	000	Machine Select GPCM-60x bus
EMEMC	0	Accesses are handled by the MSEL selected controller. No external memory controller allowed in this space.
ATOM	00	The address space is controlled by the memory controller bank and is not used for atomic operations
DR	0	No data pipelining is done.
V	1	This bank is valid

The Option Register Settings follow the form outlined for the GPCM Machine:

Table 55. CS5 Option Register Settings

Field	Recommended Setting	Description
BCTLD	0	$\overline{\text{BCTLx}}$ is asserted upon access to the current memory bank
CSNT	1	$\overline{\text{CS}}$/WE is negated a quarter of a clock early.
ACS	11	$\overline{\text{CS}}$ is output half a clock after the address lines.
SCY	5	Clock Wait states
SETA	0	$\overline{\text{PSDVAL}}$ is generated internally.
TRLX	1	Relaxed timing is generated by the GCPM for this memory region.
EHTR	00	Normal Idle Timing

Monitor FALC and LIU Register Map

The internal register map for the Monitor FALC is quite large and is not reproduced here. The map in its entirety can be found in the “Infineon Technologies ICs for Communications PEB2256 Data Sheet.” The detailed register definitions are also found in this document.

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Monitor Framer and LIU Physical Configuration

There are several functional sections in the device. Several of the sections have different pinout options for system connection to provide unique modes of operation. The following sections describe how the FALCs are configured for use in the CPC395 environment.

Line Interface Receive Configuration

The line receive interface option is set to analog input with a transformer and external line conditioning. The terminated and conditioned analog input signal is received on FALC inputs RL1 and RL2. This mode is selected in the LIM1 register by setting the DRS bit to 0 (LIM1.DRS=0).

Line Interface Transmit Configuration

The line transmit interface option is set to analog output with a transformer and external line conditioning. The terminated and conditioned analog output signal is presented to the trunk on FALC outputs XL1 and XL2 for the framer. This mode is selected in the LIM1 register by setting the DRS bit to 0 (LIM1.DRS=0). After RESET the transmit lines are in high impedance mode until FMR0.C1 is set to a 1.

Master Clock Configuration

The master clock input can be from 1.02 to 20 MHz at +/- 32ppm min. The CPC395 supplies the Master Clock input to the Monitor FALC with 20 MHz input clock at 32 ppm stability. The internal settings for the clock setup and control (see registers GCM1…6 in the datasheet) can be determined by the calculations given in the data sheet or by a PC calculator tool available on the Infineon Web site.

External DCO-R Clock SYNC Pin Configuration

The external DCO-R SYNC input pin is not supported and has no connection other then a pullup.

1 Second Timer Pin Configuration

The SEC pin can transmit or receive an input pulse on a periodic basis (typically 1 second) for use as an event timer within the part. This line is connected to both of the Monitor FALCs. Any one of the devices can be source of the signal. The default power up condition is set as a pulled up input. See register GPC1 in the datasheet for more information.

Line Receive Clock Output Pin Configuration

The Monitor FALCs have an output pin that will output the recovered line clock or the synchronized DCO-R signal. This pin is connected the reference clock mux. The output of the mux is used to drive the H.110 switch local reference input. See register PC5.CRP, CMR1.RS1, and GPC1.R1S1 in the data sheet for the appropriate configuration settings.

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Local TDM Receive Data Pin Configuration

The Monitor FALCs have a receive data out pin (RDO) that can be synchronized to a the TDM stream. The CPC395 connects the RDO pin to a local TDM input stream on the H.110 switch. The local streams is setup to use a 8.192 Mbits/sec transfer rate regardless of the line side operating rate. The received data stream is actually sourced from an internal elastic data store device which rate compensates between the trunk input rate and the local TDM stream. Refer to the data sheet for the proper control registers and their settings.

Local TDM Receive System Clock Pin Configuration

The framers have an elastic data store on the receive data output. The elastic store is used to compensate between the receiver trunk line rate and the local TDM data rate. This clock input pin (SCLKR) is used to supply the elastic data store with a clock that is synchronized to the local TDM. It has a fixed input frequency of 8.192 MHz. The SIC2.SSC2 bits are used to scale the clock input to the 1.544 Mbit/sec data rate. Refer to the data sheet for the proper control registers and their settings.

Local TDM Receive Frame Pulse Input Pin Configuration

The framers' receive data output is connected to the local TDM bus. The data output stream is typically sourced from the framer's elastic data store. In order to properly synchronize the operation of elastic data store to the local system timing a Frame Pulse is required. The H.110 switch sources the 8KHz frame pulse. The signal is input to the framer on the Receive Multifunction Port pin 1. This function is called the $\overline{\text{SYPR}}$ or Synchronous Pulse receive mode for the Receive Multifunction pin 1 on the port. Refer to the data sheet for the proper control registers and their settings.

At this time none of the other Receive Multifunction pins are used.

Local TDM Transmit Data Pin Configuration

The Monitor FALC framers have a transmit data input pin (XDI) that can be synchronized to a local TDM stream. The CPC395 uses the XDI pin to connect to a local TDM output stream on the H.110 switch. The local stream is setup to use a 8.192 Mbits/sec transfer rate regardless of the line side operating rate. The transmitted data stream is actually inputted to an internal elastic data store device which rate compensates between the trunk output rate and the local TDM stream. Refer to the data sheet for the proper control registers and their settings.

Local TDM Transmit System Clock Pin Configuration

The framers have an elastic data store on the transmit data input. The elastic store is used to compensate between the receiver trunk line rate and the local TDM data rate. This clock input pin is used to supply the elastic data store with a clock that is synchronized to the local TDM. It has a fixed input frequency of 8.192 MHz. The SIC2.SSC2 bits are used to scale the clock input to the 1.544 Mbit/sec data rate. Refer to the data sheet for the proper control registers and their settings.

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Local TDM Transmit Frame Pulse Input Pin Configuration

The Monitor FALC framers' transmit data input is connected to the local TDM bus. The data input stream is typically loaded into the framer's elastic data store. In order to properly synchronize the operation of elastic data store to the local system timing a Frame Pulse is required. The H.110 switch sources the 8KHz frame pulse. The signal is input to the framers on the Transmit Multifunction Port pin 1. This function is called the $\overline{\text{SYPX}}$ or Synchronous Pulse transmit mode for the Transmit Multifunction pin 1 on the port. Refer to the data sheet for the proper control registers and their settings.

Line Side T1 Transmit Clock Source

The framers can be setup to source their transmitter clock from a number of sources. Most of the clock sources are derived from internal sources on the chip. For the user's convenience, a 1.544 MHz clock for T1 operation is supplied on the Transmit Multifunction Port pin 3. Refer to the data sheet for the proper control registers and the settings.

Channel Associated Signaling

The framer has the ability to insert and extract the Channel Associated Signaling (CAS) for each DS0 in the receive and transmit data stream. The extracted CAS signaling from the framer is synchronized to the local TDM data rate. The CAS is sent onto the RPB signal pin and sent to the H.110 TDM switch at 8.192 Mbits/sec. This is similar to the scheme used for the received data. The timeslots on CAS line correspond to the CAS for the DS0 value that is being presented on the data line at the same time.

In a similar way the transmit CAS for the framer is received on the XPC input line and routed appropriately in the framer for insertion into the transmit data stream. The timeslots on CAS line correspond to the CAS for the DS0 value that is being presented on the data line at the same time.

FALC Interrupts

Each of the Monitor FALCs has an interrupt pin. Registers internal to the part define status and control of the pin. Refer to the data sheet for the proper control registers and their settings. The Monitor FALCs' interrupts are connected through the interrupt mask PLD PSM501directly to the MPC8260's. Monitor FALC A is on the $\overline{\text{IRQ5}}$ input and Monitor FALC B is on the $\overline{\text{IRQ6}}$ input. See "PSM501 Interrupt Mask and Control Registers" on page 120 for bit settings.

Transmitter Line Termination and Conditioning

The trunk side transmit line from the Monitor FALCs are terminated and conditioned by a series of passive components located both on the CPC395 itself and the CPC395 Line Interface Module (LIM). The CPC395 itself has series line termination resistors and over voltage protection diodes. The LIM has a line isolation transformer and a set of lightning protection modules for the set of transmit lines. There are no jumper settings or adjustments that need to be made to the line termination resistors because they are fixed for T1 operation only.

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Receiver Line Termination and Conditioning

The Trunk side receive lines from the Monitor FALC are terminated and conditioned by passive components located both on the CPC395 itself and the CPC395 Line Interface Module (LIM). The CPC395 itself has parallel line termination resistors and over voltage protection diodes. The LIM has a line isolation transformer and a set of lightning protection modules for the set of receive lines.

FALC Monitor Port Configuration and Setup

The two FALCs A and B each interface to their respective A and B side H.110 switches. The local side transmit and receive interface of the FALC Monitor is clocked by receive pin SCLKR and transmit pin SCLKX. The frequency of these working clocks is 8.192 MHz with a data rate of 8.192 Mbps. The receive and transmit interface is programmed in FALC register SIC1.SSC1/0, SIC2.SSC2 and SIC1.SSD1, FMR1.SSD0.

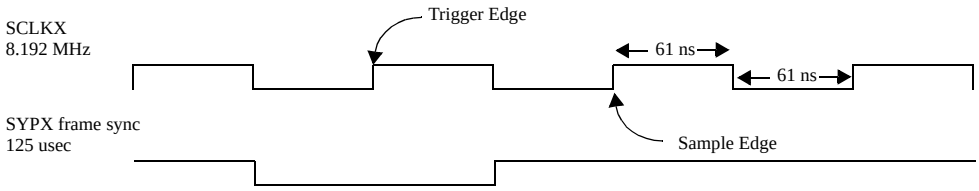
The local side frame sync signal on pin SYPR in combination with the assigned time slot offset in register RC0 and RC1 define the beginning of a frame on the receive interface. The local side frame sync signal on pin SYPX together with the assigned time slot offset in register XC0 and XC1 define the beginning of a frame on the transmit interface.

The follow diagrams represent trigger and sample clock edges that are used for the receive and transmit system interface timing on the FACL Monitor.

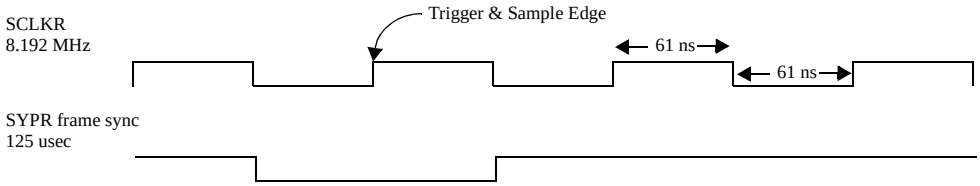
Each FALC produces one recovered and de-jittered clock on pin RCLK. These clocks are fed forward to PLD PSM499 the clock multiplexer where they can be used as possible sources for primary, secondary, or tertiary system level synchronization.

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PEB2256 Receive Signal Timing



PEB2256 Transmit Signal Timing



3.21 General Purpose Status and Control Registers

The General Purpose Status and Control Registers provide control over, and the status of, the unique functions of the CPC395 that are not included in the various peripheral devices on the board. All of the registers are 8-bit and are located on the buffered data bus.

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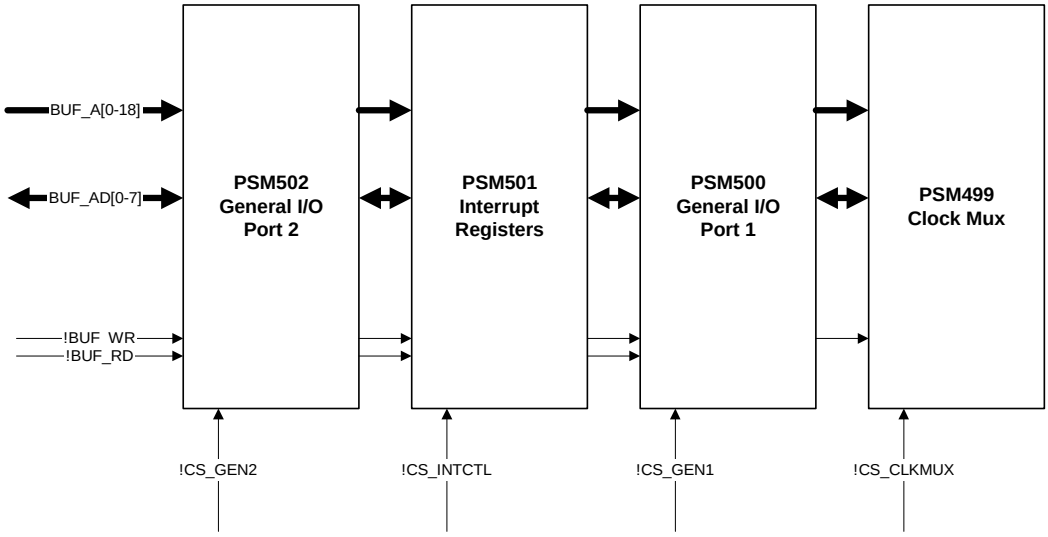


Figure 20. Status and Control Registers Block Diagram

Access to each of the register sets in the PSMXXX PAL logic begins with an address decode for each device. The primary decode comes from the MPC8260's CS4. Each device is further decoded by logic in the PSM498 PAL. It provides the following control lines to select each of the register sets.

Table 56. Address Subdecode for CS4 Devices

Address Range	Decoded Signal Name	Description
2000_0000- 2000_7FFF h	$\overline{\text{CS4}}$	MPC8260 $\overline{\text{CS4}}$ address decode range
2000_0000- 2000_00FF h	$\overline{\text{CS_GEN2}}$	Chip Select for General Purpose I/O device 2
2000_0100- 2000_01FF h	$\overline{\text{CS_INTCTL}}$	Chip Select for the Interrupt Control Register
2000_0200- 2000_02FF h	$\overline{\text{CS_GEN1}}$	Chip Select for General Purpose I/O device 1
2000_0300- 2000_03FF h	$\overline{\text{CS_CLKMUX}}$	Chip Select for Clock Multiplexer device

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The individual register decode within a register set is done by logic within each register set. The decode is based on the buffered 60x bus address provided by the PSM498 PAL anded with the appropriate chip select signal.

The necessary control and timing for each cycle comes initially from the 60x bus and the BR4 and OR4 GPCM registers. The following tables reflect the required settings for this space:

Table 57. CS4 Base Register Settings

Field	Recommended Setting
PS	01 8-bit
DECC	00 Data Errors checking disabled
WP	0 Read and write accesses are allowed
MSEL	000 Machine Select GPCM-60x bus
EMEMC	0 Accesses are handled by the MSEL selected controller. No external memory controller allowed in this space.
ATOM	00 The address space is controlled by the memory controller bank and is not used for atomic operations
DR	0 No data pipelining is done.
V	1 This bank is valid

The Option Register Settings follow the form outlined for the GPCM Machine:

Table 58. CS4 Option Register Settings

Field	Recommended Setting
BCTLD	0 $\overline{\text{BCTLx}}$ is asserted upon access to the current memory bank
CSNT	1 $\overline{\text{CS}}$/WE is negated a quarter of a clock early.
ACS	11 $\overline{\text{CS}}$ is output half a clock after the address lines.
SCY	6 Clock Wait states
SETA	0 $\overline{\text{PSDVAL}}$ is generated by the GCPM.
TRLX	1 Relaxed timing is generated by the GCPM for this memory region.
EHTR	00 Normal Idle Timing

Once the GCPM initiates the cycle on the 60x bus, the logic in the PSM497 pal then takes the 60x bus input and provides $\overline{\text{BUF_RD}}$ and $\overline{\text{BUF_WR}}$ read and write control signals. The PSM497 logic then configures the buffered bus to either drive write data or receive read data from the register PAL. The $\overline{\text{BUF_RD}}$ and $\overline{\text{BUF_WR}}$ strobes are supplied as required during the data phase of the cycle. Data is written into the registers on the

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rising edge of $\overline{\text{BUF_WR}}$. $\overline{\text{BUF_RD}}$ is essentially asserted during the entire data phase of the read cycle causing the data from the registers to be driven onto the data lines as long as the strobe is true. Read and Write cycles are completed by the GCPM's wait state timing. There is no cycle complete signal generated by the register logic.

The logic for the registers is contained the PSM499, PSM500, PSM501 and PSM5025 PAL devices.

The explicit address of each register and its associated function are contained in the following sections.

PSM502 General Purpose I/O Registers Device 2

The registers contained in the PSM 502 General Purpose I/O Register PAL, all begin at 2000_0000H in the $\overline{\text{CS4}}$ space. These registers include the following:

- H.110 Bus and Ethernet PHY Reset Control Register at address offset 00H
- General Control and Status Register 1 at address offset 01H
- General Purpose Latch Register at address offset 03H
- General Control and Status Register 2 at address offset 05H
- Board Id Register at address 0CH
- Board Revision and Build Option register at address offset 0DH

The following sections describe the register content.

H.110 Bus and Ethernet PHY Reset Control Register

The H.110 Bus and Ethernet PHY Reset Control Register, has bits that control the state of the reset output signals to the A and B side H.110 busses and the reset signals to the local Ethernet PHYs.

Table 59. H.110 Bus and Ethernet PHY Reset Control Register Bit Field

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	phy2rst	phy1rst	ctrst	0				
Reset Value	1	1	0	0				
R/W	R/W			READ ONLY				
Address	Base+00H							

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Table 60. H.110 Bus and Ethernet PHY Reset Control Register Bit Field Definitions

Bits	Name	Description
7	phy2rst	When this bit is set to a 1, the Ethernet PHY 2 chip is held in reset. The bit will always be set to 1 during a $\overline{\text{PQ_SRESET}}$. Setting the bit to a 0, will release the Ethernet PHY 2 chip from the reset state.
6	phy1rst	When this bit is set to a 1, the Ethernet PHY 1 chip is held in reset. The bit will always be set to 1 during a $\overline{\text{PQ_SRESET}}$. Setting the bit to a 0, will release the Ethernet PHY 1 chip from the reset state.
5	ctrst	This bit is active on the CT bus when the following conditions are met, the CT is set to be the system master (K2-1 to K2-2 in) and if the CPC395 board is the CT bus reset master, as selected by jumper K11-1 to K11-2 in. When this condition is set, if this bit is set to a 0, the A and B side CT buses are held in reset. The bit will always be set to 0 during a $\overline{\text{PQ_SRESET}}$. Setting the bit to a 1, will release the CT buses from the reset state.

General Control and Status Register 1

The General Control and Status Register 1 register contains status bit information and bit control for various functions on the CPC395 board. Some of the fields are read/write and some are read only depending on the function.

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Table 61. General Control and Status Register 1

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	factdflt	RSVD	smben	ctbmstr	ctrmstr	RSVD	flashwp	iamok
Reset Value	Current Value						1	0
R/W	READ ONLY						R/W	R/W
Address	Base+01H							

Table 62. General Control and Status Register 1 Bit Field Definitions

Bits	Name	Description
7	factdflt	This bit reflects that state of the K11 jumper. When the jumper is connected, the bit will indicate a 0. This indicates that user wants the PTI default software configuration loaded into all devices at bootup. When the K11 jumper is removed, the bit indicates a 1. This setting means that the customer settings will be loaded at bootup.
6	RSVD	Reserved
5	smben	This bit reflects that state of the K1 jumper. When the jumper is connected, the bit will indicate a 0. This indicates that the System Management Bus controller is installed and active. When the K1 jumper is removed, the bit indicates a 1. This setting means that the SMB is inactive.
4	ctbmstr	This bit reflects that state of the K2 jumper. When the jumper is connected, the bit will indicate a 0. This setting indicates to the CPC395 that the CT Bus is the master bus in the cardfile and that CT bus resets will produce hard resets to the CPC395. The CompactPCI reset signal will be ignored by the local reset control logic, however the CompactPCI reset will still reset the PCI 1 logic in the PowerSpan part. When K2 jumper is removed, the bit indicates a 1. This setting means that there is a CompactPCI bus in the cardfile and it has control of the reset action.
3	ctrmstr	This bit reflects the state of jumper K9. When the jumper is connected, the bit will indicate a 0. This setting indicates that the CPC395 is the Reset Master of both the A and B CT bus and controls both $\overline{\text{CT_RESET}}$ signals. The $\overline{\text{CT_RESET}}$ signals are controlled with the ctrst bit in the H.110 Bus and Ethernet PHY Reset Control Register. When the K11 jumper is removed, the bit is set to a 1 and the CPC395 cannot assert the $\overline{\text{CT_RESET}}$ signal on either CT Bus.
2	RSVD	Reserved

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Table 62. General Control and Status Register 1 Bit Field Definitions *(Continued)*

Bits	Name	Description
1	flashwp	When set to a 0, the flashwp bit will prevent a write cycle to the Application or Boot FLASH devices from being effected. The write cycle will terminate normally for the MPC8260, but the addressed FLASH device will not have its' write strobe toggled. When this bit is set to 1 write operations will be allowed to the FLASH device.
0	iamok	The iamok bit is used to signal the CompactPCI bus that the board is healthy. This bit is logically "anded" with the power good bit from the power controller IC to form the CompactPCI $\overline{\text{HEALTHY}}$ signal. The logic for this bit is contained in the PSM502 PAL. If the power good condition is true, with this bit set to a 0, the $\overline{\text{HEALTHY}}$ signal will be false and when set to a 1, the $\overline{\text{HEALTHY}}$ will indicate true on the CompactPCI Bus.

General Purpose Latch Register

The General Purpose Latch Register is an 8-bit Read/Write storage location for any general-purpose use. The location is volatile.

Table 63. General Purpose Latch Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	latch[7:0]							
Reset Value	0							
R/W	R/W							
Address	Base+03H							

Table 64. General Purpose Latch Register Bit Field Definitions

Bits	Name	Description
7:0	latch[7:0]	This register is a general purpose 8 bit storage latch. This location is volatile.

General Control and Status Register 2

The General Control and Status Register 2 register contains status bit information and bit control for various functions on the CPC395 board. Some of the fields are read/write and some are read only depending on the function.

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Table 65. General Control and Status Register 2

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	p1rst	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Reset Value	Current Value	0						
R/W	READ ONLY							
Address	Base+05H							

Table 66. General Control and Status Register 2 Bit Field Definitions

Bits	Name	Description
7	p1rst	This bit represents the current state of the CompactPCI reset signal. A 0 indicates that the CompactPCI bus is reset. A 1 indicates that the CompactPCI bus is activated.
6:0	RSVD	Reserved, 0

Board Id Register

The Board Id Register reflects the Board Id value.

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Table 67. Board Id Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	brdid[7:0]							
Reset Value	0							
R/W	READ ONLY							
Reset Value	Base+0CH							

Table 68. Board Id Register Bit Field Definitions

Bits	Name	Description
7:0	brdid[7:0]	Initial Value 0

Board Revision and Build Option Register

The Board Id Register reflects the Board Id value.

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Table 69. Board Revision and Build Option Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	brdopt[7:4]				brdrev[3:0]			
Reset Value	0							
R/W	READ ONLY							
Address	Base+0DH							

Table 70. Board Revision and Build Option Register Bit Field Definitions

Bits	Name	Description
7:4	brdopt[7:4]	CPC395 Board Build Option, value 0 for dual H.110, p/n CPC395 Board Build Option, value 1 for single H.110, p/n
3:0	brdrev[3:0]	CPC395 Board Revision Level, revision 10-01 CPC395 Board Revision Level, revision 20-10 CPC395 Board Revision Level, revision 30-11

PSM501 Interrupt Mask and Control Registers

The registers contained in the PSM501 Interrupt Mask and Control Register PAL, all begin at 2000_0100H in the $\overline{CS4}$ space. These registers include the following:

- Interrupt Control and Status Register A at address offset 100H
- Interrupt Control and Status Register B at address offset 101H
- Interrupt Mask Register A at address offset 102H
- Interrupt Mask Register B at address offset 103H
- Abort Jumper Control and Status Register at address offset 104H
- Abort Jumper Control Mask Register at address offset 105H

The following sections describe the register content.

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Interrupt Control and Status Register A

The Interrupt Control and Status Register A contains status information about the various interrupts associated with the A side telecommunications devices. The devices include the A side H.110 (MT90866) switch, the A side T3 (TEMUX) interface, the A side T3 Line Interface Unit (LIU) and the A side monitor FALC. The interrupt status bits will display the interrupt status of the respective device even if the interrupt has been masked in the interrupt mask register. See "Interrupt Mask Register A" on page 125. In addition to providing the status of the interrupt bits, the register will allow the MPC8260 to reset the bit in the register after the peripheral device has been serviced and its' interrupt cleared.

All of the devices in this register are reported to the MPC8260 on different interrupt levels. The A side H.110 CT Bus Clock A failure (ah110fla), A side H.110 CT Bus Clock B failure (ah110flb), the A side primary reference clock (apriref), and the A side secondary reference clock (asecref) interrupts, are all reported on the $\overline{\text{PQ_IRQ1}}$ interrupt input to the MPC8260. The A side T3 TEMUX (atmxin), the A side LIU loss of lock (aliulol) and the A side LIU loss of signal (aliulos) interrupts are all reported on the $\overline{\text{PQ_IRQ3}}$ interrupt input to the MPC8260. The A side Monitor FALC interrupt is reported on the $\overline{\text{PQ_IRQ5}}$ interrupt input to the MPC8260. The bit definitions and the read write functions are contained in the following tables.

Table 71. Interrupt Control and Status Register A Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	asecref	apriref	amonint	ah110flb	ah110fla	atmxint	aliulol	aliulos
Reset Value	0000							
R/W	R/W							
Address	Base+100H							

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Table 72. Interrupt Control and Status Register A Bit Field Definitions

Bits	Name	Description
7	asecref	When a 1 is read, this bit indicates that there is an interrupt from the A side H.110 switch's Secondary Reference Watchdog counter indicating that the secondary reference clock input has failed. This logic is located in PSM499. When this bit is read as a 0, there is no interrupt pending. Writing a 1 to this bit will clear the interrupt. Writing a 0 to this bit will have no impact on the bit.
6	apriref	When a 1 is read, this bit indicates that there is an interrupt from the A side H.110 switch's Primary Reference Watchdog counter indicating that the primary reference clock input has failed. When this bit is read as a 0, there is no interrupt pending. Writing a 1 to this bit will clear the interrupt. Writing a 0 to this bit will have no impact on the bit.
5	amonint	When a 1 is read, this bit indicates that there is an interrupt from the A side Monitor FALC indicating that it needs to be serviced. When read as a 0, there is no interrupt pending. Writing a 1 to this bit will clear the interrupt if the peripheral device has been serviced and its' interrupt cleared. Writing a 0 to this bit will have no impact on the bit.
4	ah110flb	When a 1 is read, this bit indicates that there is an interrupt from the A side H.110 switch indicating that the B CT Bus clock has failed. When read as a 0, there is no interrupt pending. Writing a 1 to this bit will clear the interrupt if the peripheral device has been serviced and its' interrupt cleared. Writing a 0 to this bit will have no impact on the bit.
3	ah110fla	When a 1 is read, this bit indicates that there is an interrupt from the A side H.110 switch indicating that the A CT Bus clock has failed. When read as a 0, there is no interrupt pending. Writing a 1 to this bit will clear the interrupt if the peripheral device has been serviced and its' interrupt cleared. Writing a 0 to this bit will have no impact on the bit.
2	atmxint	When a 1 is read, this bit indicates that there is an interrupt from the A side TEMUX indicating that it needs to be serviced. When read as a 0, there is no interrupt pending. Writing a 1 to this bit will clear the interrupt if the peripheral device has been serviced and its' interrupt cleared. Writing a 0 to this bit will have no impact on the bit
1	aliulol	When a 1 is read, this bit indicates that there is an interrupt from the A side T3 LIU indicating that the LIU has detected a Loss of Lock condition. When read as a 0, there is no interrupt pending. Writing a 1 to this bit will clear the interrupt if the peripheral device has been serviced and its' interrupt cleared. Writing a 0 to this bit will have no impact on the bit.
0	aliulos	When a 1 is read, this bit indicates that there is an interrupt from the A side T3 LIU indicating that the LIU has detected a Loss of signal condition. When read as a 0, there is no interrupt pending. Writing a 1 to this bit will clear the interrupt if the peripheral device has been serviced and its' interrupt cleared. Writing a 0 to this bit will have no impact on the bit.

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Interrupt Control and Status Register B

The Interrupt Control and Status Register B contains status information about the various interrupts associated with the B side telecommunications devices. The devices include the B side H.110 (MT90866) switch, the B side T3 (TEMUX) interface, the B side T3 Line Interface Unit (LIU) and the B side monitor FALC. The interrupt status bits will display the interrupt status of the respective device even if the interrupt has been masked in the interrupt mask register. See "Interrupt Mask Register B" on page 126. In addition to providing the status of the interrupt bits, the register will allow the MPC8260 to reset the bit in the register after the peripheral device has been serviced and its' interrupt cleared.

All of the devices in this register are reported to the MPC8260 on different interrupt levels. The B side H.110 CT Bus Clock A failure (bh110fla), B side H.110 CT Bus Clock B failure (bh110flb), the B side primary reference clock (bpriref), and the B side secondary reference clock (bsecref) interrupts, are all reported on the $\overline{\text{PQ_IRQ2}}$ interrupt input to the MPC8260. The B side T3 TEMUX (btmxin), the B side LIU loss of lock (bliulol) and the B side LIU loss of signal (bliulos) interrupts are all reported on the $\overline{\text{PQ_IRQ4}}$ interrupt input to the MPC8260. The B side Monitor FALC interrupt is reported on the $\overline{\text{PQ_IRQ6}}$ interrupt input to the MPC8260. The bit definitions and the read write functions are contained in the following tables.

Table 73. Interrupt Control and Status Register B Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	bsecref	bpriref	bmonint	bh110flb	bh110fla	btmxint	bliulol	bliulos
Reset Value	0000							
R/W	R/W							
Address	Base+101H							

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Table 74. Interrupt Control and Status Register B Bit Field Definitions

Bits	Name	Description
7	bsecref	When a 1 is read, this bit indicates that there is an interrupt from the B side H.110 switch's Secondary Reference Watchdog counter indicating that the secondary reference clock input has failed. This logic is located in PSM499. When this bit is read as a 0, there is no interrupt pending. Writing a 1 to this bit will clear the interrupt. Writing a 0 to this bit will have no impact on the bit.
6	bpriref	When a 1 is read, this bit indicates that there is an interrupt from the B side H.110 switch's Primary Reference Watchdog counter indicating that the primary reference clock input has failed. When this bit is read as a 0, there is no interrupt pending. Writing a 1 to this bit will clear the interrupt. Writing a 0 to this bit will have no impact on the bit.
5	bmonint	When a 1 is read, this bit indicates that there is an interrupt from the B side Monitor FALC indicating that it needs to be serviced. When read as a 0, there is no interrupt pending. Writing a 1 to this bit will clear the interrupt if the peripheral device has been serviced and its' interrupt cleared. Writing a 0 to this bit will have no impact on the bit.
4	bh110flb	When a 1 is read, this bit indicates that there is an interrupt from the B side H.110 switch indicating that the B CT Bus clock has failed. When read as a 0, there is no interrupt pending. Writing a 1 to this bit will clear the interrupt if the peripheral device has been serviced and its' interrupt cleared. Writing a 0 to this bit will have no impact on the bit.
3	bh110fla	When a 1 is read, this bit indicates that there is an interrupt from the B side H.110 switch indicating that the A CT Bus clock has failed. When read as a 0, there is no interrupt pending. Writing a 1 to this bit will clear the interrupt if the peripheral device has been serviced and its' interrupt cleared. Writing a 0 to this bit will have no impact on the bit.
2	btmxint	When a 1 is read, this bit indicates that there is an interrupt from the B side TEMUX indicating that it needs to be serviced. When read as a 0, there is no interrupt pending. Writing a 1 to this bit will clear the interrupt if the peripheral device has been serviced and its' interrupt cleared. Writing a 0 to this bit will have no impact on the bit
1	bliulol	When a 1 is read, this bit indicates that there is an interrupt from the B side T3 LIU indicating that the LIU has detected a Loss of Lock condition. When read as a 0, there is no interrupt pending. Writing a 1 to this bit will clear the interrupt if the peripheral device has been serviced and its' interrupt cleared. Writing a 0 to this bit will have no impact on the bit.
0	bliulos	When a 1 is read, this bit indicates that there is an interrupt from the B side T3 LIU indicating that the LIU has detected a Loss of signal condition. When read as a 0, there is no interrupt pending. Writing a 1 to this bit will clear the interrupt if the peripheral device has been serviced and its' interrupt cleared. Writing a 0 to this bit will have no impact on the bit.

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Interrupt Mask Register A

The Interrupt Mask Register A register, is used to mask interrupts contained in the Interrupt Control and Status Register A, so that they will not be forwarded to the MPC8260. The registers are read/write and can be set to mask and unmask the interrupts on an individual bit basis. The bit fields and their definitions are outlined in the following tables.

Table 75. Interrupt Mask Register A Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	masecref	maprieref	mamonint	mah110flb	mah110fla	matmxint	maliulol	maliulos
Reset Value	1	1	1	1	1	1	1	1
R/W	READ/WRITE							
Address	Base+102H							

Table 76. Interrupt Mask Register A Bit Field Definitions

Bits	Name	Description
7	masecref	When this bit is set to a one the A side H.110 secondary reference clock failure interrupt bit will be unmasked and allow the interrupt to be presented to the MPC8260. When this bit is set to 0 the interrupt is masked.
6	mapriref	When this bit is set to a one the A side H.110 primary reference clock failure interrupt bit will be unmasked and allow the interrupt to be presented to the MPC8260. When this bit is set to 0 the interrupt is masked.
5	mamonint	When this bit is set to a one the A side Monitor FALC interrupt bit will be unmasked and allow the interrupt to be presented to the MPC8260. When this bit is set to 0 the interrupt is masked.
4	mah110flb	When this bit is set to a one the A side H.110 CT Bus B clock failure interrupt bit will be unmasked and allow the interrupt to be presented to the MPC8260. When this bit is set to 0 the interrupt is masked.
3	mah110fla	When this bit is set to a one the A side H.110 CT Bus A clock failure interrupt bit will be unmasked and allow the interrupt to be presented to the MPC8260. When this bit is set to 0 the interrupt is masked.
2	matmxint	When this bit is set to a one the A side T3 TEMUX interrupt bit will be unmasked and allow the interrupt to be presented to the MPC8260. When this bit is set to 0 the interrupt is masked.

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Table 76. Interrupt Mask Register A Bit Field Definitions *(Continued)*

Bits	Name	Description
1	maliulol	When this bit is set to a one the A side T3 LIU Loss of Lock interrupt bit will be unmasked and allow the interrupt to be presented to the MPC8260. When this bit is set to 0 the interrupt is masked.
0	maliulos	When this bit is set to a one the A side T3 LIU Loss of Signal interrupt bit will be unmasked and allow the interrupt to be presented to the MPC8260. When this bit is set to 0 the interrupt is masked.

Interrupt Mask Register B

The Interrupt Mask Register B register, is used to mask interrupts contained in the Interrupt Control and Status Register B, so that they will not be forwarded to the MPC8260. The registers are read/write and can be set to mask and unmask the interrupts on an individual bit basis. The bit fields and their definitions are outlined in the following tables.

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Table 77. Interrupt Mask Register B Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	mbsecref	mbpriref	mbmonint	mbh110flb	mbh110fla	mbtmxint	mbliulol	mbliulos
Reset Value	1	1	1	1	1	1	1	1
R/W	READ/WRITE							
Address	Base+103H							

Table 78. Interrupt Mask Register B Bit Field Definitions

Bits	Name	Description
7	mbsecref	When this bit is set to a one the B side H.110 secondary reference clock failure interrupt bit will be unmasked and allow the interrupt to be presented to the MPC8260. When this bit is set to 0 the interrupt is masked.
6	mbpriref	When this bit is set to a one the B side H.110 primary reference clock failure interrupt bit will be unmasked and allow the interrupt to be presented to the MPC8260. When this bit is set to 0 the interrupt is masked.
5	mbmonint	When this bit is set to a one the B side Monitor FALC interrupt bit will be unmasked and allow the interrupt to be presented to the MPC8260. When this bit is set to 0 the interrupt is masked.
4	Mbh110flb	When this bit is set to a one the B side H.110 CT Bus B clock failure interrupt bit will be unmasked and allow the interrupt to be presented to the MPC8260. When this bit is set to 0 the interrupt is masked.
3	mbh110fla	When this bit is set to a one the B side H.110 CT Bus A clock failure interrupt bit will be unmasked and allow the interrupt to be presented to the MPC8260. When this bit is set to 0 the interrupt is masked.
2	mbtmxint	When this bit is set to a one the B side T3 TEMUX interrupt bit will be unmasked and allow the interrupt to be presented to the MPC8260. When this bit is set to 0 the interrupt is masked.
1	mbliulol	When this bit is set to a one the B side T3 LIU Loss of Lock interrupt bit will be unmasked and allow the interrupt to be presented to the MPC8260. When this bit is set to 0 the interrupt is masked.
0	mbliulos	When this bit is set to a one the B side T3 LIU Loss of Signal interrupt bit will be unmasked and allow the interrupt to be presented to the MPC8260. When this bit is set to 0 the interrupt is masked.

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Abort Jumper Control and Status Register

The Abort Jumper Control and Status Register contains status information about the state of the Abort Jumper. The abort jumper is used to create a Non-Maskable interrupt to the MPC8260. This action is allowed if the Abort Jumper Interrupt is unmasked. See "Abort Jumper Control Mask Register" on page 128. The bit definitions and the read write functions are contained in the following tables.

Table 79. Abort Jumper Control and Status Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	RESERVED							abt
Reset Value	0000							
R/W	R/W							
Address	Base+104H							

Table 80. Abort Jumper Control and Status Register Bit Field Definitions

Bits	Name	Description
7:1	RSVD	RESERVED.
0	abt	When a 1 is read, this bit indicates that there is an interrupt from the Abort Jumper. When read as a 0, there is no interrupt pending. Writing a 1 to this bit will clear the interrupt if the peripheral device has been serviced and its' interrupt cleared. Writing a 0 to this bit will have no impact on the bit.

Abort Jumper Control Mask Register

The Abort Jumper Control Mask Register is used to mask interrupts contained in the Abort Jumper Control and Status Register, so that they will not be forwarded to the MPC8260. The register is read/write and can be set to mask and unmask the interrupt on an individual bit basis. The bit fields and their definitions are outlined in the following tables.

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Table 81. Abort Jumper Control Mask Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	RESERVED							mabt
Reset Value	0							1
R/W	READ/WRITE							
Address	Base+105H							

Table 82. Abort Jumper Control Mask Register Bit Field Definitions

Bits	Name	Description
7:1	RSVD	RESERVED
0	mabt	When this bit is set to a one the Abort Jumper interrupt bit will be unmasked and allow the interrupt to be presented to the MPC8260. When this bit is set to 0 the interrupt is masked.

PSM500 General Purpose I/O Registers Device 1

The registers contained in the PSM500 General Purpose I/O Registers Device 1 PAL, all begin at 2000_0200H in the $\overline{CS4}$ space. These registers include the following:

- Telecom Control Register 1 at address offset 200H
- Telecom Control Register 2 at address offset 201H
- Telecom Control Register 3 at address offset 202H
- Telecom Control Register 4 at address offset 203H
- Telecom Control Register 5 and Board LED Status Register at address offset 204H
- Telecom Control Register 6 at address offset 205H
- Port Status LED Control Register at address offset 206H
- Geographic and Shelf Address Register at address offset 207H
- General Purpose Switch and Shelf Address Register at address offset 208H
- Telecom Control Register 7 at address offset 209H

The following sections describe the register content.

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Telecom Control Register 1

The Telecom Control Register 1 has bits that setup and control several different aspects of the Telecommunications portion of the CPC395. The definition of the bit fields and their usage are found in the following tables.

Table 83. Telecom Control Register 1 Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	adecodis	atxlev	amonrst	atmuxrst	b2tdmctl	en37mh	en44mh	b1tdmctl
Reset Value	0000H							
R/W	Read/Write							
Address	Base+200H							

Table 84. Telecom Control Register 1 Bit Field Definitions

Bits	Name	Description
7	adecodis	When set to a 1, this bit disables the A side T3 Line Interface Unit's (LIU) B3ZS Decoder. When set to a 0, the A Side T3 LIU's B3ZS Decoder is enabled. **NOTE: The LIU's B3ZS Encoder or Decoder should always be disabled because the T3 TEMUX B3ZS integral Encoder/Decoder is always enabled**.
6	atxlev	This bit controls the Line Build-out function on the A side LIU Set this bit to a 1, if the cable length is greater than 225 feet. Set this bit to a 0, if the cable length is less than 225 feet.
5	amonrst	This bit controls the reset line for the A side Monitor FALC. When this bit is set to a 1, the Monitor FALC is not reset. When this bit is set to a 0, the Monitor FALC is held in reset.
4	atmuxrst	This bit controls the reset line to the A side TEMUX device. When this bit is set to a 1, the TEMUX is not reset. When this bit is set to a 0, the TEMUX is held in reset.
3	b2tdmctl	This bit controls the MPC8260's external B2 TDM Input Multiplexer. The multiplexer allows the B2 TDM I/O to be connected to either the A or B side MT90866 TDM switch's STO16 output. When this bit is set to a 1, the B side H.110 STO16 is connected to the B2 TDM input. When this bit is set to a 0, the A side H.110 STO16 is connected to the B2 TDM input.

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Table 84. Telecom Control Register 1 Bit Field Definitions *(Continued)*

Bits	Name	Description
2	en37mh	This bit controls the enabling of the 37.056 MHz oscillator to both of the T3 TEMUX chips. When this bit is set to a 1, the clock is enabled. When this bit is set to a 0, the clock is disabled.
1	en44mh	This bit controls the enabling of the 44.736 MHz oscillator to both of the T3 TEMUX and LIU chips. When this bit is set to a 1, the clock is enabled. When this bit is set to a 0, the clock is disabled.
0	b1tdmctl	This bit controls the MPC8260's external B1 TDM Input Multiplexer. The multiplexer allows the B1 TDM I/O to be connected to either the A or B side MT90866 TDM switch's STO17 output. When this bit is set to a 1, the B side H.110 STO17 is connected to the B1 TDM input. When this bit is set to a 0, the A side H.110 STO17 is connected to the B1TDM input.

Telecom Control Register 2

The Telecom Control Register 2 has bits that setup and control several different aspects of the Telecommunications portion of the CPC395. The definition of the bit fields and their usage are found in the following tables.

Table 85. Telecom Control Register 2 Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	atxoff	almuten	arlb	allb	altherl	areqdis	ataos	aencodis
Reset Value	0000H							
R/W	Read/Write							
Address	Base+201H							

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Table 86. Telecom Control Register 2 Bit Field Definitions

Bits	Name	Description
7	atxoff	This bit controls the A side LIU transmitter. When this bit is set to a 1, the A side T3 LIU is configured to disable its' transmitter. When this bit is set to a 0, the A side T3 LIU is configured to enable its' transmitter.
6	almuten	This bit controls the mute output on Loss Of Signal (LOS) function on the A side LIU. When this bit is set to a 1, the T3 LIU will pull the RPOS and RNEG (receive data) lines to ground, whenever it declares a LOS condition, thereby muting the data being sent to the TEMUX device. When this bit is set to a 0, the T3 LIU will not mute the receive data lines to the TEMUX when it detects LOS.
5	arlb	This bit, along with the allb bit, controls the A Side Remote Loopback setup for the A side LIU. When this bit is set to a 1, with the allb bit set to a 0, the A side T3 LIU will operate in the Remote Loopback Mode. When this bit is set to a 1, with the allb bit set to a 1, the A side T3 LIU will operate in the Digital Local Loopback Mode. When this bit is set to a 0, and the allb bit is set to a 0, the A side T3 LIU will operate in the Normal Mode.
4	allb	This bit, along with the arlb bit, controls the A Side Local Loopback setup for the A side LIU. When this bit is set to a 1, with the arlb bit set to a 0, the A side T3 LIU will operate in the Analog Local Loopback Mode. When this bit is set to a 1, with the arlb bit set to a 1, the A side T3 LIU will operate in the Digital Local Loopback Mode. When this bit is set to a 0, and the arlb bit is set to a 0, the A side T3 LIU will operate in the Normal Mode.
3	altherl	This bit sets the input signal Loss of Signal Threshold for the receiver circuit. The bit directly controls the A_LOSTHER signal. The exact threshold levels set depend on the areqdis (which controls the A_REQDIS signal) setting. See , for the proper settings.
2	areqdis	This bit controls the state of the Receiver Equalizer on the A side LIU. When this bit is set to a 1, the A side LIU equalizer is disabled. When this bit is set to a 0, The A side LIU equalizer is enabled. NOTE: For normal operation it is recommended that the receiver equalizer always be enabled.
1	ataos	This bit controls the A side LIU's ability to transmit an all "1s" signal (AMI transmission) on the line. When the bit is set to a 1, the A side LIU will transmit a continuous AMI signal. When this bit is set to a 0, the A side LIU will be in the normal transmission mode.
0	aencodis	When set to a 1, this bit disables the A side T3 Line Interface Unit's (LIU) B3ZS Encoder. When set to a 0, the A Side T3 LIU's B3ZS Encoder is enabled. **NOTE: The LIU's B3ZS Encoder or Decoder should always be disabled because the T3 TEMUX B3ZS integral Encoder/Decoder is always enabled**.

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Telecom Control Register 3

The Telecom Control Register 3 has bits that setup and control several different aspects of the Telecommunications portion of the CPC395. The definition of the bit fields and their usage are found in the following tables.

Table 87. Telecom Control Register 3 Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	bdecodis	btxlev	bmonrst	btmuxrst	bsecrci	bprirci	asecrci	aprirci
Reset Value	0000H							
R/W	Read/Write							
Address	Base+202H							

Table 88. Telecom Control Register 3 Bit Field Definitions

Bits	Name	Description
7	bdecodis	When set to a 1, this bit disables the B side T3 Line Interface Unit's (LIU) B3ZS Decoder. When set to a 0, the B Side T3 LIU's B3ZS Decoder is enabled. **NOTE: The LIU's B3ZS Encoder or Decoder should always be disabled because the T3 TEMUX B3ZS integral Encoder/Decoder is always enabled**.
6	btxlev	This bit controls the Line Build-out function on the B side LIU Set this bit to a 1, if the cable length is greater than 225 feet. Set this bit to a 0, if the cable length is less than 225 feet.
5	bmonrst	This bit controls the reset line for the B side Monitor FALC. When this bit is set to a 1, the Monitor FALC is not reset. When this bit is set to a 0, the Monitor FALC is held in reset.
4	btmuxrst	This bit controls the reset line to the B side TEMUX device. When this bit is set to a 1, the TEMUX is not reset. When this bit is set to a 0, the TEMUX is held in reset.
3	bsecrci	This bit controls and clears the B side, H.110 Loss of Secondary Reference Clock input interrupt. The status of this signal is reflected by the mbsecref bit. See section , When this bit is set to a 1, the interrupt is enabled. When this bit is set to a 0, the interrupt is cleared.

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Table 88. Telecom Control Register 3 Bit Field Definitions *(Continued)*

Bits	Name	Description
2	bprirci	This bit controls and clears the B side, H.110 Loss of Secondary Reference Clock input interrupt. The status of this signal is reflected by the mbpriref bit. See section , When this bit is set to a 1, the interrupt is enabled. When this bit is set to a 0, the interrupt is cleared.
1	asecrci	This bit controls and clears the A side, H.110 Loss of Secondary Reference Clock input interrupt. The status of this signal is reflected by the masecref bit. See section , . When this bit is set to a 1, the interrupt is enabled. When this bit is set to a 0, the interrupt is cleared.
0	aprirci	This bit controls and clears the A side, H.110 Loss of Secondary Reference Clock input interrupt. The status of this signal is reflected by the mapriref bit. See section , . When this bit is set to a 1, the interrupt is enabled. When this bit is set to a 0, the interrupt is cleared.

Telecom Control Register 4

The Telecom Control Register 4 has bits that setup and control several different aspects of the Telecommunications portion of the CPC395. The definition of the bit fields and their usage are found in the following tables.

Table 89. Telecom Control Register 4 Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	btxoff	blmuten	brlb	bllb	bltherl	breqdis	btaos	bencodis
Reset Value	0000H							
R/W	Read/Write							
Address	Base+203H							

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Table 90. Telecom Control Register 4 Bit Field Definitions

Bits	Name	Description
7	btxoff	This bit controls the B side LIU transmitter. When this bit is set to a 1, the B side T3 LIU is configured to disable its' transmitter. When this bit is set to a 0, the B side T3 LIU is configured to enable its' transmitter.
6	blmuten	This bit controls the mute output on Loss Of Signal (LOS) function on the B side LIU. When this bit is set to a 1, the T3 LIU will pull the RPOS and RNEG (receive data) lines to ground, whenever it declares a LOS condition, thereby muting the data being sent to the TEMUX device. When this bit is set to a 0, the T3 LIU will not mute the receive data lines to the TEMUX when it detects LOS.
5	brlb	This bit, along with the bllb bit, controls the B Side Remote Loopback setup for the B side LIU. When this bit is set to a 1, with the bllb bit set to a 0, the B side T3 LIU will operate in the Remote Loopback Mode. When this bit is set to a 1, with the bllb bit set to a 1, the B side T3 LIU will operate in the Digital Local Loopback Mode. When this bit is set to a 0, and the bllb bit is set to a 0, the B side T3 LIU will operate in the Normal Mode.
4	bllb	This bit, along with the brlb bit, controls the B Side Local Loopback setup for the B side LIU. When this bit is set to a 1, with the brlb bit set to a 0, the B side T3 LIU will operate in the Analog Local Loopback Mode. When this bit is set to a 1, with the brlb bit set to a 1, the B side T3 LIU will operate in the Digital Local Loopback Mode. When this bit is set to a 0, and the brlb bit is set to a 0, the B side T3 LIU will operate in the Normal Mode.
3	bltherl	This bit sets the input signal Loss of Signal Threshold for the receiver circuit. The bit directly controls the B_LOSTHER signal. The exact threshold levels set depend on the breqdis (which controls the B_REQDIS signal) setting. See , for the proper settings.
2	breqdis	This bit controls the state of the Receiver Equalizer on the B side LIU. When this bit is set to a 1, the B side LIU equalizer is disabled. When this bit is set to a 0, The B side LIU equalizer is enabled. NOTE: For normal operation it is recommended that the receiver equalizer always be enabled.
1	btaos	This bit controls the B side LIU's ability to transmit an all "1s" signal (AMI transmission) on the line. When the bit is set to a 1, the B side LIU will transmit a continuous AMI signal. When this bit is set to a 0, the B side LIU will be in the normal transmission mode.
0	bencodis	When set to a 1, this bit disables the B side T3 Line Interface Unit's (LIU) B3ZS Encoder. When set to a 0, the B Side T3 LIU's B3ZS Encoder is enabled. **NOTE: The LIU's B3ZS Encoder or Decoder should always be disabled because the T3 TEMUX B3ZS integral Encoder/Decoder is always enabled**.

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Telecom Control Register 5 and Board LED Status Register

The Telecom Control Register 4 has bits that setup and control several different aspects of the Telecommunications portion of the CPC395. It also controls the two general-purpose status LEDs located on the front panel in LED array D1. The definition of the bit fields and their usage are found in the following tables.

Table 91. Telecom Control Register 5 and Board LED Status Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	RESERVED			esreset	stat2gr	stat2rg	stat1gy	stat1yg
Reset Value	0000H							
R/W	Read/Write							
Address	Base+204H							

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Table 92. Telecom Control Register 5 and Board LED Status Register Bit Field Definitions

Bits	Name	Description
7:5	RSVD	RESERVED.
4	esreset	Elastic Store Reset: This bit resets the A side H.110 switch to B side H.110 switch elastic store interface. Set this bit to a 1, to allow normal operation of the Elastic Store. Set this bit to a 0, to assert reset to the Elastic Store.
3:2	stat2gr stat2rg	**General Purpose Status LED S2 control bits:** **stat2gr** **stat2rg** **LED S2** 1 1 off 0 1 red 1 0 green 0 0 off
1:0	stat1gy stat1yg	**General Purpose Status LED S1 control bits:** **stat2gy** **stat2yg** **LED S2** 1 1 off 0 1 yellow 1 0 green 0 0 off

Telecom Control Register 6

The Telecom Control Register 6 has bits that setup and control several different aspects of the Telecommunications portion of the CPC395. The definition of the bit fields and their usage are found in the following tables.

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Table 93. Telecom Control Register 6 Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	bh110rst	bh1110ode	bcref1oe	bcref2oe	ah110rst	ah110ode	acref1oe	acref2oe
Reset Value	00H							
R/W	READ/WRITE							
Address	Base+205H							

Table 94. Telecom Control Register 6 Bit Field Definitions

Bits	Name	Description
7	bh110rst	B Side H.110 Switch Reset: This bit puts the B side H.110 switch in its reset state. It clears the device's internal counters and registers. Set this bit to a 1, to allow normal operation of the H.110 switch. Set this bit to a 0, to assert reset of the H.110 switch. To ensure proper reset action on the H.110 switch, the reset bit must be 0 for longer than 1ms. Upon the release of Reset, the device registers must not be accessed for a period of 1 ms.
6	bh1110ode	B Side Output Drive Enable (5V Tolerant Input): This bit is the output enable control for the H.110 switch. B_H110_ODE controls STo0 to STo20 local serial outputs and STio0 to STio31 H.110 bus serial bi-directional outputs. It also the controls signals for the C1M5o, ST_CKo and ST_FPo outputs clocks. Set this bit to a 1, to enable H.110 output and bi-directional drivers. Set this bit to a 0, to disable H.110 output and bi-directional drivers.
5	bcref1oe	B Side CT_NETREF_1 Buffer Enable: The CT bus Network Timing References is controlled in the H.110 switch. However an external buffer is required between the H.110 switch and bus. Set this bit to a 1, to enable the external buffer and allow B_CT_NETREF_1 to be driven on the B side H.110 bus. Set this bit to a 0, to disable the external buffer and prevent B_CT_NETREF_1 from being driven on the B side H.110 bus. Upon the release of Reset, the device registers must not be accessed for a period of 1 ms.

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Table 94. Telecom Control Register 6 Bit Field Definitions *(Continued)*

Bits	Name	Description
4	bcref2oe	B Side CT_NETREF_2 Buffer Enable: The CT bus Network Timing References is controlled in the H.110 switch. However an external buffer is required between the H.110 switch and bus. Set this bit to a 1, to enable the external buffer and allow B_CT_NETREF_2 to be driven on the B side H.110 bus. Set this bit to a 0, to disable the external buffer and prevent B_CT_NETREF_2 from being driven on the B side H.110 bus.
3	ah110rst	A Side H.110 Switch Reset: This bit puts the A side H.110 switch in its reset state. It clears the device's internal counters and registers. Set this bit to a 1, to allow normal operation of the H.110 switch. Set this bit to a 0, to assert reset of the H.110 switch. To ensure proper reset action on the H.110 switch, the reset bit must be 0 for longer than 1ms.
2	ah110ode	A Side Output Drive Enable (5V Tolerant Input): This bit is the output enable control for the H.110 switch. A_H110_ODE controls STo0 to STo20 local serial outputs and STio0 to STio31 H.110 bus serial bi-directional outputs. It also the controls signals for the C1M5o, ST_CKo and ST_FPo outputs clocks. Set this bit to a 1, to enable H.110 output and bi-directional drivers. Set this bit to a 0, to disable H.110 output and bi-directional drivers.
1	acref1oe	A Side CT_NETREF_1 Buffer Enable: The CT bus Network Timing References is controlled in the H.110 switch. However an external buffer is required between the H.110 switch and bus. Set this bit to a 1, to enable the external buffer and allow A_CT_NETREF_1 to be driven on the A side H.110 bus. Set this bit to a 0, to disable the external buffer and prevent A_CT_NETREF_1 from being driven on the A side H.110 bus.
0	acref2oe	A Side CT_NETREF_2 Buffer Enable: The CT bus Network Timing References is controlled in the H.110 switch. However an external buffer is required between the H.110 switch and bus. Set this bit to a 1, to enable the external buffer and allow A_CT_NETREF_2 to be driven on the A side H.110 bus. Set this bit to a 0, to disable the external buffer and prevent A_CT_NETREF_2 from being driven on the A side H.110 bus.

Port Status LED Control Register

The Port Status LED Control Register controls the illumination of the A and B port status LEDs on the front panel. The bit fields and their usage are found in the following tables.

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Table 95. Port Status LED Control Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	bt3gr	bt3rg	bt3gy	bt3yg	at3gr	at3rg	at3gy	at3yg
Reset Value	0000H							
R/W	Read/Write							
Address	Base+206H							

Table 96. Port Status LED Control Register Bit Field Definitions

Bits	Name	Description
7:6	bt3gr bt3rg	**B Side T3 Port Status LED, Red/Green LED:** **bt3gr bt3rg LED BRG** 1 1 off 0 1 red 1 0 green 0 0 off
5:4	bt3gy bt3yg	**B Side T3 Port Status LED, Yellow/Green LED:** **bt3gy bt3yg LED BYG** 1 1 off 0 1 yellow 1 0 green 0 0 off
3:2	at3gr at3rg	**A Side T3 Port Status LED, Red/Green LED:** **at3gr at3rg LED ARG** 1 1 off 0 1 red 1 0 green 0 0 off
1:0	at3gy at3yg	**A Side T3 Port Status LED, Yellow/Green LED:** **at3gy at3yg LED AYG** 1 1 off 0 1 yellow 1 0 green 0 0 off

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Geographic and Shelf Address Register

The Geographic and shelf Address Register contains the 5-bit value of the CompactPCI backplane slot identifier for the slot that the CPC395 is currently plugged into. These bits are read from the backplane through the J2 CompactPCI connector. If the CompactPCI bus is not available and only the CT bus is present in the system, they are also available and read from the J4 CT bus connector. The two connections are wire or'ed together on the board. The shelf enumeration address comes from the J4 connector as well and identifies the shelf number that the board resides in. Note that only the lower order bits of the shelf address are contained in this register. The remaining bits are located in the "General Purpose Switch and Shelf Address Register" on page 141. The bit fields are defined in the following tables:

Table 97. CompactPCI Geographic and Shelf Address Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	sga[2-0]			ga[4-0]				
Reset Value	Current Value							
R/W	READ ONLY							
Address	Base+207H							

Table 98. CompactPCI Geographic and Shelf Address Register Bit Field Definitions

Bits	Name	Description
7:5	sga[2-0]	CompactPCI Shelf Enumeration Address
4:0	ga[4-0]	CompactPCI Geographic Address

General Purpose Switch and Shelf Address Register

The General Purpose Switch and Shelf Address Register is an 8 bit read only register. It contains the bit values of the 4 bit general purpose switch (SW1) and the high order bits of the Shelf Enumeration Address. See "Geographic and Shelf Address Register" on page 141 for the remaining Shelf Enumeration Address bits.

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Table 99. General Purpose Switch and Shelf Address Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	RESERVED		sga[4-3]		gpsw[4:1]			
Reset Value	0		Current Value		Current Value			
R/W	READ ONLY							
Address	Base+208H							

Table 100. General Purpose Switch and Shelf Address Register Bit Field Definitions

Bits	Name	Description
7:6	RSVD	RESERVED
5:4	sga[4-3]	CompactPCI Shelf Enumeration Address
3:0	gpsw[4:1]	Each bit of this field represents the position of one of the four switches of SW1. Bit 3 represents switch 4, bit 2 switch 3, bit 1 switch 2 and bit 0 switch 1. A 1 represents an open switch condition. A 0 represents a closed switch position.

Telecom Control Register 7

The Telecom Control Register 7 has bits that setup and control several different aspects of the Telecommunications portion of the CPC395. The definition of the bit fields and their usage are found in the following tables.

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Table 101. Telecom Control Register 7 Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	bcctlb	bcctla	acctlb	acctla	RESERVED			
Reset Value	1	1	1	1	0H			
R/W	Read/Write							
Address	Base+209H							

Table 102. Telecom Control Register 7 Bit Field Definitions

Bits	Name	Description
7	bcctlb	B Side Clock Control B This signal is used to enable the CT bus clock and frame sync bus drivers. These bus drivers allow clocks to be driven out when the H.110 switch is used as master of the bus. When this bit is set to a 1, the B side H.110 CT_Frame_B, and CT_C8_B output driver is disabled. When this bit is set to a 0, the B side H.110 CT_Frame_B, and CT_C8_B output driver is enabled. Power up default condition disabled.
6	bcctla	**B Side Clock Control A** This signal is used to enable the CT bus clock and frame sync bus drivers. These bus drivers allow clocks to be driven out when the H.110 switch is used as master of the bus. When this bit is set to a 1, the B side H.110 CT_Frame_A, and CT_C8_A output driver is disabled. When this bit is set to a 0, the B side H.110 CT_Frame_A, and CT_C8_A output driver is enabled. Power up default condition disabled.
5	acctlb	A Side Clock Control B This signal is used to enable the CT bus clock and frame sync bus drivers. These bus drivers allow clocks to be driven out when the H.110 switch is used as master of the bus. When this bit is set to a 1, the A side H.110 CT_Frame_B, and CT_C8_B output driver is disabled. When this bit is set to a 0, the A side H.110 CT_Frame_B, and CT_C8_B output driver is enabled. Power up default condition disabled.

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Table 102. Telecom Control Register 7 Bit Field Definitions *(Continued)*

Bits	Name	Description
4	acctla	**A Side Clock Control A** This signal is used to enable the CT bus clock and frame sync bus drivers. These bus drivers allow clocks to be driven out when the H.110 switch is used as master of the bus. When this bit is set to a 1, the A side H.110 CT_Frame_A, and CT_C8_A output driver is disabled. When this bit is set to a 0, the A side H.110 CT_Frame_A, and CT_C8_A output driver is enabled. Power up default condition disabled.
3:0	RSVD	RESERVED

PSM499 Clock Multiplexer Registers

The registers contained in the PSM499 Clock Multiplexer Registers PAL, all begin at 2000_0300H in the $\overline{CS4}$ space. These registers include the following:

- A Side Primary Clock Select Register at address offset 300H
- A Side Secondary Clock Select Register at address offset 301H
- B Side Primary Clock Select Register at address offset 302H
- B Side Secondary Clock Select Register at address offset 303H
- A Side Primary Clock Watchdog Count Register at address offset 304H
- B Side Primary Clock Watchdog Count Register at address offset 305H
- A Side Secondary Clock Watchdog Count Register at address offset 306H
- A Side Secondary Clock Watchdog Count Register at address offset 307H
- A Side Tertiary Clock Select Register at address offset 208H
- B Side Tertiary Clock Select Register at address offset 209H

The following sections describe the register content.

A Side Primary Clock Select Register

The A Side Primary Clock Select Register controls the source of the primary reference clock for the A side H.110 Switch. The bit descriptions are listed in the following tables:

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Table 103. A Side Primary Clock Select Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	RESERVED				aprisel[3:0]			
Reset Value	00H							
R/W	WRITE Only							
Address	Base+300H							

Table 104. A Side Primary Clock Select Register Bit Field Definitions

Bits	Name	Description
7:4	RSVD	RESERVED
3:0	aprisel[3:0]	This register is a write only register. The bit value loaded into the 4 LSB positions is used to select a source for the A Side H.110 Switch Primary Reference input. The selection values are as follows: **Bit Field Value** — **Input Source** 0 — Ground (Default) 1 — A Side TEMUX Receiver Clock 1 2 — A Side TEMUX Receiver Clock 2 3 — B Side TEMUX Receiver Clock 1 4 — B Side TEMUX Receiver Clock 2 5 — A Side Monitor FALC Receiver Clock 6 — B Side Monitor FALC Receiver Clock 7 — A Side H.110 Switch 1.544 MHz reference 8 — B Side H.110 Switch 1.544 MHz reference 9 — 1.544 MHz 20ppm Reference Oscillator All Others — Ground

A Side Secondary Clock Select Register

The A Side Secondary Clock Select Register controls the source of the secondary reference clock for the A side H.110 Switch. The bit descriptions are listed in the following tables:

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Table 105. A Side Secondary Clock Select Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	RESERVED				asecsel[3:0]			
Reset Value	00H							
R/W	WRITE Only							
Address	Base+301H							

Table 106. A Side Secondary Clock Select Register Bit Field Definitions

Bits	Name	Description
7:4	RSVD	RESERVED
3:0	asecsel[3:0]	This register is a write only register. The bit value loaded into the 4 LSB positions is used to select a source for the A Side H.110 Switch Secondary Reference input. The selection values are as follows: **Bit Field Value** — **Input Source** 0 — Ground (Default) 1 — A Side TEMUX Receiver Clock 1 2 — A Side TEMUX Receiver Clock 2 3 — B Side TEMUX Receiver Clock 1 4 — B Side TEMUX Receiver Clock 2 5 — A Side Monitor FALC Receiver Clock 6 — B Side Monitor FALC Receiver Clock 7 — A Side H.110 Switch 1.544 MHz reference 8 — B Side H.110 Switch 1.544 MHz reference 9 — 1.544 MHz 20ppm Reference Oscillator All Others — Ground

B Side Primary Clock Select Register

The B Side Primary Clock Select Register controls the source of the primary reference clock for the B side H.110 Switch. The bit descriptions are listed in the following tables:

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Table 107. B Side Primary Clock Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	RESERVED				bprisel[3:0]			
Reset Value	00H							
R/W	WRITE Only							
Address	Base+302H							

Table 108. B Side Primary Clock Select Register Bit Field Definitions

Bits	Name	Description
7:4	RSVD	RESERVED
3:0	bprisel[3:0]	This register is a write only register. The bit value loaded into the 4 LSB positions is used to select a source for the B Side H.110 Switch Primary Reference input. The selection values are as follows: **Bit Field Value** — **Input Source** 0 — Ground (Default) 1 — A Side TEMUX Receiver Clock 1 2 — A Side TEMUX Receiver Clock 2 3 — B Side TEMUX Receiver Clock 1 4 — B Side TEMUX Receiver Clock 2 5 — A Side Monitor FALC Receiver Clock 6 — B Side Monitor FALC Receiver Clock 7 — A Side H.110 Switch 1.544 MHz reference 8 — B Side H.110 Switch 1.544 MHz reference 9 — 1.544 MHz 20ppm Reference Oscillator All Others — Ground

B Side Secondary Clock Select Register

The B Side Secondary Clock Select Register controls the source of the secondary reference clock for the B side H.110 Switch. The bit descriptions are listed in the following tables:

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Table 109. B Side Secondary Clock Select Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	RESERVED				bsecsel[3:0]			
Reset Value	00H							
R/W	WRITE Only							
Address	Base+303H							

Table 110. B Side Secondary Clock Select Register Bit Field Definitions

Bits	Name	Description
7:4	RSVD	RESERVED
3:0	bsecsel[3:0]	This register is a write only register. The bit value loaded into the 4 LSB positions is used to select a source for the B Side H.110 Switch Secondary Reference input. The selection values are as follows: **Bit Field Value** — **Input Source** 0 — Ground (Default) 1 — A Side TEMUX Receiver Clock 1 2 — A Side TEMUX Receiver Clock 2 3 — B Side TEMUX Receiver Clock 1 4 — B Side TEMUX Receiver Clock 2 5 — A Side Monitor FALC Receiver Clock 6 — B Side Monitor FALC Receiver Clock 7 — A Side H.110 Switch 1.544 MHz reference 8 — B Side H.110 Switch 1.544 MHz reference 9 — 1.544 MHz 20ppm Reference Oscillator All Others — Ground

A Side Primary Clock Watchdog Count Register

The A Side Primary Clock Watchdog Count Register is used to input a Watchdog timeout count value that is used to compare the A Side H.110 switch primary reference input clock against an internal time source. The register will accept any value from 0 to 255 (FF Hex) to use as a count value. Each count is interpreted as 50ns of count delay. The watchdog has a minimum requirement of 14 counts. Any value loaded that is less than 14 (0E Hex) will be interpreted as 14. This minimum count value works out to a delay of 700ns. This

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would correspond to the finest resolution checking available on a 1.544MHz reference clock. If a reference clock is missing, or its positive edge hasn't occurred during the timeout period, then an interrupt is issued on the $\overline{\text{PQ_IRQ1}}$ interrupt line. The apriref bit clears the interrupt. See Table 72 on page 122 for more information on this bit. The mapriref bit can mask the interrupt. See Table 76 on page 125 for more information.

Table 111. A Side Primary Clock Watchdog Count Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	apriwd[7:0]							
Reset Value	00H							
R/W	WRITE ONLY							
Address	Base+304H							

Table 112. A Side Primary Clock Watchdog Count Register Bit Field Definitions

Bits	Name	Description
7:0	apriwd[7:0]	Count Value, greater than 14 (0E Hex).

B Side Primary Clock Watchdog Count Register

The B Side Primary Clock Watchdog Count Register is used to input a Watchdog timeout count value that is used to compare the B Side H.110 switch primary reference input clock against an internal time source. The register will accept any value from 0 to 255 (FF Hex) to use as a count value. Each count is interpreted as 50ns of count delay. The watchdog has a minimum requirement of 14 counts. Any value loaded that is less than 14 (0E Hex) will be interpreted as 14. This minimum count value works out to a delay of 700ns. This would correspond to the finest resolution checking available on a 1.544MHz reference clock. If a reference clock is missing, or its positive edge hasn't occurred during the timeout period, then an interrupt is issued on the $\overline{\text{PQ_IRQ1}}$ interrupt line. The bpriref bit clears the interrupt. See Table 73 on page 123 for more information on this bit. The mbpriref bit can mask the interrupt. See Table 77 on page 127 for more information.

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Table 113. B Side Primary Clock Watchdog Count Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	bpriwd[7:0]							
Reset Value	00H							
R/W	WRITE ONLY							
Address	Base+305H							

Table 114. B Side Primary Clock Watchdog Count Register Bit Field Definitions

Bits	Name	Description
7:0	bpriwd[7:0]	Count Value, greater than 14 (0E Hex).

A Side Secondary Clock Watchdog Count Register

The A Side Secondary Clock Watchdog Count Register is used to input a Watchdog timeout count value that is used to compare the A Side H.110 switch secondary reference input clock against an internal time source. The register will accept any value from 0 to 255 (FF Hex) to use as a count value. Each count is interpreted as 50ns of count delay. The watchdog has a minimum requirement of 14 counts. Any value loaded that is less than 14 (0E Hex) will be interpreted as 14. This minimum count value works out to a delay of 700ns. This would correspond to the finest resolution checking available on a 1.544MHz reference clock. If a reference clock is missing, or its positive edge hasn't occurred during the timeout period, then an interrupt is issued on the $\overline{\text{PQ_IRQ1}}$ interrupt line. The asecref bit clears the interrupt. See Table 72 on page 122 for more information on this bit. The masecref bit can mask the interrupt. See Table 76 on page 125 for more information.

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Table 115. A Side Secondary Clock Watchdog Count Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	asecwd[7:0]							
Reset Value	00H							
R/W	WRITE ONLY							
Address	Base+306H							

Table 116. A Side Secondary Clock Watchdog Count Register Bit Field Definitions

Bits	Name	Description
7:0	asecwd[7:0]	Count Value, greater than 14 (0E Hex).

B Side Secondary Clock Watchdog Count Register

The B Side Primary Clock Watchdog Count Register is used to input a Watchdog timeout count value that is used to compare the B Side H.110 switch secondary reference input clock against an internal time source. The register will accept any value from 0 to 255 (FF Hex) to use as a count value. Each count is interpreted as 50ns of count delay. The watchdog has a minimum requirement of 14 counts. Any value loaded that is less than 14 (0E Hex) will be interpreted as 14. This minimum count value works out to a delay of 700ns. This would correspond to the finest resolution checking available on a 1.544MHz reference clock. If a reference clock is missing, or its positive edge hasn't occurred during the timeout period, then an interrupt is issued on the $\overline{\text{PQ_IRQ1}}$ interrupt line. The bsecref bit clears the interrupt. See Table 73 on page 123 for more information on this bit. The mbsecref bit can mask the interrupt. See Table 77 on page 127 for more information.

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Table 117. B Side Secondary Clock Watchdog Count Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	bsecwd[7:0]							
Reset Value	00H							
R/W	WRITE ONLY							
Address	Base+307H							

Table 118. B Side Secondary Clock Watchdog Count Register Bit Fields

Bits	Name	Description
7:0	bsecwd[7:0]	Count Value, greater than 14 (0E Hex).

A Side Tertiary Clock Select Register

The A Tertiary Primary Clock Select Register controls the source of the Tertiary reference clock for the A side H.110 Switch. The bit descriptions are listed in the following tables:

Table 119. A Side Tertiary Clock Select Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	RESERVED				atersel[3:0]			
Reset Value	00H							
R/W	WRITE Only							
Address	Base+308H							

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Table 120. A Side Tertiary Clock Select Register Bit Field Definitions

Bits	Name	Description
7:4	RSVD	RESERVED
3:0	atersel[3:0]	This register is a write only register. The bit value loaded into the 4 LSB positions is used to select a source for the A Side H.110 Switch Tertiary Reference input. The selection values are as follows: **Bit Field Value** — **Input Source** 0 — Ground (Default) 1 — A Side TEMUX Receiver Clock 1 2 — A Side TEMUX Receiver Clock 2 3 — B Side TEMUX Receiver Clock 1 4 — B Side TEMUX Receiver Clock 2 5 — A Side Monitor FALC Receiver Clock 6 — B Side Monitor FALC Receiver Clock 7 — A Side H.110 Switch 1.544 MHz reference 8 — B Side H.110 Switch 1.544 MHz reference 9 — 1.544 MHz 20ppm Reference Oscillator All Others — Ground

B Side Tertiary Clock Select Register

The B Side Tertiary Clock Select Register controls the source of the Tertiary reference clock for the B side H.110 Switch. The bit descriptions are listed in the following tables:

Table 121. B Side Tertiary Clock Select Register Bit Fields

MPC8260 Bit	0(MSB)	1	2	3	4	5	6	7(LSB)
Buffered Bus Bit	7(MSB)	6	5	4	3	2	1	0(LSB)
Field	RESERVED				btersel[3:0]			
Reset Value	00H							
R/W	WRITE Only							
Address	Base+309H							

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Table 122. B Side Primary Clock Select Register Bit Field Definitions

Bits	Name	Description
7:4	RSVD	RESERVED
3:0	btersel[3:0]	This register is a write only register. The bit value loaded into the 4 LSB positions is used to select a source for the B Side H.110 Switch Tertiary Reference input. The selection values are as follows: **Bit Field Value** — **Input Source** 0 — Ground (Default) 1 — A Side TEMUX Receiver Clock 1 2 — A Side TEMUX Receiver Clock 2 3 — B Side TEMUX Receiver Clock 1 4 — B Side TEMUX Receiver Clock 2 5 — A Side Monitor FALC Receiver Clock 6 — B Side Monitor FALC Receiver Clock 7 — A Side H.110 Switch 1.544 MHz reference 8 — B Side H.110 Switch 1.544 MHz reference 9 — 1.544 MHz 20ppm Reference Oscillator All Others — Ground

3.22 JTAG/BDM Debug Port

The JTAG testing port on the MPC8260 is used to support the EST Common On chip debug Processor (COP) debugger on the P3 connector. The connector is setup to support the extended 16-pin COP debugger signaling, but the basic 10 pin signaling devices may be used with an interposing adapter. The P3 pinout is found in the following table:

Table 123. JTAG Pinout

Pin Number	Signal Name
1	PQ_TDO – JTAG Test Data Out signal
2	!PQ_QACK- Quiescent State Acknowledge, not supported
3	PQ_TDI- JTAG Test Data In signal
4	!PQ_TRST- JTAG Reset and Tri-state signal
5	!PQ_QREQ- Quiescent State Request-
6	V3V
7	PQ_TCK- JTAG Test Clock
8	No Connection

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Table 123. JTAG Pinout *(Continued)*

Pin Number	Signal Name
9	PQ_TMS-JTAG Test Mode Select
10	No Connection
11	!PQ_SRESET- MPC8260 Soft Reset
12	Ground
13	!PQ_HRESET- MPC8260 Hard Reset
14	No Connection
15	!CHKSTPO-Checkstop output, Not supported
16	Ground

All of the control signals are pulled to V3V with a minimum 10K resistor to prevent false actuation when no JTAG controller is connected.

The mechanical requirements for the 16-pin Motorola connector are specified as follows:

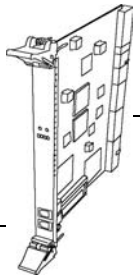
- vertical, 16 (2 X 8) pin header
- .10” between centers of adjacent pins
- .025” square pins
- .23” height of each post

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Section

4



Ethernet Interface

This chapter describes the CPC395 Ethernet Interface. The topics covered include:

- CPC395 Ethernet Overview
- CPC395 Ethernet Redundancy Mode

4.1 Ethernet Overview

Two Ethernet ports are provided on the CPC395 for management purposes. The CPC395 supports mid-plane Ethernet wiring, allowing for the cablefree interconnect between the CPC395 and other CompactPCI-based Ethernet components such as the CPC4400 Ethernet switch.

Two modes of operation are supported by the Ethernet subsystem: dual independent subnet and single subnet dual port mode.

Dual Subnet

In the dual subnet configuration, each port provides access to a separate subnet. In this mode, the CPC395 is configured with two IP addresses and two Ethernet MAC Addresses. The CPC395 can be configured as a gateway in dual subnet mode.

Single Subnet

In single-subnet mode, the CPC395 is configured with one IP address and one MAC Address. This is also called Redundant mode. In this mode, the physical ports are redundant with ENET_A acting as the Primary or preferred port. The Secondary port (ENET_B) is a backup port, used if the Primary port loses link. If there is no link on the Primary port, the CPC395 will hunt for link on both the Primary and Secondary ports. Traffic will resume on the first port where link is established. If link is established on the Secondary port, the CPC395 will continue to hunt for link on the Primary port. If link is established on the Primary port, the CPC395 will force the Secondary port link to go down and will resume traffic on the Primary port. The CPC395 does not hunt for link when the Primary port is active. The Secondary port's link partner will not establish link with the CPC395 when the Primary port is active. Transitions between ports occur within 500ms of link change. The default mode of operation is Redundant Mode.

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The CPC395 Ethernet ports conform to all requirements of the IEEE 802.3 (CSMA/CD) MAC interface. These ports support symmetric flow control using the MAC Control Client interface (Pause) specified in IEEE 802.3u.

Ethernet PHY

The Ethernet PHYs conform to the twisted pair PHY specification for 10 Mbps or 100 Mbps operation in half-duplex or full-duplex mode. The Ethernets support autonegotiation of the proper speed and duplex settings with link partner(s).

At the PHY layer, the Ethernets are presented to 4-wire mid-plane interfaces instead of the standard 100Base-TX MDI. At the mid-plane interface, this port conforms to the Ethernet signaling and voltage level requirements. Network isolation and the (optional) MDI mechanical interface is provided via a separate rear-panel Line Interface Module (LIM).

Two LIM models are available: one with rear panel RJ45 connectors that present the Ethernet interfaces to the network, and one that provides the isolation transformer and presents the Ethernet signals to the midplane. The second LIM model may be used to support applaications that have embedded Ethernet signalling in the mid-plane. If the Ethernet signals are to be embedded into the mid-plane, then it is the integrator's responsibility to provide a mid-plane that simulates the category-5 cable plant requirements specified in ANSI/EIA/TIA 568 for 100BaseTX.

Ethernet MII Management

The Ethernet ports of the CPC395 support the basic IEEE 802.3u MII management register set, including: MII Control and MII Status. The Ethernet ports also support registers 2-6 of the extended IEEE 802.3u MII management register set, including: MII PHY Identifier, MII Auto-Negotiation Advertisement, MII Auto-Negotiation Link Partner Ability, and MII Auto-Negotiation Expansion.

Ethernet Status Indicators

A visible display (LED) is provided for each port to indicate Link and Activity (transmit or receive). A second visible display (LED) is provided for each port to indicate mode (duplex) and speed.

4.2 Ethernet Redundancy Mode

Redundancy mode will typically be used in Fault Tolerant network configurations, as shown in Figure 21. In this architecture, the CPC395 is connected to two Ethernet switches. The CPC4400 is a CompactPCI Ethernet switch that is designed for use in this application.

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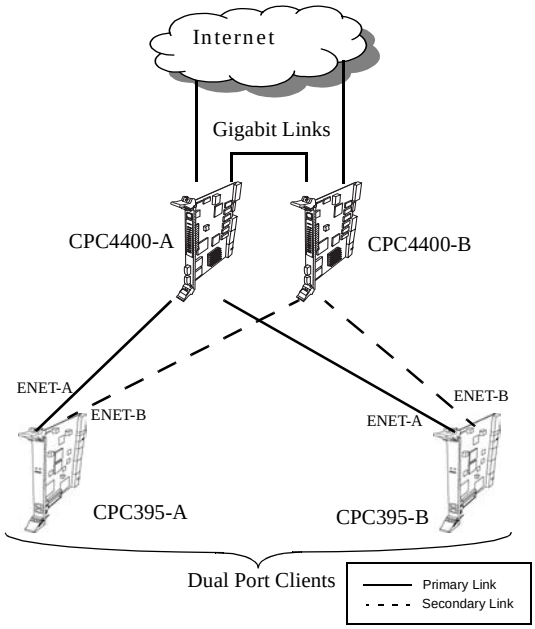


Figure 21 Fault Tolerant Network

When Ethernet Redundancy mode is selected, the two Ethernet ports are “bound” to a single IP interface. The ports are managed as a single entity. All port configuration parameters applied to the interface are applied to both physical ports.

In Redundancy mode, only one port is physically operational at a time. The CPC395 will use the primary (ENET A) port if it detects a valid link state on that port. The CPC395 will prevent a link from being established on the secondary port if the primary port is in use. If the primary port loses link, the CPC395 will hunt for link and if the secondary port is available, the CPC395 will automatically use that port.

In Redundancy mode, all traffic will carry the same IP Address and MAC Address regardless of which port is used. The MAC Address used is the address assigned to ENET_A. If DHCP is enabled, only one address is requested by the CPC395. If DHCP is not enabled, the user-assigned address eth0-IPADDR is used.

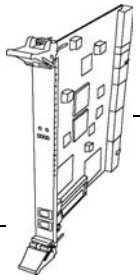
If the secondary port is active and link returns on the primary port, the CPC395 will drop link on the secondary port and use the primary port (i.e., the primary port is preferred when available). Whenever a transition between the ports occurs, the CPC395 will issue a gratuitous ARP reply to ensure that ARP tables are updated on any hosts attached to the new port.

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Section

5



Pinouts & Line Interface Modules (LIMs)

5.1 Product LIM Boards

There are two Line Interface Modules (LIMs) available with the CPC395, one with an internal Ethernet connection via the midplane, and the other with external Ethernet on the rear panel (see Table 124).

Table 124. LIM Boards

LIM Model Number	75 ohm T3 Ports	T1 Monitor Ports	Ethernet Management Ports	Part Number
PT-LIM395-11218 (Figure 22)	2	2	2 midplane	120P0380
PT-LIM395-11219 (Figure 23)	2	2	2 external	120P0392

Following are diagrams of the two available LIMs. For a description of the LEDs on the LIMs, see "LIM Front Panel LEDs" on page 17. Tables showing the LIM pinouts start on page 172.

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LIM Diagrams

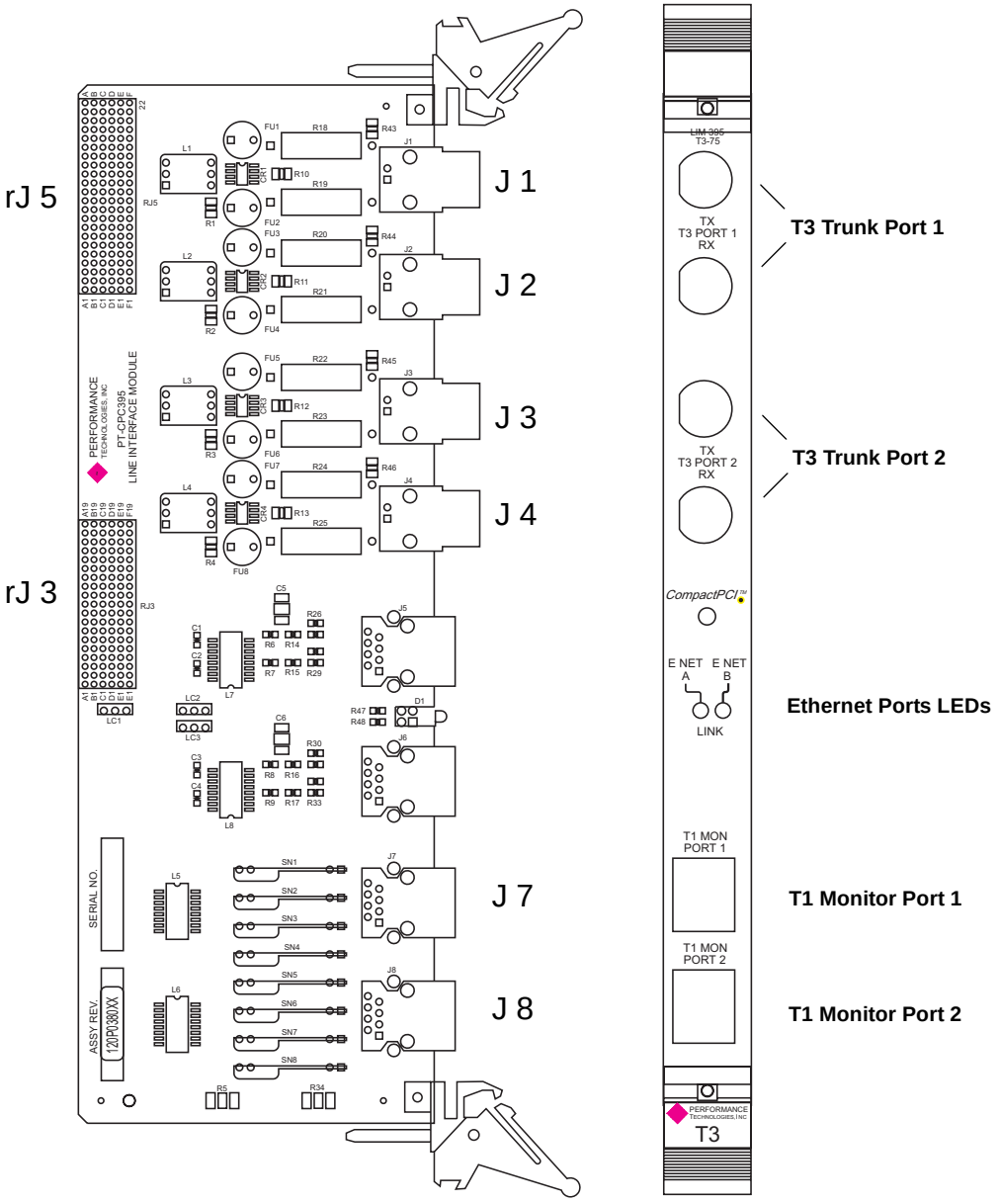


Figure 22. PT-LIM395-11218 with Internal Ethernet

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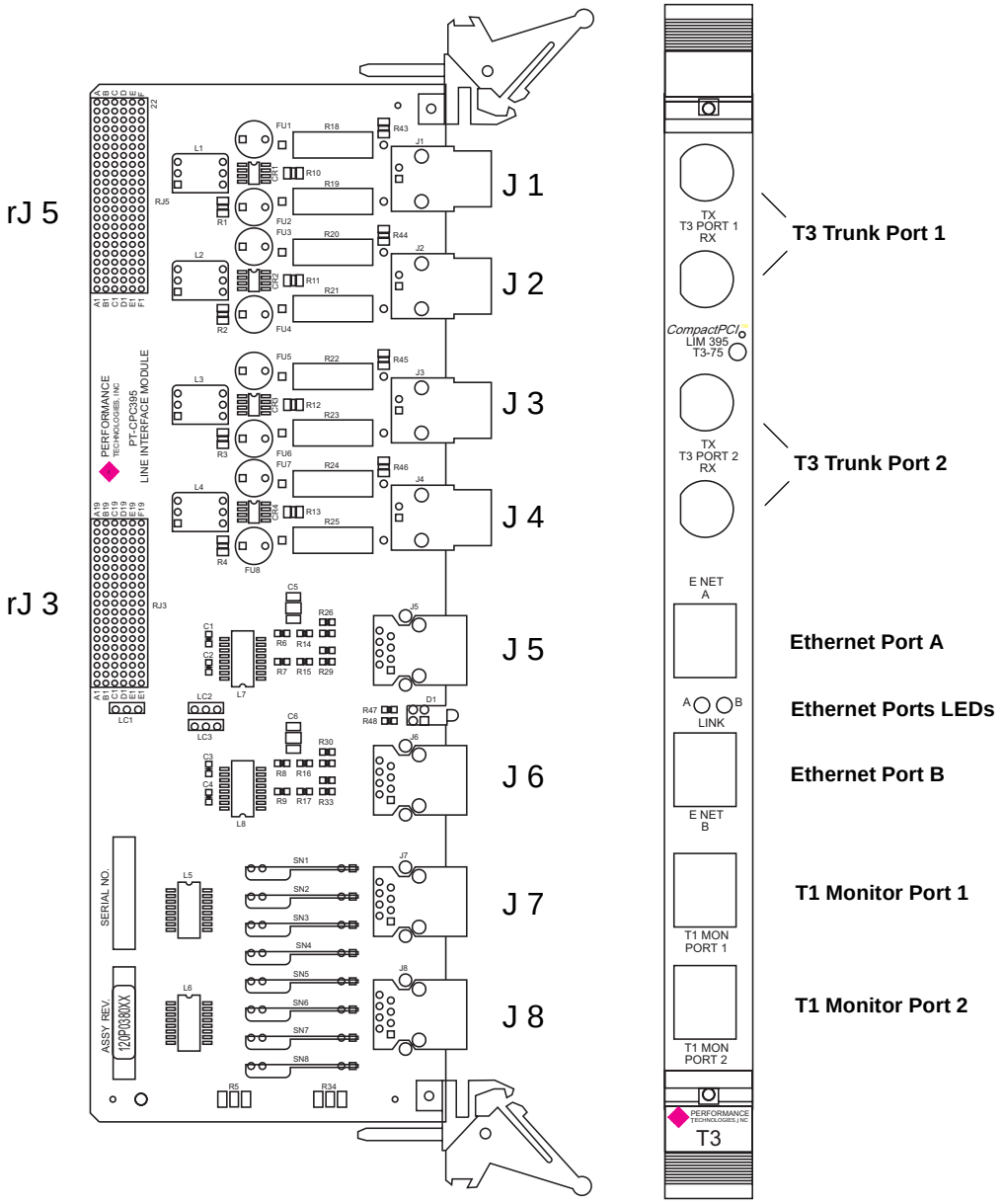


Figure 23. PT-LIM395-11219 with External Ethernet

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5.2 Pinouts

This section defines the pinouts of the interface connectors presented by the CPC395.

CompactPCI Bus Connectors

Table 125. J1 Connector Pinout

Row Number	A	B	C	D	E
25	5V	REQ64#	ENUM#	3.3V	5V
24	AD[1]	5V	V(I/O)	AD[0]	ACK64#
23	3.3V	AD[4]	AD[3]	5V	AD[2]
22	AD[7]	GND	3.3V	AD[6]	AD[5]
21	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]
19	3.3V	AD[15]	AD[14]	GND	AD[13]
18	SERR#	GND	3.3V	PAR	C/BE[1]#
17	3.3V	IPMB SCL	IPMB SDA	GND	PERR#
16	DEVSEL#	GND	V(I/O)	STOP#	LOCK#
15	3.3V	FRAME#	IRDY#	BD SEL#	TRDY#
12-14	Key Area				
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#
10	AD[21]	GND	3.3V	AD[20]	AD[19]
9	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]
7	AD[30]	AD[29]	AD[28]	GND	AD[27]
6	REQ#	GND	3.3V	CLK	AD[31]
5	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#
4	IPMBPWR	HEALTHY#	V(I/O)	INTP	INTS
3	INTA#	INTB#	INTC#	5V	INTD#
2	TCK	5V	TMS	TDO	TDI
1	5V	-12V	TRST#	+12V	5V

Key to J1 Pin Assignments:

- Refer to CompactPCI Specification.

NOTE: A pound (#) suffix indicates active-low signal.

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Table 126. J2 Connector Pinout

Row Number	A	B	C	D	E
22	GA4	GA3	GA2	GA1	GA0
21	RSV	RSV	RSV	RSV	RSV
20	RSV	RSV	RSV	GND	RSV
19	RSV	RSV	RSV	RSV	RSV
18	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18
17	BRSVP2A17	GND	RSV	RSV	RSV
16	BRSVP2A16	BRSVP2B16	RSV	GND	BRSVP2E16
15	BRSVP2A15	GND	RSV	RSV	RSV
14	AD[35]	AD[34]	AD[33]	GND	AD[32]
13	AD[38]	GND	V(I/O)	AD[37]	AD[36]
12	AD[42]	AD[41]	AD[40]	GND	AD[39]
11	AD[45]	GND	V(I/O)	AD[44]	AD[43]
10	AD[49]	AD[48]	AD[47]	GND	AD[46]
9	AD[52]	GND	V(I/O)	AD[51]	AD[50]
8	AD[56]	AD[55]	AD[54]	GND	AD[53]
7	AD[59]	GND	V(I/O)	AD[58]	AD[57]
6	AD[63]	AD[62]	AD[61]	GND	AD[60]
5	C/BE[5]#	GND	V(I/O)	C/BE[4]#	PAR64
4	V(I/O)	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#
3	RSV	GND	RSV	RSV	RSV
2	RSV	RSV	UNC	RSV	RSV
1	RSV	GND	RSV	RSV	RSV

Key to J2 Pin Assignments:

- Refer to CompactPCI Specification.

NOTE: A pound (#) suffix indicates active-low signal.

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Table 127. J3 Connector Pinout

Row Number	A	B	C	D	E
19	BUS_TX1+	BUS_TX1-	Ground	BUS_RX1+	BUS_RX1-
18	Ground	Ground	NC	Ground	Ground
17	NC	NC	NC	NC	NC
16	B_CTRFMA#	B_CTRFMB#	B_CT_MC	B_CTNR1	B_CTNR2
15	Ground	B_CT_RESET#	NC	Ground	VIO
14	B_CTD29	B_CTD30	B_CTD31	LINK1-	Ground
13	B_CTD27	V3V	B_CTD28	V3V	RD1-
12	B_CTD24	B_CTD25	B_CTD26	Ground	RD1+
11	B_CTD21	B_CTD22	B_CTD23	NC	Ground
10	B_CTD19	VDD	B_CTD20	VDD	TD1-
9	B_CTD16	B_CTD17	B_CTD18	Ground	TD1+
8	B_CTD13	B_CTD14	B_CTD15	LINK2-	Ground
7	B_CTD11	VDD	B_CTD12	VDD	RD2-
6	B_CTD8	B_CTD9	B_CTD10	Ground	RD2+
5	B_CTD4	B_CTD5	B_CTD6	B_CTD7	Ground
4	B_CTD0	V3V	B_CTD1	V3V	TD2-
3	B_CT8A	B_CT8B	B_CTD2	Ground	TD2+
2	Ground	Ground	B_CTD3	Ground	Ground
1	BUS_RX2-	BUS_RX2+	Ground	BUS_TX2-	BUS_TX2+

Signal Definitions:

- •B_CT8A Bus H.110 8.192 MHz clock A
- •B_CT8B Bus H.110 8.192 MHz clock B
- •B_CTDx Bus H.110 Data Bit
- •B_CT_MC Bus CT 2 Mbps Message Channel
- •B_CTNR1 Bus CT Net Reference Signal 1
- •B_CTNR2 Bus CT Net Reference Signal 2
- •B_CT_RESET# Bus CT Reset signal, low true
- •B_CTRFMA# Bus H.110 8KHz Frame Pulse A
- •B_CTRFMB# Bus H.110 8KHz Frame Pulse B
- •Ground Digital Ground
- •LINKx Ethernet LED Link/Activity signal to Rear Board (LIM)
- •BUS_TX1+ PSB Ethernet 10/100 Mbps Transmit + Port 1
- •BUS_TX1+ PSB Ethernet 10/100 Mbps Transmit – Port 1
- •BUS_RX1+ PSB Ethernet 10/100 Mbps Receive + Port 1
- •BUS_RX1+ PSB Ethernet 10/100 Mbps Receive - Port 1
- •BUS_TX2+ PSB Ethernet 10/100 Mbps Transmit + Port 2

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•BUS_TX2+	PSB Ethernet 10/100 Mbps Transmit – Port 2
•BUS_RX2+	PSB Ethernet 10/100 Mbps Receive + Port 2
•BUS_RX2+	PSB Ethernet 10/100 Mbps Receive - Port 2
•RD1+	Board Ethernet Port 1, 10/100 Mbps Receive + to Rear Board (LIM)
•RD1-	Board Ethernet Port 1, 10/100 Mbps Receive - to Rear Board (LIM)
•RD2+	Board Ethernet Port 2, 10/100 Mbps Receive + to Rear Board (LIM)
•RD2-	Board Ethernet Port 2, 10/100 Mbps Receive - to Rear Board (LIM)
•TD1+	Board Ethernet Port 1, 10/100 Mbps Transmit + to Rear Board (LIM)
•TD1-	Board Ethernet Port 1, 10/100 Mbps Transmit - to Rear Board (LIM)
•TD2+	Board Ethernet Port 2, 10/100 Mbps Transmit + to Rear Board (LIM)
•TD2-	Board Ethernet Port 2, 10/100 Mbps Transmit - to Rear Board (LIM)
•VDD	Early +5V supplied by the Front Board's unswitched power plane
•V3V	Early +3.3V supplied by the Front Board's unswitched power plane
•VIO	H.110 I/O (+3.3 or +5 Volts) supplied by the Front Board's unswitched power plane
•NC	No Connection

NOTE: A pound (#) suffix indicates active-low signal.

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Table 128. J4 Connector Pinout

Row #	A	B	C	D	E
25	SGA4	SGA3	SGA2	SGA1	SGA0
24	GA4	GA3	GA2	GA1	GA0
23	IN/C	/CT_Reset	/CT_EN	IN/C	CT_MC
22	PFS0#	RSVD	RSVD	RSVD	RSVD
21	IN/C	PFS1#	RSVD	RSVD	IN/C
20	NP	NP	NP	NP	NP
19	NP	NP	NP	NP	NP
18	IN/C	IN/C	IN/C	IN/C	IN/C
17	NP	NP	NP	NP	NP
16	NP	NP	NP	NP	NP
15	IN/C	IN/C	IN/C	IN/C	IN/C
12-14	Key Area				
11	CT_D29	CT_D30	CT_D31	V(I/O)	/CT_FRAME_A
10	CT_D27	+3.3V	CT_D28	+5V	/CT_FRAME_B
9	CT_D24	CT_D25	CT_D26	GND	/FR_COMP
8	CT_D21	CT_D22	CT_D23	+5V	CT_C8_A
7	CT_D19	+5V	CT_D20	GND	CT_C8_B
6	CT_D16	CT_D17	CT_D18	GND	CT_NETREF_1
5	CT_D13	CT_D14	CT_D15	+3.3V	CT_NETREF_2
4	CT_D11	+5V	CT_D12	+3.3V	SCLK
3	CT_D8	CT_D9	CT_D10	GND	SCLK-D
2	CT_D4	CT_D5	CT_D6	CT_D7	GND
1	CT_D0	+3.3V	CT_D1	CT_D2	CT_D3

Key to J4 Pin Assignments:

- •RSVD — Reserved for future use
- •NP — Required to be not populated with pin and pad (i.e. no conductive element present)
- •IN/C — Pin and pad with no connect required for safety agency insulation requirements
- •KEY AREA — Reserved area utilized for keying.
- •CT_FRAME_A — Frame sync A, 125 usec period
- •CT_FRAME _B — Frame sync B, 125 usec period
- •CT_C8_A — Bit clock A, 8.192 MHz
- •CT_C8_B — Bit clock B, 8.192 MHz
- •CT_D[0:31] — Serial data lines, 128 time slots each
- •CT_NETREF_1 — Network timing reference 1
- •CT_NETREF_2 — Network timing reference 2
- •CT_EN — Logic low signal to indicate CT Bus card is seated
- •CT_RESET — Logic low card reset

NOTE: A slash (/) prefix indicates active-low signal.

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Table 129. J5 Connector Pinout

Row Number	A	B	C	D	E
22	Tx1_T	IN/C	Tx2_T	IN/C	IN/C
21	Tx1_R	IN/C	Tx2_R	IN/C	IN/C
20	Rx1_T	IN/C	Rx2_T	IN/C	IN/C
19	Rx1_R	IN/C	Rx2_R	IN/C	IN/C
18	IN/C	IN/C	IN/C	IN/C	IN/C
17	IN/C	IN/C	IN/C	IN/C	IN/C
16	IN/C	IN/C	IN/C	IN/C	IN/C
15	IN/C	IN/C	IN/C	IN/C	IN/C
14	IN/C	IN/C	MTx1_T	IN/C	IN/C
13	IN/C	IN/C	MTx1_R	IN/C	IN/C
12	IN/C	IN/C	MRx1_T	IN/C	IN/C
11	IN/C	IN/C	MRx1_R	IN/C	IN/C
10	IN/C	IN/C	MTx2_T	IN/C	IN/C
9	IN/C	IN/C	MTx2_R	IN/C	IN/C
8	IN/C	IN/C	MRx2_T	IN/C	IN/C
7	IN/C	IN/C	MRx2_R	IN/C	IN/C
6	IN/C	IN/C	IN/C	IN/C	IN/C
5	IN/C	IN/C	IN/C	IN/C	IN/C
4	IN/C	IN/C	IN/C	IN/C	IN/C
3	IN/C	IN/C	IN/C	IN/C	IN/C
2	IN/C	IN/C	IN/C	IN/C	IN/C
1	IN/C	IN/C	IN/C	IN/C	IN/C

Key to J5 Pin Assignments:

- •Tx1_T/R — T3 Channel A Transmit Tip and Ring
- •Rx1_T/R — T3 Channel A Receive Tip and Ring
- •Tx2_T/R — T3 Channel B Transmit Tip and Ring
- •Rx2_T/R — T3 Channel B Receive Tip and Ring
- •MTx1_T/R — T1 Monitor A Transmit Tip and Ring
- •MRx1_T/R — T1 Monitor A Receive Tip and Ring
- •MTx2_T/R — T1 Monitor B Transmit Tip and Ring
- •MRx2_T/R — T1 Monitor B Receive Tip and Ring
- •NP — Required to be not populated with pin and pad (i.e. no conductive element present)
- •IN/C — Pin and pad with no connect required for safety agency insulation requirements.

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Ethernet Ports

Table 130. Switched Ethernet Port Pinout

Pin Number	Signal Name
1	RX+
2	RX-
3	TX+
4	-
5	-
6	TX-
7	-
8	-

RS-232 Console Port

The only signals used are transmit, receive, and ground. The pinout for this port is shown in Table 131.

Table 131. Console Port Pinout

Pin Number	Signal Name
1	-
2	GND
3	RX
4	TX
5	GND
6	-

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T1 Monitor Ports

The CPC395 supports two RJ48C T1 interface ports via the rear panel LIM. The pinout for these ports is shown in Table 132.

Table 132. RJ48C T1 Port Pinout

Pin Number	Signal Name
1	RX_R
2	RX_T
3	-
4	TX_R
5	TX_T
6	-
7	-
8	-

T3 Trunk Ports

The two T3 trunks are presented at the rear panel LIM via four simplex BNC connectors. Each connector is clearly labeled as to the trunk and signal carried by the connector.

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LIM Pinouts

The following table shows the pinout for the LIM rJ3 connector:

Table 133. LIM rJ3 Connector Pinout

Row Number	A	B	C	D	E
19	BUS_TX1+	BUS_TX1-	Ground	BUS_RX1+	BUS_RX1-
18	Ground	Ground	NC	Ground	Ground
17	NC	NC	NC	NC	NC
16	B_CTRFMA#	B_CTRFMB#	B_CT_MC	B_CTNR1	B_CTNR2
15	Ground	B_CT_RESET#	NC	Ground	VIO
14	B_CTD29	B_CTD30	B_CTD31	LINK1-	Ground
13	B_CTD27	V3V	B_CTD28	V3V	RD1-
12	B_CTD24	B_CTD25	B_CTD26	Ground	RD1+
11	B_CTD21	B_CTD22	B_CTD23	NC	Ground
10	B_CTD19	VDD	B_CTD20	VDD	TD1-
9	B_CTD16	B_CTD17	B_CTD18	Ground	TD1+
8	B_CTD13	B_CTD14	B_CTD15	LINK2-	Ground
7	B_CTD11	VDD	B_CTD12	VDD	RD2-
6	B_CTD8	B_CTD9	B_CTD10	Ground	RD2+
5	B_CTD4	B_CTD5	B_CTD6	B_CTD7	Ground
4	B_CTD0	V3V	B_CTD1	V3V	TD2-
3	B_CT8A	B_CT8B	B_CTD2	Ground	TD2+
2	Ground	Ground	B_CTD3	Ground	Ground
1	BUS_RX2-	BUS_RX2+	Ground	BUS_TX2-	BUS_TX2+

Signal Definitions:

- •B_CT8A Bus H.110 8.192 MHz clock A
- •B_CT8B Bus H.110 8.192 MHz clock B
- •B_CTDx Bus H.110 Data Bit
- •B_CT_MC Bus CT 2 Mbps Message Channel
- •B_CTNR1 Bus CT Net Reference Signal 1
- •B_CTNR2 Bus CT Net Reference Signal 2
- •B_CT_RESET# Bus CT Reset signal, low true
- •B_CTRFMA# Bus H.110 8KHz Frame Pulse A
- •B_CTRFMB# Bus H.110 8KHz Frame Pulse B
- •Ground Digital Ground
- •LINKx# Ethernet LED Link/Activity signal to Rear Board (LIM)

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•BUS_TX1+	PSB Ethernet 10/100 Mbps Transmit + Port 1
•BUS_TX1+	PSB Ethernet 10/100 Mbps Transmit – Port 1
•BUS_RX1+	PSB Ethernet 10/100 Mbps Receive + Port 1
•BUS_RX1+	PSB Ethernet 10/100 Mbps Receive - Port 1
•BUS_TX2+	PSB Ethernet 10/100 Mbps Transmit + Port 2
•BUS_TX2+	PSB Ethernet 10/100 Mbps Transmit – Port 2
•BUS_RX2+	PSB Ethernet 10/100 Mbps Receive + Port 2
•BUS_RX2+	PSB Ethernet 10/100 Mbps Receive - Port 2
•RD1+	Board Ethernet Port 1, 10/100 Mbps Receive + to Rear Board (LIM)
•RD1-	Board Ethernet Port 1, 10/100 Mbps Receive - to Rear Board (LIM)
•RD2+	Board Ethernet Port 2, 10/100 Mbps Receive + to Rear Board (LIM)
•RD2-	Board Ethernet Port 2, 10/100 Mbps Receive - to Rear Board (LIM)
•TD1+	Board Ethernet Port 1, 10/100 Mbps Transmit + to Rear Board (LIM)
•TD1-	Board Ethernet Port 1, 10/100 Mbps Transmit - to Rear Board (LIM)
•TD2+	Board Ethernet Port 2, 10/100 Mbps Transmit + to Rear Board (LIM)
•TD2-	Board Ethernet Port 2, 10/100 Mbps Transmit - to Rear Board (LIM)
•VDD	Early +5V supplied by the Front Board’s unswitched power plane
•V3V	Early +3.3V supplied by the Front Board’s unswitched power plane
•VIO	H.110 I/O (+3.3 or +5 Volts) supplied by the Front Board’s unswitched power plane
•NC	No Connection

NOTE: A pound (#) suffix indicates active-low signal.

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Table 134. LIM rJ5 Connector Pinout

Row Number	A	B	C	D	E
22	Tx1_T	IN/C	Tx2_T	IN/C	IN/C
21	Tx1_R	IN/C	Tx2_R	IN/C	IN/C
20	Rx1_T	IN/C	Rx2_T	IN/C	IN/C
19	Rx1_R	IN/C	Rx2_R	IN/C	IN/C
18	IN/C	IN/C	IN/C	IN/C	IN/C
17	IN/C	IN/C	IN/C	IN/C	IN/C
16	IN/C	IN/C	IN/C	IN/C	IN/C
15	IN/C	IN/C	IN/C	IN/C	IN/C
14	IN/C	IN/C	MTx1_T	IN/C	IN/C
13	IN/C	IN/C	MTx1_R	IN/C	IN/C
12	IN/C	IN/C	MRx1_T	IN/C	IN/C
11	IN/C	IN/C	MRx1_R	IN/C	IN/C
10	IN/C	IN/C	MTx2_T	IN/C	IN/C
9	IN/C	IN/C	MTx2_R	IN/C	IN/C
8	IN/C	IN/C	MRx2_T	IN/C	IN/C
7	IN/C	IN/C	MRx2_R	IN/C	IN/C
6	IN/C	IN/C	IN/C	IN/C	IN/C
5	IN/C	IN/C	IN/C	IN/C	IN/C
4	IN/C	IN/C	IN/C	IN/C	IN/C
3	IN/C	IN/C	IN/C	IN/C	IN/C
2	IN/C	IN/C	IN/C	IN/C	IN/C
1	IN/C	IN/C	IN/C	IN/C	IN/C

Key to rJ5 Pin Assignments:

- •Tx1_T/R — T3 Channel A Transmit Tip and Ring
- •Rx1_T/R — T3 Channel A Receive Tip and Ring
- •Tx2_T/R — T3 Channel B Transmit Tip and Ring
- •Rx2_T/R — T3 Channel B Receive Tip and Ring
- •MTx1_T/R — T1 Monitor A Transmit Tip and Ring
- •MRx1_T/R — T1 Monitor A Receive Tip and Ring
- •MTx2_T/R — T1 Monitor B Transmit Tip and Ring
- •MRx2_T/R — T1 Monitor B Receive Tip and Ring
- •NP — Required to be not populated with pin and pad (i.e. no conductive element present)
- •IN/C — Pin and pad with no connect required for safety agency insulation requirements.

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Table 135. LIM J1 Connector: T3 Port 1 Transmit

Connector	Pin	Signal Name	Description
J1	1	T3_TX_PORT1_TIP	T3 Transmit Port 1 Tip
J1	2	T3_TX_PORT1_RING	T3 Transmit Port 1 Ring

Table 136. LIM J2 Connector: T3 Port 1 Receive

Connector	Pin	Signal Name	Description
J2	1	T3_RX_PORT1_TIP	T3 Receive Port 1 Tip
J2	2	T3_RX_PORT1_RING	T3 Receive Port 1 Ring

Table 137. LIM J3 Connector: T3 Port 2 Transmit

Connector	Pin	Signal Name	Description
J3	1	T3_TX_PORT2_TIP	T3 Transmit Port 2 Tip
J3	2	T3_TX_PORT2_RING	T3 Transmit Port 2 Ring

Table 138. LIM J4 Connector: T3 Port 2 Receive

Connector	Pin	Signal Name	Description
J4	1	T3_RX_PORT2_TIP	T3 Receive Port 2 Tip
J4	2	T3_RX_PORT2_RING	T3 Receive Port 2 Ring

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Table 139. LIM J5 Connector: Ethernet Port A

Connector	Pin	Signal Name	Description
J5	1	LPA_TX+	10/100 Ethernet Port A Transmit Plus
J5	2	LPA_TX-	10/100 Ethernet Port A Transmit Minus
J5	3	LPA_RX+	10/100 Ethernet Port A Receive Plus
J5	4	LPA_BS1_NC4	Bob Smith Terminated Differential Pair (No Connect Pin 4)
J5	5	LPA_BS1_NC5	Bob Smith Terminated Differential Pair (No Connect Pin 5)
J5	6	LPA_RX-	10/100 Ethernet Port A Receive Minus
J5	7	LPA_BS2_NC7	Bob Smith Terminated Differential Pair (No Connect Pin 7)
J5	8	LPA_BS2_NC8	Bob Smith Terminated Differential Pair (No Connect Pin 8)

Table 140. LIM J6 Connector: Ethernet Port B

Connector	Pin	Signal Name	Description
J6	1	LPB_TX+	10/100 Ethernet Port B Transmit Plus
J6	2	LPB_TX-	10/100 Ethernet Port B Transmit Minus
J6	3	LPB_RX+	10/100 Ethernet Port B Receive Plus
J6	4	LPB_BS1_NC4	Bob Smith Terminated Differential Pair (No Connect Pin 4)
J6	5	LPB_BS1_NC5	Bob Smith Terminated Differential Pair (No Connect Pin 5)
J6	6	LPB_RX-	10/100 Ethernet Port B Receive Minus
J6	7	LPB_BS2_NC7	Bob Smith Terminated Differential Pair (No Connect Pin 7)
J6	8	LPB_BS2_NC8	Bob Smith Terminated Differential Pair (No Connect Pin 8)

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Table 141. LIM J7 Connector: T1 Monitor Port 1

Connector	Pin	Signal Name	Description
J7	1	MRX1_RING	T1 Receive Port 1 Ring
J7	2	MRX1_TIP	T1 Receive Port 1 Tip
J7	3	NC3	No Connect Pin 3
J7	4	MTX1_RING	T1 Transmit Port 1 Ring
J7	5	MTX1_TIP	T1 Transmit Port 1 Tip
J7	6	NC6	No Connect Pin 6
J7	7	NC7	No Connect Pin 7
J7	8	NC8	No Connect Pin 8

Table 142. LIM J8 Connector: T1 Monitor Port 2

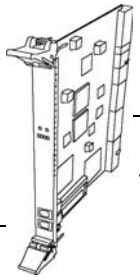
Connector	Pin	Signal Name	Description
J8	1	MRX2_RING	T1 Receive Port 2 Ring
J8	2	MRX2_TIP	T1 Receive Port 2 Tip
J8	3	NC3	No Connect Pin 3
J8	4	MTX2_RING	T1 Transmit Port 2 Ring
J8	5	MTX2_TIP	T1 Transmit Port 2 Tip
J8	6	NC6	No Connect Pin 6
J8	7	NC7	No Connect Pin 7
J8	8	NC8	No Connect Pin 8

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Section

6



Specifications

6.1 Electrical

Universal I/O

The CPC395 is a universal I/O board (i.e., no key on J1), and accepts either 5.0 vdc or 3.3 vdc for the PCI I/O signals.

Power Budget

Refer to Table 143 for a listing of board power consumption.

Table 143. Board Power Consumption

Model and Total Power Consumption	Voltage	Current	Power
CPC395 15.1 W	3.3 V	2.3 A	7.5 W
	5.0 V	1.0 A	5.2 W
	+12.0 V	0.1 A	1.2 W
	-12.0 V	0.1 A	1.2 W

6.2 Mechanical

The CPC395 adhers to the PICMG 2.0 R3.0 CompactPCI specification. The main board is a 6U CompactPCI board (233.35 mm by 160 mm). The rear panel I/O LIMs (Line Interface Modules) are 6U boards as well, however the depth of the LIM board is typically 80 mm.

Front Panel

The CPC395 has a front panel compliant with the IEEE 1101.10 specification and has the following functions.

- RJ-11 console port connection.
- LEDs for ports and system status.

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6.3 Ethernet

Two general purpose FCCs in the MPC8260 perform the full set of IEEE 802.3/Ethernet CSMA/CD media access control (MAC) and channel interface functions at bit rates up to 100Mbps through dual MII media independent interfaces. Each FCC interfaces a single Ethernet PHY on 18 signal lines. The two management signals (MDC and MDIO) required by the MII are implemented separately using the parallel I/O.

6.4 Backplane Connections

The CPC395 is designed to meet the electrical and mechanical requirements of the CompactPCI Specification, PICMG 2.0 D3.0 Oct. 1, 1999, and CompactPCI Computer Telephony Specification, PICMG 2.5 R1.0 Oct. 25, 1999, with specific connections defined on User I/O of connector J3.

6.5 Battery

The M4T28-BR12SH SNAPHAT battery is a detachable lithium power source for the non-volatile Timekeeper surface-mount SOIC device. The SNAPHAT top contains both the battery and the crystal to run the real-time clock and is designed to be “snapped on” after the SOIC is surface mounted on the circuit board. The SNAPHAT package can be snapped off for replacement.

The M4T28-BR12SH has been recognized by Underwriters Laboratories under their Component Recognition Program and carries U.L. File Number E89556.



CAUTION: To avoid draining battery, do not place SNAPHAT pins in a conductive foam.

For battery disposal, contact one of the following recyclers for more information.

Safety-Kleen/BDT Inc.
4255 Research Parkway
Clarence, NY 14031
Phone: (716) 759-2868
FAX: (716) 759-6034

ENSCO
309 American Circle
El Dorado, AR 71730
Phone: (870) 864-3602
FAX: (870) 864-3674

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Chemical Waste Management (TWI)
7 Mobile Ave.
Sauget, IL 62201
Phone: (618) 271-2804
FAX: (618) 271-2128

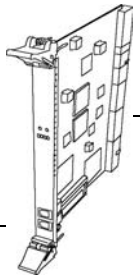
TOXCO
PO Box 232
Trail, BC, Canada, V1R 4L5
Phone: (250) 367-9882
FAX: (250) 367-9875

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Section

7



In Case of Difficulty

7.1 Product Support

If you encounter difficulty in using this Performance Technologies, Inc., product, you can contact our support personnel in several ways. The product model and serial number should be referenced.

Internet

www.pt.com

This is the preferred method of contacting customer support.

Email

support@pt.com

Describe your problem in detail. Please include your return email address and a telephone number.

Fax

585-256-0791

Mark your fax “Attention: Product Support.” Describe your problem in detail. Please include your return fax number and a telephone number.

Telephone

585-256-0248

Request Product Support. Our offices are open between 8:00 am and 5:00 pm Eastern Time, Monday through Friday.

If you are located outside North America, we encourage you to contact the local Performance Technologies distributor or agent for support. Many of our distributors or agents maintain technical support staffs.

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Product Warranty

Performance Technologies (hereinafter “PTIX”) warrants that its products sold hereunder will at the time of shipment be free from defects in material and workmanship and will conform to PTIX’s applicable specifications or, if appropriate, to Buyer’s specifications accepted by PTIX in writing. If products sold hereunder are not as warranted, PTIX shall, at its option, refund the purchase price, repair, or replace the product provided proof of purchase and written notice of nonconformance are received by PTIX within 12 months of shipment, or in the case of software and integrated circuits within ninety (90) days of shipment and provided said nonconforming products are returned F.O.B. to PTIX’s facility no later than thirty days after the warranty period expires. Products returned under warranty claims must be accompanied by an approved Return Material Authorization number issued by PTIX and a statement of the reason for the return. Please contact PTIX, or its agent, with the product serial number to obtain an RMA number. If PTIX determines that the products are not defective, Buyer shall pay PTIX all costs of handling and transportation. This warranty shall not apply to any products PTIX determines to have been subject to testing for other than specified electrical characteristics or to operating and/or environmental conditions in excess of the maximum values established in applicable specifications, or have been subject to mishandling, misuse, static discharge, neglect, improper testing, repair, alteration, parts removal, damage, assembly or processing that alters the physical or electrical properties. This warranty excludes all cost of shipping, customs clearance and related charges outside the United States. Products containing batteries are warranted as above excluding batteries.

THIS WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES WHETHER EXPRESS, IMPLIED OR STATUTORY INCLUDING IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS. IN NO EVENT SHALL PTIX BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES DUE TO BREACH OF THIS WARRANTY OR ANY OTHER OBLIGATION UNDER THIS ORDER OR CONTRACT.

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Product Return Procedure

If you find that your Performance Technologies product must be returned for repair, please use a copy of the following form and include it with the returned product:

To return any equipment, you need to obtain a Return Material Authorization (RMA) number. Performance Technologies will not accept returns without an RMA number.

To obtain an RMA number, please contact the Performance Technologies Customer Service Group by email, Fax or telephone. Outside of North America, customers should contact their Performance Technologies agent.

Performance Technologies will request the serial number of the unit and the reason for the return at the time the RMA is issued. RMA# _____

What product are you returning?

What address do you want us to return the product to? If you do not give us an address it will be shipped back to the Ship To Address as listed on the invoice.

What is the problem with the product?

Please enter the information that the Performance Technical Support representative has given you for the reason for return of this product.

Model Number: _____

Description of problem: _____

_____

_____

Return products should be shipped in the original packaging if possible. Ship via a traceable carrier and properly insure the package. No C.O.D.s are accepted and any shipping charges are non-refundable. Send your returns to:

Performance Technologies, Inc.
Attn: RMA# (Your RMA# goes here)
205 Indigo Creek Dr.
Rochester, N.Y. 14626 U.S.A.

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(Customers outside of North America should follow the return shipment instructions issued by your Performance Technologies agent.) The RMA number should be clearly marked on the outside of the shipping box to expedite correct handling at the Performance Technologies factory.

Repairs will be performed only on complete units. Return of incomplete equipment may delay the repair.

Please note that removal of original parts or product modification by a customer can void the warranty. (This does not apply to jumpers or socketed user-programmable parts.)

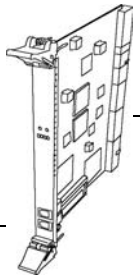
“Out of warranty” repairs cannot proceed without a Purchase Order to cover estimated cost of the repair.

Performance Technologies will supply repair information on all returns and warrants all repairs for 90 days after product is returned to the user.

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Section

8



Glossary

Agent

Software that receives queries and returns replies on behalf of an application. In network management systems, agents reside in all managed devices and report the values of specified variables to management stations.

AIS

Alarm Indication Signal or Blue Alarm - Alarm state that means either the CSU input has gone down or a regenerator on the netwok has failed.

AMI

Alternative Mark Inversion. A line coding method that does not account for one’s density. The customer must ensure sufficient pulses in the data stream.

API

Application Program Interface. Means of communication between programs to give one program transparent access to another. APIs serve various computing purposes. In networking, for example, an API offers software applications (such as a database manager) transparent access to files, devices or interprocess communications.

ARP

Address Resolution Protocol. Internet protocol for dynamically mapping Internet addresses to physical hardware addresses or LANs. Limited to LANs that support hardware broadcast.

ASCII

American Standard Code for Information Interchange

ASIC

Application-Specific Integrated Circuit.

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B3ZS

Bipolar 3 Zero Substitution signaling arrangement that allows for meeting ones density on the T3 line. This scheme substitutes a known violation pattern for 3 consecutive zeros. The substitution is removed at the far end.

B8ZS

Bipolar 8 Zero Substitution signaling arrangement that allows for meeting ones density on the T1 line. This scheme substitutes a known violation pattern for 8 consecutive zeros. The substitution is removed at the far end.

Blue Alarm

See AIS.

BRI

Basic Rate Interface. An international standard switched digital interface offering two 64 Kbps B, or bearer, channels and a 16 Kbps D, or signaling, channel to carry voice, data, or video signals.

B Channel

In ISDN, a full duplex, 64 Kbps channel for sending data.

BPS

Bits per second

BPV

Bipolar Violation. Line coding error where successive pulses are the same polarity.

C Bit Parity

T3 framing structure that uses the management overhead bits (X, P, M, F), but differs in that the Control Bits (C-Bits) are used for additional functions (FID, FEAC, FEBE, TDL, CP).

C-Bits

Cobtrol Bits. Functionality depends on the T3 framing mode. Normally used for bit stuffing.

CP Bits

C bit Parity Bits - Serve the same function as the P bits in the M13 framing format. Allows for greater error checking capability on the M frame itself.

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CompactPCI

A computer chassis standard. (http://www.picmg.org) It is an electrically similar superset of the desktop PCI bus standard with a different physical form factor. CompactPCI uses the Eurocard form factor popularized by the VME bus.

CRC

Cyclic Redundancy Code - Code used for error checking.

CSMA/CD

(Carrier-Sense Multiple Access with Collision Detection) Channel access method used by Ethernet and IEEE 802.3 in which devices transmit only after finding the data channel clear for some period of time. When two devices transmit simultaneously, a collision occurs and the colliding devices delay their retransmissions for a random length of time.

CTBus

Computer Telephony Bus - This is a standard telephony device interface defined by the ECTF. The physical layer is specified under H.100 and H.110.

D4/SuperFrame

The framing format that groups 12 frames together and utilizes the 12 T1 framing bits to provide a repetitive pattern allowing other equipment to lock on to the framing pattern.

D Channel

The D channel is the full duplex 16 Kbps (basic rate) or 64 Kbps (primary rate) ISDN signaling channel which carries messages between the customer equipment and the public switch. Messages can communicate call request information (phone numbers) and incoming call information, for example.

DCE

Data Communications Equipment. A communications device that can establish, maintain and terminate a connection (for example, a modem). A DCE may also provide signal conversion between the data terminal equipment (DTE) and the common carrier's channel. Contrast DTE.

DHCP

Dynamic Host Configuration Protocol. DHCP is the process by which servers assign IP addresses to a networked computer. It is done in a random manner from a pool of IP addresses.

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DS (Digital Signal)

Standard specifying the electrical characteristics for data transmission over four-wire telco circuits. DS-1 is 1.544 Mbps and DS-3 is 44.736 Mbps. Also referred to as T1 and T3.

DS-1

Digital (transmission) System 1, or Digital Signal level 1; refers to the 1.44 Mbps (U.S.) or 2.108 Mbps (Europe) digital signal carried on a T1 circuit.

DS-3

Digital (transmission) System 3, or Digital Signal level 3; refers to the 44 Mbps digital signal carried on a circuit.

DSR

Data Set Ready (modems)

DTE

Data Terminal Equipment. End-user equipment, typically a terminal or computer, that can function as the source or destination point of communication on the network Contrast DCE.

DTR

Data Terminal Ready (modems)

EIA/TIA

Electronic Industries Association./Telecommunications Industries Association.

ECTF

Enterprise Computer Telephony Forum. A trade group committed to the development of standards and specifications that enable interoperability between Computer Telephony equipment.

ESF

Extended Super Frame. T1 framing format that groups 24 T1 frames together. Allows optimization for framing on the T1 line. Adds additional features of CRC, FDL, and frame synchronization which are not available from D4.

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Ethernet

IEEE-standard data link protocol that specifies how data is placed on and retrieved from a common transmission medium. Forms the underlying transport vehicle used by several upper-level protocols, including TCP/IP and XNS. See CSMA/CD for a description of Ethernet's media-access method.

F Bits

Four bits per superframe that are used as a subframe alignment signal. They help to identify each of the overhead bit positions in T3.

FDL

Facility Data Link - Method in ESF to send performance information to the carriers through the framing bits. 4 kbps of the framing is used for FDL. FDL also allows proprietary information to be sent to the far end unit.

FE

Framing Error - Statistic item. Caused by errors in M/F in T3 and by frame mis-alignment in T1.

FEAC

Far End Alarm and Control Channel - Allows loop codes to be sent between devices. Also allows performance information to be exchanged.

FEBE

Far End Block Errors - Used to indicate that CP bit parity errors were received by the transmitting device and the device is notifying the far end.

FECCV

Far End Cbit Coding Violation.

FECES

Far End Cbit Errored Second - T3 Statistic.

FECSES

Far End Cbit Severely Errored Second - T3 Statistic.

FEUAS

Far End Unavailable Second - T3 Statistic.

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FID

Format ID - Identifies the M frame as a C bit Parity application (T3).

FTP

File Transfer Protocol. The Internet application and protocol used to send complete files over TCP/IP services.

Full Duplex

The ability of a device or line to transmit data simultaneously in both directions.

Gateway

Device that can interconnect networks with different, incompatible communications protocols.

H.100/H.110

A set of ECTF standards defining the physical layer operation of the CTBus. H.100 is a bus typically implemented in PCI systems. H.110 is typically implemented in CPCI systems.

Half Duplex

Data transmission that can occur in two directions over a single line, but only one direction at a time. Contrast full duplex.

IP Address

Internet Protocol Address. The number that specifies a device or machine's precise location on the Internet. It consists of four parts separated by dots.

ISDN (Integrated Services Digital Network)

The recommendation published by CCITT for private or public digital telephone networks where binary data, such as graphics and digitized voice and data transmission, pass over the same digital network that carries most telephone transmissions today.

ITU

International Telecommunications Union

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LIM

Line Interface Module - The rear panel transition module that brings I/O from a CPCI board out to user interfaces. It is typically passive to reduce the potential for failure, that would require cable disconnects to perform a swapout.

LIU

Line Interface Unit. Device that provides for electrical encoding and isolation between the framer and the physical interface.

LOF/OOF

Loss of Frame/Out of Frame - 2/4 consecutive framing errors (T1). 3/16 consecutive M or F bit errors (T3).

LOS

Loss of Signal - 175 consecutive pulse positions with no pulses.

M13 Framing

Multiplexer from DS-1 to DS-3. Utilizes all of the Cbits for bit stuffing.

MAC

Media Access Control. A method of controlling access to a transmission medium. For example, token ring, Ethernet, FDDI, etc.

Packet

Unit of data sent across a packet switching network such as the Internet.

Packet Switching

Type of data transfer that occupies a communication link only during the time of actual data transmission. Messages are split into packets and reassembled at the receiving end of the communication link

Packet-switched network

A network in which data is transmitted in units called packets. The packets can be routed individually over the best available network connection and reassembled to form a complete message at the destination.

PCI

Peripheral Component Interconnect (Bus)

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PCM

Pulse Code Modulation

Physical Layer

First layer of the OSI Reference Model; governs hardware connections and byte-stream encoding for transmission. It is the only layer that involves a physical transfer of information between network nodes.

Ping

Packet INternet Groper. A program used to test reachability of destinations by sending them an ICMP echo request and waiting for a reply. Ping is used as a verb: "Ping the host to see if it is available."

PRI

Primary Rate Interface. In the US, the Primary Rate Interface is split into 23 B channels and one 64 K bit/second D channel. PRI is delivered over the same physical link as a T1, or 1.55 M bit/second link. In Europe, PRI is split into 30 B channels and one 64 k bit/second D channel and is delivered over a single E1 link 2.08 M bit/second.

Protocol

The rules that two or more computers must follow to exchange information. These rules provide uniform specifications that computer hardware and software use to communicate, A Protocol describes the formal of messages that can be sent as well as the way a computer should respond to each message.

Protocol Stack

Related layers of protocol software that function together to implement a particular communications architecture.

PSDN

Packet Switching Data Network

QRSS

Quasi-Random Signal Source - Pattern that is used for testing T1 lines. Simulates live data.

Red Alarm/CFA

Carrier Failure Alarm - Alarm state on a T1/T3 that refers to a loss of signal or loss of frame. Can be caused by a network cable break.

SES

Severely Errored Second - greater than 320 error events (T1) or 44 error events (T3).

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SNMP

Simple Network Management Protocol - A TCP/IP based protocol used to remotely manage networking devices.

T1

Communications circuit provided by long distance carriers for voice and data transmission (1.544 Mbps in U.S. or 2.054 Mbps in Europe); may be divided in 24 separate 64 Kb channels; E-1 in Europe.

T3

Digital communications circuit standard created by AT&T that operates at 44 Mbps.

TCP/IP

Transmission Control Protocol / Internal Protocol. Set of protocols developed by the U.S. Defense Department's Advanced Research Projects Agency (ARPA) during the early 1970s. Its intent was to develop ways to connect different kinds of networks and computers. TCP/IP does not have the functionality that OSI provides.

TDM

Time Division Multiplexing. Technique where information from multiple channels may be allocated bandwidth on a single wire based on time slot assignment.

Telco

Telephone company.

Telnet

A connection that allows a user to connect to a computer from a remote location. Once connected, you can then use the applications or programs located on that computer.

Timing Slip

Loss of timing reference normally caused by clock jitter.

UAS

Unavailable Second - LOS or 10 consecutive SES.

Yellow Alarm/RAI

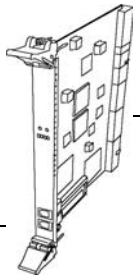
Remote Alarm Indication. Alarm state on T1/T3 that indicates the far end device is having a problem.

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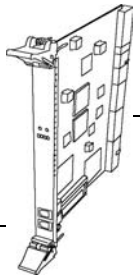
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