Product Specification

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CPC396

Dual T3/DS-3 Adapter

1.0 General Description

The CPC396 is one of Performance Technologies' IPnexus™ family of IP telephony products. It is a CompactPCI® form-factor ECTF CTBus (H.110) Interface card with dual T3 Media and dual Ethernet Control Interfaces. The product is targeted at the CompactPCI-based Computer/Telephony products marketplace. Models include:

- CPC396 - 11365, with dual T3/DS-3 adapter, PICMG 2.16 compliant.
- CPC396C - 11412, with circuit switching software.
- CPC396N - 11235, with NexusWare™ Linux development environment.

The default configuration of the CPC396 terminates all 1344 DS-0s from two T3 links to one H.110 CTBus. Options allow the CPC396 to be configured to terminate all of the 672 DS-0s on each T3 to separate H.110 buses.

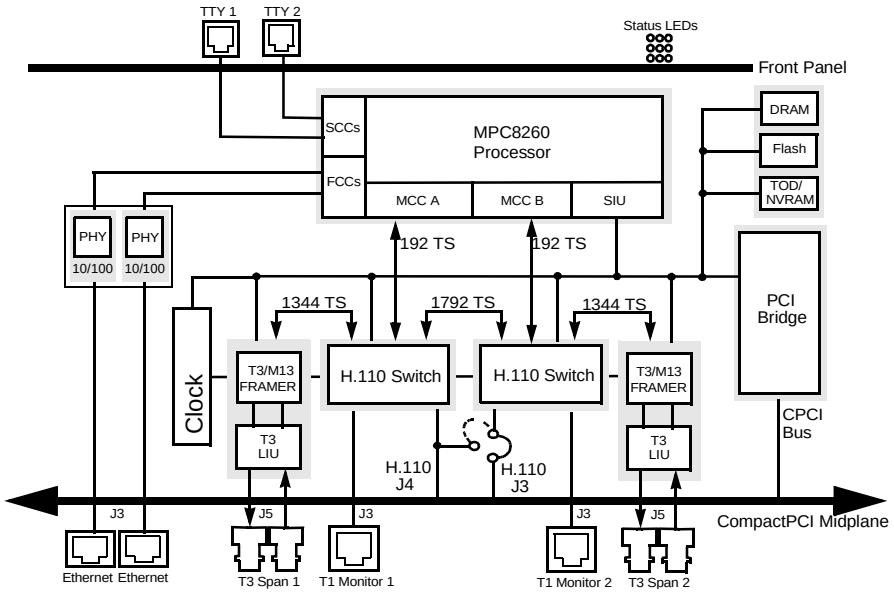
Using the Motorola MPC8260 PowerQUICC II processor, the CPC396 is fully channelized, supporting full DS-0 to DS-3 multiplexing. The CPC396 also supports an embedded Linux OS, Hot Swap, Dual-Ethernet, passive Rear I/O, and the ECTF H.110 bus.

Integral to all IPnexus products is the support of PICMG 2.16 (CompactPCI Packet Switching Backplane).

FEATURES

- 6U CompactPCI Form Factor
- PICMG 2.16 compliant
- MPC8260 PowerQUICC II processor with EC603e PowerPC 200MHz CPU/ 133MHz CPM/ 66MHz Bus microprocessor core
- NexusWare™ Embedded Linux Development Environment
- TDM Circuit Switch Software Option
- 128 MByte SDRAM
- Hot Swap CompactPCI 32/64 bit 33 MHz Interface
- Direct DS-3 to DS-0 Conversion
- Dual T3 LIUs and Framers
- Dual ECTF H.110 Controllers
- 56 T1 Framing Channels (28 per T3)
- Dual 10/100 Base-T Ethernet ports
- Dual Serial Management Controllers
- Extensive Clocking Options
- Remote TCP/IP-based API
- SNMP Management
- H.110 API (Based on opentelecom.org specification)
- Supports PICMG R.3 System Management Bus (SMB)

PICMG 2.16 is an extension to the PICMG 2.x family of specs that overlays a packet-based switching architecture on top of CompactPCI to create an Embedded System Area Network (ESAN).



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2.0 Applications

The CPC396 is designed to be an integral component in a wide array of Computer Telephony applications, including: VoIP Gateways, Interactive Voice Response Systems, Internet Intercept systems, Fax Servers, Automatic Call Distributors, Predictive Dialers, E-mail Voice Gateways, Signalling Gateways, etc. All of these applications, and many others, must provide an interface between the PSTN and the ECTF (Enterprise Computer Telephony Forum) Computer Telephony Bus (CTBus).

The CTBus provides users with a standard interface that enables inter-operability between telecom equipment vendors. This allows the user to construct a variety of telecom application solutions using off-the-shelf components. The CPC396 provides termination of two full DS-3 links to two CTBus interfaces for those applications that need to process high volumes of call traffic in as small a footprint as possible.

Following are the key attributes of the CPC396 that make it ideal for these applications:

1. Its powerful processor can handle the significant densities and provide the performance required in these applications.

2. Its capability to transfer data between T3, T1/E1/J1 spans, Ethernet, PCI Bus, or H.110 Bus.

3. Available onboard Linux operating system (NexusWare), or circuit-switching software, to simplify additional development.

4. PICMG 2.16 compliance.

Please visit our website at www.pt.com for more application examples.

2.1 Integrated Media/Signaling Gateway and Softswitch Example

Media/Signaling Gateways and Softswitches can combine the functionality of all three IP telephony functions in a single chassis. The CPC396 can be used to allocate T3/DS-3 voice trunks from the PSTN and pass data to the H.110 TDM switch and on to DSP resources, the PCI bus, rear panel Ethernet, or midplane Ethernet (CompactPCI/PSB).

2.2 VoIP Media Gateway Example

The CPC396 is particularly well suited for VoIP Media Gateway applications. The voice-over-IP media gateway consists of three major functional blocks: Allocation, Conversion, and Aggregation. These blocks make up

the simplified bridge architecture between traditional PSTN voice and packetized digital voice on the Internet.

The Allocate function allocates circuits from the PSTN through a TDM switch to H.110-based DSPs. The DSPs convert the PSTN circuit into IP frames. The IP frames are collected and aggregated into a fat-pipe to be sent over the Internet. Another Performance Technologies product, the CPC4400 24+2 CompactPCI Ethernet Switch provides the aggregation function in this example. See Figure 1.

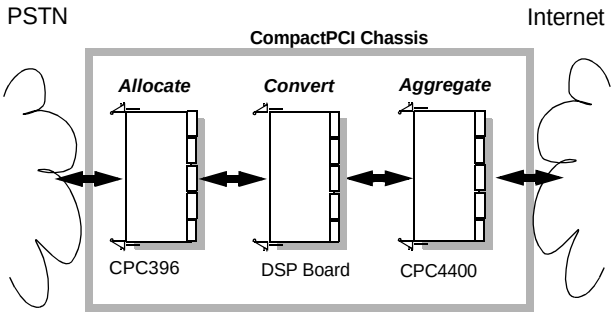

Figure 1. VoIP Media Gateway

3.0 CPC396 Architecture Overview

An overview of the major functional blocks is provided here. Subsequent sections provide more detail.

3.1 Processor

The CPC396 may be used as a standalone device. All of the functionality required for the CPC396 to operate as a TDM switch is included onboard. An onboard communication processor oversees all of the functions of the CPC396. The processor used is the MPC8260 PowerQUICC II. The PowerQUICC II is a versatile communications processor that integrates, on one chip, a high performance PowerPC™ RISC microprocessor and a variety of communications peripheral controllers. The CPC396 utilizes the on-chip communications peripherals for Ethernet (FCCs), Console ports (SCCs), and the Multi-channel Communication Controllers (MCCs).

3.2 MultiChannel Communication Controllers

The MCCs support processor access to up to 256 Full Duplex DS-0 channels, switched via the H.110 controllers. Any set of DS-0s can be terminated from the T1 Monitor ports, T3 Trunks, or H.110 buses. The processor performs protocol processing at the DS-0, fractional T1, or full T1 level.

3.3 Ethernet Ports

Two Ethernet ports are provided with support for either independent or dual-homed subnet operation. In dual-homed mode, the CPC396 will automatically switch over to the secondary Ethernet port if link is lost on the primary port.

The CPC396 supports mid-plane Ethernet wiring, allowing cable-free interconnect between the CPC396 and other CompactPCI-based Ethernet components, such as the CPC4400 Ethernet switch.

3.4 Serial Ports

The two serial ports allow for local access to the card through ASCII terminals. Port 1 is the console port where event logging and alarms are directed. The CPC396N provides two logins, while the CPC396C provides one.

3.5 T3 Trunks

Two onboard T3 transceivers, composed of individual LIUs and framers, send and receive framed serialized DS-3 bit streams, recover timing information, and demultiplex DS-3 data directly to the DS-0 level. The result is dual independent sets of 672 DS-0 channels that are terminated to the two onboard H.110 controllers.

3.6 H.110 Controllers

The H.110 controllers provide switching between one or two ECTF H.110 interfaces and the local resources. The local resources include: the T3/M13 Framers, a multi-channel communication controller within the processor, the T1 Monitor ports, and an inter-switch link used for switching between the two H.110 controllers. Each H.110 controller can support 4096x2342 H.110 bus to local resource timeslots, 2342x2342 local resource to local resource timeslots, or 2048x2048 H.110 to H.110 timeslots.

3.7 T1 Monitor Ports

Two T1 Monitor ports, located on the rear panel Line Interface Module (LIM), provide monitoring of up to 24 DS-0s each. The T1 Monitor transceivers and line interface units provide all of the necessary functions to generate ANSI T1.403 compliant T1 bit streams. The T1 bit streams are brought out to RJ-48C connectors on the LIM. The T1 Monitor transceivers' TDM system interfaces are connected to the local sides of the H.110 switches. The individual DS-0s of each T1 bit stream can be randomly assigned from any of the switched timeslots.

3.8 Clock Control

The CPC396 supports extensive clock synchronization control. The CPC396 may be configured to be a master of the H.110 clocks and supports all H.110 clock fallback recommendations. Any of the network interfaces may be configured to provide a network reference, including the T1 Monitor ports.

4.0 IPnexus™ —Incorporating a Packet Switched Backplane

As well as operating in a standard CompactPCI bus configuration, the IPnexus product family can also operate under the new PICMG 2.16 standard. PICMG 2.16 overlays an embedded Ethernet switching network fabric on the CompactPCI backplane, thus extending CompactPCI's capabilities. It allows developers of next-generation packet-based systems to reduce design complexity and component costs while increasing overall system reliability and performance.

The PICMG 2.16 architecture is based on two concepts:

- An Ethernet infrastructure is embedded in the CompactPCI midplane and is accessed via the J3 connector, with an Ethernet switching element residing in one or more of the CompactPCI slots, interconnecting all the slots in the chassis.
- All boards in the system operate as standalone systems-in-a-slot, interfacing through a network stack on top of Ethernet.

The PICMG 2.16 definition promotes the system-in-a-slot concept, where each card in a chassis operates as a discrete system or subsystem with its own processor, memory and operating system. PICMG 2.16 enables creation of integrated systems in which any card can reside in any link slot and run any operating system, provided that each card supports standard Ethernet protocol communications interfaces. Because integration occurs at the system level, rather than at the driver level, time-to-market is dramatically improved. As requirements change, individual cards, subsystems, or both can be changed without affecting other components in the system.

PICMG 2.16 dramatically improves the performance, scalability and reliability of CompactPCI while preserving its mechanical, power and hot-swap attributes. It also leaves the H.110 telephony bus intact for systems that support that standard. Components that support PICMG 2.16 can be mixed with units that still rely on the CompactPCI bus for communication within the same chassis. Developers will be able to organically grow system capabilities onto the PICMG 2.16 framework over time, since there is no need to change subsystems built around legacy CompactPCI elements. Systems can evolve over time in response to changing needs, without scrapping prior design work.

PICMG 2.16 significantly increases the performance of subsystems in a CompactPCI chassis by moving data traffic off the shared CompactPCI bus and onto an embedded, switched 10/100/1000-Mbit/s Ethernet network. To improve reliability, two fully independent packet buses are defined, providing theoretical backplane throughput rates up to 5 Gbytes/s-an improvement of an order of magnitude over current CompactPCI implementations.

In the PICMG 2.16 definition, up to 20 link slots can be supported using a single fabric (packet-switching) slot in a 19-inch CompactPCI chassis. Redundant “hot-swappable” fabric slots can support up to 19 link slots. By using only one port per slot per fabric, packet-switched backplane performance can range from 250 Mbytes/s (with a single 100-Mbit/s fabric) up to 5 Gbytes/s (with dual switched Gigabyte fabrics). System expansion is accommodated by running CAT5 Ethernet cables to external connections to extend the packet-switched bus. This technique can be used to expand the system to one or more CompactPCI or even non-CompactPCI systems, creating a “virtual backplane.”

This lets designers pick the best-of-class CompactPCI solution for their design without regard to operating system support. Integrators can choose the best solution for any given application. Ethernet connects all units in the chassis so system-integration tasks are greatly simplified. As features are added to the Ethernet standard, systems based on PICMG 2.16 can capitalize on the improvements.

5.0 Electrical

The CPC396 is designed to meet the electrical and mechanical requirements of the CompactPCI specification, PICMG 2.0 D3.0 Sept 24, 1999 and CompactPCI Computer Telephony specification, PICMG 2.5 R1.0 Oct 25, 1999, with specific connections defined on User I/O of connector J3.

5.1 Universal I/O

The CPC396 is a universal I/O board (no key on J1), accepting either 5V or 3.3V for the PCI I/O signals.

5.2 Power Requirements

The power consumption of the CPC396 is shown in Table 1.

Table 1. Board Power Consumption

Model and Total Power Consumption	Voltage	Current	Power
CPC396 16.4 W	3.3 V	2.4 A	8.0 W
	5 V	1.2 A	6.0 W
	+12 V	0.1 A	1.2 W
	-12 V	0.1 A	1.2 W

5.3 Media Connections

Except for the two serial ports, the CPC396 provides connectivity to all media interfaces through the mid-plane J3, J4, and J5 connectors. The two serial ports are presented at the faceplate via RJ11 connectors. A transition cable is provided to bring these interfaces out to standard 25-pin RS-232 connectors.

The T3 trunks and the T1 Monitor ports connect through J5.

The primary CTBus uses the standard H.110 pins on the J4 connector. The secondary CTBus on the dual H.110 model uses proprietary pins on the J3 connector. The signal names on the J3 connector are of the same type and functionality, and adhere to the same timing relationships, as those signals listed in the ECTF CTBus H.110 specification. However, several interoperability signals have been omitted on the J3 connector that were originally required for full H.110 compatibility with the ANSI VITA SCbus. These signals are:

- /FR_COMP, 125 µsec frame pulse
- SCLK, 8.192MHz clock line
- SCLK-D, 8.192MHz clock line
- CT_EN, Logic low signal to indicate CT Bus card is seated. The CT_EN signal on J4 should be used for both CT Buses.

Please note that using the dual H.110 model of the CPC396 requires a non-PICMG-standard custom backplane

For PICMG 2.16 compliance, dual redundant Ethernet is present on the J3 connector, as described in the specification for node slots. Ethernet is also available on the rear panel LIMs for non-PICMG 2.16 configurations.

5.4 Line Interface Module Options

Two LIM options are available for use with the CPC396. One of the LIM options is configured to feed the transformer-isolated Ethernet signals back to the mid-plane for use in applications where the Ethernet signals are embedded into the mid-plane.

The second LIM option presents the Ethernet ports to RJ45 connectors located on the LIM. This option does not feed the transformer-isolated Ethernet signals back to the mid-plane.

Both LIMs provide two RJ48C connectors for the T1 Monitor ports, and four BNC-style connectors for the 75-ohm coax T3 interfaces.

6.0 Mechanical

The CPC396 meets the mechanical requirements specified in the PICMG 2.0 R3.0 CompactPCI and the IEEE 1101.11 specifications.

6.1 Form Factor

The main board is a 6U (233.35 mm by 160 mm) board size. The rear panel I/O LIMs (Line Interface Modules) are also 6U size (233.35 mm). The LIMs are 80 mm in depth for standard applications.

6.2 CompactPCI Connectors

The board uses standard 2 mm Type AB CompactPCI connectors.

6.3 Front Panel

The CPC396 provides a front panel compliant with IEEE 1101.10. The CPC396 front panel provides dual RJ-11 serial port interfaces and LEDs indicating port and system status.

7.0 T3/T1/M13 Framers

The T3/T1/M13 framers perform M13 multiplexing and demultiplexing of T3 to T1 to DS-0. Each T3 framer demultiplexes the T1 channels and feeds them to dedicated onboard T1 framers. The individual DS-0's of each T1 bit stream can be randomly assigned to or from any of the switched timeslots.

The T1 framers support D4 or ESF Framing on a per DS-1 basis.

The T3 framers support B3ZS or HDB3 line encoding and M13 or C-bit Parity Framing Formats.

When using C-bit parity mode, the user has access to improved network diagnostics with the availability of Far End Alarm and Control (FEAC) channel and a Terminal Data Link (TDL). The TDL may be used to report the CPC396 Equipment ID and Location.

C-bit parity also provides the user with better error checking using Far End Block Error (FEBE) checking.

8.0 T3 Line Interface Unit (LIU)

The CPC396 provides two T3 LIU transceivers which perform clock synchronization and data encoding and recovery for transmission over 75-ohm coaxial cable.

The T3 LIUs contain a programmable “Line-Buildout” circuit and equalizer to reduce the effects of cable distortion.

The LIM card provides secondary protection circuitry against electrical hazard.

9.0 T1 Framers

Two T1 Monitor ports, located on the rear panel Line Interface Module (LIM), provide monitoring of up to 24 DS-0s each. The T1 Monitor transceivers and line interface units provide all of the necessary functions to generate ANSI T1.403 compliant T1 bit streams.

The T1 bit streams are brought out to RJ-48C connectors on the LIM. The T1 Monitor transceivers’ TDM System interfaces are connected to the local sides of the H.110 switches. The individual DS-0s of each T1 bit stream can be randomly assigned from any of the switched timeslots.

10.0 H.110 Switches

The H.110 controllers provide switching between one or two ECTF H.110 interfaces and the local resources. The local resources include: the T3/M13 Framers, a multi-channel communication controller within the processor, the T1 Monitor ports, and an inter-switch link used for switching between the two H.110 controllers.

The allocation of timeslots within the single H.110 CPC396 is shown in Figure 2.

Each H.110 controller can support 4096x2432 H.110 bus-to-local-resource timeslots, 2432x2432 local-resource-to-local-resource timeslots, or 2048x2048 H.110-to-H.110 timeslots. This provides enough switching capacity to allow all of the timeslots of the T3 Trunks to be switched between each other or the H.110 buses.

The T1 monitor ports take up 48 switched timeslots each when they are used to full capacity (24 full-duplex DS-0s).

Up to 256 timeslots per H.110 controller can be switched to and from the onboard multi-channel communication controller, integrated within the CPU. The processor is capable of termination and protocol processing on all 256 channels (DS-0s, fractional T1 channels or raw T1 channels) simultaneously. Onboard protocol processing options are provided. Consult your Performance Technologies sales representative for protocol software availability.

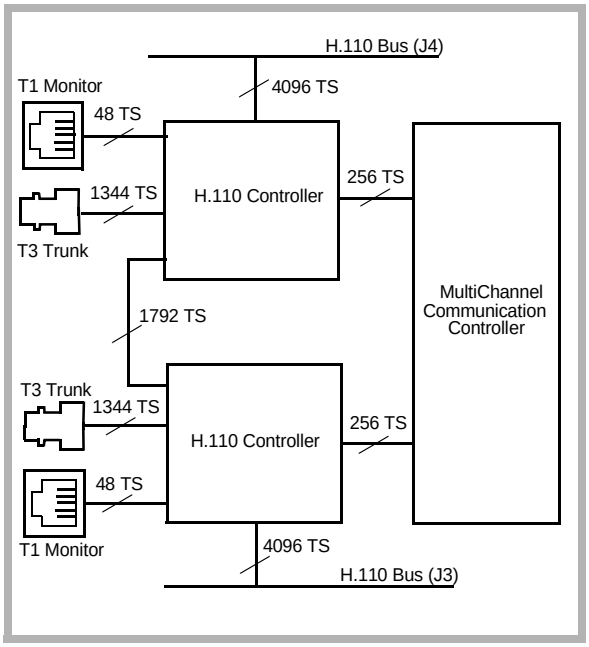

Figure 2. CPC396-11365 Dual H.110 Timeslot Allocation

The allocation of timeslots within the dual H.110 is shown in Figure 3. Note that the single H.110 CTbus is connected to both switches, allowing access to all of the channels attached to the processor and both T3 trunks or T1 Monitor ports.

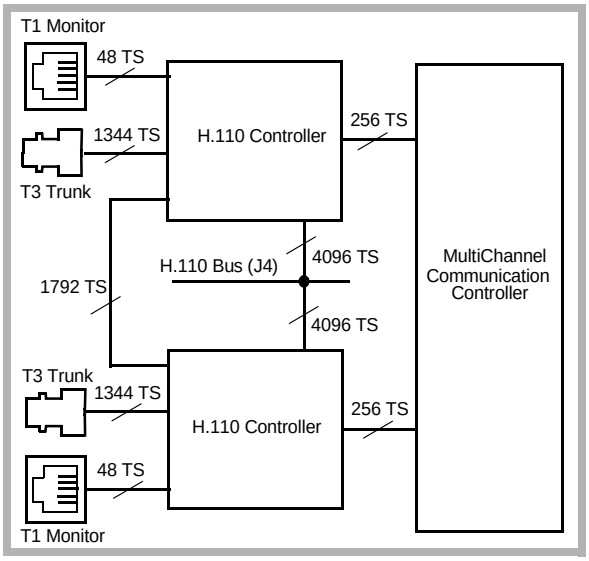

Figure 3. CPC396-11362 Single H.110 Timeslot Allocation

11.0 CompactPCI Interface

The CPC396 supports a fully compliant 33MHz 32/64 bit Compact PCI bus interface for local bus-based management and/or high speed data movement applications.

12.0 Clock Options

Clock synchronization is maintained by digital phase locked loop circuitry, which provides timing and synchronization signals for the T3 interfaces and H.110 controllers.

The CPC396 reference clock can be selected from any one of seven sources: an onboard reference clock, either of the H.110 buses, clock recovered from either of the T3 interfaces, or either of the T1 Monitor ports. The Monitor ports provide a convenient interface to a local BITS (Building Integrated Timing Supply) clock source.

The CPC396 can be configured as an H.110 clock Master or Slave, and supports all clock fallback features defined in the ECTF H.110 specification.

13.0 Ethernet Ports

Two 10Base-T/100Base-Tx Ethernet ports are provided on the CPC396 for management purposes. Two modes of operation are supported: dual independent subnet and dual-homed shared subnet.

In the dual subnet configuration, each port provides access to a separate subnet. In this mode, the CPC396 is configured with two IP addresses and two Ethernet MAC Addresses. The CPC396 can be configured as a gateway in dual subnet mode.

In single-subnet, dual-homing mode, the CPC396 is configured with one IP address and one MAC Address. The CPC396 will use only one of the ports at a time. Port 1 is the primary port and the CPC396 will always use that port if it is available. If port 1 loses link, the CPC396 will automatically switch to port 2 within 500 ms. While the secondary port is in stand-by mode, it will not establish a link with its peer.

The CPC396 Ethernet ports conform to all requirements of the IEEE 802.3 (CSMA/CD) MAC interface. These ports support symmetric flow control using the MAC Control Client interface (Pause) specified in IEEE 802.3u.

13.1 Ethernet PHY

The Ethernet ports conform to the twisted pair PHY specification for 10 Mbps or 100 Mbps operation in Half-Duplex or Full-Duplex mode. Each Ethernet port supports auto-negotiation of the proper speed and duplex settings with its link partner(s).

There are three modes of operation for the Ethernet Interface:

- Single Shared MAC Interface - both PHYs share a common Media Independent Interface (MII) bus generated by the MPC8280's FCC3.
- Dual Independent MAC Interface - the Main PHY is connected to FCC3 and the Backup is connected to FCC1.
- Dual Independent MAC Interface - the Main PHY is connected to FCC3 and the Backup is connected to FCC2 [future implementation].

At the PHY layer, the Ethernet is presented to 4-wire mid-plane interfaces instead of the standard 100Base-TX MDI. At the mid-plane interface, this port conforms to the ethernet signaling and voltage level requirements. Network isolation and the (optional) MDI mechanical interface is provided via a separate rear-panel Line Interface Module (LIM).

If the Management port Ethernet signals are to be embedded into the mid-plane, then it is the integrator's responsibility to provide a mid-plane that simulates the Category-5 cable plant requirements specified in ANSI/EIA/TIA 568 for 100BaseTX.

13.2 Ethernet Status Indicators

A visible display (LED) is provided for each port to indicate Link and Activity (transmit or receive). A second

visible display (LED) is provided for each port to indicate mode (duplex) and speed.

14.0 Supporting Software

14.1 Nexusware (CPC396N)

NexusWare is a comprehensive, highly integrated, Linux-based development, integration, and management environment. It is intended for system engineers using Performance Technologies' IPnexus products (CPC388 T1/E1/J1, CPC396 T3/DS-3) to build packet-based systems including next-generation wireless and IP telephony systems.

The philosophy behind NexusWare is to raise the level at which system integration is performed. In the past, systems depended on the conventional PCI bus for integration, forcing a low-level and time consuming process for developing IP telephony and telecom systems. The Ethernet capabilities of IPnexus hardware products, coupled with the strong Linux OS foundation of NexusWare, gives developers a simplified way to design in current PCI-based systems. It also offers a simple and rapid path to evolving packet-switched-backplane-based systems such as PICMG 2.16 CompactPCI/PSB.

NexusWare features an integrated suite of carrier-grade device drivers for full access to onboard resources (H.110, Ethernet, PCI, T3, T1/E1/J1) as well as a powerful NexusWare API. As a result, the IPnexus products, with NexusWare integrated drivers communicating over TCP/IP, operate within any host system that supports TCP/IP - without the need of bus-based device drivers. The NexusWare API provides a common interface for application development and allows system integration using either the PCI bus or the PICMG 2.16 CompactPCI/PSB architecture.

NexusWare's full Linux OS and development environment includes a pre-ported Linux 2.2.16 kernel, a complete suite of GNU/EGCS cross development tools (CDT), compilers (C, C++), debuggers, profilers, libraries and embedding tools that build software images for the embedded system. A kernel debugger supports development of custom drivers on the target system and utilities are included to make a bootable image in flash memory.

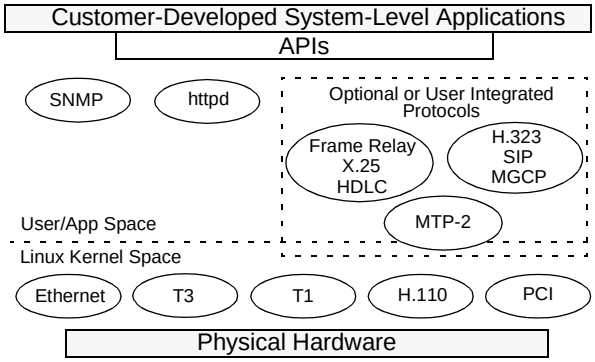

Figure 4. NexusWare Development Platform

14.2 TDM Circuit Switch Software (CPC396C)

An external management entity may be used to control the CPC396C. Management is supported over the CompactPCI bus via a chassis-based host, over Ethernet via a remote host, or locally via the RS-232 serial ports.

Command Line Interface (CLI)--The CPC396C Command Line Interface (CLI) is provided via the RS-232 TTY port or via telnet over the Ethernet ports. The CLI provides:

- An initial configuration interface
- A simple and efficient management user interface
- A command interpreter for scripting
- Access to diagnostic utilities

The detailed command list and user information is provided in the CPC396C User's Manual.

CompactPCI Device Drivers--Local CompactPCI-based hosts may manage the CPC396C through a standardized API Interface. Host-resident applications can access onboard resources on the CPC396C with an API Library provided by Performance Technologies.

Device drivers for Windows NT, Solaris, and Linux are available.

Remote TCP/IP-Based API--The CPC396C supports a remote TCP/IP-based API Interface for Windows NT, Solaris, and Linux. Using this interface API, the user may create a remote application supporting data transfer to the PSTN interface and/or management of the CPC396C hardware. From the application's perspective, the CPC396C is a co-located device supporting a read/write/ioctl API.

SNMP--The CPC396C SNMP agent is an SNMP V1/V2C/V3 implementation. The agent responds to a defined set of SNMP client requests and generates the appropriate SNMP traps to respond to CPC396C events.

All mandatory parameters for the following MIBs are provided

- MIB II (RFC1213)
- DS-1 MIB (RFC2495)
- DS-3 MIB (RFC2496)
- Performance Technologies Enterprise MIB for extended monitoring, configuration, and H.110 circuit setup.

The Performance Technologies Enterprise MIB is used for CPC396-specific parameters that are not supported by the MIBs described above. An ASN.1 document is provided that defines the Performance Technologies Enterprise MIB support, allowing SNMP clients to have complete access to the parameters supported by this MIB.

15.0 Diagnostic Facilities

The diagnostic facilities of the CPC396 support a Power On Confidence test suite (POC), continuous network validation through detection of Alarms and faults, and a set of online utilities that provide for extensive network level diagnostics.

15.1 Power-On Confidence (POC)

Power-On Confidence tests are a diagnostic suite that is run whenever the CPC396 is booted. The user can enable or disable these tests. The POC test suite includes only those diagnostic tests that do not affect externally attached devices. The CPC396 becomes available to the user within 30 seconds of a power-on or reset. All subsystems are included in the POC suite.

15.2 Network Fault Detection

Network Fault Detection supports the automatic detection of and response to network problems. These include detection of loss of H.110 Master Clock and driving the clock fallback state machine, CRC6 Validation, C-bit parity checking, Carrier Loss (RCL), T3 Alarm Indication Signal (AIS-CI), Remote Alarm Indication (RAI), and Loss of Sync detection.

15.3 Online Network Diagnostic Tools

These include a set of utilities that allow for diagnosing network related problems. These utilities allow for creating loopback paths at the T1 and T3 level, per channel code insertion, and presentation of timeslots to external T1 Monitor ports.

16.0 Ethernet Network Client Capabilities

The CPC396 runs an embedded Linux kernel which natively supports an extensive array of network client capabilities. These include:

- BootP
- DHCP
- FTP (Allows secure transfer of configuration files to off board storage)
- TFTP (Allows transfer of configuration files to off board storage)

16.1 BOOTP or DHCP Clients

The CPC396 may acquire its IP Address and configuration file from a network-based server for easy configuration management.

The DHCP Client also supports the acquisition of other network configuration parameters, such as file server address, gateway, etc.

16.2 TFTP/FTP Client

The CPC396 saves its configuration to Flash to allow for restoration on reboot and offers the ability to also save its configuration to an external file system server using the TFTP or FTP File Transfer Protocols.

17.0 Pinouts

17.1 Rear Panel LIM Ethernet

Table 2. RJ45 Ethernet Port Pinout

Pin Number	Signal Name
1	TX+
2	TX-
3	RX+
4	-
5	-
6	RX-
7	-
8	-

17.2 Front Panel Serial Ports

Table 3. RS-232 Port Pinout

Pin Number	Signal Name
1	-
2	GND
3	RX
4	TX
5	GND
6	-

17.3 Rear Panel LIM T1 Monitor Ports

Table 4. RJ48C T1 Port Pinout

Pin Number	Signal Name
1	RX_R
2	RX_T
3	-
4	TX_R
5	TX_T
6	-
7	-
8	-

The following tables outline the CPC396 CompactPCI midplane pinout.

17.4 CompactPCI P1/J1.

Table 5. CompactPCI Bus P1/J1 Connector

Row #	A	B	C	D	E
25	5V	REQ64#	ENUM#	3.3V	5V
24	AD[1]	5V	V(I/O) (2),(6)	AD[0]	ACK64#
23	3.3V	AD[4]	AD[3]	5V (6)	AD[2]
22	AD[7]	GND	3.3V (6)	AD[6]	AD[5]
21	3.3V	AD[9]	AD[8]	M66EN (5)	C/BE[0]#
20	AD[12]	GND	V(I/O) (2)	AD[11]	AD[10]
19	3.3V	AD[15]	AD[14]	GND (6)	AD[13]
18	SERR#	GND	3.3V	PAR	C/BE[1]#
17	3.3V	IPMB SCL	IPMB SDA	GND (6)	PERR#
16	DEVSEL#	GND	V(I/O) (2)	STOP#	LOCK#
15	3.3V	FRAME#	IRDY#	BD SEL# (7)	TRDY#
12-14	Key Area				
11	AD[18]	AD[17]	AD[16]	GND (6)	C/BE[2]#
10	AD[21]	GND	3.3V	AD[20]	AD[19]
9	C/BE[3]#	IDSEL (7)	AD[23]	GND (6)	AD[22]
8	AD[26]	GND	V(I/O) (2)	AD[25]	AD[24]
7	AD[30]	AD[29]	AD[28]	GND (6)	AD[27]
6	REQ#	GND	3.3V (6)	CLK	AD[31]
5	BRSVP1A5	BRSVP1B5	RST#	GND (6)	GNT#
4	IPMBPWR	HEALTHY# (18)	V(I/O) (2),(6)	INTP	INTS
3	INTA#	INTB#	INTC#	5V (6)	INTD#
2	TCK (15)	5V	TMS (15)	TDO (15)	TDI (15)
1	5V	-12V	TRST# (15)	+12V	5V

Key to J1 Pin Assignments:

- Refer to CompactPCI Specification.

17.5 CompactPCI P2/J2

Table 6. CompactPCI Bus P2/J2 Connector

Row #	A	B	C	D	E
22	GA4 (13)	GA3 (13)	GA2 (13)	GA1 (13)	GA0 (13)
21	RSV	RSV	RSV	RSV	RSV
20	RSV	RSV	RSV	GND	RSV
19	RSV	RSV	RSV	RSV	RSV
18	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18
17	BRSVP2A17	GND	RSV	RSV	RSV
16	BRSVP2A16	BRSVP2B16	RSV	GND	BRSVP2E16
15	BRSVP2A15	GND	RSV	RSV	RSV
14	AD[35]	AD[34]	AD[33]	GND	AD[32]
13	AD[38]	GND	V(I/O) (2)	AD[37]	AD[36]
12	AD[42]	AD[41]	AD[40]	GND	AD[39]
11	AD[45]	GND	V(I/O) (2)	AD[44]	AD[43]
10	AD[49]	AD[48]	AD[47]	GND	AD[46]
9	AD[52]	GND	V(I/O) (2)	AD[51]	AD[50]
8	AD[56]	AD[55]	AD[54]	GND	AD[53]
7	AD[59]	GND	V(I/O) (2)	AD[58]	AD[57]
6	AD[63]	AD[62]	AD[61]	GND	AD[60]
5	C/BE[5]#	GND	V(I/O) (2)	C/BE[4]#	PAR64
4	V(I/O) (2)	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#
3 (3)	RSV	GND	RSV	RSV	RSV
2 (3)	RSV	RSV	UNC (4)	RSV	RSV
1 (3)	RSV	GND	RSV	RSV	RSV

Key to J2 Pin Assignments:

- Refer to CompactPCI Specification.

17.6 CompactPCI P3/J3

Table 7. CompactPCI Bus P3/J3 Connector

Row #	A	B	C	D	E
19	Ground	Ground	Ground	Ground	Ground
18	LPa_DA+	LPa_DA-	Ground	RSVDGBE	RSVDGBE
17	LPa_DB+	LPa_DB-	Ground	RSVDGBE	RSVDGBE
16	LPb_DA+	LPb_DA-	Ground	RSVDGBE	RSVDGBE
15	LPb_DB+	LPb_DB-	Ground	RSVDGBE	RSVDGBE
14	Ground	Ground	Ground	Ground	Ground
13	B_CTD27	B_CTD28	B_CTD29	B_CTD30	B_CTD31
12	B_CTD22	B_CTD23	B_CTD24	B_CTD25	B_CTD26
11	B_CTD18	B_CTD19	V3V	B_CTD20	B_CTD21
10	V3V	B_CTD15	B_CTD16	B_CTD17	VDD
9	B_CTD10	B_CTD11	B_CTD12	B_CTD13	B_CTD14
8	B_CTD7	Ground	B_CTD8	Ground	B_CTD9
7	B_CTD3	B_CTD4	B_CTD5	B_CTD6	VDD
6	B_CTD0	B_CTD1	B_CTD2	B_CT_MC	B_CTNR2
5	Ground	LINKA#	B_CT_RESET#	LINKB#	B_CTNR1
4	B_CT8A	B_CT8B	VIO	B_CTRFMA#	B_CTRFMB#
3	Ground	Ground	VIO	Ground	Ground
2	TDA+	TDA-	Ground	TDB+	TDB-
1	RDA+	RDA-	Ground	RDB+	RDB-

Key to J3 Pin Assignments:

H.110 Signals--These signals are a subset of the standard H.110 signals. They are available on the CPC396 only.

- **B_CT_FRAME_A** Frame sync A, 125 usec period
- **B_CT_FRAME _B** Frame sync B, 125 usec period
- **B_CT_C8_A** Bit clock A, 8.192 MHz
- **B_CT_C8_B** Bit clock B, 8.192 MHz
- **B_CT_D[0:31]** Serial data lines, 128 time slots each
- **B_CT_NETREF_1** Network timing reference 1
- **B_CT_NETREF_2** Network timing reference 2
- **B_CT_RESET** Logic low card reset
- **B_CT_MC** Optional message channel bit serial bus

Bused Ethernet Signals--For applications that embed the Ethernet signals into the mid-plane, these are the signals that should be used. They meet the IEEE 802.3u specification for 100Base-Tx Ethernet, including transformer isolation.

- **BUS_TXA+/-** Transmit mid-plane bused Ethernet PHY 1
- **BUS_RXA+/-** Receive mid-plane bused Ethernet PHY 1
- **BUS_TXB+/-** Transmit mid-plane bused Ethernet PHY 2
- **BUS_RXB+/-** Receive mid-plane bused Ethernet PHY 2

Ethernet PHY Signals--These Ethernet signals are data lines from the main controller card to the transition card only. They are used to connect the PHYs to the Ethernet line transformers and are not bused across the mid-plane.

- **RDA+/-** Main card receive PHY 1 to rear transition card line transformer
- **TXA+/-** Main card transmit PHY 1 to rear transition card line transformer
- **RDB+/-** Main card receive PHY 2 to rear transition card line transformer
- **TXA+/-** Main card transmit PHY 2 to rear transition card line transformer

17.7 CompactPCI P4/J4

Table 8. CompactPCI Bus P4/J4 Connector

Row #	A	B	C	D	E
25	SGA4	SGA3	SGA2	SGA1	SGA0
24	GA4	GA3	GA2	GA1	GA0
23	IN/C	/CT_Reset	/CT_EN	IN/C	CT_MC
22	PFS0#	RSVD	RSVD	RSVD	RSVD
21	IN/C	PFS1#	RSVD	RSVD	IN/C
20	NP	NP	NP	NP	NP
19	NP	NP	NP	NP	NP
18	IN/C	IN/C	IN/C	IN/C	IN/C
17	NP	NP	NP	NP	NP
16	NP	NP	NP	NP	NP
15	IN/C	IN/C	IN/C	IN/C	IN/C
14-12	Key Area				
11	CT_D29	CT_D30	CT_D31	V(I/O)	/CT_FRAME_A
10	CT_D27	+3.3V	CT_D28	+5V	/CT_FRAME_B
9	CT_D24	CT_D25	CT_D26	GND	/FR_COMP
8	CT_D21	CT_D22	CT_D23	+5V	CT_C8_A
7	CT_D19	+5V	CT_D20	GND	CT_C8_B
6	CT_D16	CT_D17	CT_D18	GND	CT_NETREF_1
5	CT_D13	CT_D14	CT_D15	+3.3V	CT_NETREF_2
4	CT_D11	+5V	CT_D12	+3.3V	SCLK
3	CT_D8	CT_D9	CT_D10	GND	SCLK-D
2	CT_D4	CT_D5	CT_D6	CT_D7	GND
1	CT_D0	+3.3V	CT_D1	CT_D2	CT_D3

Key to J4 Pin Assignments:

- •RSVD = reserved for future use
- •NP = a position required to be not populated with pin and pad (i.e. no conductive element present)
- •IN/C = pin and pad with no connect required for safety agency insulation requirements
- •KEY AREA = reserved area utilized for keying.
- •**CT_FRAME_A** Frame sync A, 125 usec period
- •**CT_FRAME _B** Frame sync B, 125 usec period
- •**CT_C8_A** Bit clock A, 8.192 MHz
- •**CT_C8_B** Bit clock B, 8.192 MHz
- •**CT_D[0:31]** Serial data lines, 128 time slots each
- •**CT_NETREF_1** Network timing reference 1
- •**CT_NETREF_2** Network timing reference 2
- •**CT_EN** Logic low signal to indicate CT Bus card is seated
- •**CT_RESET** Logic low card reset

17.8 CompactPCI P5/J5

Table 9. CompactPCI Bus P5/J5 Connector

Row #	A	B	C	D	E
22	Tx1_T	IN/C	Tx2_T	IN/C	IN/C
21	Tx1_R	IN/C	Tx2_R	IN/C	IN/C
20	Rx1_T	IN/C	Rx2_T	IN/C	IN/C
19	Rx1_R	IN/C	Rx2_R	IN/C	IN/C
18	IN/C	IN/C	IN/C	IN/C	IN/C
17	IN/C	IN/C	IN/C	IN/C	IN/C
16	IN/C	IN/C	IN/C	IN/C	IN/C
15	IN/C	IN/C	IN/C	IN/C	IN/C
14	IN/C	IN/C	MTx1_T	IN/C	IN/C
13	IN/C	IN/C	MTx1_R	IN/C	IN/C
12	IN/C	IN/C	MRx1_T	IN/C	IN/C
11	IN/C	IN/C	MRx1_R	IN/C	IN/C
10	IN/C	IN/C	MTx2_T	IN/C	IN/C
9	IN/C	IN/C	MTx2_R	IN/C	IN/C
8	IN/C	IN/C	MRx2_T	IN/C	IN/C
7	IN/C	IN/C	MRx2_R	IN/C	IN/C
6	IN/C	IN/C	IN/C	IN/C	IN/C
5	IN/C	IN/C	IN/C	IN/C	IN/C
4	IN/C	IN/C	IN/C	IN/C	IN/C
3	IN/C	IN/C	IN/C	IN/C	IN/C
2	IN/C	IN/C	IN/C	IN/C	IN/C
1	IN/C	IN/C	IN/C	IN/C	IN/C

Key to J5 Pin Assignments:

- **Tx1_T/R** T3 Channel A Transmit Tip and Ring
- **Rx1_T/R** T3 Channel A Receive Tip and Ring
- **Tx2_T/R** T3 Channel B Transmit Tip and Ring
- **Rx2_T/R** T3 Channel B Receive Tip and Ring
- **MTx1_T/R** T1 Monitor A Transmit Tip and Ring
- **MRx1_T/R** T1 Monitor A Receive Tip and Ring
- **MTx2_T/R** T1 Monitor B Transmit Tip and Ring
- **MRx2_T/R** T1 Monitor B Receive Tip and Ring
- **NP** a position required to be not populated with pin and pad (i.e. no conductive element present)
- **IN/C** pin and pad with no connect required for safety agency insulation requirements.