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USER'S MANUAL

PT-VME940

High Performance
Data Network Adapter

Performance Technologies, Incorporated

315 Science Parkway Rochester, New York USA 14620

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REVISION CONTROL

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Section

1

INTRODUCTION

Scope

This document provides information for users of the Model PT-VME940 High Performance Data Network Adapter.

This manual is not intended as a stand-alone document. If you plan on writing firmware for the board the references cited below in the Applicable Documents section are necessary.

This manual does provide the information necessary to understand the operation and features of the board. A prime objective was to answer those questions raised by system developers as to whether the PT-VME940 will complement their architecture. When combined with the supporting documentation listed below, a complete description of PT-VME940 facilities are presented

Section 1 provides an introduction and general overview of the PT-VME940. It is intended as a quick summary of PT-VME940 features and provides a framework for the rest of the document.

Section 2 (Getting Started) describes the physical setup and installation procedures.

Section 3 the Functional Description provides a detailed description of PT-VME940 architecture and functional blocks.

Section 4 summarizes the PT-VME940 memory map, registers, controls, indicators, etc.

Section 5 (Jumper Descriptions) provides detailed descriptions of each jumper selectable options and their operation.

Section 6 (Connector Pinouts) summarizes the PT-VME940 external connections.

Section 7 describes mechanical and environmental characteristics of the PT-VME940.

Section 8 appendices.

Section 9 Index.

Section 10 Schematics.

Applicable Documents

a. VMEbus Specification Manual, Revision ANSI/IEEE STD 1014-1987, VMEbus International Trade Association (VITA). VITA; 10299 N. Scottsdale Road, Suite B; Scottsdale, AZ 82523.

b. M68000 Family Programmer's Reference Manual; M6800PM/AD; Motorola Incorporated, 1989. Motorola Literature Distribution; P.O. Box 20912; Phoenix, AZ 85036.

c. MC68020 32-Bit Microprocessor User's Manual; MC68020UM/AD; Motorola Incorporated, 1990. Motorola Literature Distribution; P.O. Box 20912; Phoenix, AZ 85036.

d. MC68901 Multi-Function Peripheral Specification (MFP); September, 1985. Motorola Semiconductor Products Incorporated; 3501 Ed Bluestein Boulevard; Austin, TX 78721.

Model Designations

The PT-VME940 is available with or without terminations. Both ends of a cable must be terminated with PT-VME940-T's. Additionall, the PT-VME940-U's can be added to the network. Model designations are as follows:

Model PT-VME940-T	Terminators Installed
Model PT-VME940-U	No Terminators Installed

The optional interconnection model designations are as follows:

Model PT-ACC940-A	50' Unshielded Evaluation Cable Set
Model PT-ACC940-B	Unshielded Mass Terminated Connector (each)
Model PT-ACC940-C	Unshielded Twist/Flat Cable (foot)

Features

- High Performance Network Adapter.
  - 32 Bit 68020 CPU @ 12.5 Mhz.
  - 128K zero-wait-state instruction store.
  - High performance FIFO-based VMEbus Master interface with VME64 capability. A24/A32:D08/D16/D32/D32BLT/D64BLT. VMEbus transfer rates up to 60 Mbytes/second.
  - VMEbus Slave interface implemented using the PTI-VSI ASIC Slave interface. A16/A24/A32:D08(O).
  - Fully programmable VMEbus interrupter.
  - All VMEbus and Adapter parameters (such as VMEbus Request Level) may be software controlled and stored in EEPROM.
- High Performance Data Network.
  - Network media consists of dual 50-conductor twisted-pair cables and differential drivers/receivers. Includes hardware fault tolerance.
  - Up to 16 adapters may be connected to one network.
  - Maximum total cable length of 100 feet (35 meters).
  - Cable transfer rates up to 40 Mbytes/second.
  - Flexible cabling options.
  - Hardware watchdog timer to remove a node from the network in case of a catastrophic failure.
  - Live insertion and removal.
  - Distributed arbitration.
- Network Application Firmware.
  - Master-Slave mode which allows the initiating node to read or write the memory of a target node without the consent or participation of the target node's host.
  - Peer-Peer mode which allows the initiating node to read or write the target node only when the target node's host has approved the transfer.
  - Multi-Threading of commands.
  - Chaining of commands.
  - Diagnostic port with protocol trace.

Family Members

The PT-VME940 a member of a family of PTI VME*64* products. Each represents a highly integrated VMEbus component designed to offer the user significant flexibility in meeting specific architectural requirements.

The base modules support all standard VMEbus data and operating modes including the newly defined VME*64* mode pioneered by Performance Technologies. Operating in VME*64* mode the PT-VME940 can burst data over the VMEbus at rates up to 60 MBytes per second. This high speed transfer capability makes the 141 ideal for applications that require maximum VMEbus utilization. The base modules provide many I/O features tightly coupled to the MPU. These features include four DRAM capacities from one to eight megabytes, two SRAM capacities of 256K or 1 megabyte, a Fast SCSI-2 interface with DMA support for direct flexible/hard disk interconnect, and dual serial I/O ports for asynchronous communication connectivity.

In addition to the standard base module features, the PTI specs provide an option for even further extending their single VMEbus slot functionality through its “EPAK” extension interface. This interface provides for the addition of a plug-in daughterboard (EPAK) with selectable functionality to meet current or future I/O needs. Performance Technologies offers “off-the-shelf” EPAKs which support Ethernet, high speed synchronous communications, additional asynchronous serial I/O, etc. If these EPAKs do not match the requirements, the user also has the option for a custom design based upon an available wire wrap prototyping EPAK and supplied interface documentation. Contact Performance Technologies for custom EPAK design quotations.

A key design criterion was to maintain user software compatibility across the family members. The command and register set of the EMULEX SCSI controller on the PT-VME141 and PT-VME151 is a super set of the PT-VME131s NCR SCSI controller. The MC68040 of the PT-VME151 is user code compatible with the MC68030 of the PT-VME131 and PT-VME141. These and other design considerations were made to preserve your investment in code development.

PT-VME141/141E

The PT-VME141 and PT-VME141E were designed as the VME*64* entry level members of the PTI Single Board Computer/Controller family. Their features are described in this manual and summarized in the previous section.

These boards make the step into the newly defined VME*64*™ mode pioneered by Performance Technologies. Operating in VME*64* mode the PT-VME141 can burst data over the VMEbus at rates up to 60 MBytes per second. This high speed transfer capability makes the 141 ideal for application that require maximum VMEbus utilization.

- Advanced Thirty-Two Bit Microprocessor With Internal Cache
  PT-VME141 utilizes 25 MHz 68030 MPU w/Memory Management Unit
  PT-VME141E utilizes 25 MHz 68EC030 MPU w/o Memory Management Unit

- 1, 2, 4, or 8 Megabytes of Shared DRAM
  5 Clock Local Access
  68030 Cache Burst Read Mode (5-2-2-2 Clock Timing)

- 256 Kbytes or 1 Mbyte Of Optional SRAM
  3 Clock Local Access
  68030 Cache Burst Read Mode (3-1-1-1 Clock Timing)

- Two 32 Pin JEDEC Sockets (Bytewide Port)
  - Both sockets support ROM, PROM, EPROM, and Flash EPROM devices
  - One socket is additionally capable of supporting SRAM and RTC devices
- Fast SCSI-2 Single Ended Interface Based Upon EMULEX FAS216
  - Supports ANSI X3.131-1986 and X3T9.2/86-109 Rev. 10c Standards
  - 10 MByte per second SCSI Data Transfer Rate
  - Active SCSI bus termination
  - DMA Support To Local DRAM
  - P2 SCSI Interconnect
- General Purpose Local I/O
  - 68681 DUART
    - Dual RS-232 ASYNC Serial I/O ports w/Front Panel Interconnect
    - 16-bit General Purpose Timer
  - 128 Byte EEPROM
- Flexible EPAK Interface Extension Capability
  - Supports Slave, DMA, and Buffered DMA I/O Functions
  - Options for Ethernet, High Speed SYNC SIO, High Density ASYNC SIO, etc.
  - Front Panel Interconnect
- VME*64*™ VMEbus Interface Features
  - Advanced Control Circuit (ACC) ASIC
    - Full VMEbus System Controller w/Auto-Program Option
    - VMEbus Requester, Interrupter, and Interrupt Handler
    - Tick and Watchdog Timers, General Purpose Clocks
  - Data/Address Register File (DARF64) ASIC
    - 60 MByte per second D64MBLT (VME64) Data Transfer Rate
    - VMEbus A64/A32/A24/A16 Address Interface
    - VMEbus D64MBLT/D32BLT/D16BLT/D32/D16/D8(EO), UAT, RMW Data Interface
    - Location Monitor w/Message FIFO
    - Programmable Slave Address Mapping And Protection
    - Integral A32:D32 Local DMA Controller w/Burst Capabilities
    - Programmable Burst Sizes on Local Bus DMA Operations
- Front Panel User Interface Features
  - Reset and Abort Switches
  - General Purpose Hexadecimal Switch
  - 68030 (RUN) and VMEbus (VME) Activity LED indicators
  - User Programmable FAULT LED
  - Four User Programmable LEDs
- Software Support
  - PTbug Debugger/Monitor
  - OS-9 Real-Time Operating System

PT-VME151/151E

The features of the PT-VME151 and PT-VME151E are identical to the PT-VME141 with the following exceptions:

As the top performers in the family the PT-VME151 and PT-VME151E utilize the Motorola MC68040 and MC68EC040, respectively. The MC68040 is Motorola's third generation of M68000-compatible,

high performance, 32-bit microprocessors that offers approximately twice the processing power of the MC68030 running at the same clock rate.

- MC68040 Thirty-Two Bit Microprocessor With Internal Cache and FPU
  - PT-VME151 utilizes 25 MHz MC68040 MPU w/Memory Management Unit
  - PT-VME151E utilizes 25 MHz MC68EC040 MPU w/o Memory Management Unit
  - MC68030-Compatible Integer Execution Unit
  - MC68881/MC68882-Compatible Floating Point Unit
  - Independent Instruction and Data Memory Management Units
  - 4KByte Physical Instruction Cache and 4KByte Physical Data Cache Accessible Simultaneously
  - Low Latency Bus Accesses for Reduced Cache-Miss Penalty
  - Concurrent integer unit, FPU, MMU, and Bus Controller Operation Maximizes Throughput
  - User Object-Code Compatibility with all Earlier M68000 Microprocessors

The PT-VME151 series integrates onto the card the Dallas Semiconductor DS1643 Nonvolatile Time-keeping RAM to provide the user with nonvolatile SRAM and Real Time Clock functionality.

- DS1643 Nonvolatile Timekeeping RAM
  - 8184 Bytes of Nonvolatile SRAM
  - Real Time Clock with Integrated Crystal
  - Power fail Control Circuit
  - Lithium Energy Source

PT-VME240

The PT-VME240 is a high performance VME*64* Memory board.

- 101 MByte/sec WRITE Transfer Capability (D64MBLT)
- 50.5 MByte/sec WRITE Transfer Capability (D32BLT)
- VME C.1+ Compatible (Meets Proposed VME D.1 Spec)
- 4, 8, 16, 32 MByte Capacities
- Supports A24/A32:D08(EO)/D16/D32/D32BLT/D64MBLT (VME*64*)/UAT/RMW
- Byte Wide Parity Protection
- Switch Selectable Upper/Lower Address Boundaries
- Queued Refresh to Maximize Uninterrupted BLT
- Automatic Memory and Parity Initialization
- Built In Unique Hardware Register Diagnostic Facility
- 16 Bit Command/Status Register

Glossary and Conventions

Glossary

CPU - Central Processing Unit (MC68020)

DMA - Direct Memory Access, hardware controller block data transfers.

DMAC - Direct Memory Access Controller.

longword - In this manual, this term indicates a 32-bit value.

MByte - Mega Byte.

ms. - Millisecond.

reserved - The term used for bits, bytes, fields, code values, etc. that are set aside for future use.

SRAM - Static Random Access Memory.

word - In this manual, this term indicates a 16-bit value.

xxh - Numbers followed by lowercase h are hexadecimal values. All other numbers are decimal values.

Conventions

Upper case names enclosed in square brackets ([,]) represent signal names that can be found in the schematics.

Numbers enclosed in “less than” (<) and “greater than” (>) symbols refer to individual bits of a signal bus. i.e. +MPA<0> represents a the least significant bit of the 32 bit MicroProcessor Address bus. +MPA<0:31> represents all signals associated with the MicroProcessor Address bus.

Device pins are referenced with a Reference Designator, hyphen, pin number. i.e. U52-30 indicates pin 30 of location U52.

A Jumper Block can contain one or many individual Jumpers. If a Jumper Block contains of more than two pins then the individual Jumpers consist of three pin groups starting with pin 1. i.e. Jumper 1 is comprised of pins 1 through 3, Jumper 2 is comprised of pins 4 through 6, etc. The individual Jumpers in a Jumper Block are referenced with the Jumper Block Reference Designator, underscore, and Jumper number. i.e. K6_2 indicates jumper 2 of Jumper block K6. The individual pins in a Jumper Block (or Jumper) are referenced with a Reference Designator, hyphen, pin number. i.e. K7-30 indicates pin 30 of Jumper Block K7 (or Jumper K7_10).

VMEbus signal pins are referenced with the Connector Designator, hyphen, Row Designator, Pin number. i.e. P2-B3 refers to Pin 3 of Row B on the VMEbus “P2” connector.

Section

2

GETTING STARTED

Unpacking and Inspection

CAUTION: ELECTRONIC COMPONENTS ON MODERN PRINTED CIRCUIT BOARDS ARE EXTREMELY SENSITIVE TO STATIC ELECTRICITY. ORDINARY AMOUNTS OF STATIC ELECTRICITY GENERATED BY YOUR CLOTHING OR WORK ENVIRONMENT CAN DAMAGE THE ELECTRONIC EQUIPMENT. IT IS RECOMMENDED THAT WHEN INSTALLING THE PT-VME940 IN A SYSTEM OR THE COMPONENTS ON THE BOARD ITSELF THAT ANTI-STATIC GROUNDING STRAPS AND ANTI-STATIC MATS ARE USED TO HELP PREVENT DAMAGE DUE TO ELECTROSTATIC DISCHARGE.

The shipping carton should be inspected for any possible damage that may have occurred during shipment. If there is any physical damage to the package you have opened, immediately contact the Shipping Carrier and/or Performance Technologies, Incorporated.

If this shipment is being received outside the United States or Canada and there is damage to the package, contact your local distributor or agent.

If there is shipping damage, failure to make an immediate claim may void any insurance coverage.

If no external damage is visible, carefully unpack contents from shipping carton, observing anti-static precautions identified above and verify against packing list. Inspect the PT-VME940 for any visible signs of shipping damage. If such physical damage is noted, report it immediately to Performance Technologies or appropriate agent. DO NOT PROCEED with any further configuration or installation.

NOTE: If any damage is detected follow the Product Return Procedure described in the appendix.

If no damage is visible, check that all socketed parts are firmly seated. Occasionally parts work themselves loose or partially out of their sockets during the shipping process. Reseat any loose devices by placing the printed circuit board on a flat surface and pressing firmly down on the part. If a part has worked itself completely free of the board (a highly unlikely event) be sure to verify its position and orientation before reinsertion. Check that all mounting screws of attached assemblies are tight.

The serial number can be found stamped on the solder side of the PCB along the edge closest to the front panel. A printed label identifying the assembly revision level can be found on the component side of the “P1” connector. See “PT-VME940 Device Positions” on page 10.

Hardware Configuration

A layout for the PT-VME940 is shown in “Figure 1: PT-VME940 Device Positions”. The model PT-VME940 and PT-VME940E are two versions of the same PCB with different component options. There are various jumpers to configure user options which must be set before initial bootup. Refer to the information in this section to verify that you have the correct settings.

Device Positions

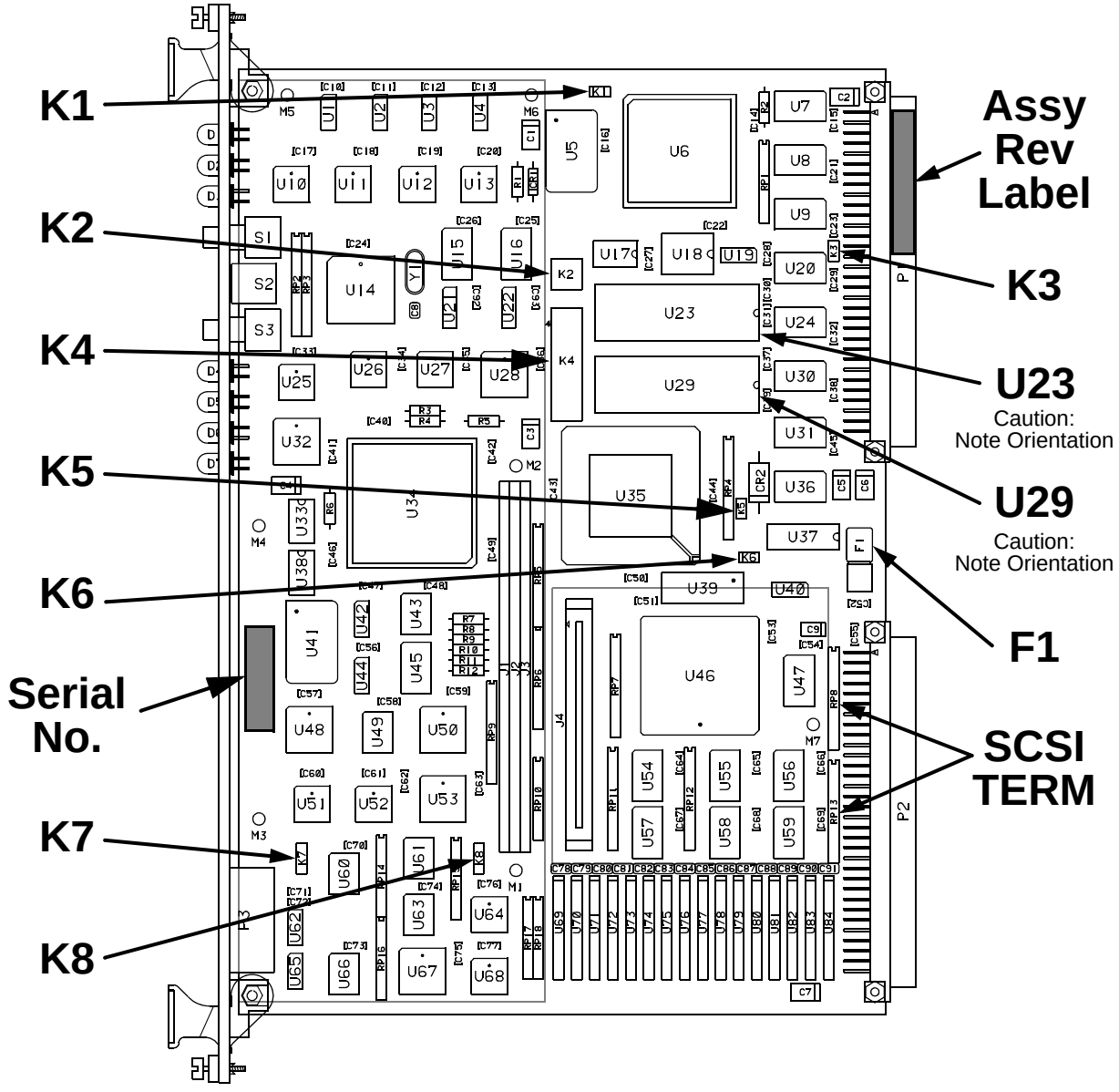
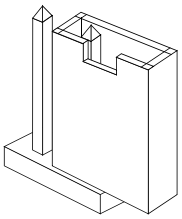


Figure 1: PT-VME940 Device Positions



All Jumper Blocks are designed to mate with standard 2 pin jumper shunts. Spare jumper shunts can be stored by slipping one side of the jumper shunt on a single, unused pin of a jumper block and allowing the other side of the jumper shunt to hang in space. As shown at left:

There are two methods of configuring the PT-VME940. The simpler method uses two rotary switches to set the network node address and select the VMEbus characteristics from one of 15 preset alternatives. The other, more flexible, method uses default parameters stored in EEPROM in conjunction with host commands to establish the characteristics of the module.

Switch Configuration

Switch S2 is used to enable/disable switch configuration and to select one of 15 preset VMEbus configurations. Switch S1 is used to select the network node address. Note that whenever Switch S2 is set to any non-zero value, switch configuration is enabled and the host command to set parameters will not operate.

Switch Setting VMEbus Configuration

Switch S2 is used to enable switch configuration and to select one of 15 preset VMEbus configurations. Switch S2, when set to zero (0), instructs the firmware to obtain the VMEbus configuration setting from EEPROM. Any other position will use one of the following preset values:

Table 1: VMEbus Switch Settings

Switch Position	Slave Address Modifier	Slave Address	Default Transfer Mode	VMEbus Request Level
Fh	2Dh	00001000h	04	03
Eh	2Dh	00002000h	04	03
Dh	2Dh	00004000h	04	03
Ch	3Dh	00064000h	04	03
Bh	3Dh	000C8000h	04	03
Ah	3Dh	00190000h	04	03
9	3Dh	00320000h	04	03
8	3Dh	00640000h	04	03
7	3Dh	00C80000h	04	03
6	0Dh	00C80000h	04	03
5	0Dh	01900000h	04	03
4	0Dh	03200000h	04	03
3	0Dh	06400000h	04	03
2	0Dh	0C800000h	04	03
1	0Dh	19000000h	04	03
0	Use EEPROM Configuration			

Switch Setting Network Node Address

Switch S1 is used to set the network Node Address.

EEPROM/Firmware Configuration

When Switch S2 is set to zero, the configuration of the PT-VME940 is set by the internal firmware based on parameters stored in the EEPROM. The EEPROM parameters, and thus the configuration, can be set by connecting a terminal to the PT-VME940's Debug Port and using an interactive menu and/or they may be changed using host command operations.

In addition to more flexible VMEbus configurations, EPROM/firmware configuration allows the software driver to specify the network node address of the PT-VME940 with the node remaining inactive on the network until that address is specified.

EEPROM Factory Configuration

The EEPROM on the PT-VME940 is shipped with the following default configuration. This configuration would be the one used if switch S2 is set to zero (0) and no interactive or software changes to the EEPROM were made:

Table 2: EEPROM Factory Configuration

Description	Default	Valid Range
VMEbus Request Level	03	00-03
Default Data Transfer Mode*	04	00-0F
Slave Access Address	0C80000	00000000-FFFFFE00
Slave Access Address Modifier	0D	00-3F
Enable Slave A.M. Don't Care Bits	00	00-0F
Node I.D. Location Flag	00	00-02
- 00 = Hardware Switch 1		
- 01 = EEPROM		
- 02 = Set By Driver		
Node I.D. Number	00	0-15
Trace Buffer Size (K Bytes)	01	0-32
Fairness Algorithm Flag	01	00-01
- 00 = priority		
- 01 = round robin		
LAN Maximum Retry Count	03	0-255

* - see section 3.6.1.10 for specific codes.

Changing the EEPROM Parameters from the Debug Port

Connect a standard asynchronous ASCII terminal to the RS-232 Debug Port connector on the front panel of the PT-VME940 (See Section 4 for connector details and terminal setup information).

Initiate a VMEbus Reset. Depress the terminal <CR>. Note that configuration options can only be examined/changed through the Debug Port after a VMEbus Reset and before the first Host command is issued to the PT-VME940.

The Set Configuration Mode will display the current status of each configuration option and ask if any changes are to be made. Depressing <CR> leaves the current status unchanged. Entering a <?> will display the available options.

Terminator Power

Power supplied to the terminators, on either end of the network cable, can be supplied from the network cable or from the host cardcage. This is determined from jumpers K2 and K3 on the PT-VME940 Mezzanine Board.

JUMPER	
K2 1-2	Host Terminator Power
K3 1-2	Host Terminator Power
K2 2-3	Terminator Power From Cable
K3 2-3	Terminator Power From Cable

Board Installation

Power Considerations

The PT-VME940 typically draws 600 ma. of +12V and -12V, and 3.7 Amps of +5V, these figures must be added to those of any attached EPAK (or EBOARD) to determine the total power requirements. It is recommended that Maximum values are used to ensure adequate margins. Add these numbers to those of the other devices in the system and check that the incorporation of the PT-VME940 (and EPAK) does not exceed the system power supply ratings.

NOTE: On the PT-VME940 both 12V supplies are used by the RS-232 drivers attached to the DUART. +12V can also be used by EPROMS that require a VPP = 12V.

Slot Considerations

If you plan on using the System Controller functions of the PT-VME940 then it must be plugged into the Slot 1 position of the VME backplane. The System Controller functions to be automatically enabled after reset if the Slot 1 [BG3IN*] signal is open (or grounded).

For applications that do not require system controller functions the PT-VME940 will can reside in any other VMEbus Slot. There are two considerations that must be made when not using the PT-VME940 in Slot 1, any jumpers on the backplane for the Bus Grant and Interrupt Priority chains must be removed, and the choice of slot location can effect the system level performance of the board.

Relative to other devices at the same Bus Grant and Interrupt Priority levels, the priority of a board goes down as it moves away from Slot 1. Typically, slot position only becomes an issue when there are extremely high levels of bus activity. The slot position, bus grant and interrupt priority levels should be reviewed from a system perspective whenever a new board is configured into a system.

Backplane Insertion

CAUTION: The chassis must be switched off before inserting the board or making any cable connections to avoid damage to the components!

After reviewing the Power Considerations and selecting a slot, insert the PT-VME940 into the backplane. Be sure that it is seated completely into the backplane then tighten the two Captive Chassis Mounting Screws on the front panel. See “Figure 3: Example Serial port Cable” on page 17. Attach cables as necessary then power up the system.

NOTE: The first time the system is powered up after inserting the card, check the supply voltages at the PT-VME940 backplane P1 and P2 connectors. Adjust the supplies as necessary to the nominal voltage levels (+12.00V, - 12.00V and +5.00V).

Network Cable Installation

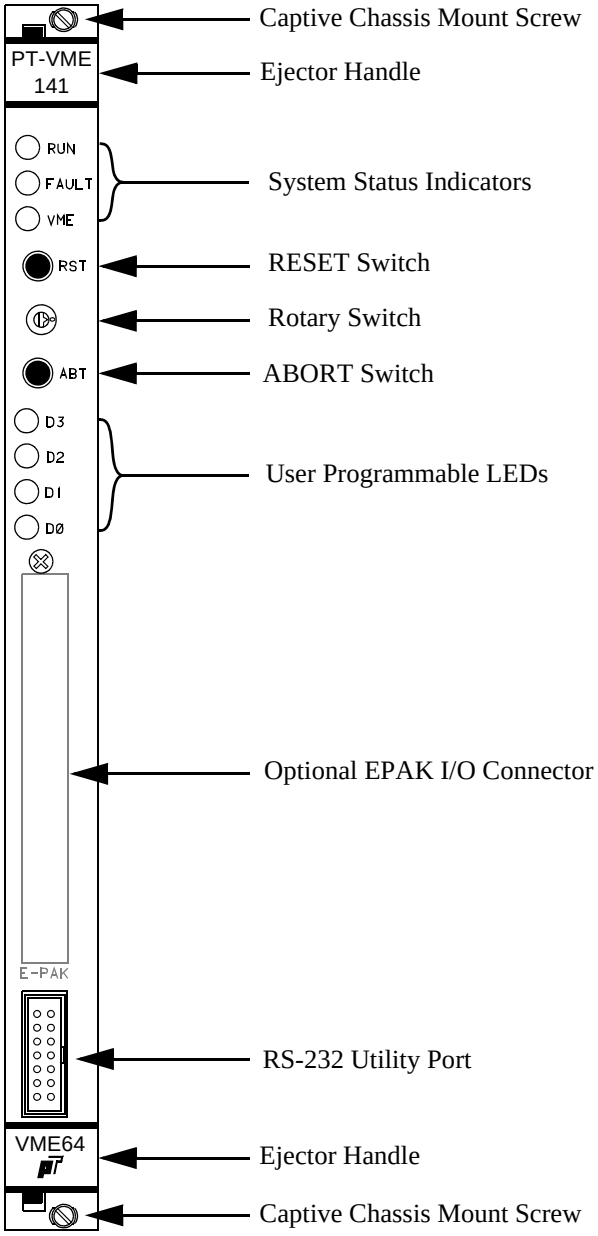
The PT-VME940 network must be terminated at both ends. To accomplish this, model PT-VME940-T modules must be used at either end of the cable. Model PT-VME940-T modules have the option of using power for the terminators either from the host cardcage or the network cable. Power must always be supplied to the terminators when the network is in operation. If either of the host cardcages containing the model PT-VME940-T modules need to be powered down during network operation then its power must be supplied from the network cable. See section 2.2.3 to describe how this is done. Any intermediate nodes must use the model PT-VME940-U modules.

Network cabling is installed using either one or a combination of two cabling schemes.

The first scheme is called "Inline" and is usually field assembled using 50 conductor twist/flat cable and 50 pin mass terminated connectors. The cable and connectors are available from Performance Technologies as accessories to the PT-VME940 or may be procured locally. In the Inline scheme, connectors are installed at the ends of the cable run and at as many intermediate points as are required to form the network. The cable connectors are then mated directly to the front panel connectors of the PT-VME940 Adapters. Inline is the simplest and least expensive cabling scheme but, because the connectors must be located at appropriate places on the cable, it must be customer defined.

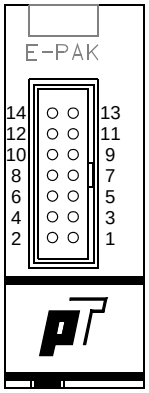
The other cabling scheme is called "T" and is assembled using T Adapter accessories from Performance Technologies and cables from Performance Technologies or fabricated locally. In the T scheme each PT-VME940 is equipped with a T Adapter which consists of a small PCB and a 3 foot cable. The 3’ cable connects to the PT-VME940 and individual cables are used to connect the T Adapters. Because each node to node cable is discrete, they can more easily be replaced or exchanged when the network configuration is changed.

Figure 2: PT-VME940Front Panel



Serial port Cabling

The PT-VME940 Utility Serial Port interconnect is provided on the front panel. The signals are organized so that a mass terminated Insulation Displacement Connectors (IDC) can be used to create an RS232 DTE interconnect. See “Table 27: Utility Serial Port Pin Assignments” on page 71. A 12 inch transition cable is supplied with the PT-VME940 which converts between the 14-pin header and a female shell (male pin) 25-pin D-Shell connector. If a longer cable or a different D-Shell connector sex is



required it can be assembled by following the example below. The Utility Port pin positions are noted in the figure to the left.

The EIA RS232C Specification limits the maximum end to end cable length to 50 ft.

Example

Following is an example cable with vendors and part numbers for the components. These configurations have been tested at PTI. Figure 3: displays an example serial cable for the PT-VME940. The view is with the connector sockets pointing towards you.

An interface cable can be constructed using a 14 conductor ribbon cable to attach a 25-Pin D-Shell IDC to a 14 contact ribbon cable IDC socket. To conserve front panel space only a 14 pin connector is used, however the 25-Pin D-Shell expects 25 conductors, so pin-1 of the ribbon cable must be justified to the pin-1 end of the D-Shell connector. It is recommended that the cable be no longer than necessary for your particular application.

D-Shell Connection

25 position Insulation Displacement Connector Male, D-Shell connector derived from DIN 41612 type C, with rows A and C populated (socket):

3M 8225-6003 or

T&B 609-25P-MA2

Ribbon cable

14 Conductor 28 AWG. Flat Cable

Spectra-Strip 843-191-2801-014 or

3M 3365/14

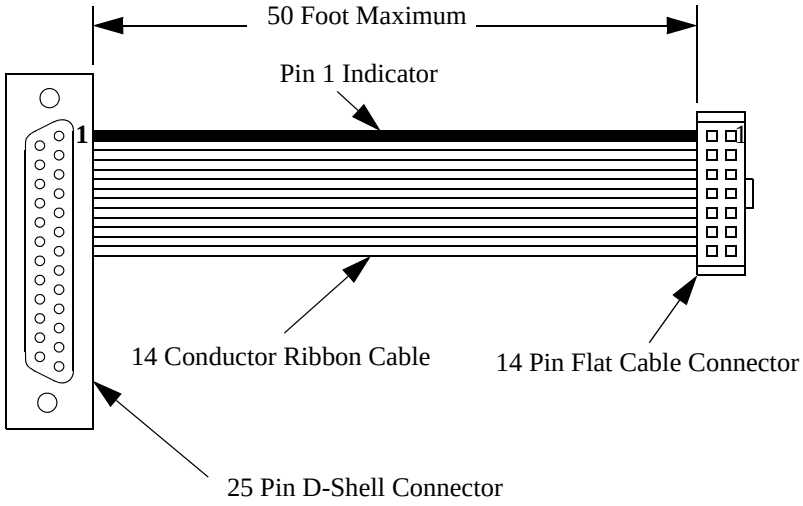
RS232 Serial Port connector

14 Pin Flat Cable Connector center polarized

Burndy FRS14BF-8 (strain relief included) or

AMP 746288-2 (connector)
AMP 499252-9 (strain relief)

Figure 3: Example Serial port Cable



Mechanical restraints

Depending upon your mechanical configuration tie wraps or cable clamps may be necessary to provide mechanical support for the cable.

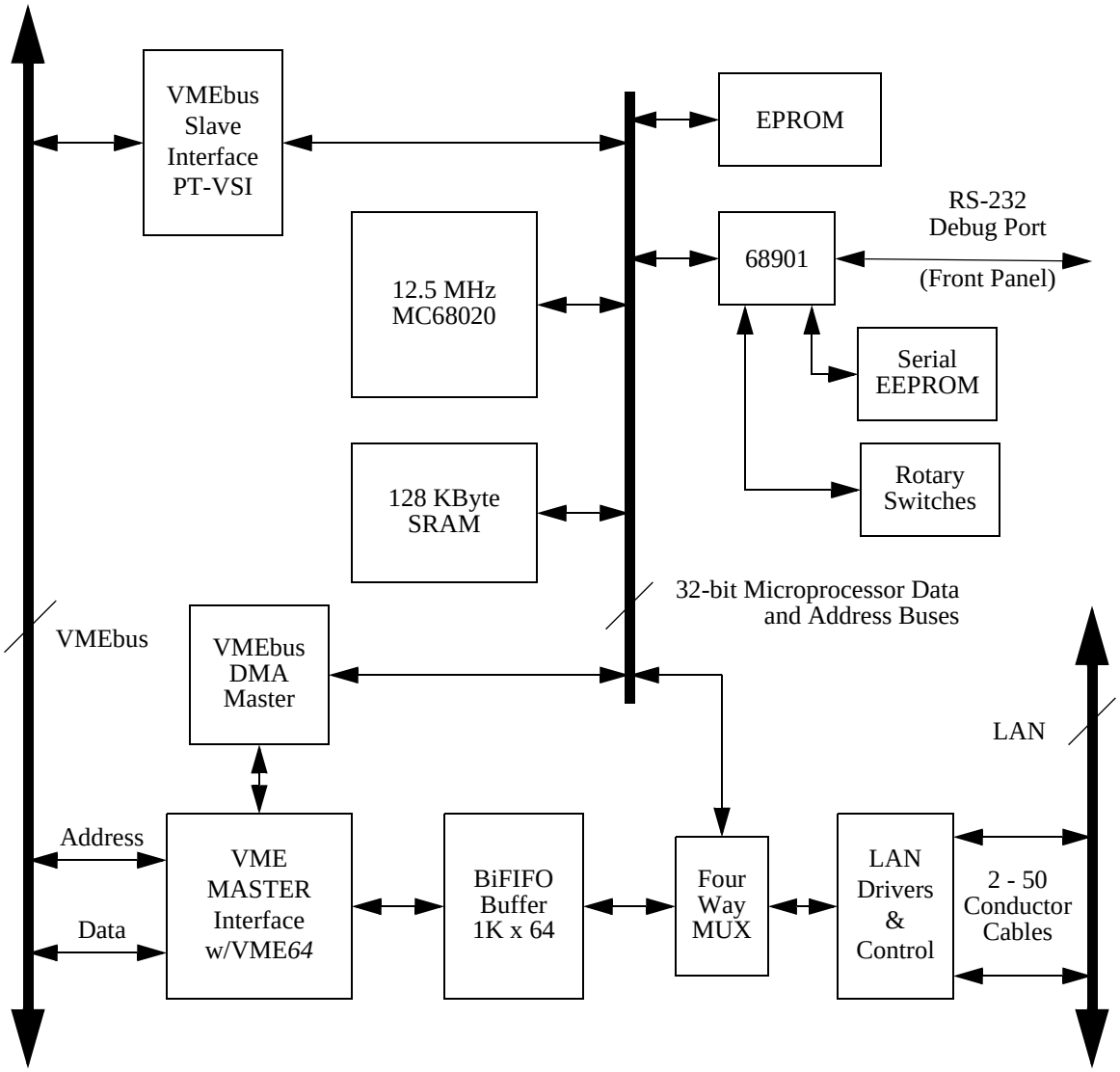
Section

3

FUNCTIONAL DESCRIPTION

A block diagram of the PT-VME940 is provided below. Down the center are the 32-bit microprocessor address and data busses. To the right is an 32-bit buffered data bus that provides high performance LAN interface connectivity. To the left is the VMEbus interface.

Figure 4: Block Diagram



Hardware Description

Static RAM

Four byte-wide static RAMs are provided for use as a 32 bit wide program store. Standard configuration provides four 32Kx8 120nsec SRAMs which allow 0 Wait State performance at 12.5 Mhz. In operation, application firmware is moved from the EPROM to the SRAM after power up/initialization and is executed from SRAM.

Processor

The PT-VME940 is equipped with a 12.5 Mhz MC68020 32 bit microprocessor.

EPROM

The PT-VME940 is equipped with a standard 32 pin JEDEC EPROM socket. The EPROM is accessed as a byte port and is used as a storage device for the application code used to manage the network protocol.

Multi-Function Peripheral

Utility functions on the PT-VME940 are provided by a 68901 Multi- Function Peripheral. This device provides the hardware support for the serial Debug Port as well as timers and I/O lines used internally.

VME*64* Master Interface

The heart of the VME64 interface is a 64-bit wide by 1024 stage bi-directional FIFO. This FIFO effectively decouples the network cable transfer rate from the VMEbus transfer rate and allows maximum size VME64 blocks to be sent/received at speeds limited primarily by the capability of the slave.

The VME64 interface is implemented using an asynchronous state machine utilizing special design techniques to minimize susceptibility to the backplane signal quality degradations commonly seen with high backplane repetition rates.

Cable Interface

The cable interface is managed by a synchronous state machine and is connected to the VME64 Interface FIFO.

VMEbus Slave Interface (VSI)

The VSI is a PTI proprietary ASIC which forms the core of the VMEbus slave interface. The VSI decodes the PT-VME940's slave address by monitoring the VMEbus for a preset address. The VSI provides 16 dual-ported mailbox registers which interrupt the on- board 68020 when they are accessed from the VMEbus. These registers are used to implement the CSB. The VSI also implements the VMEbus interrupter with fully programmable level and vector number.

Network Characteristics

Network Terms

REQUESTER: Any potential network initiator which shares the request line for the purpose of arbitration for bus ownership.

INITIATOR: The winner of Bus arbitration. An initiator must select a target.

TARGET: The object of an initiator's selection. The target must respond to the initiator during selection.

TRANSMITTER: The source of a data transfer.

RECEIVER: The destination of a data transfer.

ARBITRATION: The time period reserved for the resolution of the next bus initiator.

SELECTION: The time period in which the initiator obtains the target's attention in order to send a command.

COMPELLED: A compelled transfer requires full handshake between the transmitter and the receiver for each data transfer longword. That is, the assertion of data strobe is always followed by the assertion of an acknowledge, and the negation of data strobe is followed by the negation of the acknowledge.

NON-COMPELLED: A non-compelled transfer is one in which the transmitter may proceed with data transfers, in a preordained manner, without the full handshake of the receiver. This provides a speed advantage over compelled transfers because the cable delays and logic of a full handshake is avoided.

STREAMING: Non-compelled, hardware generated transfers. Each data transmission is accompanied with a data strobe pulse which maintains a fixed relationship with the data lines. The receiver must maintain an acknowledge (level) while it is able to accept data. In anticipation of an overflow condition, the receiver must de- assert its acknowledge with sufficient buffer remaining to handle the latency of the cable and transmitter mechanism queue.

Physical Level

Media And Devices

The network is implemented using 26LS38 open collector, differential line transceivers driving 44 twisted pairs. The cable is terminated at both ends.

Signal Names

REQuest: A wire OR'ed bus signal which is asserted by all requesters. REQ must be driven by all requesters until they win at bus arbitration and become an initiator. Use of the REQ line provides for a fairness algorithm in the arbitration method.

BuSY: A wire OR'ed bus signal which is asserted by all requesters during the arbitration period. BSY must remain driven by the arbitration winner until that initiator releases ownership of the bus.

SELect: The initiator must drive SEL to interrupt all potential targets. (The target level appears on the data bus). SEL must remain asserted until the target responds (with ATT).

STroBe: STB indicates valid data and parity driven by the transmitter (Selection level, control, status or data stream).

ACKnowledge: During compelled transfers the ACK signal must be pulsed by the receiver for each STB assertion. During non-compelled transfers the ACK signal is driven to a level by the receiver to indicate its ability to receive data.

ATTention: The target may assert ATT to interrupt the initiator. It should provide an edge detected interrupt at the initiator in response to the selection phase, and during exceptions to data transfers. These include any normal termination of the transfer or any errors detected by the target which inhibit continuation without the initiator's interaction.

NoTiCe: The initiator may assert NTC to interrupt the target. It should provide an edge detected interrupt to the target during exceptions to the data transfer. These include any normal termination of the transfer or any errors detected by the initiator which inhibit continuation without the target's interaction.

D00-D31: Data lines used for arbitration level, selection level and data transfer.

DP0-DP3: Data parity lines which provide odd parity checking for each Byte on the data bus. These lines are only used for data transfer operation. Their value is undefined during the arbitration and selection operations on the bus.

TPWR, GND: Power and a common ground reference for the termination resistor networks.

Data Link Level

Arbitration Phase

Arbitration is the process by which a node which desires control of the network bus (a requester) competes with other requesters to determine who controls the bus.

Network protocol provides for two arbitration algorithms selectable when the node is initialized.

The first algorithm (fairness mode) assigns a priority to each requester based on the node's address - address 0 the lowest and address 15 the highest. The requester with the highest priority "wins" when two or more requesters compete in one arbitration cycle. This algorithm is supplemented by a "fairness" procedure which insures that all requesters are serviced before a higher priority requester is allowed to make another request.

The second algorithm (priority mode) uses the priority scheme only and does not include the fairness procedure. As a result, a higher priority requester can "starve" lower priority requesters.

The following is a simplified sequence for "fairness mode":

Step 1 A requester samples BSY and REQ to determine that the network is not busy or in an arbitration cycle. Having found both negated, the requester proceeds to the next step.

Step 2 The requester drives BSY, REQ, and the D00-D15 bit which corresponds to its assigned address (priority).

Step 3 The requester waits a settling period determined by cable propagation characteristics.

Step 4 The requester tests D00-D15 to see if any bit has been driven corresponding to a higher priority. If a higher priority bit is seen the requester has lost the arbitration cycle and negates BSY but keeps REQ asserted. If no other bits are detected, the requester has won the arbitration cycle and can negate REQ and proceed with the selection phase.

Selection Phase

Selection is the process by which the winning requester (now an initiator) selects another network node (the target) with which it wishes to communicate.

The following is a simplified selection sequence:

Step 1 The initiator drives the D00-D15 bit corresponding to the address of the desired target and asserts SEL.

Step 2 Upon detecting the assertion of SEL, all nodes read the value on D00-D15 and compare for their address. If the value matches, the node is the target and it asserts ATT.

Step 3 Having detected the assertion of ATT, the initiator negates SEL and the address bit.

Step 4 Having detected the negation of SEL, the target completes the handshake by negating ATT.

Step 5 Having detected the negation of ATT, the initiator and target have been identified and the initiator may proceed with the command phase.

Command Phase

Once the initiator and the target have been determined by the arbitration and selection phases, the command phase is entered. During the command phase, the network handshake and the processors of the initiator and the target operate in a fully compelled mode. The command phase is the process by which the initiator informs the target about the transfer which is to take place. The following is a simplified command sequence:

Step 1 Initiator sends an eight byte command message to the target. This message contains information about the type of command and other parameters that the target will need to complete the operation.

Step 2 The target, upon receipt of the command message, will analyze it to determine if it has the resources available to complete the operation.

Step 3 Assuming that these resources are available, the target replies with a four byte "ready" response message, the command phase completes, and data phase may begin.

Step 4 If resource are not available, the target replies with a four byte "not ready" response message, the both the target and initiator will disconnect, and the operation will be reconnected when the target acquires the necessary resources.

Data Phase

In the data phase, the network operates in a non-compelled mode. Data is transferred at the rated speed of the cable. The NoTiCe signal is used by the initiator to notify the target of any errors encountered and the ATTention signal is used by the target to notify the initiator of any errors. Completion of the data phase is recognized when the transmitter, either initiator or target, communicates with the receiver using the NoTiCe or ATTention respectively.

Acknowledge Phase

Once the transmitter has signaled the end of the transfer using either NoTiCe or ATTention, it sends a four byte status message to the receiver. This status message indicates whether the message ended normally or because of some error encountered by the transmitter. Upon detecting the end of transfer signal and reading the acknowledge message, the receiver responds with its own four byte acknowledge message indicating the completion status in the receiver.

Operational Level

Master - Slave Operation

In Master - Slave operation the initiator completely controls all aspects of the transfer. The processor in the initiator cardcage specifies all parameters for both the initiator and target. In Master

- Slave transfers a block of data, specified by its physical VMEbus address in the initiator, is moved to/from a physically specified area of memory in the target. The host processor in the target card-cage, if there is one, has no involvement in any aspect of the transaction.

Peer - Peer Operation

In Peer-Peer operation the initiator and target both participate in the transfer of data. The initiator indicates to the target where to read/write the data by means of Logical Unit Number (LUN). A logical unit is a means of allowing the target to setup a buffer, for reading or writing, that is tagged with an LUN without the initiator having any knowledge of the physical size or location of this buffer. An LUN is generated when the host issues a Create Logical Unit command (description in section 3.6.2.3) to the PT-VME940. Several logical units may be created with the same LUN.

In use, the initiator issues the command, during the command phase, and the target determines if it has a logical unit for the specified LUN. If the target has an LUN of sufficient size, it will respond with a ready message and that data transfer phase will begin.

If the case of the target not having an LUN, it will respond with a not ready message and both the target and the initiator will disconnect from the LAN bus. When the target host creates an LUN, the target will perform the arbitration, selection and command phases. The command phase will consist of a reconnect command. At command recognition, the target and initiator will continue, with the data transfer phase, from the point of the disconnect.

In the case of the target not having a logical unit with a buffer of sufficient size the target will respond with an error message with the size of the largest buffer for the specific LUN. The initiator will then respond to its host with an error message and the size indicated.

Section

4

SOFTWARE INTERFACE

IOPB GENERAL

The I/O Parameter Block (IOPB) is the basic control structure used in the software interface to the PT-VME940. IOPBs are constructed for each command to be executed.

An IOPB consists of a number of fields as indicated below. IOPBs can be located virtually anywhere in physical VME memory space, on an individual basis, with minor limitations. They must be located on four or eight byte boundaries depending on the transfer mode specified to read the IOPBs. D32 transfers must be located on four byte boundaries and D64 transfers must be located on eight byte boundaries. IOPBs are "named" according to their starting addresses.

IOPBs are considered "read-only" by the PT-VME940, i.e. they are not written to or altered in any way by the PT-VME940 firmware. The format of a PT-VME940 IOPB is shown below. Those fields which have similar meanings for all operations are described in this section.

IOPB+	31 24	23 16	15 8	7 0
00h	Op Code	Control Bits	Node Address	LUN
04h	No Error Priority/Vector		Error Priority/Vector	
08h	Chain Address			
0Ch	Buffer Address 1			
10h	T/I X Mode	Transfer Byte Count		
14h	Buffer Address 2			
18h	Controller Parameters 1			
1Ch	Controller Parameters 2			

Table 3: General Form of IOPB

Operation Code Field

Address: IOPB Start + 00
Length: 1 Byte

This field contains the code for the operation to be performed.

31	30	29	28	27	26	25	24
Unused	Unused	Unused	OP4	OP3	OP2	OP1	OP0

Bits	Name	Function
28-24	OP	Operation Code Bits.

Control Bit Field

Address: IOPB Start + 01
Length: 1 Byte

This field has a number of specific control bits which apply only to the IOPB in which they reside.

23	22	21	20	19	18	17	16
Unused	INE	CNE	CEE	Unused	Unused	BTE	Unused

Bits	Name	Function
22	INE	Interrupt Enable Bit.
	1	Enable Interrupts
	0	Disable Interrupts
21	CNE	Chain On No Error Status Enable Bit.
	1	Enable IOPB Chaining On No Error Status
	0	Disable IOPB Chaining On No Error Status
20	CEE	Chain On Error Status Enable Bit.
	1	Enable IOPB Chaining On Error Status
	0	Disable IOPB Chaining On Error Status
17	BTE	Buffered Trace Enable Bit.
	1	Enable Buffered Trace
	0	Disable Buffered Trace

Node Address

Address: IOPB Start + 02
Length: 1 Byte

This field contains the 4 bit Network Node Address.

15	14	13	12	11	10	9	8
Unused	Unused	Unused	Unused	NA3	NA2	NA1	NA0

Bits	Name	Function
11-08	NA	Network Address Bits.

Logical Unit Number

Address: IOPB Start + 03
Length: 1 Byte

This field contains the 8 bit Logical Unit Number.

7	6	5	4	3	2	1	0
LUN7	LUN6	LUN5	LUN4	LUN3	LUN2	LUN1	LUN0

Bits	Name	Function
7-0	LUN	Logical Unit Number Bits.

No Error Interrupt Priority

Address: IOPB Start + 4
Length: 1 Byte

This field contains the Interrupt Priority Level to be used if the Interrupt Enable Bit (INE) is set and the operation completes with no errors.

No Error Status Interrupt Vector Number

Address: IOPB Start + 5
Length: 1 Byte

This field contains the Interrupt Vector Number to be used if the Interrupt Enable Bit (INE) is set and the operation completes with no errors.

Error Status Interrupt Priority

Address: IOPB Start + 6
Length: 1 Byte

This field contains the Interrupt Priority Level to be used if the Interrupt Enable Bit (INE) is set and the operation completes with error status.

Error Status Interrupt Vector Number

Address: IOPB Start + 7
Length: 1 Byte

This field contains the Interrupt Vector Number to be used if the Interrupt enable Bit (INE) is set and the operation completes with Error status.

Chain Address Pointer

Address: IOPB Start + 8
Length: 1 Longword (4 Bytes)

This field contains the address of the next IOPB to process when either one or both of the Chain Enable bits (CNE and/or CEE) are set.

Target/Initiator Transfer Mode

Address: IOPB Start + 10
Length: 1 Byte

This field contains a code which specifies the address modifier and data size used by the Target and Initiator PT- VME940s when transferring data.

7	6	5	4	3	2	1	0
TTM3	TTM2	TTM1	TTM0	ITM3	ITM2	ITM1	ITM0

Bits	Name	Function
7-4	TTM	Target Transfer Mode Bits, TTM. See Codes Below.
3-0	ITM	Initiator Transfer Mode Bits.
	0	A32:D32 Data, Non-Privileged
	1	A32:D32 Program, Non-Privileged
	2	A32:D32 Block, Non-Privileged
	3	A32:D64 Block, Non-Privileged
	4	A32:D32 Data, Supervisor
	5	A32:D32 Program, Supervisor
	6	A32:D32 Block, Supervisor

7	A32:D64 Block, Supervisor
8	A24:D32 Data, Non-Privileged
9	A24:D32 Program, Non-Privileged
A	A24:D32 Block, Non-Privileged
B	A24:D64 Block, Non-Privileged
C	A24:D32 Data, Supervisor
D	A24:D32 Program, Supervisor
E	A24:D32 Block, Supervisor
F	A24:D64 Block, Supervisor

Buffer Address

Address: IOPB Start + 0C or IOPB Start + 14
Length: 4 Bytes

This field contains the address of the start of the data buffer. This address must lie on a natural boundary. The natural boundary is either a four byte boundary for D32 transfers or an eight byte boundary for D64 transfers.

Transfer Byte Count

Address: IOPB Start + 11
Length: 3 Bytes

This field contains the number of bytes to be transferred from the source to the destination. This count must be an even multiple of the natural boundary. This is either evenly divisible by four for any D32 transfers or evenly divisible by eight for a D64 transfer.

OPERATIONS

This section describes each of the controller operations. For each operation, the IOPB fields specific to that operation are described. For fields not described in this section, see the previous section "IOPB GENERAL". Fields shown as blank are not required for the operation and are ignored by the firmware.

Master-Slave Read

This operation will read the indicated number of bytes from the target cardcage, target buffer address, into the initiator cardcage, initiator buffer address. Status will only be given to the initiator's host.

IOPB+	31 24	23 16	15 8	7 0
00h	00	Control Bits	Node Address	
04h	No Error Priority/Vector		Error Priority/Vector	
08h	Chain Address			
0Ch	Buffer Address 1			
10h	T/I X Mode	Transfer Byte Count		
14h	Buffer Address 2			
18h				
1Ch				

Table 4: Master-Slave Read IOPB

Initiator Buffer Address

Address: IOPB Start + 0C
Length: 1 Longword

This field contains the address of the start of the initiator (master) data buffer.

Transfer Byte Count

Address: IOPB Start + 11
Length: 3 Bytes

This field contains the length of the transfer in bytes.

Target Buffer Address

Address: IOPB Start + 14
Length: 1 Longword

This field contains the address of the start of the target (slave) data buffer.

Master-Slave Write

This operation will write the indicated number of bytes from the initiator cardcage, initiator buffer address, to the target cardcage, target buffer address. Status will only be given to the initiator's host.

IOPB+	31 24	23 16	15 8	7 0
00h	01	Control Bits	Node Address	
04h	No Error Priority/Vector		Error Priority/Vector	
08h	Chain Address			
0Ch	Initiator Buffer Address 1			
10h	T/I X Mode	Transfer Byte Count		
14h	Target Buffer Address			
18h				
1Ch				

Table 5: Master-Slave Write IOPB

Initiator Buffer Address

Address: IOPB Start + 0C
Length: 1 Longword

This field contains the address of the start of the initiator (master) data buffer.

Transfer Byte Count

Address: IOPB Start + 11
Length: 3 Bytes

This field contains the length of the transfer in bytes.

Target Buffer Address

Address: IOPB Start + 14
Length: 1 Longword

This field contains the address of the start of the target (slave) data buffer.

Peer-Peer Read

This operation will read the indicated number of bytes from the target cardcage, via the Logical Unit Number (LUN), into the initiator cardcage, buffer address. Status will be returned to both the initiator and the target hosts.

IOPB+	31 24	23 16	15 8	7 0
00h	04	Control Bits	Node Address	LUN
04h	No Error Priority/Vector		Error Priority/Vector	
08h	Chain Address			
0Ch	Buffer Address			
10h	Xfer Mode	Transfer Byte Count		
14h				
18h				
1Ch				

Table 6: Peer-Peer Read IOPB

Buffer Address

Address: IOPB Start + 0C
Length: 1 Longwor

This field contains the address of the start of the data buffer.

Transfer Byte Count

Address: IOPB + 11
Length: 3 Bytes

This field contains the length of the transfer in bytes.

Peer-Peer Write

This operation will write the indicated number of bytes from the initiator cardcage, buffer address, to the target cardcage via the Logical Unit Number (LUN). Status will be returned to both the initiator and the target.

IOPB+	31 24	23 16	15 8	7 0
00h	05	Control Bits	Node Address	LUN
04h	No Error Priority/Vector		Error Priority/Vector	
08h	Chain Address			
0Ch	Buffer Address			
10h	Xfer Mode	Transfer Byte Count		
14h				
18h				
1Ch				

Table 7: Peer-Peer Write IOPB

Buffer Address

Address: IOPB Start + 0C
Length: 1 Longword

This field contains the address of the start of the data buffer.

Transfer Byte Count

Address: IOPB + 11
Length: 3 Bytes

This field contains the length of the transfer in bytes.

Get Firmware Revision Level

This operation allows a method to check the current firmware level on other nodes in the network. This command will supply the revision level in the first byte of the auxiliary status in the Control/Status Block (CSB). This operation allows a means to test for a particular node's presence on the LAN bus. If the node is not there, a time out error will occur.

IOPB+	31 24	23 16	15 8	7 0
00h	03	Control Bits	Node Address	
04h	No Error Priority/Vector		Error Priority/Vector	
08h	Chain Address			
0Ch				
10h				
14h				
18h				
1Ch				

Table 8: Get Firmware Revision Level IOPB

Create Logical Unit

Create Logical Unit is an operation used in Peer-Peer communications. In Peer-Peer, the target host processor must assign a buffer for the reception or transmission of data. This assignment process is conducted using a Create Logical Unit operation.

IOPB+	31 24	23 16	15 8	7 0
00h	08	Control Bits	Node Address	LUN
04h	No Error Priority/Vector		Error Priority/Vector	
08h	Chain Address			
0Ch	Buffer Address			
10h	Xfer Mode	Byte Count		
14h				
18h				
1Ch				

Table 9: Create Logical Unit IOPB

Buffer Address

Address: IOPB Start + 0C
Length: 1 Longword

This longword contains the address of the start of the LUN data buffer.

Byte Count

Address: IOPB Start + 11
Length: 3 Bytes

This field contains the LUN buffer length in bytes.

Set Parameters

This operation is used to set or change local board parameters. Usually, this operation is preceded by a "Read Parameters" operation which creates an image of the "Set Parameters" IOPB. This IOPB can then be altered and the "Set Parameters" operation completed. This operation stores the new parameters in the PT-VME940 EEPROM. The new parameters will not take effect until a board or system reset is issued.

IOPB+	31 24	23 16	15 8	7 0
00h	0C	Control Bits		
04h	No Error Priority/Vector		Error Priority/Vector	
08h	Chain Address			
0Ch				
10h				
14h				
18h	Controller Parameters			
1Ch	Controller Slave Address			

Table 10: Set Parameters IOPB

Controller Parameters Field

Address: IOPB Start + 18
Length: 1 Longword

This field contains the following information.

31	30	29	28	27	26	25	24
TBSZ5	TBSZ4	TBSZ3	TBSZ2	TBSZ1	TBSZ0	BRQL1	BRQL0

Bits	Name	Function
31-26	TBSZ	Trace Buffer Size Bits. These bits specify the buffer size, in 1K byte blocks, allocated for the accumulation of trace information.
25-24	BRQL	Bus Request Level Bits. These bits specify the VMEbus request level used by the PT-VME940 VMEbus master logic.
	0	BRL0
	1	BRL1

2 BRL2
3 BRL3

23	22	21	20	19	18	17	16
Unused	Unused	Unused	Unused	DDX MD3	DDX MD2	DDX MD1	DDX MD0

Bits	Name	Function
19-16	DDXMD	Default Data Transfer Mode Bits. These bits specify one of 16 VMEbus master transfer modes to be used for the transfer of IOPBs. Codes are the same as for Target and Initiator Transfer Mode bits TTM and ITM.

15	14	13	12	11	10	9	8
UFA	Unused	SLAM5	SLAM4	SLAM3	SLAM2	SLAM1	SLAM0

Bits	Name	Function
15	UFA	Use Fairness Algorithm Control Bit. This bit controls the use of the fairness algorithm in the network arbitration phase. 1 Use Fairness Algorithm 0 Don’t Use Fairness Algorithm
13-8	SLAM	Slave Address Modifier Code Bits. These bits specify the VMEbus AM to be used in decoding the PT-VME940 slave address.

7	6	5	4	3	2	1	0
NOD ID3	NOD ID2	NOD ID1	NOD ID0	SA MSK3	SA MSK2	SA MSK1	SA MSK0

Bits	Name	Function
7-4	NODID	Network Node Address Bits. Used to specify the network node address.
3-0	SAMSK	Slave Address Modifier Mask Bits. This mask is used as a logical OR with the slave address modifier code when determining the slave response of the PT- VME940. The mask allows the PT-VME940 to respond to a group of AM codes by making some of the bits "don’t care".

Controller Slave Address

Address: IOPB Start + 1C
Length: 1 Longword

This field contains the VMEbus slave address of the controller.

Read Parameters

This operation reads the current state of the controller parameters, prepares an image of the "Set Parameters" IOPB and places that image at the address specified by the "Buffer Address" field.

If the set configuration command has not been issued or the configuration was not changed via the debug port, the default slave configuration can be found in section 2.2.2.1.

IOPB+	31 24	23 16	15 8	7 0
00h	0Dh	Control Bits		
04h	No Error Priority/Vector		Error Priority/Vector	
08h	Chain Address			
0Ch	Buffer Address			
10h				
14h				
18h				
1Ch				

Table 11: Read Parameters IOPB

Retry Manipulation

This operation allows a method to change the maximum number of LAN retries, either the current value and/or the default value. It also allows a method to get the total number of retries that have occurred since the last board reset. There is also a method to reset this total.

IOPB+	31 24	23 16	15 8	7 0
00h	0Eh	Control Bits		
04h	No Error Priority/Vector		Error Priority/Vector	
08h	Chain Address			
0Ch	Retry Count Address			
10h				
14h				
18h	Retry Cmnd			Retry Limit
1Ch				

Table 12: Retry Manupulation IOPB

Retry Address

Address: IOPB Start + 0C
Length: 1 Longword

This field contains the address to put the 32-bit retry count if requested.

Retry Cmnd

Address: IOPB Start + 18
Length: 1 Byte

This field contains the following commands.

7	6	5	4	3	2	1	0
Unused	Unused	Unused	Unused	SRL1	SRL0	RTR	RSTR

Bits	Name	Function
3-2	SRL	Set Retry Limit Bit.
	0	Ignore.
	1	Use retry limit field to update the current retry limit. The current limit will revert back to the default, located in EEPROM, after a reset.

	2	Update the default retry limit with the current value.
	3	Update the current retry limit with the retry limit field and use that value to update the default in EEPROM.
1	RTR	Read Total number of Retries into the address pointed to by the Retry Address (four bytes).
	1	Copy Retry Count.
	0	Don't Copy Retry Count.
0	RSTR	Reset the total number of retries.
	1	Reset count.
	0	Don't Reset Count.

Retry Limit

Address: IOPB Start + 1B
Length: 1 Byte

This field contains the new retry limit.

Buffer Address

Address: IOPB Start + 0C
Length: 1 Longword

This field contains the starting address of the parameters buffer.

Read Buffer

This operation will read data from the VMEbus starting at the Buffer Address specified and place it into a pre-defined on-board SRAM buffer. The number of bytes transferred will be specified by the Byte Count field. This operation is limited to 1024 transfers.

IOPB+	31 24	23 16	15 8	7 0
00h	10h	Control Bits		
04h	No Error Priority/Vector		Error Priority/Vector	
08h	Chain Address			
0Ch	Buffer Address			
10h	Xfer Mode	Byte Count		
14h				
18h				
1Ch				

Table 13: Read Buffer IOPB

Buffer Address

Address: IOPB Start + 0C
Length: 1 Longword

This field contains the starting address of the data buffer.

Byte Count

Address: IOPB Start + 10
Length: 3 Bytes

This field contains the length, in bytes, of the buffer to be transferred. The byte count is limited to 4K bytes in any D32 transfer mode and 8K bytes in D64 transfer mode.

Write Buffer

This operation will read data from the pre-defined on-board SRAM buffer and write it to the VMEbus starting at the Buffer Address specified. The number of bytes transferred will be specified by the Byte Count field. This operation is limited to 1024 transfers or less.

IOPB+	31 24	23 16	15 8	7 0
00h	11h	Control Bits		
04h	No Error Priority/Vector		Error Priority/Vector	
08h	Chain Address			
0Ch	Buffer Address			
10h	Xfer Mode	Byte Count		
14h				
18h				
1Ch				

Table 14: Write Buffer IOPB

Buffer Address

Address: IOPB Start + 0C
Length: 1 Longword

This field contains the starting address of the data buffer.

Byte Count

Address: IOPB Start + 10
Length: 3 Bytes

This field contains the length, in bytes, of the buffer to be transferred. The byte count is limited to 4K bytes in any D32 transfer mode and 8K bytes in D64 transfer mode.

Compare Buffer

This operation will read data from the pre-defined on-board SRAM buffer and compare it to data read from the VMEbus at the location specified by Buffer Address. The length of the compare operation is limited to 1024 transfers. A miscompare will generate an error status.

IOPB+	31 24	23 16	15 8	7 0
00h	12h	Control Bits		
04h	No Error Priority/Vector		Error Priority/Vector	
08h	Chain Address			
0Ch	Buffer Address			
10h	Xfer Mode	Byte Count		
14h				
18h				
1Ch				

Table 15: Compare Buffer IOPB

Buffer Address

Address: IOPB Start + 0C
Length: 1 Longword

This field contains the starting address of the data buffer to be compared.

Byte Count

Address: IOPB Start + 10
Length: 3 Bytes

This field contains the length, in bytes, of the buffer to be compared. The byte count is limited to 4K bytes in any D32 transfer mode and 8K bytes in D64 transfer mode.

Write Patterns

This operation writes the pattern specified in 32-Bit Pattern field to the VMEbus buffer specified by Buffer Address. The number of bytes written is specified by the Byte Count field and is limited to 1024 transfers.

IOPB+	31 24	23 16	15 8	7 0
00h	13h	Control Bits		
04h	No Error Priority/Vector		Error Priority/Vector	
08h	Chain Address			
0Ch	Buffer Address			
10h	Xfer Mode	Byte Count		
14h	32-Bit Pattern			
18h				
1Ch				

Table 16: Write Patterns IOPB

Buffer Address

Address: IOPB Start + 0C
Length: 1 Longword

This field contains the starting address of the data buffer to which patterns are to be written.

Byte Count

Address: IOPB Start + 10
Length: 3 Bytes

This field contains the length, in bytes, of the buffer to be transferred. The byte count is limited to 4K bytes in any D32 transfer mode and 8K bytes in D64 transfer mode.

32-Bit Pattern

Address: IOPB Start + 14
Length: 1 Longword

This field contains the 32-bit pattern to be written.

Buffered Copy

This operation will copy data starting at the Source Buffer Address into a pre-defined on-board SRAM buffer and from there to the buffer specified by the Destination Buffer Address. The number of bytes copied is specified by the Byte Count field and is limited to 1024 transfers.

IOPB+	31 24	23 16	15 8	7 0
00h	14h	Control Bits		
04h	No Error Priority/Vector		Error Priority/Vector	
08h	Chain Address			
0Ch	Source Buffer Address			
10h	T/I X Mode	Byte Count		
14h	Destination Buffer Address			
18h				
1Ch				

Table 17: Buffered Copy IOPB

Source Buffer Address

Address: IOPB Start + 0C
Length: 1 Longword

This field contains the starting address of the source VMEbus buffer.

Byte Count

Address: IOPB Start + 10
Length: 3 Bytes

This field specifies the length of the buffer to be copied. The byte count is limited to 4K bytes in any D32 transfer mode and 8K bytes in D64 transfer mode.

Destination Buffer Address

Address: IOPB Start + 14
Length: 1 Longword

This field contains the starting address of the destination VMEbus buffer.

Size Limited Non-Buffered Copy

This operation will copy data starting at the Source Buffer Address directly into the buffer specified by the Destination Buffer Address. The data is not stored in on-board SRAM but does pass through the VMEbus interface FIFOs. The number of bytes copied is specified by the Byte Count field and is limited to 1024 transfers.

IOPB+	31 24	23 16	15 8	7 0
00h	15h	Control Bits		
04h	No Error Priority/Vector		Error Priority/Vector	
08h	Chain Address			
0Ch	Source Buffer Address			
10h	T/I X Mode	Byte Count		
14h	Destination Buffer Address			
18h				
1Ch				

Table 18: Size Limimited Non-Buffered Copy IOPB

Source Buffer Address

Address: IOPB Start + 0C
Length: 1 Longword

This field contains the starting address of the source VMEbus buffer.

Byte Count

Address: IOPB Start + 10
Length: 3 Bytes

This field specifies the length of the buffer to be copied. The byte count is limited to 4K bytes in any D32 transfer mode and 8K bytes in D64 transfer mode.

Destination Buffer Address

Address: IOPB Start + 14
Length: 1 Longword

This field contains the starting address of the destination VMEbus buffer.

Transfer Mode Limited Non-Buffered Copy

This operation will copy data starting at the Source Buffer Address directly into the buffer specified by the Destination Buffer Address. The data is not stored in on-board SRAM but does pass through the VMEbus interface FIFOs. The number of bytes copied is specified by the Byte Count field. This operation is limited to only the initiator transfer mode.

IOPB+	31 24	23 16	15 8	7 0
00h	16h	Control Bits		
04h	No Error Priority/Vector		Error Priority/Vector	
08h	Chain Address			
0Ch	Source Buffer Address			
10h	T/I X Mode	Byte Count		
14h	Destination Buffer Address			
18h				
1Ch				

Table 19: Transfer Mode Limimited Non-Buffered Copy IOPB

Source Buffer Address

Address: IOPB Start + 0C
Length: 1 Longword

This field contains the starting address of the source VMEbus data buffer.

Transfer Byte Count

Address: IOPB + 11
Length: 3 Bytes

This field specifies the length of the buffer to be copied in bytes.

Destination Buffer Address

Address: IOPB Start + 14
Length: 1 Longword

This field contains the starting address of the destination VMEbus data buffer.

CSB

The Control/Status Block (CSB) is used for overall control of the PT-VME940, for submitting IOPBs, and to determine status of completed IOPBs.

The CSB is divided, by firmware convention, into three groups: the Controller Control/Status Block, the IOPB Command block, and the IOPB Status block. Basically, the IOPB Command Block is used to signal the PT-VME940 that an IOPB has been prepared and is ready to be placed in the command queue, the IOPB Status Block is where the status of completed IOPBs is found, and the Controller Control/Status Block is used for general PT-VME940 command and status transfer.

In contrast to IOPBs, which can be located virtually anywhere in VME physical memory space on an individual basis, the CSB is located at a memory address determined during the initialization of the PT-VME940. The CSB is accessed as an D8(odd) device only.

CSB+	7 0
01h	Controller CSR
03h	General Interrupt Priority
05h	General Interrupt Vector
07h	Command Byte
09h	Command Address 0
0Bh	Command Address 1
0Dh	Command Address 2
0Fh	Command Address 3
11h	Status Byte
13h	Auxillary Status 0
15h	Auxillary Status 1
17h	Auxillary Status 2
19h	Status Address 0
1Bh	Status Address 1
1Dh	Status Address 2
1Fh	Status Address 3
3Dh	Controller Reset

Table 20: CSB Structure

Controller Control/Status Register

Address: CSB Start + 01
Length: 1 Byte

This byte contains command and status bits for functions which effect the entire controller:

7	6	5	4	3	2	1	0
PUDF	TP	GTE	Unused	PUDS3	PUDS2	PUDS1	PUDS0

Bits	Name	Function
7	PUDF	Power Up Diagnostic Failure Bit.
	1	Power Up Diagnostic Failure Occurred
	0	No Power Up Diagnostic Failure
6	TP	Trace Print Bit.
	1	Print Contents of Trace Buffer
	0	Do Not Print Trace
5	GTE	Global Trace Enable Bit.
	1	Reset and Enable Sequence Trace Mode
	0	Disable Sequence Trace Mode
3-0	PUDS	Power-Up Diagnostic Status Code Bits.
	0	Passed Power-Up Test.
	1	Failed - Vector Install.
	2	Failed.
	3	Failed.
	4	Failed - VSI Mailbox Write/Read.
	5	Failed - VSI Mailbox TAS.
	6	Failed - MFP Reg. Write/Read.
	7	Failed - MFP Timers.
	8	Failed - MFP Interrupt.
	9	Failed - EEPROM Read Check.
	10	Failed - VTCR Register.
	11	Failed - FIFO Flag And SR.

General Interrupt Priority Byte

Address: CSB Start + 03
Length: 1 Byte

This byte is loaded with the priority for the general controller interrupt. If this byte is non-zero, the controller uses this interrupt priority (and the vector number in the following byte) to interrupt on conditions where an IOPB-specific interrupt is not appropriate. An example of this would be a VMEbus Bus Error while copying in an IOPB.

General Interrupt Vector Number Byte

Address: CSB Start + 05
Length: 1 Byte

This byte is used in conjunction with the General Interrupt Priority Byte when a non-IOPB specific interrupt must be generated.

Command Byte

Address: CSB Start + 07
Length: 1 Byte

This byte is used to check the readiness of the controller to accept a command. If ready, issue an IOPB to the controller, cancel one or all outstanding IOPBs or request the status of an IOPB.

In operation, the host checks this byte for zero, if the byte is zero, the controller is ready, and the appropriate command code is written. The IOPB address must then be written to the four Command Address Bytes. Writing of the last Command Address Byte (3) signals the PT-VME940 firmware and command processing begins.

Note that if multiple, independent host masters are present, the test and write of the Command Byte must be done using an uninterruptable cycle.

When reading this byte to check for "ready" the following values may be found:

FF	The controller is not "ready" because it is performing self test diagnostics.
Other Non-Zero	The controller is not "ready" because the command pool is full, the last command accepted is the value found.

The command codes are as follows:

80	GO: This command is used to issue an IOPB to the PT-VME940 and must be accompanied by the IOPB address.
81	CANCEL IOPB: This command is used to cancel a specific IOPB. The address of the IOPB must be supplied.
82	CANCEL ALL IOPB: This command is used to cancel all IOPBs currently in the active pool and Target Logical Unit table. A dummy address (usually 0000 but "don’t care") must be supplied.
84	REQUEST IOPB STATUS: This command is used to request the status of a specific IOPB. The address of the IOPB must be specified. The PT-VME940 will search its command pool and Logical Unit table for the requested IOPB and return status via the Auxiliary Status Register.

Command Address Bytes

Address: CSB Start + 09
Length: 4 Bytes

These bytes are used to supply the IOPB address when they are issued to the PT-VME940. The most significant byte of the Command Address is stored in Command Address Byte 0 and the least significant byte of the Command Address is stored in Command Address Byte 3. Command Address Byte 3 must be written last as this signals the PT-VME940 that the address is complete.

Status Byte

Address: CSB Start + 11
Length: 1 Byte

This byte contains status information pertaining to a particular IOPB whose address is contained in the Status Address Bytes. When the chain mode is enabled, the IOPB whose address appears in the Status Address Bytes is the address of the last IOPB in the chain.

In typical, interrupt driven operation, this byte is cleared by the host after the interrupt is received to indicate to the PT-VME940 that IOPB Address and Status have been read and acknowledged. Various modes of non-interrupt driven (polled) operation are possible in which the Status Byte is tested for non-zero value to determine command completion. In all cases, before status is posted to the Status Byte, the address of the IOPB concerned is posted in the Status Address Bytes.

7	6	5	4	3	2	1	0
CMP3	CMP2	CMP1	CMP0	INNA3	INNA2	INNA1	INNA0

Bits	Name	Function
7-4	CMP	Completion Code Status Bits.
	0	Never Used
	1	Command Completed With Error Status
	2	Command Completed With Good Status
	3	Target Completion With Error Status
	4	Target Completion With Good Status
	5	Command Completed With Transfer Count Error
	6	Not Used
	7	Target Completion With Transfer Count Error
	8	Chain Mode Completed With Good Status
	9	Chain Mode Completed With Error Status
	10	Not Used
	11	Chain Mode Completed With Transfer Count Error
	12	Not Used
	13	Chain Mode Target Completion With Error Status
	14	Chain Mode Target Completion With Good Status
	15	Chain Mode Target Completion With Transfer Count Error
3-0	INNA	Initiator Network Node Address Bits. This is only valid after a target completion.

Auxiliary Status Bytes

Address: CSB Start + 13
Length: 3 Bytes

Valid Auxiliary Status Codes, for commands ending in error, are as follows:

1001h	IOPB in Pool, ready to run (Request Status Only)
1002h	IOPB Running (Request Status Only)
1004h	IOPB Disconnected (threaded) (Request Status Only)
1080h	IOPB Killed (Caused by either "Cancel IOPB" or "Cancel All IOPB" commands).
10FFh	IOPB Not Found (Request Status Only)
8001h	Initiator Data Alignment Error. The initiator data buffer address presented does not align the data on a natural boundary (see section 3.6.1.11 for description).
8002h	Initiator Data Byte Count Error. The initiator data byte count presented is not an even multiple of a natural boundary (see section 3.6.1.12 for description).
8003h	Target Data Alignment Error.
8004h	Target Data Byte Count Error.
8005h	VMEbus Bus Error occurred at the target.
8006h	VMEbus Timeout occurred at the target.
8042h	Select Timeout. This code is reported when the target fails to respond to the selection phase within one second.
8900h	Network Data Parity. This error code indicates that a parity error was detected.
9000h	Unknown Op Code in IOPB.
8043h	Transfer Time Out. LAN transfer idle for greater than 150 msec.
8B00h	LAN Data Register Bus Error.
A008h	Internal bus access error. This error is reported when an internal controller bus error occurs during firmware execution.
A0xxh	Internal unexpected exception. This error is reported when an unexpected internal exception occurs. The vector number of the exception is contained in the lower byte.

B108h	Bus Error during IOPB copy. This error is reported when a VMEbus BERR occurs during DMA of an IOPB.
B208h	Bus Error during data DMA. This error is reported when a VMEbus BERR occurs during data DMA to/from the VMEbus.
C000h	EEPROM Write/Read Miscompare. This error is reported when a read-after-write check of updated data in the EEPROM fails.
D000h	Diagnostic Command Error. The compare operation failed during the Compare Buffer operation.

Status Address Bytes

Address: CSB Start + 19
Length: 4 Bytes

These bytes are used to supply the address of the IOPB which has completed or otherwise posted status. They may be read in any order.

Controller Reset

Address: CSB Start + 3D
Length: 1 Byte

This location is used to issue a "hard" reset to the PT- VME940. The reset is issued by writing an "AA" to the location and results in a complete reset and initialization of the controller. All commands and functions in progress are aborted.

TYPICAL OPERATIONS

Power-Up and Reset Initialization

The following steps would typically be used to determine the readiness of the PT-VME940 to accept commands following a power up or software controlled reset:

Attempt to read the "Command Byte" located in the CSB. Possible results are; VMEbus BERR (until the slave address decoder is enabled), a value of FF (self test running), or 00 (controller ready).

Repeat read of "Command Byte" until a 00 is detected or a period of 5 seconds has elapsed.

When a 00 (controller ready) is read, CSB Aux. Status 0 contains the Firmware Revision Number and CSB Aux. Status 1 contains the Network Node Address of the PT-VME940. These values persist until the first command is issued to the PT-VME940.

If, after 5 seconds, reading the "Command Byte" still results in FF, the PT-VME940 self test can be assumed to have failed and the self test status can be found in the Controller CSR.

Single Thread, Interrupt Driven Operation

The following steps would typically be used to set up and run commands in a single thread, interrupt driven mode:

Construct IOPB in memory with interrupt enable "on".

Test for PT-VME940 "ready" and set "go" command in CSB using an uninterruptable processor cycle. Write 32-bit address of IOPB into CSB.

Wait for interrupt.

When interrupted, acknowledge interrupt by clearing status byte in CSB.

Prepare next IOPB.

Multi-Thread, Interrupt Driven Operation

In the context of the PT-VME940, multi-threading means that a group of commands are executed in parallel, the completion of each command dependent primarily on the availability of the network bus and the status of node being accessed. Thus, the order in which the commands are presented to the controller is not the sole determining factor in the sequence in which the commands are executed or completed.

The following steps would typically be used to set up and run commands in a multi-thread, interrupt driven mode:

Construct one or more IOPBs in memory with interrupt enable "on".

Test for PT-VME940 "ready" and set "go" command in CSB using an uninterruptable processor cycle. Write 32-bit address of IOPB into CSB. Repeat for each IOPB to be submitted.

Wait for interrupt.

When interrupted, read the address and status of the IOPB causing the interrupt from the CSB and acknowledge the interrupt by clearing status byte in CSB. Each IOPB, when completed will result in an interrupt.

Prepare additional IOPBs.

Single-Thread, Chained Mode Operation

Chaining is another mechanism which the PT-VME940 offers to allow multiple commands to be submitted. In contrast to multi-threading, which exploits parallelism, chaining guarantees sequence.

In chain mode, a group of IOPBs are chained by constructing pointers from one IOPB to the next. The address of the first IOPB is submitted to the PT-VME940 and the chain is executed in sequence.

Execution of the next IOPB in a chain is dependent on the completion status of the previous IOPB. The PT-VME940 allows the option of chaining on successful or unsuccessful IOPB completion.

The following steps would typically be used to set up and run chained commands in a single-thread, interrupt driven mode:

Construct two or more IOPBs in memory with the chain address pointer in the Nth IOPB pointing to the N+1th IOPB. Select "chain on successful completion" mode.

Test for PT-VME940 "ready" and set "go" command in CSB using an uninterruptable processor cycle. Write 32-bit address of the first IOPB in the chain into CSB.

Wait for interrupt.

When interrupted, read the address and status of the IOPB causing the interrupt, should be the last IOPB in the chain if there were no errors, from the CSB and acknowledge the interrupt by clearing status byte in CSB.

Prepare additional IOPBs.

Protocol Trace Operation

The Protocol Trace function can be of assistance in debugging host software or network setup problems. The Trace function stores a running "commentary" on the firmware controlled activities taking place as commands are submitted, decoded, executed, and completed.

This trace information is stored in a pre-allocated buffer for later output to the diagnostic port. The size of this buffer can be adjusted (see section 2.2). The Trace function may be independently invoked by one of two mechanisms; a control bit in the CSB enables Trace for all IOPBs, or a bit in an individual IOPB enables Trace only for that IOPB.

Trace is typically used when debugging a new network configuration it provides a detailed account of the network transactions without seriously impacting the network performance. The following steps would be used to enable Protocol Trace globally for all IOPBs:

Connect an ASCII terminal to the diagnostic port of the PT-VME940.

Specify the size of the buffer to be used to accumulate trace information using either the configuration menu or the appropriate local operation.

Set Global Trace bit in the Controller CSR.

Initiate commands as desired.

Set the Trace Print bit in the Controller CSR to print accumulated trace information on the ASCII terminal.

Section

5 FUNCTIONAL SUMMARY

Hardware Specifications

Characteristic	Specification
Processor	68020 @ 12.5 Mhz.
Program Store Memory	Static RAM 128K Bytes 0 Wait State Performance
VMEbus Transfer Rate	60 Mbytes/second
Cable Transfer Rate	40 Mbytes/second
VMEbus Master Interface	A32/A24:D64/D32 BLT A32/A24:D32/D16/D8(EO)
Maximum Number Of Nodes	16
Maximum Length Of Cable	100 feet

Memory Map

This map describes the location of all configuration and operational registers of the PT-VME940. The sizing column indicates if the device supports 68030 data bus sizing.

Table 21: Memory Map

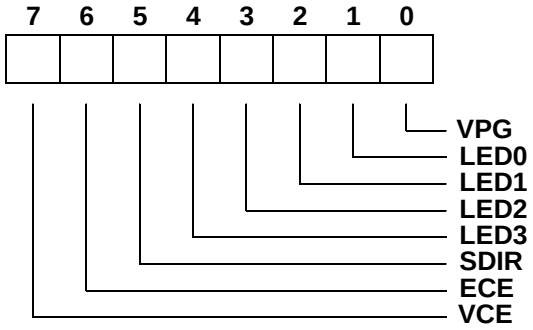
ADDRESS RANGE	DEVICE	WIDTH	SIZING
00000000h-03FFFFFFh	ROM/PROM (U23)	BYTE	Yes
04000000h-07FFFFFFh	ROM/SRAM (U29)	BYTE	Yes
08000000h-0800000Fh	68681 DUART	BYTE	Yes
0A000000h-0A00000Fh	FAS216 SCSI	BYTE	Yes
0C000000h	Status Register	BYTE	No
0D000000h	Control Register	BYTE	No
0E000000h	SCSI MAR	LWORD only	No
10000000h-1000000Fh	ACC	BYTE	Yes
18000000h-1800004Ch	DARF64	LWORD 0nly	No
20000000h-2FFFFFFFh	Main Memory	LWORD	Yes
30000000h-37FFFFFFh	EPAK	EPAK defined	
38000000h-38FFFFFFh	EPAK 0 WS	LWORD	Yes
40000000h-4FFFFFFFh	SRAM Module	LWORD	Yes
50000000h-7FFFFFFFh	UNASSIGNED		
80000000h-FFFFFFFFh	VMEbus	Slave Defined	

141 System Registers

There are three registers on the PT-VME940 that are not defined in the referenced data sheets. These registers are unique to the PT-VME940, providing control of major functional blocks and status.

System Control Register

Address 0D000000h
Byte Read/Write Only
All bits cleared to zero by reset

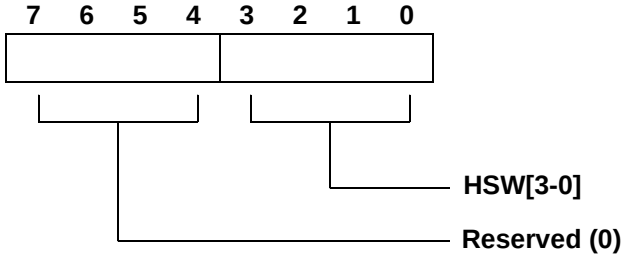


Bit	Name	Function
0	VPG	VMEbus Page bit
	1	VME address bit 31=1
	0	VME address bit 31=0
1	LED0	User Programmable LED D0
	1	LED on
	0	LED off
2	LED1	User Programmable LED D1
	1	LED on
	0	LED off
3	LED2	User Programmable LED D2
	1	LED on
	0	LED off
4	LED3	User Programmable LED D3
	1	LED on
	0	LED off
5	SDIR	SCSI DMA Direction
	1	SCSI DMA Write (read from memory)
	0	SCSI DMA Read (write to memory)
6	ECE	Enable 68030 caching of EPAK accesses
	1	Disable caching
	0	Enable caching

7	VCE	Enable 68030 caching of VMEbus accesses
	1	Disable caching
	0	Enable caching

System Status Register

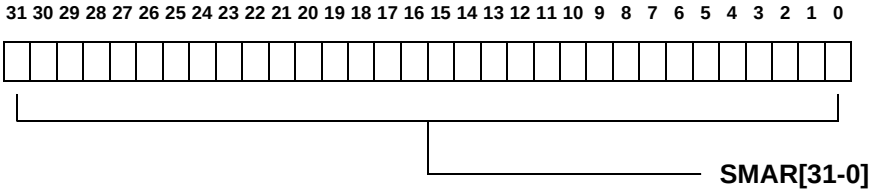
Address 0C000000h
Byte Read Only



Bits	Name	Function
3-0	HSW	Value of Hex Switch
7-4		Reserved, mask to zero when read

SCSI Memory Address Register

Address 0E000000h
Write Only



31-0	SMAR	The SCSI Memory Address Register is written with the starting address for a SCSI DMA transfer. The register retains its value after reset and is undefined after power up

Interrupt Control

The ACC controls local and VMEbus interrupts. Because the ACC allows the dynamic assignment of local interrupts to specific request levels, a fixed interrupt map is unnecessary. The following table lists the internal and VMEbus interrupt sources and the levels to which they may be assigned. The ACC interrupt input pin for each local interrupt request is also shown.

Table 22: Interrupt Request Summary

Interrupt Source	Possible Level Assignments	ACC Input
VMEbus IRQ1	1 (or off) Vectored	VIRQ1
VMEbus IRQ2	2 (or off) Vectored	VIRQ2
VMEbus IRQ3	3 (or off) Vectored	VIRQ3
VMEbus IRQ4	4 (or off) Vectored	VIRQ4
VMEbus IRQ5	5 (or off) Vectored	VIRQ5
VMEbus IRQ6	6 (or off) Vectored	VIRQ6
VMEbus IRQ7	7 (or off) Vectored	VIRQ7
Location Monitor	1-7 (or off) Auto-Vectored	LIRQ0
VMEbus Events	1-7 (or off) Auto-Vectored	LIRQ1
ACC Tick Timer	1-7 (or off) Auto-Vectored	LIRQ2
FAS216 & EPAK [EPIRQ]	1-7 (or off) Auto-Vectored	LIRQ3
EPAK [EPVIR]	1-7 (or off) Vectored	LIRQ4
68681	1-7 (or off) Vectored	LIRQ5
Abort Switch	7 (or off) Auto-Vectored	L7I0
SCSI bus Reset	7 (or off) Auto-Vectored	L7I1
VMEbus [*ACFAIL]	7 (or off) Auto-Vectored	L7I2
VMEbus [*SYSFAIL]	7 (or off) Auto-Vectored	L7I3

Register Maps

The “INIT” column in the register map descriptions below identify the initial register values typically programmed by PTI for our applications. All “INIT” values are in hexadecimal, registers that are “don’t care” at initialization time contain a hyphen.

ACC

Table 23: ACC Register Map

ADDRESS	REGISTER	FUNCTION	INIT
10000000h	STAT0	Status Register 0	-
10000001h	STAT1	Status Register 1	-
10000002h	GENCTL	General Control Register	1C
10000003h	VINT	VMEbus Interrupter Register	-
10000004h	VREQ	VMEbus Requester Register	03
10000005h	VARB	VMEbus Arbiter Register	00
10000006h	ID	ID Register	-
10000007h	CTL2	Control Register 2	00
10000008h	7IS	Level 7 Interrupt Status Register	-
10000009h	LIS	Local Interrupt Register	-
1000000Ah	7IE	Level 7 Interrupt Enable Register	-
1000000Bh	LIE	Local Interrupt Enable Register	00
1000000Ch	VIE	VMEbus Interrupt Enable Register	-
1000000Dh	IC10	Local Interrupts 1 and 0 Control	13
1000000Eh	IC32	Local Interrupts 3 and 2 Control	45
1000000Fh	IC54	Local Interrupts 5 and 4 Control	62

DARF64

Table 24: DARF64 Registers

ADDRESS	NAME	FUNCTION	INIT
18000000h	DMALAR	DMA Local Address Register	-
18000004h	DMAVAR	DMA VMEbus Address Register	-
18000008h	DMATC	DMA Transfer Count	-
1800000Ch	DCSR	Control and Status Register	-
18000010h	VMEBAR	VMEbus Slave Base Address Register	-
18000014h	RXDATA	Receive FIFO Data bits output latch	-
18000018h	RXADDR	Receive FIFO Address bits output latch	-
1800001Ch	RXCTL	Receive FIFO Control bits output latch	-
18000020h	BUSSEL	VMEbus Select	-
18000024h	IVECT	VMEbus Interrupt Vector	-
18000028h	APBR	Access Protect Boundary	-
1800002Ch	TXDATA	Transmit FIFO Data bits output latch	-
18000030h	TXADDR	Transmit FIFO Address bits output latch	-
18000034h	TXCTRL	Transmit FIFO Control bits output latch	-
18000038h	LMFIFO	Location Monitor FIFO read port	-
1800003Ch	MODE	Mode Control	-
18000040h	SA64BAR	Slave A64 Base Address Register	-
18000044h	MA64MAR	Master A64 Base Address Register	-
18000048h	LAG	Local Address Generator	-
1800004ch	DMAVTC	DMA VMEbus Transfer Count	-

EMULEX FAS216 SCSI Controller

Table 25: EMULEX FAS216 SCSI Controller Register Map

ADDRESS	READ FUNCTION	WRITE FUNCTION	INIT
0A000000h	Transfer Counter Low	Transfer Count Low	-
0A000001h	Transfer Counter Mid	Transfer Count Mid	-
0A000002h	FIFO	FIFO	-
0A000003h	Command	Command	-
0A000004h	Status	Select/Reselect Bus ID	-
0A000005h	Interrupt	Select/Reselect Time-out	-
0A000006h	Sequence Step	Synchronous Xfer Period	-
0A000007h	FIFO Flags	Synchronous Offset	-
0A000008h	Configuration 1	Configuration 1	07
0A000009h	Reserved	Clock Conversion Factor	05
0A00000Ah	Reserved	Test mode	-
0A00000Bh	Configuration 2	Configuration 2	20
0A00000Ch	Configuration 3	Configuration 3	03
0A00000Dh	Reserved	Reserved	-
0A00000Eh	Transfer Counter High	Transfer Count High	-
0A00000Fh	Reserved	Reserve FIFO Byte	-

68681 DUART

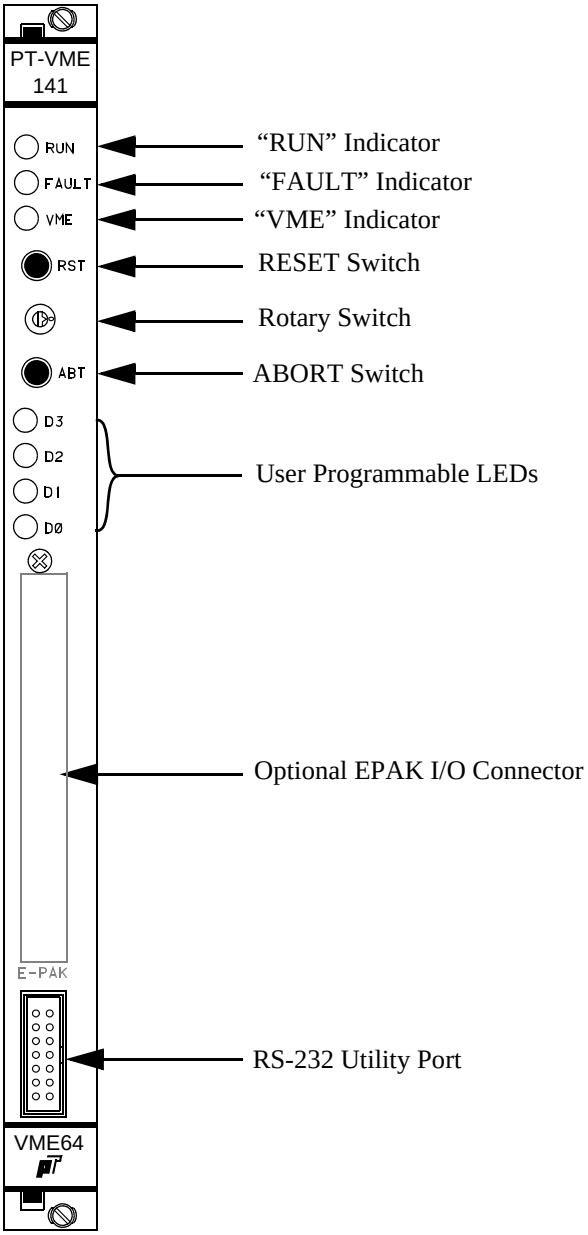
Table 26: Motorola 68681 DUART Register Map

ADDRESS	READ FUNCTION	WRITE FUNCTION	INIT
08000000h	Mode Register A	Mode Register A	13-07
08000001h	Status Register	Clock Select Register A	BB
08000002h	DO NOT READ	Command Register A	-
08000003h	Receiver Buffer A	Transmitter Buffer A	-
08000004h	Input Port Change Reg	Auxiliary Control Register	B0
08000005h	Interrupt Status Reg	Interrupt Mask Register	33
08000006h	Counter Mode: MSB	Counter/Timer Upper	-
08000007h	Counter Mode: LSB	Counter/Timer Lower	-
08000008h	Mode Register B	Mode Register B	13-07
08000009h	Status Register B	Clock Select Register B	BB
0800000Ah	DO NOT READ	Command Register B	-
0800000Bh	Receiver Buffer B	Transmitter Buffer B	-
0800000Ch	Interrupt Vector Reg	Interrupt Vector Reg	40
0800000Dh	Input Port (unlatched)	Output Port Config Reg	00
0800000Eh	Start-Counter Command	Output Port - Bit Set	FF
0800000Fh	Stop-Counter Command	Output Port - Bit Reset	00

Controls and Indicators

The figure below identifies the controls and indicators the reside on the PT-VME940 Front Panel.

Figure 5: PT-VME940 Front Panel Controls and Indicators



Rotary Switch

A hexadecimal rotary switch is provided for utility input purposes. The switch state is accessible to the firmware through the System Status Register.

"RUN" Indicator

The "RUN" indicator is a green LED which is illuminated whenever the module microprocessor is not reset and not halted.

"FAULT" Indicator

The "FAULT" indicator is a red LED, under program control, which provides a visual indication to the user that the software has detected an error condition and the VMEbus signal SYSFAIL* is asserted.

"VME" Indicator

This green indicator is illuminated during the period of a VMEbus master access attempt. The LED illumination intensity is a relative indication of the PT-VME940's VMEbus access frequency. A solid, bright light is indicative of high bus contention where the PT-VME940 is not receiving a Bus Grant.

RESET Switch

The reset switch is a red push button on the front panel which is tied to the EXTRST input pin of the ACC which in turn generates a board reset [-LRST].

ABORT Switch

The abort switch is a black push button on the front panel which is tied to the -L7I0(NMI) input pin of the ACC which in turn will generate a level 7 interrupt to the 68030.

User Programmable LEDs

Four user programmable LEDs are available on the front panel, labeled D0, D1, D2, and D3. They are programmed by software through bits in the System Control Register.

Jumper List

JUMPER	FUNCTION
K1	Disables Watchdog Reset
K2	U23 ROM/PROM socket configuration
K3	Reserved (factory configured)
K4	U28 ROM/PROM/SRAM socket configuration
K5	MMU Disable (for 68030 only)
K6	SCSI Term Power select (1-2 = local, open = SCSI bus)
K7	1M/4M DRAM select (1-2 = 4M, factory configured)
K8	1M/4M DRAM select (2-3 = 1M, factory configured)

Section

6

CONNECTOR PINOUTS

Utility Serial Port Pin Assignments

Connections to the Debug/Utility port can be made using the supplied cable. A Data Terminal Equipment RS-232C interface is provided. A transition cable is supplied which converts between the 14-pin header (P3) and a female shell (male pin) 25-pin D-Shell connector.

Table 27: Utility Serial Port Pin Assignments

DB 25 Pin	Dir	Circuit	P3 Pin	Description
1	-	AA	1	Protective Ground (Shield)
2	Out	BA	3	Port A Transmitted Data
3	In	BB	5	Port A Received Data
4	Out	CA	7	Port A Request To Send
5	In	CB	9	Port A Clear To Send
6	In	CC	11	Port A Data Set Ready
7	-	AB	13	Signal Ground (Common Return)
8-13				Unused
14	Out	SBA	2	Port B Transmitted Data (Secondary)
15			4	Unused
16	In	SBB	6	Port B Received Data (Secondary)
17			8	Unused
18			10	Unused
19			12	Unused
20	Out	CD	14	Port A Data Terminal Ready
21-25				Unused

VMEbus Pin Assignments

Table 28: VMEbus "P1" Connections

P1A	SIGNAL	P1B	SIGNAL	P1C	SIGNAL
1	D00	1	BBSY*	1	D08
2	D01	2	BCLR*	2	D09
3	D02	3	ACFAIL*	3	D10
4	D03	4	BG0IN*	4	D11
5	D04	5	BG0OUT*	5	D12
6	D05	6	BG1IN*	6	D13
7	D06	7	BG1OUT*	7	D14
8	D07	8	BG2IN*	8	D15
9	GND	9	BG2OUT*	9	GND
10	SYSCLK	10	BG3IN*	10	SYSFAIL*
11	GND	11	BG3OUT*	11	BERR
12	DS1*	12	BR0*	12	SYSRESET*
13	DS0*	13	BR1*	13	LWORD*
14	WRITE*	14	BR2*	14	AM5
15	GND	15	BR3*	15	A23
16	DTACK*	16	AM0	16	A22
17	GND	17	AM1	17	A21
18	AS*	18	AM2	18	A20
19	GND	19	AM3	19	A19
20	IACK*	20	GND	20	A18
21	IACKIN*	21		21	A17
22	IACKOUT*	22		22	A16
23	AM4	23	GND	23	A15
24	A07	24	IRQ7*	24	A14
25	A06	25	IRQ6*	25	A13
26	A05	26	IRQ5*	26	A12
27	A04	27	IRQ4*	27	A11
28	A03	28	IRQ3*	28	A10
29	A02	29	IRQ2*	29	A09
30	A01	30	IRQ1*	30	A08
31	-12V	31		31	+12V
32	+5V	32	+5V	32	+5V

Table 29: VMEbus" P2" Connections

P2A	SIGNAL	P2B	SIGNAL	P2C	SIGNAL
1	D0	1	+5V	1	GND
2	D1	2	GND	2	GND
3	D2	3	VRMC*	3	GND
4	D3	4	A24	4	GND
5	D4	5	A2	5	GND
6	D5	6	A26	6	GND
7	D6	7	A27	7	GND
8	D7	8	A28	8	GND
9	DP	9	A29	9	GND
10	GND	10	A30	10	GND
11	GND	11	A31	11	GND
12	GND	12	GND	12	GND
13	TPWR	13	+5V	13	
14	GND	14	D16	14	GND
15	GND	15	D17	15	GND
16	ATN	16	D18	16	GND
17	GND	17	D19	17	GND
18	BSY	18	D20	18	GND
19	ACK	19	D21	19	GND
20	RST	20	D22	20	GND
21	MSG	21	D23	21	GND
22	SEL	22	GND	22	GND
23	C/D	23	D24	23	GND
24	REQ	24	D25	24	GND
25	I/O	25	D26	25	GND
26		26	D27	26	GND
27		27	D28	27	GND
28		28	D29	28	GND
29		29	D30	29	GND
30		30	D31	30	GND
31		31	GND	31	GND
32		32	+5V	32	GND

VMEbus P2 connector rows A and C are User Definable connector pins. The PT-VME141 provides the connections identified above for the SCSI bus interconnect.

NOTE: VRMC* is a jumper (K3) selectable option. The IEEE 1014 Rev C VMEbus Specification defines this signal as "RESERVED".

Pin numbers without mnemonics are not used by the PT-VME141.

EPAK Connectors

The PT-VME141 EPAK module interface is comprised of connectors J1, J2, and J3, and the six EPAK standoffs.

Table 30: EPAK Connections

J1	SIGNAL	J2	SIGNAL	J3	SIGNAL
1	+12	1	+MPSZ0	1	+MPA24
2	-12	2	+MPSZ1	2	+MPA25
3	GND	3	+MPFC0	3	+MPA26
4	+MPA00	4	+MPFC1	4	+MPA27
5	+MPA01	5	+MPFC2	5	+MPA28
6	+MPA02	6	GND	6	+MPA29
7	+MPA03	7	+MPA08	7	+MPA30
8	+MPA04	8	+MPA09	8	+MPA31
9	+MPA05	9	+MPA10	9	GND
10	+MPA06	10	+MPA11	10	+MPD00
11	+MPA07	11	+MPA12	11	+MPD01
12	GND	12	+MPA13	12	+MPD02
13	+MPD24	13	+MPA14	13	+MPD03
14	+MPD25	14	+MPA15	14	+MPD04
15	+MPD26	15	GND	15	+MPD05
16	+MPD27	16	+MPA16	16	+MPD06
17	+MPD28	17	+MPA17	17	+MPD07
18	+MPD29	18	+MPA18	18	GND
19	+MPD30	19	+MPA19	19	+MPD08
20	+MPD31	20	+MPA20	20	+MPD09
21	GND	21	+MPA21	21	+MPD10
22	-EPSEL	22	+MPA22	22	+MPD11
23	-MPRMC	23	+MPA23	23	+MPD12
24	-MPUAS	24	GND	24	+MPD13
25	-MPUDS	25	+MPD16	25	+MPD14
26	-MPWRT	26	+MPD17	26	+MPD15
27	-EPSA0	27	+MPD18	27	GND
28	-EPIRQ	28	+MPD19	28	-MPSA0
29	-EPVIR	29	+MPD20	29	-MPSA1
30	-EPVIA	30	+MPD21	30	-MPBER
31	+EPKIO	31	+MPD22	31	-MPHLT
32	GND	32	+MPD23	32	-EPKPE
33	+MPCLK	33	GND	33	GND
34	-MPCLK	34	-EPSA1	34	-EPKBR
35	-MPRST	35	-EPERR	35	-MPBGA
36	-BDRST	36	+REFCK	36	-EPKBG

The EPAK mounting standoffs are used to carry power and ground to the EPAK module.

Mounting pin	SIGNAL
1	GND
2	+5V
3	GND
4	+5V
5	GND
6	GND

Table 31: EPAK mounting standoffs

SRAM Module

The SRAM Module standoff carries ground to the module. SRAM Module data signals [D<0-31>] are directly connected to Microprocessor Data bus [+MPD<0:31> and signals [A<2-21>] are directly connected to the Microprocessor Address bus [+MPA<2:21>. The signals [-CS<0:3>] are byte lane enables.]

Table 32: SRAM Module Connections

Pin	SIGNAL	Pin	SIGNAL
1	+5V	2	+5V
3	GND	4	GND
5	GND	6	GND
7	GND	8	GND
9	D0	10	A2
11	D1	12	A3
13	D2	14	A4
15	D3	16	A5
17	D4	18	A6
19	D5	20	A7
21	D6	22	A8
23	D7	24	A9
25	D8	26	A10
27	D9	28	A11
29	D10	30	A12
31	D11	32	A13
33	D12	34	A14
35	D13	36	A15

Table 32: SRAM Module Connections

Pin	SIGNAL	Pin	SIGNAL
37	D14	38	A16
39	D15	40	A17
41	D16	42	A18
43	D17	44	A19
45	D18	46	A20
47	D19	48	A21
49	D20	50	
51	D21	52	
53	D22	54	
55	D23	56	-CS0
57	D24	58	-CS1
59	D25	60	-CS2
61	D26	62	-CS3
63	D27	64	-WE
65	D28	66	
67	D29	68	SRSZ0
69	D30	70	SRSZ1
71	D31	72	
73	GND	74	GND
75	GND	76	GND
77	GND	78	GND
79	+5V	80	+5V

Section

7

MECHANICAL AND ENVIRONMENTAL

Power Requirements

The following values are without an EPAK installed.

Voltage	Typical	Maximum
PT-VME940-T +5V (±5%)	4.5 Amps	5.2 Amps
PT-VME940-U +5V (±5%)	4.0 Amps	4.7 Amps
+12V (±5%)	-	15 mA
-12V (±5%)	-	15 mA

Table 33: Power Requirements

Ambient Temperature

Use	Minimum	Maximum
Operating	0° C	+55° C
Storage	-55° C	+85° C

Table 34: Ambient Temperature

Humidity

Non condensing

Minimum	Maximum
0%	90%

Table 35: Humidity Constraints

Vibration

Designed to meet 5-100 Hz with 2g Acceleration.

Mechanical Shock

Designed to meet 20g for 6 ms (half sine).

Physical Dimensions

Base board only

Dimension	Millimeters	Inches
Width	234	9.2
Depth	160	6.3
Front Panel	20.3	.80
Component Height	13.5	.54

Table 36: Physical Dimensions

Section

8

APPENDICES

APPENDIX A: Product Warranty

Performance Technologies, Incorporated (hereinafter "PTI") warrants that its products sold hereunder will at the time of shipment be free from defects in material and workmanship and will conform to PTI's applicable specifications or, if appropriate, to Buyer's specifications accepted by PTI in writing. If products sold hereunder are not as warranted, PTI shall, at its option, refund the purchase price, repair, or replace the product provided proof of purchase and written notice of nonconformance are received by PTI within 12 months of shipment, or in the case of software and integrated circuits within ninety (90) days of shipment and provided said nonconforming products are returned F.O.B. to PTI's facility no later than thirty days after the warranty period expires. Products returned under warranty claims must be accompanied by an approved Return Material Authorization number issued by PTI and a statement of the reason for the return. Please contact PTI, or its agent, with the product serial number to obtain an RMA number. If PTI determines that the products are not defective, Buyer shall pay PTI all costs of handling and transportation. This warranty shall not apply to any products PTI determines to have been subject to testing for other than specified electrical characteristics or to operating and/or environmental conditions in excess of the maximum values established in applicable specifications, or have been subject to mishandling, misuse, static discharge, neglect, improper testing, repair, alteration, parts removal, damage, assembly or processing that alters the physical or electrical properties. This warranty excludes all cost of shipping, customs clearance and related charges outside the United States. Products containing batteries are warranted as above excluding batteries.

THIS WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES WHETHER EXPRESS, IMPLIED OR STATUTORY INCLUDING IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS. IN NO EVENT SHALL PTI BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES DUE TO BREACH OF THIS WARRANTY OR ANY OTHER OBLIGATION UNDER THIS ORDER OR CONTRACT.

APPENDIX B: Product Return Procedure

If you find that your Performance Technologies ("PTI") product must be returned for repair, note the following:

To return equipment, please obtain a Return Material Authorization (RMA) number. PTI cannot accept returns without an RMA number.

To obtain an RMA number, contact PTI's Customer Service Group at (716) 256-0200 (FAX: (716) 256-0791). Outside North America, Customers should contact their PTI agent. PTI requests the serial number of the unit and the reason for the return at the time the RMA is issued.

Return products should be shipped, prepaid, to:

Performance Technologies, Incorporated
Attn: Customer Service Group
315 Science Parkway
Rochester, N.Y. 14620, U.S.A.

(Customers outside of North America, contact your local PTI agent for return shipment instructions.) The RMA number should be marked on the outside of the shipping box to expedite correct handling at the PTI factory.

Repairs will be performed only on complete units. Return of incomplete equipment may delay repairs.

Please note that removal of original parts or product modification by a customer can void the warranty. (This does not apply to jumpers or socketed user programmable parts.)

"Out of warranty repairs" cannot proceed without a customer Purchase Order.

PTI will supply repair information on all returns.

PTI warrants all repairs for 90 days.

APPENDIX C: Installation Notes

NOTE: ELECTRONIC COMPONENTS ON PRINTED CIRCUIT BOARDS ARE EXTREMELY SENSITIVE TO STATIC ELECTRICITY. ORDINARY AMOUNTS OF STATIC ELECTRICITY GENERATED BY YOUR CLOTHING OR WORK ENVIRONMENT CAN DAMAGE THE ELECTRONIC EQUIPMENT. IT IS RECOMMENDED THAT WHEN INSTALLING THE PT-VME141 IN A SYSTEM OR THE COMPONENTS ON THE BOARD ITSELF THAT ANTI-STATIC GROUNDING STRAPS AND ANTI- STATIC MATS ARE USED TO HELP PREVENT DAMAGE DUE TO ELECTROSTATIC DISCHARGE.

NOTE: WHEN INSTALLING CHIPS INTO PROM SOCKETS, BE CERTAIN OF THEIR ORIENTATIONS. THE BOTTOM OF THE CHIP WILL BE ALIGNED WITH THE BOTTOM OF THE SOCKET. THE TOP OF THE SOCKET IS THE END CLOSEST TO THE VME CONNECTORS. PIN ONE OF THE CHIP SHOULD BE POINTING TOWARD THE VME CONNECTORS

NOTE: WHEN INSTALLING A 28 PIN DEVICE BE SURE THAT PIN 14 OF THE DEVICE ENTERS PIN 16 OF THE SOCKET (BOTTOM JUSTIFIED).

APPENDIX D: EEPROM Usage

PTI employs the Serial EEPROM to hold power-up and reset configuration information. The following table shows the usage and initial values that will be found in the EEPROM as a result of running factory testing of the PT-VME141.

The table is divided into two groups, locations 00-43h are used by PT-bug (however the information that they contain will probably be necessary for any application) and locations 44h-63h are used by OS-9 (when installed).

PTbug

The first four bytes of the EEPROM contains PTbug Magic Number. If the value is correct PTbug assumes that the rest of the locations that it uses are meaningful.

Byte locations 06h through 1Dh are used as initial values for the respective device registers.

The DARF64 requires that a reference to the location monitor be performed before it will respond as a slave to shared memory accesses. Byte location 1Eh contains a flag that determines whether the PT-VME141 will make this reference to itself (requiring that it accesses the VMEbus immediately after reset) or allows an appropriate driver make the initial reference.

Byte locations 20h through 2Fh are reserved by PTI for future use.

After reset, PTbug can perform Power On Confidence tests then launch a user application. This boot mechanism is defined in the PTbug User's Manual (811A0127xx) and uses locations 30h to 43h.

Two bytes (7Ch and 7Dh) are used by PTbug to store the ROM checksum. The Power On Confidence test uses this information to validate ROM integrity.

The last two locations (7Eh-7Fh) in the EEPROM are used by the Power On Confidence test to exercise the EEPROM read/write operation.

OS-9

PTI offers the OS-9™ Real-Time Operating System from Microware Systems Corporation for the PT-VME141. Locations 44h through 63h used by OS-9 if installed. For more information contact PTI or Microware. Address: Microware Systems Corporation; 1900 N. W. 114th Street; Des Moines, Iowa 50325. Phone number: (515) 224-1929.

Table 37: EEPROM Default Values

Address	Length	Default	Description
00	4 bytes	$01281955	PTbug Magic Number
04	2 bytes	$FFFF	Board Serial Number
06	4 bytes	$0060014C	DARF64 - VMEbus Base Address Register (VMEBAR)
0A	4 bytes	$00000001	DARF64 - Mode Control Register (MODE)

Table 37: EEPROM Default Values

Address	Length	Default	Description
0E	4 bytes	$00000001	DARF64 - Access Protect Boundary Register (APBR)
12	4 bytes	$00000040	DARF64 - VMEbus Interrupter Vector Register (IVECT)
16	1 byte	$1C	ACC - General Control Register (GENCTL)
17	1 byte	$00	ACC - Level 7 Interrupt Status Register (CTL2)
18	1 byte	$13	ACC - Local Interrupts 1 & 0 Control Register (IC10)
19	1 byte	$45	ACC - Local Interrupts 3 & 2 Control Register (IC32)
1A	1 byte	$62	ACC - Local Interrupts 5 & 4 Control Register (IC54)
1B	1 byte	$00	ACC - Local Interrupt Enable Register (LIE)
1C	1 byte	$00	ACC - VMEbus Arbiter Register (VARB)
1D	1 byte	$03	ACC - VMEbus Requester Register (VREQ)
1E	1 byte	$00	Flag To Access Location Monitor on Reset (1 - access, 2 - no access)
1F	1 byte	$07	SCSI I.D.
20	16 bytes		PTI Reserved
30	2 bytes	$B0BB	Boot Validation Word
32	2 bytes	$0007	Boot Flags (Bits 3 & 4 dependent on memory size)
34	4 bytes	$00000000	Source Address
38	4 bytes	$00000000	Destination Address
3C	4 bytes	$00000000	Transfer Byte Count
40	4 bytes	$00000000	Execute Address
44	2 bytes	$FACE	OS-9 Magic Word 1
46	2 bytes	$0000	Save Count
48	1 byte	$01	Number Of Floppy Drives
49	1 byte	$01	Number Of Hard Drives
4A	1 byte	$01	Boot Device
4B	1 byte	$01	Floppy Format
4C	8 bytes	“shell”	Shell String
54	2 bytes	$0400	Number Of 256 Byte RAM Disk Sectors
56	2 bytes	$0000	SCSI Master/Slave Boot (Slave)
58	6 bytes	XX XX XX XX XX	Ethernet Link-Level (Physical) Address
5E	4 bytes	147.139.6.9	Internet Address
62	2 bytes	$DEAD	OS-9 Magic Number 2
64	24 bytes		Not Used
7C	2 bytes	$XXXX	ROM Checksum (Used By PTbug)

Table 37: EEPROM Default Values

Address	Length	Default	Description
7E	2 bytes	$XXXX	Used By PTbug In Checking EEPROM

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SCHEMATICS

Signal name cross references are available upon request.

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