ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Find the *Ribbon / Performance Technologies PT-VME 141* at our website: ***Click HERE***

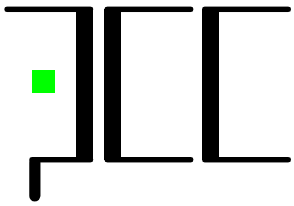
Performance Computer

A Performance Technologies Company
315 Science Parkway
Rochester, New York USA 14620

USER'S MANUAL

PT-VME151A/151AE

Extensible Single Board Computer/Controller



Document Number 126A0180

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Rev	ECN	Pages Affected	Date	Approvals
10	-	All	11/22/93	
11	Minor Rev	60	1/11/94	
20	080A000154	Schematic 1,15 (1 of 28)	4/22/94	
30	080A000179	Schematic 1,3,14 & 26	12/05/94	

REVISION CONTROL

When reviewing this document please note any issues that you may have with the document (errors, points of confusion, grammar or spelling mistakes, etc.) and contact Technical Publications at (716) 256-0200 or pccsupport@pt.com. All comments, suggestions, and criticisms are welcome.

Copyright Notice

© 1993-1994 by Performance Computer, a Performance Technologies Company. -- Printed in USA.
315 Science Parkway, Rochester, New York 14620

Trademarks

Microware and **OS-9** are trademarks of Microware Systems Corporation.

PTbug is a trademark of Performance Computer.

All other brands or names are trademarks of their respective holders.

All rights reserved. This document is the sole property of Performance Computer.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

NOTICE

This document presents information for users of the Performance Computer Models PT-VME151A Extensible Single Board Computer/Controller.

Although the information contained within this document is considered accurate and characteristic of the subject product, Performance Computer reserves the right to make changes to this document and any products described herein to improve reliability, function, or design. Performance Computer does not assume any liability arising out of the application or use of any product or circuit described herein.

No part of this document may be copied or reproduced in any form or by any means without the prior permission of Performance Computer.

WARNING

THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND, IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTION MANUAL, MAY CAUSE INTERFERENCE TO RADIO COMMUNICATIONS. AS TEMPORARILY PERMITTED BY REGULATION, IT HAS NOT BEEN TESTED FOR COMPLIANCE WITH THE LIMITS FOR CLASS A COMPUTING DEVICES PURSUANT TO SUBPART J OF PART 15 OF FCC RULES, WHICH ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST SUCH INTERFERENCE. OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE INTERFERENCE, IN WHICH CASE THE USER, AT HIS OWN EXPENSE, WILL BE REQUIRED TO TAKE WHATEVER MEASURES MAY BE REQUIRED TO CORRECT THE INTERFERENCE.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Safety Information

This section is provided as a summary of the safety recommendations throughout this manual. Performance Computer (PCC) recommends that all safety precautions are followed to prevent harm to yourself or the equipment. Please follow all warnings marked on the equipment.

Safety Precautions

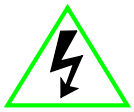
- Follow all warnings and instructions marked on the equipment.
- Ensure that the voltage and frequency of your power source matches the voltage and frequency inscribed on the equipments electrical rating label.
- Never push objects of any kind through the openings in the equipment. Dangerous voltages may be present. Conductive foreign objects could produce a short circuit that could cause fire, electrical shock, or damage your equipment.

Symbols

The following symbols appear in this document.



CAUTION: There is risk of personal injury or equipment damage. Follow the instructions.



WARNING: Hazardous voltages are present. To reduce the risk of electric shock and danger to personal heath, follow the instructions.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table of Contents

Section 1 INTRODUCTION 1

Scope 1

Applicable Documents 2

Model Designations 3

Features 4

Family Members 6

PT-VME131/131E 6
PT-VME141/141E 7
PT-VME151/151E 7

Glossary and Conventions 8

Glossary 8
Conventions 9

Section 2 GETTING STARTED 11

Unpacking and Inspection 11

Hardware Configuration 12

Device Positions 12
“Watchdog” Timer Setup 13
PROM/ROM/SRAM/EEPROM Socket Configuration 14
Location U23 Setup 15
Location U38 Setup 15
SCSI Termination 17
Disabling Termination 17
Termination Power Source 17
TERMPWR Overview 17
DRAM Module Upgrading 19
EPAK Installation 20

Board Installation 21

Power Considerations 21
Slot Considerations 21
Backplane Insertion 21

SCSI Considerations 23

Cabling 23
Example 23

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Mechanical restraints 24
SCSI device grounds 24
Device addresses 25
Serial Port Cabling 25
Example 25
Mechanical restraints 26
Section 3 FUNCTIONAL DESCRIPTION 27
Microprocessor 28
Memory 28
DRAM 28
DRAM Mapping 29
Sizing 29
Parity 30
Checking 30
Initialization 31
Testing 31
PROM/SRAM Sockets 31
Nonvolatile SRAM and Time of Day/Calendar Clock 31
Serial EEPROM 31
Interval Timer 32
VMEbus Interface 33
DARF64 33
VME*64* Transfers 33
Transfer Modes 33
Decoupled 34
Atomic 34
VMEbus Control Logic 34
VMEbus Slave Accesses 35
EPAK Access from the VMEbus 35
VMEbus Master Accesses 35
68040 Accesses 35
Read-Modify-Write 36
DMAC 36
Location Monitor 37
Registers 37
Test and Diagnostics 37
ACC 38
Reset 38
Local Bus Timer 38
Watchdog Timer 38
Tick Timer 39
Register Block 39

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Interrupt Handler 39
Local Level 7 Sources 39
Abort 40
SCSI Bus Reset 40
AC Fail 40
System Fail 40
General Purpose Local Interrupts 40
Location Monitor FIFO 41
DARF64 VME Event 41
Timer Event 41
Tick 42
Interval 42
I/O Event 42
FAS216 Requests 42
EPAK Requests (-EPIRQ) 42
EPAK Vectored Interrupt Request 43
DUART Interrupt Request (-INTP<5>) 43
VMEbus Interrupts 43
Interrupt Acknowledgment 44
VMEbus Requester 44
System Monitor Functions 44
Reset 44
System Clock Driver 44
VMEbus Arbiter 44
IACK Daisy Chain Driver 45
Bus Timer 45

I/O UTILITIES 45

System Control Registers 45
System Control Register 1 45
VMEbus Page Select 46
User LEDs 46
SCSI DMA Read/Write Direction 46
EPAK Space Cache Enable 46
VMEbus Space Cache Enable 46
System Control Register 2 47
Enable EPAK Access from the VMEbus 47
Enable Parity Error Checking 47
Enable Bad Parity 47
Enable Interval Timer Interrupts 49
Enable Tick Timer Interrupts 49
System Status Registers 50
System Status Register 1 50
Hex Switch 50
System Status Register 2 50
68040 Parity Error 50

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SCSI DMA Parity Error 50
DARF Parity Error 50
EPAK Parity Error 51
SCSI Present 51
System Status Register 3 51
DRAM Size 51
Parity Installed 51
Interval Timer Interrupt Pending 51
DUART 52
Utility Serial Ports 52
General Purpose Timer/Counter 52
Parallel Input Port 52
Clear-to-Send 52
Data-Terminal-Ready 52
EPAK General Purpose Input 53
Serial EEPROM Data In 53
Parallel Output Port 53
Request-to-Send 53
Data-Set-Ready 53
EPAK General Purpose Output 53
Serial EEPROM Select 53
Serial EEPROM Control 53
Serial EEPROM Data Out 54
SCSI Controller 55
SCSI Bus 55
Register Access 55
DMA Mechanism 56
Interrupts 56
Termination 56
EPAK Interface 58
Section 4 FUNCTIONAL SUMMARY 59
Memory Map 59
Default VMEbus Slave Addressing 60
151A System Registers 61
System Control Register 1 61
System Control Register 2 63
System Status Register 1 64
System Status Register 2 65
System Status Register 3 66
SCSI Memory Address Register 67
Jumper List (Defaults) 67

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Interrupt Control 68
Register Maps 69
ACC 69
DARF64 70
DS1643 Nonvolatile Timekeeping RAM 71
82C54 Interval Timer 71
EMULEX FAS216 SCSI Controller 72
68681 DUART 72
Controls and Indicators 73
Rotary Switch 73
“RUN” Indicator 74
“FAULT” Indicator 74
“VME” Indicator 74
RESET Switch 74
ABORT Switch 74
User Programmable LEDs 74

Section 5 CONNECTOR PINOUTS 75

Utility Serial Port Pin Assignments 75
VMEbus Pin Assignments 76
EPAK Connectors 78
DRAM Module 79

Section 6 MECHANICAL AND ENVIRONMENTAL 81

Power Requirements 81
Ambient Temperature 81
Humidity 81
Vibration 81
Mechanical Shock 82
Physical Dimensions 82

Section 7 APPENDICES 83

Product Warranty 83
Product Return Procedure 84
Installation Notes 85
EEPROM Usage 86
PTbug 86
OS-9 87

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

The differences between the PT-VME151A and the VME151 89
Renamed Registers 89
New Devices 89
DRAM Sizing 89
SRAM Access 90
PT-VME151A Differences From VME131/141 91
DARF64 uses 68040 mode 91
SCSI Controller differences 91
Effects of 68040 vs. 68030 91
Cacheability and Serialization 91
68040 Cache Control Registers 92
68040 Cache Clearing 93
68040 Exception Processing 93
PT-VME151A Control Register Differences 93
AVICS Overview 95
Functional Description 95
BI-mode 95
Location Monitor 96
VMEbus Master Memory Map 96
Master VMEbus Accesses 98
Slave VMEbus Accesses 99
AVICS Application Notes 101
Local Interrupts 101
Example: 101
Setting Up the Master Bus Memory Map 102
Example: 102
Setting Up A24/A32 Slave Images on the Bus 102
Example A: 103
Example B: 104
Generating VMEbus Interrupts 105
Example: 105
Receiving VMEbus Interrupts 105
Example: 105
Initiating a DMA Transfer 106
Example: 106
VMEbus Address Modifiers 108
Section 8 INDEX 109
Section 9 SCHEMATICS 115

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

List of Figures

Figure 1: PT-VME151A/151AE Device Positions 12
Figure 2: EPROM/ROM/SRAM/EEPROM Device Orientation 14
Figure 3: K4 and K10Jumpers 15
Figure 4: K3 and K11 Jumpers 15
Figure 5: U23 and U38 Jumper Settings 16
Figure 6: SCSI Components 17
Figure 7: PT-VME151A Front Panel 22
Figure 8: Example SCSI Cable 24
Figure 9: Example Serial port Cable 26
Figure 10: Block Diagram 27
Figure 11: Interval Timer Block Diagram 32
Figure 12: Timer Block Diagram 41
Figure 13: PT-VME151A Front Panel Controls and Indicators 73
Figure 14: DARF Memory Map 97

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

List of Figures

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

List of Tables

Table 1: EPAK Caching Options 46
Table 2: Memory Map 59
Table 3: Default VMEbus A24 Memory Map 60
Table 4: Default VMEbus A32 Memory Map 60
Table 5: Interrupt Request Summary 68
Table 6: ACC Register Map 69
Table 7: DARF64 Registers 70
Table 8: DS1643 Nonvolatile Timekeeping RAM Registers 71
Table 9: 82C54 Interval Timer Registers 71
Table 10: EMULEX FAS216 SCSI Controller Register Map 72
Table 11: Motorola 68681 DUART Register Map 72
Table 12: Utility Serial Port Pin Assignments 75
Table 13: VMEbus “P1” Connections 76
Table 14: VMEbus” P2” Connections 77
Table 15: EPAK Connections 78
Table 16: EPAK mounting standoffs 79
Table 17: DRAM Module Connections 79
Table 18: EPAK mounting standoffs 80
Table 19: Power Requirements 81
Table 20: Ambient Temperature 81
Table 21: Humidity Constraints 81
Table 22: Physical Dimensions 82
Table 23: EEPROM Default Values 87
Table 24: 151 to 151A Register Map DIfferences 89
Table 25: EPAK Caching 93
Table 26: Recommended Interrupt Assignments 101
Table 27: VMEbus Address Modifiers 108

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

List of Tables

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Section

1

INTRODUCTION

Scope

This document provides information for users of the Model PT-VME151A and PT-VME151AE Extensible Single Board Computer/Controllers.

This manual is not intended as a stand-alone document. If you plan on writing software for the board or developing an Expansion Module the references cited below in the Applicable Documents section are necessary.

This manual does provide the information necessary to understand the operation and features of the board. A prime objective was to answer those questions raised by system developers as to whether the PT-VME151A/151AE will complement their architecture. When combined with the supporting documentation listed below, a complete description of PT-VME151A/151AE facilities are presented.

Section 1 Provides an introduction and general overview of the PT-VME151A. It is intended as a quick summary of PT-VME151A/151AE features and provides a framework for the rest of the document.

Section 2 (Getting Started) describes the physical setup and installation procedures.

Section 3 The Functional Description provides a detailed description of PT-VME151A/151AE architecture and functional blocks.

Section 4 Summarizes the PT-VME151A/151AE memory map, registers, controls, indicators, etc.

Section 5 (Connector Pinouts) summarizes the PT-VME151A/151AE external connections.

Section 6 Describes mechanical and environmental characteristics of the PT-VME151A/151AE.

Section 7 Appendices.

Section 8 Index.

Section 9 Schematics.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Applicable Documents

a. VMEbus Specification Manual, Revision ANSI/IEEE STD 1014-1987, VMEbus International Trade Association (VITA). VITA; 10229 N. Scottsdale Road, Suite B; Scottsdale, AZ 85253.

b. M68000 Family Programmer's Reference Manual; M68000PM/AD; Motorola Incorporated, 1989. Motorola Literature Distribution; P.O. Box 20912; Phoenix, AZ 85036.

c. MC68040, MC68EC040, MC68LC040 Microprocessor User's Manual; M68040UM/AD; Motorola Incorporated, 1992. Motorola Literature Distribution; P.O. Box 20912; Phoenix, AZ 85036.

d. MC68040 Designers Handbook; MC68040DH/AD; Motorola Incorporated, 1990. Motorola Literature Distribution; P.O. Box 20912; Phoenix, AZ 85036.

e. MC68681 Multi-Function Peripheral Specification (DUART); September, 1985. Motorola Semiconductor Products Incorporated; 3501 Ed Bluestein Boulevard; Austin, TX 78721.

f. PT-VME131/141/151 Expansion Module Design Guide; Document Number 126A0075, Performance Technologies, Incorporated.

g. 93C46 Data Sheet; Catalyst Semiconductor, Inc. or International CMOS Technology, Inc.

h. FAS216/226/236 Technical Manual; VLSI51007-00 Rev A, January 4,1991. Emulex Micro Devices; 3545 Harbor Boulevard; Costa Mesa, CA 92626.

i. Intel Peripherals Handbook; Literature Order Number 296467. Intel Corporation, Literature Sales; P.O. Box 7641; Mt. Prospect, IL 60056-7641.

j. Openbus Interface Components - VMEbus User Manual; Issue 1; Document: 891014.MD300.02. Newbridge Microsystems; 603 March Road; Kanata, Ontario, Canada K2K 2M5.

k. Dallas Semiconductor, 1992-1993 Product Data Book. DS1643 Nonvolatile Timekeeping RAM. Dallas Semiconductor; 4401 South Beltwood Parkway; Dallas, Texas 75244-3292.

l. American National Standard for Information System - Small Computer System Interface (SCSI), ANSI X3.131-1986. American National Standard for Institute, Inc.; 1430 Broadway; New York, New York 10018.

Information regarding EPAKs is provided in a separate User's Manual for the specific EPAK.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Model Designations

The PT-VME151A is available with a 25 MHz 68040 microprocessor or a 25 MHz 68EC040 (68040 without MMU or FPU). Additionally, the PT-VME151A has options of 4, 8, 16, 32 or 64 megabytes of main memory. Model designations are as follows:

Model PT-VME151A-10439	68040-25MHz, 4 Mbyte
Model PT-VME151A-10440	68040-25MHz, 8 Mbytes
Model PT-VME151A-10441	68040-25MHz, 16 Mbytes w/ parity
Model PT-VME151A-10442	68040-25MHz, 32 Mbytes w/ parity
Model PT-VME151A-10443	68040-25MHz, 64 Mbytes w/ parity
Model PT-VME151AE-10444	68EC040-25MHz, 4 Mbyte
Model PT-VME151AE-10445	68EC040-25MHz, 8 Mbytes
Model PT-VME151AE-10446	68EC040-25MHz, 16 Mbytes w/ parity
Model PT-VME151AE-10447	68EC040-25MHz, 32 Mbytes w/ parity
Model PT-VME151AE-10448	68EC040-25MHz, 64 Mbytes w/ parity

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Features

- MC68040 Thirty-Two Bit Microprocessor With Internal Cache and FPU
  - PT-VME151 utilizes 25 MHz MC68040 MPU w/Memory Management Unit
  - PT-VME151E utilizes 25 MHz MC68EC040 MPU w/o MMU or FPU
  - MC68030-Compatible Integer Execution Unit
  - MC68881/MC68882-Compatible Floating Point Unit
  - Independent Instruction and Data Memory Management Units
  - 4KByte Physical Instruction Cache and 4KByte Physical Data Cache Accessible Simultaneously
  - Low Latency Bus Accesses for Reduced Cache-Miss Penalty
  - Concurrent Integer Unit, FPU, MMU, and Bus Controller Operation Maximizes Throughput
  - User Object-Code Compatibility with all Earlier M68000 Microprocessors
- 4, 8, 16, 32 or 64 Megabytes of Shared DRAM
  - 4 Clock Local Access
  - 68040 Cache Burst Read Mode (4-2-2-2 Clock Timing)
- Parity Checking
  - For 16, 32 or 64 Megabyte configurations
- Two 32 Pin JEDEC Sockets (Bytewide Port)
  - Both sockets support ROM, PROM, EPROM, and Flash EPROM devices
  - One socket is additionally capable of supporting SRAM and RTC devices
- Flexible EPAK Interface Extension Capability
  - Supports Slave, DMA, and Buffered DMA I/O Functions
  - Options for Ethernet, High Speed SYNC SIO, High Density ASYNC SIO, etc.
  - Front Panel Interconnect
- VME*64*™ VMEbus Interface Features
  - Advanced Control Circuit (ACC) ASIC
    - Full VMEbus System Controller w/Auto-Program Option
    - VMEbus Requester, Interrupter, and Interrupt Handler
    - Tick and Watchdog Timers, General Purpose Clocks
  - Data/Address Register File (DARF64) ASIC
    - 60 MByte per second D64MBLT (VME*64*) Data Transfer Rate
    - VMEbus A64/A32/A24/A16 Address Interface
    - VMEbus D64MBLT/D32BLT/D16BLT/D32/D16/D8(EO), UAT, RMW Data Interface
    - Location Monitor w/Message FIFO
    - Programmable Slave Address Mapping And Protection
    - Integral A32:D32 Local DMA Controller w/Burst Capabilities
    - Programmable Burst Sizes on Local Bus DMA Operations
- Fast SCSI-2 Single Ended Interface Based Upon EMULEX FAS216
  - Supports ANSI X3.131-1986 and X3T9.2/86-109 Rev. 10c Standards
  - 10 MByte per second SCSI Data Transfer Rate
  - Active SCSI bus termination
  - DMA Support To Local DRAM
  - P2 SCSI Interconnect
- 82C54 CHMOS Programmable Interval Timer
  - Three independent 16-bit counters
  - Provides Interrupt

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

- General Purpose Local I/O
  - 68681 DUART
    - Dual RS-232 ASYNC Serial I/O ports w/Front Panel Interconnect
    - 16-bit General Purpose Timer
  - 128 Byte EEPROM
- DS1643 Nonvolatile Timekeeping RAM
  - 8184 Bytes of Nonvolatile SRAM
  - Real-Time Clock with Integrated Crystal
  - Power Fail Control Circuit
  - Lithium Energy Source
- Front Panel User Interface Features
  - Reset and Abort Switches
  - General Purpose Hexadecimal Switch
  - 68040 (RUN) and VMEbus (VME) Activity LED indicators
  - User Programmable FAULT LED
  - Four User Programmable LEDs
- Software Support
  - PTbug Debugger/Monitor
  - OS-9 Real-Time Operating System
  - VxWorks Real-Time Operating System

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Family Members

The PT-VME151A and PT-VME151AE are members of a family of PTI Extensible Single Board Computer/Controllers. They each represent a highly integrated M68000-compatible MPU based VMEbus platform designed to offer the user significant flexibility in meeting specific architectural requirements.

The base modules support all standard VMEbus data and operating modes including the newly defined VME*64* mode pioneered by Performance Technologies. Operating in VME*64* mode the PT-VME151A can burst data over the VMEbus at rates up to 60 MBytes per second. This high speed transfer capability makes the 151A ideal for applications that require maximum VMEbus utilization. The base modules provide many I/O features tightly coupled to the MPU. These features include five DRAM capacities from four to sixty-four megabytes, a Fast SCSI-2 interface with DMA support for direct flexible/hard disk interconnect, and dual serial I/O ports for asynchronous communication connectivity.

In addition to the standard base module features, the PTI specs provide an option for even further extending their single VMEbus slot functionality through its “EPAK” extension interface. This interface provides for the addition of a plug-in daughterboard (EPAK) with selectable functionality to meet current or future I/O needs. Performance Technologies offers “off-the-shelf” EPAKs which support Ethernet, high speed synchronous communications, additional asynchronous serial I/O, etc. If these EPAKs do not match the requirements, the user also has the option for a custom design based upon an available wire wrap prototyping EPAK and supplied interface documentation. Contact Performance Technologies for custom EPAK design quotations.

A key design criterion was to maintain user software compatibility across the family members. The command and register set of the EMULEX SCSI controller on the PT-VME151A and PT-VME141 is a super set of the PT-VME131’s NCR SCSI controller. The MC68040 of the PT-VME151 is user code compatible with the MC68030 of the PT-VME131 and PT-VME141. These and other design considerations were made to preserve your investment in code development. See “PT-VME151A Differences From VME131/141” on page 91 for a discussion of the system level differences.

PT-VME131/131E

The features of the PT-VME131 and PT-VME131E are identical to the PT-VME151A with the following exceptions:

- Advanced Thirty-Two Bit Microprocessor With Internal Cache
  - PT-VME131 utilizes 25 MHz 68030 MPU w/MMU
  - PT-VME131E utilizes 25 MHz 68EC030 MPU w/o MMU
- 1, 2, 4, or 8 Megabytes of Shared DRAM
- Data/Address Register File (DARF32) ASIC (not VME*64*)
  - VMEbus Master/Slave A32/A24/A16:D32/D16/D8(EO) Interface
  - Location Monitor with Message FIFO
  - Programmable Slave Address Mapping and Protection
  - Integral A32:D32 Local Bus to the VMEbus DMA Controller
- SCSI-I Single Ended Interface
  - NCR 53C94 Based
  - 16 Bit DMA support to local DRAM
  - P2 SCSI Interconnect

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

- No 82C54 CHMOS Programmable Interval Timer
- No DS1643 Nonvolatile Timekeeping RAM

PT-VME141/141E

The PT-VME141 and PT-VME141E were designed as the VME*64* entry level members of the family. Their features are described in this manual and summarized in the previous section.

These boards make the step into the newly defined VME*64* mode pioneered by Performance Technologies. Operating in VME*64* mode the PT-VME141 can burst data over the VMEbus at rates up to 60 MBytes per second. This high speed transfer capability makes the 141 ideal for applications that require maximum VMEbus utilization.

The features of the PT-VME141 and PT-VME141E are identical to the PT-VME151A with the following exceptions:

- Advanced Thirty-Two Bit Microprocessor With Internal Cache
  PT-VME141 utilizes 25 MHz 68030 MPU w/MMU
  PT-VME141E utilizes 25 MHz 68EC030 MPU w/o MMU
- 1, 2, 4, or 8 Megabytes of Shared DRAM
- 256 Kbytes or 1 Mbyte Of Optional SRAM
  2 Clock Local Access
  68040 Cache Burst Read Mode (2-1-1-1 Clock Timing)
- No 82C54 CHMOS Programmable Interval Timer
- No DS1643 Nonvolatile Timekeeping RAM

PT-VME151/151E

As the top performers in the family the PT-VME151 and PT-VME151E utilize the Motorola MC68040 and MC68EC040, respectively. The MC68040 is Motorola's third generation of M68000-compatible, high performance, 32-bit microprocessors that offers approximately twice the processing power of the MC68030 running at the same clock rate.

The features of the PT-VME151 and PT-VME151E are identical to the PT-VME151A with the following exceptions:

- 1, 2, 4, or 8 Megabytes of Shared DRAM
  3 Clock Local Access
  68040 Cache Burst Read Mode (3-2-2-2 Clock Timing)
- 256 Kbytes or 1 Mbyte Of Optional SRAM
  2 Clock Local Access
  68040 Cache Burst Read Mode (2-1-1-1 Clock Timing)
- No 82C54 CHMOS Programmable Interval Timer

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Glossary and Conventions

Glossary

ACC - Advanced VMEbus System Architecture Control Circuit (CA91C014).

CPU - Central Processing Unit (MC68040 or MC68EC040)

DARF64 - Data Address Register File (CA91C064).

DMA - Direct Memory Access, hardware controller block data transfers.

DMAC - Direct Memory Access Controller.

DRAM - Dynamic Random Access Memory.

longword - In this manual, this term indicates a 32-bit value.

MByte - Megabyte.

ms. - Millisecond.

reserved - The term used for bits, bytes, fields, code values, etc. that are set aside for future use.

RTC - Real Time Clock.

SCSI - Small Computer System Interface.

word - In this manual, this term indicates a 16-bit value.

xxh - Numbers followed by lowercase h are hexadecimal values. All other numbers are decimal values.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Conventions

Upper case names enclosed in square brackets ([,]) represent signal names that can be found in the schematics.

Numbers enclosed in “less than” (<) and “greater than” (>) symbols refer to individual bits of a signal bus. i.e. +MPA<0> represents a the least significant bit of the 32 bit MicroProcessor Address bus. +MPA<0:31> represents all signals associated with the MicroProcessor Address bus.

Device pins are referenced with a Reference Designator, hyphen, pin number. i.e. U52-30 indicates pin 30 of location U52.

A Jumper Block can contain one or many individual Jumpers. If a Jumper Block contains more than two pins then the individual Jumpers consist of three pin groups starting with pin 1. (i.e., Jumper 1 is comprised of pins 1 through 3, Jumper 2 is comprised of pins 4 through 6, etc.) The individual Jumpers in a Jumper Block are referenced with the Jumper Block Reference Designator, underscore, and Jumper number. (i.e., K6_2 indicates jumper 2 of Jumper block K6.) The individual pins in a Jumper Block (or Jumper) are referenced with a Reference Designator, hyphen, pin number. (i.e., K7-30 indicates pin 30 of Jumper Block K7 (or Jumper K7_10).)

VMEbus signal pins are referenced with the Connector Designator, hyphen, Row Designator, Pin number. (i.e., P2-B3 refers to Pin 3 of Row B on the VMEbus “P2” connector.)

Throughout this document references to the Motorola MC68040 processor also imply the MC68EC040. Specific differences will be cited as necessary.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Section

2

GETTING STARTED

Unpacking and Inspection



CAUTION: ELECTRONIC COMPONENTS ON MODERN PRINTED CIRCUIT BOARDS ARE EXTREMELY SENSITIVE TO STATIC ELECTRICITY. ORDINARY AMOUNTS OF STATIC ELECTRICITY GENERATED BY YOUR CLOTHING OR WORK ENVIRONMENT CAN DAMAGE THE ELECTRONIC EQUIPMENT. IT IS RECOMMENDED THAT WHEN INSTALLING THE PT-VME151A IN A SYSTEM OR THE COMPONENTS ON THE BOARD ITSELF THAT ANTI-STATIC GROUNDING STRAPS AND ANTI-STATIC MATS ARE USED TO HELP PREVENT DAMAGE DUE TO ELECTROSTATIC DISCHARGE.

The shipping carton should be inspected for any possible damage that may have occurred during shipment. If there is any physical damage to the package you have opened, immediately contact the Shipping Carrier and/or Performance Technologies, Incorporated.

If this shipment is being received outside the United States or Canada and there is damage to the package, contact your local distributor or agent.

If there is shipping damage, failure to make an immediate claim may void any insurance coverage.

If no external damage is visible, carefully unpack contents from shipping carton, observing anti-static precautions identified above and verify against packing list. Inspect the PT-VME151A for any visible signs of shipping damage. If such physical damage is noted, report it immediately to Performance Technologies or appropriate agent. DO NOT PROCEED with any further configuration or installation.

NOTE: If any damage is detected follow the Product Return Procedure described in the appendix.

If no damage is visible, check that all socketed parts are firmly seated. Occasionally parts work themselves loose or partially out of their sockets during the shipping process. Reseat any loose devices by placing the printed circuit board on a flat surface and pressing firmly down on the part. If a part has worked itself completely free of the board (a highly unlikely event) be sure to verify its position and orientation before reinsertion. Check that all mounting screws of attached assemblies are tight.

The serial number can be found stamped on the solder side of the PCB along the edge closest to the front panel. A printed label identifying the assembly revision level can be found on the component side of the “P1” connector. See “PT-VME151A/151AE Device Positions” on page 12.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Hardware Configuration

A layout for the PT-VME151A/151AE is shown in “Figure 1: PT-VME151A/151AE Device Positions”. The model PT-VME151A and PT-VME151AE are two versions of the same PCB with different component options. There are various jumpers to configure user options which must be set before initial bootup. Refer to the information in this section to verify that you have the correct settings.

Device Positions

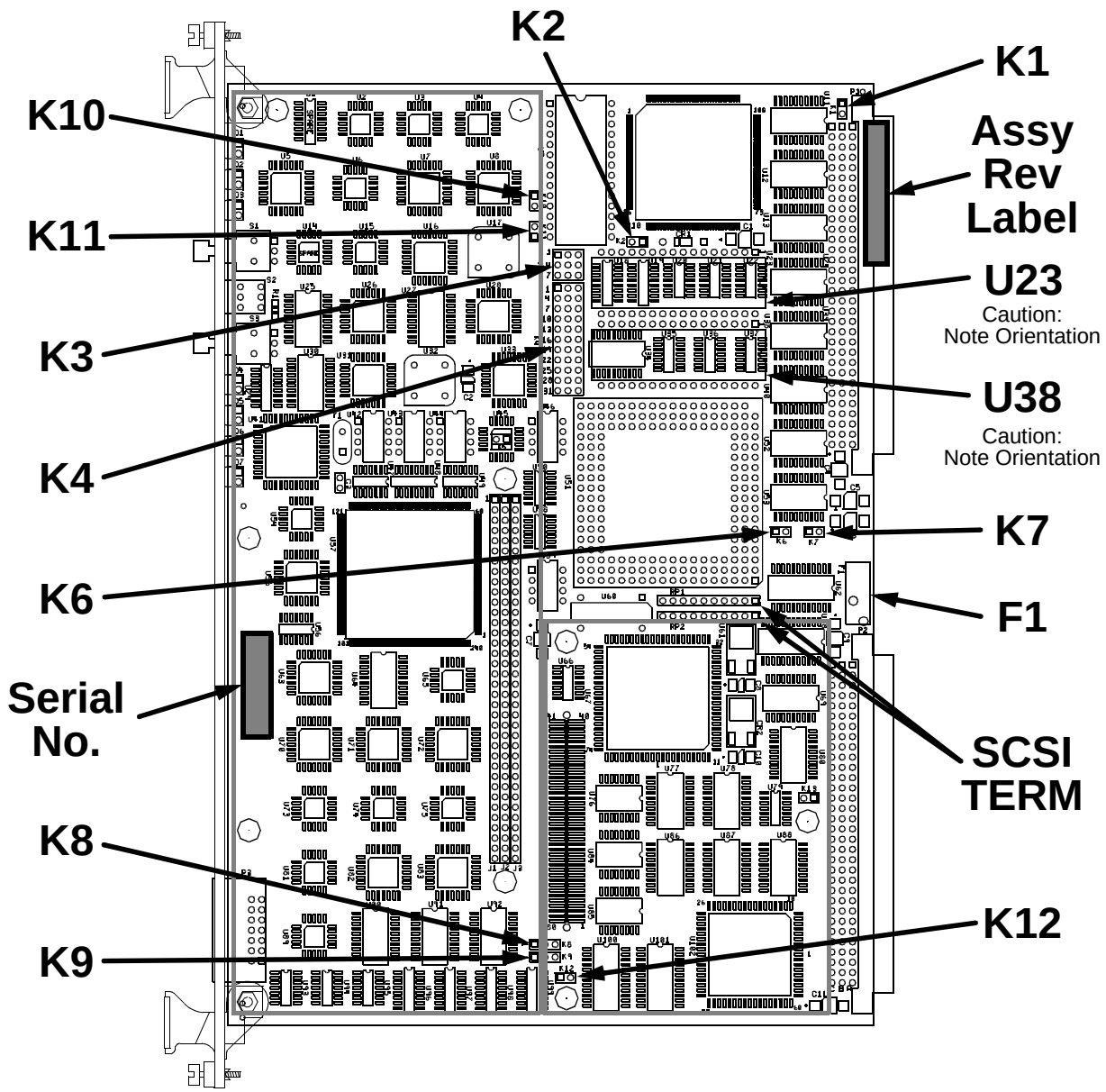
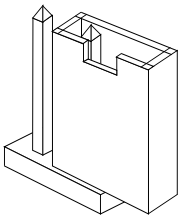


Figure 1: PT-VME151A/151AE Device Positions

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com



All Jumper Blocks are designed to mate with standard 2 pin jumper shunts. Spare jumper shunts can be stored by slipping one side of the jumper shunt on a single, unused pin of a jumper block and allowing the other side of the jumper shunt to hang in space. As shown at left:

“Watchdog” Timer Setup

If the ACC “watchdog” timer function is desired remove jumper shunt at location K1. Once enabled the “watchdog” timer will cause a local reset to occur, unless reset every two seconds by software. Jumper Block K1 consists of a single pair of pins that is either open or shorted. See “Figure 1: PT-VME151A/ 151AE Device Positions” on page 12.



CAUTION: Before enabling this function be sure that your installed software supports it. Unexpected local resets could occur.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

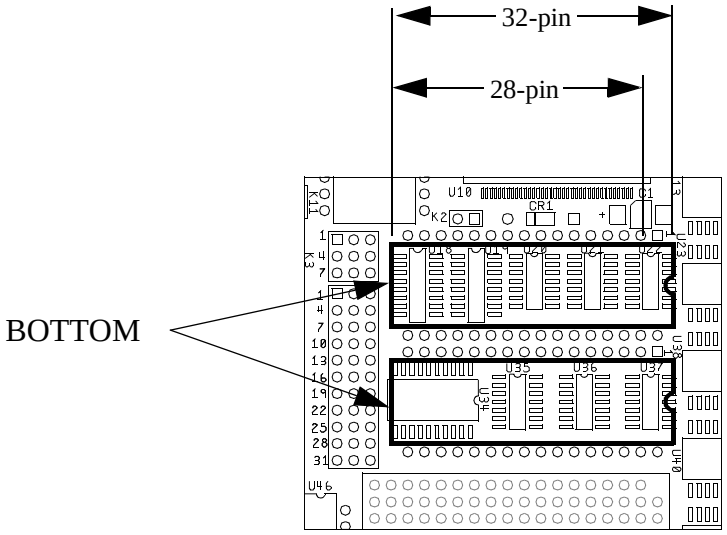
PROM/ROM/SRAM/EEPROM Socket Configuration

Locations U23 and U38 both provide support for read only devices such as ROM, PROM, EPROM, and Flash EPROM. Location U23 has additional support for read/write devices as well, SRAM and non-volatile SRAM.

The positions of locations U23 and U38 are identified in Figure 1: on page 12 and Figure 2: on page 14.

Both locations are capable of supporting 32 or 28 pin devices. The figure below demonstrates the necessary pin alignment for the respective devices. See CAUTIONS below!

Figure 2: EPROM/ROM/SRAM/EEPROM Device Orientation



CAUTION: WHEN INSERTING 28 OR 32 PIN DEVICES INTO LOCATIONS U23 OR U38 NOTE THE ORIENTATION OF THE CHIP! THE BOTTOM OF THE CHIP WILL BE ALIGNED WITH THE BOTTOM OF THE SOCKET STRIPS. THE “BOTTOM” OF THE SOCKET STRIPS ARE THE ENDS FURTHEST FROM THE VME CONNECTORS. PIN 14 OF A 28 PIN DEVICE SHOULD ENTER PIN 16 OF THE SOCKET.

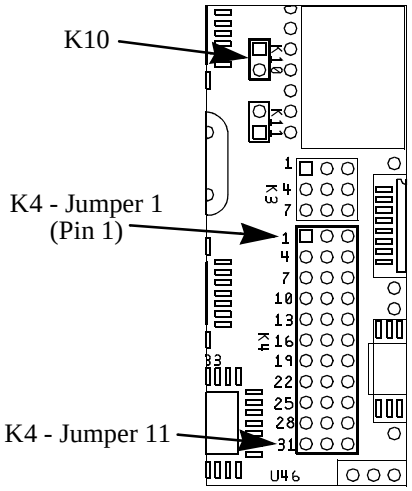
CAUTION: PIN ONE OF THE CHIP SHOULD BE POINTING TOWARDS THE VME CONNECTORS.

CAUTION: THE DEVICE MUST HAVE AN ACCESS TIME OF LESS THAN OR EQUAL TO 200 NS.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Location U23 Setup

Figure 3: K4 and K10Jumpers



The pin out configuration for location U23 is defined by Jumper Blocks K4 and K10. There are eleven jumpers at location K4 and a single jumper at K10.

Each K4 jumper position consists of a row of three adjacent pins. The Jumpers are numbered from 1 to 11 starting with Jumper 1 at the pin 1 end of the Jumper Block K4. In figure 3, pin 1 is in the upper left corner. K4 pins are numbered from left to right and top to bottom.

There are three possible states for each jumper: the center pin shorted to the left pin (bottom justified jumper shunt in figure 5), the center pin shorted to the right pin (top justified jumper shunt in figure 5), or all three pins unconnected (no jumper shunt in figure 5).

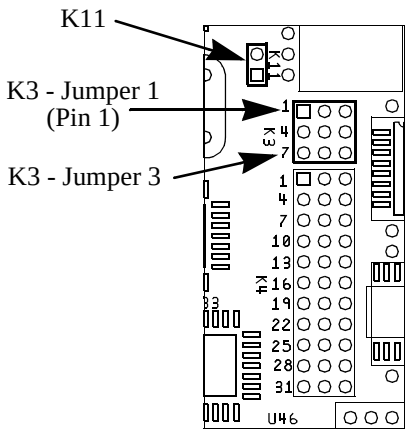
Jumper Block K10 is a simple two pin jumper where the pins are either open or shorted.

The orientation of figure 3 is with the VMEbus connectors on the right.

Figure 5 displays a schematic representation of K4 and K10 jumpers for typical U23 configurations.

Location U38 Setup

Figure 4: K3 and K11 Jumpers



The pin out configuration for location U38 is defined by Jumper Blocks K3 and K11. There are three jumpers at location K3 and a single jumper at K11.

Each K3 jumper position consists of a row of three adjacent pins. The Jumpers are numbered from 1 to 3 starting with Jumper 1 at the pin 1 end of the Jumper Block K3. In figure 4, pin 1 is in the upper left corner. The pins are numbered from left to right and top to bottom. The orientation of figure 4 is with the VMEbus connectors on the right.

There are two possible states for each jumper: the center pin shorted to the right pin (bottom justified jumper shunt in figure 5) or the center pin shorted to the left pin (top justified jumper shunt in figure 5).

Jumper Block K11 is a simple two pin jumper where the pins are either open or shorted.

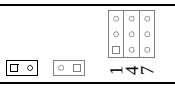
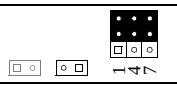
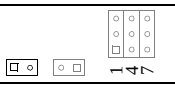
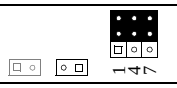
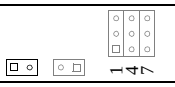
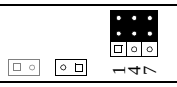
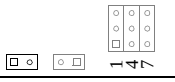
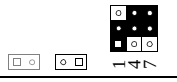
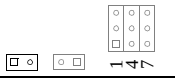
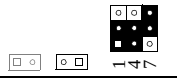
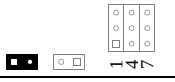
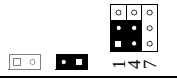
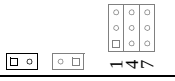
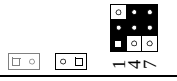
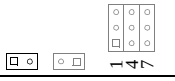
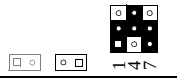
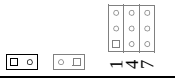
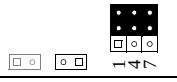
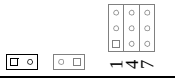
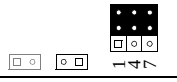
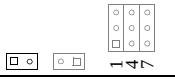
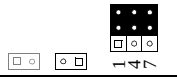
The orientation of figure 4 is with the VMEbus connectors on the right.

Figure 5 displays a schematic representation of K3 and K11 jumpers for typical U38 configurations.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Figure 5 displays Jumper Blocks K10, K4, K11, and K3 from the component side of the PCB. The pattern represented below is viewed when the PT-VME151A/151AE is placed on a work surface component side up and the Front Panel closest to the observer. "*" indicates factory configuration.

Figure 5: U23 and U38 Jumper Settings

Device Type	U23 Jumper Positions				U38 Jumper Positions			
	K10	K11	K3	K4	K10	K11	K3	K4
32Kx8, 28 pin PROM/ROM								
* 64Kx8, 28 pin PROM/ROM								
128Kx8, 32 pin PROM/ROM								
256Kx8, 32 pin PROM/ROM								
512Kx8, 32 pin PROM/ROM								
512Kx8, 32 pin, Flash EPROM Vpp = 5V								
All other 32 pin Flash EPROMs Vpp = 5V								
32 pin[1] Flash EPROMs Vpp = 12V								
8Kx8, 28 pin SRAM/EEPROM/RTC								
32Kx8, 28 pin SRAM/EEPROM								
128Kx8, 32 pin SRAM/EEROM								

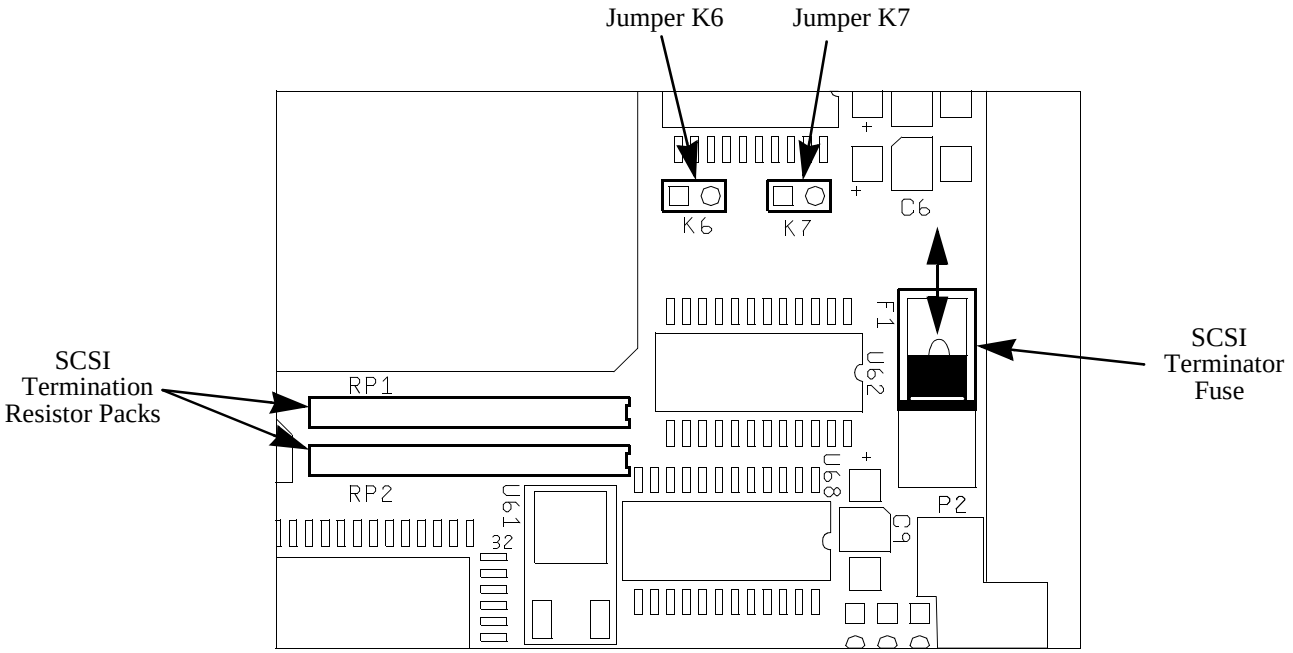
Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SCSI Termination

The configuration shipped from PTI assumes that the PT-VME151A is at the end of the SCSI cable, providing termination and the terminator power is provided directly from the board's +5V supply, SCSI Termination resistor packages RP1 and RP2 are installed and Jumper K6 is set appropriately.

If the PT-VME151A does not need to terminate the SCSI cable then see "Disabling Termination" below. You might want to review the section "Termination Power Source" if you are going to be bringing the PT-VME151A up and down and there are other SCSI Initiators attached to the SCSIbus.

Figure 6: SCSI Components



Disabling Termination

If the PT-VME151A is not at one end of the SCSI cable then the termination will be supplied by another SCSI device and, SCSI Termination resistor packages RP1 and RP2 (shown above) must be removed.

Termination Power Source

The active termination circuit on the PT-VME151A draws its power from the SCSI TERMPWR signal pin. For proper termination some device on the SCSI cable must supply +5V on the TERMPWR line. Through jumper K6 the PT-VME151A is capable of doing this. With pins 1 and 2 of K6 shunted the power is provided to TERMPWR pin directly by the board's +5V supply. When the pins 1 and 2 are open another device on the SCSI bus must supply TERMPWR. See "TERMPWR Overview" below for more information.

TERMPWR Overview

There are two classes of devices on a SCS bus, Initiators and Targets. The SCSI controller on the PT-VME151A can act as either but it typically is an initiator. Disk drives, tape drives, etc.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

are normally target devices. With a single target (disk drive) and a single initiator (the PT-VME151A) on a SCSIbus, termination is provided by the respective devices at each end of the cable. If either end were to lose power then termination would be moot because there would be no data to transfer.

Multiple PT-VME151As have been tied together on a single SCSIbus to use the SCSIbus as a very high performance Local Area Network. In this application it was advantageous to be able to power down an individual PT-VME151A without having to worry about whether it was the one supplying the SCSIbus termination. The SCSI TERMPWR mechanism provided the solution.

The PT-VME151A's +5V supply goes through fuse F1 then diode CR2 to be OR'ed into the SCSI TERMPWR signal. This allows the PT-VME151A to supply SCSIbus termination power when it is powered up and some other device on the SCSIbus to provide it when it is not. The fuse protects the PT-VME151A's power supply from short circuit conditions on the TERMPWR signal.

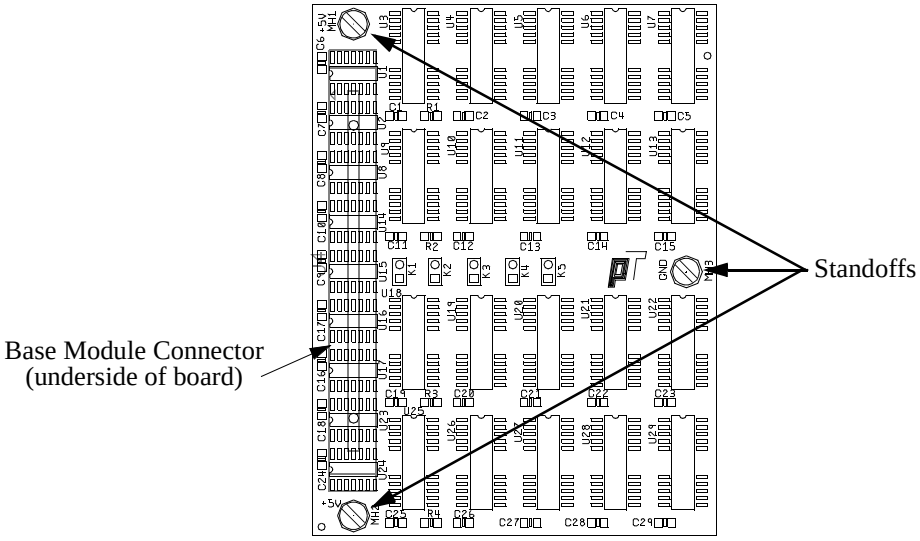
If for some reason you do not want the PT-VME151A to contribute to TERMPWR remove fuse F1. Fuse F1 is removed by pulling it to the right as shown by the bidirectional arrow on top of it in Figure 6.

NOTE: If unreliable SCSI operation occurs, the fuse, terminator resistor packs and jumper settings should be checked.

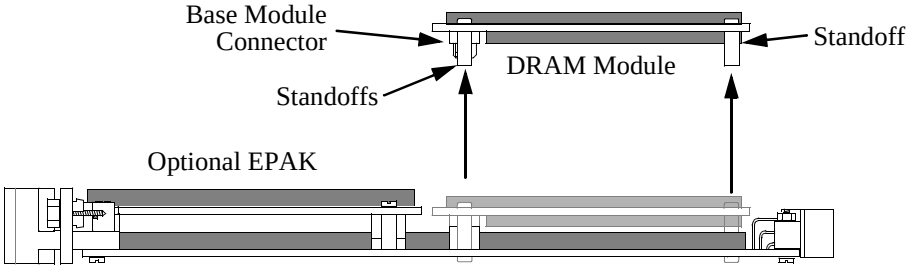
Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

DRAM Module Upgrading

The DRAM module is designed to be easily upgraded by the user[1]. The low insertion force 80 pin surface mount connection to the PT-VME151A allows the module to be snapped on.



There are three standoffs[2] that support the DRAM module. To upgrade the DRAM module, place the PT-VME151A on a work surface component side down and remove the three screws from the standoffs. Turn the board over and pop off the DRAM module by lifting it straight up from the board. In the drawing below the grayed area indicates the “component” side.



PT-VME151A Base Module

To install the new DRAM module, place the PT-VME151A on a work surface component side up. Carefully align the bodies of the DRAM module connectors, and press firmly on top of the connector with both thumbs to snap it in. Check to see that the DRAM Module connector is tightly seated. The standoffs should be flush with the surface of the PT-VME151A.

Turn the PT-VME151A with the attached DRAM Module over (component side down) then install and tighten the three screws into the standoffs.

---

1 The jumpers (K1-K5) on the DRAM Module are factory configured, no user modifications are required.

2 Standoff - A threaded tube with a screw in each end.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

NOTE: All 3 standoffs must be properly installed because they are also used to carry power and ground to the DRAM Module.

EPAK Installation

If not already installed do it now! Follow the instructions contained in your EPAK Users Manual.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Board Installation

Power Considerations

The PT-VME151A typically draws 25 ma. of +12V and -12V, and 3.9 Amps of +5V. These figures must be added to those of any attached EPAK or EBOARD to determine the total power requirements. It is recommended that Maximum values are used to ensure adequate margins. Add these numbers to those of the other devices in the system and check that the incorporation of the PT-VME151A (and Option Modules) does not exceed the system power supply ratings.

NOTE: On the PT-VME151A both 12V supplies are used by the RS-232 drivers attached to the DUART and passed to the EPAK connector. +12V can also be used by EPROMS that require a VPP = 12V.

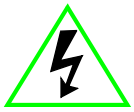
Slot Considerations

If you plan on using the System Controller functions of the PT-VME151A then it must be plugged into the Slot 1 position of the VME backplane. The System Controller functions will be automatically enabled after reset if the Slot 1 [BG3IN*] signal is open (or grounded).

For applications that do not require system controller functions the PT-VME151A can reside in any other VMEbus Slot. There are two considerations that must be made when not using the PT-VME151A in Slot 1, any jumpers on the backplane for the Bus Grant and Interrupt Priority chains must be removed, and the choice of slot location can effect the system level performance of the board.

Relative to other devices at the same Bus Grant and Interrupt Priority levels, the priority of a board goes down as it moves away from Slot 1. Typically, slot position only becomes an issue when there are extremely high levels of bus activity. The slot position, bus grant and interrupt priority levels should be reviewed from a system perspective whenever a new board is configured into a system.

Backplane Insertion



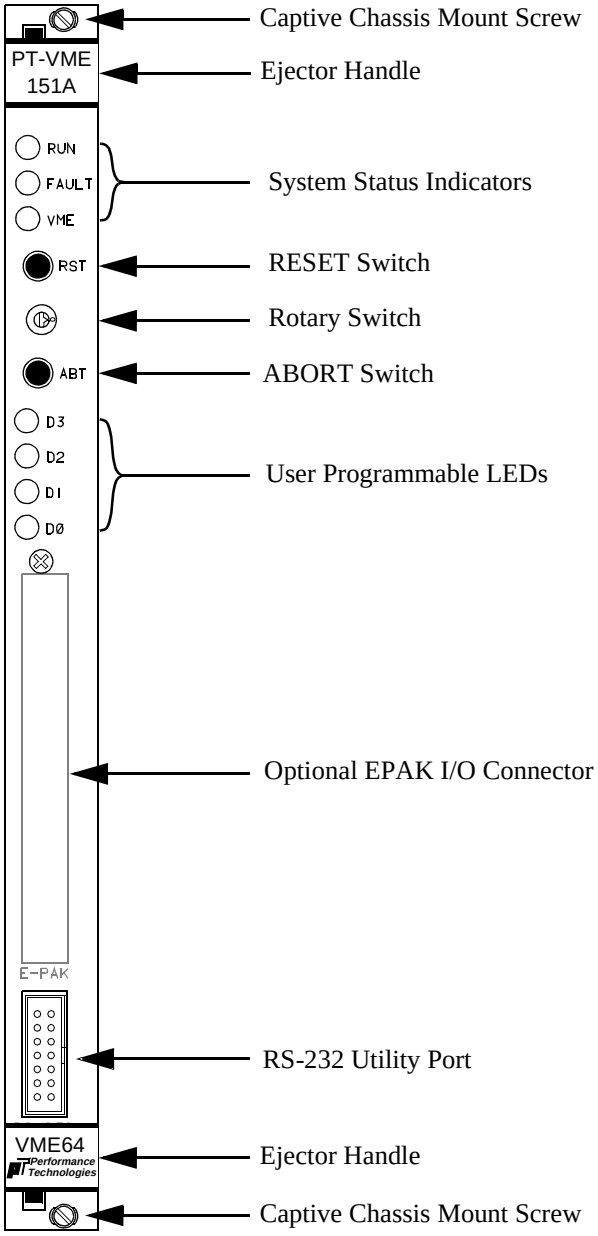
WARNING: The chassis must be switched off before inserting the board or making any cable connections to avoid damage to yourself or the components!

After reviewing the Power Considerations and selecting a slot, insert the PT-VME151A into the backplane. Be sure that it is seated completely into the backplane then tighten the two Captive Chassis Mounting Screws on the front panel. See “Figure 9: Example Serial port Cable” on page 26. Attach cables as necessary then power up the system.

NOTE: The first time the system is powered up after inserting the card, check the supply voltages at the PT-VME151A backplane P1 and P2 connectors. Adjust the supplies as necessary to the nominal voltage levels (+12.00V, - 12.00V and +5.00V)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Figure 7: PT-VME151A Front Panel



Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SCSI Considerations

Cabling

The PT-VME151A SCSI interconnect is provided through the User Defined Signal pins of the VMEbus P2 connector. The signals are organized so that a mass terminated Insulation Displacement Connectors (IDC) can be used to attach SCSI devices to the PT-VME151A. See “Table 14: VMEbus” P2” Connections” on page 77.

An interface cable can be constructed using a 50 conductor ribbon cable to attach a Eurocard (DIN 4612) IDC with only rows A and C populated to a 50 contact ribbon cable IDC socket. The VMEbus User Definable signals occupy 64 of the 96 positions on the P2 connector (rows A and C), however the SCSI specification only requires 50 conductors, so pin-1 of the ribbon cable must be justified to the pin-1 end of the Eurocard connector.

The SCSI Specification specifies that the maximum end to end length of a single-ended (TTL) SCSIbus cannot exceed 6 meters or 19.69 ft.

Example

Following is an example cable with vendors and part numbers for the components. These configurations have been tested at PTI. Figure 9 displays an example SCSI cable for the PT-VME151A. The view is with the connector sockets pointing towards you.

As long as the 6 meter maximum length identified in the SCSI specification is not exceeded there are no constraints on the spacing between connectors other than those imposed by your physical configuration. It is recommended that the cable be no longer than necessary for your particular application. The SCSIbus is basically asynchronous, so long cable lengths do contribute to control signal handshaking delays, affecting the overall performance.

VMEbus P2 Connection

64 position Insulation Displacement Connector derived from DIN 41612 type C, with rows A and C populated (socket):

Burndy BPS3B96ACROFSZ1 or

AMP 746603-1

Ribbon cable

50 Conductor 28 AWG. Flat Cable

Spectra-Strip 843-191-2801-050 or

3M 3365/50

SCSI device connector

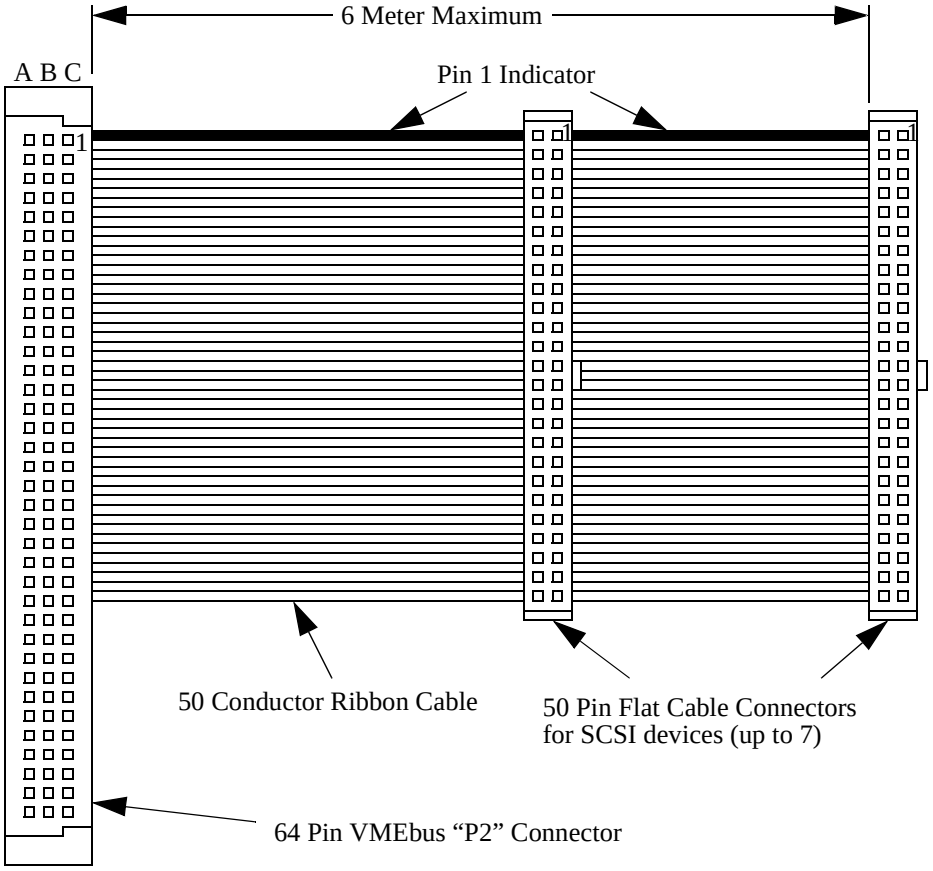
50 Pin Flat Cable Connector center polarized

Burndy FRS50BF-8 (strain relief included) or

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

AMP 1-746288-0 (connector)
AMP 499252-4 (strain relief)

Figure 8: Example SCSI Cable



Mechanical restraints

Depending upon your mechanical configuration, tie wraps or cable clamps may be necessary to provide mechanical support for the cable. Most VME backplanes and SCSI devices do not provide locking mechanisms or other means of mechanically securing the connectors. They depend on the insertion force of 50+ pin and socket connections to hold the attached connector and cable in place. Nothing is more frustrating than intermittent errors due to a connector that has been pulled out by the weight of its own cable.

PTI recommends that, if possible, you attach the cable to some nearby metal work with tie wraps or cable clamps to provide mechanical support for the cable, especially if it is long (more than 18 inches between device connections) or if it is in a high vibration environment.

SCSI device grounds

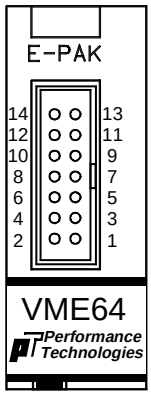
Most SCSI device vendors provide a method for connecting their device to chassis ground. It is suggested that you follow the vendor’s recommendations for its use. Proper use of these connections generally improves the overall noise margins of a system.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Device addresses

Check the device addresses of all SCSI devices to ensure that no conflicts occur. The device address of the PT-VME151A is programmable and will be determined by your installed software.

Serial Port Cabling



The PT-VME151A Utility Serial Port interconnect is provided on the front panel. The signals are organized so that a mass terminated Insulation Displacement Connectors (IDC) can be used to create an RS-232 DTE interconnect. See “Table 12: Utility Serial Port Pin Assignments” on page 75. A 12 inch transition cable is supplied with the PT-VME151A which converts between the 14-pin header and a female shell (male pin) 25-pin D-Shell connector. If a longer cable or a different D-Shell connector sex is required it can be assembled by following the example below. The Utility Port pin positions are noted in the figure to the left.

The EIA/RS-232C Specification limits the maximum end to end cable length to 50 ft.

Example

Following is an example cable with vendors and part numbers for the components. These configurations have been tested at PTI. Figure 9 displays an example serial cable for the PT-VME151A. The view is with the connector sockets pointing towards you.

An interface cable can be constructed using a 14 conductor ribbon cable to attach a 25-Pin D-Shell IDC to a 14 contact ribbon cable IDC socket. To conserve front panel space only a 14 pin connector is used, however the 25-Pin D-Shell expects 25 conductors, so pin-1 of the ribbon cable must be justified to the pin-1 end of the D-Shell connector. It is recommended that the cable be no longer than necessary for your particular application.

D-Shell Connection

25 position Insulation Displacement Connector Male, D-Shell connector derived from DIN 41612 type C, with rows A and C populated (socket):

3M 8225-6003 or

T&B 609-25P-MA2

Ribbon cable

14 Conductor 28 AWG. Flat Cable

Spectra-Strip 843-191-2801-014 or

3M 3365/14

RS232 Serial Port connector

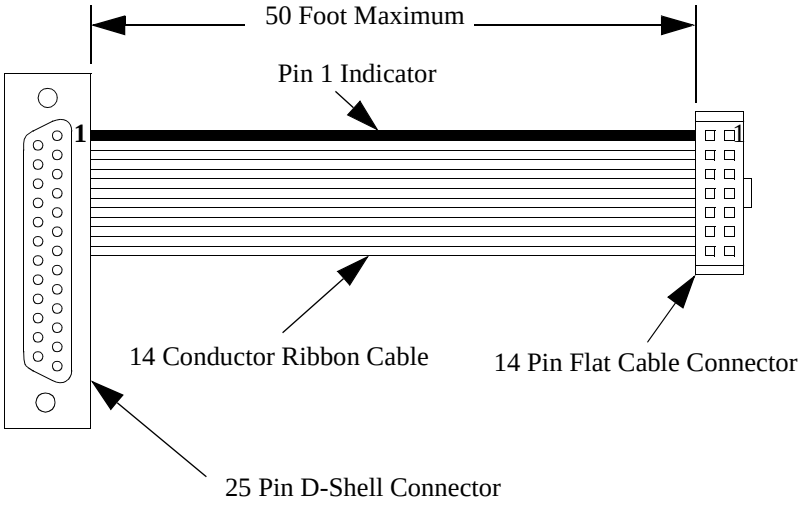
14 Pin Flat Cable Connector center polarized

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Burndy FRS14BF-8 (strain relief included) or

AMP 746288-2 (connector)
AMP 499252-9 (strain relief)

Figure 9: Example Serial port Cable



Mechanical restraints

Depending upon your mechanical configuration, tie wraps or cable clamps may be necessary to provide mechanical support for the cable.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

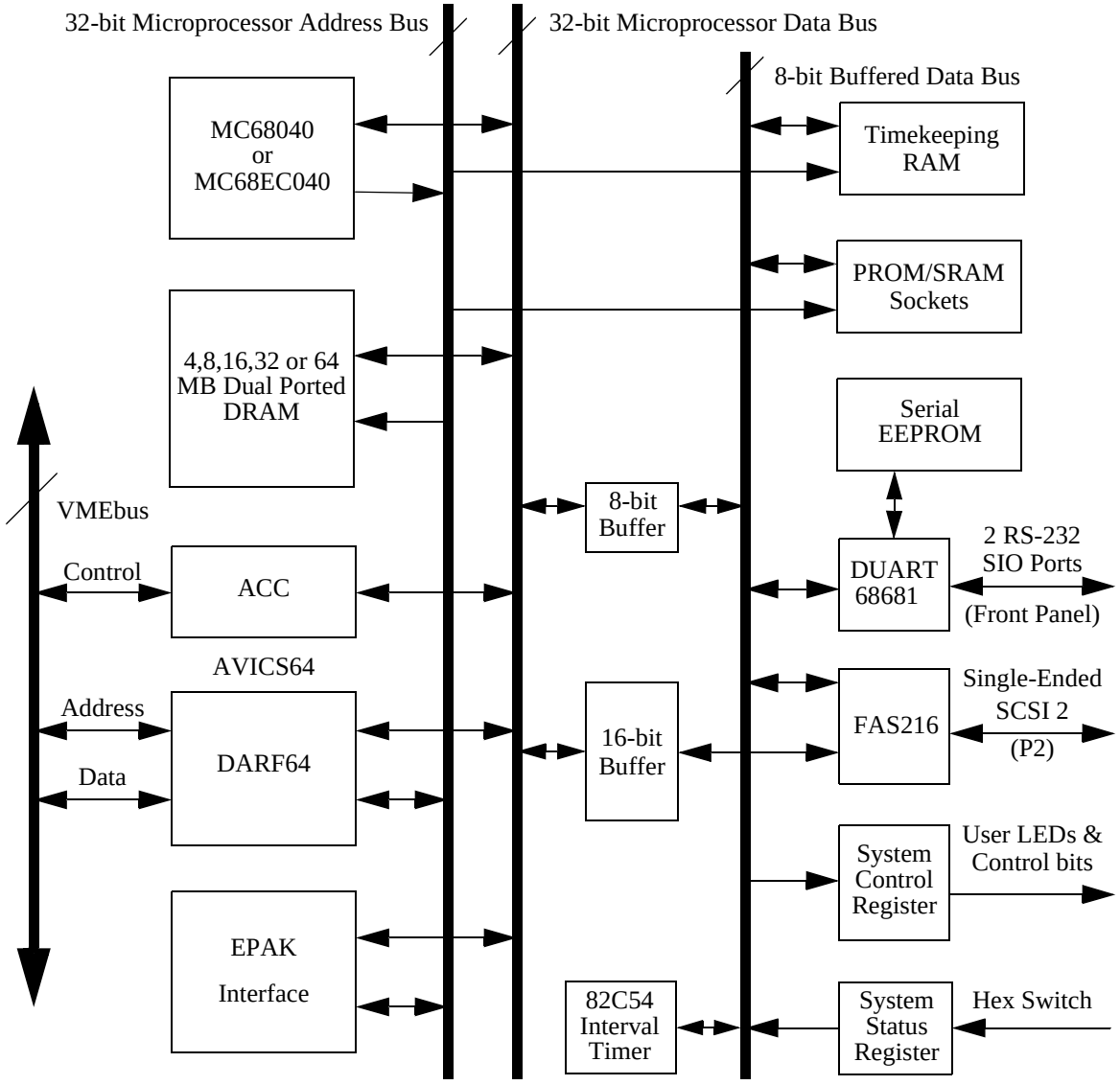
Section

3

FUNCTIONAL DESCRIPTION

A block diagram of the PT-VME151A/151AE is provided below. Down the center are the 32-bit microprocessor address and data busses. To the right is an 8-bit buffered data bus that provides I/O interface connectivity. To the left is the VMEbus interface, provided by the Advanced VMEbus Interface Chip Set.

Figure 10: Block Diagram



Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Through the remainder of this document references to the Motorola MC68040 processor imply the MC68EC040 also. Specific differences will be cited as necessary.

Microprocessor

The PT-VME151A utilizes a Motorola MC68040 microprocessor running at 25 MHz. This processor combines a full 32-bit Central Processing Unit (CPU) core, a data cache, an instruction cache, a Floating Point Processor, and an enhanced bus controller in a single VLSI device. The MC68EC040 is identical to the MC68040 except that it lacks the MMU and FPU. The MMU of the 68040 may be disabled by installing jumper K2.

Memory

There are four separate memory mechanisms available on the PT-VME151A: up to 64 megabytes of DRAM, two 32-pin JEDEC sockets for ROM, PROM, EPROM, etc., 8184 bytes of nonvolatile SRAM, and 128 bytes of nonvolatile EEPROM.

DRAM

The main memory is composed of 70 ns. fast page mode DRAM. Available memory configurations are 4, 8, 16, 32, or 64 megabytes of DRAM. All of main memory can be mapped to the VMEbus through the DARF64. Additionally, EPAK address space may be mapped to the VMEbus by overlaying its address space with a portion of main memory. The overlaying is enabled at reset, making a portion of the main memory inaccessible for the VMEbus. If the ability to address the EPAK from the VMEbus is not desired, it may be removed by writing a 1 to the Enable EPAK Access from VME bit (0) of Control Register 2. See “Enable EPAK Access from the VMEbus” on page 47 for more information.

The 68040 and 68EC040 support a burst mode for filling their on-chip data and instruction caches. The PT-VME151A utilizes the fast page mode of the DRAM to accelerate the burst transfer operation. During a burst transfer four sequential long words are fetched from the DRAM, requiring four clock cycles for the first long word transfer and two clock cycles for subsequent long word fetches.

Parity[1] is generated and checked by PT-VME151A hardware on local DRAM accesses by the MC68040. A Bus Error may be generated as an acknowledgement to a reference if a parity error is detected. See “Parity” on page 30 for more information.

The address space from 20000000h to 2FFFFFFFh is allocated to the DRAM. Any reference to this 256 MByte space will complete without a bus error. The installed DRAM will repeat throughout this range. Repeatability is described below. ‘Blank’ areas of memory cannot be written and will return unpredictable results when read. The DRAM size may be determined by reading the Status Register.

[1] Not availiable on 4M and 8M Configurations.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

DRAM Mapping

DRAM Size	Address Range	Response
4 MBytes	20000000-203FFFFFh	Normal
	20400000-20FFFFFFh	Blank
	21000000-213FFFFFh	Normal - repeat of 20000000-203FFFFF
	21400000-21FFFFFFh	Blank

The pattern of (4M Normal) - (12M Blank) - (4M Normal) - (12M Blank) repeats throughout the range of 20000000-2FFFFFFFh. Thus address 20000000h may be read or written at 21000000h, 22000000h, etc.

8 MBytes	20000000-207FFFFFh	Normal
	20800000-20FFFFFFh	Blank
	21000000-217FFFFFh	Normal - repeat of 20000000-207FFFFF
	21800000-21FFFFFFh	Blank

The pattern of (8M Normal) - (8M Blank) - (8M Normal) - (8M Blank) repeats throughout the range of 20000000-2FFFFFFFh. Thus address 20000000h may be read or written at 21000000h, 22000000h, etc.

16 MBytes	20000000-20FFFFFFh	Normal
	21000000-21FFFFFFh	Normal - repeat of 20000000-20FFFFFF

The pattern of (16M Normal) - (16M Normal) repeats throughout the range of 20000000-2FFFFFFFh. Thus address 20000000h may be read or written at 21000000h, 22000000h, etc.

32 MBytes	20000000-21FFFFFFh	Normal
	22000000-23FFFFFFh	Blank
	24000000-25FFFFFFh	Normal - repeat of 20000000-21FFFFFF
	26000000-27FFFFFFh	Blank

The pattern of (32M Normal) - (32M Blank) - (32M Normal) - (32M Blank) repeats throughout the range of 20000000-2FFFFFFFh. Thus address 20000000h may be read or written at 24000000h, 28000000h, etc.

64 MBytes	20000000-23FFFFFFh	Normal
	24000000-27FFFFFFh	Normal - repeat of 20000000-23FFFFFF

The pattern of (64M Normal) - (64M Normal) repeats throughout the range of 20000000-2FFFFFFFh. Thus address 20000000h may be read or written at 24000000h, 28000000h, etc.

Sizing

To size DRAM perform the following steps:

Step 1 Write location 20000000h with AA55AA55h.

Step 2 Set Memory pointer to 20400000h

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Step 3 Write CC33CC33h to the longword pointed to by the Memory Pointer.

Step 4 Read the location pointed to by the Memory Pointer.

If the value read back value does not equal CC33CC33h then the end of memory has been reached. Go to Step 5.

If the read back value does match CC33CC33h then check location 0 to see if it still contains AA55AA55h. If location 0 equals CC33CC33h then the end of memory has been reached. Go to Step 5.

If location 0 equals AA55AA55h then the end of memory has not been reached. Go to Step 4.

Step 5 Add 00400000h to the Memory pointer to step it to the next 4 MByte boundary. Go to Step 2.

Step 6 Done.

Parity

Parity RAM is provided for the 16, 32, and 64 MByte configurations. Parity is generated and checked on all DRAM accesses, which include accesses by the 68040, DARF64, SCSI controller, and EPAK bus masters.

Parity errors detected during 68040 reads or reads by an EPAK bus master return a bus error. Parity errors detected during a DARF64 or SCSI controller reference will assert the L7IMEM pin of the ACC, generating a level 7 interrupt request. The source of the a parity error is latched in PT-VME151A System Status Register 2. Parity errors that generate a Bus Error (68040 and EPAK bus masters) will not generate a Level 7 interrupt however, the source of the error will be latched in Status Register 2. Any Level 7 interrupts that do result from parity errors (DARF64 and SCSI controller) will remain asserted until Status Register 2 is read. If a parity error is detected during a DARF64 local burst cycle, any remaining accesses in the burst will be aborted by releasing the VMEGR signal to the DARF64.

NOTE: Status Register 2 must be read to determine the source of any Level 7 interrupt request, because the ACC L7IMEM pin is also used to signal a SCSIbus Reset conditions.

Checking

Parity checking is enabled by setting the Enable Parity Error Checking (EPEC) bit in Control Register 2 (bit 1). Parity checking is disabled following reset or if Parity RAMs are not installed (4M and 8M configurations).

Parity is always written to DRAM regardless of the state of EPEC. If EPEC is disabled then level 7 interrupts and bus errors will not be generated and the associated flags (bits 0-3) in Status Register 2 will not be asserted.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Initialization

DRAM **must** be initialized before enabling parity error checking. The initialization process consists of writing any data value to all installed memory locations. This operation sets the parity RAM to a valid state.

Testing

For testing purposes bad parity may be intentionally written. By setting the Enable Bad Parity bit (2) in Control Register 2, the parity bit written with each data byte will be complemented causing a parity error to be generated when the byte is read.

NOTE: If EBP is enabled then the Enable Parity Error Checking (EPEC) **must** be disabled, otherwise parity errors will be generated on every memory reference.

Diagnostics should include checking parity on an individual byte basis to fully check the parity RAM.

PROM/SRAM Sockets

The board is equipped with two 32-pin JEDEC sockets configured as bytewide ports. Both sockets support ROM, PROM, EPROM and Flash EPROM read-only devices, as well as 28-pin or 32-pin configurations.

One of the two sockets is also capable of supporting SRAM and Nonvolatile SRAM read/write devices.

Jumpers are provided to select between read-only and read/write operation and the 28-pin or 32-pin configurations. See “ PROM/ROM/SRAM/EEPROM Socket Configuration” on page 14.

Nonvolatile SRAM and Time of Day/Calendar Clock

The Dallas Semiconductor DS1643 Nonvolatile Timekeeping RAM features 8184 Bytes of Nonvolatile SRAM and a Real Time Clock (RTC) with integrated crystal, power fail control circuit and a lithium energy source. The clock registers are accessed identical to the static RAM. The registers reside in the top eight RAM locations. The the base address of the Timekeeping RAM is at 0F000000h. See “Table 8: DS1643 Nonvolatile Timekeeping RAM Registers” on page 71 for more information.

Serial EEPROM

The EEPROM supports 128 bytes of nonvolatile memory. The part is capable of 10,000 erase/write cycles and ten year data retention. Performance Technologies normally uses this memory to store various parameters and options used in the initialization and operation of the PT-VME151A.

This device is socketed so that it can be moved to another board if necessary. For instance, if board level replacement is typically performed on failures in the field, the EEPROM can be moved to the replacement board to maintain the configuration information of the original board.

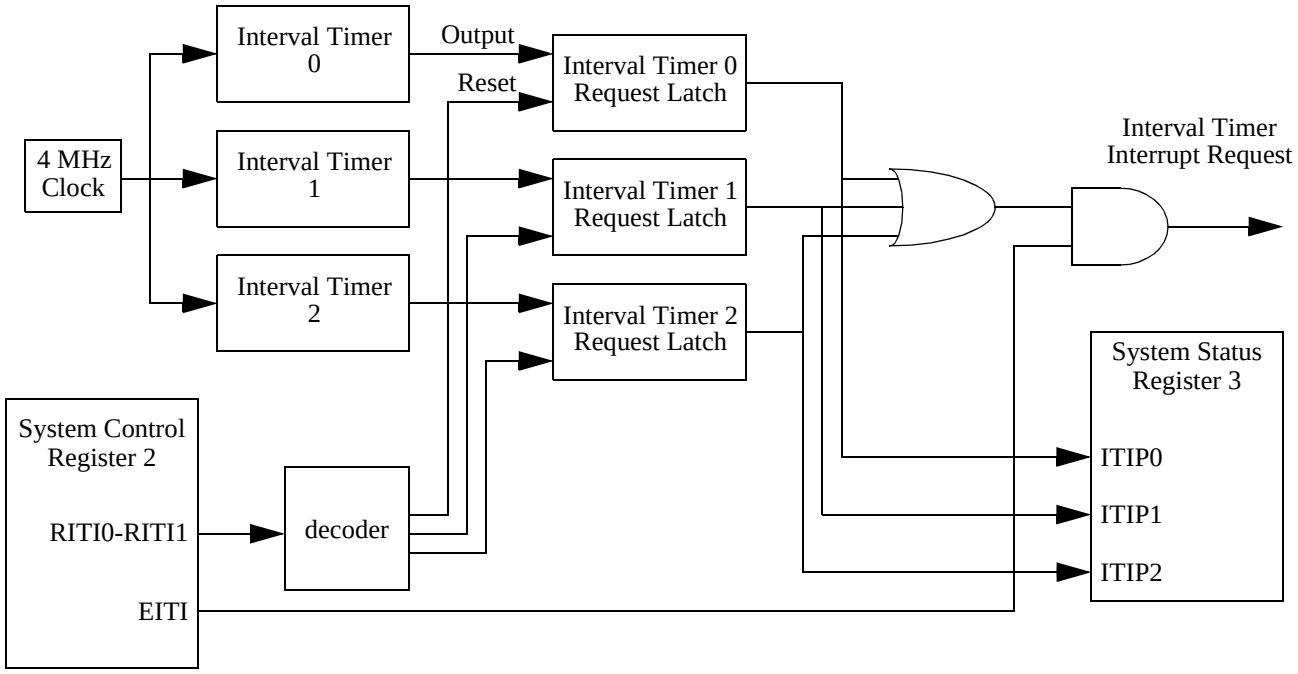
Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Interval Timer

The Interval Timer, an Intel 82C54, provides three independent 16-bit timers running off the same 4 MHz clock. These three timers are identical in operation. Refer to the Intel Peripherals Handbook for a complete description of the 82C54[2].

When an Interval Timer is programmed in "Mode 2", it will perform the following functions when it counts down to zero: pulse its OUTPUT pin, reload the initial count, and continue counting. The output pulse of each timer is latched into the respective Interval Timer Interrupt Request Latch and the outputs of the three latches are OR'ed together to generate the Interval Timer Interrupt Request.

Figure 11: Interval Timer Block Diagram



The Interval Timer Interrupt Request generates an interrupt through the LIRQ2 pin of the ACC. This pin is shared with the ACC Tick Timer (which can be disabled). The Interval Timer Interrupt Request can be enabled by setting the EITI bit (5) in System Control Register 2. When the Interval Timer interrupts are disabled, the latching of the individual timer output pulses is also disabled. After reset, the state of the 82C54 is undefined so the Interval Timer interrupts are disabled, this also maintains compatibility with PT-VME151.

An interrupt on the LIRQ2 pin can be programmed (in the ACC Local Interrupts 3 and 2 Control Register) to generate an auto-vector operation on any one of the 68040's seven interrupt request levels.

Any of the Interval Timers may have its counting disabled by programming it to "Mode 1". Mode 1 requires a rising edge on the timer's GATE input to enable counting. Since each GATE input is hard-wired to logic 1, Mode 1 will never count and thus may be used as a "Disable Counting" mode.

[2] See "Applicable Documents" on page 2 for Intel Peripherals Handbook ordering information.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

The current state of the individual Interval Timer Request Latches (0, 1, and 2) may be determined by reading the Interval Timer Interrupt Pending bits in System Status Register 3. SSR3 bits 4, 5, and 6 reflect the state of ITIP0, ITIP1, and ITIP2, respectively.

VMEbus Interface

The VMEbus interface provides VME*64* data transfers as well as a fully functional high performance 32-bit VMEbus interface as defined by the IEEE 1014 Rev C VMEbus Specification. It is based upon the Advanced VMEbus Interface Chip Set (AVICS 64) which is comprised of the Advanced VMEbus System Architecture Control Circuit (ACC) and the VMEbus 64-bit Data Address Register File (DARF64).

See the DARF64 Data Sheet, the Newbridge Microsystems data book and the AVICS Technical Manual for more information.

DARF64

The DARF64 is a 64-bit Data/Address Register File which interfaces the VMEbus address and data buses with the local PT-VME151A bus. It may act as a VMEbus Master or Slave. The local DRAM and EPAK address spaces of the PT-VME151A are accessible to a VMEbus Master through the DARF64. The DARF64 is also capable of DMA transfers between local memory (DRAM or EPAK) and the VMEbus.

VME*64* Transfers

VME*64* is a newly defined capability of the VMEbus. VMEbus Block Transfer mode (BLT) only uses the address bus during the first transfer cycle to pass the start address of the transfer. The slave is responsible for latching this address and incrementing it internally as subsequent data arrives. As a result the address lines on the VMEbus are unused during all but the first transfer. Data is passed every transfer cycle on the data bus.

The 64 bit Multiplexed Block Transfer (D64MBLT) mode makes a minor change to the first cycle and takes advantage of the address bus being otherwise unused during a block transfer data phase. A MBLT cycle is divided into two phases, address and data. During the first transfer cycle address only is passed and on all subsequent cycles data is passed. The combination of the 32 data lines, 31 address lines, and the [LWORD*] signal provide a 64 bit path on the VMEbus. A double longword can then be transferred on each Data Strobe/Data Acknowledge handshake. The address phase can be either A32 or A64. A32 transfers pass the address normally (on the address bus) and the 32 data lines are unused, A64 transfers pass the high order 32 bits of the 64 bit address on the data lines. During the data phase the 31 address lines, and the [LWORD*] signal are used to pass the high order 32 bits of the 64 bit data. Specific Address Modifiers are used to identify A64:D64MBLT and A32:D64MBLT cycles.

Transfer Modes

The DARF64 is capable of two operational modes: “decoupled” and the traditional “atomic”. The decoupled mode takes full advantage of the VMEbus bandwidth by using the receive and transmit FIFOs, built into the chip, that decouple the local bus from the VMEbus. The FIFOs immediately accept writes from one bus, release that bus for use, then finish the write to the destination bus. In atomic mode the DARF64 bypasses the FIFOs, simply buffering the data and address to the destination bus, forcing any associated wait states back to the source bus.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

All read, read-modify-write, and interrupt acknowledge cycles are atomic. To preserve data integrity, atomic cycles are not performed until all write cycles queued ahead of the atomic cycle are completed.

Decoupled

This feature allows transfers on the VMEbus to be completely “decoupled” from any latencies incurred on the local bus. VMEbus transfers can proceed at a rate that is determined strictly by the VMEbus handshaking rate. The receive and transmit FIFOs can be individually enabled using the RXATOM and TXATOM bits in the DARF64 Mode Control Register.

The receive FIFO captures write transfers from VMEbus devices or DMAC VMEbus reads. Data can be moved into the FIFO using D64MBLT, D32BLT, D16BLT, or individual transfers. As soon as there is data in the FIFO, the DARF64 requests the local bus and the data will be transferred to the appropriate address in DRAM or EPAK memory.

The transmit FIFO decouples local bus write references to the VMEbus, either from the CPU or the DMAC. On DMA transfers you can optionally wait until the FIFO is full before writing to the VMEbus. DMA data can be transferred from the FIFO using D64MBLT, D32BLT, D16BLT, or individual transfers. CPU references are always handled as individual transfers. As soon as there is data in the FIFO, the DARF64 requests the VMEbus and transfers the data to the appropriate address.

If the FIFO Burst Enable (FIFOBEN) bit or DMA Burst Enable (DMABEN) bit in the DARF64 Mode Control Register is set then “burst mode” is used on the local bus to transfer the respective data. Otherwise the incoming data will be moved as individual 32 bit references.

Atomic

When the RXATOM or TXATOM bit in the DARF64 Mode Control Register is set, the respective FIFO is bypassed. In atomic mode, cycles are performed in direct-connected mode where the address, data, DTACK and BERR signals are connected between the local bus and the VMEbus.

VMEbus Control Logic

The VMEbus interface of the AVICS 64 is fully asynchronous, thus avoiding the delays and reliability problems associated with synchronous designs. The VMEbus data transfer control lines Address Strobe [AS*], Data Strobe [DS0* and DS1*] and Data Transfer Acknowledge [DTACK*] perform asynchronous handshaking to pass data across the bus. Any delays in turning these handshaking signals around slow down the associated data transfer. In the AVICS 64 fully asynchronous design, the delays are strictly a function of propagation times through the control logic.

Synchronous designs require sampling of the VMEbus transfer control signals in order to be reliably used by the synchronous control logic. High sampling rates are necessary to achieve performance equivalent to asynchronous designs, but these higher sampling rates increase the probability of metastability conditions occurring. When a metastable condition does occur its statistical duration falls off with time, therefore the longer that one waits to act upon the sampled signal the less likely they are to see it metastable. A designer must make a performance vs. reliability trade off on what this delay should be. This Metastability Settling Time will add a fixed delay to every sampled signal.

Another delay added by sampling is due to the sampling clock rate. An incoming signal can change anywhere between two sample clock edges. Best case is when the incoming signal changes just

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

before the sample clock, worst case is when the incoming signal just misses the sample clock. On the average, a Sampling Delay of one half of the sample clock time must be added to each sampled signal.

Therefore, every signal that requires sampling must have a Sample Delay and Metastability Settling Time must be added to propagation times of the control logic. All synchronous designs that interface to the asynchronous VMEbus pay a performance penalty and make the associated performance vs. reliability trade-offs.

VMEbus Slave Accesses

The Slave Image is the VMEbus address range throughout which the local memory of the board can be accessed. The slave image of the PT-VME151A is defined in programmable registers of the DARF64. Separate slave images, different in size, can be set up in the A64, A32 and A24 address spaces. The DARF64 does not provide an A16 slave image. The respective slave images are defined by base address and size registers. The A64 image base address can be programmed to start on any 4 gigabyte boundary and is size 128 megabytes in size. A64 addressing is only supported during D64 Multiplexed Block Transfers (D64MBLT). The A32 image base address can be programmed to start on any 128 megabyte boundary and be any size from 4 kilobytes to 128 megabytes in binary increments. The A24 image base address can start on any 512 kilobyte boundary or multiple of its programmed size, whichever is larger, within the 16 megabyte A24 addressing space. The A24 image size can be programmed to 512K, 1, 2, or 4 megabytes.

The DARF64 responds to Standard and Extended, non-privileged and supervisory address modifiers. VMEbus access types include read, write and read-modify-write. Up to 128 megabytes of each slave image can be protected from writes, or reads and writes.

Parity is generated and checked by PT-VME151A hardware on local DRAM accesses by VMEbus masters. A level 7 interrrupt may be generated if a parity error is detected. See “Parity” on page 30 for more information.

EPAK Access from the VMEbus

See “EPAK Interface” on page 58.

VMEbus Master Accesses

The DARF64 can request the VMEbus under a number of conditions: the transmit FIFO contains write cycles, the DMAC starting transfers, the 68040 begins a read cycle to the VMEbus, the DARF64 is in atomic mode and the 68040 begins a write cycle to the VMEbus, or the DARF64 was signaled with a VMEbus [IACK*] to begin an interrupt acknowledge cycle.

The ACC provides an Ownership Timer which can be programmed to limit the time that the DARF64 maintains VMEbus mastership, from immediately off to 2, 4, or 8 ms., to unlimited use. The Ownership Timer is used to ensure predictable bus access latencies to other VMEbus masters.

While performing bus transactions from the FIFO the VMEbus “address pipelining” feature is used.

68040 Accesses

CPU accesses can be set up to be decoupled or atomic. In decoupled mode the FIFO accepts the data, acknowledges 68040 writes then, the VMEbus immediately requests the bus. In atomic

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

mode the FIFO is bypassed and the CPU waits for the VMEbus acquisition and transfer to take place. All 68040 reads bypass the FIFO.

Access to the VMEbus address space by the 68040 CPU is through addresses 80000000h - FFFFFFFFh. In order to access the full VMEbus address space the Page bit in the 151A System Control Register defines VMEbus address bit 31. When the Page bit is 0, PT-VME151A addresses 80000000h-FFFFFFFFh are mapped to VMEbus addresses 00000000h - 7FFFFFFFh. When the Page bit is 1, PT-VME151A addresses 80000000h-FFFFFFFFh are mapped to VMEbus addresses 80000000h-FFFFFFFFh.

For CPU accesses the DARF64 splits 4 Gigabyte VMEbus address space into 32-128 megabyte pages. Most pages are defined to be A32:D32, however selected ranges may define to be A24:D32, A24:D16 and A16:D16 spaces.



CAUTION: When the CPU performs an access in the A16:D16 range, the DARF64 will respond to the CPU as a 16 bit device, unlike the 68030, the 68040 will **NOT** split up the cycles if necessary. Similarly, for references in the A24:D16 space.

A24:D32 and all A32 accesses allow 32 bit transfers from the 68040. The implied addressing space and the CPU function codes determine the data or program, and supervisory or nonprivileged aspects of the Address Modifier code.

Read-Modify-Write

The DARF64 is capable of supporting single address Read-Modify-Write MC68040 instructions (TAS) across the VMEbus. The 68040 CAS and CAS2 instructions can require two addresses during a “locked” operation, thus translating into a requirement for Address Strobe to be asserted twice on the VMEbus while remaining “locked” in between. The VMEbus Specification provides no mechanism for supporting this class of operations.

DMAC

The DMA Controller in the DARF64 can transfer data between the VMEbus and DRAM or EPAK memory in several different address and data modes. It is controlled through four internal registers: DMA Local Address Register, DMA VMEbus Address Register, DMA Transfer Count Register, and the DARF64 Mode Control Register.

The DMAC can be programmed to use A64, A32, or A24 addressing, in supervisor or nonprivilege mode. The upper 32 bits of the A64 address are static and provided by the Master A64 Address Register. The lower 32 bits of the A64 address and A32 or A24 addresses are provided by the DMA VMEbus Address Register.

Data transfers can be programmed to occur in discreet (D32/D16), block (D32BLT/D16BLT), or multiplexed block (D64MBLT) mode. The DMA Transfer Count Register allows up to 4 megabytes of data to be transferred. The hardware automatically releases Address Strobe on the proper boundaries on the local and VMEbus.

To further improve transfer rates the PT-VME151A supports “Burst Mode” transfers from the DARF64 on the local bus. Burst lengths of 4, 8, 16, or 32 longwords can be programmed using the BLEN field of the DARF64 Mode Control Register. Given 32 longword bursts and the 4-2-2-2...2 DRAM burst timing a maximum data transfer rate of 49.2 megabytes per second is achievable over the local bus. The DMA Burst Enable (DMABEN) and FIFO Burst Enable (FIFOBEN) bits in the

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

DARF64 Mode Control Register allow the “Burst Mode” feature of the individual mechanisms to be enabled.

The transfer rate over the VMEbus is a function of the master/slave handshaking rate and transfer mode. When “decoupled” D64MBLT transfers were tested with the PT-VME240 VME*64* Memory Board a burst transfer rate exceeding 53 megabytes per second was measured.

DMA completions and errors can generate interrupts to the 68040, through interrupt handler of the ACC ([- INTP<1>], LIRQ1).

The advanced features of the DARF64 can be used to tune DMAC and VMEbus performance. The Transmit FIFO can be configured to begin VMEbus transfers immediately upon having data, or configured to wait until the FIFO is full. The No-Release mode (NOREL) bit in the DARF64 Mode Control Register causes the DARF64 to maintain ownership of the VMEbus until either the ACC requests the DARF64 to release the bus, or until the bit is turned off. The Ownership Timer in the ACC can be used in conjunction with the NOREL bit to throttle DMAC use of the VMEbus. By using the DMA Burst Enable and FIFO Burst Enable bits the “Burst Mode” feature of the respective mechanism can be enabled. The length of burst transfers on the local bus can be throttled with the BLEN field of the DARF64 Mode Control Register.

Parity is generated and checked by PT-VME151A hardware on local DRAM accesses during DMAC operation. A level 7 interrrupt may be generated if a parity error is detected. See “Parity” on page 30 for more information.

Location Monitor

The location monitor assists in inter-processor and inter-process communication. It consists of a 32-bit wide, 31-entry deep message FIFO loaded from the VMEbus. D32 or D16 operations are supported. If the even word is written, the upper 16 bits of the FIFO entry are set to one. The message FIFO is not bidirectional.

The Location Monitor exists at the top longword and the lower (even) word of the top longword in each of the A32 and A24 slave images. The monitor is equally accessible by the VMEbus and the local CPU. A process on the PT-VME151A does not need to determine whether the process it’s sending a message to is local or not.

The existence of entries in the message FIFO can generate interrupts to the 68040, through interrupt handler of the ACC ([- INTP<0>], LIRQ0).

Registers

The DARF64 is a longword wide device with 16 directly addressable internal registers. Status bits are generally sampled by the DARF64 at the start of a register access cycle to ensure up-to-date data for the reference. Detailed descriptions of the registers are available in the AVICS Technical Manual, a summary is provided in “Table 7: DARF64 Registers” on page 70. Bits that are unused have defined values and may be used in future versions of the DARF64. It is recommended that such unused bits be masked to zero before writing or after being read by software to maximize the probability of future software compatibility.

Test and Diagnostics

The Loopback Enable bit (LPBK) in the DARF64 Mode Control Register allows the CPU to test the address and data paths and the control logic. In Loopback mode any write cycle to its own slave

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

image by the CPU does not go directly to memory, but goes out on the VMEbus then back in again through the FIFOs. The VMEbus address and data transceivers drive the cycle onto the VMEbus, but the DARF64 loads the cycle into its receive FIFO from its own I/O pads. The loopback acquires mastership of the VMEbus for the process but the data read back through the Receive FIFO Address, Data, and Receive Registers does not pass through the VMEbus buffers.

If a Bus Error [BERR*] occurs during a write to the VMEbus the VBERR bit in the Control and Status Register is set, asserting the VMEINT pin. The Transmit FIFO Data, Address, and Control Registers will contain the respective information for the bus cycle in error. When the VBERR bit is cleared the DARF64 resumes with the next cycle in the FIFO.

If a Local Bus Error [-KBER] occurs during a write from the VMEbus the LBERR bit in the Control and Status Register is set, asserting the VMEINT pin. The Receive FIFO Data, Address, and Control Registers will contain the respective information for the bus cycle in error. When the VBERR bit is cleared the DARF64 resumes with the next cycle in the FIFO.

ACC

The ACC (Advanced VMEbus System Architecture Control Circuit) provides the control logic for the AVICS 64. The functions of the ACC are separated into several distinct modules. Some of these modules provide hardware controlled service functions and have little interaction with system software. The remaining modules can be configured by software to operate in various modes. They are accessed via the Register Block.

Reset

The Reset block provides control of the PT-VME151A local reset signal [-LRST]. Local Reset is asserted when the PT-VME151A detects a power on condition, if VMEbus [SYSRST*] is asserted, the front panel Reset button is pressed, the watchdog timer expires, or software sets the SWRST bit in the ACC General Control Register.

Local Reset will also be asserted if the ACC is the VMEbus System Controller and VMEbus [BG0IN*] is asserted.

Local Bus Timer

The Local Bus Timer is used to recover from unsuccessful local transfers (internal to the PT-VME151A). If a Local Dtack [-KSA0] is not detected within 512 us. of the assertion of Local Data Strobe [- KDS] the ACC will assert Local Bus Error [-KBER] until the Local Data Strobe signal is released. The timer duration is not user programmable, however it can be disabled by the control bit LTOEN in the ACC General Control Register.

References to UNASSIGNED addresses on the Local Bus will not generate Local Dtack, requiring the time-out mechanism for recovery. If the timer is disabled and such a condition occurs, the CPU will hang. It is recommended that the timer only be disabled in a system development environment. The timer is automatically enabled after the assertion of reset.

Watchdog Timer

The Watchdog Timer can be used to recover from software failures. The timer’s 2 seconds delay is restarted automatically by the release of Power On Reset [-PRST] and under program control by 0 to 1 transition of the CLRDOG bit in ACC Status Register 0. Failure to toggle the CLRDOG bit

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

before the 2 seconds delay expires results in the assertion of Local Reset [-LRST]. Local Reset initializes the 68040 and all I/O devices on the PT-VME151A.

The Watchdog Timer can be disabled by jumper K1.

Tick Timer

The Tick Timer is a user programmable timer in the ACC. It can be set to one of two different modes by the TICKM bit in the ACC Control and Status Register: normal or fast. In normal mode, the interval can be set to 5, 10, 50, or 100 ms. In fast mode, the interval can be set to 0.2, 0.4, 2.0, or 4.0 ms. The intervals are selected by the TLEN1 and TLEN0 bits in the ACC General Control Register. The TICK pin of the ACC is asserted (driven low) each time the timer expires and remains asserted until software resets it via the CLRTIK bit in ACC Status Register 0.

Assertions of the TICK pin are at multiples of the selected interval, not a new interval from the 0 to 1 transition of CLRTIK.

The TICK pin generates the Tick Timer Interrupt Request through the LIRQ2 pin of the ACC. The Tick Timer Interrupt Request can be disabled by setting the ETTI bit (6) in System Control Register 2. The current state of the TICK pin can be determined by reading the ITIP bits in System Status Register 3 and the LI2 bit in the ACC Local Interrupt Status Register. If LI2 is asserted (1 = asserted) and ITIP0, ITIP1, and ITIP2 are all negated (0) then a Tick Timer Interrupt Request is pending. After reset, the Tick Timer Interrupt Request is enabled, maintaining compatibility with PT-VME151.

An interrupt on the LIRQ2 pin can be programmed (in the ACC Local Interrupts 3 and 2 Control Register) to generate an auto-vector operation on any one of the 68040's seven interrupt request levels. See "Timer Event" on page 41.

This timer is not used by any PTI supplied software or firmware.

Register Block

The ACC is a byte wide device with 16 directly addressable internal registers. Status bits, such as active interrupts, are generally sampled by the ACC at the start of a register access cycle to ensure stable data for the reference. Control bits with the exception of INT on the VMEbus Interrupter register, are always stable. Detailed descriptions of the registers are available in the AVICS Technical Manual. A summary is provided in the Appendix.

Interrupt Handler

The ACC Interrupt Handler prioritizes interrupts from dedicated local level 7 sources, general purpose local sources and the VMEbus. The Interrupt Handler also allows each source to be individually enabled, each of the six general purpose sources to be mapped to any of the seven interrupt levels and the status of any local interrupt to be read.

In the case of multiple active interrupts on a level that is being acknowledged, auto-vector sources have the highest priority followed by local vectored interrupts and finally, VMEbus interrupts. Details of PT-VME151A use of the ACC interrupt inputs follows:

Local Level 7 Sources

On the ACC there are five interrupts dedicated to level 7: the internal BI-mode signal and the external L7INMI, L7IMEM, L7IACF and L7ISYF signals. On the schematics ACC symbol the

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

four external signals are labeled L7I0(NMI) [-INTP<6>], L7I1(MEM) [-INTP<7>], L7I2(ACF) [-INTP<8>], and L7I3(SYF) [- INTP<9>], respectively. For detailed information on the operation of the Level 7 interrupt mechanisms and the BI-mode signal refer to the AVICS Technical Manual.

Abort

Pressing the ABORT button on the front panel will generate a non-maskable interrupt to the 68040. This interrupt request cannot be disabled. This input is edge sensitive and can be reset by writing a zero to control bit NMIIE in ACC Level 7 Interrupt Status Register. The current state of this signal can be read in the NMIIP status bit of the ACC Status Register 0.

SCSI Bus Reset

When a RESET condition [RST] occurs on the SCSIbus a L7IMEM interrupt is generated in the ACC. The interrupt is enabled by setting the MEMIS bit in the ACC Level 7 Interrupt Status Register. The SCSI RESET condition is used to immediately clear all SCSI devices from the bus. The current state of this signal can be read in the MEMIP status bit of the ACC Status Register 0.

An L7IMEM interrrupt is also generated if a parity error occurs during a SCSI DMA cycles or DARF64 local bus master cycles. System Status Register 2 must be read to detrmine the source of the interrupt. See “Parity” on page 30 for more information.

AC Fail

If the VMEbus [ACFAIL*] signal is asserted an interrupt can be generated to the 68040. The AC Failure warning allows the PT-VME151A software to execute appropriate shutdown procedures. The interrupt is enabled by setting the ACFIS bit in the ACC Level 7 Interrupt Status Register. The current state of this signal can be read in the ACFIP status bit of the ACC Status Register 0.

System Fail

If the VMEbus [SYSFAIL*] signal is asserted an interrupt can be generated to the 68040. SYSFAIL is typically used by a board to indicate to the system that it has detected a catastrophic error. Software can then execute the appropriate recovery procedures. The interrupt is enabled by setting the SYFIS bit in the ACC Level 7 Interrupt Status Register. The current state of this signal can be read in the SYFIP status bit of the ACC Status Register 0.

General Purpose Local Interrupts

The six General Purpose Local Interrupts [-INTP<5-0>] can be mapped to any of the seven CPU interrupt request levels. Each have their own enable and status bits. On the schematics ACC symbol, the six external signals are labeled -LIRQ5 through -LIRQ0.

General Purpose Local Interrupts 3 through 0 [-INTP<3-0>] are “auto-vector” only to the 68040. The AVICS allows General Purpose Local Interrupts 5 and 4 [-INTP<5-4>] to be configured as “vectored” or “auto-vectored” to the 68040. The PT-VME151A/151AE hardware implementation requires that General Purpose Local Interrupts 5 and 4 always be configured as

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

"vectored" for the EPAK and DUART interfaces. The vector is supplied by the interrupting device, not the AVICS 64, during the interrupt acknowledge cycle.

Location Monitor FIFO

This interrupt indicates that there are entries in the DARF64 Location Monitor FIFO. It will remain active until the FIFO becomes empty.

The interrupt is enabled by setting the L0E bit in the ACC Local Interrupt Enable Register. The current state of this signal can be read in the LI0 status bit of the ACC Local Interrupt Status Register. The interrupt request level presented to the 68040 is determined by 0L2, 0L1, and 0L0 control bits in the ACC Local Interrupts 1 and 0 Control Register. The DARF64 -LMINT output drives the ACC interrupt input pin -LIRQ0 through signal line [-INTP<0>].

DARF64 VME Event

This interrupt indicates that an event related to VMEbus use has occurred - such as DMA has finished or a bus error (DARF64 [-KBER] or VMEbus [BERR*]) has occurred. It is negated when the appropriate flags in the DARF64 status register are cleared.

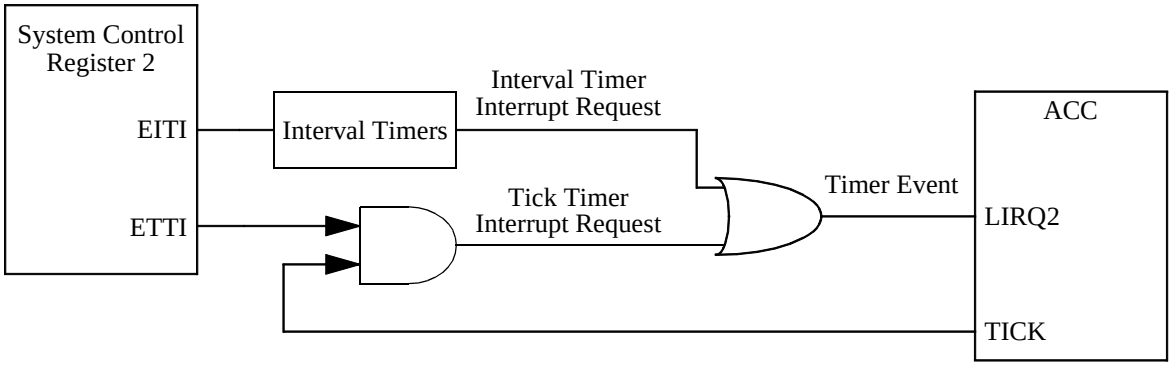
The interrupt is enabled by setting the L1E bit in the ACC Local Interrupt Enable Register. The current state of this signal can be read in the LI1 status bit of the ACC Local Interrupt Status Register. The interrupt request level presented to the 68040 is determined by 1L2, 1L1, and 1L0 control bits in the ACC Local Interrupts 1 and 0 Control Register. The DARF64 -VMEINT output drives the ACC interrupt input pin -LIRQ1 through signal line [-INTP<1>].

Timer Event

The outputs of the Tick Timer and three Interval Timers are OR'ed together generating a single interrupt to the CPU. This interrupt indicates that a Timer period has expired.

The Timer Event interrupt is enabled by setting the L2E bit in the ACC Local Interrupt Enable Register. The current state of this signal can be read in the LI2 status bit of the ACC Local Interrupt Status Register. The interrupt request level presented to the 68040 is determined by 2L2, 2L1, and 2L0 control bits in the ACC Local Interrupts 3 and 2 Control Register.

Figure 12: Timer Block Diagram



Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

The ACC interrupt input is driven by the logical OR of the ACC TICK output and the 82C54 interrupt output. System Status Register 3 identifies the source of the Timer Event.

After reset, the Tick Timer interrupts are enabled and the Interval Timer interrupts are disabled to maintain compatibility with PT-VME151.

Tick

The output of the Tick Timer is negated by clearing the CLRTIK control bit in the ACC Status Register 0.

Interrupts from the Tick Timer can be disabled by clearing the ETTI bit (6) in System Control Register 2. See “Tick Timer” on page 39 for more information.

Interval

The latched outputs of the individual Interval Timers may be cleared by writing the appropriate bit combinations to the RITI field of System Control Register 2.

Interrupts from the three Interval Timers can be disabled by clearing the EITI bit (5) in System Control Register 2. See the section “Interval Timer” on page 32.

I/O Event

This input to the ACC is the logical OR of the Fast SCSI Processor Chip (FAS216) Interrupt Request and the EPAK Interrupt Request.

FAS216 Requests

This interrupt indicates that an event related to the FAS216 operation has occurred - such as a SCSI state sequence has completed. It is negated by a hardware or software reset to the FAS216 or a read from the FAS216 Interrupt Register.

The FAS216 does not provide a single mechanism (or bit) to disable all interrupt requests. Individual interrupt sources can be controlled within the chip, see the FAS216 documentation for more information. The current state of FAS216 Interrupt Request signal (INT) can be read in the INT status bit of the FAS216 Status Register.

EPAK Requests (-EPIRQ)

The EPAK module can request 68040 interrupt service. It is typically used by EPAK devices that do not support vectored interrupt requests. It is negated when the appropriate flags in the EPAK module are cleared.

The ability to disable or check the state of this interrupt request is a function of the EPAK module design.

The interrupt is enabled by setting the L3E bit in the ACC Local Interrupt Enable Register. The current state of this signal can be read in the LI3 status bit of the ACC Local Interrupt Status Register. The interrupt request level presented to the 68040 is determined by 3L2, 3L1, and 3L0 control bits in the ACC Local Interrupts 3 and 2 Control Register. The ACC interrupt input is driven by the FAS216 INT or the EPAK EPIRQ signal. The FAS216 INT

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

[-SCINT] or the EPAK [-EPIRQ] signals drive the ACC interrupt input pin -LIRQ3 through signal line [-INTP<3>].

EPAK Vectored Interrupt Request

This interrupt is driven by the EPAK Vectored Interrupt Request signal [-EPVIR]. When the 68040 acknowledges the interrupt the ACC asserts EPAK Vectored Interrupt Acknowledge (-EPVIA) back to the EPAK module. The interrupt request is negated automatically by logic on the EPAK that responds to the interrupt acknowledge (-EPVIA) generated by the ACC.

The interrupt is enabled by setting the L4E bit in the ACC Local Interrupt Enable Register. The current state of this signal can be read in the LI4 status bit of the ACC Local Interrupt Status Register. The interrupt request level presented to the 68040 is determined by 4L2, 4L1, and 4L0 control bits in the ACC Local Interrupts 5 and 4 Control Register. The 4AV bit in the ACC Local Interrupts 5 and 4 Control Register determines whether a “vectored” or “auto-vectored” interrupt is presented to the 68040. The EPAK [-EPVIR] signal drives the ACC interrupt input pin -LIRQ4 through signal line [-INTP<4>].



CAUTION: Due to the PT-VME151A/151AE hardware implementation the “vectored” option must always be used for the ACC Local Interrupts 5 and 4 Control Register 4AV bit.

DUART Interrupt Request (-INTP<5>)

This interrupt is driven by the DUART Interrupt Request signal. When the 68040 acknowledges the interrupt the ACC asserts an interrupt acknowledge (-INTA<5>) back to the DUART. The interrupt request is negated by servicing the appropriate interrupt source in the DUART.

The interrupt is enabled by setting the L5E bit in the ACC Local Interrupt Enable Register. The current state of this signal can be read in the LI5 status bit of the ACC Local Interrupt Status Register. The interrupt request level presented to the 68040 is determined by 5L2, 5L1, and 5L0 control bits in the ACC Local Interrupts 5 and 4 Control Register. The 5AV bit in the ACC Local Interrupts 5 and 4 Control Register determines whether a “vectored” or “auto-vectored” interrupt is presented to the 68040. The DUART IRQ pin drives the ACC interrupt input pin -LIRQ5 through signal line [-INTP<5>].



CAUTION: Due to the PT-VME151A/151AE hardware implementation the “vectored” option must always be used for the ACC Local Interrupts 5 and 4 Control Register 5AV bit.

VMEbus Interrupts

The VMEbus interrupts map directly onto the 68040 CPU interrupt levels. Each has its own enable bit and each is always vectored. All VMEbus interrupts are level sensitive and not latched, nor can their status be directly determined, with the exception or IRQ1*. See the AVICS Technical Manual for more information on this exception.

The ACC VMEbus Interrupt Enable Register allows the individual interrupt request levels to be enabled or disabled.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Interrupt Acknowledgment

The ACC interrupt handler generates the acknowledgment signals during the 68040 IACK cycle to: auto-vector the cycle, indicate to Local Interrupt level 5 and 4 requesters that they must supply a vector, or requests the DARF64 to obtain the VMEbus for a VMEbus interrupt acknowledge cycle.

The order of priorities within any given interrupt request level is auto-vector first, followed by Local Interrupt level 5 and 4 and finally VMEbus.

VMEbus Requester

Several request and release modes can be selected via the ACC Requester Control Register. The bus release options include: Bus Clear [BCLR*], VMEbus ownership timer, and Release on Request (ROR) or Release when Done (RWD).

System Monitor Functions

The ACC is capable of providing VMEbus System Controller functions. These include Bus Arbitration, System Clock Driver, IACK Daisy Chain Driver and Bus Timer. The PT-VME151A does not generate the AC Failure detection feature of the VMEbus Power Monitor [ACFAIL*] however, it is capable of monitoring the signal. The VMEbus Serial Clock Driver functions are not provided.

The ACC samples the VMEbus signal [BG3IN*] shortly after the PT-VME151A detects a power on condition and on every negating edge of VMEbus [SYSRST*]. If [BG3IN*] is low, the ACC enables itself as the VMEbus System Controller. The System Controller functions will be enabled automatically if the PT-VME151A is in slot 1 and [BG3IN*] is open. Software can determine if this has occurred by reading the SYSC status bit of the ACC Status Register 1.



CAUTION: The PT-VME151A requires that the card preceding in the bus grant daisy chain adhere to the IEEE 1014 (VMEbus) rule that requires all Bus Grant outputs to be driven high during reset. If the preceding card is driving [BG3OUT*] low at the end of reset, a system malfunction could result.

Reset

The VMEbus [SYSRST*] signal can always be driven by the ACC, whether or not it is the System Controller. There are three conditions under which [SYSRST*] is driven: the PT-VME151A detects a power on condition, VMEbus [BG0IN*] is asserted (while System Controller), or software sets the SWRST bit in the ACC General Control Register.

System Clock Driver

If the PT-VME151A is the System Controller the 16 MHz, 50% duty cycle [SYSCLK] signal will be generated on the VMEbus.

VMEbus Arbiter

Only enabled when the PT-VME151A is the System Controller, the VMEbus Arbiter provides four programmable arbitration schemes along with arbitration time-out.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

The arbitration mode is determined by the ARB1 and ARB0 bits in the ACC VMEbus Arbiter Register. The possible modes are: Full Round Robin. Bus Request Level 3 has priority over levels 2, 1, and 0 which are handled in Round Robin mode. Bus Request Levels 3 and 2 have priority over levels 1 and 0 which are handled in Round Robin mode. And, full Priority mode.

Arbitration time-out is enabled by the ATEN bit in the ACC VMEbus Arbiter Register. The Bus Grant issued by the arbiter will be withdrawn after 16 us, if no card asserts BBSY* to take ownership of the VMEbus. The arbiter then waits 16 us to allow the deasserted grant to fully propagate through the daisy chain, then rearbitrates the bus.

IACK Daisy Chain Driver

The IACK Daisy Chain Driver (DCD) performs the standard VMEbus System Controller IACK DCD function, as well as providing the VMEbus Interrupt Generator logic.

Bus Timer

The ACC as System Controller provides VMEbus Data Transfer Time-out functionality. VMEbus data transfers are terminated with the error signal BERR*, if a slave does not respond within a programmed time. The time-out period may be 16, 32, or 64 us, or “never”. The default value after reset is 64 us. The VXL1 and VXL0 control bits in the ACC VMEbus Arbiter Register determine the time-out period.

I/O UTILITIES

System Control Registers

The System Control Registers provide the PT-VME151A with miscellaneous control functions not provided in other registers. They are all 8-bit, read/write registers.

These registers can be read back. This allows the use of AND or OR instructions to clear and set individual bits.



CAUTION: These registers should only be referenced using byte operations! Reading any of them as a word or longword will be translated into multiple byte reads by the sizing logic, with the same data byte being repeated on each reference. Writing them as a word or longword can cause problems because the bus sizing forces multiple byte writes to occur. This will leave only the last (most significant) byte in the selected register. The other bytes will have previously been pumped through the register and if they are not identical to the MSB the respective bits of the control register will toggle.

System Control Register 1

System Control Register 1 is an 8-bit, read/write register. All bits are cleared to zero (0) by Local Reset. It resides at location 0D000000h.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

VMEbus Page Select

Access to the VMEbus address space is through the local addresses 80000000h-FFFFFFFFh. In order to access the full VMEbus address space, the VMEbus Page Select bit (VPG) in the System Control Register is used to define VMEbus address bit 31. When the VMEbus Page Select bit is 0, PT-VME151A addresses 80000000h-FFFFFFFFh are mapped to VMEbus addresses 00000000h - 7FFFFFFFh. When the VMEbus Page Select bit is 1, PT-VME151A addresses 80000000h-FFFFFFFFh are mapped to VMEbus addresses 80000000h-FFFFFFFFh. Local Reset clears (0) this bit.

User LEDs

There are four LEDs on the front panel (D3, D2, D1, and D0) that are under program control. Writing a one to the LED3-LED0 bits in the System Control Register will light the respective LED. When Local Reset is asserted all the four LEDs will be turned off.

SCSI DMA Read/Write Direction

SDIR in the System Control Register determines the direction of a data transfer during a SCSI DMA operation. Setting this bit will generate data movement from DRAM to the FAS216, a write to the SCSI bus. Clearing it moves data from the FAS216 to DRAM, a read from the SCSI bus. Local Reset clears (0) this bit (SCSI DMA Read).

EPAK Space Cache Enable

The ability to cache information in the EPAK address space (30000000h-3FFFFFFFh) is determined by the MC68040 Transparent Translation Registers. This makes the Enable EPAK Caching bit of the Control Register irrelevant. Below are the possible combinations of events:

Table 1: EPAK Caching Options

68040 DTTR EPAK Cache Enable	VME151 Control Register EPAK Cache Enable	EPAK Caching?
Disabled	Don’t Care	No (Normal mode)
Enabled	True	Yes
Enabled	False	No, but 4 lwords fetched

Local Reset clears (0) this bit, enabling caching. See “APPENDIX F: PT-VME151A Differences From VME131/141” on page 91 for an in-depth discussion of EPAK caching.

VMEbus Space Cache Enable

Reads from the VMEbus address (80000000h-FFFFFFFFh) space can be cached. When the VCE bit in the System Control Register is cleared (0) VMEbus space caching is enabled. When set (1) it is disabled. Local Reset clears (0) this bit, enabling caching.

With respect to VME memory space, VME space is not explicitly affected by the mapping of the MC68040 Transparent Translation Registers (discussed in “PT-VME151A Control Register Differences” on page 93). Therefore, the VME Caching Enable bit in the System Control Register still controls the cacheability of VME address space.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

NOTE: If the VMEbus Page Select bit is toggled while caching is enabled a system failure could result!

System Control Register 2

System Control Register 2 is an 8-bit, read/write register. All bits except ETTI are cleared to zero (0) by Local Reset. ETTI is set to 1 by Local Reset. This register resides at location 50000000h.

Enable EPAK Access from the VMEbus

The EPAK expansion module can be accessed by a VMEbus master as part of the PT-VME151A slave image when the EEAV bit is 0, the VMEbus address bit 24 is 1, and the A32SIZ field of the DARF VMEBAR register is programmed to allow a A32 Slave Image Size greater than or equal to 32MBytes (Dh). In this case a portion of the PT-VME151A slave image is replaced by the EPAK's address space. When EPAK accesses from the VMEbus are disabled, all of the PT-VME151A installed DRAM may be accessed by a VMEbus master. EEAV is cleared at reset, enable EPAK access. EEAV is register bit 0.

Enable Parity Error Checking

Parity generation and checking is available for the 16M, 32M, and 64M DRAM configurations. When EPEC is 1, parity checking is enabled for all DRAM reads. Parity errors detected during 68040 or EPAK DRAM reads will return a Bus Error to the respective device. Parity errors detected during SCSI DMA transfers or DARF64 Local Bus Master cycles will result in an interrupt request on the ACC's L7IMEM input. The source of the error may be determined by reading System Status Register 2. See "System Status Register 2" on page 50.

Parity is generated and stored on all DRAM write cycles, regardless of the state of EPEC. If parity is not available (4M or 8M configurations), parity checking is disabled and EPEC will be ignored. Reset clears EPEC, disabling parity checking.

NOTE: EPEC should **never** be set while EBP is set. See "Enable Bad Parity" below.

EPEC is register bit 1.

Enable Bad Parity

For testing purposes it may be desirable to force parity errors. When EBP is 1, the parity bit written to DRAM with the data is complemented, generating faulty parity. Subsequent read cycles from the same address will generate parity errors until good parity is written.

NOTE: EBP should **never** be set while EPEC is set. Otherwise each DRAM write will generate a parity error.

It should be kept in mind that the 68040 may reorder a sequence of reads and writes in a code segment. NOPs should be placed in the instruction stream to eliminate the effect. The code segment to write bad parity should be as follows:

```
NOP
move.b  #$04,$50000000     ;Set EBP and clear EPEC
```


Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

```
NOP
  [Move data with bad parity to DRAM addresses]
NOP
move.b  #$02,$50000000     ;Clear EBP and Set EPEC
```

EBP is always cleared at reset allowing good parity to be written. EBP is register bit 2.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Reset Interval Timer Interrupts

The RITI bits are encoded to reset the Request Latch of the individual Interval Timers. When an Interval Timer reaches it's terminal count, the event is recorded by its Request Latch. The outputs of the three Request Latches are OR'ed together, generating the Interval Timer Interrupt Request to the 68040. The interrupt request from an individual Interval Timer remains active until its Request Latch is reset using this field.

Value	Function
3	Reset Interval Timer 2 Request Latch
2	Reset Interval Timer 1 Request Latch
1	Reset Interval Timer 0 Request Latch
0	No action

RITI is a two bit field. It consists of register bits 3 and 4, where bit 3 is the least significant bit. This field is always read as 0.

Enable Interval Timer Interrupts

All interrupt requests from the three Interval Timers can disabled. When the EITI bit in System Control Register 2 is cleared (0) Interval Timer interrupt requests are disabled. When set (1) they are enabled. Local Reset clears (0) this bit, disabling Interval Timer interrupts. EITI is register bit 5.

Enable Tick Timer Interrupts

Interrupt requests from the ACC Tick Timer can disabled. When the ETTI bit in System Control Register 2 is cleared (0) Tick Timer interrupt requests are disabled. When set (1) they are enabled. Local Reset sets (1) this bit, enabling Tick Timer interrupts. ETTI is register bit 6.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

System Status Registers

The System Status register provides the PT-VME151A with status information not provided in other registers. It is a read only register. All unused bits (31-4) should be masked to zero (0) for future expansion.

This register should only be referenced using byte operations. Reading it as a word or longword will be translated into multiple byte reads by the sizing logic, with the same data byte being repeated on each reference.

System Status Register 1

System Status Register 1 is an 8-bit, read only register. This register resides at location 0C000000h.

Hex Switch

The current setting of the front panel hexadecimal switch can be read through this register. The hex switch value will be presented as a nibble on data bits 3-0 at location 0C000000h (bit 0 is the least significant bit). This four bit field is referred to as HSW.

System Status Register 2

System Status Register 2 is an 8-bit, read only register. This register resides at location 60000000h.

68040 Parity Error

When the 68040 Parity Error bit (named 040PE) is read as 1, it indicates that a parity was detected during a 68040 DRAM read cycle. Notification of the error is though a Bus Error that is generated as a acknowledgment on the DRAM reference. The Bus Error Handler must check this bit to determine if bad DRAM parity was the source of the Bus Error. 040PE is cleared by reset and after each time System Status Register 2 is read. 040PE is register bit 1.

SCSI DMA Parity Error

When the SCSI DMA Parity Error bit (named SDMAPE) is read as 1, it indicates that a parity was detected during a SCSI DMA DRAM read cycle. Notification of the error is though a level 7 Interrupt to the 68040 that is generated immediately after the DRAM reference in error. The Level 7 Interrupt Handler must check this bit to determine if bad DRAM parity was the source of the interrupt. SDMAPE is cleared by reset and after each time System Status Register 2 is read. SDMAPE is register bit 2.

DARF Parity Error

When the DARF Parity Error bit (named DARFPE) is read as 1, it indicates that a parity was detected during a DARF DRAM read cycle. Notification of the error is though a level 7 Interrupt to the 68040 that is generated immediately after the DRAM reference in error. The Level 7 Interrupt Handler must check this bit to determine if bad DRAM parity was the source of the interrupt. DARFPE is cleared by reset and after each time System Status Register 2 is read. DARFPE is register bit 3.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

EPAK Parity Error

When the EPAK Parity Error bit (named EPAKPE) is read as 1, it indicates that a parity was detected during a DRAM read cycle by an EPAK master. Notification of the error is though a Bus Error that is generated as a acknowledgment to the EPAK module on the DRAM reference. The Bus Error Handler for the EPAK must check this bit to determine if bad DRAM parity was the source of the Bus Error. EPAKPE is cleared by reset and after each time System Status Register 2 is read. EPAKPE is register bit 4.

SCSI Present

When the SCSI Present bit (named SCSIP) is read as 1, it indicates that the SCSI controller and associated logic is installed. SCSIP is register bit 5.

System Status Register 3

System Status Register 3 is an 8-bit, read only register. This register resides at location 68000000h.

DRAM Size

The DRAM Size field (named DRAMSZ) indicates the size of the DRAM module installed on the PT-VME151A base board. DRAMSZ is a three bit field. It consists of register bits 0 through 2, where bit 0 is the least significant bit. The following table elaborates the possible values:

Value	DRAM Size
7-5	Reserved
4	64 Meg
3	32 Meg
2	16 Meg
1	8 Meg
0	4 Meg

Parity Installed

If equal to 1, the Parity Installed bit (named PARI) indicates parity logic and memory is populated on the DRAM module. PARI is register bit 3.

Interval Timer Interrupt Pending

The ITIP bits reflect the state of the respective Interval Timer Request Latch. When set (1) the bit indicates that the Interval Timer's OUTPUT pin has been asserted. These bits will remain set until explicitly reset using the RITI field in System Control Register 2. After Local Reset all ITIP bits will be cleared (0). ITIP0, ITIP1, and ITIP2 correspond to register bits 4, 5, and 6, respectively.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

DUART

The Motorola Dual Asynchronous Receiver/Transmitter (MC68681 DUART) provides a General Purpose Timer, Parallel Input and Output Ports, besides the dual Serial Port capability.

Utility Serial Ports

The DUART provides two general purpose asynchronous serial ports. Port “A” is equipped with basic modem controls: DTR, DSR, RTS, CTS. Port “B” is transmit and receive data only. Both ports are equipped with RS-232 line drivers and receivers. The baud rate for each port can be set independently over the common asynchronous speed range (50 to 38.4K baud). The ports can be controlled via interrupts or polled I/O.

If you recieved a Performance Computer Debugger (PTBUG) as part of your order, Port A of the DUART will be set to 9600 baud, 1 stop bit, no parity. PTBUG ignores CTS and DTR and deasserts RTS and DSR (false).

The Utility Serial Port interconnect is located on the front panel and uses a 14-pin dual row pin header connector.

General Purpose Timer/Counter

The General Purpose Timer is a flexible user programmable 16-bit counter/timer. The clock source of the timer is derived from the 3.6864 MHz crystal attached to the DUART. Parallel Output Port pin 3 can be programmed as an output of the timer allowing EPAK boards to take advantage of this timer function through the [+EPKIO] signal.

DUART parallel Input Port pin 2 is unconnected, therefore the “External (IP2)” clock sources identified in the Counter/Timer Mode and Source Select field of the DUART Auxiliary Control Register (ACR[6:4]) are not valid choices.

This timer is used by OS-9 for its real-time clock. For detailed information on the DUART and the General Purpose Timer/Counter refer to the MC68681 Multi-Function Peripheral Specification.

Parallel Input Port

Clear-to-Send

Parallel Input 0 of the DUART is attached to the RS-232 Clear-to-Send (CTS) receiver for Serial Port “A”. To allow CTS to act as a hardware enable for the transmitter, CTS Enable Transmitter bit (4) in DUART Channel A Mode Register must be set to 1. The state of this control signal can be read from IP0 bit (0) of the DUART Input Port Register.

Data-Terminal-Ready

Parallel Input 1 of the DUART is attached to the RS-232 Data-Terminal-Ready (DTR) receiver for Serial Port “A”. The state of this control signal can be read from the IP1 bit (1) of the DUART Input Port Register.

The DUART is capable of generating an interrupt to the 68040 if a change of state occurs on this signal. To accomplish this, the Delta IP1 IRQ bit (1) of the DUART Auxiliary Control Register must be set and the ACC registers associated with the DUART Interrupt Request must be setup.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

EPAK General Purpose Input

Parallel Input 3 of the DUART is attached to the EPAK +EPKIO signal. The state of this control signal can be read from the IP3 bit (3) of the DUART Input Port Register. The function of this pin is determined by the attached EPAK Expansion Module.

The DUART is capable of generating an interrupt to the 68040 if a change of state occurs on this signal. To accomplish this, the Delta IP3 IRQ bit (3) of the DUART Auxiliary Control Register must be set, and the ACC registers associated with the DUART Interrupt Request must be setup.

Serial EEPROM Data In

Parallel Input 5 of the DUART is attached to the Data Out (DO) pin of the 93C46 Serial EEPROM. The state of this control signal can be read from the IP5 bit (5) of the DUART Input Port Register.

Parallel Output Port

Request-to-Send

Parallel Output 0 of the DUART is attached to the RS-232 Request-to-Send (RTS) transmitter for Serial Port “A”. To allow RTS to act as a hardware indicator that the channel A transmit FIFO has data ready to send, Tx RTS Control bit (5) in DUART Channel A Mode Register must be set to 1. Programmed I/O can control the state of this signal with the OPR0 bit (0) of the DUART Output Port Register.

Data-Set-Ready

Parallel Output 1 of the DUART is attached to the RS-232 Data- Set-Ready (DSR) transmitter for Serial Port “A”. Programmed I/O can control the state of this signal with OPR1 bit (1) of the DUART Output Port Register.

EPAK General Purpose Output

Parallel Output 3 of the DUART is attached to the EPAK +EPKIO signal. The state of this control signal can be controlled by the OPR3 bit (3) of the DUART Output Port Register. The function of this pin is determined by the attached EPAK Expansion Module.

Serial EEPROM Select

Parallel Output 5 of the DUART is attached to the Chip Select (CS) pin of the 93C46 Serial EEPROM. Programmed I/O can control the state of this signal with the OPR5 bit (5) of the DUART Output Port Register.

Serial EEPROM Control

Parallel Output 6 of the DUART is attached to the Control (SK) pin of the 93C46 Serial EEPROM. Programmed I/O can control the state of this signal with the OPR6 bit (6) of the DUART Output Port Register.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Serial EEPROM Data Out

Parallel Output 7 of the DUART is attached to the Data In (DI) pin of the 93C46 Serial EEPROM. Programmed I/O can control the state of this signal with OPR7 bit (7) of the DUART Output Port Register.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SCSI Controller

The Emulex FAS126 Fast SCSI Processor Chip is a high performance CMOS device that conforms to the ANSI standards, X3.131-1986 (SCSI-1) and X3T9.2/86-109 Rev.10c (SCSI-2), for Small Computer Systems Interface (SCSI). An 8-bit bus provides FAS216 register access to the 68040. The FAS216's internal sequencer is capable of performing common SCSI algorithms, or sequences, in response to a single command, thus reducing the SCSIbus protocol overhead.

The FAS216 uses a register superset of the NCR 53C94 used on the PT-VME131 to provide SCSI-2 functionality. This compatibility offers the user an easy upgrade to SCSI-2 performance.

The FAS216 is permanently strapped in Bus Configuration Mode 2 (dual bus, multiplexed, byte control, 16-bit DMA transfers). Also, because of the hardware implementation, the "Alternate DMA mode" option in FAS216 Configuration Register 3 must not be enabled.

The FAS216 is driven with a 40 MHz (25 ns.) clock. Various programmable parameters derive their timing from this clock.

SCSI Bus

The FAS216 incorporates on-chip 48 mA drivers for single-ended (TTL) transmission. It is capable of operating at a sustained data transfer rate of up to 5 megabytes per second (SCSI-1) and 10 megabytes per second (SCSI-2) synchronous modes or 7 megabytes per second in asynchronous mode. Parity generation and checking is optional on all SCSI bus transfers.

The SCSI interface is through the P2 VME connector. Termination is provided by optional plug-in resistor packs. The resistor packs should be installed if the PT-VME151A is at either end of a SCSI cable. Conversely, the resistor packs should be removed if the PT-VME151A is installed in the middle of the SCSI cable.

The local SCSI termination circuit draws its power from the SCSI TERMPWR signal [TPWR]. Jumper K6 determines whether the PT-VME151A sources SCSI TERMPWR [TPWR] (pins 1-2 shunted) or not (pins 1-2 open).

A 1 amp fuse (Littelfuse 273-001) protects the SCSI termination power [TPWR] from short circuit conditions.

For more information see " SCSI Termination" on page 17 and " SCSI Considerations" on page 23.

Register Access

The sixteen internal register locations of the FAS216 reside at locations 0A000000h through 0A00000Fh in the 68040's address space. They are accessed through the 8-bit Buffered Data/Address bus attached to bits <24:31> of the MicroProcessor Data Bus. The PT-VME151A incorporates logic that invokes the dynamic bus sizing mechanism of the 68040 forcing byte operations on any size reference to the 8-bit Buffered Data/Address Bus.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

DMA Mechanism

SCSI data phase bytes can be transferred with Direct Memory Access of the PT-VME151A. Under program control the following steps must be performed to initiate a SCSI DMA transfer:

The SCSI Memory Address Register must be loaded with the source/destination address for the transfer.

The System Control Register, SCSI DMA Read/Write Direction (SCDRD) bit is written to indicate to the PT-VME151A control logic the direction of the transfer.

The FAS216 Transfer Count register is loaded with the desired size of the transfer (up to 64 KBytes).

Issue a data transfer command to the FAS216.

The hardware will handle the data transfer between the FAS216 and local DRAM.

Parity is generated and checked by PT-VME151A hardware on local DRAM accesses during SCSI DMA. A level 7 interrrupt may be generated if a parity error is detected. See “Parity” on page 30 for more information.

Interrupts

The 68040 can be notified of the completion of an operation of a change in state through the interrupt mechanism provided on the FAS216 and ACC. The FAS216 Interrupt Register, in conjunction with the FAS216 Status and FAS216 Sequence Step registers, are used to determine the source of an FAS216 interrupt.

For FAS216 interrupts to be forwarded to the 68040 the ACC the interrupt mechanism must be enabled by setting the L3E bit in the ACC Local Interrupt Enable Register. The current state of this signal can be read in the LI3 status bit of the ACC Local Interrupt Status Register. See the VMEbus Interface, ACC, General Purpose Local Interrupts, I/O Event, FAS216 Requests section above for further information.

NOTE: The ACC General Purpose Local Interrupt input is driven by the FAS216 INT or the EPAK EPIRQ signal!

A second interrupt mechanism exists that allows the detection of a RESET condition on the SCSIbus. A Level 7 L7IMEM interrupt can be generated in the ACC. The interrupt is enabled by setting the MEMIS bit in the ACC Level 7 Interrupt Status Register. The current state of this signal can be read in the MEMIP status bit of the ACC Status Register 0. See VMEbus Interface, ACC, Interrupt Handler, Local Level 7 Sources section above.

See the FAS216 Technical Manual for more information on the Fast SCSI Processor Chip.

Termination

Fuse F1 (Littelfuse Part No. 273-001) provides short circuit protection for TERMPWR. To remove the fuse, place the PT-VME151A on a work surface component side up with the VMEbus connectors closest to the observer. Grip the clear body of fuse F1 and pull to the right. To replace the fuse reverse the

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

process. The bidirectional arrow in “Figure 6: SCSI Components” on page 17 shows the direction of motion.

See “TERMPWR Overview” on page 17 for a discussion of the uses of TERMPWR.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

EPAK Interface

The Performance Technologies family of Single Board Controllers features provisions for user defined expansion modules. Two basic expansion module strategies are available. The “EPAK” is a 3" x 9" mezzanine board which is intended for applications that must be limited to a single slot. The “EBOARD” is a full-sized VMEbus 6U module which requires the use of a second slot. EBOARDs may be designed with or without backplane access.

The interface between the PT-VME151A and the expansion module is implemented using three 36-pin connector strips (referred to in the Expansion Module Design Guide as J1, J2, and J3).

The interface is organized such that simple slave expansion modules need to connect only to the J1 connector, which provides 8 bits of address and data and the control signals to support this class of slave. Adding a J2 connector to the expansion module brings the number of address lines up to 24 and the number of data lines up to 16. Full A32:D32 slave, as well as all master expansion modules, must use all three connectors.

Many signals on the expansion module interface are simply extensions of the MC68040 signal of a similar name (MP prefix). Refer to the Motorola MC68040 User’s Manual for additional information on the behavior of these signals. Other signals are annotated as “Expansion” (EP prefix) and are uniquely defined for this application.

The PT-VME151A partitions the expansion module (EPAK) memory space into two regions: the first requires that the expansion module generate Data Size Acknowledgments (-EPSA0,1) to accommodate the timing delay of the selected expansion module slave device, the second region requires no response signal from the expansion module ([-EPSA0] and [-EPSA1] need not be driven). The second region allows zero wait state access to SRAM or registers on an EPAK.

The EPAK may be accessed form the VMEbus as part of the PT-VME151A address space. To do so, VMEbus address bit A24 must be 1, the EEAV bit in System Control Register 2 must be 0, and the A32SIZ field of the DARF VMEBAR register must be programmed to allow an A32 Slave Image Size greater than or equal to 32MBytes (Dh). See “Enable EPAK Access from the VMEbus” on page 47 for more information.

Parity is generated and checked by PT-VME151A hardware on local DRAM accesses by EPAK masters. A Bus Error may be generated as an acknowledgement to a reference if a parity error is detected. See “Parity” on page 30 for more information.

For more information refer to the Expansion Module Design Guide.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Section

4

FUNCTIONAL SUMMARY

Memory Map

Table 2 describes the location of all configuration and operational registers of the PT-VME151A as seen by the MC68040. The sizing column indicates if the device supports data bus sizing.

Table 2: Memory Map

ADDRESS RANGE	DEVICE	WIDTH	SIZING
00000000h-03FFFFFFh	ROM/PROM (U38)	BYTE	Yes
04000000h-07FFFFFFh	ROM/SRAM (U23)	BYTE	Yes
08000000h-0800000Fh	68681 DUART	BYTE	Yes
0A000000h-0A00000Fh	FAS216 SCSI	BYTE	Yes
0C000000h	Status Register 1	BYTE	No
0D000000h	Control Register 1	BYTE	No
0E000000h	SCSI MAR	LWORD only	No
0F000000h	DS1643 RTC	BYTE	No
10000000h-1000000Fh	ACC	BYTE	Yes
18000000h-1800004Ch	DARF64	LWORD only	No
20000000h-2FFFFFFFh	Main Memory	LWORD	Yes
30000000h-37FFFFFFh	EPAK	EPAK defined	
38000000h-38FFFFFFh	EPAK 0 WS	LWORD	Yes
40000000h-4FFFFFFFh	UNASSIGNED		
50000000h	Control Register 2	BYTE	No
60000000h	Status Register 2	BYTE	No
68000000h	Status Register 3	BYTE	No
70000000h-70000003h	82C54 Interval Timer	BYTE	No
80000000h-FFFFFFFFh	VMEbus	Slave Defined	

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Default VMEbus Slave Addressing

If you received a Performance Computer Debugger (PTBUG) as part of your order, the firmware will initialize the DARF VMEbus Base Address Register (VMEBAR) with the value 0060014Ch and the DARF Access Protect Boundary Register (APBR) with 00000001h. These values will result in the following address maps as seen by a VMEbus master.

After PTBUG initialization the PT-VME151A will respond to all Standard and Extended, non-privileged and supervisory, data and program VMEbus accesses. These include 32-bit and 64-bit block transfers. (Address Modifier codes 38h-3Fh and 08h-0Fh.)

NOTE: Due to the way the DARF is initialized by PTBUG, only 4 MBytes of PT-VME151A address space is accessible to the VMEbus. So even though Local Reset enables “EPAK access from the VMEbus” (EEAV in System Control Register 2 = 0), the EPAK address space cannot actually be accessed by a VMEbus master. The A32SIZ field of the DARF VMEBAR register must be re-programmed to allow an A32 Slave Image Size greater than or equal to 32MBytes (Dh).

Table 3 describes the default address map of the PT-VME151A as seen by a VMEbus master using A24 addressing.

Table 3: Default VMEbus A24 Memory Map

ADDRESS RANGE	DEVICE	ACCESS
000000h-00FFFFh	Local DRAM (Write Protected)	BYTE, WORD, LWORD, D32 and D64 BLOCK
010000h-3FFFFBh	Local DRAM	BYTE, WORD, LWORD, D32 and D64 BLOCK
3FFFFCh	Location Monitor	BYTE, WORD, LWORD
400000h-FFFFFFh	UNASSIGNED	

Table 4 describes the default address map of the PT-VME151A as seen by a VMEbus master using A32 addressing.

Table 4: Default VMEbus A32 Memory Map

ADDRESS RANGE	DEVICE	ACCESS
00000000h-5FFFFFFFh	UNASSIGNED	
60000000h-6000FFFFh	Local DRAM (Write Protected)	BYTE, WORD, LWORD, D32 and D64 BLOCK
60010000h-603FFFFBh	Local DRAM	BYTE, WORD, LWORD, D32 and D64 BLOCK
603FFFFCh	Location Monitor	BYTE, WORD, LWORD
60400000h-FFFFFFFFh	UNASSIGNED	

NOTE: An attempt to write PT-VME151A “Write Protected” DRAM will result in a Bus Error being returned to the VMEbus master on the reference.

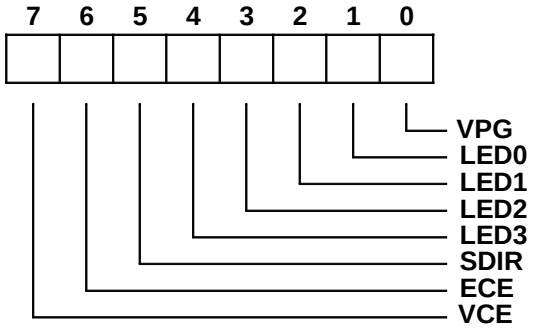
Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

151A System Registers

There are six registers on the PT-VME151A that are not defined in the referenced data sheets. These registers are unique to the PT-VME151A, providing control of major functional blocks and status.

System Control Register 1

Address 0D000000h
Byte Read/Write Only
All bits cleared to zero by reset



Bit	Name	Function
0	VPG	VMEbus Page bit
	1	VME address bit 31=1
	0	VME address bit 31=0
1	LED0	User Programmable LED D0
	1	LED on
	0	LED off
2	LED1	User Programmable LED D1
	1	LED on
	0	LED off
3	LED2	User Programmable LED D2
	1	LED on
	0	LED off
4	LED3	User Programmable LED D3
	1	LED on
	0	LED off
5	SDIR	SCSI DMA Direction
	1	SCSI DMA Write (read from memory)
	0	SCSI DMA Read (write to memory)
6	ECE	Enable MC68040 caching of EPAK accesses. See “PT-VME151A Control Register Differences” on page 93 for in-depth discussion.
		Not Used.

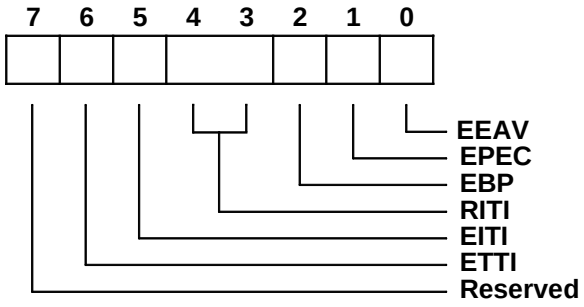
Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

7	VCE	Enable 68040 caching of VMEbus accesses. See “PT-VME151A Control Register Differences” on page 93 for in-depth discussion.
	1	Disable caching
	0	Enable caching

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

System Control Register 2

Address 50000000h
Byte Read/Write Only
All bits cleared to zero by reset, except ETTI



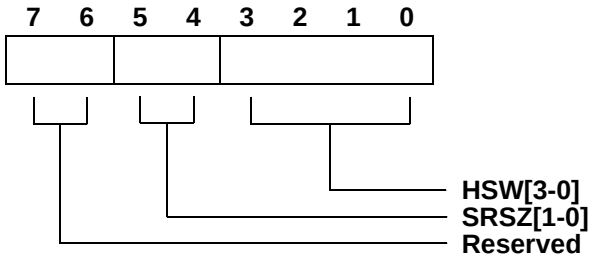
Bit	Name	Function
0	EEAV	Enable EPAK Access from VMEbus
	1	Enable EPAK Access from VMEbus when A24 = 1
	0	Disable EPAK Access from VMEbus
1	EPEC[1,2]	Enable Parity Error Checking
	1	Check for parity errors
	0	Do not check for parity errors
2	EBP[3]	Enable Bad Parity
	1	Write bad parity
	0	Write normal parity
4-3	RITI[4]	Reset Interval Timer Interrupt pending latch
	3	Reset Interval Timer 2 Interrupt Pending Latch
	2	Reset Interval Timer 1 Interrupt Pending Latch
	1	Reset Interval Timer 0 Interrupt Pending Latch
	0	No action
5	EITI	Enable Interval Timer Interrupts
	1	Enable interrupts
	0	Disable interrupts
6	ETTI	Enable Tick Timer Interrupts
	1	Enable interrupts
	0	Disable interrupts
7		Reserved, mask to zero when read

1 DRAM MUST be initialized before parity checking is enabled.
2 DO NOT enable if EBP = 1.
3 DO NOT enable if EPEC = 1.
4 RITI always read as 0.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

System Status Register 1

Address 0C000000h
Byte Read Only



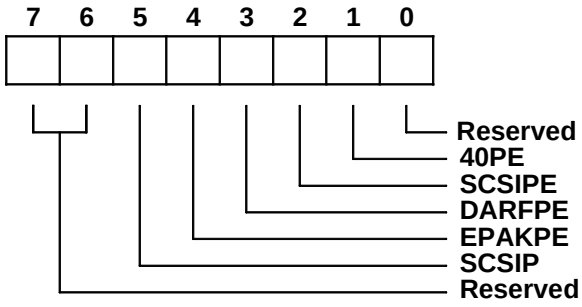
Bits	Name	Function
3-0	HSW	Value of Hex Switch
5-4	SRSZ	SRAM Size[5]
	0	No SRAM installed
7-6		Reserved, mask to zero when read

[5] The PT-VME151A does not support SRAM so this field is always read as zero. This provides backwards compatibility with the PT-VME151.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

System Status Register 2

Address 60000000h
Byte Read Only

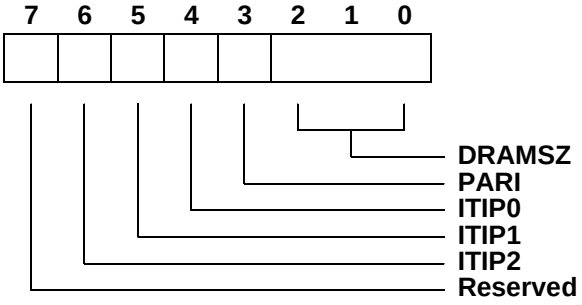


Bit	Name	Function
0		Reserved, mask to zero when read
1	40PE	68040 Parity Error
	1	A parity error was detected during a 68040 DRAM read
	0	No 68040 Parity error since last read of System Status Register 2
2	SDMAPE	SCSI DMA Parity Error
	1	A parity error was detected during a SCSI DMA DRAM read
	0	No SCSI DMA Parity error since last read of System Status Register 2
3	DARFPE	DARF64 Parity Error
	1	A parity error was detected during a DARF64 DRAM read
	0	No DARF64 Parity error since last read of System Status Register 2
4	EPAKPE	EPAK Master Parity Error
	1	A parity error was detected during a EPAK Master DRAM read
	0	No EPAK Parity error since last read of System Status Register 2
5	SCSIP	SCSI Present
	1	SCSI Controller present
	0	SCSI Controller depopulated
7-6		Reserved, mask to zero when read

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

System Status Register 3

Address 68000000h
Byte Read Only

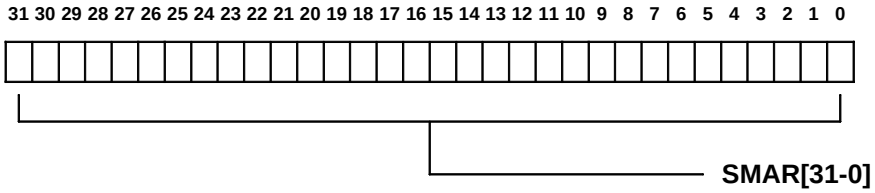


Bit	Name	Function
2-0	DRAMSZ	Indicates the amount of DRAM installed
	7-5	Reserved
	4	64 Meg
	3	32 Meg
	2	16 Meg
	1	8 Meg
	0	4 Meg
3	PARI	Parity Installed
	1	Parity generation and checking logic installed
	0	Parity logic not installed - no parity errors generated
4	ITIP0	Interval Timer 0 Interrupt Pending
	1	Interrupt pending
	0	No interrupt pending
5	ITIP1	Interval Timer 1 Interrupt Pending
	1	Interrupt pending
	0	No interrupt pending
6	ITIP2	Interval Timer 2 Interrupt Pending
	1	Interrupt pending
	0	No interrupt pending
7		Reserved, mask to zero when read

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SCSI Memory Address Register

Address 0E000000h
Write Only



31-0	SMAR	The SCSI Memory Address Register is written with the starting address for a SCSI DMA transfer. The register retains its value after reset and is undefined after power up

Jumper List (Defaults)

This section provides a summary of the jumpers on the PT-VME151A/151AE and their default settings.

JUMPER	DEFAULT (Shorted pins)	FUNCTION
K1	1 to 2	Disables Watchdog Reset
K2	all open	MMU Disable (for MC68040 only)
K3 & K11	K3-8 to K3-9 K3-5 to K3-6 K3-2 to K3-3 K11 all open	U38 ROM/PROM/SRAM socket configuration 64Kx8, 28 pin PROM/ROM device
K4 & K10	K4-26 to K4-27 K4-20 to K4-21 K4-16 to K4-17 K4-11 to K4-12 K4-7 to K4-8 K4-5 to K4-6 K4-2 to K4-3 K10 all open	U23 ROM/PROM socket configuration 64Kx8, 28 pin PROM/ROM device
K5	all open	Reserved (factory configured)
K6	1 to 2	SCSI Term Power select (1-2 = local, open = SCSI bus)
K7	all open	Reserved (factory configured)
K8	1 to 2	4Mb/16Mb DRAM select (1-2 = 4M, factory configured)
K9	1 to 2	4Mb/16Mb DRAM select (2-3 = 16M, factory configured)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Interrupt Control

The ACC controls local and VMEbus interrupts. Because the ACC allows the dynamic assignment of local interrupts to specific request levels, a fixed interrupt map is unnecessary. The following table lists the internal and VMEbus interrupt sources and the levels to which they may be assigned. The ACC interrupt input pin for each local interrupt request is also shown.

Table 5: Interrupt Request Summary

Interrupt Source	Possible Level Assignments	ACC Input
VMEbus IRQ1	1 (or off) Vectored	VIRQ1
VMEbus IRQ2	2 (or off) Vectored	VIRQ2
VMEbus IRQ3	3 (or off) Vectored	VIRQ3
VMEbus IRQ4	4 (or off) Vectored	VIRQ4
VMEbus IRQ5	5 (or off) Vectored	VIRQ5
VMEbus IRQ6	6 (or off) Vectored	VIRQ6
VMEbus IRQ7	7 (or off) Vectored	VIRQ7
Location Monitor	1-7 (or off) Auto-Vectored	LIRQ0
VMEbus Events	1-7 (or off) Auto-Vectored	LIRQ1
Tick & Interval Timer	1-7 (or off) Auto-Vectored	LIRQ2
FAS216 & EPAK [EPIRQ]	1-7 (or off) Auto-Vectored	LIRQ3
EPAK [EPVIR]	1-7 (or off) Vectored	LIRQ4
68681	1-7 (or off) Vectored	LIRQ5
Abort Switch	7 (or off) Auto-Vectored	L7I0
Parity Error & SCSI bus Reset	7 (or off) Auto-Vectored	L7I1
VMEbus [*ACFAIL]	7 (or off) Auto-Vectored	L7I2
VMEbus [*SYSFAIL]	7 (or off) Auto-Vectored	L7I3

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Register Maps

The “INIT” column in the register map descriptions below identify the initial register values typically programmed by PTI for our applications. All “INIT” values are in hexadecimal, registers that are “don’t care” at initialization time contain a hyphen.

ACC

See “APPENDIX F: PT-VME151A Differences From VME131/141” on page 91 for in-depth discussion of initialization issues. See APPENDIX G: and APPENDIX H: for more information.

Table 6: ACC Register Map

ADDRESS	REGISTER	FUNCTION	INIT
10000000h	STAT0	Status Register 0	-
10000001h	STAT1	Status Register 1	-
10000002h	GENCTL	General Control Register	1C
10000003h	VINT	VMEbus Interrupter Register	-
10000004h	VREQ	VMEbus Requester Register	03
10000005h	VARB	VMEbus Arbiter Register	00
10000006h	ID	ID Register	-
10000007h	CTL2	Control Register 2	00
10000008h	7IS	Level 7 Interrupt Status Register	-
10000009h	LIS	Local Interrupt Register	-
1000000Ah	7IE	Level 7 Interrupt Enable Register	-
1000000Bh	LIE	Local Interrupt Enable Register	00
1000000Ch	VIE	VMEbus Interrupt Enable Register	-
1000000Dh	IC10	Local Interrupts 1 and 0 Control	13
1000000Eh	IC32	Local Interrupts 3 and 2 Control	45
1000000Fh	IC54	Local Interrupts 5 and 4 Control	62

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

DARF64

See “APPENDIX F: PT-VME151A Differences From VME131/141” on page 91 for in-depth discussion of initialization issues. See APPENDIX G: and APPENDIX H: for more information.

Table 7: DARF64 Registers

ADDRESS	NAME	FUNCTION	INIT
18000000h	DMALAR	DMA Local Address Register	-
18000004h	DMAVAR	DMA VMEbus Address Register	-
18000008h	DMATC	DMA Transfer Count	-
1800000Ch	DCSR	Control and Status Register	-
18000010h	VMEBAR	VMEbus Slave Base Address Register	-
18000014h	RXDATA	Receive FIFO Data bits output latch	-
18000018h	RXADDR	Receive FIFO Address bits output latch	-
1800001Ch	RXCTL	Receive FIFO Control bits output latch	-
18000020h	BUSSEL	VMEbus Select	-
18000024h	IVECT	VMEbus Interrupt Vector	-
18000028h	APBR	Access Protect Boundary	-
1800002Ch	TXDATA	Transmit FIFO Data bits output latch	-
18000030h	TXADDR	Transmit FIFO Address bits output latch	-
18000034h	TXCTRL	Transmit FIFO Control bits output latch	-
18000038h	LMFIFO	Location Monitor FIFO read port	-
1800003Ch	MODE	Mode Control	-
18000040h	SA64BAR	Slave A64 Base Address Register	-
18000044h	MA64MAR	Master A64 Base Address Register	-
18000048h	LAG	Local Address Generator	-
1800004ch	DMAVTC	DMA VMEbus Transfer Count	-

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

DS1643 Nonvolatile Timekeeping RAM

Table 8: DS1643 Nonvolatile Timekeeping RAM Registers

ADDRESS	FUNCTION	VALUES	INIT
0F000000h- 0F001FF7h	Nonvolatile RAM	User Definable	-
0F001FF8h	Control Register	-	00
0F001FF9h	Seconds	00-59	msb = 0
0F001FFAh	Minutes	00-59	-
0F001FFBh	Hours	00-23	-
0F001FFCh	Day	01-07	-
0F001FFDh	Date	01-31	-
0F001FFEh	Month	01-12	-
0F001FFFh	Year	00-99	-

82C54 Interval Timer

Table 9: 82C54 Interval Timer Registers

ADDRESS	FUNCTION
70000000h	Interval Timer 0 Counter
70000001h	Interval Timer 1 Counter
70000002h	Interval Timer 2 Counter
70000003h	Control Word Register

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

EMULEX FAS216 SCSI Controller

Table 10: EMULEX FAS216 SCSI Controller Register Map

ADDRESS	READ FUNCTION	WRITE FUNCTION	INIT
0A000000h	Transfer Counter Low	Transfer Count Low	-
0A000001h	Transfer Counter Mid	Transfer Count Mid	-
0A000002h	FIFO	FIFO	-
0A000003h	Command	Command	-
0A000004h	Status	Select/Reselect Bus ID	-
0A000005h	Interrupt	Select/Reselect Time-out	-
0A000006h	Sequence Step	Synchronous Xfer Period	-
0A000007h	FIFO Flags	Synchronous Offset	-
0A000008h	Configuration 1	Configuration 1	07
0A000009h	Reserved	Clock Conversion Factor	05
0A00000Ah	Reserved	Test mode	-
0A00000Bh	Configuration 2	Configuration 2	20
0A00000Ch	Configuration 3	Configuration 3	01
0A00000Dh	Reserved	Reserved	-
0A00000Eh	Transfer Counter High	Transfer Count High	-
0A00000Fh	Reserved	Reserve FIFO Byte	-

68681 DUART

Table 11: Motorola 68681 DUART Register Map

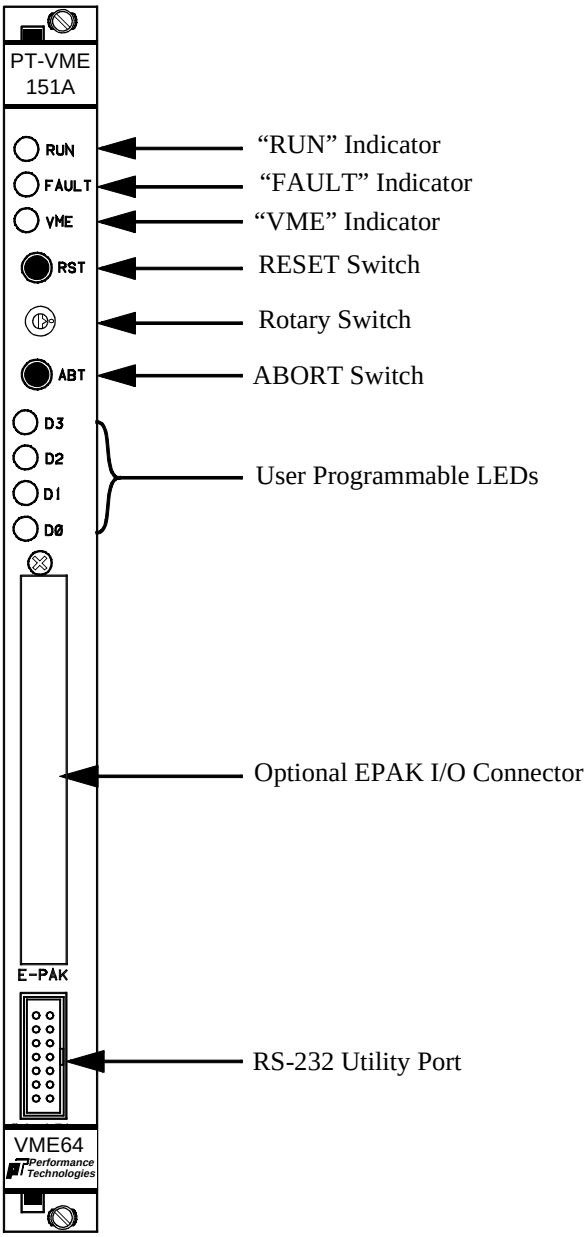
ADDRESS	READ FUNCTION	WRITE FUNCTION	INIT
08000000h	Mode Register A	Mode Register A	13-07
08000001h	Status Register	Clock Select Register A	BB
08000002h	DO NOT READ	Command Register A	-
08000003h	Receiver Buffer A	Transmitter Buffer A	-
08000004h	Input Port Change Reg	Auxiliary Control Register	B0
08000005h	Interrupt Status Reg	Interrupt Mask Register	33
08000006h	Counter Mode: MSB	Counter/Timer Upper	-
08000007h	Counter Mode: LSB	Counter/Timer Lower	-
08000008h	Mode Register B	Mode Register B	13-07
08000009h	Status Register B	Clock Select Register B	BB
0800000Ah	DO NOT READ	Command Register B	-
0800000Bh	Receiver Buffer B	Transmitter Buffer B	-
0800000Ch	Interrupt Vector Reg	Interrupt Vector Reg	40
0800000Dh	Input Port (unlatched)	Output Port Config Reg	00
0800000Eh	Start-Counter Command	Output Port - Bit Set	FF
0800000Fh	Stop-Counter Command	Output Port - Bit Reset	00

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Controls and Indicators

The figure below identifies the controls and indicators that reside on the PT-VME151A Front Panel.

Figure 13: PT-VME151A Front Panel Controls and Indicators



Rotary Switch

A hexadecimal rotary switch is provided for utility input purposes. The switch state is accessible to the firmware through the System Status Register.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

“RUN” Indicator

The “RUN” indicator is a green LED which is illuminated whenever the module microprocessor is not reset and not halted.

“FAULT” Indicator

The “FAULT” indicator is a red LED, under program control, which provides a visual indication to the user that the software has detected an error condition and the VMEbus signal SYSFAIL* is asserted.

“VME” Indicator

This green indicator is illuminated during the period of a VMEbus master access attempt. The LED illumination intensity is a relative indication of the PT-VME151A’s VMEbus access frequency. A solid, bright light is indicative of high bus contention where the PT-VME151A is not receiving a Bus Grant.

RESET Switch

The reset switch is a red push button on the front panel which is tied to the EXTRST input pin of the ACC which in turn generates a board reset [-LRST].

ABORT Switch

The abort switch is a black push button on the front panel which is tied to the -L7I0(NMI) input pin of the ACC which in turn will generate a level 7 interrupt to the 68030.

User Programmable LEDs

Four user programmable LEDs are available on the front panel, labeled D0, D1, D2, and D3. They are programmed by software through bits in the System Control Register.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Section

5

CONNECTOR PINOUTS

Utility Serial Port Pin Assignments

Connections to the Debug/Utility port can be made using the supplied cable. A Data Terminal Equipment RS-232C interface is provided. A transition cable is supplied which converts between the 14-pin header (P3) and a female shell (male pin) 25-pin D-Shell connector.

Table 12: Utility Serial Port Pin Assignments

DB 25 Pin	Dir	Circuit	P3 Pin	Description
1	-	AA	1	Protective Ground (Shield)
2	Out	BA	3	Port A Transmitted Data
3	In	BB	5	Port A Received Data
4	Out	CA	7	Port A Request To Send
5	In	CB	9	Port A Clear To Send
6	In	CC	11	Port A Data Set Ready
7	-	AB	13	Signal Ground (Common Return)
8-13				Unused
14	Out	SBA	2	Port B Transmitted Data (Secondary)
15			4	Unused
16	In	SBB	6	Port B Received Data (Secondary)
17			8	Unused
18			10	Unused
19			12	Unused
20	Out	CD	14	Port A Data Terminal Ready
21-25				Unused

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

VMEbus Pin Assignments

Table 13: VMEbus "P1" Connections

P1A	Signal	P1B	Signal	P1C	Signal
1	D00	1	BBSY*	1	D08
2	D01	2	BCLR*	2	D09
3	D02	3	ACFAIL*	3	D10
4	D03	4	BG0IN*	4	D11
5	D04	5	BG0OUT*	5	D12
6	D05	6	BG1IN*	6	D13
7	D06	7	BG1OUT*	7	D14
8	D07	8	BG2IN*	8	D15
9	GND	9	BG2OUT*	9	GND
10	SYSCLK	10	BG3IN*	10	SYSFAIL*
11	GND	11	BG3OUT*	11	BERR
12	DS1*	12	BR0*	12	SYSRESET*
13	DS0*	13	BR1*	13	LWORD*
14	WRITE*	14	BR2*	14	AM5
15	GND	15	BR3*	15	A23
16	DTACK*	16	AM0	16	A22
17	GND	17	AM1	17	A21
18	AS*	18	AM2	18	A20
19	GND	19	AM3	19	A19
20	IACK*	20	GND	20	A18
21	IACKIN*	21		21	A17
22	IACKOUT*	22		22	A16
23	AM4	23	GND	23	A15
24	A07	24	IRQ7*	24	A14
25	A06	25	IRQ6*	25	A13
26	A05	26	IRQ5*	26	A12
27	A04	27	IRQ4*	27	A11
28	A03	28	IRQ3*	28	A10
29	A02	29	IRQ2*	29	A09
30	A01	30	IRQ1*	30	A08
31	-12V	31		31	+12V
32	+5V	32	+5V	32	+5V

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 14: VMEbus" P2" Connections

P2A	Signal	P2B	Signal	P2C	Signal
1	D0	1	+5V	1	GND
2	D1	2	GND	2	GND
3	D2	3	VRMC*	3	GND
4	D3	4	A24	4	GND
5	D4	5	A2	5	GND
6	D5	6	A26	6	GND
7	D6	7	A27	7	GND
8	D7	8	A28	8	GND
9	DP	9	A29	9	GND
10	GND	10	A30	10	GND
11	GND	11	A31	11	GND
12	GND	12	GND	12	GND
13	TPWR	13	+5V	13	
14	GND	14	D16	14	GND
15	GND	15	D17	15	GND
16	ATN	16	D18	16	GND
17	GND	17	D19	17	GND
18	BSY	18	D20	18	GND
19	ACK	19	D21	19	GND
20	RST	20	D22	20	GND
21	MSG	21	D23	21	GND
22	SEL	22	GND	22	GND
23	C/D	23	D24	23	GND
24	REQ	24	D25	24	GND
25	I/O	25	D26	25	GND
26		26	D27	26	GND
27		27	D28	27	GND
28		28	D29	28	GND
29		29	D30	29	GND
30		30	D31	30	GND
31		31	GND	31	GND
32		32	+5V	32	GND

VMEbus P2 connector rows A and C are User Definable connector pins. The PT-VME151A provides the connections identified above for the SCSIbus interconnect.

NOTE: VRMC* is a jumper (K7) selectable option. The IEEE 1014 Rev C VMEbus Specification defines this signal as "RESERVED".

Pin numbers without mnemonics are not used by the PT-VME151A.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

EPAK Connectors

The PT-VME151A EPAK module interface is comprised of connectors J1, J2, and J3, and the six EPAK standoffs.

Table 15: EPAK Connections

J1	Signal	J2	Signal	J3	Signal
1	+12	1	+MPSZ0	1	+MPA24
2	-12	2	+MPSZ1	2	+MPA25
3	GND	3	+MPFC0	3	+MPA26
4	+MPA00	4	+MPFC1	4	+MPA27
5	+MPA01	5	+MPFC2	5	+MPA28
6	+MPA02	6	GND	6	+MPA29
7	+MPA03	7	+MPA08	7	+MPA30
8	+MPA04	8	+MPA09	8	+MPA31
9	+MPA05	9	+MPA10	9	GND
10	+MPA06	10	+MPA11	10	+MPD00
11	+MPA07	11	+MPA12	11	+MPD01
12	GND	12	+MPA13	12	+MPD02
13	+MPD24	13	+MPA14	13	+MPD03
14	+MPD25	14	+MPA15	14	+MPD04
15	+MPD26	15	GND	15	+MPD05
16	+MPD27	16	+MPA16	16	+MPD06
17	+MPD28	17	+MPA17	17	+MPD07
18	+MPD29	18	+MPA18	18	GND
19	+MPD30	19	+MPA19	19	+MPD08
20	+MPD31	20	+MPA20	20	+MPD09
21	GND	21	+MPA21	21	+MPD10
22	-EPSEL	22	+MPA22	22	+MPD11
23	-MPRMC	23	+MPA23	23	+MPD12
24	-MPUAS	24	GND	24	+MPD13
25	-MPUDS	25	+MPD16	25	+MPD14
26	-MPWRT	26	+MPD17	26	+MPD15
27	-EPSA0	27	+MPD18	27	GND
28	-EPIRQ	28	+MPD19	28	-MPSA0
29	-EPVIR	29	+MPD20	29	-MPSA1
30	-EPVIA	30	+MPD21	30	-MPBER
31	+EPKIO	31	+MPD22	31	-MPHLT
32	GND	32	+MPD23	32	-EPKPE
33	+MPCLK	33	GND	33	GND
34	-MPCLK	34	-EPSA1	34	-EPKBR
35	-MPRST	35	-EPERR	35	-MPBGA
36	-BDRST	36	+REFCK	36	-EPKBG

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

The EPAK mounting standoffs are used to carry power and ground to the EPAK module.

Table 16: EPAK mounting standoffs

Mounting pin	Signal
1	GND
2	+5V
3	GND
4	+5V
5	GND
6	GND

DRAM Module

The DRAM Module standoff carries ground to the module.]

Table 17: DRAM Module Connections

Pin	Signal	Pin	Signal
1	GND	41	GND
2	D0	42	D8
3	D1	43	D9
4	D2	44	D10
5	D3	45	D11
6	D4	46	D12
7	D5	47	D13
8	D6	48	D14
9	D7	49	D15
10	GND	50	GND
11	WE0	51	WE1
12	GND	52	GND
13	RAS0	53	RAS1
14	A0	54	A6
15	A1	55	A7
16	A2	56	A8
17	MSIZ2	57	GND
18	MSIZ0	58	CAS1
19	GND	59	GND
20	MSIZ1	60	PERR
21	GND	61	SPARE
22	CAS0	62	PARPR

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 17: DRAM Module Connections

Pin	Signal	Pin	Signal
23	GND	63	OE
24	A3	64	A9
25	A4	65	A10
26	A5	66	A11
27	GND	67	GND
28	RAS2	68	RAS3
29	PTST	69	RASP
30	WE2	70	WE3
31	GND	71	GND
32	D16	72	D24
33	D17	73	D25
34	D18	74	D26
35	D19	75	D27
36	D20	76	D28
37	D21	77	D29
38	D22	78	D30
39	D23	79	D31
40	GND	80	GND

The DRAM mounting standoffs are used to carry power and ground to the DRAM module.

Table 18: EPAK mounting standoffs

Mounting pin	Signal
1	+5V
2	+5V
3	GND

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Section

6

MECHANICAL AND ENVIRONMENTAL

Power Requirements

The following values are without an EPAK installed.

Table 19: Power Requirements

Voltage	Typical	Maximum
+5V (±5%)	3.9 Amps	4.4 Amps
+12V (±5%)	25 mA	42 mA
-12V (±5%)	25 mA	42 mA

Ambient Temperature

Table 20: Ambient Temperature

Use	Minimum	Maximum
Operating	0° C	+55° C
Storage	-55° C	+85° C

Humidity

Non condensing

Table 21: Humidity Constraints

Minimum	Maximum
0%	90%

Vibration

Designed to meet 5-100 Hz with 2g Acceleration.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Mechanical Shock

Designed to meet 20g for 6 ms (half sine).

Physical Dimensions

Base board only

Table 22: Physical Dimensions

Dimension	Millimeters	Inches
Width	234	9.2
Depth	160	6.3
Front Panel	20.3	.80
Component Height	14	.55

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Section

7

APPENDICES

APPENDIX A: Product Warranty

Performance Computer, A Performance Technologies Company (hereinafter “PCC”) warrants that its products sold hereunder will at the time of shipment be free from defects in material and workmanship and will conform to PCC’s applicable specifications or, if appropriate, to Buyer’s specifications accepted by PCC in writing. If products sold hereunder are not as warranted, PCC shall, at its option, refund the purchase price, repair, or replace the product provided proof of purchase and written notice of nonconformance are received by PCC within 12 months of shipment, or in the case of software and integrated circuits within ninety (90) days of shipment and provided said nonconforming products are returned F.O.B. to PCC’s facility no later than thirty days after the warranty period expires. Products returned under warranty claims must be accompanied by an approved Return Material Authorization number issued by PCC and a statement of the reason for the return. Please contact PCC, or its agent, with the product serial number to obtain an RMA number. If PCC determines that the products are not defective, Buyer shall pay PCC all costs of handling and transportation. This warranty shall not apply to any products PCC determines to have been subject to testing for other than specified electrical characteristics or to operating and/or environmental conditions in excess of the maximum values established in applicable specifications, or have been subject to mishandling, misuse, static discharge, neglect, improper testing, repair, alteration, parts removal, damage, assembly or processing that alters the physical or electrical properties. This warranty excludes all cost of shipping, customs clearance and related charges outside the United States. Products containing batteries are warranted as above excluding batteries.

THIS WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES WHETHER EXPRESS, IMPLIED OR STATUTORY INCLUDING IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS. IN NO EVENT SHALL PCC BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES DUE TO BREACH OF THIS WARRANTY OR ANY OTHER OBLIGATION UNDER THIS ORDER OR CONTRACT.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

APPENDIX B: Product Return Procedure

If you find that your Performance Computer ("PCC") product must be returned for repair, note the following:

To return equipment, please obtain a Return Material Authorization (RMA) number. PCC cannot accept returns without an RMA number.

To obtain an RMA number, contact PCC's Customer Service Group at (716) 256-0200 (FAX: (716) 256-0791). Outside North America, Customers should contact their PCC agent. PCC requests the serial number of the unit and the reason for the return at the time the RMA is issued.

Return products should be shipped, prepaid, to:

Performance Technologies, Incorporated
Attn: Customer Service Group
315 Science Parkway
Rochester, N.Y. 14620, U.S.A.

(Customers outside of North America, contact your local PCC agent for return shipment instructions.) The RMA number should be marked on the outside of the shipping box to expedite correct handling at the PCC factory.

Repairs will be performed only on complete units. Return of incomplete equipment may delay repairs.

Please note that removal of original parts or product modification by a customer can void the warranty. (This does not apply to jumpers or socketed user programmable parts.)

"Out of warranty repairs" cannot proceed without a customer Purchase Order.

PCC will supply repair information on all returns.

PCC warrants all repairs for 90 days.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

APPENDIX C: Installation Notes



CAUTION: ELECTRONIC COMPONENTS ON PRINTED CIRCUIT BOARDS ARE EXTREMELY SENSITIVE TO STATIC ELECTRICITY. ORDINARY AMOUNTS OF STATIC ELECTRICITY GENERATED BY YOUR CLOTHING OR WORK ENVIRONMENT CAN DAMAGE THE ELECTRONIC EQUIPMENT. IT IS RECOMMENDED THAT WHEN INSTALLING THE PT-VME151A IN A SYSTEM OR THE COMPONENTS ON THE BOARD ITSELF THAT ANTI-STATIC GROUNDING STRAPS AND ANTI-STATIC MATS ARE USED TO HELP PREVENT DAMAGE DUE TO ELECTROSTATIC DISCHARGE.



CAUTION: WHEN INSTALLING CHIPS INTO PROM SOCKETS, BE CERTAIN OF THEIR ORIENTATIONS. THE BOTTOM OF THE CHIP WILL BE ALIGNED WITH THE BOTTOM OF THE SOCKET. THE TOP OF THE SOCKET IS THE END CLOSEST TO THE VME CONNECTORS. PIN ONE OF THE CHIP SHOULD BE POINTING TOWARD THE VME CONNECTORS.



CAUTION: WHEN INSTALLING A 28 PIN DEVICE BE SURE THAT PIN 14 OF THE DEVICE ENTERS PIN 16 OF THE SOCKET (BOTTOM JUSTIFIED).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

APPENDIX D: EEPROM Usage

PTI employs the Serial EEPROM to hold power-up and reset configuration information. The following table shows the usage and initial values that will be found in the EEPROM as a result of running factory testing of the PT-VME151A.

The table is divided into two groups, locations 00-43h are used by PTbug (however the information that they contain will probably be necessary for any application) and locations 44h-63h are used by OS-9™ (when installed).

PTbug

The first four bytes of the EEPROM contains PTbug Magic Number. If the value is correct, PTbug assumes that the rest of the locations that it uses are meaningful.

Byte locations 06h through 1Dh are used as initial values for the respective device registers.

The DARF64 requires that a reference to the location monitor be performed before it will respond as a slave to shared memory accesses. Byte location 1Eh contains a flag that determines whether the PT-VME151A will make this reference to itself (requiring that it accesses the VMEbus immediately after reset) or allows an appropriate driver make the initial reference.

Byte locations 20h through 2Fh are reserved by PTI for future use.

After reset, PTbug can perform Power On Confidence tests then launch a user application. This boot mechanism is defined in the PTbug User's Manual (811A0127xx) and uses locations 30h to 43h.

Two bytes (7Ch and 7Dh) are used by PTbug to store the ROM checksum. The Power On Confidence test uses this information to validate ROM integrity.

The last two locations (7Eh-7Fh) in the EEPROM are used by the Power On Confidence test to exercise the EEPROM read/write operation.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

OS-9

PTI offers the OS-9 Real-Time Operating System from Microware Systems Corporation for the PT-VME151A. Locations 44h through 63h are used by OS-9 if installed. For more information contact PTI or Microware. Address: Microware Systems Corporation; 1900 N. W. 114th Street; Des Moines, Iowa 50325. Phone number: (515) 224-1929.

Table 23: EEPROM Default Values

Address	Length	Default	Description
00	4 bytes	$01281955	PTbug Magic Number
04	2 bytes	$FFFF	Board Serial Number
06	4 bytes	$0060014C	DARF64 - VMEbus Base Address Register (VMEBAR)
0A	4 bytes	$81000001	DARF64 - Mode Control Register (MODE)
0E	4 bytes	$00000001	DARF64 - Access Protect Boundary Register (APBR)
12	4 bytes	$00000040	DARF64 - VMEbus Interrupter Vector Register (IVECT)
16	1 byte	$1C	ACC - General Control Register (GENCTL)
17	1 byte	$00	ACC - Level 7 Interrupt Status Register (CTL2)
18	1 byte	$13	ACC - Local Interrupts 1 & 0 Control Register (IC10)
19	1 byte	$45	ACC - Local Interrupts 3 & 2 Control Register (IC32)
1A	1 byte	$62	ACC - Local Interrupts 5 & 4 Control Register (IC54)
1B	1 byte	$00	ACC - Local Interrupt Enable Register (LIE)
1C	1 byte	$00	ACC - VMEbus Arbiter Register (VARB)
1D	1 byte	$03	ACC - VMEbus Requester Register (VREQ)
1E	1 byte	$00	Flag To Access Location Monitor on Reset (1 - access, 2 - no access)
1F	1 byte	$07	SCSI I.D.
20	16 bytes		PTI Reserved
30	2 bytes	$B0BB	Boot Validation Word
32	2 bytes	$0007	Boot Flags (Bits 0-2 are always 1. Bits 3-5 are dependent on memory size[a]. See footnote below)
34	4 bytes	$00000000	Source Address
38	4 bytes	$00000000	Destination Address
3C	4 bytes	$00000000	Transfer Byte Count
40	4 bytes	$00000000	Execute Address
44	2 bytes	$FACE	OS-9 Magic Word 1
46	2 bytes	$0000	Save Count
48	1 byte	$01	Number Of Floppy Drives
49	1 byte	$01	Number Of Hard Drives
4A	1 byte	$01	Boot Device

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 23: EEPROM Default Values

Address	Length	Default	Description
4B	1 byte	$01	Floppy Format
4C	8 bytes	“shell”	Shell String
54	2 bytes	$0400	Number Of 256 Byte RAM Disk Sectors
56	2 bytes	$0000	SCSI Master/Slave Boot (Slave)
58	6 bytes	XX XX XX XX XX XX	Ethernet Link-Level (Physical) Address
5E	4 bytes	147.139.6.9	Internet Address
62	2 bytes	$DEAD	OS-9 Magic Number 2
64	24 bytes		Not Used
7C	2 bytes	$XXXX	ROM Checksum (Used By PTbug)
7E	2 bytes	$XXXX	Used By PTbug In Checking EEPROM

a. Memory size decoding of bits 5 through 3:

Value	Size in MegaBytes
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	Reserved

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

APPENDIX E: The differences between the PT-VME151A and the VME151

It may be desirable to run software written for the PT-VME151 on a PT-VME151A. Most of the new features on the 151A are disabled after reset, making them transparent to existing software. This appendix is an overview of the programming issues that must be considered when porting code from the PT-VME151/151E to the PT-VME151A/151AE.

Renamed Registers

The PT-VME151 System Control Register and the System Status Register have been renamed on the PT-VME151A to System Control Register 1 and System Status Register 1, respectively. All fields in these registers remain consistent with those defined by the PT-VME151.

New Devices

The “UNASSIGNED” addresses of the PT-VME151 would return Bus Errors when accessed. Several of these address have been assigned to the new devices on the PT-VME151A. Any PT-VME151 code that purposely accessed these locations to produce a Bus Error, may produce unwanted results on the PT-VME151A.

Software may determine whether it is running on a PT-VME151 or a PT-VME151A by reading one of the new device registers. If a no Bus Error occurs then the code is running on a PT-VME151A. A summary of the new register assignment follows:

Table 24: 151 to 151A Register Map DIfferences

ADDRESS RANGE	PT-VME151	PT-VME151A
0D000000h-0DFFFFFFh	System Control Register	System Control Register 1
50000000h-5FFFFFFFh	UNASSIGNED	System Control Register 2
0C000000h-0CFFFFFFh	System Status Register	System Status Register 1
60000000h-67FFFFFFh	UNASSIGNED	System Status Register 2
68000000h-6FFFFFFFh	UNASSIGNED	System Status Register 3
70000000h-7FFFFFFFh	UNASSIGNED	82C54 Interval Timer

DRAM Sizing

The PT-VME151 could be configured with 1, 2, 4, or 8 MBytes of DRAM (Main Memory). The PT-VME151A can be configured with 4, 8, 16, 32, or 64 Mbytes of DRAM. The installed DRAM repeats throughout the address range 20000000h - 2FFFFFFFh. The pattern of repeatability differs from the 151 to the 151A. Software that takes advantage of the repeat pattern to size memory will have to be modified. See “DRAM” on page 28 for a discussion of 151A DRAM repeatability.

As an alternative to the memory sizing algorithms required by the 151, the 151A System Status Register 2 provides DRAM size information. See “System Status Register 3” on page 66 for list of the encoded values.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SRAM Access

The PT-VME151A does not support the SRAM option that was available on the 151. As a result the SRSZ field in System Status Register 1 will always return 0, indicating that **NO** SRAM is installed.

On the 151 accesses to address space allocated to the SRAM would never generate a Bus Error. Accesses to the same space on the PT-VME151A will terminate with a local Bus Error. PT-VME151 software that is intended to run on the PT-VME151A should be checked for references to this space.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

APPENDIX F: PT-VME151A Differences From VME131/141

This appendix is an overview of the programming issues that must be considered when porting code from the PT-VME131/131E or PT-VME141/141E to the PT-VME151A/151AE.

DARF64 uses 68040 mode

The PT-VME151A is configured in hardware to automatically come up in 68040 mode. This means that a read from the DARF64 Mode Control Register will show a 1 in bit 24 (040 mode enabled) instead of 0 (as in VME141).

One effect of 68040 mode is that longword writes by the 68040 to D16 VME space will fail.

SCSI Controller differences

Alternate DMA mode in Emulex SCSI chip is no longer used. This means that the Alternate DMA mode bit of FAS216 Configuration Register 3 is written with 0 rather than 1 (as in VME131/141).

Effects of 68040 vs. 68030

Cacheability and Serialization

One difference between the 68040 and 68030 is the way cache line refills are handled. In 68030 cycles, devices may acknowledge themselves as noncacheable so that the 68030 will not attempt to cache the data obtained during the read cycle. The 68040, however, will still fetch four longwords to fill its cache line even if the device acknowledges itself as noncacheable (using the TCI signal). In that case, the processor fetches the four longwords and then discards them internally, retaining the original data sought.

What can happen, then, is that if an instruction reads a byte, the processor actually does four longword read cycles. These extra read cycles may potentially cause loss of data in I/O device registers which are cleared after reading. They may also produce an error or unpredictable results when illegal addresses are read.

When the caches are enabled, the entire address space is considered cacheable by default. It is necessary to specify critical address spaces as noncacheable so that the processor does not attempt to do cache refills, incurring the extra longword reads. The noncacheability is specified using the 68040's Transparent Translation Registers, discussed later.

To increase processing efficiency, the 68040 may not perform read and write bus cycles in the same order found in the instruction stream. Write cycles may be queued internally while read cycles occurring downstream in the code are executed. This can increase execution efficiency if the hit rate in the data cache is high. Rather than forcing read cycles to wait for the completion of pending write cycles (which usually require wait states), read data may often be found in the data cache. Thus, many read cycles can be performed internal to the chip while the longer external write cycles are executing. Address spaces where writes and reads may be out of sequence with respect to each other are said to be nonserialized. Note that reads are performed in the order found in the code and writes are also performed in order. It is the order of writes with respect to reads that may be out of sequence. Also, the 68040 will not do a read from an address that is still in the write queue.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Problems may arise with I/O devices where a read from a data register may depend on a write to a different register. In these cases, because the addresses are different, the 68040 has no way of determining the dependency of the read and write instructions so that the register read may occur before the write.

One way to remedy this situation is to place a NOP instruction before an I/O device register read. The NOP has the effect of freezing instruction execution until all pending bus cycles complete. The NOP, in effect, forces serialization.

A more general way to force serialization of I/O accesses is to use the 68040's Transparent Translation Registers. These registers operate independently of the 68040's MMU and are also available on the 68EC040 and the 68LC040. There are two registers for data accesses (DTTR0 and DTTR1) and two for instruction accesses (ITTR0 and ITTR1). The registers are read and written using the MOVEC instruction in Supervisor mode.



CAUTION: The Transparent Translation Registers allow instruction and data address spaces to have their serialization and cacheability controlled using address mapping. In the case of the PT-VME151A, 8-bit devices and the EPAK need to be serialized and specified as noncacheable for data accesses.

To accomplish this the following values must be written to the DTTRs (using the MOVEC instruction) at initialization.

DTTR0 - 000FE040h

maps addresses 0xxxxxxxh as serialized, noncacheable.

These addresses include: EPROM socket, EPROM/SRAM socket, 68681 DUART, Control/Status Registers, SCSI MAR, Real Time Clock, and FAS216 SCSI chip.

DTTR1 - $102FE040

maps addresses 1xxxxxxxh and 3xxxxxxxh as serialized, noncacheable.

These addresses include: DARF internal registers, ACC and EPAK.

Since instruction space implicitly uses reads only, serialization is not an issue and the Instruction Translation Registers are not enabled. The user is free to use the Instruction Translation Registers as he sees fit.

If the MMU of the 68040 is used, each page descriptor may also control serialization and cacheability.

68040 Cache Control Registers

NOTE: The user should note that the 68040 cache control register format is different from the format of the 68030.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

68040 Cache Clearing

NOTE: The user should note that the 68040 caches are disabled after a reset but are not cleared or invalidated. The user needs to explicitly clear the instruction and data caches using the CINV instruction as part of initialization.

68040 Exception Processing

NOTE: The user should note that 68040 exception processing differs from that of the 68030. In particular, the format and lengths of some of the exception stack frames are different. The 68040 User's Manual should be consulted for further information.

PT-VME151A Control Register Differences

Since the cacheability of the 68040 address space is controlled using the Transparent Translation Registers, two bits in the System Control Register ECE and VCE, now have different meanings. Bit 6 (ECE) is defined as EPAK Caching Enable and Bit 7 (VCE) is defined as VMEbus Caching Enable.

As described previously, cacheability of an address may be determined in hardware (using the TCI signal), but the processor will still attempt to fetch four longwords to fill the cache line, but then discard them. Cacheability may also be controlled using the 68040 Transparent Translation Registers to eliminate the extra longword fetches and to control serialization.

EPAK address space is defined as noncacheable in the Transparent Translation Registers as defined previously. Thus, the Enable EPAK Caching bit of the Control Register does not entirely control EPAK cacheability (as it did in the VME131/141).

If an EPAK were to be constructed which could make use of data caching (such as an all-memory EPAK), then the Transparent Translation would be redefined to allow EPAK caching. In this case, the caching of the EPAK would then also depend on the state of the Enable EPAK Caching bit of the Control Register.

In summary, in normal PT-VME151A operation with existing EPAKs, EPAK address space is defined internal to the 68040 as noncachable. This makes the Enable EPAK Caching bit of the Control Register irrelevant. Below are the possible combinations of events:

Table 25: EPAK Caching

68040 DTTR EPAK Cache Enable	151A Control Register EPAK Cache Enable	EPAK Caching?
Disabled	Don't Care	No (Normal mode)
Enabled	True	Yes
Enabled	False	No, but 4 lwords fetched

With respect to VME memory space, VME space is not explicitly affected by the mapping defined above in the Transparent Translation Registers. Therefore, the VME Caching Enable bit in the System Control Register still controls the cacheability of VME address space. However, if the 68040 data caches are enabled, but the VME Caching Enable bit in the System Control Register is false, VME address space will not be cached, but the processor will still fetch four longwords from the VMEbus, afterwards

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

discarding the data it doesn't need. This could have adverse effects on VMEbus bandwidth since the PT-VME151A could be doing four times as many reads as it needs. If this situation occurs, the only solutions are to disable all data caching (using the 68040 Cache Control Register) or to use the MMU of the 68040 to make VME space noncacheable.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

APPENDIX G: AVICS Overview

The Advanced VMEbus Interface Chip Set (AVICS) consists of two distinct integrated circuits: the Advanced System Architecture Control Circuit (the ACC) and the Data/Address Register File VME*64* (the DARF64). This pair of ICs integrates all the functions commonly required to interface an intelligent card to the VMEbus, while adding features that provide major architectural improvements including the capability to perform 64-bit transfers (VME64).

The ACC contains functions such as a VMEbus requester, arbiter, interrupter and system controller (VMEbus System Controller functions are automatically provided when internal circuitry detects that the host card is installed in slot 1), and functions related to internal operation such as an interrupt handler, tick timer and watchdog circuit. The DARF64 provides an address and data path between the VMEbus and the local CPU and memory, and also contains a Location Monitor with an associated message queue.

The traditional VMEbus card design forces the CPU to enter wait states whenever it requires the bus, and ties up the VMEbus when an external master is waiting for access to a card's internal bus. The architectural advance the DARF64 provides is a pair of 15-stage deep FIFOs that decouple the local bus and VMEbus (termed “decoupled” mode). These FIFOs immediately accept writes from one bus, releasing that bus for further use, and finish the write to the destination bus themselves. This provides data transfer rates much higher than the traditional “atomic” mode.

The DARF64 has the capability to perform data transfers as a master or slave on the VMEbus and local bus in a variety of modes. Writes to the VMEbus can take place in either traditional atomic mode or in decoupled mode, while reads are always atomic.

When operated as a master, the DARF64 provides a programmable, 32 page, memory map which determines the addressing mode and data width to generate on the VMEbus. The DARF64 can also create a “slave image” which allows some of the local resources (typically RAM) to be accessible by other VMEbus devices. Base addresses of the DARF64's A24 and A32 VMEbus slave images are programmable, as are the sizes of each image and the access protection range.

A DMA controller is provided to transfer data to/from the VMEbus in a variety of ways, including D32BLT and D64MBLT (VME*64*). To support the high transfer rate of the D64MBLT cycles on the VMEbus, the local bus interface of the DMA machine can use a memory burst protocol similar to that used by the 68030 for cache fill operations.

Another feature of the AVICS is the ability to isolate the DARF64 from the VMEbus by pointing its transceivers inwards (known as BI-mode). While the DARF64 is in this mode, it will cease any master or slave activity on the VMEbus, such as requesting or owning the bus, or asserting interrupts. System controller functions and all functions related to internal card activities are not affected.

Functional Description

BI-mode

While the DARF64 is in BI-mode, its VMEbus transceivers will be pointed inwards, and it will not assert any signals on the VMEbus. Even though its slave images may have been programmed, it will not respond to any accesses to them (except by the local CPU), and the VMEbus would timeout if such an access occurred. If the local CPU attempts to access the VMEbus, the DARF64 will ignore the cycle and the local bus will timeout (if enabled in the ACC). If the DARF64 enters BI-mode with cycles remaining in its two FIFOs, the receive FIFO will complete its writes to local memory, while the cycles in the transmit FIFO will be lost.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

The internal registers of the DARF64 and ACC are fully accessible by the local CPU while in BI-mode. The slave image of local memory, at the programmed base address and size, is also accessible to the CPU, since such an access does not use the VMEbus or FIFOs unless the DARF64 is in loop-back mode (described in the “Test and Diagnostic Modes” section of the AVICS Technical Manual).

Location Monitor

The location monitor is a specialized function of the DARF64 to assist in inter-processor communication. It is a 32-bit wide, 31-entry deep message FIFO loaded from the data bus when the location monitor is written to, so that either 16- or 32-bit messages or memory pointers can be sent between processes. This FIFO is written to using the slave image VMEbus address and is read by the local CPU. Writing to this location is the method defined for exiting from BI-mode, enabling the card to perform master and slave VMEbus accesses.

The location monitor's address exists at the top longword and the lower (even) word of the top longword in each of the A24 and A32 slave images presented on the VMEbus. It replaces the longword of memory (that is accessible through the slave images) which would otherwise exist at that address, so writes to the location monitor do not enter into memory (however, that memory location is still accessible by the local bus). In order for the local CPU to access its own location monitor, it must also use the A24 or A32 slave image VMEbus address. When the CPU writes to this specialized location (or accesses any other location in the slave image), the transfer does not involve use of either the transmit FIFO or the VMEbus.

If the location monitor FIFO is full when a write to it is made, the cycle will not be responded to. If the local CPU reads out an item while a write is waiting on the other end, then a position would become available and the write accepted. Otherwise, the bus timeout would expire and end the cycle with a Bus Error.

Messages in the location monitor FIFO are read in the form of longwords from the Location Monitor FIFO Read Port (LMFIFO). If a write happened to be 16 bits (the lower word of the top longword of the slave image), then the upper 16 bits of that FIFO entry are recorded as ones. Once the FIFO becomes empty, further reads will return undefined data.

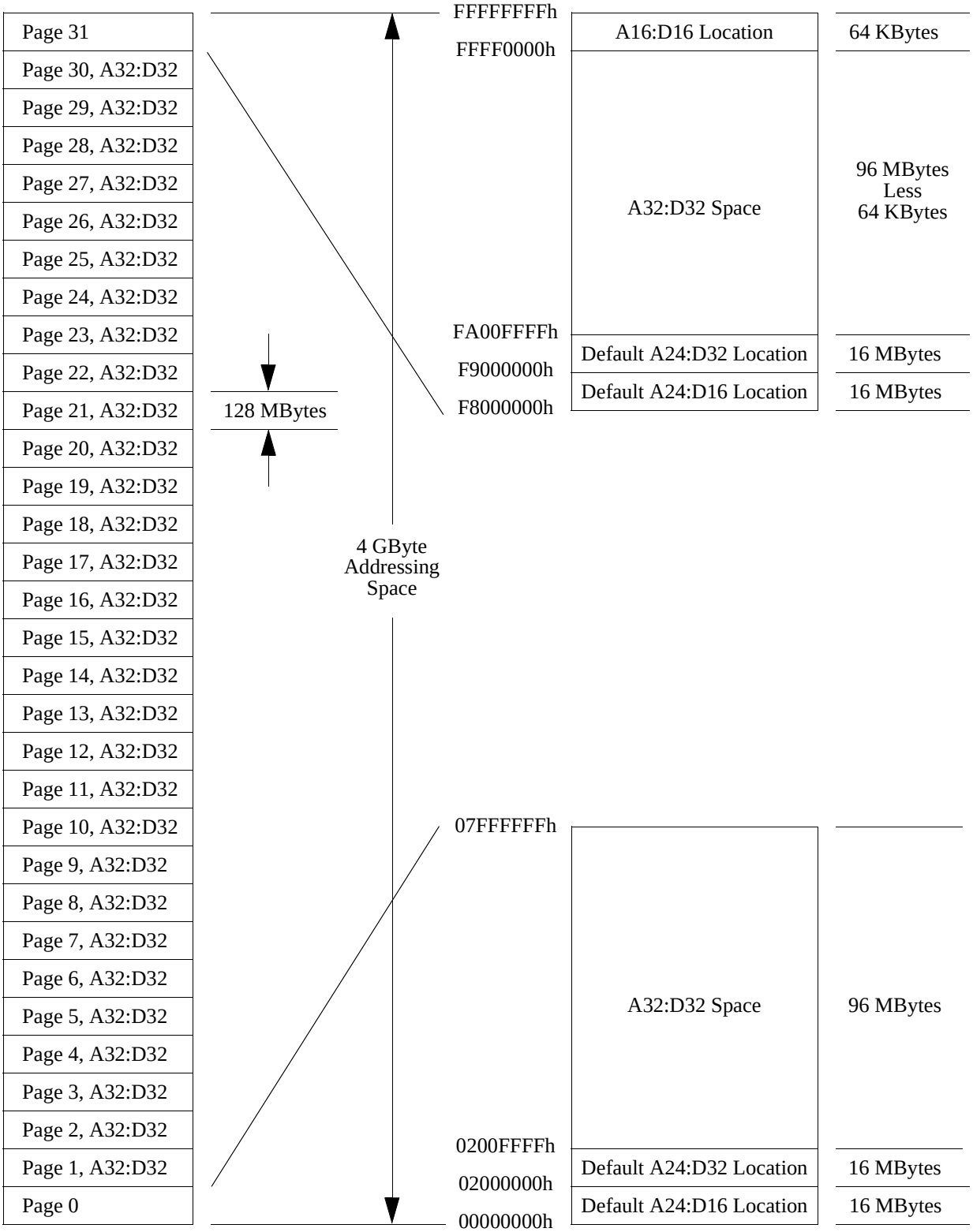
A status bit (LMHD) is available in the Control and Status Register (DCSR) which is high when the FIFO has data available for the local CPU to read. While there are entries in the FIFO, the DARF64 generates an interrupt request to the local CPU. This allows software to either poll the status bit or the interrupt request signal, or use an interrupt service routine to support the location monitor.

VMEbus Master Memory Map

The programmable memory map of the DARF64 determines the type of cycle to perform on the VMEbus during discrete master transfers (DMA excluded). When the CPU accesses the VMEbus, the address used by the CPU determines the address and data modes the DARF64 will use to perform the cycle. The valid bits (depending on the addressing mode) of this address will always map directly to the VMEbus, while the unused bits are used by the DARF64 to determine the type of cycle. For example, when the CPU attempts to access an A24 device on the VMEbus, the top 8 bits of the 32-bit address sent to the DARF64 are used to signal that an A24 address modifier is needed. The possible addressing modes are A16, A24, or A32, and the data modes are D16 or D32. (Note: additional addressing and data modes, i.e. A64, D64MBLT, etc., are available in DMA mode). All addresses that are not defined as A16 or A24 space cause the DARF64 to use A32:D32 mode when using the VMEbus. The “DARF Memory Map” on page 97 provides a graphical representation of how these different modes are organized in the memory map.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Figure 14: DARF Memory Map



Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

The A16:D16 region is located at the top of the memory map, in the last 64Kb (FFFF0000h-FFFFFFFFh). This space can be disabled using the A16DI bit in the DARF64 Mode Control Register, in which case that address range becomes A32:D32. If the A16 region is enabled and the CPU accesses that region, the DARF64 will perform the cycle on the VMEbus with address bits 31 through 16 set to one, and will use the address modifier codes indicating short addressing.

Two types of A24 master modes are provided, A24:D16 and A24:D32. By default, the addresses for both are located at the bottom of the memory map in page 31, A24:D16 in the first 16 Mbytes (F8000000h-F8FFFFFFh) and A24:D32 in the second 16M bytes (F9000000h-F9FFFFFFh). This pair of A24 spaces can also be relocated to page 0, in address range 00000000h-00FFFFFFh for A24:D16 and 01000000h-01FFFFFFh for A24:D32, by using the A24PO bit in the DARF Mode Control Register. This feature is useful if an A32:D32 device exists at an A24 memory map region. Within these areas, the DARF64 will set VMEbus address bits 31 through 24 to one, and use the appropriate address modifier for standard addressing. A24 space can also be disabled by the A24DI bit, also located in the DARF Mode Control Register, which causes that address range to become A32:D32.

All of these mapping options affect master VMEbus accesses only; they do not affect accesses to the card's dual-port memory from the VMEbus. Accesses by the local CPU to its own slave image (if programmed) are not affected by the VMEbus mapping, nor is the address or data mode affected. The local memory would be selected within the programmed slave image, and the memory control logic would provide the required interface signals.

Master VMEbus Accesses

The DARF64 will request the VMEbus for any of the following purposes:

- the transmit FIFO contains write cycles

- the CPU begins a read cycle to the VMEbus

- the DARF64 is in atomic mode and the CPU begins a write cycle to the VMEbus

- the DARF64 is responding to an interrupt request

The ACC can be programmed to limit the time that the DARF64 uses the VMEbus, ranging from immediately off, 2, 4 or 8 microseconds, or unlimited. When the limit is reached, the DARF64 will complete its current cycle and possibly one more if it has already selected the next one from the transmit FIFO. Other reasons the ACC can request the DARF64 to give up the VMEbus are pending VMEbus ownership requests (Release On Request mode), receipt of a Bus Clear from the system arbiter if Bus Clear recognition is enabled, assertion of L7IMEM to the ACC, or entry into BI-mode.

If the DARF64 is waiting for VMEbus ownership to perform an atomic operation (a write while in atomic mode, any read or read-modify-write, or an interrupt acknowledge) and some other VMEbus device begins an atomic operation to the local memory through the DARF64, then the DARF64 will assert its local bus request signal and request the local CPU to retry its cycle. This will force the CPU off the bus and allow the incoming cycle to be completed first, resolving the contention. The 68020 and 68030 do not retry read-modify-write cycles so the DARF64 will assert the bus error signal (BERR).

Entering BI-mode or receiving a local reset will immediately cause the DARF64 to end any VMEbus cycle in progress. Any cycles remaining in the transmit FIFO will be lost; the CPU cannot unload them from the FIFO, nor will they be done when the DARF64 leaves BI-mode.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

The transmit and receive channels of the DARF64 can each be programmed to operate in atomic or decoupled mode by using the RXATOM and TXATOM bits in the DARF Mode Control Register. Read cycles and interrupt acknowledge cycles are always atomic. In atomic mode accesses, the CPU transfer is not enqueued by the transmit FIFO; the CPU becomes directly linked to the VMEbus once ownership is obtained. The CPU will then execute wait states until an acknowledge or bus error is generated by the VMEbus slave.

CPU write cycles to the VMEbus, with the DARF64 transmit channel in decoupled mode, complete with no wait states. The transmit FIFO will enqueue (both FIFOs are 15 stages deep) the address, data and control signals needed to perform the cycle on the VMEbus. Once the DARF64 has obtained the VMEbus, it will begin the cycles, operating with close to minimum VMEbus specified timing to start and end each cycle. A pending atomic cycle from the local CPU will wait until all write cycles loaded in the FIFO are completed first, so that data integrity is maintained - read cycles cannot skip ahead of uncompleted write cycles.

A VME bus error received by the DARF64 will cause it to stop performing VMEbus cycles, set the VBERR bit in DARF Control and Status Register, and generate an interrupt to the CPU. The DARF64 will not allow further VMEbus master cycles until the VBERR bit is cleared. If the DARF64 is in decoupled mode, the remaining cycles in the transmit FIFO will begin being sent again once VBERR is cleared. The failed cycle is not re-run by the DARF64 since it no longer is in the FIFO. Three registers in the DARF64 (TDATA, TADDR, TCTL) can be used by the CPU to read the output stage of the FIFO to determine the address, data, and control codes involved in the failed write cycle.

If the FIFO is full when the CPU writes to the VMEbus in decoupled mode, the DARF64 will not respond and the CPU will attempt to wait until there is room. If the local bus timeout has been enabled in the ACC, and the CPU waits for longer than 512 microseconds for access to the FIFO, then the CPU will receive a local bus error and set the LBERR bit in the DARF Control and Status Register and the local timeout bit (LTO) in ACC Status Register 0.

Slave VMEbus Accesses

The AVICs allows some, all, or none of the local memory to be accessible as a VMEbus slave through the programming of a “slave image”. This image can vary in its VMEbus base address, size, and access protection range. Separate images can be set up in A24 and A32 address spaces. The local CPU can also access its own slave image at their programmed addresses, within the size configured; however, the DARF64 only acts as an address decoder and does not implement access protection, use the VMEbus or its FIFOs, unless the DARF64 is in loopback mode.

The DARF64 does not provide a slave image on the VMEbus until its base address and image size have been programmed in the DARF VMEbus Base Address Register. The BARDY bit in the DARF Control and Status Register indicates whether the slave image has been programmed since a reset condition occurred. The VINEN bit in the DARF Mode Control Register is used to enable or disable the slave images on the VMEbus.

The A24 and A32 slave images are defined by the VMEbus Base Address Register. The A24 image base can be programmed to any half megabyte boundary or multiple of its programmed size, whichever is larger, within the 16Mb A24 addressing space. The size of this image can be set to 512Kb, 1, 2, or 4Mb. The A32 image base can be programmed to any 128Mb boundary and to any size from 4Kb to 128Mb in binary increments (i.e. 4k, 8k, 16k, etc.) The location monitor appears at the last longword of each programmed slave image.

Although the slave image bases and sizes can be programmed to many values, only certain combinations are valid. The restriction described below ensures that when the local memory is addressed

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

directly by the CPU, or by the CPU via one of its slave images, or by the VMEbus through the DARF64, the same memory locations are selected. Otherwise, it is possible that different areas of local memory could be accessed through those three paths.

The restriction on the slave image base is that it must be a multiple of the amount of memory installed on the CPU card. For example, if the card had 4Mb of memory, the possible A24 slave image bases would be 000000h, 400000h, 800000h, and C00000h, irrespective of the A24 size programmed. It's not expected that this slave base restriction will be a problem for A32 images, since they are already multiples of 128Mb.

Part or all of the slave image can be protected from either writes, or reads and writes. If an access is made to the protected area from the VMEbus slave image, the DARF64 will respond with a bus error. Protection is not implemented for memory accesses by the local CPU to its own slave images. The PROT bit in the DARF Mode Control Register is used to select read/write protection options.

The lower four bits of the DARF Access Protect Boundary Register select how much of the lower part of the slave images (this affects both the A24 and A32 image in the same way) is protected; 0 selects none protected, 1 selects the lower 64Kb, through to F protecting the lower 128Mb.



CAUTION: It is possible to protect the entire slave image, in which case the location monitor would also be protected (from the VMEbus only, not from a local access using the slave image).

To change the receive mode between atomic and decoupled, incoming slave cycles must be disabled first by writing zero to the VINEN bit in the DARF Mode Control Register, then waiting until the DARF64 acknowledges the new mode by setting VINEN to zero. The DARF Mode Control Register, RXATOM bit may then be changed and VINEN set high again. Any slave VMEbus accesses to the DARF64 during this time will be ignored, which may cause a timeout bus error to be received by the master performing the cycle.

Read accesses to the DARF64 are always atomic; if the DARF64 is in decoupled mode, a read access by the slave will wait until any writes queued up in the FIFO are completed. Due to the wait while up to seven writes must be done before the read, it is recommended that the VMEbus data transfer timeout be longer than 4 microseconds.

If the DARF64 receives a local bus error while performing an enqueued write from a slave card, the LBERR bit will become set in DARF Control and Status Register, and an interrupt will be generated. The DARF64 will not stop transferring cycles in or out, and does not save the faulted cycle for diagnostics.

The DARF64 will request the local bus whenever it has cycles waiting in the receive FIFO, an atomic VME-in cycle is pending, or the DMA needs to read/write local memory. The DARF can be requested to give up the local bus if a higher priority device needs it.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

APPENDIX H: AVICS Application Notes

Note: All registers specified are located on the DARF unless otherwise specified.

Local Interrupts

Registers 0h, 8h-Fh (except Ch) of the ACC control the masking, level mapping, vector options and show the status of the six general purpose local interrupts (LIRQ0-LIRQ5) and the five local interrupts dedicated to level 7 (L7I0-L7I3, BI-mode). All of the general interrupts and four of the level 7 (all except L7I0) interrupts can be masked. All interrupts are autovectored, except for LIRQ4 and LIRQ5 which can be programmed to be vectored or autovectored.

Example:

The following interrupt assignments are recommended for a PT-VME151A/151AE board:

Table 26: Recommended Interrupt Assignments

Signal Source*	ACC Pin*	AVEC/VEC	Level
DARF Location Monitor	LIRQ0	AVEC	3
DARF VMEbus Events	LIRQ1	AVEC	1
ACC Tick Timer	LIRQ2	AVEC	5
E-PAK EPIRQ & 33C93A	LIRQ3	AVEC	4
E-PAK EPVIR	LIRQ4	VEC	2
68681 DUART	LIRQ5	VEC	6
Abort Switch	L7I0 (NMI)	AVEC*	7*
SCSIbus Reset	L7I1 (MEM)	AVEC*	7*
VMEbus ACFAIL	L7I2 (ACF)	AVEC*	7*
VMEbus SYSFAIL	L7I3 (SYF)	AVEC*	7*

* Note: Items marked by an asterisk cannot be changed by software.

The following steps enable the interrupts according to the above table (all registers are located on the ACC):

Step 1 Write 1Fh to the ACC Level 7 Interrupt Enable Register to enable the level 7 interrupts.

Step 2 Write 3Fh to ACC Local Interrupt Enable Register to enable the general interrupts.

Step 3 Write 13h to ACC Local Interrupts 1 and 0 Control Register to map LIRQ0 to level 3 and LIRQ1 to level 1.

Step 4 Write 45h to ACC Local Interrupts 3 and 2 Control Register to map LIRQ2 to level 5 and LIRQ3 to level 4.

Step 5 Write 62h to ACC Local Interrupts 5 and 4 Control Register to map LIRQ4 to level 2, vectored and LIRQ5 to level 6, vectored.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Setting Up the Master Bus Memory Map

When the host accesses the VMEbus, the address used by the CPU determines the address and data modes the DARF will use to perform the cycle. All outgoing VMEbus accesses are affected by a programmed memory map. See “DARF Memory Map” on page 97. Memory Map Pages 1-30 are dedicated to A32 space, while pages 0 and 31 can be customized by the following steps:



CAUTION: For PTI products, one must set bit 31 of the address to specify that it is a VME address. The PAGE bit in the Control Register is then used as bit 31 of the VME address before being used by the DARF. From this point forward, all address references will be in respect to what the DARF sees.

Step 1 Make sure the system is not in BI-mode (refer to steps 6-9 of Setting Up A24/A32 Slave Images) if VMEbus accesses are desired.

Step 2 Clear the A16DI bit in the DARF Mode Control Register, if the A16 region is desired; set this bit to disable A16 space, in which case that address range becomes A32. When A16 space is enabled, the local CPU can access the region by using the address range FFFF0000h-FFFFFFFF. The low four bytes constitute the actual VME address of the 16-bit device, while the upper four bytes tells the DARF to generate a D16 address modifier.

Step 3 Clear the DARF Mode Control Register, A24DI bit to enable A24 space; set this bit to disable the A24 space programmed in the memory map which causes that space to become A32.

Step 4 Set the DARF Mode Control Register, A24PO bit to assign page 31 as A24 space; clear it to locate A24 space in page 0. Addresses 00000000h-00FFFFFFh (if in page 0) and F8000000h-F8FFFFFFh (if in page 31) are used to perform an A24:D16 cycle. Addresses 01000000h- 01FFFFFFh (if in page 0) and F9000000h-F9FFFFFFh (if in page 31) are used to perform an A24:D32 cycle.

Example:

To set up a master memory map with A16 disabled and A24 space located at page 0, perform the following steps:

Step 1 Exit BI-mode if VMEbus accesses are desired. Follow steps 7-9 of the section “Setting Up A24/A32 Slave Images on the Bus” in this appendix.

Step 2 Set DARF Mode Control Register A16DI bit to disable the A16 space.

Step 3 Clear DARF Mode Control Register A24DI bit to enable the A24 space.

Step 4 Set DARF Mode Control Register A24P0 bit to locate the A24 space at 00xxxxxh of VME space.

Setting Up A24/A32 Slave Images on the Bus

In order for other boards in a VMEbus system to access the host's DRAM, the following steps must be taken to present a slave image onto the bus:

Step 1 Program DARF VMEbus Slave Base Address Register with appropriate A24 and/or A32 image size and base address value according to the register description.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com



CAUTION: The A24 base address must be a multiple of the amount of memory installed on board.

Step 2 Select the desired address protection boundary by entering the required value into DARF Access Protect Boundary Register.

Step 3 Set the A24SLVEN bit (located in the DARF Mode Control Register) if an A24 image is desired; clear it to disable the A24 image.

NOTE: The A32 slave image is always enabled unless all slave images (A24 and A32) are disabled as discussed in Step 5.

Step 4 Set the PROT bit (located in the DARF Mode Control Register) if both read and write protection of the selected address protection boundary is desired; clear it if only write protection is required.

NOTE: Access protection is only valid when memory is accessed using a slave image address.

Step 5 Set the VINEN bit (located in the DARF Mode Control Register) to enable all programmed A24/A32 images; clear it to disable all A24/A32 slave images.

NOTE: The following steps are only necessary when the slave image is programmed for the first time following power-up or board reset, and also after the system is forced into BI-mode by setting the SBI bit in the ACC General Control Register. When host is in BI-mode, all CPU cycles to/from the VMEbus are ignored.

Step 6 Check the BARDY bit of the DARF Control and Status Register to make sure it is set, which means that the slave image has been programmed correctly.

Step 7 Write any value to the location monitor (located at the top longword and the lower (even) word of the top longword in each of the A24 and A32 slave images) in order to exit from BI-mode, allowing accesses to/from VMEbus.



CAUTION: Since the location monitor is located in VME space, bit 31 of the address generated by the PTI host must be set, and the page bit (VPG) of the System Control Register programmed appropriately. Be aware that in order for the host to have access to the location monitor, the slave image must be in a proper space according to the master memory map. That is, in order to access the location monitor in the A32 slave image, the address must be in A32 space.

Step 8 Read from the DARF Location Monitor FIFO Read Port in order to clear the entry. A read access directly to the location monitor will be ignored.

Step 9 Check the BI bit in ACC Status Register 1 to make sure it is cleared, meaning that the ACC is not in BI-mode.

Example A:

To set up a 4 MByte, A32 image starting at VME address 08000000h with the lower 128KByte read/write protected, perform the following steps according to the above outline:

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Step 1 Write 141h to DARF VMEbus Base Address Register to select the size and base address.

Step 2 Write 2h to DARF Access Protect Boundary Register to select protection of lower 128 KBytes.

Step 3 Clear the A24SLVEN bit of DARF Mode Control Register to disable the A24 image.

Step 4 Set the PROT bit of DARF Mode Control Register to select read and write access protection of slave image.

Step 5 Set VINEN bit of DARF Mode Control Register to enable the slave image.

Step 6 Read the BARDY bit of DARF Control and Status Register to make sure it is set, verifying that the slave image has been programmed.

Step 7 Clear the VPG bit of the PT-VME151A System Control Register (address $0D000000) to select access of lower 2GB VMEbus space.

Write the value 0 (word or longword only) to address 883FFFFCh, disabling BI-mode by writing to the location monitor (with bit 31 of the address set).

Step 8 Do a dummy read from DARF Location Monitor FIFO Read Port to clear the useless location monitor entry from above step.

Step 9 Read the BI bit of ACC Status Register 1, make sure it's cleared, verifying that the slave image is now available on the VMEbus.

Example B:

To set up a 512 KByte, A32 image starting at VMEbus address 80000000h, and a 4 MByte, A24 image starting at VME address 400000h, with no image protection desired, perform the following steps:

Step 1 Write 6800F0h to DARF VMEbus Base Address Register selecting the size and base address of both A24/A32 images.

Step 2 Write 0 to DERF Access Protect Boundary Register selecting no protection.

Step 3 Set bit 10 of DARF Mode Control Register. Enable the A24 image.

Step 4 No need to program rd/wr protection bit since the no protection option is being used.

Step 5 Set the A24SLVEN bit of DARF Mode Control Register, enabling the slave image.

Step 6 Read the BARDY bit of DARF Control and Status Register, make sure it is set, verifying that the slave image has been programmed.

Step 7 Set VPG bit of PT-VME151A System Control Register (address $0D000000) selecting access of the upper 2GB VME space.

Write $0 (word or longword only) to address 883FFFFCh to disable BI-mode.

NOTE: If the A24 image was located in the DARF's master A24 space, then one could also access the location monitor at the A24 location, i.e. if the A24 image was set at address 01000000h, then a write to 804FFFFCh would access the location monitor. However,

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

another board can get at the location monitor in A24 space at any address with a valid A24 address modifier.

Step 8 Do a dummy read from DARF Location Monitor FIFO Read Port to clear the previous location monitor entry.

Step 9 Read the BI bit of ACC Status Register 1 to make sure it's cleared. Thus, verifying that the slave image is now available on the VMEbus.

Generating VMEbus Interrupts

Step 1 Make sure the system is not in BI-mode (refer to steps 6-9 of “Setting Up A24/A32 Slave Images on the Bus”).

Step 2 Program the DARF VMEbus Interrupt Vector Register with the interrupt vector desired.

Step 3 Select appropriate VMEbus interrupt level and assert the VMEbus interrupt by writing to the ACC VMEbus Interrupter Register.

Example:

To generate a level 4, vector 40h VMEbus interrupt, perform the following steps:

Step 1 Exit BI-mode. Follow steps 7-9 of the section “Setting Up A24/A32 Slave Images on the Bus” on page 102.

Step 2 Write 40h to DARF VMEbus Interrupt Vector Register, programming the interrupt vector.

Step 3 Write Ch to ACC VMEbus Interrupter Register, selecting a level 4 interrupt and asserting it on the VMEbus.

Receiving VMEbus Interrupts

Step 1 Make sure the system is not in BI-mode (refer to steps 7-9 of Setting Up A24/A32 Slave Images).

Step 2 Program the ACC VMEbus Interrupt Enable Register to accept the desired VMEbus interrupt levels.

Example:

To accept only level 1 and level 7 VMEbus interrupts, perform the following steps:

Step 1 Exit BI-mode. Follow steps 7-9 of the section “Setting Up A24/A32 Slave Images on the Bus”.

Step 2 Write 41h to the ACC VMEbus Interrupt Enable Register. This will allow level 1 and 7 VMEbus interrupts to be accepted.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Initiating a DMA Transfer

Step 1 Make sure the system is not in BI-mode (refer to steps 7-9 of “Setting Up A24/A32 Slave Images on the Bus” on page 102).

Step 2 Set the DARFEN bit (located in the DARF Mode Control Register) to enable DARF64 functions.

Step 3 Program the MBLT, BLT, BLT16 and DMARD bits (located in the DARF Mode Control Register) according to the type of DMA to be performed (i.e. D16/32/64, discrete or block transfers, reads or writes).

Step 4 Load the beginning local address into DARF DMA Local Address Register.

Step 5 Load the beginning VMEbus address into DARF DMA VMEbus Address Register. (Note: the DMA24 bit of the DARF Mode Control Register will override whatever addressing mode is implied by the VMEbus address being transferred to (A24:D16, etc.), and the A24PO bit will have no effect on the DMA's transfers).

Step 6 Load the transfer count into DARF DMA Transfer Count Register.

Step 7 Make sure that transmit FIFO is in decoupled mode by clearing the TXATOM bit (located in the DARF Mode Control Register).

Step 8 Make sure that the LBERR, VBERR, DONE and DMAGO bits (located in the DARF Control and Status Register) are cleared.

Step 9 Set the DMAGO bit to begin the DMA operation.

Step 10 Wait for the DONE bit to become set which means that the DMA has completed.

NOTE: If an error occurs during the DMA, it will stop and either the DLBER or VBERR bit will be set and the DONE bit will be cleared in the DARF Control and Status Register.

Example:

To start a 2 Kbyte, D32 write DMA with discrete cycles from local address 20001000h to an A24 VME address of 90000000h, perform the following steps:

Step 1 Exit BI-mode. Follow steps 7-9 of the section “Setting Up A24/A32 Slave Images on the Bus” on page 102.

Step 2 Set bit 31 of DARF Mode Control Register enabling DARF64 functions.

Step 3 Clear the MBLT, BLT, and DMARD bits of DARF64 Mode Control Register. MBLT low selects no D64 transfer, BLT low selects discrete VMEbus cycles and DMARD low selects writes from the local to the VMEbus. DMAD16 is a don't care, no BLT transfers. (These bits do not exist on a DARF32.)

Step 4 Write 1000h to DARF DMA Local Address Register to load the local address 20001000h. (The top 5 bits are unused.)

Step 5 Write 90000000h to DARF DMA VMEbus Address Register to load a VME address of 90000000h.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Step 6 Set the DMA24 bit of DARF Mode Control Register to enable the DMA to operate as an A24 master.

Step 7 Write 200h to DARF DMA Transfer Count Register to perform 512 longword transfers (2 Kbytes).

Step 8 Clear TXATOM bit of DARF Mode Control Register to put tx FIFO into decoupled mode.

Step 9 Write 0 to DARF Control and Status Register, clearing the LBERR, VBERR, DONE and DMAGO bits.

Step 10 Set the DMAGO bit of DARF Control and Status Register to start the DMA.

Step 11 Wait for the DONE bit of the DARF Control and Status Register to become set, which indicates DMA completion, if the VBERR or LBERR bits become set instead, an error has occurred.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

APPENDIX I: VMEbus Address Modifiers

VMEbus Address Modifier is a 6 bit field that is presented on the VMEbus Address Modifier signal lines during data transfer cycles. This table provides a quick summary of the Address Modifier codes. All values in hex.

Table 27: VMEbus Address Modifiers

Value	Function	PT-VME151A Transfer
3F	Standard supervisory block transfer	D32BLT
3E	Standard supervisory program access	D32
3D	Standard supervisory data access	D32
3C	Standard supervisory VME*64* transfer	D64MBLT
3B	Standard nonprivileged block transfer	D32BLT
3A	Standard nonprivileged program access	D32
39	Standard nonprivileged data access	D32
38	Standard nonprivileged VME*64* transfer	D64MBLT
2D	Short supervisory access	D32
29	Short nonprivileged access	D32
0F	Extended supervisory block transfer	D32BLT
0E	Extended supervisory program access	D32
0D	Extended supervisory data access	D32
0C	Extended supervisory VME*64* transfer	D64MBLT
0B	Extended nonprivileged block transfer	D32BLT
0A	Extended nonprivileged program access	D32
09	Extended nonprivileged data access	D32
08	Extended nonprivileged VME*64* transfer	D64MBLT
	Other codes either Reserved or User-defined.	Indeterminate (fault)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Section

8

INDEX

Symbols

+EPKIO 52, 53

Numerics

68040
see - MC68040
82C54 59, 71

A

A64 Addressing 33, 36
A64, A32, A24, A16
see - VMEbus, Address Modifiers
ACC 59, 69
Control and Status Register
TICKM 39
General Control Register
LTOEN 38
SBI 103
SWRST 38, 44
TLEN0 39
TLEN1 39
Interrupt Handler 39
interrupts 68, 101
Level 7 Interrupt Enable Register 101
Level 7 Interrupt Status Register
ACFIS 40
MEMIS 30, 40, 56
NMIIE 40
SYFIS 40
Local Interrupt Enable Register 101
L1E 41
L2E 41
L3E 42, 56
L4E 43
L5E 43
Local Interrupt Status Register
LI1 41
LI2 39, 41
LI3 42, 56
LI4 43
LI5 43
Local Interrupts 1 and 0 Control Register 101
1L1-1L0 41
Local Interrupts 3 and 2 Control Register 101
2L2-2L0 41
3L2-3L0 42
LIRQ2 32, 39
Local Interrupts 5 and 4 Control Register 101
4L2-4L0 43
5AV 43
5L2-5L0 43
setup 40
Requester Control Register 44
Status Register 0
ACFIP 40
CLRDOG 38
CLRTIK 39, 42
LTO 99
MEMIP 40, 56
NMIIP 40
SYFIP 40
Status Register 1
BI 103
SYSC 44
VMEbus Arbiter Register
VXL1-VXL0 45
VMEbus Interrupt Enable Register 105
VMEbus Interrupter Register 105
watchdog timer 13
ACFAIL* 40, 44

B

BBSY* 45
BCLR* 44
BERR* 45
BG0IN* 38, 44
BG3IN* 44
BI-mode
see - DARF64, BI-mode

C

Caching 91
CTS 52

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

D

D64MBLT
- description 33

DARF
- VMEbus Slave Base Address Register
  - A32SIZ 47, 58

DARF64 59, 70
- 68040 considerations 91
- Access Protect Boundary Register 100, 103
- address modifiers 35
- BI-mode 95, 98, 103
- Control and Status Register
  - BARDY 99, 103
  - DLBER 106
  - DMAGO 106
  - DONE 106
  - LBERR 38, 99, 100, 106
  - LMHD 96
  - VBERR 99, 106
- decoupled mode 33, 99
- DMA 36
  - performance 36
- DMA Local Address Register 36, 106
- DMA Transfer Count Register 36, 106
- DMA VMEbus Address Register 36, 106
- location monitor 37
- Location Monitor FIFO Read Port 103
- Memory Map Pages 102
- message FIFO 37
- Mode Control Register 36
  - 040 91
  - A16DI 98, 102
  - A24DI 98, 102
  - A24P0 102
  - A24PO 98, 102, 106
  - A24SLVEN 103
  - BLEN 36, 37
  - BLT 106
  - BLT16 106
  - DARFEN 106
  - DMA24 106
  - DMABEN 34, 37
  - DMARD 106
  - FIFOBEN 34, 37
  - LPBK 37
  - MBLT 106
  - NOREL 37
  - PROT 100, 103
  - RXATOM 34, 99, 100
  - TXATOM 34, 99, 106
  - VINEN 99, 100, 103
- Receive FIFO Address 38
- Receive FIFO Control 38
- Receive FIFO Data 38
- VMEbus addressing 35
- VMEbus Base Address Register 99
- VMEbus Interrupt Vector Register 105
- VMEbus mastership timeout 35
- VMEbus Slave Base Address Register 102

DRAM
- See RAM

DS1643 31, 59, 71
DSR 52, 53
DTR 52
DUART 52, 59, 72
- Auxiliary Control Register
  - ACR6-ACR4 52
  - Delta IP1 IRQ 52
  - Delta IP3 IRQ 53
- Channel A Mode Register
  - Tx RTS Control 53
- General Purpose Timer 52
- Input Port Register
  - IP1 52
  - IP3 53
  - IP5 53
- Interrupt Request 43
- interrupt setup 41
- Output Port Register
  - OPR0 53
  - OPR1 53
  - OPR3 53
  - OPR5 53
  - OPR6 53
  - OPR7 54

E

EBOARD 58
EEPROM, serial 31, 53, 54
EPAK 42, 58, 59
- address space 46, 93
- EPIRQ 42
- installation 20
- Interrupt Request 42
- interrupt setup 41
- Master Bus Error - DRAM Parity 30
- Pin assignments 78
- VMEbus Master access 47
- zero wait state access 58

EPROM 31
- configuration 14

Example
- Initiating DMA transfers 106
- VMEbus Interrupts

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

generation 105
receiving 105
VMEbus setup 104

F

FAS216 55, 59, 72
Alternate DMA mode 55, 91
Configuration Register 3 55
Alternate DMA mode 91
DMA 46, 56
Interrupt Register 42
Interrupt Request 42
Mode 2 55
Status Register
INT 42
Flash EPROM 31
configuration 14
front panel 73
Abort button 40
hexadecimal switch 50
indicators 74
Reset button 38
User LEDs 46

H

hexadecimal notation 8

I

Initialization requirements 92
inter-processor communication
see - Location Monitor 96
Interval Timer 71
Interrupt Request 41

J

JEDEC Devices 14
see ROM, PROM, EPROM, Flash EPROM and SRAM
Jumper Block
conventions 9
Default settings 67
K1 13, 67
K10 15, 67
K11 15, 67
K2 67
K3 15, 67
K4 15, 67
K5 67
K6 17, 67
K7 67
K8 67
K9 67
positions 12
summary 67

L

Local Reset 38, 45, 46, 47
Location Monitor 96
access 103
default address 60
longword data types 8

M

Main Memory 59
burst mode 36
MC68040 28
8-bit I/O considerations 92
auto-vector interrupts 40, 43, 44
burst mode 28
Bus Error - DRAM Parity 30
Cache clearing 93
Cache Control Register 92
Caching 91
caching EPAK space 46
CINV instruction 93
EPAK considerations 92
Exception processing 93
initialization 92
interrupts 68
non-serialized accesses 91
NOP instruction 92
Transparent Translation Registers 46, 92, 93
MC68681, see DUART
MC68EC040 9
Memory Map 59
message FIFO 37

N

Nonvolatile Timekeeping RAM 31, 59, 71

O

OS9 52

P

Parity 30
PROM 31
configuration 14
PTBUG 52, 60

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

R

RAM
- DRAM 28
  - Write Protected 60
- Initialization 31
- Nonvolatile
  - EEPROM 31
  - SRAM 31, 59
  - Timekeeping 31
- Parity 30
- SRAM 31

read-modify-write cycles 98
Register Maps 69
reserved fields 8
ROM 31
- configuration 14

RS-232 52
RTC 31, 59
RTS 52, 53

S

SCSI
- Cabling 23
- DMA Mechanism 46, 56
- MAR 59, 67
- RESET 30, 56
- termination 17, 55, 56
- TERMPWR 17
  - Overview 18

serial number location 11
Serial Port
- cabling 25
- setup, see DUART

signal name conventions 9
SRAM 31
- configuration 14

SRAM Module
- installation 19
- pin assignments 79

SYSCLK 44
SYSFAIL* 40
SYSRST* 38, 44
System Control Register 1 45, 59, 61
- ECE 93
- LED3-LED0 46
- SDIR 46
- VCE 46, 93
- VPG 46, 103

System Control Register 2 47, 59, 63
- EBP 31, 47
- EEAV 28, 47, 58
- EITI 32, 42, 49
- EPEC 30, 31, 47
- ETTI 39, 42
- RITI 42, 49

System Status Register 1 59, 64
- HSW 50

System Status Register 2 50, 59, 65
- 040PE 30, 50
- DARFPE 30, 50
- EPAKPE 30, 51
- SCSIP 51
- SCSIPE 30
- SDMAPE 50

System Status Register 3 51, 59, 66
- DRAMSZ 51
- ITIP2-ITIP0 33, 39, 42, 51
- PARI 51

T

TERMPWR 56
Timer
- General Purpose 52
- Interval 32
  - Interrupt Request 32
- Local Bus 38
- RTC 31
- Tick 39
  - Interrupt Request 39
- Timekeeping RAM 31
- VMEbus Data Transfer 45
- VMEbus Mastership 35, 44
- Watchdog 13, 38

U

Utility Serial Port
- connections 75
- see DUART

V

VME64
- features 33

VMEbus 59
- Address Modifiers 60, 96, 99, 102
  - list 108
- address pipelining 35
- address space 36, 46, 102
  - default 60
- Arbiter 44
- bandwidth considerations 94
- Bus Arbitration 44

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

bus error 100
Caching considerations 94
Data Transfer Time-out 45
data transfer timeout 100
IACK Daisy Chain Driver 44, 45
interrupt acknowledge cycle 41
Interrupt handler 39
interrupts 43, 68
memory map 96
ownership timer 44
P2 Connector 55
Page Selection 47
Pin assignments 76
Read-Modify-Write 36
Release on Request (ROR) 44
Release when Done (RWD) 44
setup 104
slave image 99, 100, 102, 103
Slot selection 21
System Clock Driver 44
System Controller functions 44

W

word data types 8

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Section

9

SCHEMATICS

Signal name cross references are available upon request.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP