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VMEbus EXPANSION INTERFACE

MODEL PT-VME901

USER'S MANUAL

DRAWING NUMBER: 126A000301

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PT-VME901
USER'S MANUAL

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1. GENERAL INFORMATION

1.1 Scope

This document provides support information for users of the Performance Technologies, Incorporated' VMEbus Expansion Interface, Model PT-VME901.

1.2 Applicable Documents

Reference to the following documents should be made in conjunction with this manual:

VMEbus Specification Manual, VMEbus Manufacturers Group

PAL Programmable Array Logic Handbook (Third Edition), Monolithic Memories, Incorporated

1.3 Features

The Model PT-VME901 VMEbus Expansion Interface has the following features:

* Buffered Interface That Supplies Drive For An Additional, Full Capacity VMEbus Load Configuration.
* VMEbus A24,D16 Compatible Master/Slave On Both Sides Of The Interface.
* Seven-Level Interrupt Support.
* VMEbus "System Clock" (SYSCLK) Generation And Bus Arbitration on The Non-Host Side Of The Interface.
* Supports VMEbus Maintenance Signals "Power Fail" (ACFAIL), "System Fail" (SYSFAIL) And "System Reset" (SYSRESET).
* Conforms To VMEbus Specification - Revision B.
* Two Board Set Consisting Of Two Double-Width EuroCard VMEbus Interfaces With Interconnect Cables Up To Six Feet Long.

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1.4 Specifications

Power, timing, environmental, and physical specifications for the PT-VME901 VMEbus Expansion Interface are as shown in Table 1-1.

Table 1-1 MODEL PT-VME901 SPECIFICATIONS

Characteristic	Specification(s)
Power Requirements Per Board	+5VDC(+/-5%) at 2.3 amperes, typ. at 2.9 amperes, max.
Total Signal Delay	Address Strobe (RD/WR) - 260ns typ. - 335ns max. Data Transfer Ack (RD) - 110ns typ. - 140ns max. Data Transfer Ack (WR) - 50ns typ. - 75ns max.
Ambient Temperature	0° to +55° C, operating -55° to +85° C, storage
Humidity	0% to 90% (non-condensing)
Physical	Two Standard Double-Width VME Boards (Per Board Dimensions) Width : 234 mm. (9.2 inches) Depth : 160 mm. (6.3 inches) Comp Height: 14 mm. (.55 inches) Front Panel: 20.3 mm. (.8 inches) Two Interconnection Shielded Cables 50 Cond Length: 1830 mm. (72 inches) 60 Cond Length: 1830 mm. (72 inches)

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1.5 General Description

The PT-VME901 supplies the electrical and physical means for interconnecting two VMEbus compatible subsystems, designated as Host and Non-Host, together. The Non-Host subsystem becomes an extension of the Host subsystem under the following guidelines:

1. A device in the Non-Host card-cage can interrupt a device in the Host card-cage or Non-Host card-cage. However, a device in the Host card-cage can only interrupt a device in the Host card-cage.

2. The System Controller Board (bus arbiter) must be located in the Host card-cage and provides the bus arbitration for the Host and Non-Host.

3. The direction of the "Power Fail" (ACFAIL) signal and "System Reset" (SYSRESET) signal is from the Host to the Non-Host, and the direction of the "System Fail" (SYSFAIL) signal is from the Non-Host to the Host.

The PT-VME901 provides the ability to readily expand a VMEbus based system that may be limited in its card slot or bus drive capacity. One application example for the interface is that of interconnecting a VMEbus compatible workstation or terminal having a limited expansion capacity to a full VMEbus card-cage. Another application example is that of interconnecting two VMEbus card-cages vertically stacked in a common cabinet or enclosure. A detailed block illustration of the PT-VME901 is depicted in Figure 1.

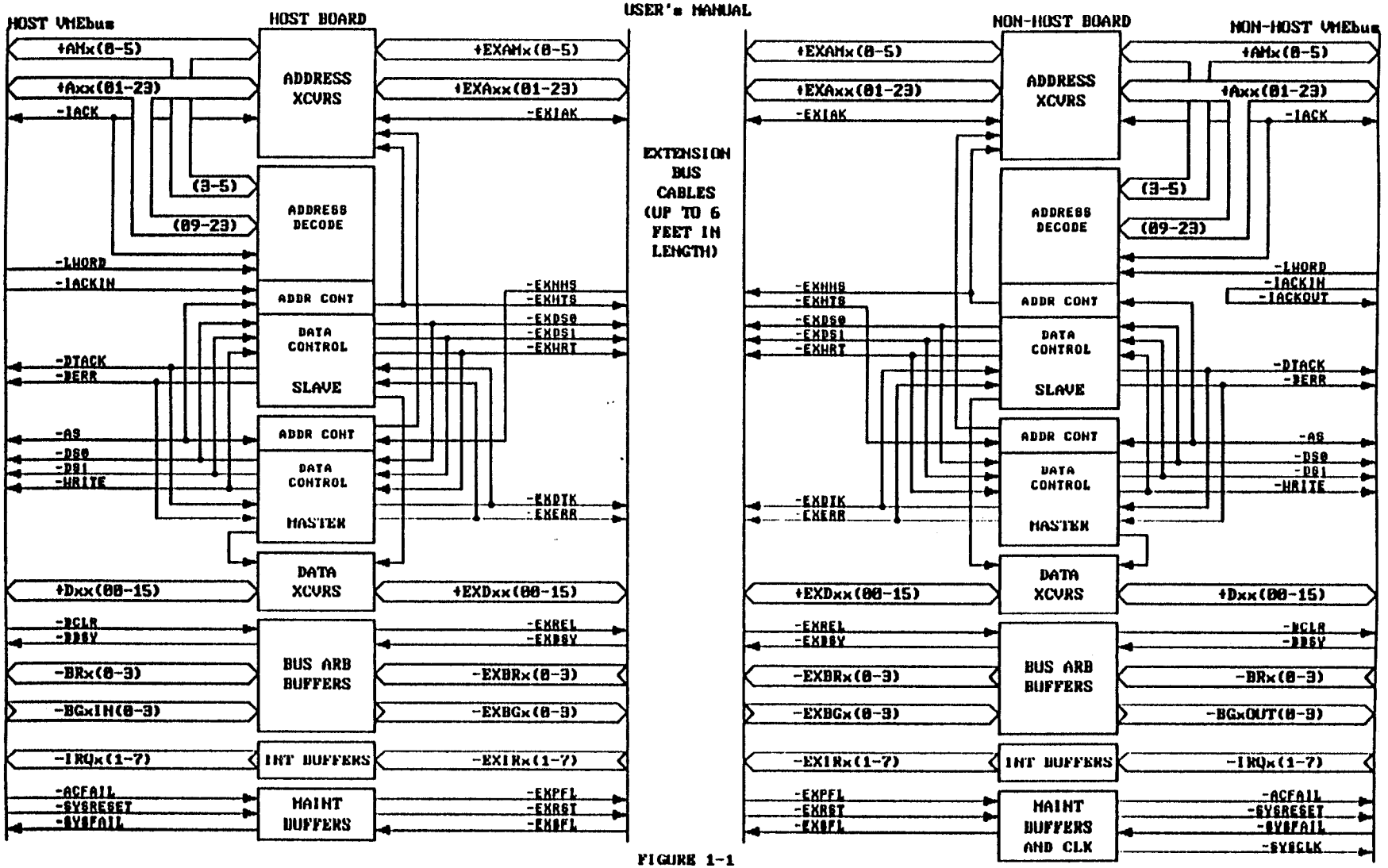


FIGURE 1-1
MODEL PT-VME901 BLOCK DIAGRAM
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2. HARDWARE PREPARATION

2.1 Unpacking And Inspection

******* CAUTION *******

The PT-VME901 contains integrated circuits that may be damaged by electrostatic discharge. Precautions should be taken when handling and touching the PT-VME901 to minimize the risk of such static damage.

The shipping carton should be inspected for any possible damage that may have occurred during shipment. If such damage is noted, an agent of the shipping carrier should be present at any further unpacking and contents inspection.

Unpack contents from shipping carton and verify against packing list. Inspect the PT-VME901 assembly for any visible signs of shipping damage. If such damage is noted, report such damage to Performance Technologies, Incorporated and **do not proceed** with any further configuration and installation.

2.2 Factory Configuration

2.2.1 Slave Address Select Range

The PT-VME901 utilizes a PAL[1] (PTI Part #800P013200) on each board (Host and Non-Host) of the interface to decode the slave I/O and memory address range. At time of shipment, these PALs are identically programmed with a factory standard configuration which is as follows:

Host Memory Address Range	000000 - 7FFFFF
Host I/O Address Range	0000 - 7FFF
Non-Host Memory Address Range	800000 - FFFFFF
Non-Host I/O Address Range	8000 - FFFF

Note that the user should consult the factory prior to shipment if an address range configuration, other than the specified standard, is required. Refer to section 2.3.1 for PAL programming information if the user wishes to program the PAL in-house.

(1) PAL (Programmable Array Logic) is a registered trademark of Monolithic Memories, Incorporated

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2.2.2 Jumper Options (K1,K2)

The PT-VME901 provides one (1) jumper per board (Host and Non-Host) for configuration purposes, with board location as illustrated in Figure 2-1. At time of shipment, these jumpers are installed per a factory standard configuration. The factory standard configuration is given in Table 2-1. Note that the designation (C) indicates that a jumper should be installed between the points indicated, whereas the designation (NC) indicates that no connection should be made to the point(s) indicated.

Table 2-1 FACTORY CONFIGURATION

Jumper	Function	Factory Configuration
Host K1	Extension Bus Release	Host VMEbus "Bus Clear" (BCLR) Sent To Non-Host 2-3(C),1(NC)
Host K2	Host/Non-Host Select	Host Selected 1,2(NC)
Non-Host K1	Extension Bus Release	"Don't Care" When Non-Host Selected 1-3(NC)
Non-Host K2	Host/Non-Host Select	Non-Host Selected 1-2(C)

Host K1 should have a jumper pin 2 to 3
K2 should not have a jumper

Non-Host K1 should not have a jumper
K2 should have a jumper pin 1 to 2

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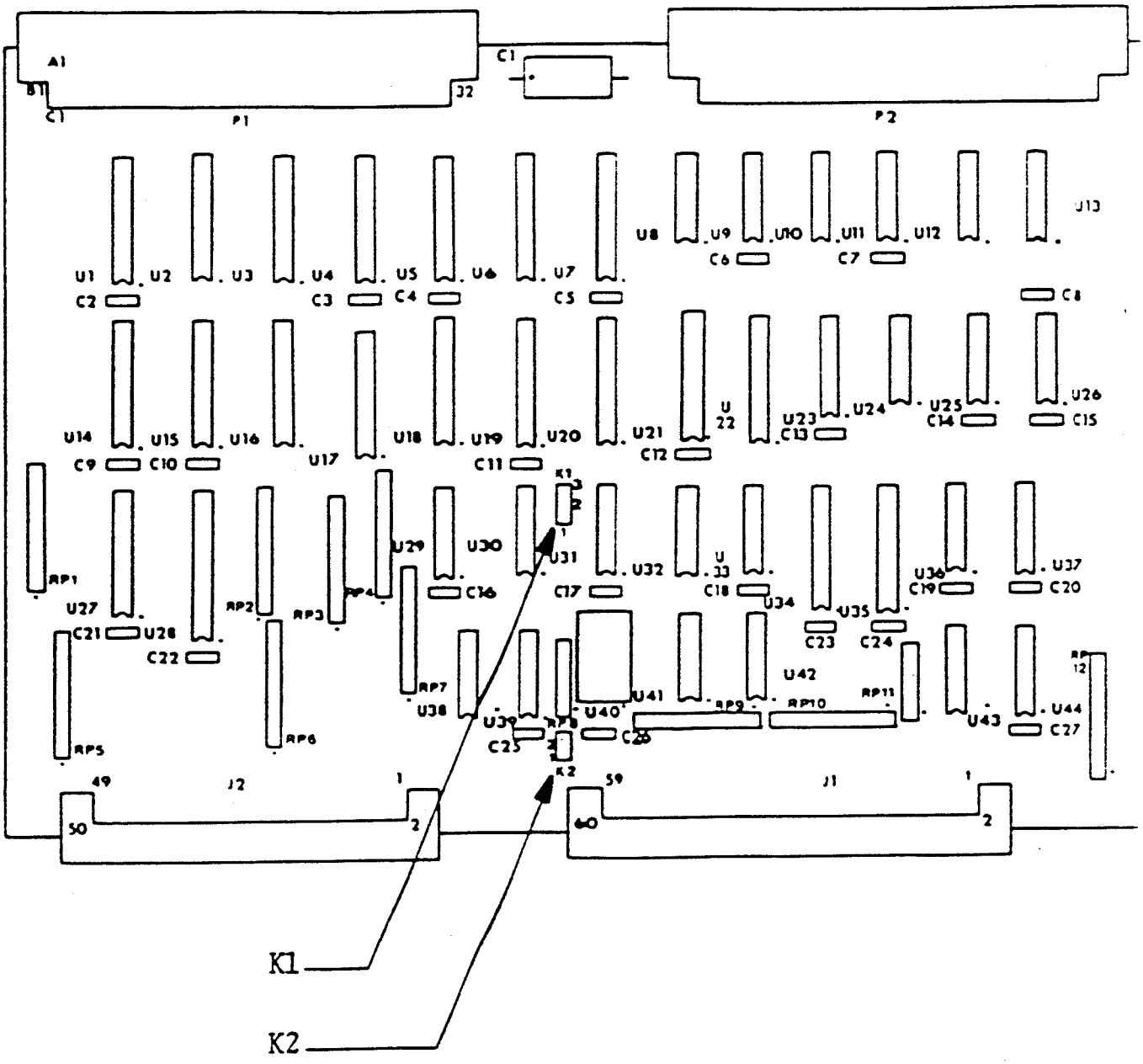


FIGURE 2-1

MODEL PT-VME901 CONFIGURATION JUMPER LOCATION

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2.3 Configuration Options

2.3.1 Slave Address Select Range

The PT-VME901 uses two identically programmed PALs (Monolithic Memories Part #PAL20L8ACNS or equivalent), one on the Host and the other on the Non-Host, to decode the slave I/O and memory address range. The PALs are located in IC location U28, and the pin-out for these PALs are as follows:

Pin 1	VMEbus Address Bit 23 Input
Pin 2	VMEbus Address Bit 22 Input
Pin 3	VMEbus Address Bit 21 Input
Pin 4	VMEbus Address Bit 20 Input
Pin 5	VMEbus Address Bit 19 Input
Pin 6	VMEbus Address Bit 18 Input
Pin 7	VMEbus Address Bit 17 Input
Pin 8	VMEbus Address Bit 16 Input
Pin 9	VMEbus Address Bit 15 Input
Pin 10	VMEbus Address Bit 14 Input
Pin 11	VMEbus Address Bit 13 Input
Pin 13	VMEbus Address Bit 12 Input
Pin 14	VMEbus Address Bit 11 Input
Pin 17	VMEbus Address Bit 10 Input
Pin 18	VMEbus Address Bit 09 Input
Pin 19	VMEbus Address Modifier Bit 5 Input
Pin 20	VMEbus Address Modifier Bit 4 Input
Pin 23	VMEbus Address Modifier Bit 3 Input
Pin 15	I/O - Address Modifier Decode Output
Pin 16	I/O - Address Decode Output
Pin 21	Memory - Address Modifier Decode Output
Pin 22	Memory - Address Decode Output

All eighteen (18) of the PAL inputs are "high true". The two (2) Address Decode Outputs (I/O and Memory) are "low true" and should be programmed with the desired Non-Host address range using the VMEbus Address Bits available to the PAL. Note that Address Bits 16 through 23 should never be used for the I/O Address Decode since the maximum range for I/O is 64K bytes. The two (2) Address Modifier Decode Outputs (I/O and Memory) are "low true" and should be programmed with the bits 3*4*5 for memory (Pin 21) and 3*/4*5 for I/O (Pin 15) using the VMEbus Address Modifier Bits available to the PAL.

An example would be the following equations using the above mentioned pin numbers for the factory standard specified in section 2.2.1:

```
/22 = 1              /16 = 9
/21 = 19*20*23       /15 = 19*/20*23
```

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2.3.2 **Jumper Options (K1,K2)**

The configuration options for the PT-VME901 are outlined in the following sub-sections. Reference Figure 2-1 for configuration option jumper locations. Note that the designation (C) indicates that a jumper should be installed between the points indicated, whereas the designation (NC) indicates that no connection should be made to the point(s) indicated.

2.3.2.1 **Extension Bus Release (K1)**

Host (ref. 2.3.2.2) jumper header K1 provides the means on the PT-VME900 Series Interface Adapters of configuring the Non-Host "bus release" function as one of the following options:

Host "Bus Clear" (BCLR)	K1-2 To K1-3(C) K1-1(NC)
Any Host "Bus Request" (BR0-3)	K1-1 To K1-2(C) K1-3(NC)
Not Used	K1-1,K1-2,K1 3(NC)

For continuity between both sides of the PT-VME901, the recommended Non-Host "bus release" function is the Host "Bus Clear" (BCLR) since this becomes the Non-Host "Bus Clear" (BCLR). Note that the Non-Host (ref. 2.3.2.2) jumper header K1 is a "don't care" since the direction of the "Bus Clear" (BCLR)

signal is only from the Host to the Non-Host.

2.3.2.2 **Host/Non-Host Select (K2)**

Jumper header K2 provides the means of configuring each board of the PT-VME901 (two board set) as a Host or Non-Host. The following options distinguish the two identical boards and configure the boards for the respective functions:

Host	K2-1,K2-2(NC)
Non-Host	K2-1 To K2-2(C)

Note that one board of the two board set must be configured as the Host and the other as the Non-Host (ref. 1.5).

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2.4 INSTALLATION

2.4.1 Pre-Installation Procedure

Before proceding with the PT-VME901 installation, a decision must be made as to which card-cage is to be the Host and which card-cage is to be the Non-Host. Use the following points for a basis to make this decision:

1. A device in the Non-Host card-cage can interrupt a device in the Host card-cage or Non-Host card-cage. However, a device in the Host card-cage can only interrupt a device in the Host card-cage.

2. The System Controller Board (bus arbiter) must be located in the Host card-cage.

3. The direction of the "Power Fail" (ACFAIL) signal and "System Reset" (SYSRESET) signal is from the Host to the Non-Host, and the direction of the "System Fail" (SYSFAIL) signal is from the Non-Host to the Host.

Also, before installing the PT-VME901, both boards should be configured as required (ref. 2.3), and the voltage levels supplied to both the Host and Non-Host card-cages into which the PT-VME901 is to be installed should be measured **before installation** to insure that they are within the range given in Table 1-1. Note that if the same power supply is not used for both the Host and Non-Host card-cages, a good common reference ground should be established between the two power supplies for proper operation of the PT-VME901.

********** CAUTION **********

The PT-VME901 should never be inserted or removed from the Host and Non-Host card-cages while power is applied. Such insertion/removal with power applied could seriously damage the PT-VME901 components.

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2.4.2 Installation Procedure

The System Controller Board (bus arbiter), which is not part of the PT-VME901, should be located in slot A01 of the Host card-cage. The Host (ref. 2.3.2.2) side of the PT-VME901 should be installed as the last board in the interrupt acknowledge and bus arbitration daisy-chains on the VMEbus backplane in the Host card-cage.

The Non-Host (ref. 2.3.2.2) side of the PT-VME901 should be installed in slot A01 of the Non-Host card-cage. No System Controller Board should be installed into the Non-Host card-cage since all system controller functions are handled by the PT-VME901.

Connect the Host and Non-Host boards of the PT-VME901 together by attaching the 50 conductor and 60 conductor shielded cables (6 ft) into the front panel of each board.

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3. FUNCTIONAL ELEMENTS

The PT-VME901 is made-up of two (2) identical boards and uses two shielded cables to interconnect them. Jumper header K2 (ref. 2.3.2.2) on each board determines if that board is to be the Host or Non-Host. The Host/Non-Host function determines the direction of several control signals on the Extension Bus (ref. 4.2 and 4.3) which is used to connect the Host and Non-Host together. The functional elements for the PT-VME901 are outlined in the following sub-sections and depicted in Figure 1-1.

3.1 Data Transfer Control

The data transfer control uses a full master and slave to transfer data between the Host and Non-Host and is VMEbus A24,D16 compatible.

The Host or Non-Host slave decodes memory and I/O address ranges (ref. 2.2.1 and 2.3.1) in response to a VMEbus master within that card-cage, and if the decoded address range is in the other card-cage, the slave will send a select signal across the Extension Bus (ref. 4.2 and 4.3) to the PT-VME901 master on the opposite side. This master will then generate the necessary signals and timing to access the appropriate slave. Note that no response is given on any attempt to transfer longword (32 bit) data.

3.2 Interrupt Signals

The seven (7) "Interrupt Request" (IRQ1-7) signals are buffered across the Extension Bus (ref. 4.2) from the Non-Host to the Host, and only a Host master can initiate an interrupt acknowledge cycle across the PT-VME901. This in no way restricts a Host device from interrupting a Host device and a Non-Host device from interrupting a Non-Host device.

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3.3 Bus Arbitration Signals

The four (4) "Bus Request" (BR0-3) signals and "Bus Busy" (BBSY) signal are buffered across the Extension Bus (ref. 4.2) from the Non-Host to the Host, and the four (4) "Bus Grant" (BG0-3) signals and "Bus Clear" (BCLR) signal (ref. 2.3.2.1) are buffered from the Host to the Non-Host. The direction of these signals specify that the bus arbiter (system controller function) must be located in the Host card-cage.

3.4 Maintenance Signals

The maintenance signals "Power Fail" (ACFAIL) and "System Reset" (SYSRESET) are buffered across the Extension Bus (ref. 4.2) from the Host to the Non-Host, and the maintenance signal "System Fail" (SYSFAIL) is buffered across the Extension Bus from the Non-Host to the Host. The "System Clock" (SYSCLK) signal is generated by the PT-VME901 Non-Host.

3.5 Extension Bus

The Extension Bus is used to interconnect the Host and Non-Host boards together through two shielded cables. This bus is made-up of seventy-three (73) signal lines that are terminated with 330/470 resistor networks and thirty-six (36) signal grounds (GND) that are connected to logic ground. Refer to section 4.2 and 4.3.

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4. PRODUCT SUPPORT INFORMATION

4.1 VMEbus P1 Interface

The PT-VME901 VMEbus P1 interface is made via a standard DIN 41612, 96 pin, male connector. Table 4-1 details the specific P1 interface interconnection assignments.

4.2 Extension Bus J1 Interface

The PT-VME901 Extension Bus J1 interface is made via a 60 pin male connector. The J1 interface is for all control signals. Table 4-2 details the specific J1 interface interconnection assignments.

4.3 Extension Bus J2 Interface

The PT-VME901 Extension Bus J2 interface is made via a 50 pin male connector. The J2 interface is for all address and data signals. Table 4-3 details the specific J2 interface interconnection assignments.

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Table 4-1 VMEbus P1 Interface

PIN	SIGNAL	DESCRIPTION
A1	+D00	Data Bit 00
A2	+D01	Data Bit 01
A3	+D02	Data Bit 02
A4	+D03	Data Bit 03
A5	+D04	Data Bit 04
A6	+D05	Data Bit 05
A7	+D06	Data Bit 06
A8	+D07	Data Bit 07
A9	GND	Ground
A10	+SYSCLK	System Clock
A11	GND	Ground
A12	-DS1	Data Strobe 1
A13	-DS0	Data Strobe 0
A14	-WRITE	Read/Write Control
A15	GND	Ground
A16	-DTACK	Data Transfer Acknowledge
A17	GND	Ground
A18	-AS	Address Strobe
A19	GND	Ground
A20	-IACK	Interrupt Acknowledge
A21	-IACKIN	Interrupt Daisy-Chain Input
A22	-IACKOUT	Interrupt Daisy-Chain Output
A23	+AM4	Address Modifier Bit 4
A24	+A07	Address Bit 07
A25	+A06	Address Bit 06
A26	+A05	Address Bit 05
A27	+A04	Address Bit 04
A28	+A03	Address Bit 03
A29	+A02	Address Bit 02
A30	+A01	Address Bit 01
A31	N/U	Not Used
A32	+5V	+5VDC Input

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Table 4-1 VMEbus P1 Interface (continued)

PIN	SIGNAL	DESCRIPTION
B1	-BBSY	Bus Busy
B2	-BCLR	Bus Clear
B3	-ACFAIL	AC Power Fail
B4	-BG0IN	Bus Grant 0 Input
B5	-BG0OUT	Bus Grant 0 Output
B6	-BG1IN	Bus Grant 1 Input
B7	-BG1OUT	Bus Grant 1 Output
B8	-BG2IN	Bus Grant 2 Input
B9	-BG2OUT	Bus Grant 2 Output
B10	-BG3IN	Bus Grant 3 Input
B11	-BG3OUT	Bus Grant 3 Output
B12	-BR0	Bus Request 0
B13	-BR1	Bus Request 1
B14	-BR2	Bus Request 2
B15	-BR3	Bus Request 3
B16	+AM0	Address Modifier Bit 0
B17	+AM1	Address Modifier Bit 1
B18	+AM2	Address Modifier Bit 2
B19	+AM3	Address Modifier Bit 3
B20	GND	Ground
B21	N/U	Not Used
B22	N/U	Not Used
B23	GND	Ground
B24	-IRQ7	Interrupt Request 7
B25	-IRQ6	Interrupt Request 6
B26	-IRQ5	Interrupt Request 5
B27	-IRQ4	Interrupt Request 4
B28	-IRQ3	Interrupt Request 3
B29	-IRQ2	Interrupt Request 2
B30	-IRQ1	Interrupt Request 1
B31	N/U	Not Used
B32	+5V	+5VDC Input

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Table 4-1 VMEbus P1 Interface (continued)

PIN	SIGNAL	DESCRIPTION
C1	+D08	Data Bit 08
C2	+D09	Data Bit 09
C3	+D10	Data Bit 10
C4	+D11	Data Bit 11
C5	+D12	Data Bit 12
C6	+D13	Data Bit 13
C7	+D14	Data Bit 14
C8	+D15	Data Bit 15
C9	GND	Ground
C10	-SYSFAIL	System Fail
C11	-BERR	Bus Error
C12	-SYSRESET	System Reset
C13	-LWORD	Long Word Transfer
C14	+AM5	Address Modifier Bit 5
C15	+A23	Address Bit 23
C16	+A22	Address Bit 22
C17	+A21	Address Bit 21
C18	+A20	Address Bit 20
C19	+A19	Address Bit 19
C20	+A18	Address Bit 18
C21	+A17	Address Bit 17
C22	+A16	Address Bit 16
C23	+A15	Address Bit 15
C24	+A14	Address Bit 14
C25	+A13	Address Bit 13
C26	+A12	Address Bit 12
C27	+A11	Address Bit 11
C28	+A10	Address Bit 10
C29	+A09	Address Bit 09
C30	+A08	Address Bit 08
C31	N/U	Not Used
C32	+5V	+5VDC Input

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Table 4-2 Extension Bus J1 Interface

PIN	SIGNAL	DESCRIPTION
1	GND	Ground
2	-EXIR7	Interrupt Request 7
3	GND	Ground
4	-EXIR6	Interrupt Request 6
5	GND	Ground
6	-EXIR5	Interrupt Request 5
7	GND	Ground
8	-EXIR4	Interrupt Request 4
9	GND	Ground
10	-EXIR3	Interrupt Request 3
11	GND	Ground
12	-EXIR2	Interrupt Request 2
13	GND	Ground
14	-EXIR1	Interrupt Request 1
15	GND	Ground
16	-EXIAK	Interrupt Acknowledge
17	GND	Ground
18	-EXREL	Bus Release
19	GND	Ground
20	-EXBSY	Bus Busy
21	GND	Ground
22	-EXSFL	System Fail
23	GND	Ground
24	-EXPFL	Power Fail
25	GND	Ground
26	N/U	Not Used
27	GND	Ground
28	-EXBR3	Bus Request 3
29	GND	Ground
30	-EXBR2	Bus Request 2

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Table 4-2 Extension Bus J1 Interface (continued)

PIN	SIGNAL	DESCRIPTION
31	GND	Ground
32	-EXBR1	Bus Request 1
33	GND	Ground
34	-EXBR0	Bus Request 0
35	GND	Ground
36	-EXBG3	Bus Grant 3
37	GND	Ground
38	-EXBG2	Bus Grant 2
39	GND	Ground
40	-EXBG1	Bus Grant 1
41	GND	Ground
42	-EXBG0	Bus Grant 0
43	GND	Ground
44	-EXERR	Bus Error
45	GND	Ground
46	-EXDTK	Data Transfer Acknowledge
47	GND	Ground
48	-EXDS1	Data Strobe 1
49	GND	Ground
50	-EXDS0	Data Strobe 0
51	GND	Ground
52	-EXWRT	Read/Write Control
53	GND	Ground
54	-EXNHS	Non-Host Select (AS)
55	GND	Ground
56	-EXHTS	Host Select (Address Strobe)
57	GND	Ground
58	GND	Ground
59	-EXRST	Reset
60	GND	Ground

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Table 4-3 Extension Bus J2 Interface

PIN	SIGNAL	DESCRIPTION
1	GND	Ground
2	+EXA01	Address Bit 01
3	+EXA02	Address Bit 02
4	+EXA03	Address Bit 03
5	+EXA04	Address Bit 04
6	+EXA05	Address Bit 05
7	+EXA06	Address Bit 06
8	+EXA07	Address Bit 07
9	+EXA08	Address Bit 08
10	+EXA09	Address Bit 09
11	+EXA10	Address Bit 10
12	+EXA11	Address Bit 11
13	+EXA12	Address Bit 12
14	+EXA13	Address Bit 13
15	+EXA14	Address Bit 14
16	+EXA15	Address Bit 15
17	+EXA16	Address Bit 16
18	+EXA17	Address Bit 17
19	+EXA18	Address Bit 18
20	+EXA19	Address Bit 19
21	+EXA20	Address Bit 20
22	+EXA21	Address Bit 21
23	+EXA22	Address Bit 22
24	+EXA23	Address Bit 23
25	GND	Ground

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Table 4-3 Extension Bus J2 Interface (continued)

PIN	SIGNAL	DESCRIPTION
26	+EXAM5	Address Modifier Bit 5
27	+EXAM4	Address Modifier Bit 4
28	+EXAM3	Address Modifier Bit 3
29	+EXAM2	Address Modifier Bit 2
30	+EXAM1	Address Modifier Bit 1
31	+EXAM0	Address Modifier Bit 0
32	GND	Ground
33	GND	Ground
34	+EXD15	Data Bit 15
35	+EXD14	Data Bit 14
36	+EXD13	Data Bit 13
37	+EXD12	Data Bit 12
38	+EXD11	Data Bit 11
39	+EXD10	Data Bit 10
40	+EXD09	Data Bit 09
41	+EXD08	Data Bit 08
42	+EXD07	Data Bit 07
43	+EXD06	Data Bit 06
44	+EXD05	Data Bit 05
45	+EXD04	Data Bit 04
46	+EXD03	Data Bit 03
47	+EXD02	Data Bit 02
48	+EXD01	Data Bit 01
49	+EXD00	Data Bit 00
50	GND	Ground

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