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32-BIT VMEBUS REPEATER
MODEL PT-VME910

USER'S MANUAL

DRAWING NUMBER: 106A0130

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This document presents information for users of the Performance Technologies, Incorporated' Model PT-VME910 32 Bit VMEbus Repeater.

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1.0 GENERAL INFORMATION

SCOPE

This document provides support information for users of the Performance Technologies, Incorporated' 32 Bit VMEbus Repeater, Model PT-VME910.

APPLICABLE DOCUMENTS

Reference to the following documents should be made in conjunction with this manual:

- VMEbus Specification Manual (Revision C.1)
- IEC 821 Bus and IEEE P1014/D1.2,
- VMEbus International Trade Association (VITA)

FEATURES

The Model PT-VME910 32 Bit VMEbus Repeater has the following features:

- Buffered Interface That Supplies Drive For An Additional, Full Capacity, VMEbus Load Configuration.
- Master/Slave Timing Compensation - VMEbus A32,D32 Compatible.
- Bidirectional Seven (7) Level VMEbus Interrupt Channel - VMEbus IH(1-7) Compatible.
- Four (4) Level VMEbus Arbitration - VMEbus RWD/ROR Compatible.
- Supports Both "Star" And "Daisy-Chain" Configurations For Multiple VMEbus Card-Cage Systems.
- Host Board To Non-Host Board Interconnect Use Readily Available Fifty Conductor Cable And Connectors.
- Conforms To VMEbus Specification - Revision C.1.
- Consists Of Two (2) 32 Bit VMEbus Interface Boards (Double-Width EuroCard Form Factor) With Standard Six (6 Foot Long Interconnect Cables (20 Foot Absolute Maximum).

2.0 INSTALLATION

UNPACKING AND INSPECTION

The PT-VME910 contains integrated circuits that may be damaged by electrostatic discharge. Precautions should be taken when handling and touching the PT-VME910 to minimize the risk of such static damage.

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The shipping carton should be inspected for any possible damage that may have occurred during shipment. If such damage is noted, an agent of the shipping carrier should be present at any further unpacking and contents inspection.

Unpack contents from shipping carton and verify against packing list. Inspect the PT-VME910 assembly for any visible signs of shipping damage. If such damage is noted, report such damage to Performance Technologies, Incorporated and do not proceed with any further configuration and installation.

HARDWARE CONFIGURATION

The PT-VME910 has been configured at the factory to meet the needs of the majority of users. Your specific application may, however, require that the factory configuration be altered. It is recommended that the "Functional Element" descriptions in Section 3 of this manual be studied prior to altering any configuration options.

INTERRUPT HANDLER LOCATION SELECT

Switch U48, located on the Host PCB and switch U26, located on the Non-Host PCB, select the direction in which interrupts are routed. The switches should be set so that interrupts are sent to the card cage (Host or Non-Host) in which the Interrupt Handler for that level is located.

"*" indicates factory configuration.

Interrupt Handler Level/Location	Switch Positions	
*Level 1 (IRQ1) in Host	Host	U48-1 Off
	Non-Host	U26-1 On
Level 1 (IRQ1) in Non-Host	Host	U48-1 On
	Non-Host	U26-1 Off
*Level 2 (IRQ2) in Host	Host	U48-2 Off
	Non-Host	U26-2 On
Level 2 (IRQ2) in Non-Host	Host	U48-2 On
	Non-Host	U26-2 Off

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*Level 3 (IRQ3) in Host	Host	U48-3 Off
	Non-Host	U26-3 On
Level 3 (IRQ3) in Non-Host	Host	U48-3 On
	Non-Host	U26-3 Off
*Level 4 (IRQ4) in Host	Host	U48-4 Off
	Non-Host	U26-4 On
Level 4 (IRQ4) in Non-Host	Host	U48-4 On
	Non-Host	U26-4 Off
*Level 5 (IRQ5) in Host	Host	U48-5 Off
	Non-Host	U26-5 On
Level 5 (IRQ5) in Non-Host	Host	U48-5 On
	Non-Host	U26-5 Off
*Level 6 (IRQ6) in Host	Host	U48-6 Off
	Non-Host	U26-6 On
Level 6 (IRQ6) in Non-Host	Host	U48-6 On
	Non-Host	U26-6 Off
*Level 7 (IRQ7) in Host	Host	U48-7 Off
	Non-Host	U26-7 On
Level 7 (IRQ7) in Non-Host	Host	U48-7 On
	Non-Host	U26-7 Off

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RELEASE-ON-REQUEST NON-HOST MASTER ENABLE/DISABLE

Jumper header K1 located on both the Host and Non-Host PCBs are used to enable/disable the Non-Host master release-on-request feature. If this feature is enabled, Non-Host Bus Request Level 0 (BR0) will become the Oared condition of all four Host Bus Request Levels (BR0 through BR3) for Non-Host release-on-request (ROR) masters.

Non-Host Master R-O-R Mode	**Jumpers IN, all others OUT**	
*Enabled	Host	K1-1 to K1-2
	Non-Host	K1-1 to K1-2
Disabled	Host	K1-2 to K1-3
	Non-Host	K1-2 to K1-3

3.0 INSTALLATION

PRE-INSTALLATION PROCEDURE

Before proceeding with the PT-VME910 installation, a decision must be made as to which card-cage is to be the Host and which card-cage is to be the Non-Host. Use the following points for a basis to make this decision:

The System Controller Board (bus arbiter) must be located in the Host card-cage.

The direction of the System Reset (SYSRESET) signal and Power Fail (ACFAIL) signal are from the Host to the Non-Host, and the direction of the System Fail (SYSFAIL) signal is from the Non-Host to the Host.

Also, before installing the PT-VME910, both boards should be configured as required, and the voltage levels supplied to both the Host and Non-Host card-cages into which the PT-VME910 is to be installed should be measured before installation to insure that they are within the specified range. Note that if the same power supply is not used for both the Host and Non-Host card-cages, a good common reference ground should be established between the two power supplies for proper operation of the PT-VME910.

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The PT-VME910 should never be inserted or removed from the Host and Non-Host card-cages while power is applied. Such insertion/removal with power applied could seriously damage the PT-VME910 components.

CARD-CAGE PREPARATION

The System Controller Board (bus arbiter), which is not part of the PT-VME910, must be located in slot A01 of the Host card-cage. The Host side of the PT-VME910 may be installed in any slot on the VMEbus backplane in the Host card-cage keeping in mind that the interrupt acknowledge daisy-chain (IACKIN/IACKOUT) and the bus grant daisy-chains (BG0IN/BG0OUT through BG3IN/BG3OUT) must be used. The daisy-chain jumpers on the backplane must be removed for this slot. Note that multiple “first level” Non-Host card-cages may be added to a single Host card-cage by adding an extra PT-VME910 for every Non-Host card-cage added (star configuration).

The Non-Host side of the PT-VME910 must be installed in slot A01 on the VMEbus backplane in the Non-Host card-cage. The daisy-chain jumpers on the backplane must be removed for this slot. No System Controller Board should be installed into the Non-Host card-cage since all system controller functions are handled by the PT-VME910. Note that one or more “second level” Non-Host card-cages may be added to this “first level” Non-Host card-cage by installing the Host side of an additional PT-VME910 into any slot of the “first level” Non-Host card-cage (daisy-chain configuration).

NOTE: A large percentage of customer assistance requests received by Performance Technologies, regarding the PT-VME910, are caused by improper installation of card-cage jumpers. CHECK YOUR JUMPERS!

CABLE INSTALLATION

The PT-VME910 uses four, industry standard, 50-pin flat cables as the board-to-board connection.

The cables must be connected before the boards are installed in the cardcage. To install the cables, remove the cable clamp by removing three M2.5 screws which secure it to the front panel. The cables are installed by matching the “J” numbers on the PCB silk-screen with the numbers stamped on the cables. After making the connections, reinstall the cable clamp using the three M2.5 screws.

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4.0 PRODUCT SPECIFICATIONS

GENERAL DESCRIPTION

The PT-VME910 32 Bit VMEbus Repeater is a fully buffered and timing compensated interface for connecting two VMEbus compatible card-cages together. VMEbus masters, slaves, interrupt handlers and interrupters located on either side of the repeater functionally appear to be in the same cardcage.

The PT-VME910 supplies the electrical and physical means for interconnecting two VMEbus compatible subsystems, designated as Host and Non-Host, together. The Non-Host subsystem becomes an extension of the Host subsystem under the following guidelines:

The system controller function, located in the Host cardcage, provides the bus arbitration and system reset for the Host and Non-Host.

The direction of the System Reset and Power Fail signals are from the Host to the Non-Host, and the direction of the System Fail signal is from the Non-Host to the Host.

Multiple VMEbus card-cages may be interconnected in a “star” or “daisy-chain” configuration, or a combination of the two, by adding a PT-VME910 for each additional VMEbus cardcage.

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SPECIFICATIONS

Table 1. Mechanical & Environmental Specifications

Characteristic	Specification
Ambient Temperature	0^{o} to $+55^{o}$ C, operating
	-55^{o} to $+85^{o}$ C, storage
Humidity	0% to 90% (non-condensing)
Mechanical	Per Board Dimensions For Two (2) Standard Double-Width VMEbus Boards:
	Width: 234 mm. (9.2 inches)
	Depth: 160 mm. (6.3 inches)
	Comp Height:12.7 mm. (0.5 inches)
	Front Panel:20.3 mm. (0.8 inches)
	Per Cable Dimensions For Four 50 conductor flat cables:
	Length: 1830 mm. (72 inches)

ELECTRICAL SPECIFICATIONS

Table 2. Electrical Specifications

Characteristic	Specification
Power Requirements (Per Board)	+5Vdc (5%) at 3.8 Amps, typical. 5.8 Amps, maximum.
Total Signal Delay With 6 Foot Cables	AS (RD/WR) 115ns typical - 135ns max.
	DSx (RD) 135ns typ.- 155ns max.
	DSx (WR) 190ns typ.- 215ns max.
	DTACK (RD) 100ns typ.- 120ns max.
	DTACK (WR) 35ns typ. - 50ns max.
Required Bus Timing	AS Asserted - 100ns min. (false-to-true transition to true-to-false transition)

FUNCTIONAL ELEMENTS

The PT-VME910 is made up of a Host and a Non-Host 32 Bit VMEbus Interface Board and uses the Extension Bus to interconnect them via four cables. The functional elements for the PT-VME910 are outlined in the following subsections.

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DATA TRANSFER CONTROL

The data transfer control on the PT-VME910 is used by the VMEbus master to transfer data to/from an addressed slave in another VMEbus cardcage and used by a VMEbus interrupt handler to transfer the interrupt vector from an interrupter in another VMEbus cardcage. The data transfer control is VMEbus A32,D32 compatible and supports byte/word/longword aligned/unaligned data transfers, read-modify-write cycles, sequential block cycles and address pipelining. The added delay in the data transfer cycle incurred by the master when the slave is on the opposite side of the repeater, is the amount of time added for the Address Strobe/Data Strobes (AS/DS0/DS1) to be received by the slave plus the Data Transfer Acknowledge (DTACK) to be received by the master. A typical added delay of 235 nanoseconds is incurred for a READ cycle and 225 nanoseconds is incurred for a WRITE cycle.

When a data transfer is initiated in the Host or Non-Host by the bus master, the data transfer control on the PT-VME910 will initiate the same transfer on the other end of the repeater with compensation for any signal skew. If the addressed slave is located on the opposite side of the repeater relative to the bus master, the data transfer control will respond to the bus master in the same way that the slave responded.

INTERRUPT CONTROL

The interrupt control on the PT-VME910 is used by a VMEbus interrupter to interrupt a VMEbus interrupt handler in another VMEbus cardcage. The interrupt control is VMEbus IH(1-7) compatible, supplies an IACK daisy-chain driver and supports interrupt requests/acknowledges across the repeater in both directions.

When an Interrupt Request (IRQ1-IRQ7) is issued in the Host or Non-Host by an interrupter and, if the interrupt request direction switch is set accordingly, for that interrupt request level, the interrupt control on the PT-VME910 will issue that Interrupt Request on the other end of the repeater. When the interrupt handler responds with an interrupt acknowledge cycle, the data transfer control on the PT-VME910 will initiate the same interrupt acknowledge cycle back on the other side of the repeater with compensation for any signal skew. The Interrupt Acknowledge daisy-chain (IACKIN/IACKOUT) will always originate in the Host and then branch to the first Non-Host cardcage or Host interrupter that is issuing an Interrupt Request on that level.

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BUS ARBITRATION CONTROL

The bus arbitration control on the PT-VME910 is used by a Non-Host VMEbus master to gain control of the Host and Non-Host data transfer buses. The bus arbitration control is VMEbus RWD/ROR compatible and supports Non-Host VMEbus arbitration and an optional Host VMEbus request for Non-Host VMEbus Release-On-Request (ROR) masters.

Since the VMEbus Requests (BR0-BR3) are buffered from the Non-Host to the Host, a Non-Host VMEbus Release-On-Request (ROR) master will not be able to sense when a Host VMEbus master is requesting the use of the Host and Non-Host data transfer busses. However, the Non-Host Bus Request level 0 (BR0) may be optionally jumpered on the PT-VME910 to be either buffered to the Host Bus Request level 0 (same as other levels) or an OR'ed condition of all the Host Bus Requests (BR0 through BR3) buffered to the Non-Host. The OR'ed condition has timing compensation so the Non-Host master will not sense its own Bus Request.

MAINTENANCE SIGNALS

The maintenance signals System Reset (SYSRESET) and AC Power Fail (ACFAIL) are buffered across the Extension Bus from the Host to the Non-Host, and the maintenance signal System Fail (SYSFAIL) is buffered across from the Non-Host to the Host. The Non-Host System Clock (SYSCLK) is generated by the PT-VME910.

EXTENSION BUS

The Extension Bus is used to interconnect the Host and Non-Host 32 Bit VMEbus Interface Boards together through four 50 conductor cables.

5.0 PRODUCT SUPPORT

If you encounter difficulty in using this Performance Technologies, Inc. product, you can contact our support personnel in one of several ways.

Internet

www.pt.com

This is the preferred method of customer support. If you have email services, email us at, support@pt.com.

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Telephone

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Request Product Support. Our offices are open between 8:00 am and 5:00 pm Eastern Time, Monday through Friday.

If you are located outside North America, we encourage you to contact the local PTI distributor or agent for support. Many of our distributors or agents maintain technical support staffs.

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