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Performance Technologies

ZT 4804

Rear Transition Module

User’s and System Integrator’s Guide

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Contents

Tables **5**

Figures **5**

1 Introduction **6**

1.1 Product Definition 6

1.2 Features 6

1.3 Functional Blocks 8

Rear-Panel I/O 9

Dual Ethernet Channels 9

SMBus Interface 10

Isolated User Inputs 10

Alarm Relay Outputs 10

Serial I/O 10

ACO Switch 10

Reset Switch 10

Hot Swap Activation 11

EIDE Interface 11

Floppy Drive Interface 11

PS/2 Keyboard Port 11

PS/2 Mouse Port 11

LED Indicators 12

2 Configuration **13**

2.1 SMBus Registers 13

2.2 Jumper Options and Locations 14

2.3 Jumper Descriptions 16

W1—W6 (Alarm Relay Outputs) 16

W7 (External User Input 1: DC Voltage Selection) 16

W8 (External User Input 2: DC Voltage Selection) 17

2.4 Cuttable Trace Definitions 17

3 Connectors **18**

3.2 Backplane Connectors 20

J1 (User Input/Alarm Relay Output Connector) 20

3.3 Front Panel Connectors 21

J2, J4 (COM1, COM2 Serial Ports) 21

J3 (Rear-Panel User I/O Connector) 21

J5 (Keyboard Connector) 22

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J6 (Mouse Port Connector) 22
J7, J8 (Ethernet A, B Connectors) 22
3.4 Internal Connectors 23
J9 (EIDE Connector) 23
J10 (Floppy Drive Connector) 24
J11 (Reserved) 25
4 Specifications 26
4.1 Electrical Specifications 26
4.2 Environmental Specifications 26
4.3 Reliability 27
4.4 Mechanical Specifications 27
Board Dimensions and Weight 27
Connectors 27
5 In Case of Difficulty 28

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Tables

Table 1. SMBus Output Register 13
Table 2. SMBus Input Register 14
Table 3. Jumper Cross-Reference 14
Table 4. Cuttable Trace Definitions 17
Table 5. Connector Assignments 18
Table 6. J1 User Input/Alarm Relay Output Connector Pinout 20
Table 7. J2, J4 (COM1, COM2 Serial Ports) Pinout 21
Table 8. J3 Rear-Panel User I/O Connector Pinout 21
Table 9. J5 Keyboard Connector Pinout 22
Table 10. J6 Mouse Port Connector 22
Table 11. J7, J8 (Ethernet A, B Connectors) Pinout 22
Table 12. J9 EIDE Connector Pinout 23
Table 13. J10 Floppy Drive Connector Pinout 24
Table 14. J11 Reserved Connector Pinout 25

Figures

Figure 1. Faceplate 8
Figure 2. Functional Block Diagram 9
Figure 3. Factory Default and Customer Jumper Configuration 15
Figure 4. Connector Locations 19
Figure 5. Board Dimensions 27

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Section

1 Introduction

This section provides a brief introduction to the ZT 4804 Rear Transition Module (RTM). It includes a product definition, a list of product features, a "Faceplate" figure, a functional block diagram, and a description of each block.

See Section 2, "Configuration," for configuration details and Section 3, "Specifications," for complete power and temperature requirements, as well as connector locations, descriptions, and pinout tables.

1.1 Product Definition

The ZT 4804 is a single slot, 6U rear-panel transition board providing rear-panel access to the I/O functions of specific Performance Technologies processor boards. The ZT 4804 also provides interfaces for two user inputs and six alarm relay outputs. It is designed to function only in the rear-panel slot of a 6U CompactPCI* system (such as a ZT 5411 enclosure).

1.2 Features

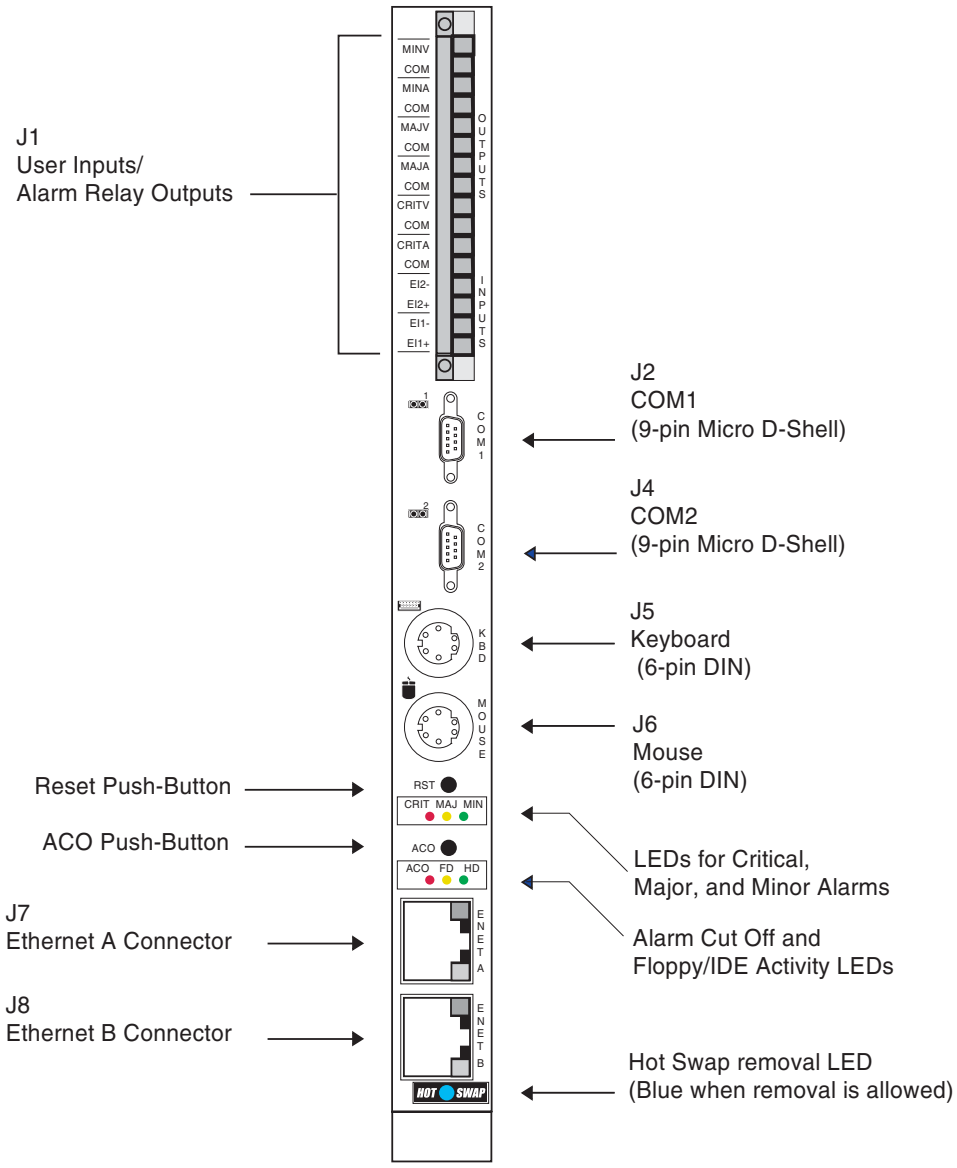
- SMBus interface for alarm control
- Six single-pole normally open or normally closed (jumper-selectable) relay outputs (critical, major and minor; audible and visual)
- Two optically-isolated debounced user inputs (5 V or 60 V input range, jumper-selectable)
- Host hot-swap activation via bottom ejector latch circuitry
- Rear-panel interface connectors for host:
  - COM 1 micro-miniature (MDSM) DB-9 serial
  - COM 2 micro-miniature (MDSM) DB-9 serial
  - PS/2 Keyboard
  - PS/2 Mouse
  - Ethernet A
  - Ethernet B (in non-High Availability systems only)
- Internal interfaces (i.e., not on the faceplate):
  - Floppy Interface
  - IDE Interface (Host secondary channel only)

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- Rear-panel switches:
  - ACO Switch
  - Reset Switch
  - Hot-Swap Initiate (integrated in the bottom ejector lever)
- Rear-panel LEDs indicate:
  - Critical, Major, and Minor Alarms
  - Floppy drive active
  - IDE drive active
  - Alarm Cut-off (ACO)
  - Hot Swap LED (indicates when it's OK to remove the board)
- Five-year warranty

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Figure 1. Faceplate

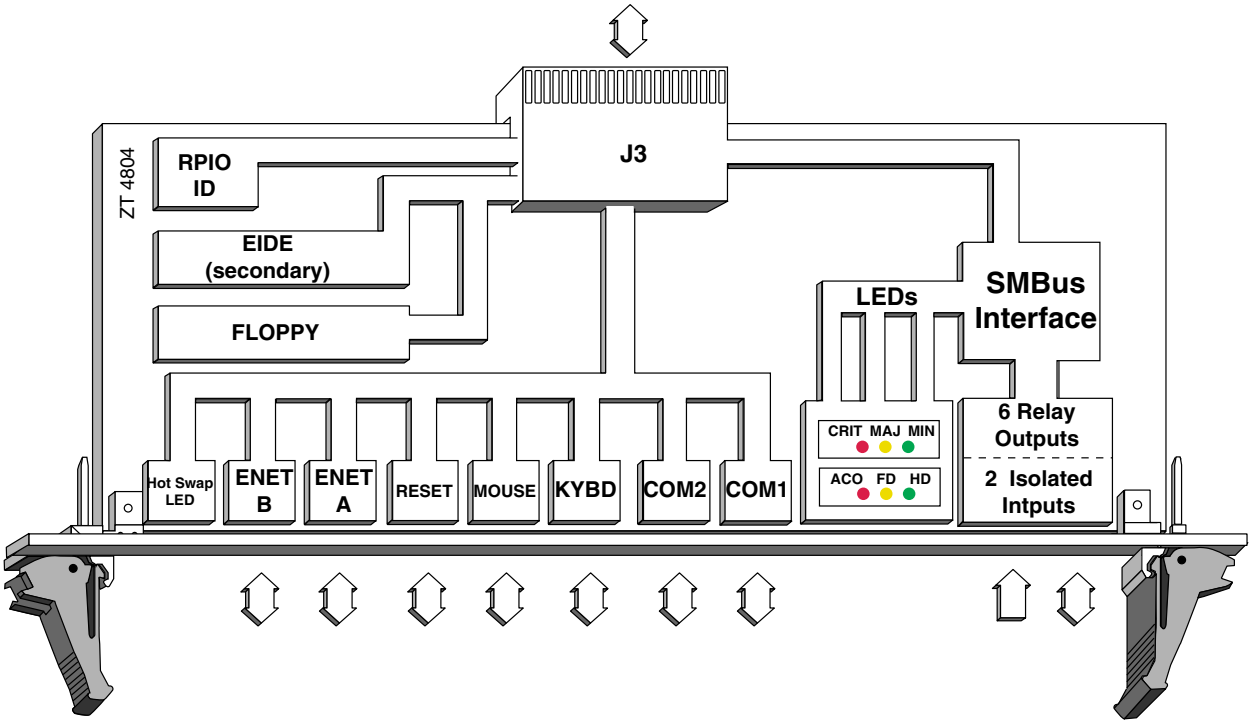


1.3 Functional Blocks

Below is a functional block diagram of the ZT 4804. The following topics provide overviews of the functional blocks.

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Figure 2. Functional Block Diagram



Rear-Panel I/O

The ZT 4804 transitions I/O signals from the processor board for rear-panel use via a 95-pin, 2 mm x 2 mm, female connector (J3).

Dual Ethernet Channels

The ZT 4804 transitions the processor board's Ethernet channels A and B for rear-panel access. Both 10 Mbit/s and 100 Mbit/s Ethernet protocols are provided through each of two RJ-45 rear-panel connectors.

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SMBus Interface

The ZT 4804 incorporates an SMBus interface between the processor board and the ZT 4804 to provide access to alarm and system monitoring functions. The ZT 4804 provides isolation of the local SMBus from the processor board during Hot Swap cycles. All SMBus devices are accessed via a Performance Technologies device driver. The ZT 4804 SMBus implementation provides two 8-bit registers for I/O and control functions. Refer to "SMBus Registers" in Section 3 for register information.

Isolated User Inputs

The ZT 4804 provides two optically isolated debounced inputs for application use. These inputs are available on J1, a 16-pin, 150 mil connector. The inputs must be biased from an external source and are configurable through jumpers (W7 and W8) to sense either 0-5 VDC or 0-60 VDC input levels. Reverse polarity and over-voltage protection are provided. These inputs are available as rear-panel inputs only; no provision is made for front-panel (processor board) connections.

Alarm Relay Outputs

The ZT 4804 provides six alarm relay outputs. These outputs are available on J1, a 16-pin, 150 mil connector. J1 provides one output pole per relay. The ZT 4804 allows configuration of the output pin pair as either a normally open or normally closed pole through jumpers (W1 - W6).

Serial I/O

The ZT 4804's two serial port connectors, J2 (COM1) and J4 (COM2), provide an alternative means of accessing the processor board's COM1 and COM2 serial ports. The optional ZT 90248 adapter cable is available for use with J2 and J4. Contact Performance Technologies for more information.

ACO Switch

The ZT 4804 provides an Alarm Cut Off (ACO) push button switch (S2) for defeating the three audible alarm output signals. Under software control, an LED indicator is illuminated when the ACO switch is activated.

Reset Switch

The ZT 4804 features a reset push-button switch (S1) on the faceplate. When S1 is pressed, a System Reset is issued to the host processor board to force the processor to restart program execution. No local debounce is implemented.

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Hot Swap Activation

The ZT 4804 provides an ejector sense mechanism for triggering a Hot Swap event. Opening the ZT 4804's lower ejector handle initiates a Hot Swap event to begin the extraction process; closing the handle signals an insertion request. A change in the ejector position causes the PCI signal ENUM# to be asserted, which in turn signals the Hot Swap Manager to begin handling the event. A blue LED indicator on the faceplate illuminates when board removal is permitted.

For a complete definition of CompactPCI Hot Swap, obtain a copy of the *CompactPCI Hot Swap Specification, PICMG 2.1, Version 1.0.* The document is available for a nominal fee from PICMG at:

http://www.picmg.org

EIDE Interface

The ZT 4804 provides access to the processor board's secondary EIDE channel through an internal connector (J9), a 40-pin 0.1" vertical header.

Floppy Drive Interface

The ZT 4804 provides access to the processor board's floppy controller through an internal connector (J10), a 34-pin 0.1" vertical header.



Caution: Do not connect the floppy drive directly to system power. Floppy disks in the drive may become corrupted. Power the floppy drive from the host processor board. This causes the floppy drive power and control lines to become active at the same time, thereby maintaining signal integrity. For development purposes floppy power may be sourced from J11.

PS/2 Keyboard Port

The ZT 4804 provides a PS/2 style keyboard port (J5) that duplicates the processor board's keyboard connector. Either the ZT 4804 keyboard port or the processor board keyboard connector, but not both, may be used at any one time.

PS/2 Mouse Port

The ZT 4804 provides a PS/2 style mouse port (J6) that duplicates the processor board's mouse connector. Either the ZT 4804 mouse port or the processor board mouse connector, but not both, may be used at any one time.

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LED Indicators

As shown in the “Faceplate” figure, the ZT 4804 provides several LEDs indicating the following:

- Floppy access
- IDE access
- Alarm Cut-off
- Alarm Conditions
  - Critical (red)
  - Major (yellow)
  - Minor (green)
- Hot Swap Removal Indicator

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Section

2 Configuration

The ZT 4804 RTM's SMBus implementation provides two 8-bit registers for I/O and control functions.

Several jumper options on the ZT 4804 tailor its operation to meet the requirements of specific applications. In most cases, the default jumper settings are appropriate for normal operation. However, some applications may require different settings. Jumper options are made by installing and removing shorting receptacles.

The ZT 4804’s cuttable traces are reserved and should not be modified by the user. This section describes SMBus registers and jumper options and lists the cuttable traces on the ZT 4804. An illustration showing jumper locations is also provided.

2.1 SMBus Registers

Table 1. SMBus Output Register

Bit	Description
7	Control the ACO LED state
6	Clear the ACO switch latch state
5	Control the Minor Visual relay state
4	Control the Minor Audible relay state
3	Control the Major Visual relay state
2	Control the Major Audible relay state
1	Control the Critical Visual relay state
0	Control the Critical Audible relay state

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Table 2. SMBus Input Register

Bit	Description
7	Read the state of option strap bit ID1
6	Read the state of option strap bit ID0
5	Read the status of the local 3.3V DC-DC converter
4	Read the state of the ACO switch latch
3	Not used
2	Not used
1	Read the state of the EXT2 input
0	Read the state of the EXT1 input

2.2 Jumper Options and Locations

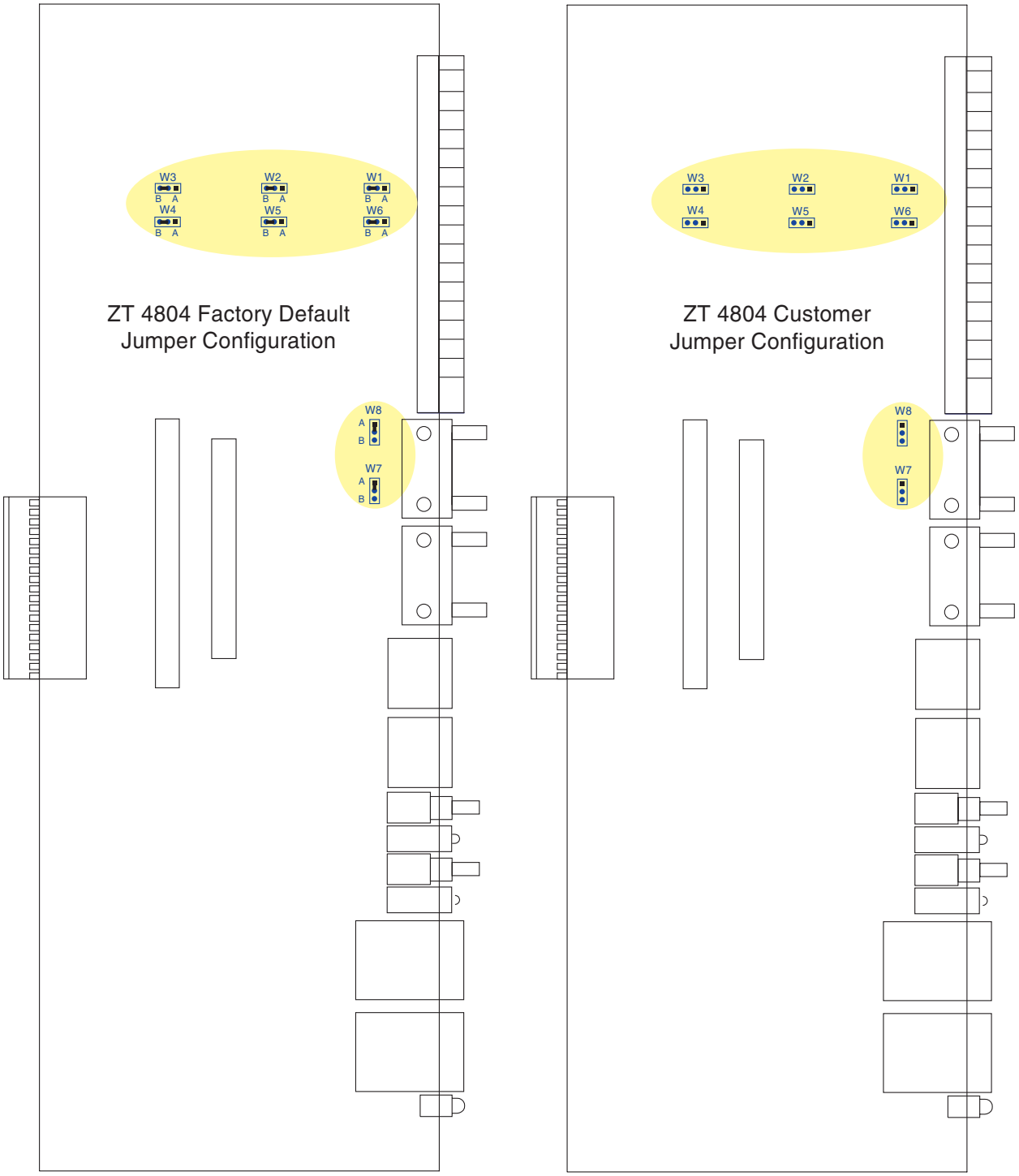
The ZT 4804's eight jumpers are listed and briefly described in the "Jumper Cross-Reference" table below. Factory default jumper configuration is shown in the figure "Factory Default and Customer Jumper Configuration". The customer portion of the figure provides a blank jumper layout; use this to document your configuration if it differs from the factory default. This will allow you to easily restore the configuration if it is changed for any reason.

Table 3. Jumper Cross-Reference

Function	Jumper
Alarm Relay Outputs	W1-W6
External User Inputs	W7, W8

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Figure 3. Factory Default and Customer Jumper Configuration



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2.3 Jumper Descriptions

The following topics present the jumpers in numerical order and provide a detailed description of each jumper.

W1—W6 (Alarm Relay Outputs)

The ZT 4804 provides six alarm relay outputs. These outputs are available on J1, a 16-pin, 150 mil connector. J1 provides two output terminals per relay. The ZT 4804 allows configuration of the output terminal pair as either a normally open (default) or normally closed connection, as defined in the following table.

Alarm Relay	Normally Open (1)	Normally Closed	J1 Common Terminal	J1 Switched Terminal
Critical audible	W6B	W6A	Pin 5	Pin 6
Critical visual	W5B	W5A	Pin 7	Pin 8
Major audible	W4B	W4A	Pin 9	Pin 10
Major visual	W3B	W3A	Pin 11	Pin 12
Minor audible	W2B	W2A	Pin 13	Pin 14
Minor visual	W1B	W1A	Pin 15	Pin 16

NOTE:

1. Factory Default

W7 (External User Input 1: DC Voltage Selection)

W7 is used to select the DC voltage level of **external user input 1** (EI1+ and EI1-). The voltage level is configurable to be either 0-5 VDC or 0-60 VDC, as shown in the table below. This input is available on connector J1. The factory default is position A.

Position	User Input 1: DC Voltage Selection	J1
W7B	0 - 5 VDC	Pin 1, EI1+
W7A Default	0 - 60 VDC	Pin 2, EI1-

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W8 (External User Input 2: DC Voltage Selection)

W8 is used to select the DC voltage level of **external user input 2** (EI2+ and EI2-). The voltage level is configurable to be either 0-5 VDC or 0-60 VDC, as shown in the table below. This input is available on connector J1. The factory default is position A.

Position	User Input 2: DC Voltage Selection	J1
W8B	0 - 5 VDC	Pin 3, EI2+
W8A Default	0 - 60 VDC	Pin 4, EI2-

2.4 Cuttable Trace Definitions

The ZT 4804 contains several cuttable traces (zero Ω shorting resistors) listed in the "ZT 4804 Cuttable Trace Definitions" table below.



Caution: The ZT 4804's cuttable traces are reserved and should not be modified by the user. The product warranty is voided if the board is damaged by customer modifications.

Table 4. Cuttable Trace Definitions

CT#	Default	Description
CT1	In	Configure Input circuits for 12.5 ms debounce delay (319 Hz)
CT2	Out	Configure Input circuits for 125.2 us debounce delay (31.9 kHz)
CT3	Out	Reserved — Do not modify
CT4	In	Reserved — Do not modify
CT5	In	Reserved — Do not modify
CT7	In	Reserved — Do not modify
CT8	In	Reserved — Do not modify
CT9	In	Connect Floppy Activity LED to MTR0
CT10	Out	Reserved — Do not modify
CT11	In	Reserved — Do not modify
CT12	In	Reserved — Do not modify
CT13	In	Reserved — Do not modify
CT14	In	Reserved — Do not modify
CT15	Out	Reserved — Do not modify

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Section

3 Connectors

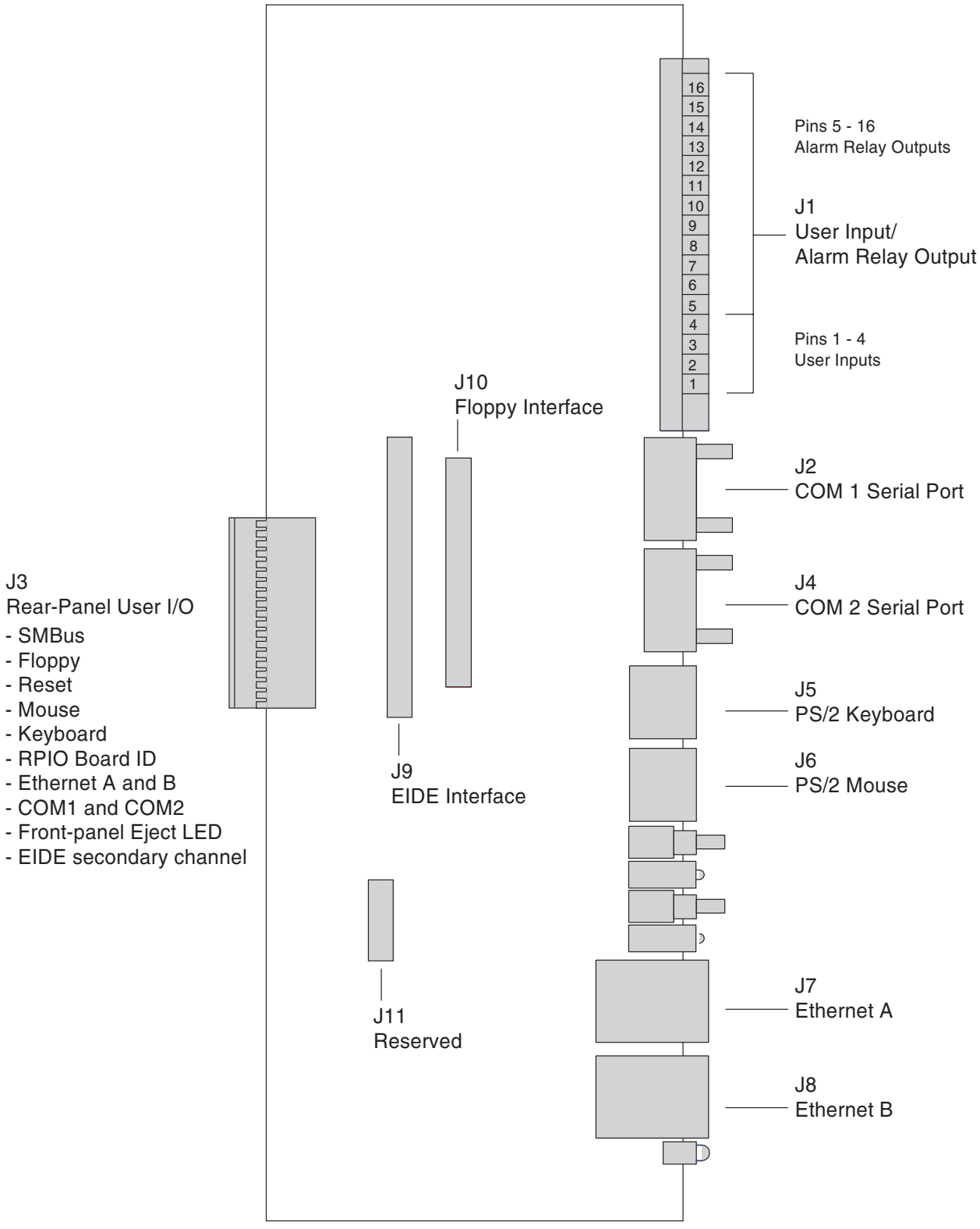
As shown in the "Connector Locations" figure, the ZT 4804 includes several connectors to interface to application-specific devices. A brief description of each connector is given in the "ZT 4804 Connector Assignments" table below. A detailed description and pinout for each connector is given in the following topics.

Table 5. Connector Assignments

Connector	Function
J1	User Input/Alarm Relay Output Connector (16-position)
J2	COM1 Serial Port (9-pin, D-Shell)
J3	Rear-Panel User I/O Connector (95-pin 2 mm x 2 mm, female)
J4	COM2 Serial Port (9-pin, D-Shell)
J5	PS/2 Keyboard Connector (6-pin, DIN)
J6	PS/2 Mouse Port Connector (6-pin, DIN)
J7	Ethernet Connector A (8-pin, RJ-45)
J8	Ethernet Connector B (8-pin, RJ-45)
J9	EIDE Connector (40-pin)
J10	Floppy Drive Connector (34-pin)
J11	Reserved

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Figure 4. Connector Locations



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3.2 Backplane Connectors

J1 (User Input/Alarm Relay Output Connector)

J1 is a 16-position, 3.81 mm pitch connector (Phoenix Contact type MC 1,5/16-GF-3,81; order # 18 28 00 03) providing an interface for two user inputs and six alarm relay outputs. The corresponding Phoenix Contact mating connector is order # 18 27 84 02.

User inputs must be biased from an external source and are configurable through jumpers (W7 and W8) on the processor board to sense either 0-5 VDC or 0-60 VDC input levels. There are two output terminals per alarm relay (one each for visual and audible). Jumpers (W1-W6) are used to configure the output pin pair as either a normally open or normally closed connection.

See the “J1 User Input/Alarm Relay Output Connector Pinout” table below for pin definitions.

Table 6. J1 User Input/Alarm Relay Output Connector Pinout

Pin #	Alarm Relay Outputs	Normally Open	Normally Closed
16	Minor Visual (Switched)	W1B	W1A
15	Minor Visual (Common)		
14	Minor Audible (Switched)	W2B	W2A
13	Minor Audible (Common)		
12	Major Visual (Switched)	W3B	W3A
11	Major Visual (Common)		
10	Major Audible (Switched)	W4B	W4A
9	Major Audible (Common)		
8	Critical Visual (Switched)	W5B	W5A
7	Critical Visual (Common)		
6	Critical Audible (Switched)	W6B	W6A
5	Critical Audible (Common)		
Pin #	**User Inputs**	**Input Range Selection**	
4	External Input 2 (-)	W8A = 0-5 VDC / W8B = 0-60 VDC	
3	External Input 2 (+)		
2	External Input 1 (-)	W7A = 0-5 VDC / W7B = 0-60 VDC	
1	External Input 1 (+)		

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3.3 Front Panel Connectors

J2, J4 (COM1, COM2 Serial Ports)

J2 and J4 are 9-pin Micro D-shell connectors (ITT/Cannon MDSM-9PE-Z10-VR25 or equivalent) providing rear-panel interfaces to the processor board's COM1 and COM2 serial channels. See the "J2/J4 COM1/COM2 Serial Ports Pinout" table below for pin definitions.

Table 7. J2, J4 (COM1, COM2 Serial Ports) Pinout

Pin #	Function	Pin #	Function	Pin #	Function
1	DCD	4	DTR	7	RTS
2	RXD	5	GND	8	CTS
3	TXD	6	DSR	9	RIN

J3 (Rear-Panel User I/O Connector)

J3 is a 95-pin, 2 mm x 2 mm, female connector (AMP 646488-1 or equivalent) transitioning I/O signals from the processor board for rear-panel use. See the "J3 Rear-Panel User I/O Interface Pinout" table below for pin definitions.

Table 8. J3 Rear-Panel User I/O Connector Pinout

Pin #	Z	A	B	C	D	E	F
19	(GND)	PWRGD	IOCS16#	IORDY	**SMALRT#**	**IRQ15**	GND
18	(GND)	**SMDATA**	**SMCLK**	**CS3S#**	**CS1S#**	**RPID**	GND
17	(GND)	DD15	DD14	DD13	DD12	**EJECT#**	GND
16	(GND)	DD11	DD10	DD9	DD8	SDDAK#	GND
15	(GND)	DA0	DA1	**J3VCC**	DA2	SDDRQ	GND
14	(GND)	DD7	DD6	DD5	DD4	SDIOW#	GND
13	(GND)	DD3	DD2	DD1	DD0	SDIOR#	GND
12	(GND)	DR0#	MSEN0	MTR0#	INDEX#	WDATA#	GND
11	(GND)	DR1#	DSKCHG#	MTR1#	DENSL	RDATA#	GND
10	(GND)	WP#	HDSEL#	DIR#	TRK0#	STEP#	GND
9	(GND)	WGATE#	**RXA-**	**GND**	**HSLED**	NC	GND
8	(GND)	**GND**	**RXA+**	**J3VCC**	**CTB**	NC	GND
7	(GND)	**RXB-**	**GND**	**TXB-**	**CTA**	**GND**	GND
6	(GND)	**RXB+**	**GND**	**TXB+**	**GND**	**TXA-**	GND
5	(GND)	NC	MSDAT	SPKR	KBDAT	**TXA+**	GND
4	(GND)	PRST#	MSCLK	**J3VCC**	KBCLK	S1RXD	GND
3	(GND)	S1CTS	S1RTS	S1DSR	S1DCD	S1TXD	GND
2	(GND)	S2RIN	S2DTR	S1RIN	S1DTR	S2RXD	GND
1	(GND)	S2CTS	S2RTS	S2DSR	S2DCD	S2TXD	GND
Pin #	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

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J5 (Keyboard Connector)

J5 is a 6-pin D-shell connector (AMP 749180-1 or equivalent) transitioning the processor board's keyboard signals for rear-panel access. See the "J5 Keyboard Connector Pinout" table below for pin definitions.

Table 9. J5 Keyboard Connector Pinout

Pin#	Function	Pin#	Function
1	KBDAT	4	Vcc (PTC)
2	No Connect	5	KBCLK
3	GND	6	No Connect

J6 (Mouse Port Connector)

J6 is a 6-pin PS/2 mouse port connector (AMP 749180-1 or equivalent). See the "J6 Mouse Port Connector Pinout" table below for pin definitions.

Table 10. J6 Mouse Port Connector

Pin#	Function	Pin#	Function
1	MSDAT	4	VCC (PTC)
2	No Connect	5	MSCLK
3	GND	6	No Connect

J7, J8 (Ethernet A, B Connectors)

J7 (ENET A) and J8 (ENET B) are RJ-45 connectors (Stewart SI-40231) transitioning the processor board's Ethernet signals to the rear panel. Depending on the application's Ethernet requirements (front panel/rear-panel access; HA/non-HA system), configuration of switches on the processor board may be necessary. See the processor board manual for details. See the "J7/J8 Ethernet A/B Connectors Pinout" table for pin definitions.

NOTES:
1. J8 ENET B is not available in a High Availability system.
2. The two LEDs located inside the ZT 4804's RJ-45 connectors are non-functional.

Table 11. J7, J8 (Ethernet A, B Connectors) Pinout

Pin#	Function	Pin#	Function
1	TX+	5	GND
2	TX-	6	RX-
3	RX+	7	GND
4	GND	8	GND

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3.4 Internal Connectors

J9 (EIDE Connector)

J9 is an internal (not on the faceplate) 40-pin male connector (unshrouded 0.025" square posts on 0.1" 2 x 20 grid) providing access to the processor board's secondary EIDE channel. See the “J9 EIDE Connector Pinout” table below for pin definitions.

Table 12. J9 EIDE Connector Pinout

Pin #	Function	Pin #	Function
1	PWRGD	21	SDDRQ
2	GND	22	GND
3	DD7	23	SDIOW#
4	DD8	24	GND
5	DD6	25	SDIOR#
6	DD9	26	GND
7	DD5	27	IORDY
8	DD10	28	10K PULL UP
9	DD4	29	SSDAK#
10	DD11	30	N/C
11	DD3	31	IRQ15
12	DD12	32	ISAIO16#
13	DD2	33	DA1
14	DD13	34	N/C
15	DD1	35	DA0
16	DD14	36	DA2
17	DD0	37	CS1S#
18	DD15	38	CS3S#
19	GND	39	IDELED#
20	N/C	40	GND

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J10 (Floppy Drive Connector)

J10 is an internal (not on the faceplate) 34-pin male connector (unshrouded 0.025" square posts on 0.1" 2 x 17 grid) providing access to the processor board's floppy signals. See the “J10 Floppy Drive Connector Pinout” table below for pin definitions.



Caution: Do not connect the floppy drive directly to system power. Floppy disks in the drive may become corrupted. Power the floppy drive from the host processor board. This causes the floppy drive power and control lines to become active at the same time, thereby maintaining signal integrity. For development purposes floppy power may be sourced from J11.

Table 13. J10 Floppy Drive Connector Pinout

Pin #	Function	Pin #	Function
1	GND	18	DIR#
2	DENSL	19	GND
3	GND	20	STEP#
4	N/C	21	GND
5	GND	22	WDATA#
6	MSEN0	23	GND
7	GND	24	WGATE#
8	INDEX#	25	GND
9	GND	26	TRK0#
10	MTR0#	27	GND
11	GND	28	WP#
12	DR1#	29	GND
13	GND	30	RDATA#
14	DR0#	31	GND
15	GND	32	HDSEL#
16	MTR1#	33	GND
17	GND	34	DSKCHG#

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J11 (Reserved)

J11 is an internal (not on the faceplate) 5-pin male connector (unshrouded 0.025" square posts on a 0.1" 1 x 5 grid) providing access to the ZT 4804 local isolated SMBus signals. VCC and Logic Ground are also provided. Note that VCC may or may not be switched from a host Hot Swap processor board, depending on the backplane used. The VCC pin (pin 5) is fused for 1A DC. See the “J11 Reserved Connector Pinout” table below for pin definitions.

Table 14. J11 Reserved Connector Pinout

Pin	Function
1	Logic Ground
2	SMB Clock
3	SMB Data
4	SMB Alert
5	VCC

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Section

4 Specifications

This section describes the electrical, environmental, and mechanical specifications of the ZT 4804 Rear-Panel I/O Transition Board. It includes connector descriptions and pinouts, as well as illustrations of the board dimensions and connector locations.

4.1 Electrical Specifications

Power Requirements	Minimum	Typical	Maximum
Supply Voltage, VCC	4.75 V	5.00 V	5.25 V
Supply Current, VCC = 5.0 V	0 mA	—	500 mA

Each ZT 4804 relay output offers a normally open and normally closed pole position, with the following maximum contact ratings:

- Rated Resistive Load: 0.4 A @ 125 VAC, 2.0 A @ 30 VDC
- Rated Inductive Load: 0.2 A @ 125 VAC, 1.0 A at 30 VDC
- Operating voltage: 250 VAC, 220 VDC
- Operating current: 3.0 A (AC resistive), 3.0 A (DC resistive)
  1.5 A (AC inductive), 1.5 A (DC inductive)
- Switching capacity: 50 VA, 60 W (resistive)
  25 AV, 30 W (inductive)
- Minimum load: 10 µA at 10 mVDC

Power is supplied to an external keyboard and mouse via J5 and J6, respectively.

4.2 Environmental Specifications

- Operating Temperature: 0º to +65º Celsius
- Storage Temperature: -40º to +85º Celsius
- Relative Humidity: < 95% at 40º Celsius, non-condensing

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4.3 Reliability

- MTBF: 24.9 years at 40º Celsius
- MTTR: 3 min (based on hot-swap board replacement) plus system startup

4.4 Mechanical Specifications

The topics listed below provide the following mechanical specifications:

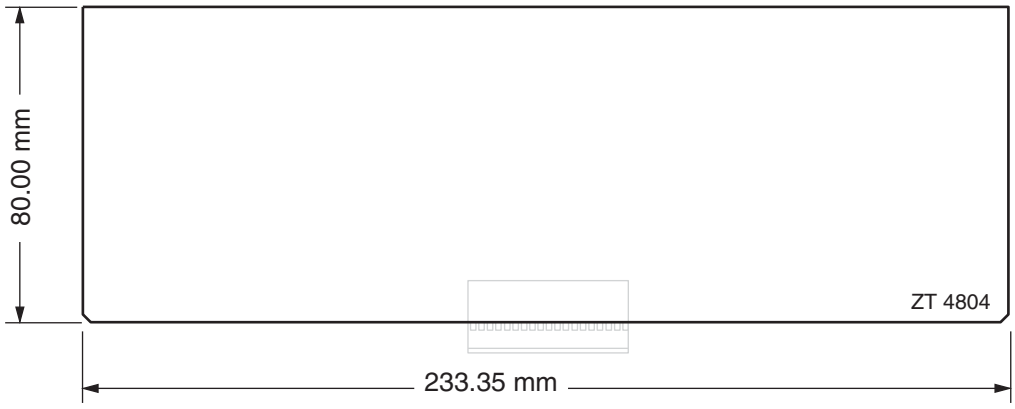
- Board dimensions and weight
- Connectors (including connector locations, descriptions, and pinouts)

Board Dimensions and Weight

Mechanical dimensions for the ZT 4804 are shown in the “Board Dimensions” illustration and outlined below.

- Board Length: 80 mm (3.150 inches)
- Board Width: 233.35 mm (9.187 inches)
- Board Thickness: 1.6 mm (0.063 inches)
- Board Weight: 236 grams (8.00 ounces)

Figure 5. Board Dimensions



Connectors

The ZT 4804 includes several connectors to interface to application-specific devices. A detailed description and pinout for each connector is given in Section 3, “Connectors.”

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Section

5 In Case of Difficulty

If you encounter difficulty in using this Performance Technologies product, you can contact our support personnel in several ways. Please have the product model and serial number handy before contacting Product Support.

Internet

www.pt.com

Email

support@pt.com

Describe your problem in detail. Please include your return email address and telephone number.

FAX

(805) 541-5088

Mark your FAX “Attention: Product Support.” Describe your problem in detail. Please include your return FAX number and telephone number.

Telephone

(805) 541-0488

Request Product Support. Our offices are open between 8:00 am and 5:00 pm Pacific Time, Monday through Friday.

If you are located outside North America, we encourage you to contact the local Performance Technologies distributor or agent for support. Many of our distributors or agents maintain technical support staffs.

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