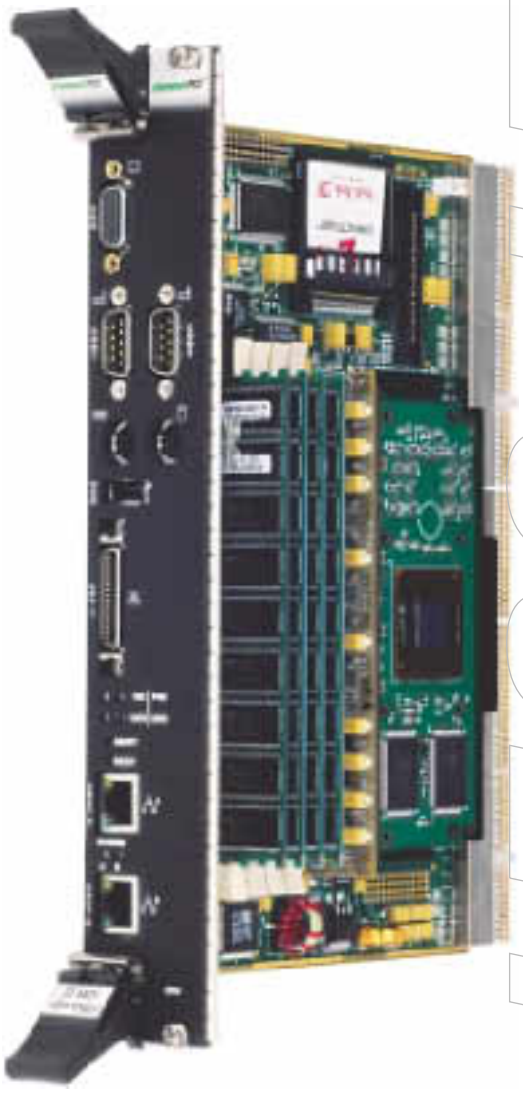
CompactPCI

ZT 5521

CPU Board with Pentium® III Processor



ZT 5521

Hardware Manual

reliable

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TABLES

FIGURES

MANUAL ORGANIZATION

This manual describes the operation and use of the ZT 5521 CPU Board with Pentium® III Processor†. The following summarizes the focus of each chapter in this manual.

Chapter 1, "Introduction," introduces the key features of the ZT 5521 CPU. It includes a product definition, a list of product features, a functional block diagram, and a brief description of each block. This chapter is most useful to those who wish to compare the features of the ZT 5521 against the needs of a specific application.

Chapter 2, "Getting Started," summarizes the information you need to make the ZT 5521 operational and should be read before attempting to use the board. It also describes system requirements for the ZT 5521 CPU.

Chapter 3, "Configuration," describes the switches and cuttable traces on the ZT 5521 CPU. This chapter details factory default settings and provides information allowing you to tailor your board to the needs of specific applications.

Chapter 4, "Enhanced IDE Interface," provides an introduction to the ZT 5521's Enhanced IDE Interface Controller. It covers drive configuration, software device drivers, and the ZT 5521's support for "CompactFlash" IDE disk drives and optional remote drive(s).

Chapter 5, "Watchdog Timer," explains the operation of the ZT 5521's watchdog timer. Sample code is provided to illustrate how the watchdog's functions are used in an application.

Chapter 6, "Flash Memory," discusses on-board flash memory, including the system BIOS EPROM. Recovery from BIOS corruption is also covered in this chapter.

Appendix A, "Specifications," contains the electrical, environmental, and mechanical specifications for the ZT 5521 CPU. It also provides an illustration of connector locations, as well as connector descriptions and pinout tables.

Appendix B, "Reset," explains the ZT 5521's various reset types and reset sources.

Appendix C, "System Registers," provides register descriptions and illustrations, as well as a brief overview of the System registers used to control and monitor a variety of functions on the ZT 5521.

Appendix D, "Thermal Considerations," addresses the special cooling issues associated with the ZT 5521's Slot 1 Pentium processor.

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† The ZT 5521 CPU board also supports the Pentium II processor. Except where noted, the information in this manual applies equally to ZT 5521 CPU boards implementing a Pentium II processor or a Pentium III processor.

Appendix E, "ZT 5521 Vs. ZT 5520 Technical Differences," describes the technical differences between the ZT 5520 and the ZT 5521 CPU boards. It includes information to help existing ZT 5520 customers adapt their applications to the ZT 5521.

Appendix F, "Data Sheet Reference," provides links to data sheets for many of the devices located on the boards in your system.

Appendix G, "Power Supplies And Hot Swap Circuitry," addresses the issue of power supply loading requirements in hot swap systems.

Appendix H, "Agency Approvals," presents UL, CE, and FCC agency approval and certification information.

Appendix I, "Customer Support," offers technical assistance and warranty information, as well as RMA instructions should you need to return your ZT 5521 or optional boards for repair.

1. INTRODUCTION

This chapter provides a brief introduction to the ZT 5521. It includes a product definition, a list of product features, a "Connector Plate" figure, a functional block diagram, and a description of each block. Unpacking, initial board configuration, and other setup information is provided in Chapter 2, "Getting Started."

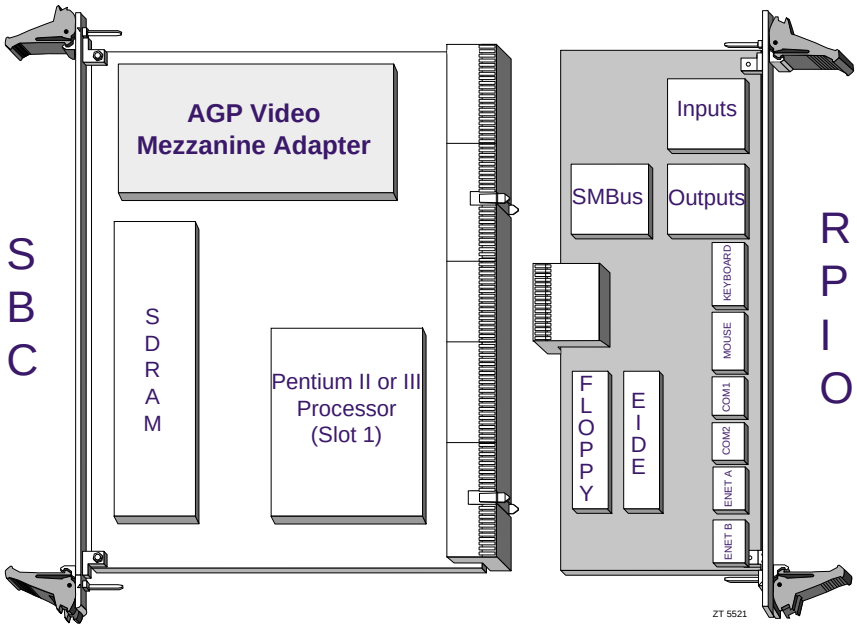
PRODUCT DEFINITION

The ZT 5521 is a 6U CompactPCI™ CPU board featuring the Intel® Slot 1 Pentium® III processor†. The ZT 5521 is designed for high performance communications applications and provides System Master control of the CompactPCI backplane.

The ZT 5521's Pentium III processor provides optimum performance in uniprocessing or multiprocessing systems. The ZT 5521 supports hosting hot swap peripherals in a powered system. The ZT 5521 itself is not Hot Swap capable. The board occupies two CompactPCI slots (8HP) with one Pentium III Processor installed.

As shown in the "CPU with Optional Boards" figure below, the ZT 5521's 114-pin AGP mezzanine connector supports on-board AGP video via the optional ZT 96079 AGP Video Mezzanine Adapter. Additionally, rear-panel access to the ZT 5521's I/O functions is supported via the optional ZT 4804 Rear Panel Transition Board. Refer to Ziatech's *ZT 96079 AGP Video Mezzanine Adapter* hardware manual and to Ziatech's *ZT 4804 Rear-Panel Transition Board* hardware manual for more information.

CPU with Optional Boards



†The ZT 5521 CPU board also supports the Pentium II processor.

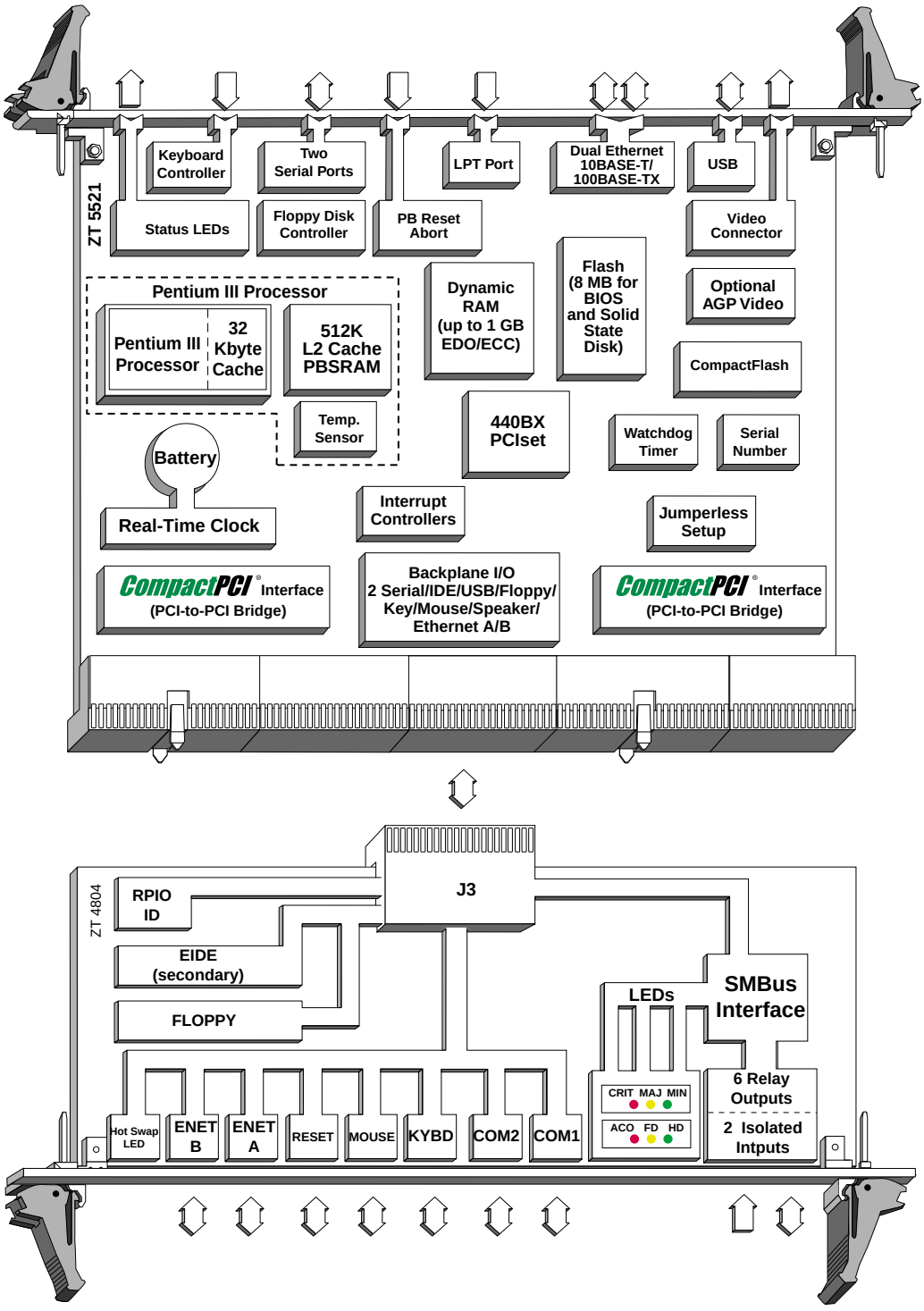
FEATURES

- CompactPCI System Master
- CompactPCI Specification, PICMG 2.0, Version 2.1 compliant
- CompactPCI Hot Swap Specification, PICMG 2.1, Version 1.0 compliant
- Supports Pentium II processors and Pentium III processors
- Occupies two 6U CompactPCI slots
- Supports an optional AGP Video Mezzanine Adapter
- Built-in numeric coprocessor support
- 16 KB of CPU instruction cache
- 16 KB of CPU data cache
- 512 KB pipelined burst L2 cache
- Dual 10/100 Mbit/s Ethernet® interfaces
- Supports 64-bit PCI memory-to-memory transfers
- Four PC100 SDRAM sockets supporting a maximum of 1 GB memory with ECC
- 8 MB of flash memory
- CompactFlash™ memory socket. Flash disk appears as standard “IDE” disk to software
- Standard AT® peripherals include:
  - Two enhanced interrupt controllers (8259)
  - Three counter/timers (one 8254)
  - Real-time clock/CMOS RAM (146818)
  - Two enhanced DMA controllers (8237)
  - 8042 compatible keyboard controller
- IEEE® 1284 printer port (ECP/EPP compatible)
- Two 16C550 RS-232 serial ports
- Dual stage watchdog timer
- Speaker interface
- Push-button reset
- Software programmable LEDs
- DC power monitors (3.3 V and 5 V)

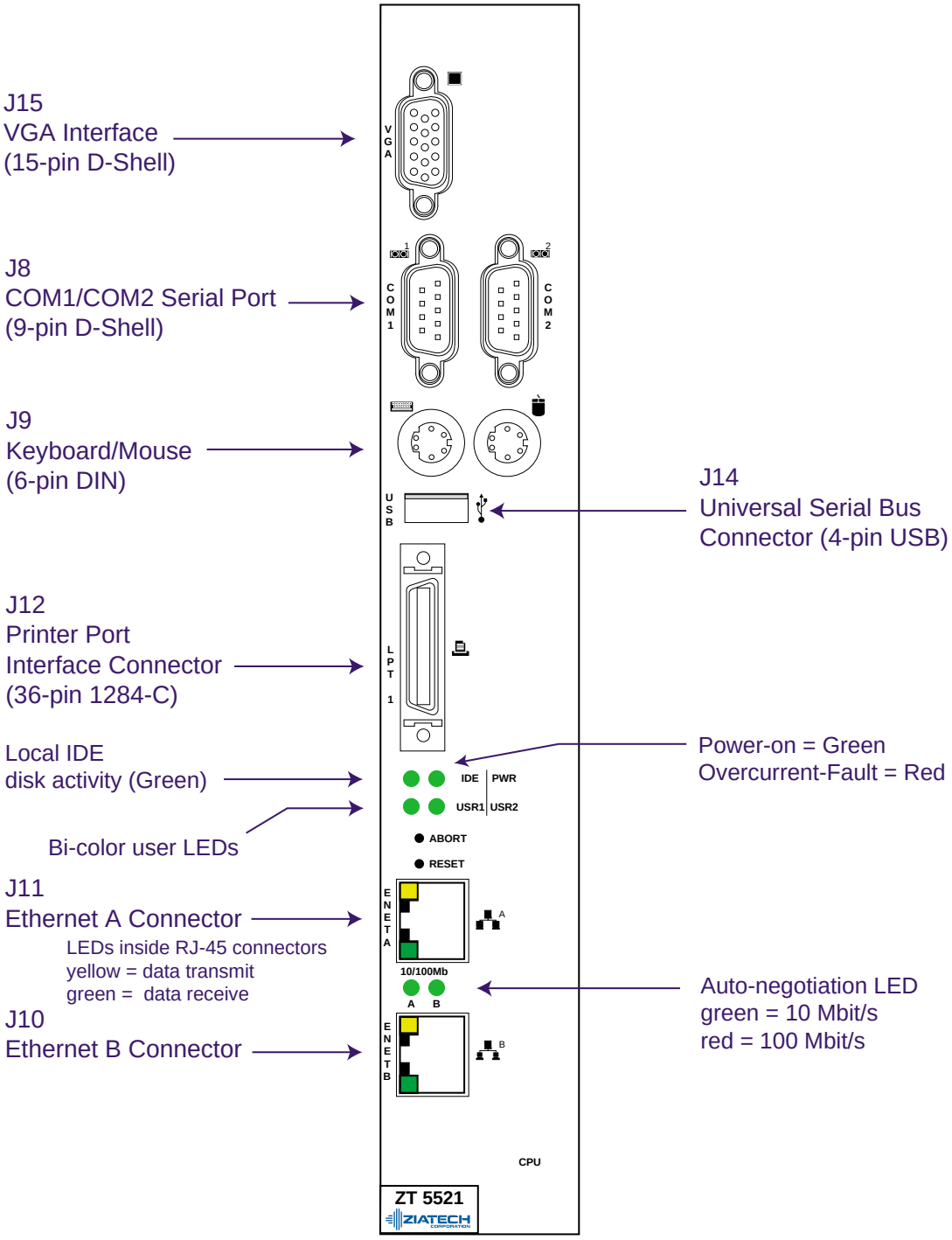
FUNCTIONAL BLOCKS

Below is a functional block diagram of the ZT 5521. The following topics provide overviews of the functional blocks.

Functional Block Diagram



Connector Plate



CompactPCI Bus Interface

The ZT 5521 CPU operates in a 6U CompactPCI system. The CompactPCI standard is electrically identical to the PCI local bus standard and has been enhanced to support rugged industrial environments and more slots. Additionally, when used in a Hot Swap compliant backplane and in accordance with the *CompactPCI Hot Swap Specification, PICMG 2.1, Version 1.0*, the ZT 5521 supports hosting hot swap peripherals in a powered system. The ZT 5521 can also function in a standard (non-Hot Swap) CompactPCI system. The ZT 5521 itself is not hot swappable.

Rear-Panel I/O

The ZT 5521 transitions many I/O signals out the rear of the board on J3 to a rear-panel transition board such as the ZT 4804. Refer to your rear-panel transition board hardware manual for more information.

I/O routed through each connector is listed below:

- Speaker
- Floppy
- Keyboard
- PS/2 mouse
- USB Port (Port 1)
- IDE secondary channel
- Push button NMI (abort)
- Push button System Reset
- Ethernet Channels A and B
- Two serial ports (COM1 and COM2)
- Rear-Panel Transition board identification signal

PCI-to-PCI Bridge

The ZT 5521 features two Intel 21154 PCI-to-PCI bridges to support both the J1/J2 and J4/J5 CompactPCI buses. Each bridge provides the isolation, arbitration, and clocks for seven PCI peripheral cards, meaning support for up to 14 CompactPCI peripherals (all bus masters) without the need for an external bridge board.

Special features of the 21154 include:

- Support for independent primary and secondary PCI clocks
- 64-bit PCI operation
- 33 MHz PCI bus operation

The topic "PCI to PCI Bridge" in Appendix F, “Data Sheet Reference,” contains a link to the data sheet for this device.

Slot 1 Pentium III Processor

The ZT 5521 features the Intel Slot 1 Pentium III processor† with Single Edge Contact Cartridge 2 (S.E.C.C.2) package technology. The Pentium III processor is a small, highly integrated assembly containing an Intel Pentium processor and its immediate system-level support. The Pentium III processor includes 32 KB of code and data cache (L1 cache), a secondary 512 KB cache (L2 cache), and the core logic required to bridge the processor to the standard system buses. The module interfaces electrically to its host system bus via the host controller GTL interface, operating at 100 MHz.

The topic "Pentium III Processor" in Appendix F, “Data Sheet Reference,” contains a link to the data sheet for the processor.

AGP Mezzanine

The ZT 5521 provides a 114-pin AGP mezzanine connector for interfacing to Ziatech’s optional ZT 96079 AGP Video Mezzanine Adapter. The ZT 96079 utilizes the Accelerated Graphics Port (AGP) Interface to give exceptional video performance targeted at 3D or other high bandwidth graphical display applications. The AGP bus supports 64 bits of data and runs at a speed of 66 MHz, giving it a theoretical bandwidth of 266 MB in 1x AGP mode, or 533 MB in 2x AGP mode (two transfers per clock cycle).

Refer to Ziatech's *ZT 96079 AGP Video Mezzanine Adapter* hardware manual for more information about the ZT 96079 AGP Video Mezzanine Adapter.

Dual Ethernet Interfaces

The ZT 5521’s Ethernet® interfaces are provided through two industry standard Intel 21143 PCI-Ethernet Bridges. The Physical Interface (PHY) is provided by the Intel LXT970 Dual-Speed Fast Ethernet Transceiver. Two RJ-45 connectors are used to bring both Ethernet channels to the front panel. Both 10 Mbit/s and 100 Mbit/s Ethernet protocols are supported. LEDs indicate the status of each Ethernet channel.

† The ZT 5521 CPU board also supports the Pentium II processor.

Both Ethernet channels are available through the rear-panel via the optional ZT 4804 Rear-Panel Transition Board. Each channel is independently configurable for front or rear operation via switches on the ZT 5521.

The section "Ethernet" in Appendix F, “Data Sheet Reference,” contains links to the data sheets for the ZT 5521's Ethernet devices.

Memory and I/O Addressing

The ZT 5521 provides four 168-pin connectors for local memory. The connectors support PC100 128 MB or 256 MB SDRAM modules. The SDRAM is implemented as Error Correcting Coded (ECC), which will correct single bit errors (97% of all DRAM errors are single bit errors) and report multiple bit errors to the operating system.

In addition to SDRAM, the ZT 5521 has 8 MB of on-board flash memory. The flash memory contains the system BIOS, and the remainder may be allocated as solid state drive. If more flash memory is required, the ZT 5521 supports expansion through the use of a CompactFlash™ memory card. A variety of CompactFlash card sizes are currently available. The flash memory market is continuously evolving and larger size drives will be supported when they are available. The ZT 5521 addresses the CompactFlash memory card as an IDE disk. The CompactFlash format works with most operating systems without the need for special drivers.

See the “Memory Configuration” and “I/O Configuration” topics in Chapter 2 for more information. See Chapter 4, "Enhanced IDE Interface," for more on the ZT 5521's CompactFlash support.

Serial I/O

The ZT 5521 provides two 16C550 PC-compatible serial ports:

Front Panel: COM1 and COM2

Rear Panel: COM1 and COM2 via J3 to the optional ZT 4804 Rear-Panel Transition Board

The serial ports are implemented with a 5 V charge pump technology to eliminate the need for a ±12 V supply. Both serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115.2 Kbaud. The serial ports are configured as DTE.

The ZT 5521’s serial controller resides in the National Semiconductor® PC87309 SuperI/O® device. The topic "SuperI/O" in Appendix F, “Data Sheet Reference,” provides a link to the data sheet for this device.

Interrupts

Two enhanced, 8259-style interrupt controllers provide the ZT 5521 with a total of 15 interrupt inputs. Interrupt controller features include support for:

- Level-triggered and edge-triggered inputs
- Individual input masking
- Fixed and rotating priorities

Interrupt sources include:

- Counter/Timers
- Serial I/O
- Real-Time Clock
- Keyboard
- Printer Port
- Floppy
- IDE
- Digital
- CompactPCI
- On-board

Enhanced capabilities include the ability to configure each interrupt level for active high-going edge or active low-level inputs.

The ZT 5521's interrupt controllers reside in the Intel 82371EB (PIIX4E) device. The topic "PIIX4" in Appendix F, "Data Sheet Reference," provides a link to the data sheet for this device.

Counter/Timers

Three 8254-style counter/timers are included on the ZT 5521 as defined for the PC/AT®. Operating modes supported by the counter/timers include interrupt on count, frequency divider, square wave generator, software triggered, hardware triggered, and one shot.

The ZT 5521's interrupt controllers reside in the Intel 82371EB (PIIX4E) device. The topic "PIIX4" in Appendix F, "Data Sheet Reference," provides a link to the data sheet for this device.

DMA

Two enhanced, 8237-style DMA controllers are provided on the ZT 5521 for use by the on-board peripherals. DMA channel 2 is assigned to the optional floppy drive and DMA channels 1 or 3 are assigned to the parallel printer port for ECP mode support

The ZT 5521's interrupt controllers reside in the Intel 82371EB (PIIX4E) device. The topic "PIIX4" in Appendix F, "Data Sheet Reference," provides a link to the data sheet for this device.

Real-Time Clock

The real-time clock performs timekeeping functions and includes 256 bytes of general-purpose, battery-backed, CMOS RAM. Timekeeping features include an alarm function, a maskable periodic interrupt, and a 100-year calendar. The system BIOS uses a portion of this RAM for BIOS setup information. The system BIOS is also Year 2000 Compliant.

The ZT 5521's interrupt controllers reside in the Intel 82371EB (PIIX4E) device. The topic "PIIX4" in Appendix F, “Data Sheet Reference,” provides a link to the data sheet for this device.

Hot Swap

The ZT 5521 complies with the *CompactPCI Hot Swap Specification, PICMG 2.1, Version 1.0* for System Masters, supporting hosting of hot swap peripherals in a powered system. The ZT 5521 itself is not Hot Swappable.

Power Ramp Circuitry

The ZT 5521 features a hot swap controller with power ramp circuitry to allow the board's voltages to be ramped in a controlled fashion. The power ramp circuitry eliminates any large voltage or current spikes caused by removing or inserting hot swappable boards while the system is still under power. This controlled ramping is a requirement of the *CompactPCI Hot Swap Specification, PICMG 2.1, Version 1.0*.

The ZT 5521's hot swap controller unconditionally resets the board when it detects that the 3.3 V, 5 V, and 12 V supplies are below an acceptable operating limit. These limits are defined as 4.75 V (5 V supply), 3.0 V (3.3 V supply), and 10.0 V (+12 V supply). Fault current sensing is also provided. If a board fault (short circuit) or over-current condition is detected, the hot swap controller automatically removes power from the ZT 5521 components and the “Fault/Power” indicator LED turns red.

Reset

The ZT 5521 provides the following reset types:

- Backend Power Down
- General Reset
- Hard Reset
- Soft Reset
- NMI

See Appendix B, “Reset,” for more information.

Two-Stage Watchdog Timer

The watchdog timer optionally monitors system operation and is programmable for one of eight different timeout periods (from 0.25 seconds to 256 seconds). It is a two-stage watchdog, meaning that it can be enabled to produce a non-maskable interrupt (NMI) before it generates a System Reset.

Failure to strobe the watchdog timer within the programmed time period may result in an NMI, a System Reset, or both. A register bit is set if the watchdog timer caused the reset event. This watchdog timer register is only cleared on power-up, enabling system software to take appropriate action on reboot. See Chapter 5, "Watchdog Timer," for more information.

IEEE-1284 Parallel Port/Printer Interface

The ZT 5521 includes an IEEE-1284 compatible parallel port for connection to a printer or other parallel port devices such as software keys required by many application packages. The parallel port is ECP/EPP compatible.

The printer interface is available on the connector plate through connector J12 as LPT. The mode (Normal, Extended, EPP, or ECP) for the printer interface is selectable through the BIOS SETUP Utility (see the section "BIOS Configuration Overview" in Chapter 2).

The ZT 5521's parallel port resides in the National Semiconductor PC87309 SuperI/O device. The topic "SuperI/O" in Appendix F, "Data Sheet Reference," provides a link to the data sheet for this device.

Universal Serial Bus (USB)

The emerging Universal Serial Bus (USB) provides a common interface to slower-speed peripherals. In the future, functions such as keyboard, serial ports, printer port, and mouse ports will be consolidated into USB, greatly simplifying the cabling requirements of future computers. The ZT 5521 provides a front-panel USB port (J14, Port 0). A second USB port (Port 1) is available through the rear-panel I/O connector J3.

The ZT 5521's USB reside in the Intel 82371EB (PIIX4E) device. The topic "PIIX4" in Appendix F, "Data Sheet Reference," provides a link to the data sheet for this device.

Speaker Interface

For external speaker interfacing, the ZT 5521 supports an external AT-compatible speaker through an on-board, 2-pin connector. The speaker outputs are also available through the rear-panel I/O connector J3.

Enhanced IDE Controller/Floppy Controller

The ZT 5521 includes a Floppy Disk Controller (PC87309) and an Enhanced IDE Controller (PIIX4E). These devices support optional internal or external floppy disks and EIDE drives. Floppy signals are available only through the rear-panel I/O connector J3; EIDE signals are available through the CompactFlash connector J22 (primary channel) and the rear-panel I/O connector J3 (secondary channel).

See Chapter 4, "Enhanced IDE Interface," for more about the ZT 5521's EIDE support. Appendix F, "Data Sheet Reference," provides links to the data sheets for the EIDE (PIIX4) and floppy controllers (SuperI/O).

Keyboard Controller

The ZT 5521 includes an on-board PC/AT® keyboard controller, available through front-panel connector J12A. The keyboard signals are also available through the rear-panel I/O connector J3.

The ZT 5521's keyboard controller resides in the National Semiconductor® PC87309 SuperI/O® device. The topic "SuperI/O" in Appendix F, "Data Sheet Reference," provides a link to the data sheet for this device.

Mouse Controller

The ZT 5521 includes an on-board PC/AT mouse controller, available through front-panel connector J12B. The mouse signals are also available through the rear-panel I/O connector J3.

The ZT 5521's mouse port resides in the National Semiconductor PC87309 SuperI/O device. The topic "SuperI/O" in Appendix F, "Data Sheet Reference," provides a link to the data sheet for this device.

LED Indicators

Several LEDs are located on the ZT 5521 connector plate for the following features:

- Ethernet Channels A and B:

  Status LEDs, one per channel: green = 10Base-T; red = 100Base-T
  RJ-45 LEDs, two per connector: green = data receive; yellow = data transmit

- **IDE:** (Local EIDE disk activity) green = active; off = not active
- **USR1 USR2:** Bi-color user LEDs
- **PWR** (Power)**:** green = power on; red = overcurrent fault

SOFTWARE

The ZT 5521 includes the Ziatech Embedded BIOS loaded in on-board flash. The Year 2000-compliant BIOS is user-configurable to boot an operating system residing in local flash memory, from a fixed or floppy drive, or over a network.

The ZT 5521 is compatible with all major PC operating systems. Ziatech provides enhanced support, including additional drivers for Ziatech peripherals and flash drives, for the following operating systems:

Windows NT

Ziatech offers two CompactPCI Windows NT Toolkits. Both include a BIOS recovery CD with flash utilities and a development kit manual. The ZT 94081 includes Windows NT 4.0 *Workstation* OS recovery CD. The ZT 94084 includes Windows NT 4.0 *Server* OS recovery CD.

Linux

The ZT 5521 can be purchased loaded with Hard Hat™ Linux, an embedded and fully supported version of Linux from MontaVista Software. Ziatech's latest software device drivers for Linux multiprocessing software can be downloaded from www.compactnet.com, the web site for Ziatech's CompactNET multiprocessing technology. The ZT 94083 includes MontaVista Hard Hat Linux OS recovery CD, a BIOS recovery CD with flash utilities, and a development kit manual.

VxWorks

Ziatech offers a comprehensive board support package for VxWorks (ZT 94078A), which streamlines the implementation of VxWorks on the ZT 5521. ZT 94078A CompactPCI VxWorks-Tornado II BSP includes the VxWorks BSP on CD, a BIOS recovery CD with flash utilities, and a development kit manual. The VxWorks OS must be purchased directly from WindRiver.

Other Software

Windows 2000 server support for ZT 5521 will be available in the future. Contact Ziatech for information on other operating systems.

2. GETTING STARTED

This chapter summarizes the information you need to make the ZT 5521 operational and should be read before attempting to use the board.

Customers upgrading their systems from the ZT 5520 CPU to the ZT 5521 CPU and adapting their applications to the newer board should read Appendix E, "ZT 5521 Vs. ZT 5520 Technical Differences" before attempting to use the ZT 5521.

UNPACKING

Please check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Ziatech for an insurance settlement. Retain the shipping carton and packing material for inspection by the carrier. Save the anti-static bag for storing or returning the ZT 5521.

Do not return any product to Ziatech without a Return Material Authorization (RMA) Number. See Appendix I, "Customer Support", for an explanation of the procedure for obtaining an RMA number from Ziatech.

Caution: Like all equipment utilizing MOS devices, the ZT 5521 must be protected from static discharge. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the ZT 5521 to handle the board.

SYSTEM REQUIREMENTS

The following ZT 5521 system requirements are briefly described below:

- BIOS version
- Backplane requirements
- Electrical and environmental requirements

BIOS Version

For proper operation, the ZT 5521 must run the Ziatech Embedded BIOS version 5.00 or greater.

Backplane Connectivity

The ZT 5521 is designed for use in a backplane providing a CompactPCI bus on connectors J1/J2 and J4/J5. To support the optional ZT 4804 Rear-Panel Transition Board, the backplane's rear panel J3 connector must be available and have through-pins to the ZT 5521's J3 connector.

See the "Connectors" topic in Appendix A for complete connector descriptions and pinout tables.

Electrical and Environmental

The ZT 5521 requires a maximum of +5 VDC ± 5% @ 10 A, +3.3 VDC ± 5% @ 7 A and +12 VDC ± 5% @ 500 mA. Electrical specifications are covered in more detail in Appendix A, "Specifications."

Ziatech recommends vertical mounting. The ZT 5521 is supplied with an integrated processor heatsink. The heatsink requires a minimum of 250 LFM to allow operation between 0º and approximately 45º C ambient.

Maintain these parameters to avoid improper operation and possible damage to the board. See Appendix D, "Thermal Considerations," and Appendix A, "Specifications," for more about the ZT 5521's thermal requirements.

Warning: Operating the ZT 5521 without adequate airflow may damage the CPU module.

MEMORY CONFIGURATION

The ZT 5521 addresses up to 4 GB of memory. The address space is divided between memory local to the board and memory located on the CompactPCI bus (or buses). Any memory not reserved or occupied by a local memory device (DRAM/flash) is available to the CompactPCI bus.

The ZT 5521 is populated with several memory devices. Local SDRAM is contained in four industry-standard, 168-pin, DIMM sockets (J13, J15, J18, and J20) supporting up to 1 GB (PC100) of SDRAM.

In addition to SDRAM, the ZT 5521 has 8 MB of on-board flash memory. The flash memory contains the system BIOS, and the remainder may be allocated as solid state drive. If more flash memory is required, the ZT 5521 supports expansion through the use of a CompactFlash memory card. The ZT 5521 addresses the CompactFlash memory card as an IDE disk. The CompactFlash format works with most operating systems without the need for special drivers. See Chapter 4, "Enhanced IDE Interface," for more on the ZT 5521's CompactFlash implementation.

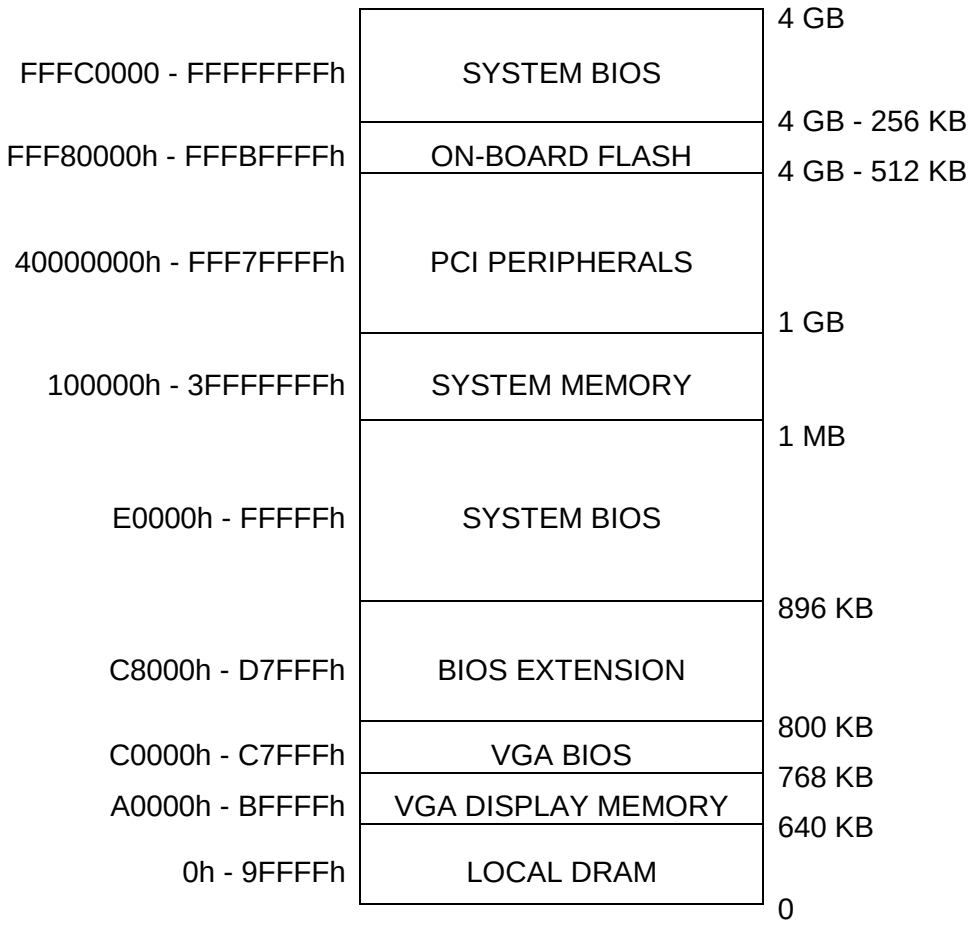
The "Memory Address Map Example" illustration shows example memory addressing for the ZT 5521.

I/O CONFIGURATION

The ZT 5521 addresses up to 64 KB of I/O using a 16-bit I/O address. The address space is divided between I/O local to the board and I/O on the CompactPCI bus. Any I/O space not occupied by a local I/O device is available for the CompactPCI bus.

The ZT 5521 is populated with many of the most commonly used I/O peripheral devices for industrial control and computing applications. The I/O address location for each of the peripherals is shown in the "I/O Address Map" illustration.

Memory Address Map Example



I/O Address Map

*ISA Peripherals decode 11 Bits of address (A0 - A10). Therefore, ISA Peripherals will Alias throughout the 16-bit I/O space at the following ranges:

x100-x3FFh
x500-x7FFh
x900-xBFFh
xD00-xFFFh

PCI devices can fully utilize the address space from D00 - FFFFh, since subtractive decoding is used for the onboard ISA devices.

64 K	D00 - FFFFh	PCI*
	CF8 - CFFh	PCI Config/RST Control
	780 - CF7h	PCI Reserved
	778 - 77Fh	LPT ECP Registers
	400 - 777h	RESERVED
1 K	3F8 - 3FFh	COM1
	3F0 - 3F7h	Floppy / IDE Registers
	3E0 - 3EFh	Reserved
	3B0 - 3DFh	VGA Registers
	380 - 3AFh	Reserved
	378 - 37Fh	LPT
	300 - 377h	Reserved
768	2F8 - 2FFh	COM2
	200 - 2F7h	Reserved
512	1F8 - 1FFh	Reserved
	1F0 - 1F7h	Primary IDE Registers
	178h - 1DFh	Reserved
	170h - 177h	Secondary IDE Registers
	100 - 16Fh	Reserved
256	F0 - FFh	Coprocessor
	E0 - EFh	Digital I/O
	C0 - DFh	On-board Slave DMA Controller
	B4 - BFh	Reserved
	B2 - B3h	APM Registers
	B0 - B1h	Reserved
	A0 - AFh	On-board Slave Interrupt Controller
	93 - 9Fh	Reserved
	92h	Fast RESET and Gate A20
	90 - 91h	Reserved
	81 - 8Fh	On-board DMA Page Registers
	80h	Diagnostic Port
	79h	ZT 5521 System Register 2 (Watchdog Timer CSR)
	78h	ZT 5521 System Register 1
	70 - 77h	On-board Real-Time Clock
	60 - 6Fh	Keyboard and System Ports
	50 - 5Fh	Reserved
	40 - 4Fh	On-board Timer/Counters
	30 - 3Fh	Reserved
	2E - 2Fh	87309 SuperI/O Configuration
	22 - 2Dh	Reserved
	20 - 21h	On-board master Interrupt Controller
0	0 - 1Fh	On-board Master DMA Controller

CONNECTIVITY

The boards in your system provide several connectors for interfacing to application-specific devices. Refer to the topics listed below for complete connector descriptions and pinouts.

- "Connectors" in Appendix A, "Specifications."
- "Connectors" in Ziatech's *ZT 4804 Rear-Panel Transition Board* hardware manual, in Chapter 3, "Specifications."
- "ZT 96079 Connectors" in Ziatech's *ZT 96079 AGP Video Mezzanine Adapter* hardware manual, in Chapter 2, "Specifications."

LPT1 Signaling

The ZT 5521 CPU does not direct LPT1 signals out the J3 Rear-Panel I/O connector. Therefore, if your system includes a ZT 5980 System Utility Board and/or a ZT 4800 Rear-panel I/O board, be aware that the LPT1 interfaces on these boards will not work with the ZT 5521 CPU, and hardware that may be connected to these interfaces can be damaged in a ZT 5521 implementation.

Refer to the topic "LPT1 Signaling" in Appendix E, "ZT 5521 Vs. ZT 5520 Technical Differences" for more about the ZT 5521's compatibility with ZT 5980 and ZT 4800.

Warning: ZT 5521 users should not connect hardware to the ZT 5980 or ZT 4800 LPT1 interfaces!

SWITCHES AND CUTTABLE TRACES

The ZT 5521 provides switch and cuttable trace configuration options for features that cannot be provided through the BIOS Setup Utility (discussed in the section "BIOS Configuration Overview" in this chapter). Refer to the following topics for location figures and descriptions: "Switch Options and Locations" and "Cuttable Trace Options And Locations" in Chapter 3.

REMOVING MEZZANINE BOARDS

Your system may implement a Ziatech mezzanine board (such as the ZT 97074 AGP Video Adapter). Mechanical connection of mezzanine boards is reinforced by metal or nylon stand-offs screwed through mounting holes in each board.

Caution: If it is necessary to disconnect a mezzanine card, Ziatech recommends removing only the screw attaching the card to the stand-off. If it is necessary to remove the stand-off from the CPU, be aware that on some CPUs washers may be located between the PCB and the stand-off. Be sure to retain and re-install these washers to their original position if they are removed for any reason.

Care should also be taken when installing and removing cards to prevent premature wear or accidental bending of pins and receptacles. When removing a mezzanine card, try to disengage the pins evenly across the length of the connector instead of prying only from one side. It may be helpful to gently wiggle the mezzanine card from side-to-side when removing it.

Warning: To avoid damage to the CPU and the mezzanine card, perform the installation or removal at a static-free workstation.

BIOS CONFIGURATION OVERVIEW

This topic presents a brief introduction to the Ziatech Embedded BIOS. For more detailed information about the BIOS and other utilities, see the *Ziatech Embedded BIOS* software manual.

The Ziatech Embedded BIOS has many separately configurable features. These features are selected by running the built-in Setup Utility.

Setup is a utility you use to configure your system. The system configuration settings are saved in a portion of the battery-backed RAM in the real-time clock device and are used by the BIOS to initialize the system at boot up or reset. The configuration is protected by a checksum word for system integrity.

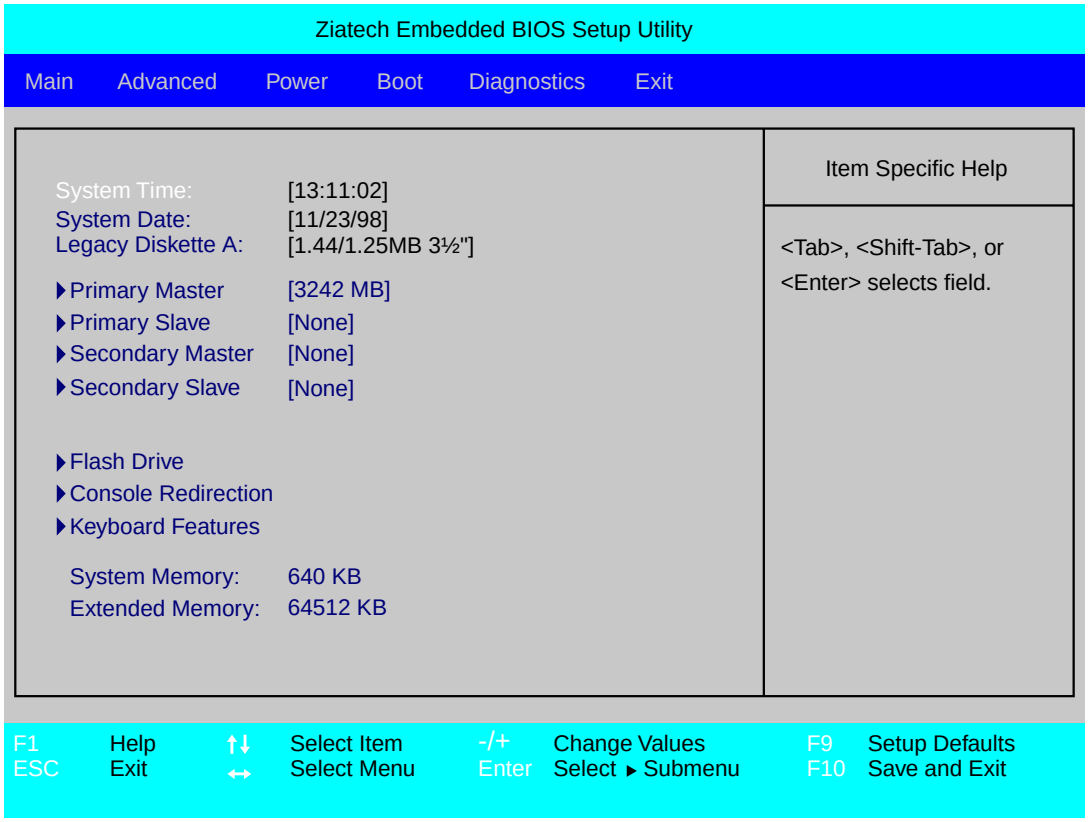
To access the Setup Utility, press the “F2” key during the system RAM check when the system is booting up. When Setup runs, an interactive configuration screen displays. See the illustration “Setup Screen“ for an example.

Setup parameters are divided into different categories. The available categories are listed in a menu across the top of the Setup screen. The parameters within the highlighted (current) category are listed in the main (left) portion of the Setup screen. Context sensitive help is displayed in the right portion of the screen for each parameter. A legend of keys is listed at the bottom of the Setup screen.

Use the left and right arrow keys to select a category from the menu. Use the up and down arrow keys to select a parameter in the main portion of the screen. Use the + or – keys to change the value of a parameter.

Items in the main portion of the screen that have a triangular mark to their left are submenus. To display a submenu, use the up and down arrow keys to highlight the submenu and then press the “Enter” key.

Setup Screen



IDENTIFYING MEDIA OPTIONS

The “Media Options” table below identifies the media options that may be available depending on the hardware in your system.

Media Options

Media	Device Locations	Cable Interfaces
On-board flash device	ZT 5521 CPU — a portion of this 8 MB device may be available as solid state drive, used to contain user programs and data.	N/A
IDE devices		
Hard Drive/ or CD-ROM	• Peripheral board (such as the ZT 5980) • Media bay (if applicable) • External to the enclosure	The ZT 4804 RPIO board provides an internal 40-pin floppy cable interface (J9) to the CPU’s secondary IDE channel.
CompactFlash †	• ZT 5521 CPU — J22, 50-pin, Primary	N/A
Floppy devices	• Peripheral board (such as the ZT 5980) • Media bay (if applicable) • External to the enclosure	The ZT 4804 RPIO board provides an internal 34-pin floppy cable interface (J10).

OPERATING SYSTEM INSTALLATION

For more detailed information about your operating system, refer to the documentation provided by the operating system vendor.

1. Install peripheral devices. CompactPCI devices are automatically configured by the BIOS during the boot sequence.

2. Most operating systems require initial installation on a hard drive from a floppy or CD-ROM drive. These devices should be configured, installed, and tested with the supplied drivers before attempting to load the new operating system.

3. Read the release notes and installation documentation provided by the operating system vendor. Be sure to read any “README” files or documents provided on the

† Configuration of switch SW3-2 and cuttable trace CT42 may be required for proper CompactFlash operation.

distribution disks, as these typically note documentation discrepancies or compatibility problems.

4. Select the appropriate boot device order in the SETUP boot menu depending on the OS installation media that is used. For example, if the OS includes a bootable installation floppy, select "Removable Media" as the first boot device and reboot the system with the installation floppy installed in the floppy drive.

   Note: If the installation requires a non-bootable CD-ROM, it is necessary to boot an OS with the proper CD-ROM drivers in order to access the CD-ROM drive.

5. Proceed with the OS installation as directed, being sure to select appropriate device types if prompted. Refer to the appropriate hardware manuals for specific device types and compatibility modes of Ziatech products.

6. When installation is complete, reboot the system and set the boot device order in the SETUP boot menu appropriately.

RE-INSTALLING WINDOWS NT

Note: This step is unnecessary for BIOS versions 5.10 or greater.

ZT 5521 boards ordered with Windows NT are shipped with the operating system partially pre-installed. If for some reason you need to reinstall Windows NT on the ZT 5521 CPU, be aware that the board may hang during the installation process after the board reboots. The problem occurs because the ZT 5521 CPU, though it is a single processor board, is designed with a Multi-Processor Specification (MPS) architecture. Windows NT detects the board's MPS hardware and MPS table in the BIOS and tries to install the Symmetric Multiprocessing (SMP) Hardware Abstraction Layer (HAL).

Fixing this problem involves pausing the Windows NT installation process after creating the three "Windows NT Workstation Boot Disks" floppies and then modifying some lines in the Txtsetup.sif file on disk #1. These modifications cause the standard ISA/EISA HAL to be loaded instead of the SMP HAL.

Perform the steps below:†

1. From a command prompt, change directories to the I386 directory on the Windows NT CD-ROM.

2. Enter the following command on the command line to create the three "Windows NT Workstation Boot Disks" floppies:

   ```
   WINNT /OX
   ```

† This solution is a modified version of one found in the *Windows NT 4.0 Setup Troubleshooting Guide* available on Microsoft's web site at http://support.microsoft.com/support/kb/articles/q126/6/90.asp.

The **/OX** switch pauses the installation process after creating the disks.

3. Disk #1 is the last disk created. On this disk, edit the **Txtsetup.sif** file as follows:

   In the **[HAL]** section, change the following line:

   ```
   mps_up  = halapic.dll ,2,hal.dll
   ```

   to:

   ```
   mps_up  = hal.dll  ,2,hal.dll
   ```

   In the [**HAL.LOAD]** section, change the following line:

   ```
   mps_up  = halapic.dll
   ```

   to:

   ```
   mps_up  = hal486c.dll
   ```

   In the **[COMPUTER]** section, change the following line:

   ```
   mps_up  = "MPS Uniprocessor PC",files.none
   ```

   to:

   ```
   mps_up  = "Standard PC",files.none
   ```

PROGRAMMING THE LEDS

The ZT 5521 includes two user-controlled bi-color (red/green) Light-Emitting Diodes (LEDs) located on the front panel. The user LEDs are software programmable through bits 0-3 of System Register 7 (Port E5h). The LEDs are turned off after a power cycle or a reset.

As shown below, two bits each are used to control the state of User LEDs 1 and 2. Since bi-color LEDs are used, there are three states for each LED: green, red, and off.

	S T A T E			
User LED 1	**Red**	**Green**	**Off**	**Off**
Bit 2	0	1	1	0
Bit 3	1	1	0	0
User LED 2				
Bit 0	0	1	1	0
Bit 1	1	1	0	0

The LED bits are in the same register as other functions. It is important not to change the state of other bits in this register when modifying the User LED status. The following code demonstrates the mechanism for modifying the bits for User LED 2:

```
; set USER LED 2 ON (GREEN)
cli                         ; clear interrupts
in    al, E5h               ; read current state
and   al, FCh               ; preserve other register bits
or    al, 03h               ; set USER LED 2 (GREEN and enabled)
out   E5h, al               ; output new value for register
sti                         ; re-enable interrupts
; set USER LED 2 ON (RED)
cli                         ; clear interrupts
in    al, E5h               ; read current state
and   al, FCh               ; preserve other register bits
or    al, 02h               ; set USER LED 2 (RED and enabled)
out   E5h, al               ; output new value for register
sti                         ; re-enable interrupts
; set LED OFF
cli                         ; clear interrupts
in   al, E5h                ; read current state
and   al, FCh               ; set bit 1 to turn off LED
out  E5h, al                ; output new value for register
sti                         ; re-enable interrupts
```

3. CONFIGURATION

The ZT 5521 includes several options that tailor the operation of the board to requirements of specific applications. Most of the options are selected through the BIOS Setup mechanism (discussed in the topic "BIOS Configuration Overview" in Chapter 2). Some options cannot be software controlled and are configured with switches or cuttable traces. Switch options are made by closing or opening the desired switch. Cuttable trace options are made by installing and removing surface mount 0 Ω resistors.

This chapter details the ZT 5521's switch and cuttable traces options. Illustrations showing the locations of switches and cuttable traces are also included.

SWITCH OPTIONS AND LOCATIONS

The ZT 5521 contains four banks of switches located on the solder side of the board (SW1-SW4). S1 and S2 are push-button switches located on the connector plate.

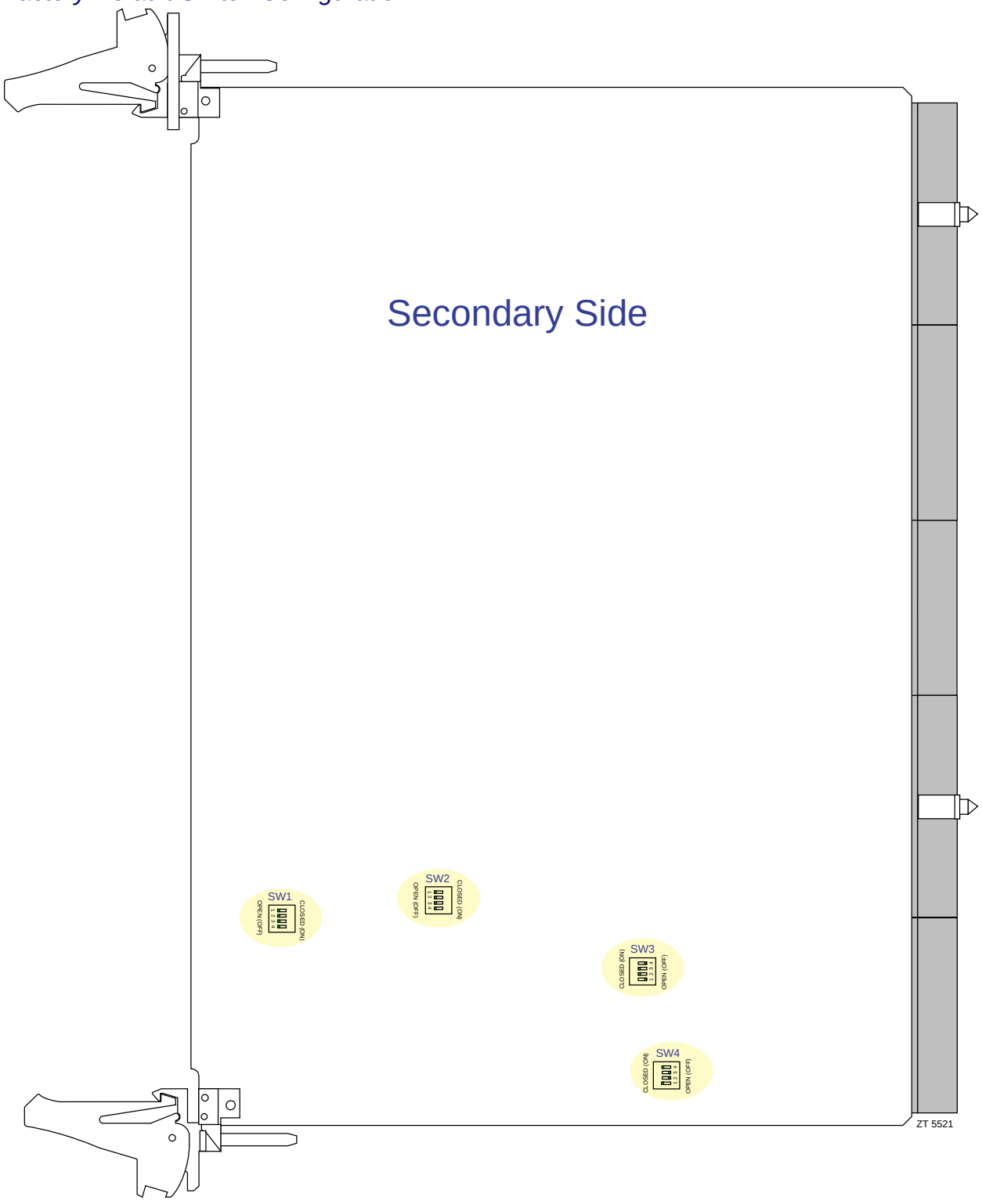
The "Factory Default Switch Configuration" figure shows the ZT 5521's factory default switch settings. The "Customer Switch Configuration" illustration provides a blank switch layout; print this figure and use it to document your switch configuration if it differs from the factory default. This will allow you to restore the configuration if it is changed for any reason.

The "Switch Cross-Reference" table below divides the switch options into functional groups.

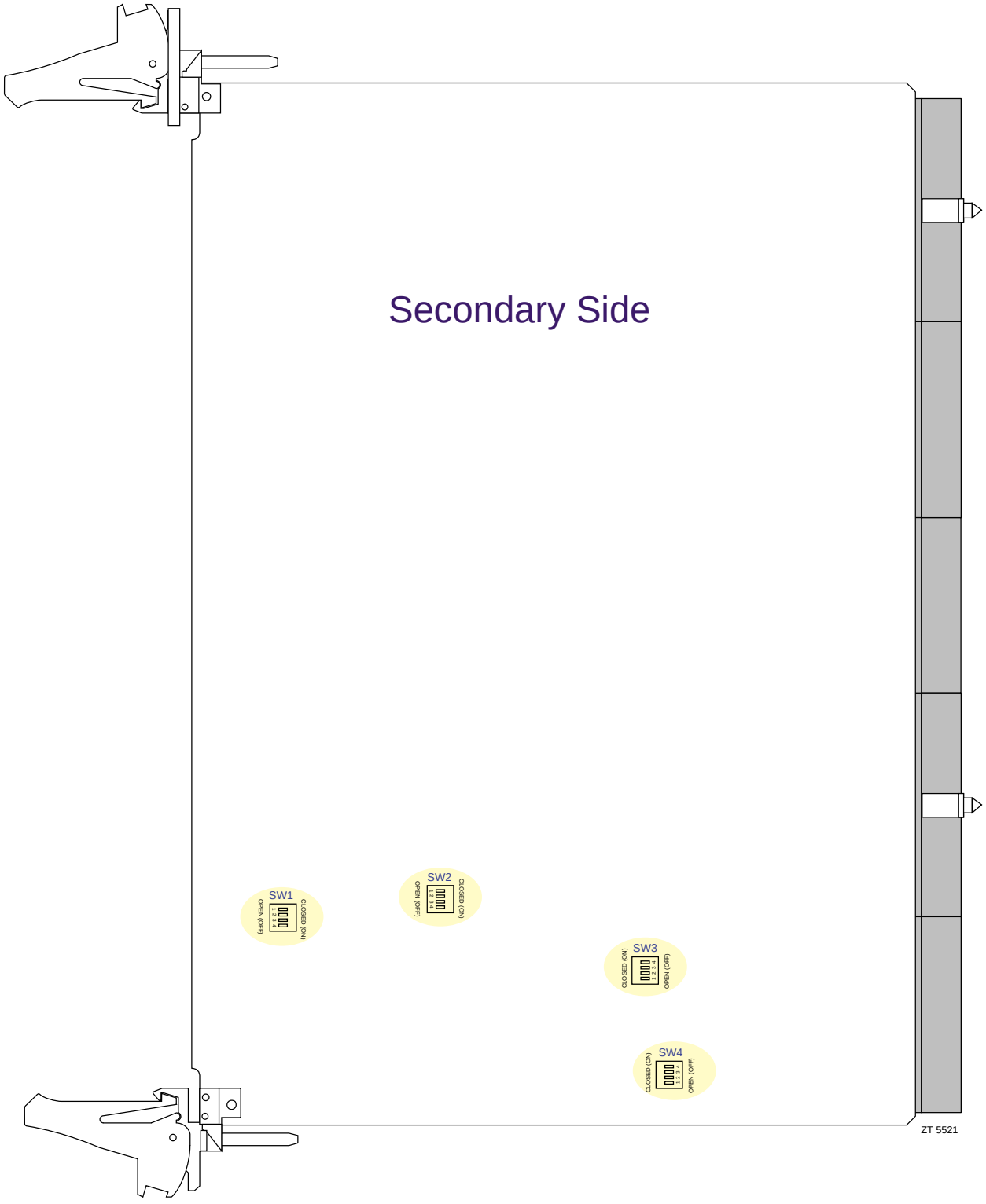
Switch Cross-Reference Table

Function	Switch
System Reset	S1 (push-button on connector plate)
NMI (Abort)	S2 (push-button on connector plate)
BIOS Recovery	SW1-1
Console Redirection	SW1-2
Software Configuration	SW1-3, SW1-4, SW3-1
Ethernet Channel/Port Select	SW2-1, SW2-2
Flash Write Protect	SW2-3
Port 80 Test Mode	SW2-4
CompactFlash (IDE Master/Slave)	SW3-2
CMOS Clear / Battery Backup	SW3-3, SW3-4
CPU Speed Configuration	SW4-1, SW4-2, SW4-3, SW4-4

Factory Default Switch Configuration



Customer Switch Configuration



SWITCH DESCRIPTIONS

The following topics present the switches in numerical order and provide a detailed description of each switch. Switches are titled in the form “SWx-N,” where “x” is the switch number and “-N” is the switch position (for example, SW4-2 means “switch number 4, position 2”). A dagger (†) indicates the default switch configuration.

S1 (System Reset)

S1 is a push-button on the ZT 5521's connector plate. When pressed, S1 issues a System Reset to the CPU.

S2 (Abort Request)

S2 is a push-button on the ZT 5521's connector plate. When pressed, S2 issues a abort request to the host CPU.

SW1-1 (BIOS Recovery)

SW1-1 allows booting from the BIOS Recovery Socket (U10). When SW1-1 is open, the BIOS boots from the on-board flash memory. When SW1-1 is closed, the BIOS boots from the BIOS Recovery Socket (U10). See the section, “BIOS Recovery,” in Chapter 6 for details on how to flash the BIOS. Factory default is open.

	SW1-1	Function
†	Open	Normal operation (boot from flash)
	Closed	Boot from the BIOS recovery socket (U10)

SW1-2 (Console Redirection)

Console Redirection provides a serial communication link (through COM1 or COM2) between a terminal or terminal emulation program and the ZT 5521. This feature requires specific parameters to be set in the BIOS Setup Utility before configuring SW1 2. Refer to the “Console Redirection” chapter in the *“Ziatech Embedded BIOS Manual”* before attempting to use this feature. The status of this switch is monitored by System Register 5 (Port E3h, bit 0). Factory default is open.

	SW1-2	Function
†	Open	Normal Operation
	Closed	Console redirection enabled

† Factory default configuration

SW1-3, SW1- 4, SW3-1 (Software Configuration)

The status of these switches is monitored by the user's software through System Register 5 (Port E3h, bits 1-3) to provide user-configurable features. When open these switches read back a 0; when closed they read back a 1. Factory default is open.

SW1-3, SW1-4, SW3-1	Read-back
† Open	0
Closed	1

SW2-1, SW2-2 (Ethernet Channel/Port Select)

These switches are used to route Ethernet channels A and B to front-or rear-panel Ethernet connectors, according to the table below. By default (open), both channels are configured for front-panel Ethernet.

SW2-1	Ethernet Channel A
† Open	Front-Panel Ethernet (via J11)
Closed	Rear-Panel Ethernet (via J3)

SW2-2	Ethernet Channel B
† Open	Front-Panel Ethernet (via J10)
Closed	Rear-Panel Ethernet (via J3)

SW2-3 (Flash Write-Protect)

Close this switch to hardware write-protect the BIOS and flash disk portion of the flash memory. Open this switch to use the FLASH.EXE utility to recover from a corrupted BIOS. The status of this switch can be read back at System Register 5 (Port E3h, bit 7). Flash can be software write-protected through System Register 1 (Port 78h, bit 1). Factory default is open.

SW2-3	Function
† Open	Flash disk and BIOS is read/write
Closed	Flash disk and BIOS is read only

† Factory default configuration

SW2-4 (Port 80 Test Mode)

This switch allows Port 80 transactions to be accessed at Port E0h. The system BIOS outputs Port 80 POST codes during bootup. The Port 80 data is output on Port 0, bits 0 to 7. These bits are accessible at the I/O Expansion connector J6, pins A8-15. Use this mode for debugging custom software and hardware. Port E0h is also accessible at its default address (E0h). Factory default is open.

	SW2-4	Function
†	Open	Normal operation
	Closed	Port 80 Test Mode

SW3-2 (IDE Master/Slave Selection)

This switch allows the CompactFlash card to be configured as an IDE master or slave device. By factory default (closed), the CompactFlash card is configured as the master device. When SW3-2 is open, the CompactFlash card is the slave device.

Note: The current revision of the ZT 5521 requires that the CompactFlash card must always be configured as the master IDE device.

	SW3-2	Function
	Open	CompactFlash (J22) is IDE Slave
†	Closed	CompactFlash (J22) is IDE Master

SW3-3, SW3-4 (CMOS Clear / Battery Backup)

These switches are used to battery back and clear the CMOS memory. When closed, SW3-3 connects the CMOS memory to the on-board battery (normal operation). If the CMOS needs to be cleared, open SW3-3 and close SW3-4. After two seconds, return SW3-4 to the open position and SW3-3 to the closed position. Factory default is SW3-3 closed and SW3-4 open.

Warning: Do not have SW3-3 and SW3-4 closed at the same time. Doing so will significantly shorten battery life.

	SW3-3	SW3-4	CMOS Configuration RAM
†	Closed	Open	Normal operation - battery backed
	Open	Closed	Clear CMOS (return to default after clearing)

† Factory default configuration

SW4-1—SW4-4 (CPU Configuration Bits 0-3)

These switches are used to control the CPU/PCI bus frequency and CPU Speed Multiplier for different speed processors, according to the following table.

SW4-4 (Bit 4) LINT[1]	SW4-3 (Bit 3) LINT[0]	SW4-2 (Bit 2) A20M#	SW4-1 (Bit) 1 IGNNE#	CPU Speed 66 MHz Bus	CPU Speed 100 MHz Bus	Processor Core Frequency vs. Bus Frequency
Closed	Closed	Closed	Closed			2/1
Closed	Closed	Closed	Open			3/1
Closed	Closed	Open	Closed	266	400	4/1
Closed	Closed	Open	Open	333	500	5/1
Closed	Open	Closed	Closed			5/2
Closed	Open	Closed	Open	233	350	7/2
† **Closed**	**Open**	**Open**	**Closed**		**450**	**9/2**
Closed	Open	Open	Open		550	11/2
Open	Closed	Closed	Closed		600	6/1
Open	Closed	Closed	Open			7/1
Open	Closed	Open	Closed			8/1
Open	Closed	Open	Open			Reserved
Open	Open	Closed	Closed		650	13/2
Open	Open	Closed	Open			15/2
Open	Open	Open	Closed			3/2
Open	Open	Open	Open			2/1

CUTTABLE TRACE OPTIONS AND LOCATIONS

The ZT 5521 contains several cuttable traces (zero Ω shorting resistors) that allow the user to configure certain options not configurable through the BIOS Setup Utility. The "Cuttable Trace Locations" figure shows the placement of the ZT 5521 cuttable traces. The "Cuttable Trace Definitions" table provides a quick cross-reference for the ZT 5521 cuttable trace descriptions that follow.

There are two types of cuttable traces on the ZT 5521: single-option, and double-option. **Single option cuttable traces** are implemented using 0603 surface mount pads. A 0 Ω shorting resistor is then soldered between these pads to make the connection. **Double**

† Factory default configuration

option cuttable traces (CTx, CTy, CTz) are implemented using three 0603 surface mount pads. The 0 Ω shorting resistor is then soldered between one set of pads, depending on the chosen option.

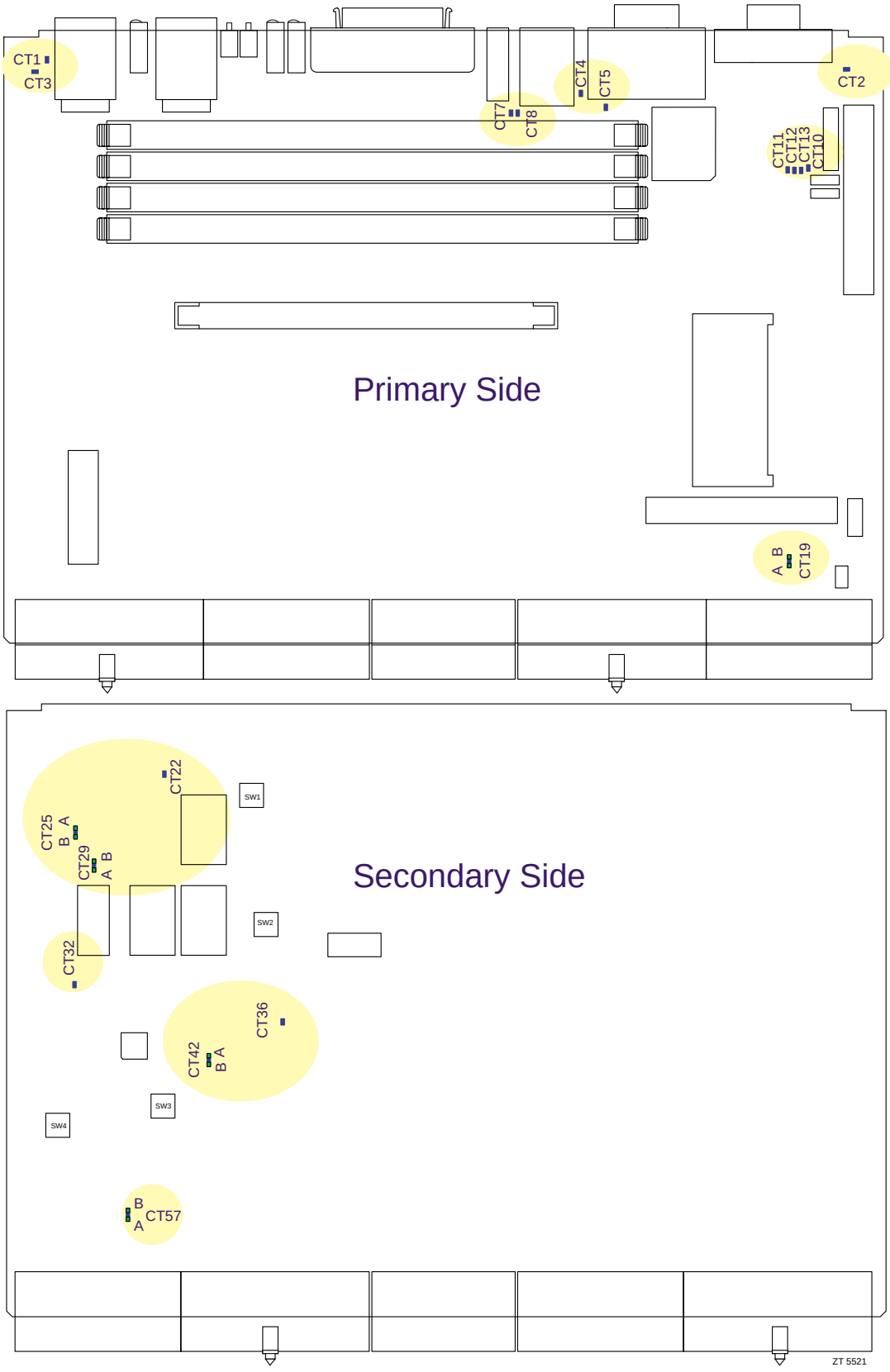
Caution: The ZT 5521 has other cuttable traces not documented in this manual. These are reserved for Ziatech use only and should not be modified by the user.

For documented cuttable traces, modifications should only be performed by a qualified technician familiar with surface mount soldering techniques. The product warranty is voided if the board is damaged by customer modifications.

Cuttable Trace Definitions

CT#	Default	Description
CT1	Out	Left ejector chassis GND to logic GND
CT2	Out	Right ejector chassis GND to logic GND
CT3	Out	J7, LPT GND to logic GND
CT4	Out	J12, Mouse GND to logic GND
CT5	Out	J8, COM1 GND to logic GND
CT7	Out	J9, USB GND to logic GND
CT8	Out	J12, Keyboard GND to logic GND
CT19	A	USB Port 1 Routing
CT22	Out	J8, COM2 GND to logic GND
CT25	B	Fan Select 12V/5V (12V def.)
CT29	Out	EGND to GND ENETA
CT32	Out	DRATE0 or MSEN0 Selection
CT34	In	PDIAG between master/slave IDE devices
CT36	In	Watchdog “NMI” to IOCHK-
CT37	Out	EGND to GND ENETB
CT42	A	CompactFlash Voltage Select 3.3V/5V (3.3V def.)
CT57	A	USB Port 1 Routing

Cuttable Trace Locations



CT1-5, CT7-8, CT22 (Connect Chassis GND to Logic GND)

By default, the ZT 5521's front-panel connectors are on an isolated chassis ground. These connectors can be connected to the ZT 5521 logic ground by installing these eight cuttable traces. All eight cuttable traces should be in or all eight should be out. The factory default is All Out.

Position	Function
All In	Front panel connectors connected to logic ground.
† All Out	Front panel connectors on an isolated chassis ground.

CT19, CT57 (USB Port 1 Routing)

These cuttable traces route USB Port 1 to connector backplane J3 for rear-panel use, or to the on-board I/O Expansion connector J19, according to the following table. The factory default is position A for both traces.

CT19	Function	CT57	Function
† A	USB Port 1 to J3	† A	USB Port 1 to J3
B	USB Port 1 to J19	B	USB Port 1 to J19

CT25 (FAN Voltage Selection)

This cuttable trace selects the operating voltage for applications implementing a user-supplied on-board fan, according to the table below. Factory default is position B.

Position	Function
A	5 V fan operation
† B	12 V fan operation

CT29, CT37 (Earth Ground to Ethernet Ground)

These cuttable traces connect earth ground to Ethernet A and B ground, according to the table below. Factory default is out.

Position	Cuttable Trace	Function
† Out	CT29	EGND to GND ENETA
† Out	CT37	EGND to GND ENETB

† Factory default configuration

CT32 (Floppy DRATE0 to MSEN0)

Some manufacturer's floppy drives require a connection between the floppy drive MSEN0 pin and the floppy controller's DRATE0 pin. Install CT32 if your system requires this. The factory default is out.

CT32	Function
In	Floppy MSEN0 pin connected to controller's DRATE0 pin.
† Out	Floppy MSEN0 pin not connected to controller's DRATE0 pin.

CT34 (PDIAG Between Master/Slave IDE Devices)

Installing CT34 connects the IDE PDIAG signal between the CompactFlash connector (J22) and the IOX Connector (J19). The factory default is in.

CT 34	Function
† In	IDE controller PDIAG signal connected between CompactFlash card and IOX Connector, J19.
Out	IDE controller PDIAG signal not connected.

CT36 (Watchdog NMI to IOCHK-)

CT36 connects the programmable watchdog timer NMI output to the ISA bus IOCHK- signal. When CT36 is installed and the watchdog timer times out, a non-maskable interrupt is generated. See Chapter 5, "Watchdog Timer," for more about NMI and the Watchdog Timer. The factory default is in.

CT36	Function
† In	NMI generated when watchdog times out.
Out	NMI connected to the ISA bus IOCHK- signal.

CT42 (CompactFlash Voltage Select)

CT42 selects the voltage for the CompactFlash device loaded in connector (J22). The A position selects 3.3 V; the B position selects 5 V. The factory default is position A.

Position	Function
† A	3.3 V CompactFlash operation
B	5 V CompactFlash operation

† Factory default configuration

4. ENHANCED IDE INTERFACE

This chapter provides an introduction to the ZT 5521's Enhanced IDE Interface Controller. It covers the ZT 5521's support for remote or internal EIDE disk drives, including on-board solid state IDE capability provided by a CompactFlash drive.

The ZT 5521's EIDE interface provides two EIDE channels for interfacing with up to four drives. The EIDE controller is incorporated into the Intel PIIX4E (82371EB) chipset, thus it utilizes the Peripheral Component Interconnect (PCI) bus to give exceptional EIDE performance. The EIDE interface can sustain a maximum transfer rate of 33 MB per second between the EIDE drive buffer and PCI.

FEATURES OF THE EIDE INTERFACE

- IBM-AT compatible
- 32-bit, 33 MHz, high performance PCI bus interface
- Supports PIO and Bus Master EID
- "Ultra DMA/33" Synchronous DMA Operation
- Bus Master IDE transfers up to 33 MB
- Primary and Secondary channels for interfacing up to four devices
- On-board CompactFlash EIDE flash drive
- Individual software control for each EIDE channel

DISK DRIVE SUPPORT

The ZT 5521 supports either internal or external EIDE disks. These configurations are described below. The "Identifying Media Options" topic in Chapter 2 details many disk drive connection options depending on the boards in your system.

Note: Configuration of switch SW3-2 and cuttable trace CT42 may be required for proper EIDE operation.

Internal Disks

The ZT 5521 provides a CompactFlash option as its internal EIDE support. This option directs the EIDE primary channel signals to connector J22 for CompactFlash memory cards configured as solid state drive. J22 is a 50-position right angle surface mount header designed to accommodate CompactFlash expansion cards which appear to the system as a hard drive and are automatically supported by most operating systems.

External Disks

For external EIDE disk drives (i.e., not on the ZT 5521) EIDE secondary channel signals are directed via rear-panel I/O connector J3 to an optional transition board (such as the ZT 4804), providing connection to the external disk(s).

I/O MAPPING

The I/O map for the EIDE interface varies depending on the mode of operation. The default mode is “compatibility mode,” which means that the interface uses the PC-AT legacy addresses of 1F0h-1F7h, with 3F6h and interrupt IRQ14 for the primary channel. The secondary channel uses I/O addresses 170h-177h, 376h and interrupt IRQ15. No memory addresses are used.

Input Characteristics

The ZT 5521's CompactFlash connector J22 works only with Type 1 CompactFlash cards with 3.3 V minimum Vih, I1Z, (Type 1), CMOS voltage input, (Vcc = 5.0 V). SanDisk™ currently manufactures cards with these tolerances.

CompactFlash Card Installation and Removal

To install or remove a CompactFlash card, perform the steps below.

Warning: To avoid damage to the CPU, perform the installation and removal at a static-free workstation.

Installation

1. Make sure the system is powered off.
2. Put on an anti-static grounding strap.
3. Most CompactFlash cards have an arrow on the top label to indicate correct orientation. Align the arrow on the CompactFlash card with the arrow on the connector and slide the card into place until the connection is snug. The dimensions of the grooves in the sides of the CompactFlash card prevent incorrect installation.

Removal

1. Make sure the system is powered off.
2. Put on an anti-static grounding strap.
3. Grasp the card and pull it out of the header.

DEVICE DRIVERS

The EIDE interface works with all applications by default. To fully utilize the EIDE interface, you may install additional drivers to increase the performance under MS-DOS, Windows 3.X, Windows 95, Windows NT, IBM® OS/2®, SCO®, UNIX® and Novell® Netware™. Contact the vendors of individual operating systems for the latest drivers for the Intel PIIX4E (82371EB) EIDE interface.

Note: You may have difficulty installing the QNX operating system, ver. 4.24, on CompactFlash cards. If problems occur, restart the install program and specify regular IDE drivers (Fsys.ide) instead of the default EIDE drivers (Fsys.eide).

5. WATCHDOG TIMER

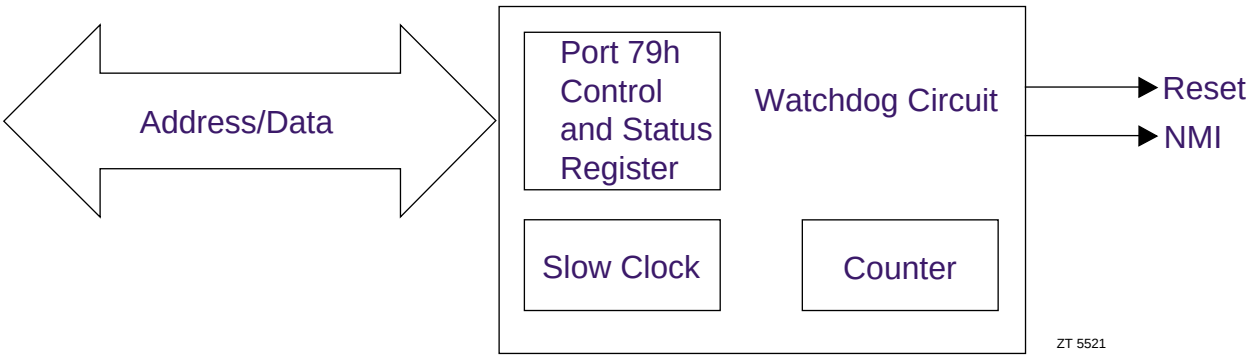
This chapter explains the operation of the ZT 5521's watchdog timer. It provides an overview of watchdog operation and features, as well as sample code to help you learn how the watchdog timer works with applications.

WATCHDOG TIMER OVERVIEW

The primary function of the watchdog timer is to monitor ZT 5521 operation and take corrective action if the system fails to function as programmed. The major features of the watchdog timer are:

- Two-stage
- Enabled and disabled through software control
- Armed and strobed through software control

Watchdog Timer Architecture



The ZT 5521's custom watchdog timer circuit is implemented in a programmable logic device. The watchdog timer contains a Control and Status Register (documented in the manual as System Register 2, Port 79h. See Appendix C for the register table). The register allows the BIOS or user applications to determine the source of a particular reset (watchdog time out, power up, power out-of-range/low voltage, etc.). The watchdog timer drives NMI and RST. When the watchdog times out, NMI is driven first, followed by RST 250 ms later. Watchdog NMI and RST can be independently disabled.

Eight timeout intervals are selectable from the watchdog Control and Status Register. Minimum timeout period = 250 ms. Maximum timeout period = 256 s. The watchdog is strobed by reading the Control and Status Register. This resets the timer.

Power Up Initialization

The watchdog timer's programmable logic is only initialized at power up. This ensures that the NMI, RST, NMI ENABLE, and RESET ENABLE status and control bits power

up to unasserted states, allowing the BIOS or user applications to determine the reset source (watchdog time out, power up, power out-of-range/low voltage, etc.).

Time Out Values

The watchdog timer has its own separate slow clock source. This clock runs at a maximum frequency of 32 Hz (25 Hz nominal). Because this slow clock is based on a RC oscillator, the nominal timeout period is approximately 30% longer than the minimum value. The watchdog is guaranteed to timeout in no less than the programmed minimum value.

USING THE WATCHDOG IN AN APPLICATION

The following topics are provided to help you learn how to use the watchdog in an application. The watchdog's Reset and NMI functions are described and sample code is provided. Watchdog Reset and NMI are controlled through the watchdog's "Control and Status Register" (documented in this manual as System Register 2, Port 79h).

Watchdog Reset

An application using the reset feature enables the watchdog reset, sets the terminal count period, then periodically strobes the watchdog to keep it from resetting the system. If a strobe is missed, the watchdog assumes that an application error has occurred and resets the system hardware.

Enabling the Watchdog Reset

C code for enabling the watchdog reset might look like the following:

```
#define WD_RESET_EN_BIT_SET 0x20

Void EnableWatchdogReset(void){
   Unsigned char WdValue;              // Holds watchdog register
                                          values.
                                       //
   WdValue = inb(WD_CSR_IO_ADDRESS);   // Read the current contents of
                                          the watchdog // register.
   WdValue |= WD_RESET_EN_BIT_SET;     // Assert the enable bit in the
                                          local copy.
   Outb(WD_CSR_IO_ADDRESS,WdValue); // Assert the enable in the
                                       watchdog register.
}
```

Setting the Terminal Count

The terminal count determines how long the watchdog waits for a strobe before resetting the hardware. C code for setting the terminal count might look like the following:

```
#define WD_CSR_IO_ADDRESS   0x79    // IO address of the watchdog
#define WD_T_COUNT_MASK     0x07    // Bit mask for terminal count
                                       bits.
#define WD_500MS_T_COUNT    0x01    // Terminal count values . . . .
#define WD_1S_T_COUNT       0x00    //
#define WD_250MS_T_COUNT    0x00    //
.
.
.
Void SetTerminalCount(void){
   Unsigned char WdValue;           // Holds watchdog register values.
                                    //
WdValue = inb(WD_CSR_IO_ADDRESS);   // Get the current contents of the
                                       watchdog register.
   WdValue &= ~ WD_T_COUNT_MASK;    // Mask out the terminal count
                                       bits.
   WdValue |= WD_500MS_T_COUNT;     // Set the desired terminal count.
   Outb(WD_CSR_IO_ADDRESS,WdValue); // Furnish the watchdog register
                                       with the new count value.
}
```

Strobing the Watchdog

Once the watchdog is enabled, it must be continuously strobed within the terminal count period to avoid resetting the system hardware. C code to strobe the watchdog might look like the following:

```
Void StrobeWatchdog(void){
   Inb(WD_CSR_IO_ADDRESS);          // A single read is all it takes.
}
```

Watchdog NMI

When enabled, an NMI precedes a watchdog reset by 250 ms. The NMI generation feature gives the application 250 ms to perform essential tasks before the hardware is reset. Before using watchdog NMI, ensure the following:

- The code for performing the essential tasks is included in an interrupt service routine (ISR)
- The ISR is chained to the existing NMI ISR
- The watchdog NMI is enabled

Chaining the ISRs

Save the original NMI ISR vector so that it can be invoked from the new watchdog NMI ISR. Alter the interrupt vector table so that the NMI ISR vector is overwritten with a vector to the watchdog ISR. C code to do this in DOS might look like the following:

```
#define NMI_INTERRUPT_VECTOR_NUMBER 2

void interrupt far (*OldNmiIsr)();


Void HookWatchdogIsr(void){

//
// To be absolutely certain the interrupt table is not accessed by an
   NMI (This is quite unlikely.), the application could  disable NMI in
   the chip set before installing the new vector.
//
.
.
.
//
// Install the new ISR.
//
OldNmiIsr = getvect(IsrVector);        // Save the old vector.
setvect(NMI_INTERRUPT_VECTOR_NUMBER, WatchdogIsr);  // Install the new.
}
```

Enabling the Watchdog NMI

To activate the NMI feature, enable it in the watchdog register (Port 79h). The code to do this might look like the following:

```
#define WD_NMI_EN_BIT_SET     0x10
Void EnableWatchdogNmi(void){
   Unsigned char WdValue;             // Holds watchdog register values.
                                      //
WdValue = inb(WD_CSR_IO_ADDRESS);     // Read the current contents of
                                              the watchdog register.
   WdValue |= WD_NMI_EN_BIT_SET;      // Assert the enable bit in the
                                              local copy.
   Outb(WD_CSR_IO_ADDRESS,WdValue);   // Assert the enable in the
                                              watchdog
// register.
}
```

NMI Handler

Because the NMI may have originated from another source such as a RAM Error Correction Code (ECC) error, the NMI handler cannot assume that the NMI occurred due to a watchdog time out. Therefore, the NMI handler must check the watchdog status register before taking watchdog-related emergency action. When the NMI handler completes handling the emergency, it invokes the original NMI Handler (discussed above). The code to do this might look like the following:

```
#define WD_NMI_DETECT_BIT_SET   0x40  // Bit that indicates an NMI
                                          occurred, set.
                                      //
Void WatchdogIsr(void){               //
                                      //
                                      //
// Did the watchdog cause the NMI?
//
   if(inb(WD_CSR_IO_ADDRESS) & WD_NMI_DETECT_BIT_SET){
                                      //
   TripAlarm();                       // Take care of essential tasks.
                                      //
   TurnOffTheGas();                   //
   }                                  //
   _chain_intr(OldNmiIsr);            // Invoke the originally
                                          installed ISR.
}
```

Other Watchdog NMI Uses

The watchdog NMI feature can be used independently of the watchdog reset feature. It can also be used without actually causing NMIs. For example, the CPU board could be configured such that the watchdog does not actually drive the NMI line. In this case, in a multi-tasking operating system, one thread could be responsible for strobing the watchdog and a second thread could monitor the NMI bit of the watchdog register. The second thread could then take emergency action if the first thread falters. Code for checking the bit is provided in the “NMI Handler” topic above.

6. FLASH MEMORY

The ZT 5521 provides 8 MB of on-board flash memory. In addition to containing the system BIOS, the flash device may contain space usable for a non-volatile solid state drive. The size of the solid state drive is configurable through the BIOS Setup Utility. A device driver is required for drive emulation. This solid state drive can be used to store user programs and data; however, since it is a flash memory, it has a limited write cycle life (approximately 1,000,000 cycles).

See the *Ziatech Embedded BIOS Software Manual* for more information on the solid state drive and available device drivers.

The flash device is divided into 16 pages mapped into a window in extended memory. Access to the flash disk is transparent to the user and handled by a software driver. The operating system determines which driver is used.

Write-protect the flash memory through switch SW2-3. The BIOS portion of the flash memory is mapped as a block in lower memory. To reprogram the BIOS or update it if it becomes corrupted, use the FLASH.EXE utility available from Ziatech and discussed later in this chapter.

The remainder of the flash memory is user programmable. The following information is required for successful flash programming:

1. The base address of the flash window.

2. The size of the flash window.

3. The portions of flash reserved for other purposes.

4. The flash device programming method.

5. How to map a page of flash memory.

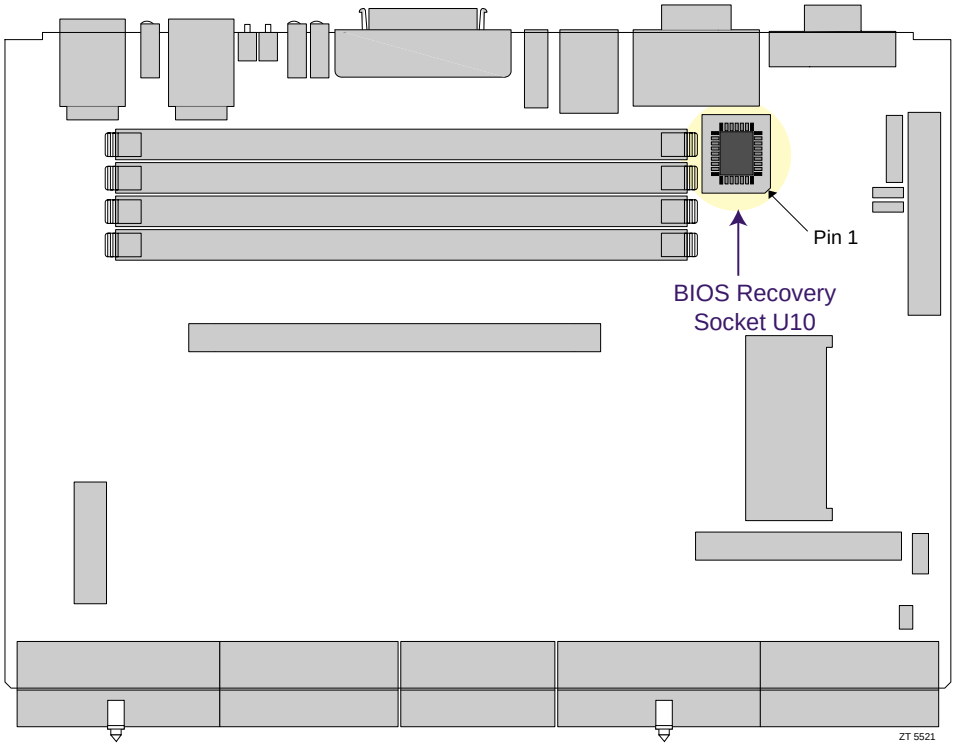
6. How to write-protect the flash device through software.

Refer to the “Ziatech System Information Structure" appendix in the *Ziatech Embedded BIOS* software manual for instructions on how to determine items 1-4. System Register 1 (Port 78h) controls items 5 and 6.

BIOS RECOVERY

ZT 5521 provides a BIOS Recovery Socket (U10) for use if the ZT 5521's BIOS becomes corrupted. This 32-pin socket accommodates an EPROM programmed with the BIOS to allow the board to boot when powered on. The board is shipped with the EPROM pre-installed.

BIOS Recovery Socket Location



To boot from the boot socket:

1. Close switch SW1-1.
2. Make sure flash write protection is disabled (SW2-3 = open).
3. Insert the EPROM into the boot socket. Make sure the device is correctly oriented with pin 1 facing the backplane connectors.
4. After powering on the board, reprogram the on-board flash with the BIOS by using the FLASH.EXE utility (see the "Flash Utility Program" topic below for detailed instructions).
5. After flashing the BIOS, turn off power and open switch SW 1-1.
6. If desired, enable flash write protection by closing switch SW2-3.

FLASH UTILITY PROGRAM

FLASH.EXE is a utility program that comes with the Ziatech Software Development Kit. It allows the user to quickly modify the BIOS in the on-board flash memory. This eliminates the need for a PROM programmer and frees the user from having to remove boards and chips from the system. Before attempting to program the flash, make sure that switch SW2-3 is open (Flash Write Protect switch).

To reprogram the BIOS on the ZT 5521, use the following syntax at a DOS prompt:

```
FLASH  /b  BIOS.XXX
```

where BIOS.XXX is the BIOS image for the ZT 5521. See the *Ziatech Embedded BIOS* software manual for more information on the flash utility.

A. SPECIFICATIONS

This appendix describes the electrical, environmental, and mechanical specifications of the ZT 5521. It includes illustrations of the board dimensions and connector locations, as well as connector descriptions and pinout tables.

ELECTRICAL AND ENVIRONMENTAL SPECIFICATIONS

The following topics provide tables and illustrations showing the following electrical and environmental specifications:

- Absolute maximum ratings
- DC operating characteristics
- Battery backup characteristics

Absolute Maximum Ratings

The values below are stress ratings only. Do not operate the ZT 5521 at these maximums. See the "DC Operating Characteristics" topic in this appendix for operating conditions.

Supply Voltage, Vcc:	5.25 V
Supply Voltage, Vcc3:	3.6 V
Supply Voltage, AUX +:	13 V
Storage Temperature:	-40° to +85° Celsius
Non-Condensing Relative Humidity:	<95% at 40° Celsius

Operating Temperature

The ZT 5521 comes from the factory with an integrated heatsink for cooling the processor† module. The maximum processor core temperature must not exceed 90° C. The heatsink allows a maximum ambient air temperature of 45° C with 250 linear feet per minute (LFM) of airflow. The maximum power dissipation of the CPU is 32 W.

Warning: External airflow must be provided at all times during operation to avoid damaging the CPU module. Ziatech strongly recommends use of a fan tray below the card rack to supply the external airflow.

† Thermal data for ZT 5521 boards implementing the Pentium III processor was not available at the time this manual was produced. Contact Ziatech for additional information.

The "Thermal Requirements" table in Appendix D shows the relationship between ambient air temperature, board temperature, and processor core temperature.

DC Operating Characteristics

Supply Voltage, Vcc:	4.75 V min. to 5.25 V maximum
Supply Voltage, Vcc3:	3.0 V min. to 3.6 V maximum
Supply Voltage, AUX+:	11.0 min. to 13.0 V maximum

Supply Current

450 MHz Pentium II processor

Icc (A)	5 A typical to 10 A maximum
Icc3 (A)	5 A typical to 7 A maximum
AUX + (12 V)	300 mA typical to 500 mA maximum

500 MHz, 850 MHz Pentium III processors

Icc (A)	5 A typical to 10 A maximum
Icc3 (A)	5 A typical to 7 A maximum
AUX + (12 V)	300 mA typical to 500 mA maximum

Note: Numbers assume 512 MB of SDRAM, 512 KB cache, 8 MB flash. Additional SDRAM does not change these numbers.

Battery Backup Characteristics

Battery Voltage:	3 V
Battery Capacity:	250 mAh
Real-Time Clock Requirements:	8 µA maximum (Vbat = 3 V, Vcc=0 V)
Real-Time Clock Data Retention:	31,250 Hours/ 3.7 years minimum (not powered) 5.2 years minimum (with Vcc power applied 8 hours per day)
Electrochemical Construction:	Poly carbonmonofluoride

RELIABILITY

MTBF: 7.9 years

MTTR: 5 minutes

MECHANICAL SPECIFICATIONS

This section includes the following mechanical specifications:

- Board dimensions and weight
- Connectors (including connector locations, descriptions, and pinouts)

Board Dimensions and Weight

The ZT 5521 meets the *CompactPCI Specification, PICMG 2.0, Version 2.1* for all mechanical parameters. In a CompactPCI enclosure with 0.8 inch spacing, the ZT 5521 with a single CPU and integrated heatsink requires two card slots.

Mechanical dimensions are shown in the "Board Dimensions" illustration and are outlined below.

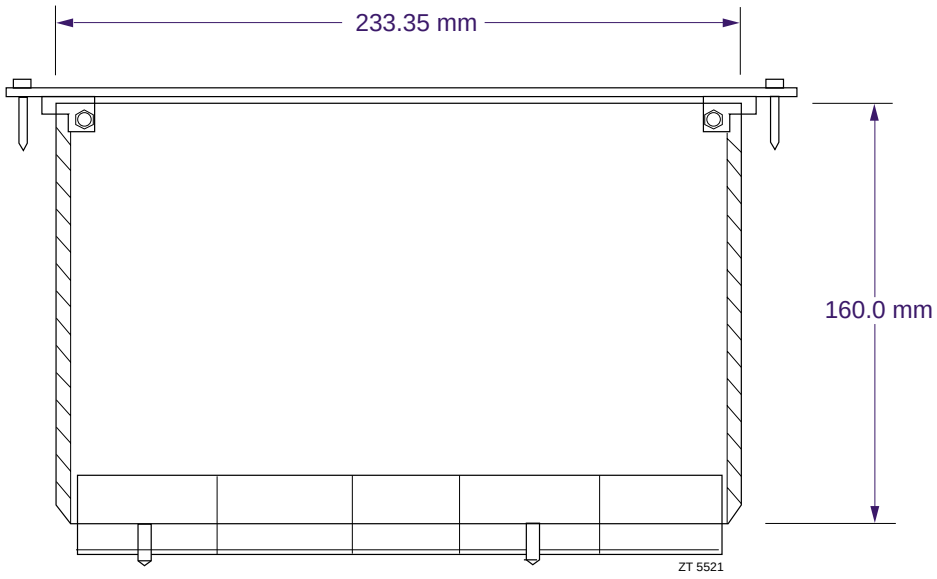
Board Length: 160 mm (6.304 inches)

Board Width: 233.35 mm (9.194 inches)

Board Height: 34.29 mm (1.350 inches)

Board Weight: 0.907 Kilograms (2.0 pounds) with heatsink and 4 SDRAM modules

Board Dimensions



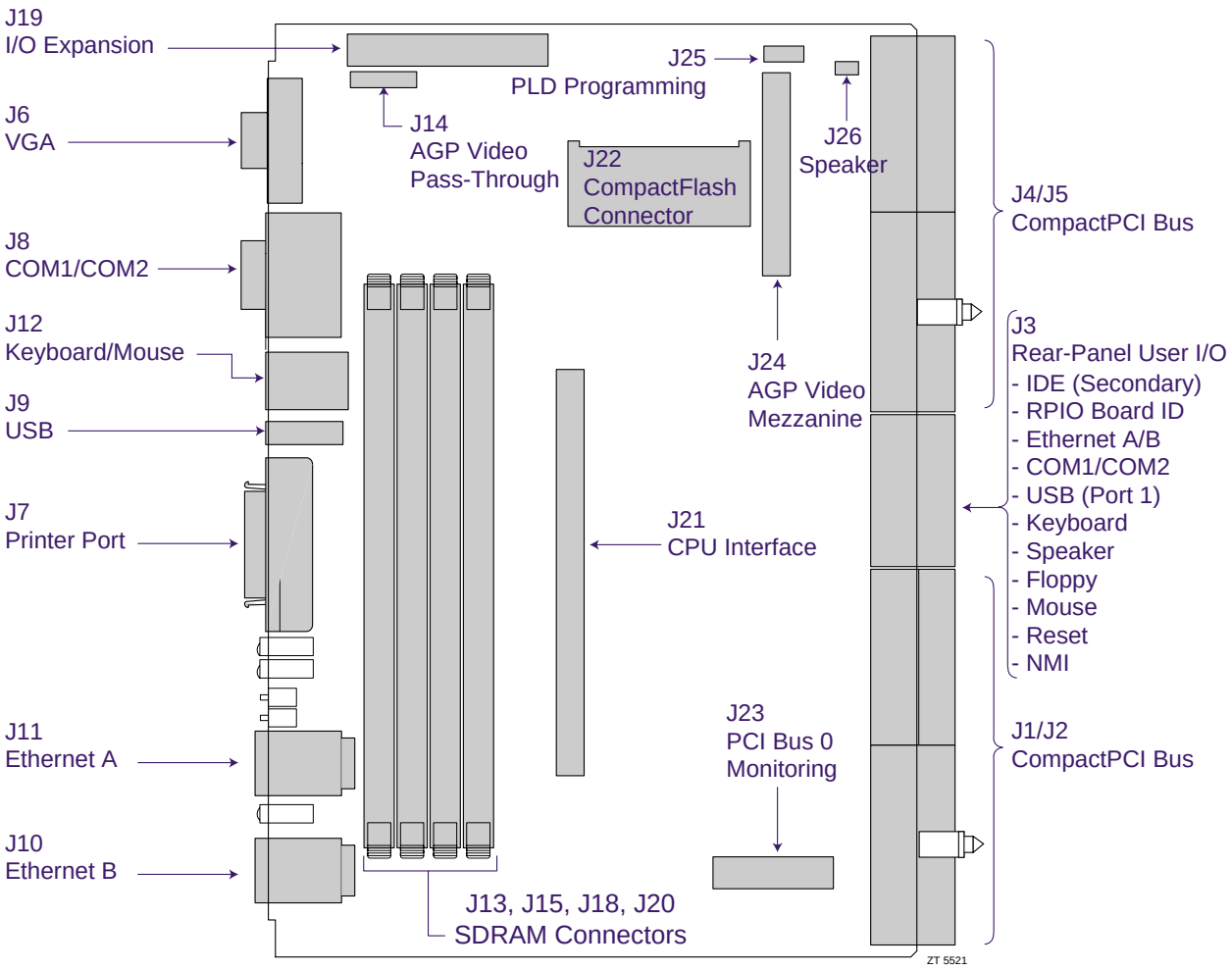
Connectors

As shown in the "Connector Locations" figure, the ZT 5521 includes several connectors to interface to application-specific devices. A brief description of each connector is given in the "Connector Assignments" table below. A detailed description and pinout for each connector is given in the following topics.

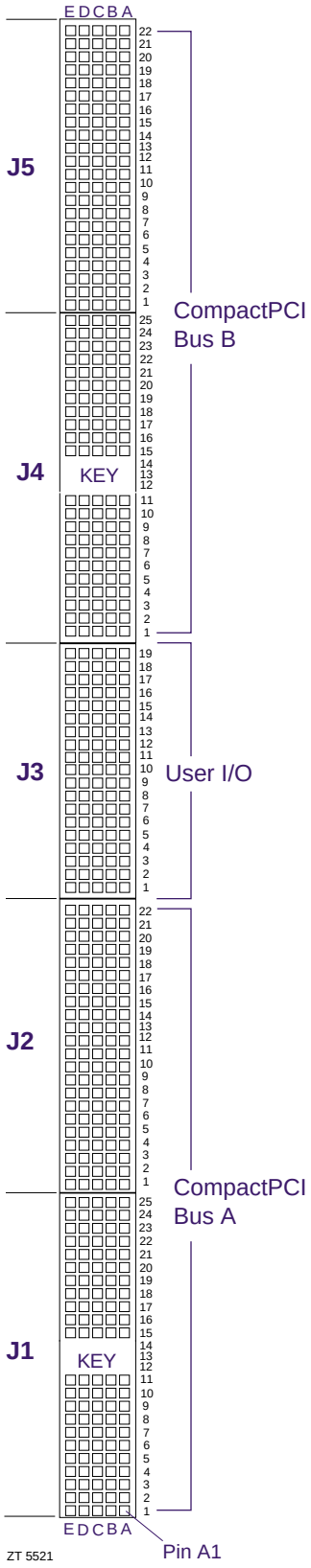
Connector Assignments

Connector	Function
J1, J4	CompactPCI Bus Connectors (110-pin, 2 mm x 2 mm, female)
J2, J5	CompactPCI Bus Connectors (110-pin, 2 mm x 2 mm, female)
J3	Rear-Panel User I/O Connector (95-pin 2 mm x 2 mm, female)
J6	Front-panel Video Interface (15-pin, D-Shell)
J7	Printer Port Interface Connector (IEEE-1284, 36-pin 1284-C)
J8	COM1 and COM2 Serial Ports (Dual 9-pin, D-Shell)
J9	Universal Serial Bus Connector (4-pin, USB, Port 0)
J10, J11	Ethernet B/A Connectors (8-pin, RJ-45)
J12	PS/2 Keyboard/Mouse Connectors (Dual 6-pin, DIN)
J13, J15, J18, J20	SDRAM Connectors (168-pin)
J14	AGP Video Pass-Through Connector (16-pin)
J19	I/O Expansion Connector (100-pin, 2 mm)
J21	CPU Interface Connector (Mictor 266-pin); Reserved for Ziatech use
J22	CompactFlash Connector (50-pin, CF Card Slot Header)
J23	PCI Bus 0 Monitoring Connector
J24	AGP Video Mezzanine Connector (Mictor 114-pin)
J25	PLD Programming Connector (10-pin, 2 mm, male)
J26	Speaker Connector (2-pin)

Connector Locations



Backplane Connectors Pin Locations



J1, J4 (CompactPCI Bus Connectors)

J1 and J4 are a 110-pin, 2 mm x 2 mm, female 32-bit CompactPCI connectors (AMP 352068-1 or equivalent). Rows 12-14 are used for connector keying. See the "J1, J4 CompactPCI Bus Connectors Pinout" table below for pin definitions and the figure "Backplane Connectors Pin Locations" on the previous page showing pin placement.

J1, J4 CompactPCI Bus Connectors Pinout

Pin	A	B	C	D	E	F
25	5V	REQ64#	**ENUM#**	3.3V	5V	GND
24	AD[1]	5V	**V(I/O)**	AD[0]	ACK64#	GND
23	3.3V	AD[4]	AD[3]	**5V**	AD[2]	GND
22	AD[7]	GND	**3.3V**	AD[6]	AD[5]	GND
21	3.3V	AD[9]	AD[8]	GND	C/BE[0]#	GND
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	3.3V	AD[15]	AD[14]	**GND**	AD[13]	GND
18	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	3.3V	NC	NC	**GND**	PERR#	GND
16	DEVSEL#	GND	V(I/O)	STOP#	NC	GND
15	3.3V	FRAME#	IRDY#	**BD_SEL#**	TRDY#	GND
12-14	KEY AREA					
11	AD[18]	AD[17]	AD[16]	**GND**	C/BE[2]#	GND
10	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	C/BE[3]#	**IDSEL**	AD[23]	**GND**	AD[22]	GND
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	**GND**	AD[27]	GND
6	REQ#	GND	**3.3V**	CLK	AD[31]	GND
5	NC	NC	**PCI_RST#**	**GND**	GNT#	GND
4	NC	**HEALTHY#**	**V(I/O)**	NC	NC	GND
3	INTA#	INTB#	INTC#	**5V**	INTD#	GND
2	NC	5V	NC	NC	NC	GND
1	5V	-12V	NC	+12V	5V	GND

= long pins = short pins All others = medium length pins

Note: Row F GND pins are long length as is standard for CompactPCI.

J2, J5 (CompactPCI Bus Connectors)

J2 and J5 are a 110-pin 2 mm x 2 mm right-angle female 64-bit Compact PCI connectors (AMP 352152-1 or equivalent). See the "J2, J5 CompactPCI Bus Connectors Pinout" table below for pin definitions and the "Backplane Connectors Pin Locations" figure showing pin placement.

J2, J5 CompactPCI Bus Connectors Pinout

Pin #	A	B	C	D	E	F
22	GA4	GA3	GA2	GA1	GA0	GND
21	CLK6	NC	NC	NC	NC	GND
20	CLK5	NC	NC	GND	NC	GND
19	NC	NC	NC	NC	NC	GND
18	NC	NC	NC	GND	NC	GND
17	NC	GND	PRST#	REQ7#	GNT6#	GND
16	NC	NC	DEG#	GND	NC	GND
15	NC	GND	FAL#	REQ5#	GNT5#	GND
14	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	C/BE[5]#	64EN-	V(I/O)	C/BE[4]#	PAR64	GND
4	V(I/O)	NC	C/BE[7]#	GND	C/BE[6]#	GND
3	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	CLK2	CLK3	NC	GNT2#	REQ3#	GND
1	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
Pin #	**A**	**B**	**C**	**D**	**E**	**F**

J3 (Rear-Panel User I/O Connector)

J3 is a 95-pin 2 mm x 2 mm female connector (AMP 352171-1 or equivalent) providing rear-panel user I/O. See the "J3 Rear-Panel User I/O Connector Pinout" table for pin definitions and the "Backplane Connectors Pin Locations" figure showing pin placement.

J3 Rear-Panel User I/O Connector Pinout

Pin #	A	B	C	D	E	F
19	PWRGD	HDIO16-	SIORDY	SMBALRT	IRQ15	GND
18	SMBDATA#	SMBCLK-	CS3S-	CS1S-	RP_ID	GND
17	DD15	DD14	DD13	DD12	NC	GND
16	DD11	DD10	DD9	DD8	SDDACK	GND
15	DA0	DA1	SW-VCC	DA2	SDDRQ	GND
14	DD7	DD6	DD5	DD4	SDI0W-	GND
13	DD3	DD2	DD1	DD0	SDIOR-	GND
12	DR0-	MSEN0	MTR0-	INDEX-	WDATA-	GND
11	DR1-	DSKCHG-	MTR1-	DENSL	RDATA-	GND
10	WP-	HDSEL-	DIR-	TRK0-	STEP-	GND
9	WGATE-	RXBACKA-	GND	NC	USB+	GND
8	GND	RXBACKA+	SW-VCC	TXCTB	USB-	GND
7	RXBACKB-	GND	TXBACKB-	TXCTA	GND-	GND
6	RXBACKB+	GND	TXBACKB+	GND	TXBACKA-	GND
5	ABORT-	MSDAT	SPKR	KBDAT	TXBACKA+	GND
4	PBRST-	MSCLK	SW-VCC	KBCLK	S1RXD	GND
3	S1CTS	S1RTS	S1DSR	S1DCD	S1TXD	GND
2	S2RIN	S2DTR	S1RIN	S1DTR	S2RXD	GND
1	S2CTS	S2RTS	S2DSR	S2DCD	S2TXD	GND
Pin #	**A**	**B**	**C**	**D**	**E**	**F**

J6 (Video Interface)

J6 is an HD15, 15-pin, female, D-shell connector (AMP 177514-9 or equivalent) providing an interface for front-panel VGA signals routed from the J14 AGP Video Pass-Through Connector. See the “J6 Video Interface Pinout” table below for pin definitions.

J6 Video Interface Pinout

Pin #	Signal	Pin #	Signal	Pin #	Signal
1	RED	6	RGND	11	NC
2	GRN	7	GGND	12	SDA
3	BLUE	8	BGND	13	HSYNC
4	NC	9	VCC	14	VSYNC
5	DGND	10	SGND	15	SCL

J7 (Printer Port Interface Connector)

J7 is a 36-pin IEEE-1284 Printer Port Interface connector (AMP 2-178238-5 or equivalent) providing connection to standard printer functions. The connector adheres to the *IEEE 1284-C Specification*. Printer port signals are not available on J3 for rear-panel operation. See the “J7 Printer Port Interface Connector Pinout” table below for pin definitions.

J7 Printer Port Interface Connector Pinout

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	BUSY	10	PPD4	19	GND	28	GND
2	SLCT	11	PPD5	20	GND	29	GND
3	ACK-	12	PPD6	21	GND	30	GND
4	ERR-	13	PPD7	22	GND	31	GND
5	PE	14	INIT-	23	GND	32	GND
6	PPD0	15	STB-	24	GND	33	GND
7	PPD1	16	SLIN-	25	GND	34	GND
8	PPD2	17	AFD-	26	GND	35	GND
9	PPD3	18	HLD	27	GND	36	PLH

J8 (COM1 and COM2 Serial Ports)

J8 is a dual 9-pin D-shell connector (OUPIIN 7936-09MMY1 or equivalent) providing the COM1 and COM2 interfaces on the ZT 5521's front panel. COM1 and COM2 interface signals are also directed out J3 for use by an optional rear-panel transition board (such as the ZT 4804). See the “J8 COM1 and COM2 Serial Ports Pinout” table below for pin definitions.

J8 COM1 and COM2 Serial Ports Pinout

Pin#	COM1/COM2 Function	Pin#	COM1/COM2 Function
1	DCD	6	DSR
2	RXD	7	RTS
3	TXD	8	CTS
4	DTR	9	RIN
5	GND		

J9 (Universal Serial Bus Connector)

J9 is the Port 0 Universal Serial Bus (USB) interface connector (AMP 440260-1 or equivalent) located on the front panel. J9 can be used simultaneously with a USB connector (Port 1) on a rear-panel transition board (such as the ZT 4804). See the “J9 Universal Serial Bus Connector Pinout” table below for pin definitions.

J9 Universal Serial Bus Connector Pinout

Pin #	Function
1	Vcc (Fused)
2	DATA-
3	DATA+
4	GND

J10, J11 (Ethernet Connectors)

J10 (ENET B) and J11 (ENET A) are RJ-45 connectors (Stewart SI-40231 or equivalent) providing both 10 Mbit (10BASE-T) and 100 Mbit (100BASE-TX) protocols. Two LEDs are located inside each RJ-45 connector: a yellow LED to indicate data transmission, and a green LED to indicate data reception.

Depending on application requirements, configuration of switches SW2-1 and SW2-2 may be necessary. See the “J10, J11 Ethernet B/A Connectors Pinout” table below for pin definitions.

J10, J11 Ethernet Connectors Pinout

Pin#	Function	Pin#	Function
1	TX+	4-5	Unused pair, terminated on the ZT 5521
2	TX-	6	RX-
3	RX+	7-8	Unused pair, terminated on the ZT 5521

J12 (Keyboard/Mouse Connector)

J12 is a dual 6-pin DIN connector (AMP 84401-1 or equivalent) providing front-panel connection to standard PS/2 style keyboard and mouse devices. Keyboard and mouse signals are also directed out J3 for use by an optional rear-panel transition board (such as the ZT 4804). See the “J12 Keyboard and Mouse Interface Connector Pinout” table for pin definitions.

J12 Keyboard and Mouse Connector Pinout

Keyboard

Pin#	Function	Pin#	Function
1	KBDAT	4	Vcc (Fused)
2	No Connect	5	KBCLK
3	GND	6	No Connect

Mouse

Pin#	Function	Pin#	Function
1	MSDAT	4	VCC (Fused)
2	No Connect	5	MSCLK
3	GND	6	No Connect

J13, J15, J18, J20 (SDRAM Connectors)

J13, J15, J18, J20 are 168-pin connectors (AMP 390074-6 or equivalent) for the board's SDRAM modules.

J14 (AGP Video Pass-Through Connector)

J14 is a 2-row x 8 pin, 2 mm surface mount socket (Samtec SQT-108-01-L-D or equivalent) used to pass signals from a mezzanine video adapter (such as the ZT 96079) to the J6 Video Interface connector on the front panel. See the "J14 AGP Video Pass-Through Connector Pinout" table below for pin definitions.

J14 AGP Video Pass-Through Connector Pinout

Pin #	Signal	Pin #	Signal
1	RED	9	VCC
2	GRN	10	SGND
3	BLUE	11	NC
4	NC	12	SDA
5	DGND	13	HSYNC
6	RGND	14	VSYNC
7	GGND	15	SCL
8	BGND	16	NC

J19 (I/O Expansion Connector)

J19 is a 100-pin 2 mm connector providing an interface for IDE, floppy, and video signals for test purposes only. See the “J19 I/O Expansion Connector Pinout“ table for pin definitions.

J19 I/O Expansion Connector Pinout

Pin #	A	B	C	D
25	GND	GRNIN	RSVD	RSVD
24	REDIN	GND	RSVD	RSVD
23	GND	BLUIN	RSVD	RSVD
22	VCCVID	GND	GND	OFFBD_PWG
21	GND	HSYNCIN	DDP8	DDP7
20	VSYNCIN	GND	DDP9	DDP6
19	GND	DDCDATIN	DDP10	DDP5
18	DDCCLKIN	VID_EN-	DDP11	DDP4
17	VCC	VCC3	DDP12	DDP3
16	VCC	VCC3	DDP13	DDP2
15	DIGIO7	INDEX-	DDP14	DDP1
14	DIGIO6	WGATE-	DDP15	DDP0
13	DIGIO5	DSKCHG-	N/C	GND
12	DIGIO4	DR0-	GND	PDREQ-
11	DIGIO3	MSEN0	GND	PDIOW-
10	DIGIO2	DR1-	GND	PDIOR-
9	DIGIO1	MTR0-	N/C	PIORDY
8	DIGIO0	DENSL	GND	PDDACK-
7	BDSELMMEZ-	DIR-	HDIO16-	IRQ14
6	+12VDC	STEP-	PDIAG	DAP1
5	+12VDC	WDATA-	DAP2	DAP0
4	GND	TRK0-	CS3P-	CSP1-
3	GND	WP-	GND	IDE_ACT
2	GND	RDATA-	VCC	VCC
1	GND	HDSEL-	XTAT	GND
Pin #	**A**	**B**	**C**	**D**

J22 (CompactFlash Connector)

J22 is a 50-pin Surface Mount Right Angle CF Card Slot Header (AMP 120615-1 or equivalent) designed to accommodate a CompactFlash card. Refer to the CompactFlash Specification, Revision 1.X for pinout and device information. The topic "CompactFlash" in Appendix F, “Data Sheet Reference,” provides a link to the CompactFlash Association’s website.

J23 (PCI Bus 0 Monitoring)

J23 is used by Ziatech to monitor PCI Bus 0. No user function exists.

J24 (AGP Video Mezzanine Interface Connector)

J24 is a 114-pin AMP Mictor Series 25 receptacle (AMP 767054-3 or equivalent) providing an interface for a Ziatech AGP Video Mezzanine Adapter (such as the ZT 96079). Refer to the “J24 AGP Video Mezzanine Interface Connector Pinout” table below for pin definitions.

J24 AGP Video Mezzanine Interface Connector Pinout

Column A Pins	Signal	GND Pins	Signal	Column B Pins
1	spare	GND	12 V	1
2	5.0 V	—	spare	2
3	5.0 V	—	Reserved*	3
4	GND	—	GND	4
5	USB+	GND	USB-	5
6	GND	—	GND	6
7	INTB#	—	INTA#	7
8	CLK	—	RST#	8
9	GND	GND	GND	9
10	REQ#	—	GNT#	10
11	VCC3.3	—	VCC3.3	11
12	ST0	—	ST1	12
13	ST2	GND	Reserved	13
14	RBF#	—	PIPE#	14
15	spare	—	spare	15
16	SBA0	—	SBA1	16
17	VCC3.3	GND	VCC3.3	17
18	SBA2	—	SBA3	18
19	SB_STB	—	Reserved	19
20	SBA4	—	SBA5	20
21	SBA6	GND	SBA7	21
22	GND	—	GND	22
23	AD31	—	AD30	23
24	AD29	—	AD28	24

J24 AGP Video Mezzanine Interface Connector Pinout (continued)

Column A Pins	Signal	GND Pins	Signal	Column B Pins
25	VCC3.3	GND	VCC3.3	25
26	AD27	—	AD26	26
27	AD25	—	AD24	27
28	AD_STB1	—	Reserved	28
29	AD23	GND	C/BE3#	29
30	Vddq3.3	—	Vddq3.3	30
31	AD21	—	AD22	31
32	AD19	—	AD20	32
33	AD17	GND	AD18	33
34	C/BE2#	—	AD16	34
35	Vddq3.3	—	Vddq3.3	35
36	IRDY#	—	FRAME#	36
37	VCC3.3	GND	VCC3.3	37
38	DEVSEL#	—	TRDY#	38
39	Vddq3.3	—	STOP#	39
40	PERR#	—	Spare	40
41	GND	GND	GND	41
42	SERR#	—	PAR	42
43	VCC3.3	—	VCC3.3	43
44	C/BE1#	—	AD15	44
45	Vddq3.3	GND	Vddq3.3	45
46	AD14	—	AD13	46
47	AD12	—	AD11	47
48	AD10	—	AD9	48
49	AD8	GND	C/BE0#	49
50	Vddq3.3	—	Vddq3.3	50
51	AD_STB0	—	Reserved	51
52	AD7	—	AD6	52
53	AD5	GND	AD4	53
54	AD31	—	AD2	54
55	Vddq3.3	—	Vddq3.3	55
56	AD1	—	AD0	56
57	SMB0	GND	SMB1	57

J25 (PLD Programming Connector)

J25 is the In-System-Programming (ISP) port used during the manufacturing process to program on-board PLD devices. No user function exists.

J26 (Speaker Connector)

J26 is a 2-pin connector (Molex 39-27-0021 or equivalent) for an optional PC speaker. See the “J26 Speaker Connector Pinout” for pin definitions.

J26 Speaker Connector Pinout

Pin#	Function
1	VCC
2	SPK2

B. RESET

This appendix discusses the various reset types and reset sources on the ZT 5521. Because many embedded systems have different requirements for board reset functions, the incorporation of this sub-system on the ZT 5521 has been designed to provide maximum flexibility.

RESET TYPES AND SOURCES

The ZT 5521's five reset types are listed below. The sources for each reset type are detailed in the following topics.

- **Backend Power Down:** The backend logic is powered off. All on-board devices are reset and PCIRST# is driven on the system backplane.
- **General Reset:** All on-board devices are reset and PCIRST# is driven on the System backplane.
- **Hard Reset:** All on-board devices are reset and PCIRST# is driven on the System backplane.
- **Soft Reset:** CPU initialization only. Other devices are not reset.
- **NMI:** Non-maskable interrupt. Though not a reset in the strict sense, an NMI can have the same effect as other resets.

Backend Power Down Sources

Board Extraction

When a board is extracted from an enclosure (specifically, when the short “board select” pin is disengaged), the Hot Swap controller unconditionally removes backend power from the board and holds the ZT 5521 in reset.

Low Voltage

When the 3.3 V, 5 V, and 12 V supply voltages are detected as below an acceptable operating limit, the Hot Swap controller unconditionally removes backend power and holds the ZT 5521 in reset.

Overcurrent Fault

If a power fault condition (overcurrent) is detected, the Hot Swap controller removes backend power and turns the “Fault/Power” LED indicator red. The ZT 5521 is held in reset.

General Reset Sources

Push-Button Reset

When the System Reset button (S1) is pressed, the ZT 5521 resets itself and drives PCI RST on both CompactPCI buses. Sources for push-button reset include:

- Front panel push-button switch (S1)
- Programmable Watchdog Timer
- CompactPCI bus push-button reset signal, PRST# (J5-C17)
- Optional ZT 4804 Rear-Panel Transition Board push button switch S2 (J3-A4)
- Software programmable System Register 7 (Port E5h, bit 6).

Hard Reset Sources

System Register CF9h (PIIX4 Reset Control Register)

The PIIX4 Reset Control Register can generate a hard reset or a soft reset (through bits 1 and 2). During a hard reset, the PIIX4 asserts CPURST, PCIRST#, and RSTDRV, and resets its core and suspend well logic.

Soft Reset Sources

System Register CF9h (PIIX4 Reset Control Register)

The PIIX4 Reset Control Register can generate a hard reset or a soft reset (through bits 1 and 2). During a soft reset, the PIIX4 asserts INIT to the CPU.

Keyboard Controller Reset

The keyboard controller generates a keyboard controller reset when FEh is written to port 64h. This causes the PIIX4 to assert INIT to the CPU.

Keyboard Ctrl-Alt-Del

Simultaneously pressing these keys calls a BIOS function that reboots the system.

Note: This method does not work under operating systems that trap calls to this BIOS function.

NMI Sources

Front-Panel Abort Push-Button (S2)

The ZT 5521 provides a push-button (S2) on the front panel to force an NMI interrupt to the host CPU controller.

The Watchdog Timer (Port 79h)

The watchdog timer can be programmed through System Register 2 (Port 79h, bit 4) to generate a non-maskable interrupt if it is not strobed within a given time-out period. The watchdog timer is discussed in Chapter 5.

Rear-Panel Transition Board (ZT 4804) NMI Push Button

An NMI push-button is available on the optional ZT 4804 RPIO Transition Board. Pressing this button causes the ZT 5521 to generate a non-maskable interrupt.

C. SYSTEM REGISTERS

The ZT 5521 provides several system registers to control and monitor a variety of functions on the ZT 5521. Normally, only the system BIOS uses these registers, but they are documented here for application use as needed. Take care when modifying the contents of these registers as the system BIOS may be relying on the state of the bits under their control.

System Registers 1 and 2 are in an on-board PAL device and accessible at ports 78h and 79h, respectively. System Registers 3 through 7 are in the on-board 16C50A Digital I/O ASIC device and accessible at ports E1h through E5h. As Digital I/O ASIC inputs, these registers are inverting; thus, a logic high (+5 V) is read as a logic low.

SYSTEM REGISTER DEFINITIONS

The System Registers are accessible as follows:

	I/O Address	Register Name	Default Value	Access	Size
PAL	78h	System Register 1	0x00	R/W	8 bits
	79h	System Register 2	0x00	R/W	8 bits
Digital I/O ASIC	E1h	System Register 3	0x00	RO	8 bits
	E2h	System Register 4	0x00	R/W	8 bits
	E3h	System Register 5	0x00	RO	8 bits
	E4h	System Register 6	0x00	R/W	8 bits
	E5h	System Register 7	0x00	R/W	8 bits

System Register 1 (78h)

I/O Address: 78h
Default Value: 0x00
Size 8 bits
Attribute: R/W

Bit	Description	Default
7:4	**Flash Paging**. These bits are used to map one of the 16 pages of flash memory into the flash window, as shown in the table below. These pages are numbered 0 - 15, with page 0 being at the lowest address of the device and page 15 being at the highest address. Flash programming is discussed in more detail in Chapter 6.	0
3	**Reserved**. This bit should always be written as 0	0
2	**Device Select**. 0=standard flash, 1=optional flash	0
1	**Flash Write-Protection**. 0=write-protected, 1=writable. Flash can be hardware write-protected through switch SW2-3.	1
0	**Reserved**. This bit should always be written as 0	0

Bit 7	Bit 6	Bit 5	Bit 4	Page
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
…	…	…	…	…
…	…	…	…	…
1	1	1	1	15

System Register 2 (79h)

I/O Address: 79h
Default Value: 0x00
Attribute: R/W

Bit	Description
7	**Reset Detection Bit** Read Value: 0=Watchdog has not timed out since power up or since this bit was last cleared; 1=Watchdog timed out and the Reset output was asserted. Bit 5, Reset Enable (below) must be set for this bit to assert. Write Value: 0=Clear this bit; 1 = No effect. Power Up Value: =0.
6	**NMI Detection Bit** Read Value: 0=Watchdog has not timed out since power up or since this bit was last cleared; 1=Watchdog timed out and the NMI output was asserted. Bit 4, NMI Enable (below) must be set for this bit to assert. Write Value: 0=Clear this bit; 1=No affect. Power Up Value: =0.
5	**Reset Enable** Read Value: 0, 1=value written to the bit. Write Value: 0=Reset operation of the watchdog is not enabled. When the watchdog times out, neither the Reset Detection status nor the Reset output will be asserted. 1=Reset operation of the watchdog is enabled. When and if the watchdog times out: • The Reset output asserts for one clock count. • The RstDet status bit goes high and stays high until cleared by software. • Reset action actually occurs a clock cycle after the NMI action. Power Up Value: =0. Value After Timeout =0. If “PCI Reset” occurs for non-watchdog reasons, value =0.

(System Register 2 - 79h continued)

4	**NMI Enable** Read Value: Reflects the value written to the bit. Write Value: 0=NMI operation of the watchdog is not enabled. When the watchdog times out, neither the NMI status bit nor the NMI output is asserted. 1=NMI operation of the watchdog is enabled. When and if the watchdog times out: • The NMI output asserts for one clock count. • The NMI status bit goes high and stays high until cleared by software. • NMI action actually occurs a clock cycle before the Reset action to give the system software some time to shut down. Power Up Value: =0. Value After Timeout =0. If "PCI Reset" occurs for non watchdog reasons, Value =0.
3	**Reserved:** This bit is reserved. It has no user function and should always be written as 0. Power Up Value =0.
2:0	**Terminal Count (TrmCnt2…TrmCnt0):** Read Value: Reflects the value written to the bit. Write Value: These bits determine the terminal count of the watchdog timer in seconds. Their value has the following meaning: Bit 2, Bit 1, Bit 0. The minimum timeout period is given. The watchdog times out in no less than the minimum value. The nominal timeout period is 30% longer than the minimum. 000 = 250 ms 100 = 32 s 001 = 500 ms 101 = 64 s 010 = 1 s 110 = 128 s 011 = 8 s 111 = 256 s Power Up Value =000

System Register 3 (E1h)

I/O Address: E1h
Default Value: 0x00
Size 8 bits
Attribute: RO

Bit	Description
7	**Watchdog NMI Status.** This bit monitors the Watchdog Timer's NMI output. A 0 = watchdog circuit did not generate an NMI, a 1 = watchdog circuit generated an NMI.
6	**ENUM.** This bit reports that a hot swap peripheral card has been installed or removed from the system. This bit should always be written as 0.
5	**FANTACH 2.** The heatsink on the ZT 5521 standard product does not include a fan. However, the rotation of a user-supplied fan can be monitored through this bit. User-written software must read the I/O port at precise time intervals to determine if the fan is working properly. Most fan tachometers have an output rate of approximately 100 Hz; this input therefore changes states approximately every 5 ms. This bit is read as 0 when the fan is not spinning and as 1 when the fan is spinning. If no user-supplied fan is implemented, this bit is read as 0.
4:3	**Power Supply DEG#, FAL#**. These bits monitor the DEG# and FAL# signals on CompactPCI connector J5. See the *CompactPCI Specification, PICMG 2.0, Version 2.1* for more information on these signals.
2	**Reserved.** This bit is reserved and should not be modified by the user.
1	**FANTACH 1.** The heatsink on the ZT 5521 standard product does not include a fan. However, the rotation of a user-supplied fan can be monitored through this bit. User-written software must read the I/O port at precise time intervals to determine if the fan is working properly. Most fan tachometers have an output rate of approximately 100 Hz; this input therefore changes states approximately every 5 ms. This bit is read as 0 when the fan is not spinning and as 1 when the fan is spinning. If no user-supplied fan is implemented, this bit is read as 0.
0	**Reserved.** This bit is reserved and should not be modified by the user.

System Register 4 (E2h)

Address Offset: E2h
Default Value: 0x00
Size 8 bits
Attribute: R/W

Bit	Description
7:4	**Serial # ID.** These bits are used by the built-in diagnostic software for reading board serial numbers. The serial numbers are stored in the DS2401 Silicon Serial Number devices located on CPUs, mezzanine boards, and rear-panel boards, etc., and allow boards to be uniquely identified in a system. Bits 4 - 7 read serial numbers as follows: **Bit 7** = ZT 4804; **Bit 6** =Not Used; **Bit 5** =Not Used; **Bit 4** = ZT 5521 The topic "Board Serial #ID" in Appendix F, “Data Sheet Reference” provides a link to the data sheet for the DS2401 device.
3:0	**Board Revision.** This port is used to read the status of cuttable traces CT10 - CT13 to determine the current board revision (Revision 0 = Fh). The user should not change these cuttable traces since these values may be used by the system BIOS.

System Register 5 (E3h)

Address Offset: E3h
Default Value: 0x00
Size 8 bits
Attribute: RO

Bit	Description
7	**Flash Write-Protect Status**. This bit reads back the status of switch SW2-3. A 0 means that the flash is **not** write-protected by SW2-3; a 1 means the flash **is** write-protected by SW2-3.
6:4	**Reserved.** These bits are reserved and should not be modified by the user. Do not write software that requires these bits to be read as 0.
3:0	**Software Configuration**. These bits are used to provide configuration information to the user's software by monitoring the status of the switches listed below. An open switch reads back a 0; a closed switch reads back a 1. The bits correspond to switch positions as follows: **Bit 0** = SW1-2; **Bit 1** = SW1-3; **Bit 2** = SW1-4; **Bit 3** = SW3-1

System Register 6 (E4h)

Address Offset: E4h
Default Value: 0x00
Size 8 bits
Attribute: R/W

Bit	Description
7:5	**Reserved.** These bits are reserved and should not be modified by the user.
4:0	**Geographic Addressing.** CompactPCI defines several signal additions to the PCI specification. One of these is GA[4..0], used for geographic addressing on the backplane. Geographic addressing uniquely differentiates each board based upon the physical slot into which it has been inserted. Each backplane connector in a CompactPCI system has a unique encoding for GA[4..0]. See the *CompactPCI Specification, PICMG 2.0, Version 2.1* for more information on geographic addressing. The bits correspond to signals as follows: **Bit 0** = GA0; **Bit 1** = GA1; **Bit 2** = GA2; **Bit 3** = GA3; **Bit 4** = GA4.

System Register 7 (E5h)

Address Offset: E5h
Default Value: 0x00
Size 8 bits
Attribute: R/W

Bit	Description
7	**Video/Keyboard Enable**. This bit selects the location for the video signal output. A 1 routes video signals to the on-board VGA connector J17 and keyboard signals to connector J16; a 0 disables the video and keyboard signals.
6	**Software Reset**. This bit sends a software reset to the CPU.
5:4	**Reserved.** These bits are reserved and should not be modified by the user.
3:2	**User LED 1.** These bits set the status of User LED 1. Bit 2 sets the LED's color as follows: 0=red; 1=green. Bit 3 enables/disables the driver for the LED as follows: 0=driver disabled; a 1=driver enabled.
1:0	**User LED 2.** These bits set the status of User LED 2. Bit 0 sets the LED's color as follows: 0=red; 1=green. Bit 1 enables/disables the driver for the LED as follows: 0=driver disabled; a 1=driver enabled.

D. THERMAL CONSIDERATIONS

This appendix describes the thermal requirements for reliable operation of a ZT 5521 CPU board implementing the Pentium II processor†. It provides specifics regarding basic thermal requirements and monitoring the board and processor temperature.

THERMAL REQUIREMENTS

The ZT 5521 comes from the factory with an integrated heatsink for cooling the processor module. The maximum processor core temperature must not exceed 90º C. The heatsink allows a maximum ambient air temperature of 45º C with 250 linear feet per minute (LFM) of airflow. The maximum power dissipation of the CPU is 32 W.

Caution: External airflow must be provided at all times during operation to avoid damaging the CPU module. Ziatech strongly recommends use of a fan tray below the card rack to supply the external airflow.

The "Thermal Requirements" table following shows the relationship between ambient air temperature, board temperature, and processor core temperature.

Thermal Requirements

External Ambient Air Temperature (°C)	Temperature Around the Board (°C)	Pentium II Processor Core Temperature (°C)
0	13	44
5	18	49
10	22	54
15	27	60
20	33	65
25	37	69
30	42	74
35	47	79
40	52	84
45	**57**	**89 = maximum**
50	63	95

† Thermal data for ZT 5521 boards implementing the Pentium III processor was not available at the time this manual was produced. Contact Ziatech for additional information.

TEMPERATURE MONITORING

Because reliable long-term operation of the ZT 5521 depends on maintaining proper temperature, Ziatech strongly recommends that you verify the operating temperature of the processor module and processor core in your final system configuration.

The Pentium III processor† incorporates an on-die diode that can be used to monitor the processor's die temperature. The ZT 5521 includes a Maxim 1617 Remote/Local Thermal Temperature Sensor to monitor the die temperature of the processor for thermal management purposes. The ZT 5521's BIOS can read the temperature via the SMB Data Interface to determine if clock throttling is necessary to control the temperature of the CPU.

Use the BIOS Diagnostics to obtain readings of the module and processor core temperature. To access the BIOS Diagnostics, enter the BIOS Setup Utility by pressing **F2** during the system RAM check at boot time and select the Diagnostics tab. This area of the Setup Utility allows you to view the "Processor Core" and "PCB" temperatures. As shown in the "Thermal Requirements" table, the maximum processor core temperature must not exceed 90º C.

† Thermal data for ZT 5521 boards implementing the Pentium III processor was not available at the time this manual was produced. Contact Ziatech for additional information.

E. ZT 5521 vs. ZT 5520 TECHNICAL DIFFERENCES

This appendix describes the technical differences between the ZT 5521 and the ZT 5520 CPU boards. It includes information to help existing ZT 5520 customers adapt their applications to the ZT 5521.

FUNCTIONAL HARDWARE DIFFERENCES

Existing ZT 5520 customers should be aware of the functional hardware differences between the ZT 5520 and the ZT 5521 CPU boards. These differences are detailed in the following topics.

Processors

ZT 5520: Dual 200 MHz Pentium Pro Processors

ZT 5521: Slot 1 Pentium II processor or Pentium III processor

Symetric multiprocessing code written for the dual processor ZT 5520 will not work on the single processor ZT 5521.

RAM

ZT 5520: 512 MB DRAM maximum

ZT 5521: 1024 MB SDRAM maximum

Flash ROM Module

ZT 5520: Intel Flash (2-8 MB; P/N DD28F032SA)

ZT 5521: AMD Flash (4-8 MB; P/N AM29F032B)

- Both flash types are read in the same manner, but each has unique programming and erase algorithms. Refer to the flash device data sheet for details.
- Intel devices support "block locking" (write-protection of individual 64K blocks). AMD devices do not.
- AMD devices must be write-enabled in order to accept any commands, including the “Identify” command. Intel devices only require write-enabling in order to perform programming or erase commands.

Video

ZT 5520: PCI video (zPM11) operating at 33 MHz.

ZT 5521: AGP video (ZT 96079) supports 32 bits of data and operates 66 MHz.

Depending on the operating system, video device drivers used with the ZT 5520 may not work with the ZT 5521.

Watchdog Timer

ZT 5520: Single-stage watchdog

ZT 5521: Two-stage watchdog. Sample code to help you learn how to program the watchdog is provided in Chapter 5, "Watchdog Timer."

Ethernet

Be aware that the zPM15 Fast Ethernet LAN PCI Mezzanine Adapter does not attach . Also, unless you are running VxWorks, drivers for the zPM15 Adapter (DEC 21140A) will not work with the ZT 5521's Ethernet devices (Intel 21143).

ZT 5520: Single Ethernet channel is optional and provided by the zPM15 Fast Ethernet LAN PCI Mezzanine Adapter (DEC 21140A).

ZT 5521: Dual Ethernet channels are standard and provided by two Intel 21143 PCI-Ethernet Bridges and two onboard RJ-45 connectors. The zPM15 does not attach to the ZT 5521 CPU board. Also, unless you are running VxWorks, drivers for the zPM15 will not work with the ZT 5521's Intel 21143 device.

Mouse

ZT 5520: Mouse available to rear-panel only.

ZT 5521: Mouse available to front- and rear-panel.

REAR-PANEL I/O SIGNALING DIFFERENCES

The ZT 5520 and ZT 5521 CPU boards have different pinouts for their respective J3 rear-panel I/O connectors. These differences are especially significant for systems that include a ZT 5980 System Utility Board and/or a ZT 4800 Rear-Panel Transition I/O board. To avoid damage to your hardware and to ensure proper operation of your system, carefully review the following topics.

LPT1 Signaling

Unlike the ZT 5520, the ZT 5521 CPU does not direct LPT1 signals out the J3 Rear-Panel I/O connector. Therefore, if your system includes a ZT 5980 System Utility Board and/or a ZT 4800 Rear-panel I/O board, be aware that the LPT1 interfaces on these boards will not work with the ZT 5521 CPU, and hardware that may be connected to these interfaces can be damaged in a ZT 5521 implementation.

Warning: ZT 5521 users should not connect hardware to the ZT 5980 or ZT 4800 LPT1 interfaces!

The relevant portion of each board's J3 pinout is shown below.

ZT 5520

Pin#	A	B	C	D	E	F
9	WGATE-	**ERR-**	**AFD**	**BUSY**	USB+	GND
8	**PE**	**SLIN-**	VCC	**STB-**	USB-	GND
7	**PPD7**	**PPD6**	**PPD5**	**PPD4**	**INIT-**	GND
6	**PPD3**	**PPD2**	**PPD1**	**PPD0**	**ACK-**	GND
5	ABORT-	MSDAT	SPKR	KBDAT	**SLCT**	GND

ZT 5521

Pin#	A	B	C	D	E	F
9	WGATE-	**RXBACKA-**	**J3GND**	**NC**	USB+	GND
8	**J3GND**	**RXBACKA+**	SW-VCC	**TXCTB**	USB-	GND
7	**RXBACKB-**	**J3GND**	**TXBACKB-**	**TXCTA**	**J3GND**	GND
6	**RXBACKB+**	**J3GND**	**TXBACKB+**	**J3GND**	**TXBACKA-**	GND
5	ABORT-	MSDAT	SPKR	KBDAT	**TXBACKA+**	GND

IDE Signaling

The ZT 5520 and ZT 5521 CPU boards handle rear-panel IDE signaling differently. These differences are described in the following topics. The relevant portion of each board's J3 pinout is shown below.

ZT 5520

Pin#	A	B	C	D	E	F
19	PWRGD	**ISAIO16-**	**IORDY**	**MIRQ0**	**IRQ14**	GND
18	**CS3S-**	**CSIS-**	**CS3P-**	**CS1P-**	**DDAK1-**	GND
17	DD15	DD14	DD13	DD12	**DDRQ1**	GND
16	DD11	DD10	DD9	DD8	**DDAK0-**	GND
15	DA0	DA1	SW-VCC	DA2	**DDRQ0**	GND
14	DD7	DD6	DD5	DD4	**DIOW-**	GND
13	DD3	DD2	DD1	DD0	**DIOR-**	GND

ZT 5521

Pin#	A	B	C	D	E	F
19	PWRGD	**HDIO16-**	**SIORDY**	**SMBALRT**	**IRQ15**	GND
18	**SMBDATA#**	**SMBCLK-**	**CS3S-**	**CS1S-**	**RP_ID**	GND
17	DD15	DD14	DD13	DD12	**NC**	GND
16	DD11	DD10	DD9	DD8	**SDDACK**	GND
15	DA0	DA1	SW-VCC	DA2	**SDDRQ**	GND
14	DD7	DD6	DD5	DD4	**SDIOW-**	GND
13	DD3	DD2	DD1	DD0	**SDIOR-**	GND

Channels

While the ZT 5520 directs **both** primary and secondary IDE channels out connector J3, the ZT 5521 CPU directs **only the secondary** IDE channel out J3. Also, the secondary IDE channel on the ZT 5521 is mapped to the pins that carried the primary IDE channel on the ZT 5520's J3 connector. Therefore, using a ZT 5521 CPU with a ZT 5980 System Utility Board and/or a ZT 4800 Rear-panel I/O board affects rear-panel IDE interfaces as follows:

5980 System Utility Board

- J5 and J10 become **secondary** IDE interfaces
- J11 no longer functions. *Do not connect a drive to J11.*

4800 Rear-Panel I/O Transition Board

- J4 becomes a **secondary** IDE interface
- J5 no longer functions. *Do not connect a drive to J5.*

Drive Letter Designation

Depending on your operating system, the drive letter designation of drives connected to the ZT 5980 System Utility Board and/or the ZT 4800 Rear-Panel I/O Transition Board may be different when using a ZT 5521 CPU board.

BIOS DIFFERENCES

There are several important differences between the *Ziatech Industrial BIOS* installed on the ZT 5520 and the *Ziatech Embedded BIOS* installed on the ZT 5521. Some of these differences are discussed below.

Size: At 320 KB, the newer *Ziatech Embedded BIOS* is more than twice the size of the older 128 KB *Ziatech Industrial BIOS*. For this reason, it is important that you know the size of any code or programs contained in the Flash ROM module on your ZT 5520 boards. Data that fit in your ZT 5520's flash device could, if too big, overwrite portions of the BIOS contained on your new ZT 5521 boards when ported over.

Accessing the BIOS Setup Utility: In the *Ziatech Embedded BIOS* the BIOS Setup Utility is accessed by pressing the **F2** key during the system RAM check at boot up time (as opposed to the **S** key, as in the Ziatech Industrial BIOS).

No ROM DOS Support: Unlike the ZT 5520's *Ziatech Industrial BIOS*, the ZT 5521's *Ziatech Embedded BIOS* does not include Microsoft ROM DOS. This change eliminates the DOS flash drive (P:) previously supported with the *Ziatech Industrial BIOS*. However, like the ZT 5520, the ZT 5521 also allows a portion of flash memory to be used for storing bootable operating system images (such as those created with the

VxWorks Development Toolkit). Some operating systems, such as VxWorks, that support solid state drives on the ZT 5520 may also support solid state drives for the ZT 5521, although updated drivers are required.

System Information Table: The ZT 5521's *Ziatech Embedded BIOS* includes a System Information Table that describes the type and size of flash, the size of the BIOS image, and other useful information about the CPU board on which the BIOS is running. This table allows the elimination of most or all compile-time options related to flash. The *Ziatech Industrial BIOS* installed on ZT 5520 CPU boards does not have a system information table.

PROGRAMMING ISSUES

- In most cases, ZT 5520 applications that do not program any chipset registers or flash memory directly will not require modification in order to run on the ZT 5521. However, configurable board options on the ZT 5521 such as Ethernet and video adapters will require new drivers to be installed.
- The COM1, COM2, and LPT1 peripherals are in the same I/O locations on both boards.
- The available interrupt routing selections for all legacy devices (COM ports, IDE drives, keyboard, mouse, floppy drives, system clocks, and NMI) are the same on both boards, as they are for all PC compatibles. PCI interrupts are, by definition, dynamically configured. Almost all PCI drivers will properly share interrupts and properly interrogate PCI configuration headers in order to determine interrupt routing, and will work without modification. Any non-PCI-compliant drivers with hard-coded interrupt routing will require modification to work on the ZT 5521.
- Software configuration of interrupt routing is different between the ZT 5520 and the ZT 5521. The ZT 5521's BIOS SETUP Utility provides more control over the configuration of interrupt routing.

F. DATA SHEET REFERENCE

This appendix provides links to data sheets, standards, and specifications for the technology designed into the boards in your system.

AGP VIDEO

For more information on Intel's Accelerated Graphics Port (AGP) technology, visit their website at:

http://developer.intel.com/technology/agp/

BOARD SERIAL # ID

Refer to the Dallas Semiconductor™ *DS2401 Silicon Serial Number* data sheet for more information about the DS2401 device. The data sheet is in Adobe® Acrobat® format (PDF) and is available online at:

http://www.dalsemi.com/DocControl/PDFs/pdfindex.html

CompactFlash

For more information about CompactFlash, visit the CompactFlash Association's website at:

http://www.compactflash.org/

CompactPCI

The *CompactPCI Specification, PICMG 2.0, Version 2.1* can be purchased from PICMG (PCI Industrial Computers Manufacturers Group) for a nominal fee. A short form specification in Adobe® Acrobat® format (PDF) is also available on PICMG's website at:

http://www.picmg.org/gcompactPCI.htm

ETHERNET

Refer to the Intel *21143A PCI/CardBus 10/100-Mb/s Ethernet LAN Controller* data sheet for more information on the Ethernet LAN Controller. The data sheet is available online at:

http://developer.intel.com/design/network/products/lan/controllers/21143.htm

Refer to the Intel LXT970 Dual-Speed Fast Ethernet Transceiver data sheet for more information on the ZT 5521's Ethernet Physical Interface. The data sheet is available online at:

http://developer.intel.com/design/network/products/lan/docs/LXT970A_docs.htm

PCI-TO-PCI BRIDGE

For more information about the Intel 21154 PCI-to-PCI bridges used on the ZT 5521 CPU, visit the Intel website addressed below.

http://developer.intel.com/design/bridge/datashts/

PENTIUM III PROCESSOR

For more information about the Intel Pentium® III Processor, see the Intel *Pentium® III Processor for the PGA370 Socket at 500 MHz to 1 GHz* data sheet and the *Pentium III Processors Specification Update*. Both documents are available online at:

http://developer.intel.com/design/pentiumiii/datashts/

http://developer.intel.com/design/pentiumiii/specupdt/

PIIX4

For more information on the following ZT 5521 functions, refer to the Intel *82371AB (PIIX4) PCI ISA IDE Xcelerator* data sheet and the Intel *82371EB (PIIX4E)* specification update.

- USB
- Counter/Timers
- DMA controllers
- Real-Time Clock
- Interrupt controllers
- Reset Control register
- EIDE Interface Controller

The documents are in Adobe Acrobat format (PDF) and are available online at:

http://developer.intel.com/design/chipsets/datashts/index.htm

http://developer.intel.com/design/chipsets/specupdt/index.htm

SDRAM

The ZT 5521 supports 128 and 256 MB double-sided SDRAM DIMMs with ECC. Specifications for the SDRAM modules are in Adobe Acrobat format (PDF) and are available online at:

http://developer.intel.com/technology/memory/pcsdram/

SUPERI/O™

Refer to the National Semiconductor *PC87309 SuperI/O Plug and Play Compatible Chip in Compact 100-Pin VLJ Packaging* data sheet for more information on the following ZT 5521 functions:

- Floppy Disk controller
- Serial Port controller
- Mouse and Keyboard controller
- Parallel Port

The data sheet is in Adobe Acrobat format (PDF) and is available online at:

http://www.national.com/ds/PC/

G. POWER SUPPLIES AND HOT SWAP CIRCUITRY

HOT SWAP CIRCUITRY

Ziatech hot swap products, such as the ZT 5521, are essentially electrically isolated from the backplane when installed or removed. This prevents transients from corrupting backplane communication when a product is removed or installed while the system is operating.

This circuitry has several consequences in the way in which the boards power up. One is the ability of the circuit to monitor the power supply voltages necessary for proper operation of the product. Until the proper voltages are present, the ZT 5521 will not power up. This creates a concern when using power supplies that require a minimum load to start up.

THE POWER SUPPLY PERSPECTIVE

Power supplies typically have two different minimum load requirements for the primary output to operate properly. The first requirement is the load necessary for the power supply to start up. This is typically on the order of 100-200mA.

The second minimum load requirement is the regulation requirement and must be met to guarantee that the auxiliary outputs of the power supply regulate properly if they are fully loaded when the primary output is not. This is typically specified as 10% of the maximum output capability of the primary output. In a hot swap system, it is the minimum start up load requirement that is of concern.

In a pure hot swap system, the power supply essentially sees no load even after the input power to the system is applied. This is because the hot swap circuitry remains disabled until the voltage levels reach the appropriate value. The power supply never generates the proper voltage until it sees a load. They both wait for each other and the system never powers up.

When configuring a pure hot swap system, minimum start up loads for the power supply must be considered. This can be accomplished in a number of ways. The most direct solution is to include a simple power resistor in the system to provide the start up load necessary for the supply.

ZIATECH POWER SUPPLIES

The power supplies that Ziatech currently provides have a minimum start up load and a minimum guaranteed regulation load. These are:

Start up load: +5V @ 100 mA

Regulation: +5V @ 2.5 A

These requirements should be met for EACH SUPPLY in the system. In a hot swap system with four power supplies, a *minimum* load of 400 mA on the +5V output must be present to guarantee that the power supplies start up properly.

H. AGENCY APPROVALS

This appendix presents agency approval and certification information for the ZT 5521 CPU Board with Pentium III Processor.

UL 1950 CERTIFICATION

Underwriters Laboratories, Inc.®

Safety: UL Safety of Information Technology Equipment, including Electrical Business Equipment IEC 950 and UL 1950 (UL file # E179737)

CE CERTIFICATION

The ZT 5550 meets intent of Directive 89/336/EEC for Electromagnetic Compatibility & Low-Voltage Directive 73/23/EEC for Product Safety. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities:

EN 50081-1 Emissions:

EN 55011	Class A Radiated CISPR Pub 22
EN 605555-2	AC Power Line Harmonic Emissions CISPR Pub 22

EN 50082-1 Immunity:

EN 61000 4-2	Electro-static Discharge (ESD)
EN 61000 4-3	Radiated Susceptibility 30 to 100 MHz
ENV 50204	900 MHz Carrier
EN 61000 4-4	Electrical Fast Transient Burst (EFTB)
EN 61000 4-5	Surge, per Power Cord
EN 61000 4-6	Conducted Immunity 150 KHz to 30 MHz
EN 61000 4-8	Power Frequency Magnetic Fields
EN 61000 4-11	Voltage dips, Variations, & Short Interruptions

Low Voltage Directive 73/23/EEC:

UL 1950/EN 60950	Safety of Information Technology Equipment, Including Electrical Business Equipment

FCC REGULATORY INFORMATION

Regulatory information Federal Communications Commission (FCC) (USA only)

Warning: This equipment has been tested and found to comply with the limits for a Class A or B digital device, pursuant to FCC 47 CFR Part 15, Subpart B, Class A or B of the FCC Rules. This equipment generates and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

Ziatech Corporation system RFI and Radiated Immunity tests were conducted with Ziatech Corporation-supported peripheral devices and Ziatech Corporation-shielded cables. Changes or modifications not expressly approved by Ziatech Corporation could result in EMI interference. FCC compliance was achieved under the following conditions:

- Shielded signal cables and a shielded power cord.
- Shielded cables on all I/O ports.
- Cable shields connected to earth ground via metal shell connectors.
- Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.
- Front panel screws properly tightened.

For minimum RF emissions, it is essential that the conditions above are implemented; failure to do so could compromise the FCC compliance of the equipment containing the system.

I. CUSTOMER SUPPORT

This appendix offers technical and sales assistance information for this product, and also the necessary information should you need to return a Ziatech product.

TECHNICAL ASSISTANCE

If you have a technical question, please contact Ziatech's Customer Support Service:

- Phone: (805) 783-6004
- Email: tech_support@ziatech.com
- FTP site: ftp://Ziatech.com/Tech_support

SALES ASSISTANCE

If you have a sales question, please contact your local Ziatech Sales Representative or the Regional Sales Office for your area. Addresses, telephone and FAX numbers, and additional information are available at Ziatech's website, located at:

- http://www.ziatech.com.

Corporate Headquarters

1050 Southwood Drive
San Luis Obispo, CA 93401 USA
Tel (805) 541-0488
FAX (805) 541-5088

RELIABILITY

Ziatech takes extra care in the design of the product in order to ensure reliability. The product was designed in top-down fashion, using the latest in hardware and software design techniques, so that unwanted side effects and unclean interactions between parts of the system are eliminated. Each product has an identification number. Ziatech maintains a lifetime data base on each board and the components used. Any negative trends in reliability are spotted and Ziatech's suppliers are informed and/or changed.

RETURNING FOR SERVICE

Before returning any of Ziatech's products, you must phone Ziatech at (805) 783-6003 and obtain a Returned Material Authorization (RMA) number. The following information is needed to expedite a replacement shipment:

- Your company name and address for invoice.
- Your shipping address and phone number.
- The product I.D. number.
- The name of a technically qualified individual at your company familiar with the board failure.

Once you have an RMA number, follow these steps to return your product to Ziatech:

1. Contact Ziatech for pricing if the warranty expired.

2. Supply a purchase order number for invoicing the repair if the warranty expired.

3. Pack the board in **anti-static** material and ship in a sturdy cardboard box with enough packing material to adequately cushion it.

Note: Any product returned to Ziatech improperly packed will immediately void the warranty for that particular product.

4. Mark the RMA number clearly on the outside of the box.

ZIATECH WARRANTY

Warranty information for Ziatech products is available at Ziatech's website, located at http://www.ziatech.com.

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