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Operators Manual

for

Pulse Instruments
Data Acquisition Systems

and

PI-Controller Software

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1. WARRANTY AND SAFETY INFORMATION

1.1. Warranty

Pulse Instruments warrants these products to be free from defects in material and workmanship for a period of one year from date of shipment.

During the warranty period, Pulse Instruments will, at its discretion, repair or replace products or materials returned, freight prepaid, which prove to be defective through normal use.

This warranty does not apply to defects resulting from unauthorized modification misuse, or neglect. This warranty is in lieu of all other warranties expressed or implied, and Pulse Instruments shall not be liable for any consequential damages resulting from the use of this product.

Pulse Instruments will also not warrant the specifications as listed in this manual if other than Pulse Instruments supplied power supplies are used with this system.

1.2. Safety Information

1.2.1. General

The 4005 Acquisition Mainframe and the PI-4008 Analog Power Mainframe use a detachable 3-wire power cord for connection to both the power source and to earth ground. These units are to be connected only to a power source outlet that has provision for properly grounding the plug.

These products are designed to operate from a power source that will not exceed more than 250 volts RMS between the supply conductors or between either supply conductor and ground. A protective ground connection (earth ground) through a ground conductor in the power cord is essential for safe operation.

1.2.2. Grounding

The products are grounded through the grounding conductor in the power cord. It is essential to avoid electrical shock, to have the unit plugged into a properly wired receptacle before using the equipment. If the protective ground is lost, or not connected, all accessible conductive parts of the instruments can render an electrical shock.

1.2.3. Use The Proper Power Cord

Use only the power cord specified for the product. This power cord must be in good condition. The outer insulation of the power cord should not be frayed, cut, broken, or melted. The receptacle and plug ends should be in good condition such that they tightly fit into the respective connections.

To avoid personal injury **do not operate these instruments with the product covers removed.** Only qualified personnel should perform any procedures with the instrument power on and the covers off. Service on these instruments should only be performed by authorized Pulse Instruments personnel. Unless permission to service is granted by Pulse Instruments, any service performed on these instruments could void all warranty claims.

1.2.4. Fuses

The PI-4005 and PI-4008 use slow blow fuses designed for general circuit protection. Be certain that input power is disconnected before checking or replacing the fuses.

Use only a fuse of proper type, voltage, and current ratings. Never install a fuse of a higher rating than specified for the instrument.

1.2.5. servicing precautions

Do not service units without supervision. When internal calibration is performed another person capable of rendering assistance and first aid should be present.

Use care when performing any procedure with the power on. Dangerous Voltage exist at several points within the instruments. **Always disconnect or turn off power before removing protective panels, or removing PC cards from the instruments.**

1.3. Maintenance

1.3.1. Removal Of Instrument Covers

Dangerous potentials exist at several points in the instrument. When an instrument must be operated with the top cover off, **do not touch exposed connections or components**. Some transistors have voltage present on their cases. **Always disconnect the AC power form the instrument before cleaning.**

1.3.2. PI-4005 Instrument Cover Removal

The top and bottom covers of the PI-4005 are held in place by hidden sliding latches. To remove the cover, push the latch releases located at the top and bottom of the rear panel. There is a latch release for each side of the cover. After disengaging the latches, lift the cover straight up.

To reinstall, align the cover with the latch releases and push straight down on the cover. Make sure the handle clearance cut outs on the cover lip are at the front panel.

1.3.3. PI-4008 Analog Power Mainframe Cover Removal

To remove the top cover of the PI-4008, remove the six screws around the sides of the top cover. Lift the cover straight up.

DO NOT try to remove the bottom cover of the instrument. This pan is an integral part of the structure of the instrument, and should only be removed in the event of major service.

Reinstall the top cover by reversing the removal procedure. Make sure the venting holes in the cover are to the rear of the instrument. To protect the interior of the unit from dust and remove personnel shock hazards, do not operate with the top cover off.

1.3.4. PI-4007 Preamplifier Cover Removal

To remove the top cover of the PI-4007 Preamplifier Module, remove the eight screws around the top. DO NOT remove the bottom cover of the unit. The bottom cover is used to mount the board via snap-top standoffs. To replace the cover, align the reference data on the top cover with the appropriate connectors and replace the screws.

To protect the interior electronics from dust, moisture and other contaminates, do not operate the preamplifier module with the cover off.

You will note that both the top and bottom covers have a return lip with two holes on each end. The purpose of the returns is to facilitate stacking of the modules. The top cover holes are tapped for 2-56 screws, which can be used to secure any number of modules together.

1.4. Preventative Maintenance

To enhance the reliability of the system components it is recommended that a periodic preventative maintenance program be established for the PI-4005 Data Acquisition System. The frequency of preventative maintenance will be determined by the environmental conditions. It is recommended that preventative maintenance be performed no less than every six months.

1.4.1. Cleaning The Instrument

Avoid using chemical cleaning agents that might damage plastic or rubber parts.

1.4.2. PI-4005/PI-4008 Air Filter Removal And Cleaning

The air filters on the PI-4005/PI-4008 instruments should be checked visually every few weeks. Dirty filters should be cleaned or replaced. If the equipment is operated under severe conditions more frequent inspection of the air filters may be required.

If a filter needs to be replaced, order the filter directly from Pulse Instruments. For the PI-4005, order Pulse Instruments Part Number RDDA17. For the PI-4008 order Part Number H260053.

1.4.2.1. PI-4005 Air Filter Removal

To remove the PI-4005 filter, remove the two 4-40 Pan Head Phillips screws securing the filter frame to the rear panel. These screws are located at the ends of the filter frame. DO NOT REMOVE THE TWO SMALLER BINDER HEAD SLOTTED SCREWS ON THE FILTER FRAME. Carefully slide the filter frame out of the instrument. The filter is held to the frame by Velcro strips. Simply lift the filter up to remove.

1.4.2.2. PI-4008 Air Filter Removal

To remove the PI-4008 filter, carefully unsnap the filter grille from the outside of the fan on the rear panel.

1.4.2.3. Air Filter Cleaning

Remove the loose dirt from the filter with a stream of hot water.

Submerse the filter in a solution of mild detergent and hot water, allowing it to soak for a few minutes.

Squeeze the filter to wash out any remaining dirt.

Rinse the filter in clean water and let the filter thoroughly dry. This drying process can be accelerated by blowing air from a compressor through the filter.

Reinstall the filter by reversing the procedures in 1.4.2.1 and 1.4.2.2 above.

1.4.3. Cleaning The Interior And Exterior Of The Instruments

When cleaning either the exterior or the interior of the instrument, always disconnect the AC power cord from the instrument.

1.4.3.1. Exterior of Instruments

Loose dust and dirt can be removed from the exterior of the instrument with a soft cloth. A damp cloth and mild detergent or cleaner may be used. Abrasive cleaner should never be used.

1.4.3.2. Interior of Instruments

Cleaning of the instrument's interior could alter the setting on calibration adjustments. Accumulated dust can be removed with low-velocity compressed air. Dirt that has hardened can be removed with as soft brush or a cloth dampened with a solution of water and mild detergent. Make sure the instrument interior is completely dry before reinstalling the top cover, or applying power.

To prevent personal injury and possible damage to the PC cards, always power down both mainframes (PI-4005 and PI-4008) before removing or installing any card.

1.4.4. Subassembly Removal From The Pi-4005 Mainframe

The PI-4005 is designed to allow quick and easy removal, from a completed chassis, of all subassemblies susceptible to component failure.

There are three subassemblies within the chassis that may require removal. These subassemblies are the power supply, the fan subassembly and the DC switching board.

The following procedures describe the removal from the completed chassis. In each procedure, it is assumed the top cover, or both the top and bottom covers are removed from the instrument.

1.4.4.1. Internal Power Supply Removal from PI-4005

Remove the two screws holding the assembly to the bottom panel. Access to these screws requires removal of the bottom cover. Remove the three kepnuts securing the assembly to the front panel. Slide the Mu Metal shield toward the card cage enough to clear the front panel studs and then lift straight up. Move the power supply subassembly toward the card cage, clearing the front panel studs then lift straight up.

The power supply cable does not require disconnection to lift the power supply from the chassis.

To reassemble the power supply to the chassis, reverse the above procedure. Make sure the cable harness is appropriately located in the chassis. Make sure when the Mu Metal shield is reinstalled, the bottom edge of the shield is inserted into the shield locators.

1.4.4.2. PI-4005 Fan Assembly Removal

Remove the fan filter as described in Section 1.4.2.1. The fan assembly is held in place with ten screws (5 top and 5 bottom) accessible at the side panel. After removing these screws, lift the fan subassembly straight up.

To reinstall the fan subassembly, reverse the above procedure. Sandwiched between the side panel and the fan subassembly is a filter grille. This must be aligned with the mounting holes when installing the fan subassembly.

1.4.4.3. PI-4005 DC Switching Board

The DC switching board is held in place by four snap-top standoffs. To remove this board, unsnap the board from the standoffs and lift straight up. The wiring does not require disconnection to lift the DC switching board from the chassis.

To reinstall the DC switching board reverse the above procedure. When reinstalled, make sure the cables are dressed appropriately in the chassis.

2. INSTALLATION

The PI-4005 Data Acquisition System is a complex instrument that is capable of performing many tasks. To use this instrument to its full advantage, a thorough reading of this section of the manual is required.

2.1. Packing And Unpacking

The PI-4005 and PI-4008 Mainframes were shipped to you in foam filled cartons that were designed to withstand normal shipping conditions. If you find any damage to the shipping cartons or any internal damage, please report it to the carrier as soon as possible.

The PI-4005 Acquisition Mainframe was shipped with the following accessories:

1-Operator's Manual
1-Power Cord
1-Set Rack Slides (If unit is Rack Mount Version)

Please contact Pulse Instruments immediately if you find any discrepancies.

DO NOT TURN THE POWER ON UNTIL YOU HAVE READ THE FOLLOWING

2.2. Power Requirements

The Pulse Instruments Model PI-4005 Acquisition Mainframe and the PI-4008 Analog Power Mainframe are designed to operate from either a 120V or 220V power source. The internal power supply is rated for both.

Please verify that the Voltage indicated is correct for your intended application before connecting power cords to the units, or the units to the power source.

2.3. Cooling And Ventilation

To prevent damage or over-heating to your PI-4005/4008, please make certain that there are no obstructions near either unit that would defeat fan operation or function of the air flow vents located around the unit. Adequate air circulation and ventilation are necessary for proper unit operation and instrument life.

All instrument and system fan filter should be cleaned at regular intervals depending upon your operating environment. See Section 1.3.

2.4. Configuration

The PI-4005/4008 is normally supplied in rack mount configuration. If you intend to use the unit for bench top applications only, the factory should be notified at the time of ordering, as removal of the rack mount slide brackets require operations from inside the unit.

The backplane is compatible with the VME specifications on Connector P1, with the exception that +5V standby is not provided. Connector P2 contains connections that are reserved by Pulse Instruments for use in the system. The internal VME motherboard is floating with respect to the case.

The PI-4005 contains 12 VME slots. Up to eight slots (slots 3-10) are to be used for the installation of Acquisition Cards, and the remainder of the slots are to be used for other system cards, such as 40511 Preamplifier Controller Cards (slots 9-11), the 40502 PCI to VME Adapter Card (slot 1), and the PI-4009 Clock Fan Out Card (slot 12).

All printed circuit cards that are supplied as part of your unit were installed in the mainframe and the factory. Changing card locations may affect any software that is written based on previous card locations. The software automatically renumbers the channels based on location in the mainframe. The addresses specified by the DIP switches on the data acquisition cards must increase as the card move up in the mainframe. An error will occur if a card with a larger address is positioned below a card with a smaller address.

2.5. PI-4005 Acquisition Mainframe Rear Panel

The following information is a description of the indicator LED's, Monitoring points and connections to be made on the rear of the PI-4005 Acquisition Mainframe.

The DC Power Cable that is supplied connects form the J202 DC Power connector on the PI-4005 Acquisition Mainframe, to J1 the top connector on the PI-4008 Analog Power Mainframe. The PI-4008 is a four wire (Low and Hi power/sense) system. Only connector J1 carries the power supply sense lines.

2.5.1. VME Adapter Card

The output connectors on the VME Adapter Card (Pulse Instruments Part Number 40502), in the PI-4005 mainframe are labeled A and B. Connect the 40097 VME to PC Cable also labeled A and B, to the respective input connectors on the card.

There are also three LED Indicators on this card's rear panel. These indicate:

Remote	Presently being accessed by the CPU or System Computer.
Local	Not used.
Ready	The card is operational or ready to use. This does not mean that the total system is initialized or ready.

2.5.2. Data Acquisition Card

The output cables from your device under test are connected to the single ended BNC input connectors on the PI-4007 Preamplifier Module. The two BNC output connectors on each preamplifier output channel should be connected to the VIDEO AND VIDEOL BNC Connectors on the Selected Data Acquisition Card. The cables carrying the differential signal from the Preamplifier to the data acquisition card should be matched in length.

There are three BNC connectors on the rear of the Data Acquisition Cards that are the inputs for the control signals required to acquire data. They are:

FSYNC The FSYNC or Frame Sync is a pulse used to indicate the beginning of a frame. This pulse increments the frame counter on the board.

LSYNC The LSYNC or Line Sync pulse indicates the beginning of each line in the data stream.

PCLK The PCLK or Pixel Clock is the clock that ultimately provides the timing of the acquisition up to the A/D converter.

There are four BNC connectors provided for monitoring internal signals. These signals must be terminated into 50Ω to reduce transmission line effects and noise on the board. The monitoring signals are:

CDS CLK Not used.

CONV CLK (Convert Clock) This connector allows monitoring of the Convert and Clamp Clocks that are used to set the A/D conversion point or the two sampling points of the Correlated Double Sampling Circuitry. These two clocks are combined for monitoring at this BNC. The Clamp Clock should be aligned with the Video Reset portion of the signal, when CDS is selected. The Convert Clock should be aligned with the signal portion of the video signal.

VID MON (Video Monitor) Allows monitoring of the video signal at the input of the A/D Converter. Use this signal and the Convert Clock to fine tune the timing of the acquisition system. The VID MON signal will offset at the point of the Clamp edge to the ground reference of the A/D when CDS is selected.

A/D MON—A/D Monitor—Allows monitoring of the signal from the output of the Analog to Digital Converter. This is the digital information just prior to the optical isolators and the digital section of the card. This signal has only eight bits of resolution and has DC offset. It should be used only as a “quick functional” check of operation.

2.5.3. Preamplifier Controller Card

The 40096 Preamplifier to Controller Cable connects the Preamplifier Controller Card to the Preamplifier Module. The first preamplifier used in the system should be connected to J301 Control Ch1-Ch4. The second Preamplifier should be connected to J302 Control Ch5- Ch8. If another Preamplifier Controller Card is in the PI-4005, the third and fourth preamplifier modules should be connected to J301 and J302 respectively. The opposite ends of these cables connect to their respective preamplifier modules.

The other connector on the 40511 Preamplifier Controller Card is J303 Out Monitor. This BNC connector is used to monitor the Global Offset from each of the 1 to 8 channels of preamplifier used with this card. This BNC connector should be connected to your DVM to monitor the preamplifier Global Offsets on each channel based upon selection of the channels in software through the PI-4005 software module in PI-Controller or PI-DATS.

2.5.4. Clock Fanout Card

There are three BNC connectors on the rear of the Clock Fanout Card that are the inputs for the control signals required to acquire data. These signals are then distributed to the data acquisition cards through the VME backplane. They are:

FSYNC The FSYNC or Frame Sync is a pulse used to indicate the beginning of a frame.

LSYNC The LSYNC or Line Sync pulse indicates the beginning of each line in the data stream.

PCLK The PCLK or Pixel Clock is the clock that ultimately provides the timing of the acquisition up to the A/D converter.

2.5.5. Rear Panel Dc Monitor Jacks

The PI-4005 Acquisition Mainframe has its own internal power supplies and should be connected to your AC power source. The internal DC Power Supplies in the PI-4005 Acquisition Mainframe are used for the digital section of the Data acquisition Cards. This Power Supply is shielded and floating with respect to the PI-4008 Analog Power Mainframe that is used to power the analog section of the Data Acquisition Cards and the Preamplifier Module. The analog and digital sections of the data acquisition cards are isolated on the card and must be powered by the two supplies.

The DC monitor jacks on the rear panel of the PI-4005 are for monitoring the internal DC supplies and the power applied to the mainframe from the PI-4008 Analog Power Mainframe.

These jacks are to be used as monitor points only, and are not to be used as power connections, or as power sources to power any other devices or instruments. Each Voltage monitor line to the jacks has a series 10k resistor. Ground lines do not have a series resistor.

DO NOT GROUND THE ANALOG AND DIGITAL GROUND POINTS ON THE REAR OF THE MAINFRAME TOGETHER. This will defeat the isolated grounds in the system and lead to inaccuracies and increased noise in the system.

The analog chassis ground point is floating to reduce noise. The digital ground is connected to chassis ground. The mainframe chassis is grounded to your rack by the slides and by the connection of the screws into the rack mount ears.

2.6. Remote Operation Of PI-4005 Acquisition Mainframe

The PI-4005 Acquisition Mainframe can be placed a maximum of 25 feet from your computer. The 40097 cable supplied has a length of 25 feet. Please consult the factory for cables of shorter length.

Once all the connections such as analog power, VME interface and signal input have been made to the PI-4005 Acquisition Mainframes, power can be applied to the system. Turn on the DC Power Supplies, the PI-4008 Analog Power Mainframe. Then turn on the pI-4005 Acquisition Mainframe. You will hear a click as the DC switching board relays pull in. This will occur after an approximate a 1 second delay. This is normal.

3. SYSTEM CONFIGURATION INFORMATION AND OPTIONS

A typical Data Acquisition system would consist of a PI-4005 Acquisition Mainframe with a number of Data Acquisition Cards, a PI-4008 Analog Power Mainframe, a Preamplifier Module and a computer with Data Acquisition software.

The PI-4005 consists of the Mainframe, Internal DC power supplies, 10 layer High Speed VME Backplane, and 40502 VME-to-PCI adapter card set. The mainframe contains 12 VME slots, allocated as follows:

Type	Slot
Data Acquisition Cards (up to 8)	3-10
Preamplifier Controller Cards (up to 3)	9-11
Clock Fan Out Card	12
VME Adapter Card	1
Repeater Card	2 (master)
	1 (slave)

PI-4008 Analog Power Mainframe supplies the DC power for the analog and “clean digital” sections of the Acquisition Mainframe and PI-4007 Preamplifier Module to limit system noise. One Analog Power Mainframe will provide power for one PI-4005 Acquisition Mainframes (up to 8 channels) and up to six PI-4007 Preamplifier Modules.

Larger systems with multiple mainframes are available.

3.1. Data Acquisition Cards

400530 10 MHz 12 bit Data Acquisition Card. Provides amplification, filtering, correlated double sampling and analog to digital conversion with 16MB of RAM.

400550 2 MHz 16 bit Data Acquisition Card. Provides amplification, filtering, correlated double sampling and analog to digital conversion with 16MB of RAM.

400540 5 MHz 14 bit Data Acquisition Card. Provides amplification, filtering, correlated double sampling and analog to digital conversion with 16MB of RAM.

400520 40 MHz 10 bit Data Acquisition Card. Provides amplification, filtering, correlated double sampling and analog to digital conversion with 16MB of RAM.

400510 40MHz Digit Data Acquisition Card. Accommodates up to 16 bit parallel or serial digital input data with 16MB of RAM.

3.2. PI-4007 Preamplifier Module

Four channel programmable preamplifier designed to be placed near the Dewar or device under test for signal conditioning. The Preamplifier can be used as four separate preamplifier channels, or can be set up in a multiplexed mode to allow the four channels to share one Data Acquisition Card. The preamplifier requires a 40511 Preamplifier Controller Card. This Card controls all of the programmable functions of the PI-4007 Preamplifier Module and is located in the PI-4005 Acquisition Mainframe. Each Preamplifier Controller Card can control two PI-4007 Preamplifier Modules and is connected via the 40096 Preamplifier to Controller Cable.

3.3. PI-4009 Clock Fan Out Card

This card routes one set of FSYNC, LSYNC, and PIXEL clocks through the VME backplane to all data acquisition cards present in the PI-4005. The three inputs are connected via BNC connectors. The purpose of this card is to minimize the number of timing signals required from the pattern generator for multiple data acquisition cards.

3.4. 40502 PCI To VME Adapter Card Set

Adapts the VME backplane directly to the PCI bus of the PC; includes two Cards; one for the VME backplane in the PI-4005 Acquisition Mainframe, and one that is installed on the PCI motherboard of the computer. The 40097 VME to PCI PC Cable is required to connect the two cards.

3.5. Typical System Configuration

The following is a typical configuration for a minimum system, with four channels of preamplifier multiplexed to one data acquisition channel:

1 PI-4005 Acquisition Mainframe
1 PI-4008 Analog Power Mainframe
1 Data Acquisition PC Card
1 PI-4007 Preamplifier Module
1 40511 Preamplifier Controller
1 40502 PCI to VME Adapter PC Card
1 40097 Cable
1 40096 Cable
1 Computer

The Data Acquisition system is delivered with the PI-4005 Control Software Module and PI-Controller. This software controls all file handling functions such as Save, Load, etc, and the use of all programmable functions. The software will be preloaded in the computer supplied with the acquisition system.

4. BASIC SYSTEM DESCRIPTION

The PI-4005 Acquisition System is designed specifically for the acquisition of data from Charge Coupled Devices (CCD's), IR Detectors, and Focal Plane Arrays. The system consists of a mainframe, a host computer and software to control, acquire, analyze, report and archive data used to characterize and test these devices. Direct Connection from the host computer to the VME backplane provides maximum data transfer efficiency. Taking advantage of the VME bus, the PI-4005 Acquisition System can acquire data at up to 40 MHz data rates with 10 bit accuracy or with accuracies up to 16 bits at 2MHz.

The PI-4007 Preamplifier Module is available for applications that require the device under test output to be taken from close proximity to the device under test.

A host of programmable features makes the system ideal for Research and Development, Characterization, and Production Test. All system software is written to operate under Microsoft Windows NT 4.0.

Each Data Acquisition Card is complete with analog signal processing including offset and gain correction, filtering and correlated double sampling before the A/D converter, and 16MB of RAM. An Area of Interest (AOI) feature is provided for sub-image acquisition. This feature will allow processing and display of a window of the focal plane of any size up to 2048 x 2048 pixels.

The PI-4005 Acquisition Mainframe contains slots for up to eight Data Acquisition Cards and additional slots for the PCI to VME interface card, clock Fan Out card and up to three preamplifier controller cards. The Data Acquisition Cards are a modified 6U in size. Up to 24 channels of data acquisition can be supported in a single mainframe with six data acquisition cards and six PI-4007 Preamplifier Modules operating in the multiplexed mode. The system can be expanded by using additional mainframes.

The chassis has a blank front panel with rear outputs, which are cabled directly to the host computer through the VME interface cards and cable for fast data transfer. The cards are loaded into the mainframe from the rear.

Separate power supplies and separate ground systems are used for Analog and Digital Circuitry, with only the required ground connection underneath the A/D converter as the common point.

All inputs to the Data Acquisition Cards, and all outputs from the A/D converter are optically isolated to prevent outside sources of noise from entering the system.

4.1. PI-4007 Preamplifier Module

The PI-4007 Preamplifier Module is a four channel preamplifier packaged in an aluminum chassis that is designed to set close to the device under test or the dewar. This allows minimum lead length between the device under test and the PI-4007 Preamplifier Module. The PI-4007 is designed to drive the longer cable between the preamplifier module and the PI-4005 Data Acquisition Mainframe. Each Channel has a single-ended video input and a differential video output capable of driving 50 Ohm loads.

The preamplifier allows the four channels to output data simultaneously, or to be used in a mode that allows the four channels to be multiplexed into one Data Acquisition Card to reduce the number of Data Acquisition Cards required.

A high compliance current load under microprocessor control is provided, with eight bit resolution for p-type and n-type output structures from the device under test. The load current can be adjusted for each channel independently with eight-bit accuracy.

The input Offset for each preamplifier channel can be controlled independently with 16 bit resolution to optimize the dynamic range for each preamplifier. The DC voltage offset at the video input to the preamplifier is monitored for all channels. A multiplexed test point is provided through the 40511 Preamplifier Controller Card to monitor the individual offset DC Voltages.

The input to the preamplifier will accept signals in the range of ±15 volts. The input is a programmable window that accepts a signal level to a maximum of 10 volts peak to peak while allowing at the same time, a correction of the DC offset of up to ±10 volts.

The input capacitance of the preamplifier channels is approximately 15pf, and can be a programmable current pump that will allow selection of the current load from the device.

The preamplifier gain, input to differential output is 1.0 with back termination and 2.0 without back termination. Accuracy of gain is 1% over a temperature range of 20 to 50° C.

DC Power for the PI-4007 Preamplifier Module is supplied by the PI-4008 Analog Power Mainframe. The power is routed to the preamplifier module through the 40511 Preamplifier Controller Card located in the PI-4005 Acquisition Mainframe. The 40511 Preamplifier Controller also supplies all control functions for the Preamplifier Module.

The output of the Preamplifier Module is differential. The bandwidth of the Preamplifier is 50 MHz. The output of the Preamplifier is connected directly to the PI-4005 Acquisition Mainframe through coax cable pairs.

4.2. Data Acquisition Card Features

Analog input Voltage range on the Data Acquisition Card is ±10 Volts (±5 V offset adjustable and ±5 V signal). A buffered analog output is available at a BNC connector on the rear panel for viewing the analog signal with an oscilloscope just prior to A/D conversion. The Correlated Double Sampling is programmable to allow selectable sampling points.

Data Acquisition Card inputs include Frame Sync, Line Sync, and Pixel Clock. The system uses these external clocks for synchronization. The system allows the Frame Sync, Line Sync, and Pixel Clock to be used on each Data Acquisition Card independently. The user also has the choice of selecting a master Frame Sync, Line Sync, and Pixel Clock that is available through the VME bus from the Clock Fan Out Card. The selection of the source of the Frame Sync, Line Sync and Pixel Clock to the card is controlled by the host computer and each card can be set up individually.

A Card ID register is used for identifying card locations.

Optical Isolators are used after the A/D and prior to the RAM for additional noise isolation. All other inputs to the unit are also optically isolated for noise immunity.

Output of the A/D converter is stored in a 32 bit structure for increased system speed.

There is a D/A converter with buffered BNC output on the rear panel card flange for viewing the output data from the A/D converter.

4.3. Host Computer

The host computer must be supplied by or integrated by Pulse Instruments. The computer provided will be configured with at least the following features:

- 1.0 GHz Pentium IV processor
- 20 GB Hard disk
- SVGA Graphics Adapter
- 512 MB RAM
- CD-RW drive
- 10/100 Fast Ethernet card
- Monitor, keyboard, and mouse

The host computer is the operator's interface to the test system. The operator first defines the physical configuration of the DUT, and the test conditions. Once the test has been defined, the computer communicates with the acquisition system over the VME bus.

Analog pixel data from the DUT is sent to the Acquisition system where it is ultimately converted and stored in memory that can be accessed by the computer as shared memory via the VME bus.

Once, the digitized pixels are available to the computer, images and pixel data can be displayed and analyzed. Further analysis on the data can be displayed in the form of charts and graphs.

Data can be formatted for export to Excel and MatLab for further analysis.

5. SOFTWARE

The Data Acquisition system is setup and controlled through the Data Acquisition module of either PI-DATS or PI-Controller/PI-Controller+. The settings are the same in both programs. PI-DATS allows you to program multiple acquisitions within a test plan. PI-Controller gives you real time control of the instrument.

5.1. Operating Concepts And Menu Items

5.1.1. Mnemonic Label

PI-Controller and PI-DATS use the concept of instrument "mnemonics" to represent hardware devices and test plan objects (PI-DATS only). Each object under user control is represented by a graphical icon and a user-assigned mnemonic name (collectively referred to as a "mnemonic" throughout this manual). This allows the user to refer to an instrument by a recognizable mnemonic instead of by its generic description or location. For example, a DC bias channel can be assigned the name $\mathbf{V_{CC}}$ instead of "Mainframe 1, slot 2, channel 2, ±8 V DC Bias." Examples:

Mnemonic	Function or Instrument Module
BIAS1	Channel 1 of 41701 DC Bias card in CompactPCI
CKDR2	Channel 1 of 41400 Clock Driver card in CompactPCI
VCLK1	Channel 2 of 40460 Clock Driver card in 4002
RESULT1	Non-hardware component for managing measured data.

Mnemonics may be renamed by the user at any time. Mnemonic labels are unique within the scope of each PIP file.

Mnemonics for a given function or instrument module can appear several times in a test plan, either with the same label, or with different labels. When running a test plan (available only in PI-DATS), different instances of a mnemonic represent different states of the hardware in the test plan sequence.

In the standard PI-Controller mode, multiple instances of a mnemonic can be used to switch among frequently used settings for a single mnemonic. You can create multiple instances of a mnemonic either by using the **Copy/Paste** functions or by using the **Mnemonic Selection** dialog box to add the item repeatedly.

5.1.2. .PIP File (Pulse Instruments Part file)

This is the basic file that PI-Controller creates and uses. PIP is the file extension. When **New** is selected from the File menu, a new PIP file is created (Untitled.PIP). When **Save** is selected from the File menu or when PI-Controller is exited and **Save Changes** is specified, the PIP file is saved to disk. The PIP file contains all mnemonics with their configurations and all hardware components with their connections and attributes.

PIP files can be read or modified by anyone else who also has PI-Controller on their computer. Thus PIP files are transportable because they are complete within themselves.

5.2. Adding Mnemonics

To enable control of a Pulse Instruments hardware device, you must add the channel or card from the **Mnemonic Selection** window. Clicking the **Mnemonics** button Mn displays a list of available mnemonics. Select the ⊞ symbol to view the multiple mnemonic choices of an instrument type:

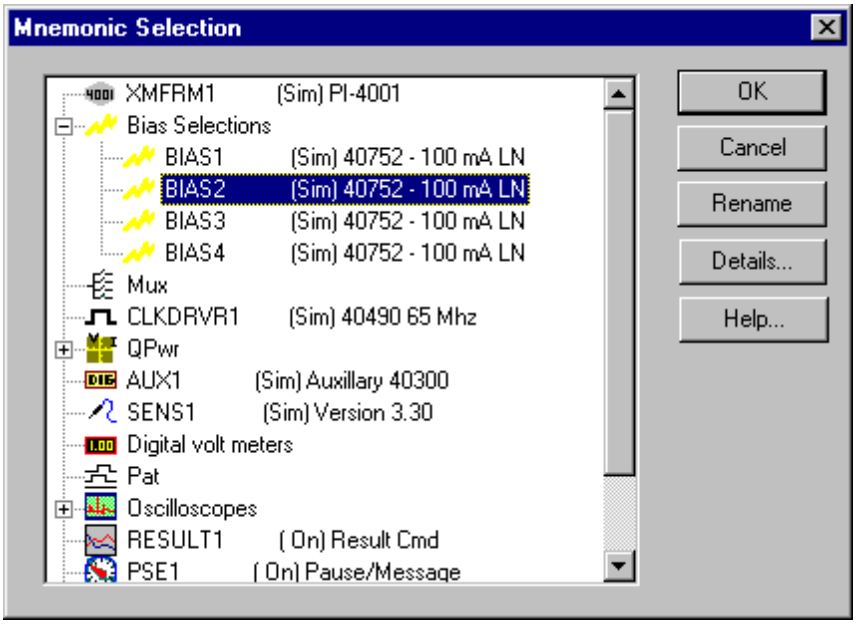


Figure 1: Mnemonic Selection Dialog Box

Add a mnemonic by clicking on its name and then clicking the **OK** button. You can add multiple items by holding the **Ctrl** key as you click, or by holding down the **Shift** key and typing the up and down arrow keys.

You do not need to add mnemonics for instrument cards or channels that you do not wish to control at this time. Mnemonics can be added at any time.

5.2.1. (Sim) or (On)

These symbols represent the current hardware state. **(Sim)** or Simulation means that there will be no hardware commands sent. **(On)** means that the Instrument is On-Line, and that hardware commands will be sent.

5.2.2. Rename

By default, each mnemonic is assigned a name that describes its model number and function, e.g. **41701BIAS**. The Rename button allows you to give your instrument channels names that are meaningful in your application, such as **V_{CC}**, **V_{DD}** or **VertClk1**. You can also single-click the mnemonic label directly in the Main Window to rename it.

5.2.3. Details

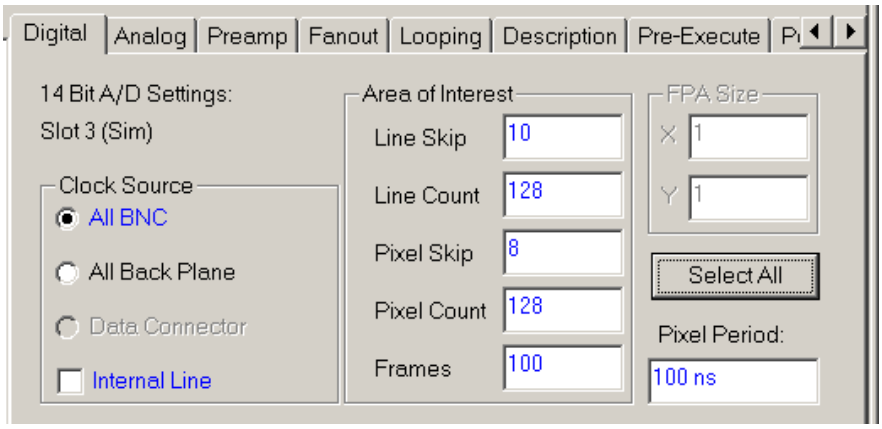
Press this button to display more details about the selected type of Instrument or Function, including its physical slot and channel number.

5.3. PI-4005 Mnemonic

The settings of the PI-4005 acquisition system are divided into property pages.

Digital	Sets up digital acquisition parameters
Analog	Sets up acquisition timing and filter and gain control.
Preamp	Sets up the PI-4007 Pre-Amplifier Module.
Channels	Select the active channels.
Plot	Setup the retrieved data for plotting.
Save File	Defines the format and options for data to be saved
Fanout	Sets up the Fan Out card
Description	Describes the PI-4005 hardware and sets Pre-Amp fixed gain.
Controls	Contains buttons to control the hardware.

5.4. Digital



This menu is used to set up the Area of Interest, the path for the clocks and the pixel period.

The Area of Interest defines the amount of data collected. This is determined from the number of lines entered at Line Pass, the number of pixels at Pixel Pass and the number of Frames. This can be a subset of or the whole array. The area of interest can be moved around by skipping pixels and lines. The timing for the device under test must include all Frame, Line and Pixels clocks required for a full output sequence.

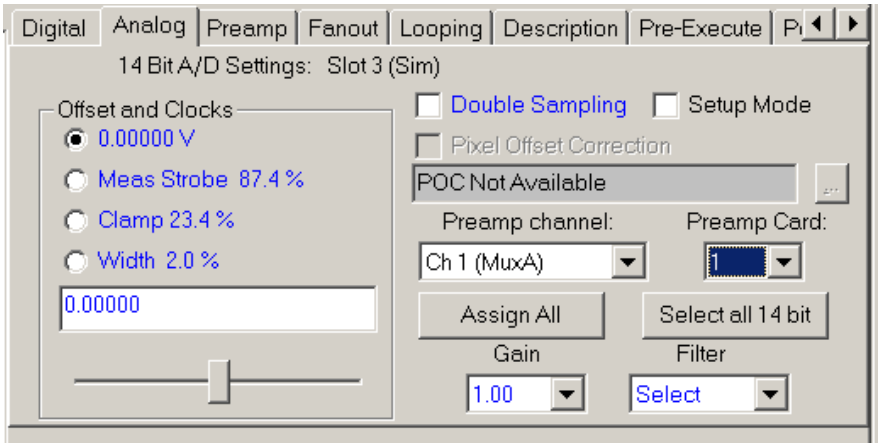
The source for the clock signals can come from the BNC connectors on the edge of the individual cards or through the VME backplane. The VME backplane should be selected when multiple acquisition cards are present in the PI-4005 to reduce the number of signals required.

If your test application does not supply a Line Sync signal, the PI-4005 can generate one internally after a specified number of pixels. To use this feature, check the Internal Line checkbox. The FPA Size entries will become enabled, allowing you to enter the number of pixels (X) and lines (Y) in your device. Every pixel clock is counted in this mode.

The Pixel Period entered defines the time period over which the Clamp and Convert pulses can be adjusted.

The Select All button causes all cards to be set as shown.

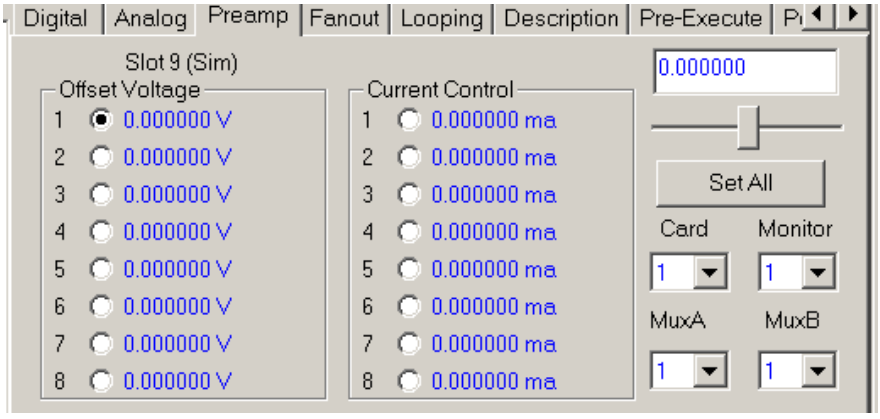
5.5. Analog



Offset and Clocks and double sampling is chosen here. Also one can set all cards with the same number of bits to all the settings on this page by pressing the Select all button. The available gains and filters can be selected here. This is a real time property page: As selections are made, the hardware is set if online and in Controller mode.

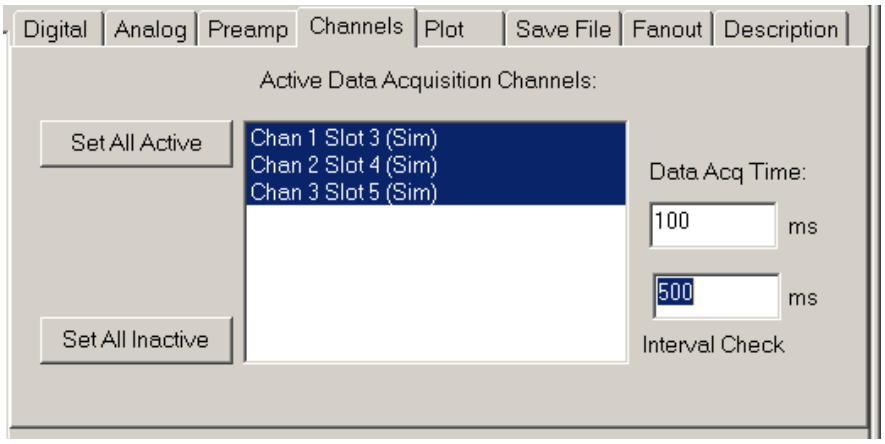
The Data Acquisition channel can be linked to a Preamplifier channel by selecting an available channel from the pull-down menu. This linkage is used by the software to determine the offset to use when calculating and displaying data. If Setup Mode is selected the data displayed represent the signal at the input to the A/D converter chip. Normal mode represents the signal at the input to the card or the preamplifier channel.

5.6. Preamp Property Page



This property page is used to set the Preamplifier offset voltages. This is done by selecting a channel its radio button and then entering a value or using the slider in the upper right corner of the page. You can also set the multiplexer channel with the pull-down menus. All selections take effect immediately if you are Online and in Controller mode.

5.7. Channels



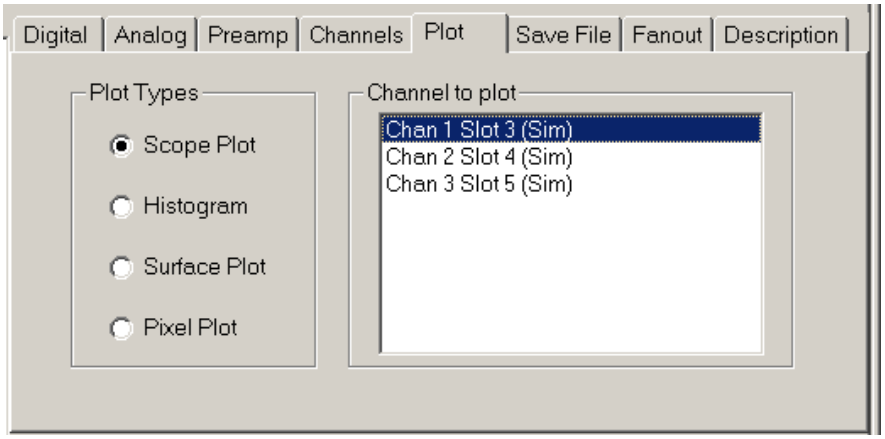
Data will be collected only for the channels selected here. To select more than one channel, hold down the Ctrl key while clicking additional channels.

The **Data Acq** time window is used for setting a time-out period for the total acquisition. For examle, if a frame of data is 100 x 100 pixels at a pixel period of 1 usec, then the total time for a frame of data would be 10,000 us. If 10 frames were taken the expected total acquisition time would be 100,000 us or 100 ms. (The area of interest is irrelevant for this setting). Type an entry here to return control to the user if the acquisition is not completed within that interval.

The system will also calculate a minimum acquisition time based on the Area of Interest and the Pixel Period. After this minimum interval has passed the system will check if the acquisition is complete.

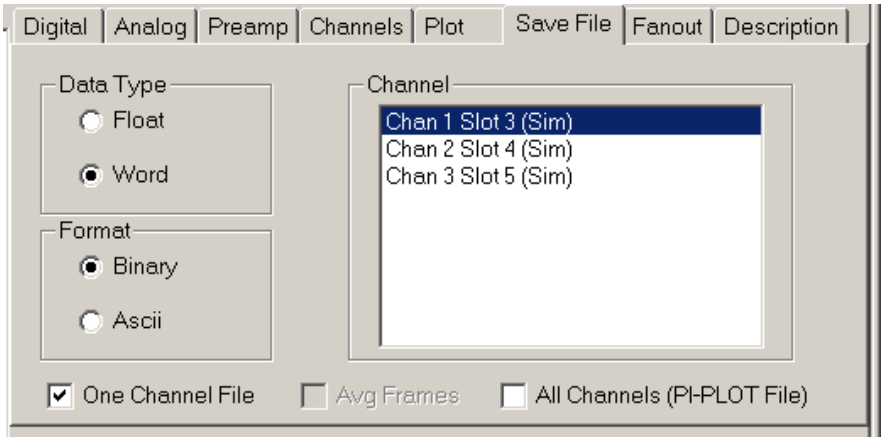
If the “interval check” does not have an entry the system will check for acquisition completion only once. If “interval check has a value, for example 1 ms, the software willl continue to check for acquisition completion every milliscond until the data acquisition has timed out.

5.8. Plot



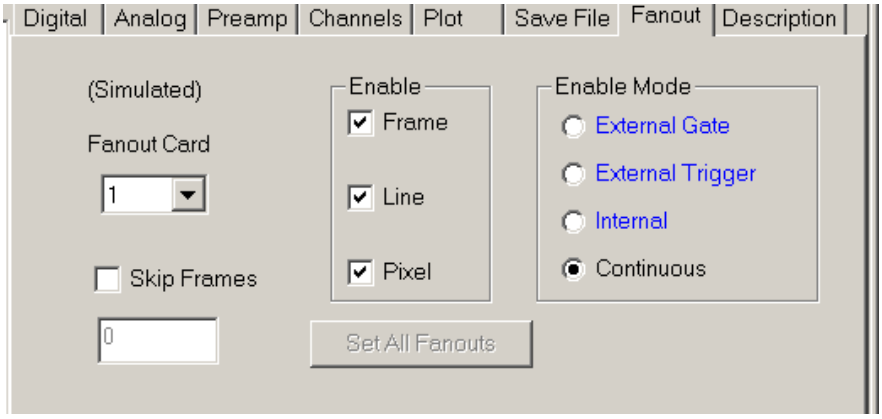
Select the desired plot and the channel(s) to be plotted after data have been acquired.

5.9. Save File



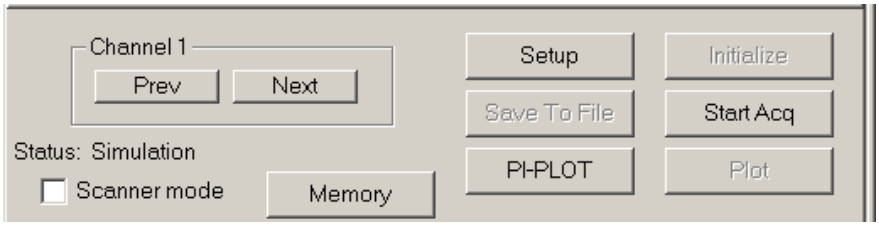
This property page specifies the channels of data to be saved and the data format.

5.10. Fanout Property Page



This property page sets the clock options for each fanout card. Functions in blue are not presently available.

5.11. Controls



The Controls buttons are common to every property page. The different channels are selected and appear on the other property pages with the **Prev** and **Next** buttons. The **Setup** button (Controller mode only) sets the digital property page.

Initialize causes the A/D cards to be rescanned and reset. The **Start Acq** button starts a data acquisition. The **Plot** button causes Matlab to plot the latest data acquired.

Save To File saves the raw data to a file. Please see 6.5.2. PI-DATS archive (*.img or *.dat) for details on the file format.

The **Status** will indicate whether the acquisition is complete or waiting to complete. It will time-out based on the a maximum acquisition time calculated based on the Area of Interest set on the Digital property page or by the Data Acq Time set on the Channels property page.

Check **Scanner mode** box to execute the Spot Scanner at data acquisition.

The PI-PLOT button launches the PI-PLOT application. Please see **Section 6. PI-PLOT** for details.

6. PI-PLOT

PI-PLOT provides a variety of ways to view your data graphically.

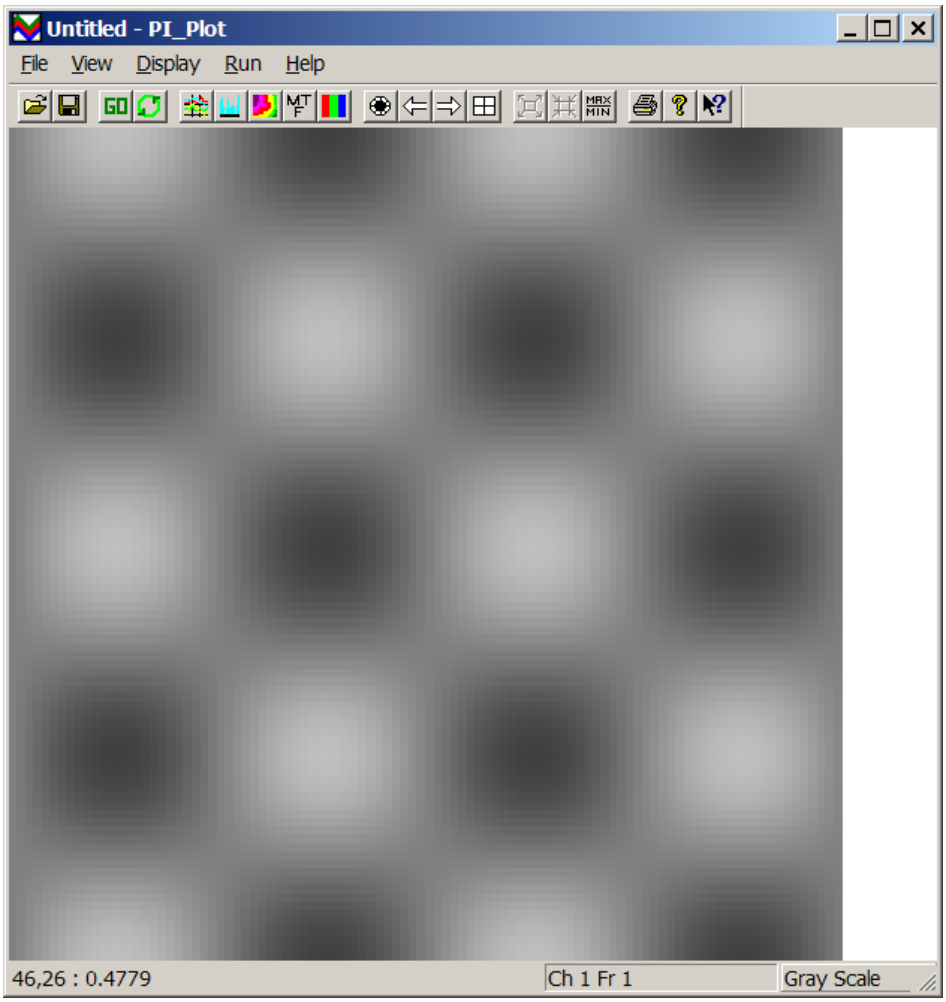


Figure 2: PI-PLOT window

There are four supported viewing formats in PI-PLOT.

- Scope plot
- Grayscale
- False color/True Color
- Histogram

A fifth display mode (MTF plot) is currently unsupported, and may be revised in a future update to PI-DATS.

To launch PI-PLOT, click select the PI-4005 Setup mnemonic in PI-DATS and click the PI-PLOT.

6.1. Scope Plot

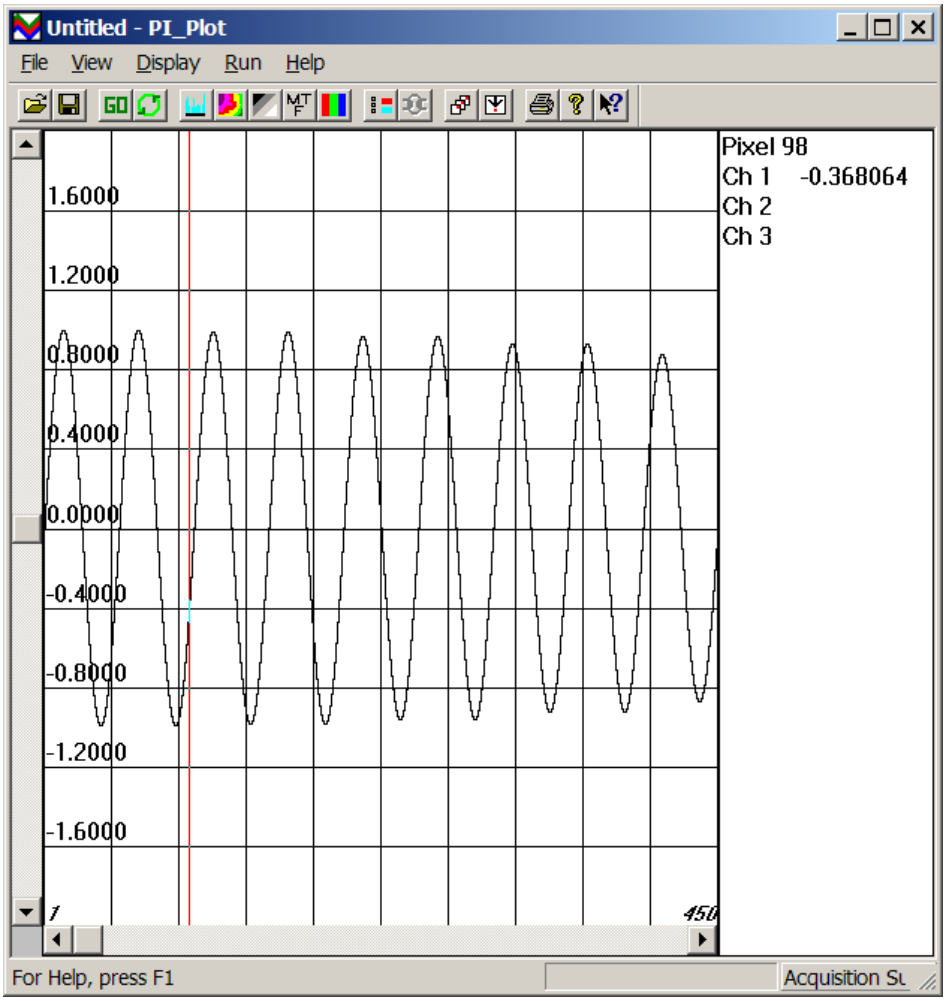


Figure 3: Scope Plot

PI-PLOT launches in **Scope Plot** mode by default. You can also select **Scope Plot** at any time by clicking on the **Scope Plot** button  or by choosing **Scope Plot** from the **View** menu.

In a Scope Plot (also called a “skyline” plot) all acquired pixels are displayed in sequential fashion, with each pixel’s value represented by the height of the “skyline” at its position.

The Pixel pane in the right margin of the PI-PLOT window displays information about the pixel under the red cursor line. The red cursor line may be dragged with the mouse.

Pixels are numbered in the order they are acquired; therefore the first pixel of the second frame of a 100 x 100 array would be the 10,001st pixel.

Use the **Settings** button  or the **View:Settings** menu item to change the appearance of the Scope Plot:

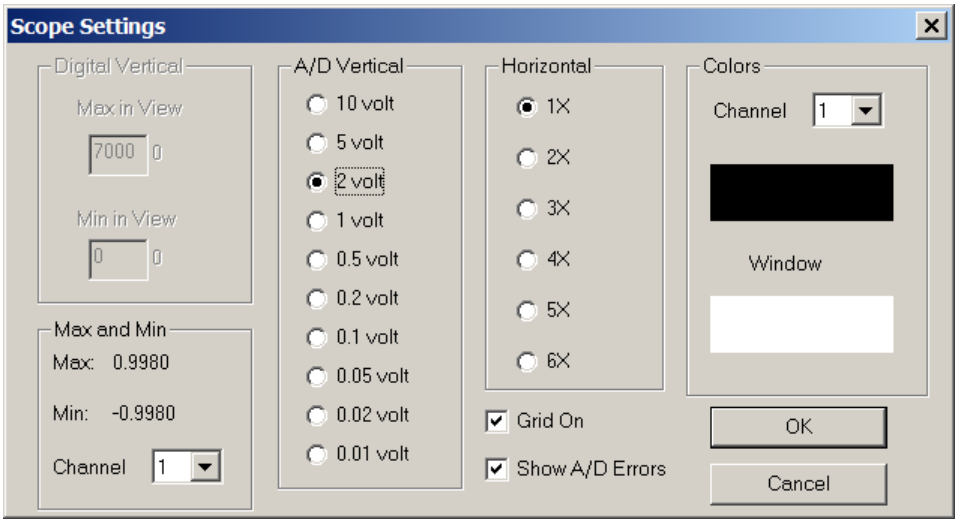


Figure 4: Scope Plot settings

Use the **Vertical** section on the left side of the **Scope Settings** window to adjust the vertical scale or the maximum and minimum values in view. Note that there is an assumed "0" in the entry (e.g. a **Max in View** entry of 6554 would cause the maximum viewable value to be 65,540).

Use the **Horizontal** radio buttons to select the horizontal scale.

Use the checkboxes to show or hide the **Grid** and any **A/D sampling errors**.

Use the **Colors** entries to adjust the colors on the plot. Select a channel from the drop-down menu, then click on the default color to display a Windows standard color-picker. Click on the Window color to adjust the background color for the plot.

6.2. Grayscale Plot

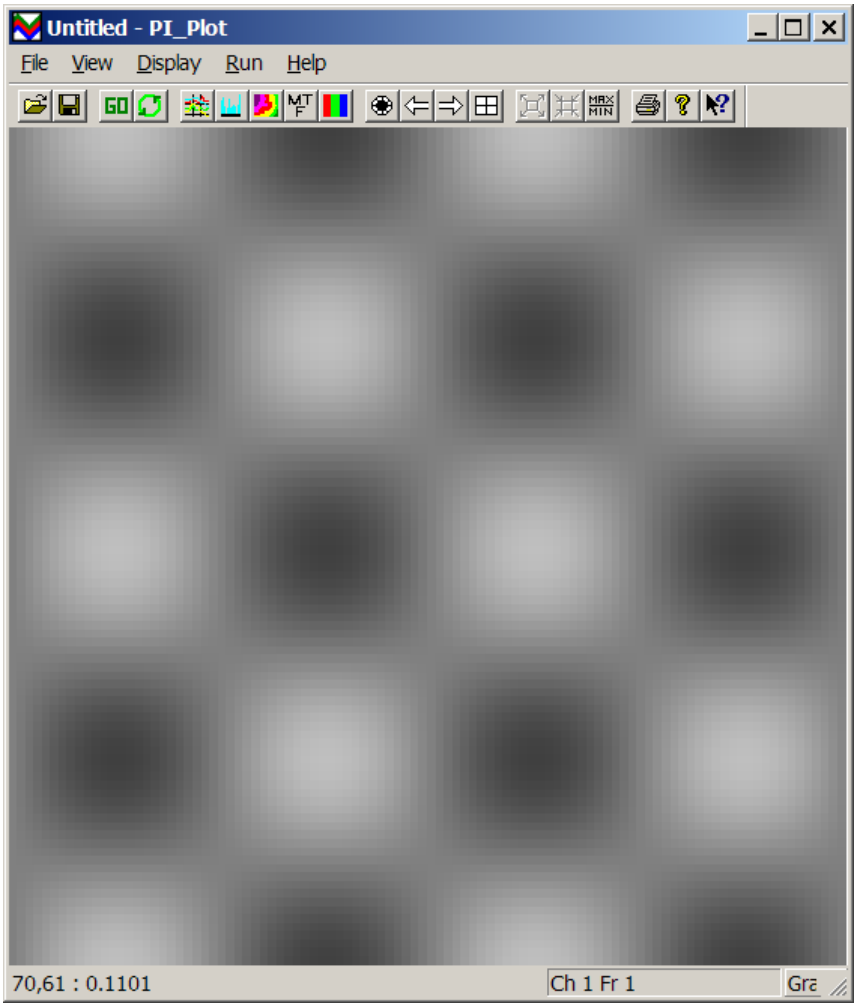


Figure 5: Grayscale Plot

Select **Grayscale Plot** by clicking the **Grayscale Plot** button  or by selecting **Grayscale Plot** from the **View** menu.

In a Grayscale Plot the acquired data are displayed as an image, with pixel values represented by brightness. Acquired images are scaled (up or down) to display at the size of the PI-PLOT window at the time the image is acquired.

By default, the grayscale luminosity is scaled to 2^n, where ***n*** is the number of bits specified in the Acquisition Setup property page. For example, if the acquisition is set for **12-bit** data, then a value of 4096 will be displayed as white, and 0 will be displayed as black.

The luminosity can be re-scaled to the minimum and maximum values actually acquired either by clicking the **Max/Min** button  or by choosing **Scale to Data** from the **Display** menu. For example, **Figure 5: Grayscale Plot** shows an 8-bit modulated sinewave plotted on a 14-bit luminosity scale. When **Max/Min** is clicked, the display changes to the following:

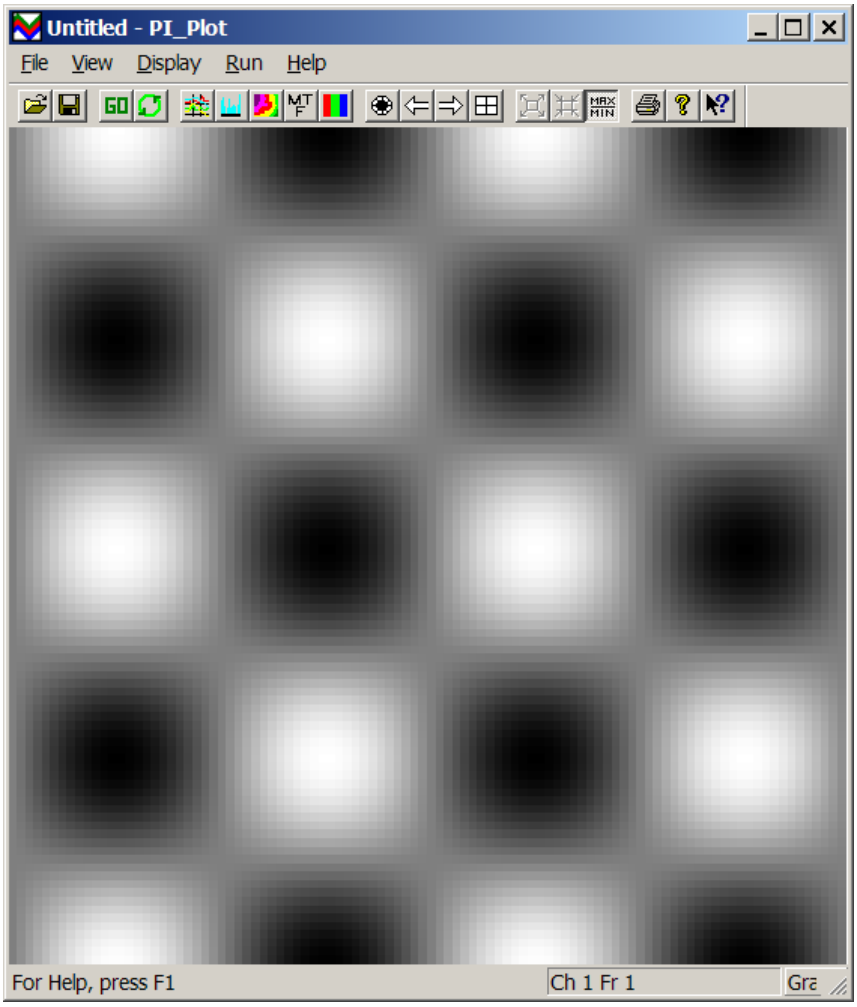


Figure 6: Grayscale Plot, scaled to data

As the mouse moves over the grayscale plot, the status bar in the lower-left corner of the PI-PLOT window will display the pixel address (row, column) and the pixel value under the mouse pointer.

If multiple frames of data have been acquired, the user may "page" through the frames by using the **Display Prev**  and **Display Next**  buttons on the toolbar or by selecting **View:Previous Frame** or **View:Next Frame**. The user may also jump to any frame number using the **Pick Frame**  button or the **Pick Frame** item from the **View** menu.

The user may zoom in on a selection of pixels by dragging anywhere inside the grayscale plot. The selected pixels will be scaled up to fill the PI-PLOT window. The zooming process may be repeated by dragging again in the new grayscale plot.

Once zoomed, the user may flip through different levels of zoom by using the **Prev Zoom**  and **Next Zoom**  buttons on the toolbar, or by selecting the **Prev Zoom** and **Next Zoom** items in the Display menu.

6.3. False Color Plot

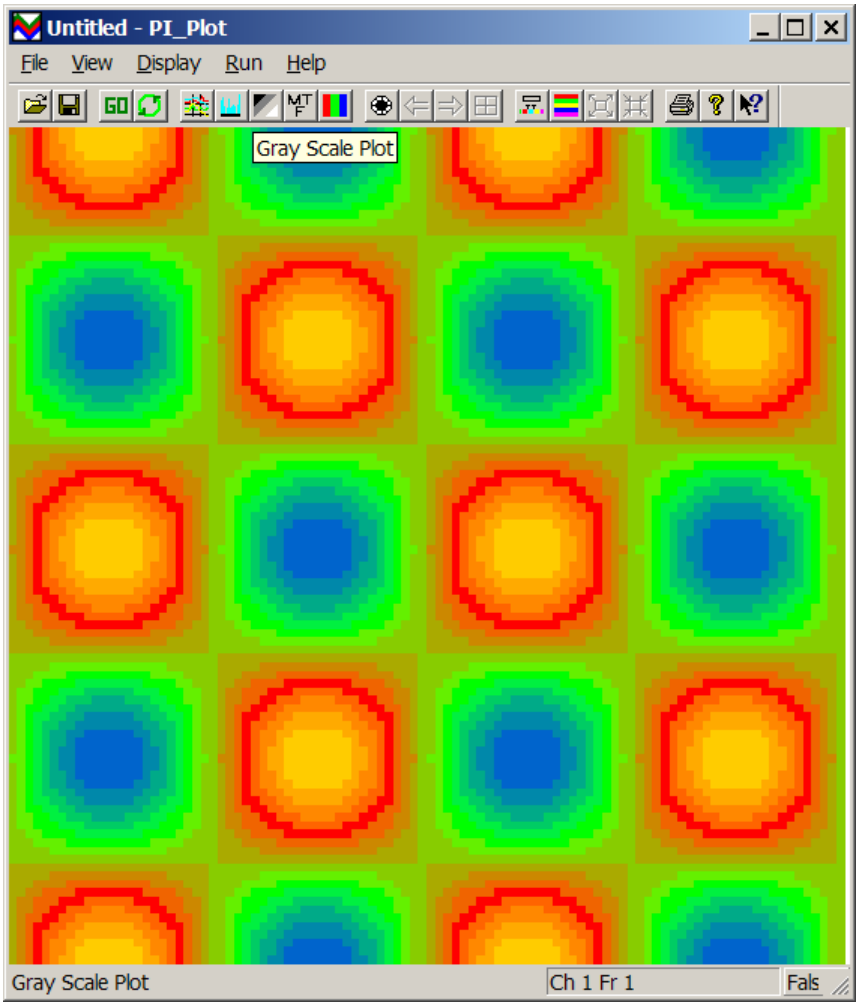


Figure 7: False Color Plot

Select **False Color Plot** by clicking the **False Color Plot**  button or by selecting **False Color Plot** from the **View** menu.

In a False Color Plot the acquired data are displayed as an image, with pixel values represented by a range of colors. Acquired images are scaled (up or down) to display at the size of the PI-PLOT window at the time the image is acquired.

By default, the color table is set for 32 colors, evenly spaced from 0 to 2^n, where n is the number of bits specified in the Acquisition Setup. For example, if the acquisition is set up for 12 bits of data, then a value of 4096 will be displayed as white, 0 will be displayed as black, and intermediate values will be displayed in colors.

If analog data have been acquired, the minimum and maximum values will be set to the full range of the A/D. This value will be ±2.0 V for the PI-4005 and ±4.0 V for the PI-3105.

The current color table can be displayed by clicking the **Color Table**  button or by selecting the **Color Table** item from the **Display** menu.

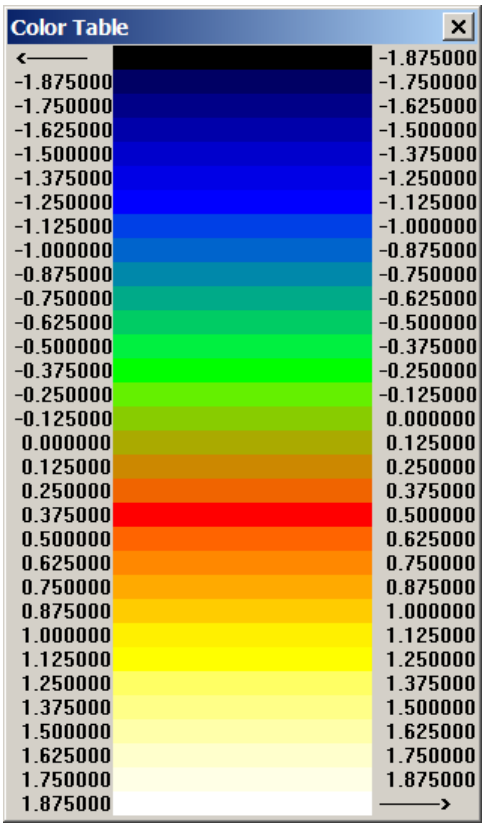


Figure 8: False Color Plot, color table

The color table can be modified to reduce the number of colors used and/or to adjust the thresholds for each color. Click the **Color Limits** button  or select **Color Limits** from the **Display** menu to display the **Color Limits** dialog box:

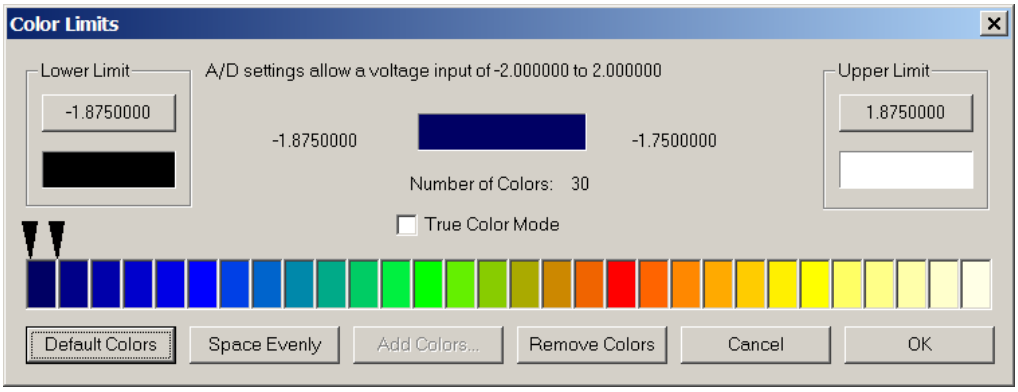


Figure 9: False Color Plot, edit color limits

To modify the thresholds for a single color, click it to select it, then drag the black triangular pointers to adjust the upper and lower thresholds for that color.

To automatically space all colors evenly between the current upper and lower limits, click the **Space Evenly** button.

To adjust the upper and lower limits for the entire table, click the **Upper Limit** or **Lower Limit** button and enter a new value.

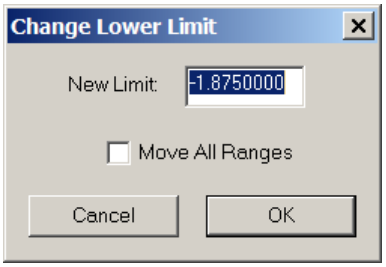


Figure 10: False Color Plot, edit lower limit

To automatically space all colors evenly between the new upper and lower limits, check the **Move All Ranges** box before clicking OK.

To remove a color, click to select it, then drag its pointers together and click the **Remove Colors** button. If there are currently fewer than 32 colors (including the upper and lower limits), the **Add Colors** button will be enabled.

The default color table can be restored at any time by clicking the **Default Colors** button.

As the mouse moves over the grayscale plot, the status bar in the lower-left corner of the PI-PLOT window will display the pixel address (row, column) and the pixel value under the mouse pointer.

If multiple frames of data have been acquired, the user may “page” through the frames by using the **Display Prev**  and **Display Next**  buttons on the toolbar or by selecting **View:Previous Frame** or **View:Next Frame**. The user may also jump to any frame number using the **Pick Frame**  button or the **Pick Frame** item from the **View** menu.

The user may zoom in on a selection of pixels by dragging anywhere inside the false color plot. The selected pixels will be scaled up to fill the PI-PLOT window. The zooming process may be repeated by dragging again in the new false color plot.

Once zoomed, the user may flip through different levels of zoom by using the **Prev Zoom**  and **Next Zoom**  buttons on the toolbar, or by selecting the **Prev Zoom** and **Next Zoom** items in the Display menu.

If your device has a Bayer mosaic color filter, the data can be “de-mosaiced” by clicking the **True Color** checkbox in the **Color Limits** dialog box. If **True Color** is checked, then the color limits are not used, and all pixels will be displayed as RGB values.

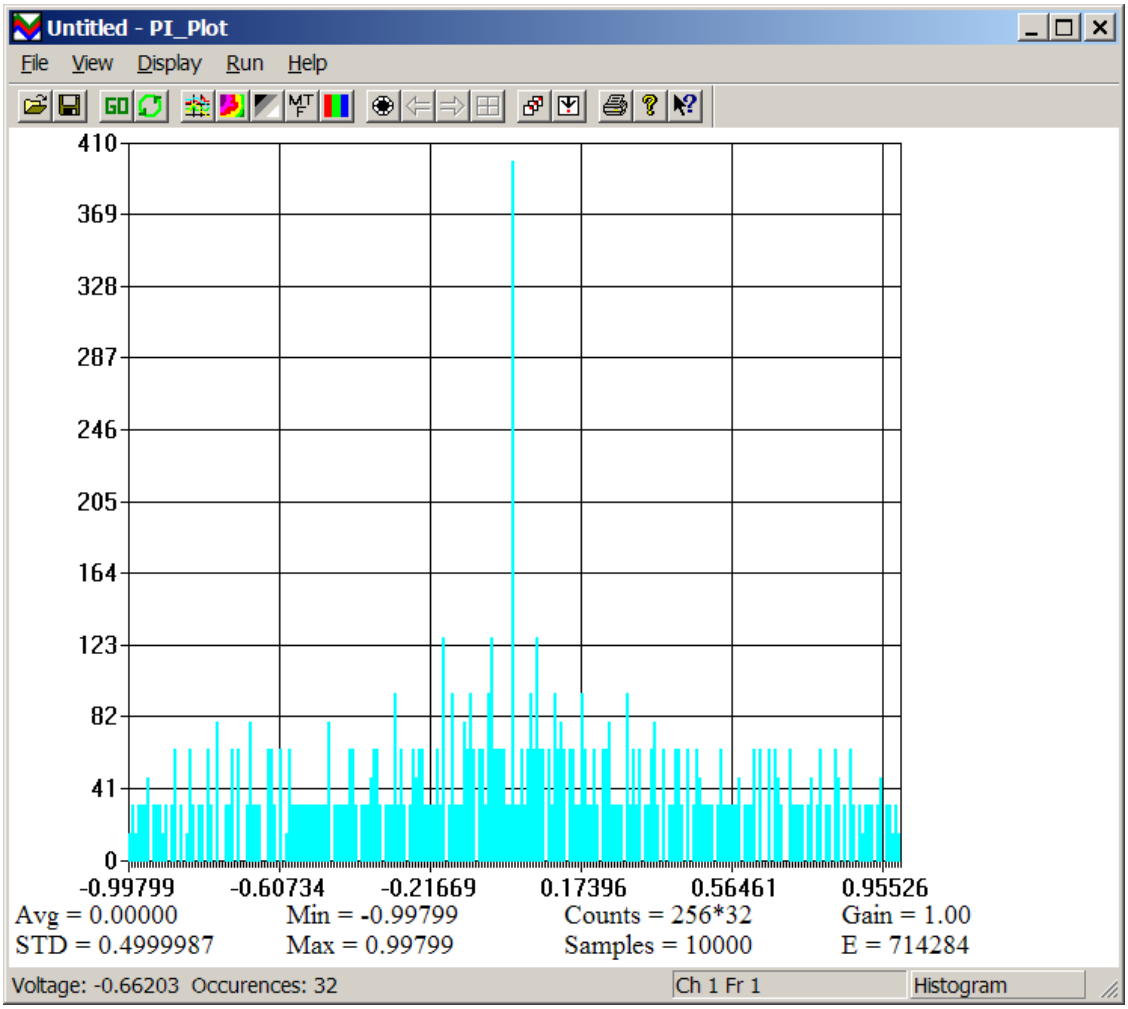


Figure 11: Histogram Plot

The Histogram plot displays the frequency of acquired pixel values. The height of each bar represents the frequency (number of occurrences) of each pixel value.

To select a **Histogram plot**, click the **Histogram Plot** button  or select **Histogram** from the **View** menu.

There are no settable parameters for the Histogram plot.

As the mouse moves over the PI-PLOT window, the pixel value and pixel frequency under the pointer will be displayed in the PI-PLOT status bar.

6.4. Acquisition Controls

PI-PLOT provides basic controls for running data acquisitions. There are two buttons on the toolbar and three menu items:

6.4.1. Start

The user may start a data acquisition by click the **Go** button  or by selecting the **Start Acq** item from the **Run** menu. This is equivalent to click the **Start** button in the PI-DATS main window. When the acquisition and data transfer are complete, PI-PLOT will automatically update the display with the new data, at the currently selected frame number and zoom level.

6.4.2. Continuous Acquisition

PI-PLOT can also display near-real-time video by running acquisitions continuously. Use the **Continuous** button  or select the **Continuous** item from the **Run** menu to enable this feature. When enabled, the **Continuous** button on the toolbar will retain a “depressed” appearance, and the **Continuous** item on the **Run** menu will be checked.

If the **Start/Go** button is clicked (either from PI-PLOT or from PI-DATS) while PI-PLOT is in Continuous Acquisition mode, data acquisitions and screen updates will run continously until interrupted by the user.

To stop continuous acquisition, click the **Continuous** button on the PI-PLOT toolbar. PI-DATS will complete the current acquisition and then stop.

To introduce a delay between the end of one data acquisition and the start of the next, use the **Pause Time** item in the **Run** menu.

Note that the acquisition parameters on the Data Acquisition property page in PI-DATS will remain the same for every acquisition in Continuous mode. For example, if the Frame Count is set to 10 frames, then each click of the **Start/Go** button will collect 10 frames. If PI-PLOT is set to Continuous mode, it will repeatedly collect 10 frames and update the screen after every 10th frame has been collected. To display the fastest possible frame rate, set the **Frame Count** to 1 before starting a continuous acquisition.

6.5. Saving Files

Data collected and displayed in PI-PLOT may be saved to a file. There are two available file formats:

6.5.1. PI-PLOT file (*.plo)

Use the **Save** button  on the toolbar or the **Save** item from the **File** menu to save a file in PI-PLOT format. PI-PLOT files can be re-opened directly in PI-PLOT and manipulated as if the data had just been acquired.

6.5.2. PI-DATS archive (*.img or *.dat)

Use the **Save As PI_DATS File** item from the **File** menu to save the acquired data as a raw PI-DATS archive. This file can then be used by 3rd-party applications. This is the same file format used by PI-DATS and PI-Controller in the **Save To File** button.

PI-PLOT will prompt the user to specify the data type and format:

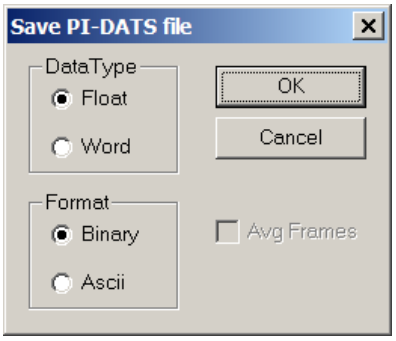


Figure 12: Save PI-DATS file, options dialog box

If **Float** is chosen each pixel value will be written as a floating-point voltage. If **Word** is chosen each pixel value will be written as a 16-bit integer.

If **Binary** is chosen, the file will be written as a binary stream. Choose this format to minimize the file size. If **ASCII** is chosen, the file will be written as text. Choose this format to maximize portability and human readability.

The data will be written to disk as a short header followed by raw data. The header of the file is in the following format.

```
struct HDRSTRUCT
{
      char Title[8];    // Unique tag: "PI-Img" or "PI-Asc"
      long x;           // Num Columns
      long y;           // Num Rows
      long nFrames;
      long nType;       //0 = float, 1 = word
      long nVersion;
      long nPixelSkip;
      long nLineSkip;
      long empty[7]; // Spares
};
```

The raw data is stored following the header, row by row. If the file format is specified as binary, the file is given an .img extension. If the file format is specifed as ASCII, the file is given a .dat extension.

If multiple frames have been acquired, the user may choose to average all frames into a single frame by clicking the Avg Frames checkbox.

The following are the first several lines of a sample PI-DATS file, written with the Float data type and ASCII format:

```
PI-Asc
Pixels = 100
Lines = 100
Frames = 1
File Type = 0
Version = 1
Pixel Skip = 0
Line Skip = 0
-2.0000
-1.9597
-1.9192
-1.8788
-1.8384
-1.7980
-1.7576
-1.7172
-1.6768
.
.
.
```

7. USING THE PI-4005 DATA ACQUISITION SYSTEM IN A SYSTEM APPLICATION

If your PI-4005 Data Acquisition System was integrated with a Pulse Instruments Pattern Generator at the time of purchase, then the timing information contained in this section is for reference only. The appropriate delays have been accommodated already in the cabling that connects your Pattern Generator to your PI-4005.

You should read this section if you purchased your PI-4005 on a stand-alone basis, if you intend to modify any of the cabling, or if you introduce other elements in the system that will affect system timing.

The PI-4005 Data Acquisition System is specifically designed for an automated test system environment. There are propagation times or time delays that must be taken into consideration for maximum performance of the instrument.

Within this system there is a timing relationship between the electronic Stimulus/Data Out Path and the Measurement Path.

Within these tow paths there are timing or sub timing issues tat need to be addressed. An example of the sub timing is the coincidence of clock edges at the Device Under Test (DUT).

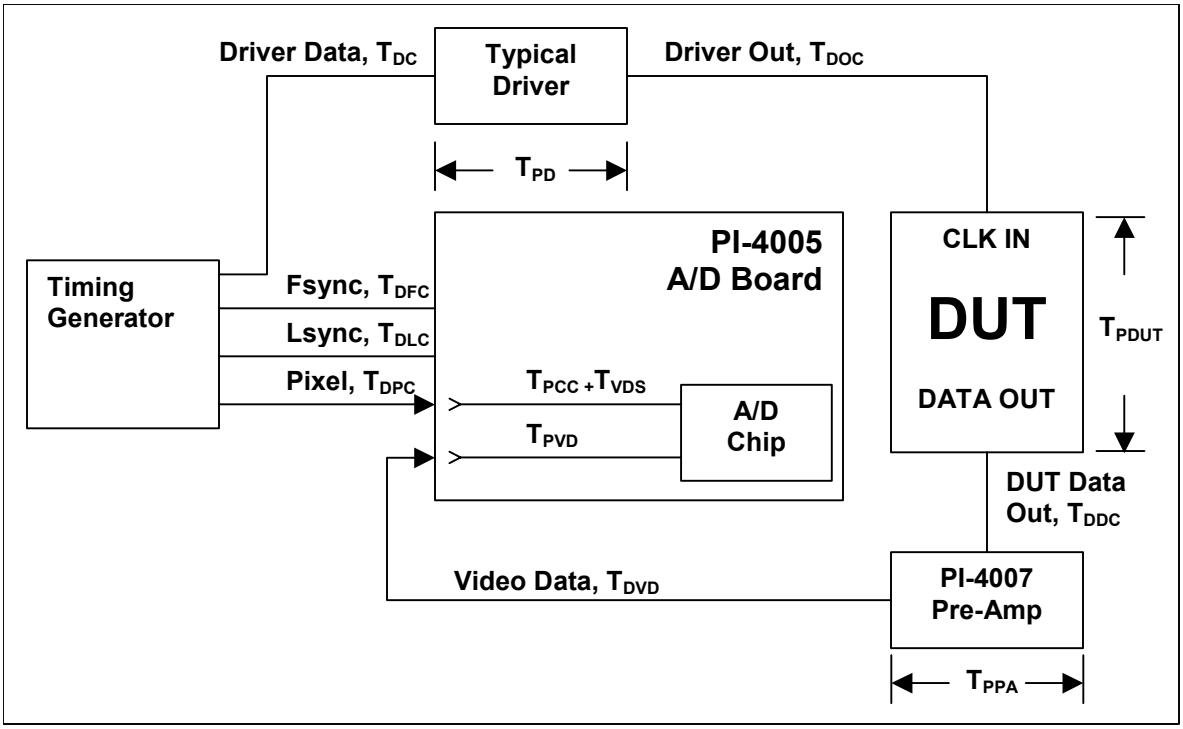


Figure 6-1, Timing Relationships

Figure 6-1 shows the timing relationship of the two major timing paths, Stimulus/Data Out Path and the Measurement Path. The Timing Generator is used as the Master Clock. All references to the Timing Generator in this section will be referred to as the Master Clock. The Maser Clock provides the timed signals for the clock drivers, Frame Sync, Line Sync, and Pixel Clock. These data signals are coincident in time (typically within 600 psec) at the Timing Generator output. This is valid if the starting bit of each data signal is the same, for example bit one. The output of the data generator or Master clock will be referred to as time zero. (T_o).

7.1. Stimulus/Data Out Path

The output of the Master Clock is connected to the input of the typical clock driver via cable. From the typical clock driver, a cable is used to connect this clock driver signal to the DUT input. The DUT output is connected via another cable to the PI-4007 Preamplifier input. The preamplifier output, video data, is routed via a cable to the video inputs of the PI-4005 Data Acquisition Cards.

Along with the various cable delays, you need to take into consideration the in-path device propagation times. The equation for summing the delay elements in the Stimulus/Data Out Path is:

$$T_{DSP} = T_{DC} + T_{PD} + T_{DOC} + T_{PDUT} + T_{DDC} + T_{PPA} + T_{DVD} + T_{PVD}$$

Where:

T_{DSP}=	Total of all delays in stimulus/data out path
T_{DC}=	Cable delay from Master Clock to typical driver
T_{PD}=	Typical driver propagation time
T_{DOC}=	Cable delay driver output to DUT
T_{PDUT}=	Propagation time of the DUT
T_{DDC}=	Cable delay from DUT output to (PI-4007) Preamplifier Input
T_{PPA}=	Preamplifier propagation time
T_{DVD}=	Cable delay of Preamplifier output to Data Acquisition Card Input
T_{PVD}=	Propagation time of Data Acquisition Card internal video path

In the above equation, given a set of minimum driver settings, the only variable in the equation is the propagation time, T_{PDUT}, of the DUT.

7.2. Measurement Path

The Measurement Path is simpler that the Stimulus/Data Out Path.

The signal of real importance to the Measurement Path is the Pixel Clock, since the role of Frame Sync ad Line Sync are secondary to the operation of the Data Acquisition Card.

The only cable used in this path is the cable between the Master Clock and the Pixel Clock input, T_{DPC}. The equation for summing the delay elements in the Measurement Path is:

$$T_{DMP} = T_{DPC} + T_{PCC} + T_{VDS}$$

Where:

T_{DMP}= Total of all delays in measurement path

T_{DPC}= Cable delay from Master Clock to pixel clock input

T_{PCC}= Propagation time of the internal circuitry generating the convert and clamp clocks

T_{VDS}= The variable or programmable delay to position the convert and clamp clocks in time with respect to the video data to be measured.

**In the above equation, the only variable is the programmable clock delay.

To time the system, the delay equations for the Stimulus/Data Out Path and Measurement Path should be equal for a specific minimum condition.

When establishing the specific minimum condition, the delay equations generated from Figure 7-1 will only be modified slightly.

To generate the specific minimum condition for the stimulus/data out delay equations, we will define the driver minimum condition and assume the DUT propagation is zero. The clock driver settings are minimum delay (if applicable), minimum (fastest) rise/fall times at a maximum amplitude.

Therefore the equation becomes:

$$T_{DSP} = T_{DC} + T_{PD} + T_{DOC} + T_{DDC} + T_{PPA} + T_{DVD} + T_{PVD}$$

Note: The term T_{PDUT}, DUT propagation defined as zero, is removed from the equation.

The Measurement Path delay equation is a simpler situation. The only modified term is the programmable delay to position the Convert and Clamp Clocks, T_{VDS}.

This should be set to the minimum delay setting. This term is also dependent upon the Pixel Clock period. The programmable delay range for the Convert and Clamp Clocks is determined and set by the Pixel Clock period. The maximum frequency of the 12 bit Data Acquisition Card is 10 MHz or a 100 nanosecond period.

Therefore, the equation becomes:

$$T_{DMP} = T_{DPC} + T_{PCC} + 25 \text{ ns}$$

For maximum performance, the system timing relationship should be:

$T_{DSP} = T_{DMP}$

This relationship gives a maximum performance system. But before we can use the relationship, we need to determine and/or measure the times of the individual terms.

To do this we must refer to the sub-timing issues.

The first sub-timing issue is the rise/fall edge coincidence of the clocks at the DUT socket. The more precisely these clock edges are aligned, the more accurately you can set the clock driver conditions at the DUT.

In the Pulse Instruments System 4700, the Master Clock is the PI-2005 Timing Generator. The pattern card that is used to generate data signals to the clock drivers may have the programmable delay option. The reason for using programmable delay is not to provide the gross de-skewing of clock driver outputs, but to make minor adjustments to the edge positions for coincidence.

This minor adjustment is less than 3 or 4 nanoseconds of the usable edge positioning at the DUT socket. If this delay is used for gross de-skewing of the clock drier clocks you then limit the capability of the test system.

Referring to Figure 7-1, the test system will have multiple clock drivers, so there are multiple coaxial cables connecting the Timing Generator, to the individual driver inputs.

These cables, $T_{DC}(1)$ through $T_{DC}(n)$, should be of identical lengths. The minimum length will be determined by the physical rack position of the data generator with respect to the rack position of the PI-4002 Instrument Mainframe containing the clock driver cards. In the Pulse Instruments System 4700 these cable lengths are approximately 14 feet.

The driver output cables, T_{DOC} (1) through T_{DOC} (n), to the test head or DUT socket should also be the same length.

The minimum length of these cables is determined by the physical position of the PI-4002 Driver Cards with respect to the test head or DUT socket. These cables should be as short as possible.

Within limits, the shorter these coax cables are, the better the signal bandwidth the device under test. The coax interconnection cables are required to have a nominal impedance, Z_0, of 50 Ohms.

We recommend the use of either RG58C/U or RG58A/U for the driver output cables. Both cables are 50 Ohm nominal characteristic impedance with a low DC series resistance of approximately 4.1 Ohms per 100 feet.

DO NOT use RG58/U or RG58B/U to cable the equipment. The nominal characteristic impedance of these cables is 53.5 Ohms. Using these Cable types will cause signal reflections due to the impedance mismatch.

Smaller diameter coaxial cables, such as RG174/U or RG174A/U, can be used for signal cabling from the data generator to the clock driver inputs. The RG174 type cable has a nominal characteristic impedance of 50 Ohms but has a high DC series resistance, of approximately 10.3 Ohms per 100 feet.

The RG174 type cable is not recommended for either the clock driver outputs or DC bias outputs to the DUT.

When installing the driver input cables, master clock to driver input, T_{DC} (1) through T_{DC} (n), make sure they are connected to the opto inputs of the driver cards. The only exception to this is the 40465 Tri-Level Driver Card. This card has only one input connector (BNC) that serves as the input connector for both the optically isolated input and the non-isolated input. This card must be programmed via the PI-4001 Control Mainframe for optical isolation.

The reason for cabling and /or programming the driver for optical isolation is primarily to reduce noise at the device under test.

The time effect of the optical isolator is important when setting edge coincidence and system timing. An optical isolator will add 25 to 30 nanoseconds to the propagation time of the clock driver. After cabling is installed, the PI-2005 Pattern Generator Master Clock through to the Test Head, edge coincidence can be determined.

Program the PI-2005 or other pattern generator, to have zero nanoseconds of channel delay (if applicable), non-invert, NRZ, 100 nanoseconds period with the bit pattern shown below.

Channel	1 Bits 16	Related Driver Channels
1	10000000000000000	TDC (1)
2	10000000000000000	TDC (2)
3	10000000000000000	TDC (3)
4	10000000000000000	TDC (4)
↓	↓	↓
N-1	10000000000000000	TDC(N-1)
N	10000000000000000	TDC (N)
N+1	10000000000000000	Scope Trigger

The Instruction Entry and Editing Screen on the Timing Generator should have the following entries:

L1 Begin 1

L2 Subpattern 1X1

Refer to the Timing Generator Operators Manual for instructions on programming the instrument.

After programming the pattern generator, the clock drivers must be programmed for a specific set of conditions. Set all drivers for maximum amplitude, swinging around ground. (20 Volt amplitude, V High Level and V Low Level set for +10 V and –10V respectively in the case of Pulse Instruments 4000 Series Drivers.) Program the Rise and Fall times for the fastest times. Driver delay circuits, if applicable, should be programmed for minimum delay. If you have a Tri-Level Driver Card, program the output for two levels with opto coupling.

After the above instrumentation is programmed, set the, Timing Generator to "RUN" and the clock driver Control Mainframe, "ONLINE".

The oscilloscope should be triggered from the pattern generator channel N+1 and a single coax cable or probe should be used to make the relative time measurements of each channel. Using the same cable/probe into the same vertical channel of the oscilloscope will eliminate any difference in the time measurements that could be caused by dissimilar cable lengths or the slight differences in oscilloscope propagation times of the vertical channels.

It is anticipated that the propagation time from the master clock output to the test head input will be around 100 nanoseconds. The trigger bit is set one clock period (100ns) after the driver data bits, therefore it should be possible to display the driver edge on a horizontal sweep of 2 ns or 5 ns per division.

Measure all waveforms at the 50% point of the rising (leading) edge. Note the delta time difference between the leading edges of each driver output. Refer to Table 6-1 for approximate propagation times of the available drivers.

TABLE 6-1

Clock Driver Propagation Times

Model	Description	T_{PD}
40460	8 to 10 MHz Dual Channel	83-87ns
40465	Tri-Level Driver (Opto Input)	75-85ns
40465	Tri-Level Driver (TTL Input)	58-62ns
40490	65 MHz Driver (Opto Input)	45-55ns
40490	65 MHz Driver (TTL Input)	20-24ns

NOTE: The propagation ties T_{PD} are determined with risetime set at minimum, amplitude set for 10 V swing around ground. Times may vary slightly out of the above range due to performance of the opto-isolator.

As you can see from Table 6-1, and verify with your measurements, there can be a variation in the overall propagation time to the DUT or test head. This delta time of edge coincidence can vary from several nanoseconds to possibly 40 nanoseconds, depending upon the combination of clock driver models within the system.

At this point in time, we also have enough information to estimate the path delay or propagation time from the Master Clock output to the DUT input.

If we apply and approximate or rule of thumb estimate to the propagation time of the coaxial cable, both RG-58 and RG-174 cable have an approximate propagation time on 1.5 nanoseconds per foot.

If we know the lengths of the interconnecting cables, an overall estimated propagation time from master clock to DUT can be determined. Refer to Figure 6-1.

T_P (MC to DUT) is approximately: $T_{DC} + T_{PD} + T_{DOC}$

Assuming: T_{DC} These cables are fourteen feet in length.

T_{PD} Using a 40460 Clock Driver Card

T_{DOC} These cables are six feet in length.

Then: $T_{DC} = 14 \times 1.5ns = 21$ nanoseconds

$T_{PD} = 85$ nanoseconds

$T_{DOC} = 6 \times 1.5ns = 9$ nanoseconds

T_P (MC to DUT) is Approximately 21ns + 85ns + 9ns = 115ns.

There are various techniques to provide a fixed delay to align the clock edges. It is strongly recommended not to use the channel delay of the pattern generator for any adjustment greater than 3 nanoseconds, because you will need to remember to program this adjustment every time.

The technique used most of the time is trimmed coax cables. Given the propagation time of coax cable, 1.5ns/ft, it is reasonable to expect delay cables can be made within 125 to 250 picoseconds. This only requires making the cable within an inch or two of the correct length in time.

For example:

We have measured the time difference between the two driver channels to be 10 nanoseconds. These drivers need an edge coincidence within 1 nanosecond.

We need to make a cable of 6.67 feet long i.e. (10/1.5)= 6.67

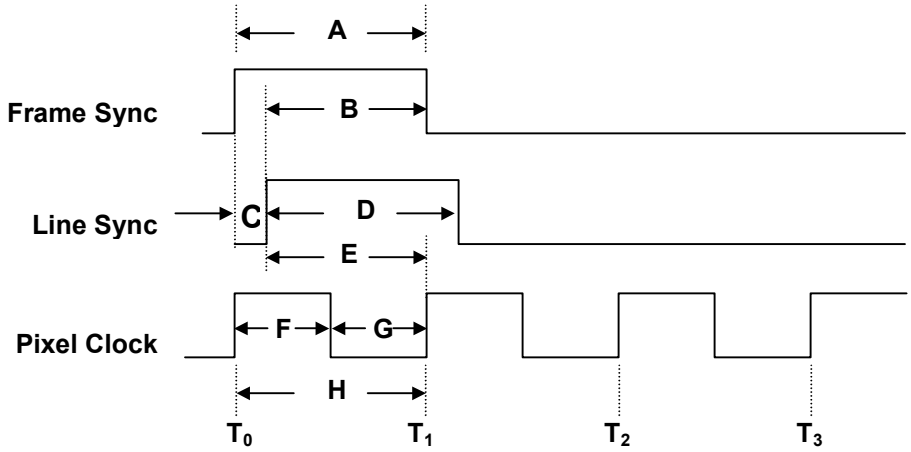
This equates to a cable that is 6 feet 8 inches. This cable is placed in the path between the Timing Generator output and the signal input to the driver with the shortest overall propagation time. The edge coincidence should be within one nanosecond.

All of the driver rising edges can be aligned using this technique. Fixed delays of 30 nanoseconds, which would be 20 feet of coax should be done with the larger diameter cable, either RG-58C/U or RG-58A/U.

7.3. Frame Sync, Line Sync And Pixel Clock Timing Relationship

The second sub timing issue is the time relationship between the signals enabling the PI-4005 Data Acquisition System. These signals are: Frame Sync, Line Sync, and Pixel Clock. In figure 6-1, these delays are labeled T_{DFC}, T_{DLC}, and T_{DPC}.

Figure 6-2 Shows the minimum timing requirements for the Frame Sync, Line Sync, and Pixel Clock, labeled “A” in Figure 7-2.



A	**32 ns (min.)**	**Frame HI level duration**
B	**0 ns (min.)**	**Line HI to Frame LOW**
C	**32 ns (min.)**	**Frame HI to Line HI**
D	**20 ns (min.)**	**Line HI level duration**
E	**20 ns (min.)**	**Line HI to Pixel HI**
F	**10 ns (min.)**	**Pixel HI level duration**
G	**40 ns (min.)**	**Pixel LOW level duration**
H	**100 ns (min.)**	**Pixel period**

Figure 6-2

Frame Sync and Pixel Clock should be nearly coincident in time (T_0), as shown in Figure 6-2. The time delay from the rising edge of FRAME to the rising edge of LINE (C in Figure 6-2) is a fixed delay for all operating frequencies of 10 MHz and below.

The minimum pixel clock period, H, is determined by the maximum operating frequency of the A/D. The Pixel Clock, if operated from a Pulse Instruments pattern generator, will typically have a duty cycle of 50%, although the specification as shown in Figure 6-2 can have a duty cycle variance of 10% to 60%.

Analyzing the time relationships in Figure 6-2, specifically times C, E, and H, shows the range for delay time C is from a minimum of 32 ns to a maximum of 80 ns with respect to time T_0.

In order to determine the cable lengths required for the Frame Sync, Line Sync, and Pixel Clock, we need to estimate the total delay time for the Stimulus/Data Out Path. Table 6-2 defines the remaining non-cable propagation times of the PI-4007 Preamplifier and the Data Acquisition Card.

TABLE 6-2

PI-4007 Preamplifier and Data Acquisition Card Propagation Times		
Instrument	**Figure 1 Mnemonic**	**Propagation Times**
Preamplifier	T_{PPA}	7-8 nanoseconds
A/D	T_{PVD}	40 nanoseconds
A/D	T_{PCC}	115 nanoseconds
A/D	T_{VDS} (variable)	25 nanoseconds (minimum)

Using the values previously derived for the drivers and the values above we can solve the delay equations for Stimulus/Data Out Paths:

Stimulus/Data Out Equation:

$$T_{DSP} = T_{DC} + T_{PD} + T_{DOC} + T_{DDC} + T_{PPA} + T_{DVD} + T_{PVD}$$

$$T_{DSP} = 14 \text{ ns} + 85 \text{ ns} + 9 \text{ ns} + T_{DDC} + 7 \text{ ns} + T_{DVD} + 40 \text{ ns}$$

$$T_{DSP} = 155 \text{ ns} + T_{DDC} + T_{DVD}$$

Measurement Path Equation

$$T_{DMP} = T_{DPC} + T_{PCC} + 25 \text{ ns}$$

$T_{DMP} = T_{DPC} + 115\ ns + 25\ ns$

$T_{DMP} = 140\ ns + T_{DPC}$

When the cable delay T_{DPC} for the Pixel Clock is defined, we have also defined the cable lengths for Frame Sync and Line Sync.

The cable from the DUT output to the PI-4007 Preamplifier Input should be as short as possible. A typical length would be approximately 24 inches. Using the rule of thumb for coaxial propagation time gives TDDC as 3 nanoseconds.

A typical length for the interconnecting coax from the PI-4007 Preamplifier Output to Pixel Clock Input of the Data Acquisition Card is approximately seven feet. A cable of this length will have a propagation time of 10.5 nanoseconds.

Therefore:

$T_{DSP} = 155\ ns + T_{DDC} + T_{DVD}$

$= 155\ ns + 3\ ns + 10.5\ ns$

$T_{DSP} = TDMP = 140\ ns + T_{DPC}$

$T_{DPC} = 28.5\ ns$

The coaxial cable connecting the Master Clock Output (PI-2005) to the Pixel Clock input of the Data Acquisition Card should be 19 feet long, given the above set of cable lengths. Refer to Figure 6-3 (next page) for a summation of the above propagation time analysis.

The cable length of the Frame sync is the same as the Pixel Clock, 19 feet. The cable length for Line Sync will need to take into consideration the 32 nanosecond delay offset plus the length of the Pixel Clock Cable. Therefore, the Line sync Cable should be approximately 40.5 to 41 feet.

Setting up the timing as per the timing diagram is the most important part of the setup.

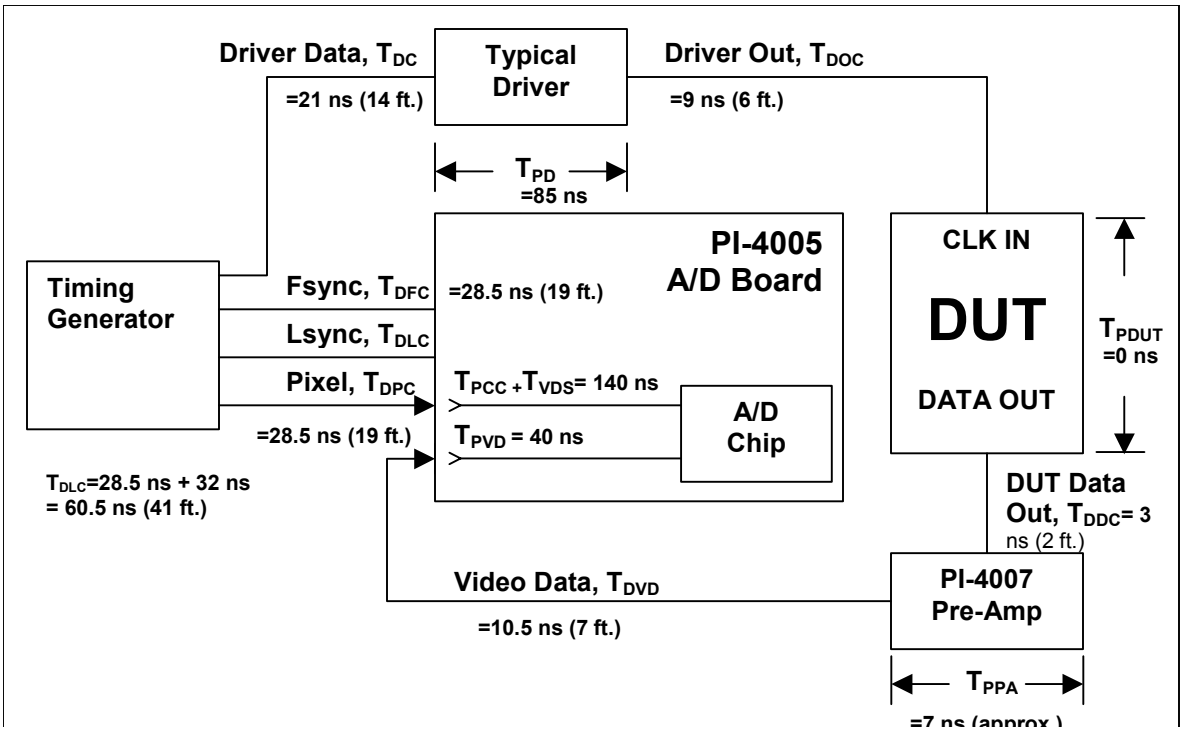


Figure 6-3

7.4. Timing Requirements That Must Be Met

There are three timing requirements that must be met:

1. The Line sync must have one positive transition within the Frame Sync high time. This means that Frame Sync must have setup time prior to the Line Sync's rising edge.

2. The Pixel Clock must have one positive transition with the Line Sync high time. The best way to achieve this is to make the Frame and Line sync one pixel clock in duration and delay the Line Sync 32ns. This will meet the timing requirements.

3. The number of Pixel Clocks presented to the A/D input must be at least one more than the total of the pixel skip and pixel pass, and the number of Line syncs presented to the A/D must at least equal the total of the line skip and line pass as setup in the Area of Interest in the A/D Digital property page.

The extra Pixel Clock is required because the A/D discards the first pixel of each line, that is the pixel that has the rising edge in the line sync period. Normally the extra pixel is not a problem since most FPA's and CCD's have dead pixels at the edges of the array.

By presenting the A/D with the number of dead and active pixels in the array row, you can then set the pixel skip and pixel pass registers accordingly. For example, if your device has 536 total pixels in the array row, and 6 were dead and 500 were active, you would set the Pixel Skip for 6, and the Pixel Pass for 500.

IF the array has no dead pixels at the edges, the A/D will require an extra clock at the end of each line.

For some devices the video changes on both the rise and fall of the clock applied to the device. In this case, the Pixel Clock applied to the A/D must be half the period of the clock applied to the device.

You must analyze the timing requirements of the device to determine where in the timing to place the Frame, Line, and Pixel Clocks.

Obviously, the Pixel Clock must be placed wherever video will be output. Line Sync will be placed in the timing at the start of each line when a new row of pixels is loaded into the output shift register. The Frame Sync will be placed at the same place as the Line Sync, but only in the first row of the array.

For linear array, the timing is easier; the Frame and Line Syncs are the same, except for the previously mentioned 32 ns skew in the line sync. The pixel clock is placed wherever the video output changes.

7.5. Set Up After Timing Requirements Met

Once the clocking for the device under test has been established, the next step is to setup the software.

Refer to Section 5, Software, of the manual for a description of the software settings described below.

On the Digital property page, select the type of clocking you intend to use from the Clock Source Box, and select the method of clock connection you intend to use.

Set the area of interest register and number of frames, keeping in mind the requirements regarding dead and active pixels and the total available memory on the acquisition card.

Once the correct number of frame cycles has been run, the A/D will stop automatically. There is no need to put an extra frame clock at the end of the last frame.

Set the Pixel Period. The period that is entered here is the period of the Pixel Clock at the input of the Data Acquisition Card, and is the period value of the clock from leading edge to leading edge. Setting the period to a value that is less than the actual period will reduce the adjustable delay range of the Convert and Clamp Clocks.

The total adjustable delay will be approximately 15% - 98% of the actual pixel clock period. Setting the period too high may result in no data being collected, or may result in a very coarse delay setting.

The final setting in the digital setup would be to position the Convert Clock into the valid video portion of the signal. This is done by connecting a scope to the VID MON and CONV CLK BNCC connectors, and positioning the clock where desired in the valid video area. If there is no video or the video is drastically offset from zero, use the Analog property page to adjust the position of the signal into the range of the ADC (approximately ±2 V).

For best resolution, set the gain for maximum amplitude that does not clip (2.0 V max. If the offset of the device is known, it can be entered directly. Set the filter for a value that is closest to the pixel period.

If the PI-4007 Preamplifier Module is being used additional offset can be corrected using the Preamplifier property page. The PI4007 Global Offset can be monitored by connecting a DVM to the J303 GL OUT MONITOR BNC connector on the Preamplifier control card (available at the rear of the PI-4005 Acquisition Mainframe).

You should always set the Preamplifier Global Offset before setting the Data Acquisition Card Global Offset. 'The Preamplifier Global Offset has a wider offset range, and therefore, has a little less accuracy.

Set the Current Control on the Pre-amp Control Menu to the amount of current the device output expects to see.

For example, if the device should be sinking 0.75mA for normal operation, then set the current to 0.75mA. At the present the current control is set up from the devices point of view, e.g. at a negative current setting, the device is sinking current. In the positive current setting, the device is sourcing current. A change in the current control is planned to provide a clearer picture of the current control as well as a limit for the current control. The current control will be from zero to 2mA with a selection button to indicate direction of current and maximum current. The direction of the current can only be changed when the current is at zero.

Assuming the PI-4000 has been setup and the Timing Generator is running the proper pattern for the device, the next step is to click Setup button in the control section to set up the hardware. Clicking the Start Acq button will arm the system and initiate the data acquisition.

To verify time placement of the clocks with respect to the video data, set up the following test.

Connect a clock output cable T_{DOC} to the input cable T_{DDC} of the PI-4007 Preamplifier. Using a real time oscilloscope with at least tow vertical input channels, connect "VID MON' and "CONV CLK" output BNC'S to the inputs of the oscilloscope. These connecting cables should be of the same length, terminated into 50 Ohms.

Program the connected clock High Level for +1Volt and the Low Level to –1 Volt.

Program your Timing Generator to give the selected clock channel one bit, the Frame Sync two bits, Line Sync two bits, and the Pixel Clock for ten clocks. The bit pattern should be the following, with the subpattern set from bit one to bit 20.

	Bits
Channel	1 20
Selected Clk	10000000000000000000
Frame Sync	11000000000000000000
Line Sync	11000000000000000000
Pixel Clk	10101010101010101010

Set the Timing Generator period for 100 nanoseconds. The Timing Generator Instruction Entry and Editing Menu should have the following entries.

L1 Begin 1

L2 Subpattern 1 x 1

Refer to the Timing Generator Operators Manual for instructions on programming the instrument.

Using the PI-DATA Software in the digital menu, set the A/D for a Line Pass =1, Line Skip = 0, Pixel Pass = 8, and Pixel Skip =0.

IN the analog menu, set the Meas Strobe for 50% delay. Set the A/D pixel period for 200ns, the A/D Gain should be set at unity.

Start the Timing Generator. You do not need the A/D capturing data to view the time relationship between VID MON and CONV CLK outputs.

The A/D Offset, on the Analog Menu, may require a slight adjustment around zero Volts.

The oscilloscope can be triggered on the VID MON signal. By varying the Convert Clock Delay you should see the Convert Clock vary in time with respect to the VID MON signal. When the Convert clock is set to 0% delay, the leading edges of the Convert Clock and video data should be nearly in alignment. If they do not align, adjust the cable length to obtain the appropriate timing.

If the placement of the VID MON and Convert Clock signals are aligned or nearly aligned, data can be taken and displayed.

IN the A/D digital settings menu, set the number of frames to a convenient number such as 5 or 10. The FPA size should be set to x = 8 and y = 1. The Setup button must be clicked to apply the digital setup.

Click the Start Acq button to collect data. The Status text will display “Acquisition Completed” when the selected number of frames has been acquired.

To view the data, click the PI-PLOT button. The collected data will be displayed as an oscilloscope presentation by default, but can be changed to grayscale, false color, or histogram by clicking the appropriate buttons in the PI-PLOT window.

To vary the display, change the number of bits programmed for the clock.

8. SPECIFICATIONS

8.1. PI-4005 Acquisition Mainframe

Backplane:	VME bus 8 Layer High Speed, 12 Slots
Dimensions	
Benchtop:	10.50 " H x 17.5" W x 23.75" D,
Rackmount:	10.50" H x 19.0" W x 23.75"D
Operating Temperature:	20°C to 50°C.
Forced Air Cooling:	Three fans per Mainframe at 94 cfm each with internal plenum chamber, damped, and Mu metal shielded.
EMI/RFI Suppression:	Per MIL-STD-461
Slot Spacing:	0.80" Spacing
Power:	115 or 230 VAC, 47-63 Hz, Jumper selectable.
Power Supply:	For Digital Circuitry—Located in PI-4005 Acquisition Mainframe; analog circuitry requires PI-4008 Analog Power Mainframe.
Output DC Volts:	5 VDC, and ±12 VDC, 500 Watts.
Load Regulation:	±1.5% (60% ±40% load change).
Line Regulation:	0.2% (15% line change).
Noise and Ripple:	1.0% peak to peak.
Temperature Coefficient:	±0.02% / °C maximum.
Weight:	25 lbs.

8.2. PI-4007 Preamplifier Module

Input Power Requirements:	±30 V ± 1% 50 mA per channel (four channels) ±15 V ± 1% 100 mA per channel (four channels) ±5 V ± 1% 25 mA per channel (four channels)
Video Input Load:	
Resistive:	≥ 100 kΩ
Capacitive:	≤ 15 pf
Video Input Signal Characteristics:	
Voltage Range:	± 15V
Global Offset Range:	20 V_{pp} ± 10V
Signal Amplitude:	10 V_{pp} centered around Global Offset

Video Output Characteristics:

Output Type:	Differential
Output Load:	50Ω Max.
Max. Output Voltage:	10 V_{pp} (differential)
Power Bandwidth:	≥ 30 MHz
Signal Bandwidth:	≥ 40 MHz
Output Noise:	≤ 30 nV/√Hz. At 50 kHz
Settling Time to 12 bits:	≤ 40 nsec.
Output DC Offset:	≤ ±20 mV (differential).
Voltage Gain:	2.0 ± 1% with no back termination (differential). 1.0 ± 1% with back termination (differential).
Ground Noise Rejection:	≥ 50 dB at 1 MHz
Power Supply Rejection Ratio:	≥ 50 dB at 1 MHz
Output DC Drift:	≤ 25 μV/ °C

Global DC Monitor Output:

Gain:	1.0 ± 0.1%
Max Voltage Swing:	± 10 V
Bandwidth:	0.3 Hz ± 0.1 Hz.

8.3. PI-4008 Analog Power Mainframe

Output:	+8 VDC 12 Amps (for Analog Section Only) -8 VDC 12 Amps +5 VDC 5 Amps (For Clean Digital Section Only) +30 VDC 5 Amps -30 VDC 5 Amps
AC Line Input Voltage:	100 VAC, 230 VAC, All ± 10%, 47 – 63 Hz
Ambient Operating Environment:	0 to 50°C Continuous operation under full load and High Line at 50°C ambient.
Temperature Coefficient:	0.01% / °C Maximum
Load Regulation:	0.1% (0% to 100% load).
Line Regulation:	0.2% (± 10% AC line change).
Stability:	± 0.1% Maximum for 24 hours after warm up.

Transient Response:	Recovery to within 1% of nominal Voltage in less than 50 μsec for 50% load change.
Overshoot:	No Voltage spikes on turn-on, turn-off, or power fail.
Overload:	Each supply protected against overload and short circuit conditions. Automatic recovery.
Over Voltage Protection:	1 Volt or 15%, whichever is greater above nominal supply levels.
Remote Sense:	All supplies have remote sensing (4 wire) accommodating power/sense potential difference of 0.5 Volts.
Voltage Adjustment Range:	± 10% all supplies (Front panel access).
Noise and Ripple:	0.1% peak to peak (all supplies).
EMI/RFI Input Filtering:	Shall Meet requirements of FCC 20790 Class B and VDE 0871 Class A.
Transformers:	Individual transformers for each voltage; ±8 V, +5V, ±30V.
Accessibility:	All supplies are accessible through two rear panel connectors. Remote sensing on power out #1 connector only.
Front Panel Display:	Voltage and current display for each supply Overload Indication for each supply.

8.4. 40502 VME to PCI Adapter

VME bus Access:	Memory Mapped
Bus Communication:	Computer acts as bus master allowing memory references to it to pass to the VME bus.
Addressing:	A0-A15
Data Accesses:	D0-D15
Bus Arbitration:	Release on Request (ROR).

Access Times and Data Rates:

PCI read/write access to remote RAM:	2.2 μsec.
PCI read/Write access to dual port RAM:	2.1μsec.
VME bus read/write access to dual port RAM:	400 nsec

Interrupt Passing:

Number of Interrupts:	7 (IRQ7-IRQ1).
Programmed Interrupt Pass:	Write to I/O register.
Read-Modify-Write:	Simulated by a bus lock control bit in control register
Interrupt Acknowledge:	Through Control Register.
Power Requirements:	VMEbus adapter, 3.5 A at 5 V. PCI Adapter, 3.0 at 5 V.

8.5. Data Acquisition Cards

8.5.1. 40517 10 MHz 12 Bit

Amplifier Input:	Differential or Single Ended
Maximum Input Voltage:	±5V offset, 5V signal, sum not to exceed ±7.5 Volts.
Input Load Resistance:	50, 75 and 100 Ohms, factory installed, jumper selectable. User may select other values.
Global DC Control:	Independent microprocessor control of global DC offsets for each channel.
Logic Type:	TTL Binary
Resolution:	16 bit.
Range:	± 5 Volts.

Gain Control

Logic Type:	TTL Binary
Accuracy:	± 1%.

Filter Control

Logic Type:	TTL Binary
Filter Type:	Low Pass Single Pole
Frequency Cutoff (-3db):	1 kHz, 10 kHz, 100 kHz, 1 MHz, 10MHz, and Select (defined at time of order).

Video Processing Characteristics

Resolution:	12 bits
Maximum Pixel Rate:	10 MHz
Maximum Signal Bandwidth:	DC to 25 MHz, Correlated Double Sample and Hold disconnected.

Input Referred Noise:	≤ 25 μV (DC to 1 MHz) at Gain 64. ≤ 50 μV (DC to 5 MHz) at Gain 64.
Slew Rate to A/D:	≥ 200 V/μ sec
Input Offset Drift:	≤ 10 μ V / °C.
Settling Time to 12 bits:	40 nsec.
Signal Coupling:	DC at input.
Input Voltage Range:	± 5V offset, 5V signal, sum not to exceed ± 7.5V.
Sampling:	All Inputs Simultaneous.
Global Input Programmable Gain:	¼, ½, 1, 2, 4, 8, 16, 32, and 64.
Global Input Offset Range:	Programmable in range of ± 5 V; 16 bits resolution. (See also PI-4007 Preamplifier Module).
Optical Isolation:	47 Optically isolated lines. Complete isolation between analog and digital sections.
Correlated Double Sampling:	Programmable sampling, programmable 10kHz to 10 MHz pixel rate.
A/D Accuracy:	± 1 LSB
Memory:	16 Megabytes RAM.
Area of Interest:	Maximum Frame size 2048 x 2048 pixels. Minimum Frame Size 4 Pixels.
Analog Buffer Output Connector:	BNC (video monitor).
Post A/D Buffer Output Connector:	BNC (A/D monitor).
Frame Sync Input Connector:	BNC
Line Sync Input Connector:	BNC
Clock Input Connector:	BNC

8.5.2. 40527 2 MHz 16 Bit

Amplifier Input:	Differential or Single Ended.
Maximum Safe Overload Protection:	± 20 V.
Signal Coupling:	DC
Input Voltage Range:	± 10 Volts.
Sampling:	All Channels Simultaneous.
Input Programmable Gain:	1, 2, 4, 8, 16, 32, and 64.
Global Input Offset Range:	Programmable in range of ± 5 V; 16 bits resolution.
Optical Isolation:	47 Locations, all inputs and A/D output to RAM.
Double Correlated Sample and Hold:	Selectable sampling points, programmable.
A/D Accuracy:	±1.5 LSB
Area of Interest:	Maximum frame size 2048 x 2048 pixels. Minimum frame size 4 Pixels.
Analog Buffer Output Connector:	BNC (video monitor).
Post A/D Buffer Output Connector:	BNC (A/D monitor).
Frame Sync Input Connector:	BNC
Line Sync Input Connector:	BNC
Clock Input Connector:	BNC

8.5.3. 40537 5 MHz 14 Bit

Amplifier Input:	Differential or Single Ended.
Maximum Safe Overload Protection:	± 20 V.
Signal Coupling:	DC
Input Voltage Range:	± 10 Volts.
Sampling:	All Channels Simultaneous.

Input Programmable Gain:	¼, ½, 1, 2, 4, 8, 16, 32, and 64.
Global Input Offset Range:	Programmable in range of ± 5 V; 16 bits resolution.
Optical Isolation:	47 Locations, all inputs and A/D output to RAM.
Double Correlated Sample and Hold:	Selectable sampling points, programmable.
A/D Accuracy:	±1.5 LSB
Area of Interest:	Maximum frame size 2048 x 2048 pixels. Minimum frame size 1 Pixel.
Analog Buffer Output Connector:	BNC (video monitor).
Post A/D Buffer Output Connector:	BNC (A/D monitor).
Frame Sync Input Connector:	BNC
Line Sync Input Connector:	BNC
Clock Input Connector:	BNC

8.5.4. 40547 40 MHz 10 Bit

Amplifier Input:	Differential or Single Ended.
Maximum Safe Overload Protection:	± 20 V.
Signal Coupling:	DC
Input Voltage Range:	± 10 Volts.
Sampling:	All Channels Simultaneous.
Input Programmable Gain:	1, 2, 4, 8, 16, 32, and 64.
Global Input Offset Range:	Programmable in range of ± 5 V; 16 bits resolution.
Optical Isolation:	47 Locations, all inputs and A/D output to RAM.
Double Correlated Sample and Hold:	Selectable sampling points, programmable.
A/D Accuracy:	±1.5 LSB

Area of Interest:	Maximum frame size 2048 x 2048 pixels. Minimum frame size 2 Pixels.
Analog Buffer Output Connector:	BNC (video monitor).
Post A/D Buffer Output Connector:	BNC (A/D monitor).
Frame Sync Input Connector:	BNC
Line Sync Input Connector:	BNC
Clock Input Connector:	BNC

8.6. 40511 Preamplifier Controller Card

Two PI-4007 Preamplifier Modules (eight channels) can be controlled by a single controller card.

Current Load Control

Voltage Range:	0 to +2.0 Volts
Resolution:	8 bits.
Input Resistance:	≥100 kΩ.
Control Bandwidth:	0.3 Hz ± 0.1 Hz.
Global DC Control:	Each control Card supplies independently controlled analog input Voltages to eight preamplifier channels.
Voltage Range:	±10 Volts.
Resolution:	16 bits.
Input Resistance:	≥100 kΩ.
Control Bandwidth:	0.3 Hz ±0.1 Hz.

Preamplifier Logic Select:

Input	Channel
00	1 or 1-4 (multiplexed)
01	2
10	3
11	4

9. APPENDIX

9.1. Frequency Response Vs Gain Chart

The following table shows the typical frequency response vs. gain of the 40517 10 MHz 12 bit Data Acquisition Card. (Values shown in dB)

Gain=	0.25	0.50	1.00	2.00	4.00	8.00	16.00	32.00
100Hz	12.02	6.00	0.02	0.01	0.01	0.00	0.00	-0.01
1kHz	12.04	6.03	-0.02	-0.02	0.03	0.00	-0.02	-0.05
10kHz	12.00	6.01	-0.04	-0.03	-0.05	-0,04	-0.01	-0.06
100kHz	12.00	6.01	-0.02	-0.01	-0.04	-0.05	0.00	-0.03
1MHz	11.99	6.01	-0.01	0.01	0.00	-0.04	0.06	-0.02
3MHz	11.99	5.98	0.02	-0.02	-0.02	0.01	0.03	-0.03
5MHz	11.95	5.97	0.05	-0.03	0.00	0.00	0.01	-0.01
10MHz	11.67	5.88	0.21	-0.11	0.05	0.12	-0.10	-0.05
20MHz	11.41	5.84	0.36	0.35	0.31	0.65	-0.15	-0.23

9.2. Noise Vs. Gain Chart

The following figure shows the typical noise vs. gain of the 40517 10 MHz 12 bit Data Acquisition Card.

Gain	Noise at A/D Input Incl. A/D (nV/√Hz)	Input Noise (nV/√Hz)	Total Noise (nV/√Hz)
64	1783	27.9	1889
32	940	29.4	1129
16	522	32.6	814
8	225	28.0	664
4	119	29.8	636
2	72	36.0	629
1	48	48.0	627

Total Noise = $(A/Dn)^2$ + (In2)

The A/D converter has a typical Signal to Noise Ratio of –66db or 625 (nV/√Hz).

At gains of 16 or less, the total noise is dominated by the A/D converter noise of 625 (nV/√Hz). The total noise is measured at the output of the A/D.

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