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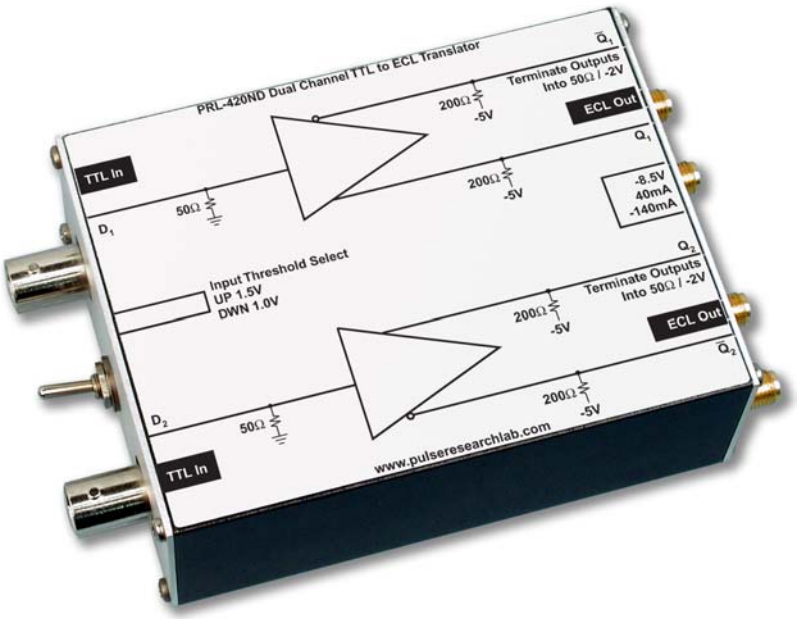
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PRL-420ND DUAL CHANNEL TTL TO NECL LOGIC LEVEL TRANSLATOR
PRL-420PD DUAL CHANNEL TTL TO PECL LOGIC LEVEL TRANSLATOR
PRL-420LPD DUAL CHANNEL TTL TO LVPECL LOGIC LEVEL TRANSLATOR

APPLICATIONS

- **Converting TTL/CMOS signals to Differential NECL/PECL/LVPECL Signals**
- **High Speed Digital Communications system testing**
- **High Speed SONET Clock Level Translation**
- **Converting TTL/CMOS Clocks to NECL/PECL Clocks for connection to Transient Recorders**



FEATURES

- **f_{max} > 300 MHz**
- **750 ps/1100 ps t_r for PRL-420ND/420PD**
- **50 Ω TTL/CMOS Input**
- **1.5V or 1V Selectable Input Threshold**
- **Complementary NECL/PECL Outputs**
- **BNC Input/SMA Output Connectors**
- **DC Coupled I/O's**
- **Self-contained 1.3 x 2.9 x 3.9-in. units including AC/DC Adapters**

DESCRIPTION

The PRL-420ND and PRL-420PD are, respectively, dual channel TTL/CMOS to NECL and TTL/CMOS to PECL Logic Level Translators. Each unit has a switch-selectable 1.5V or 1V input threshold voltage. The PRL-420ND has a pair of complementary NECL outputs suitable for driving 50 Ω loads terminated to -2V. The complementary PECL outputs from the PRL-420PD are suitable for driving 50 Ω loads terminated to +3V. The outputs of both units can also drive AC coupled or floating 50 Ω.

These Logic Level Translators are designed specifically for use in testing and interfacing of high speed digital communications circuits, where conversions from TTL/CMOS level signals to NECL and PECL level signals are often required. They are ideal building blocks that complement other PRL Logic Level Translators, such as the PRL-450ND, PRL-450PD, PRL-460NPD and PRL-460PND, etc. in systems integration applications where interconnections of mixed logic signals are often necessary.

They are ready-to-use functional modules housed in 1.3 x 2.9 x 3.9-in. extruded aluminum enclosures and are supplied with ±8.5V AC/DC Adaptors. Both units have BNC input connectors and SMA output connectors. Block diagrams of these Logic Level Translators are shown in Fig. 1A and Fig. 1B.

If mounting is desired, a pair of 35001420 mounting brackets can accommodate two PRL modules of the same length. A number of PRL modules can also share a single ±8.5V AC/DC adaptor using the PRL-730 or PRL-736 voltage distribution module. Please see the Accessories Section for more detail.

PULSE RESEARCH LAB

1234 Francisco Street, Torrance, CA 90502
Tel: 310-515-5330 Fax: 310-515-0068
Email: sales@pulseresearchlab.com
www.pulseresearchlab.com

*SPECIFICATIONS (0^{o} C ≤ T_A ≤ 35^{o}C)

Unless otherwise specified, dynamic measurements are made with all outputs terminated into 50Ω/V_{TT}.

SYMBOL	PARAMETER	PRL-420ND			PRL-420PD			UNIT
		Min	Typ	Max	Min	Typ	Max	
R_{in}	Input Resistance	49.5	50	50.5	49.5	50	50.5	Ω
R_{out}	Output Resistance		NPN emitter		49.5	50	50.5	Ω
V_{TosH}	Input Threshold Voltage (High)	1.4	1.5	1.6	1.4	1.5	1.6	V
V_{TosL}	Input Threshold Voltage (Low)	0.9	1.0	1.1	0.9	1.0	1.1	V
V_{OL}	Output Low Level	-1.85	-1.7	-1.55	3.2	3.4	3.5	V
V_{OH}	Output High Level	-1.0	-0.8	-0.7	3.9	4.1	4.3	V
I_{DC}	DC Input Current		35 -132	45 -145		180 -315	200 335	mA
V_{DC}	DC Input Voltage	±7.5	±8.5	±12	±7.5	±8.5	±12	V
V_{AC}	AC/DC Adapter Input Voltage	103	115	127	103	115	127	V
t_{PLH}	Propagation Delay to output ↑		1.5			2		ns
t_{PHL}	Propagation Delay to output ↓		1.5			2		ns
t_r/t_f (1)	Rise/Fall Times (20%-80%)		750	850		1100	1250	ps
t_{SKEW}	Skew: Vo↑↔ Vo↓		200	500		200	500	ps
t_{SKEW}	Skew: Vo1↑↔ Vo2↑		200	500		200	500	ps
f_{max} (2) V_{TosH}	Max Clock Frequency Input Threshold Voltage (High)	200	300		200	300		MHz
f_{max} (2) V_{TosL}	Max Clock Frequency Input Threshold Voltage (Low)	300	400		300	400		MHz
	Size		1.3x2.9x3.9			1.3x2.9x3.9		in.
	Shipping Weight, incl. AC adapter		3			3		lb.

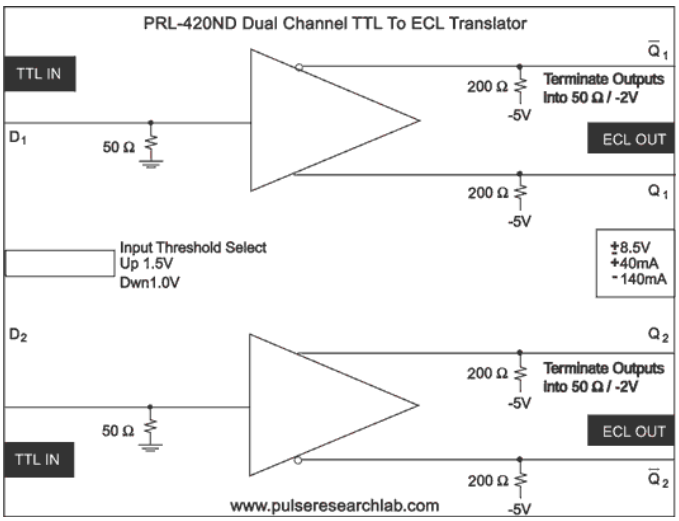


Fig. 1A PRL-420ND Block Diagram

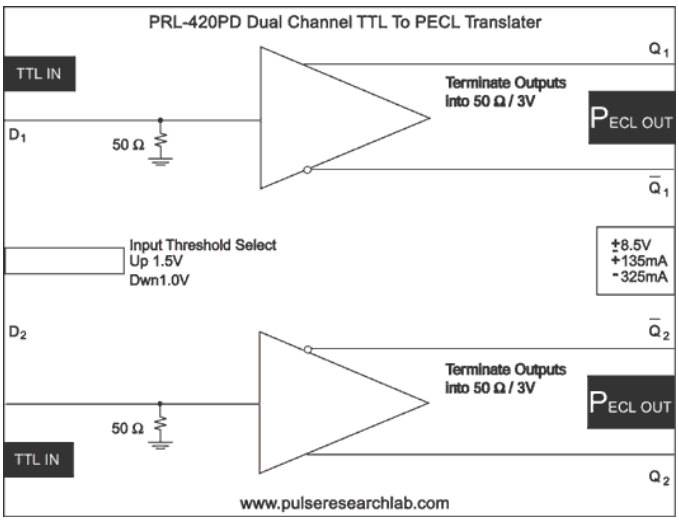


Fig. 1B PRL-420PD Block Diagram

Notes:

(1). The output rise and fall times are measured with both the Q and $\overline{Q}$ outputs terminated into 50 Ω/V_{TT}, using the PRL-550NQ4X/PRL-550PQ4X, four channel NECL/PECL Terminators, connected to a 50Ω input sampling oscilloscope. V_{TT} =-2V for NECL and +3V for PECL. If either output is left unterminated, both the rise and fall times will increase by approximately 15%, due to slight degradation of the pulse corners.

(2). f_{MAX} for the PRL-420ND is measured by connecting its inputs to the PRL-450ND, NECL to TTL Logic Level Translator, and its outputs to the ÷2 differential inputs of the PRL-255N NECL frequency divider. The outputs of the PRL-255N are then measured using the PRL-550NQ4X, four channel NECL Terminators, connected to a 50 Ω input sampling 'scope. Similarly, f_{MAX} for the PRL-420PD is measured using the PRL-450PD as the input driver, and its outputs are connected to the differential inputs of the PRL-255P PECL frequency divider. The outputs of the PRL-255P are then measured using the PRL-550PQ4X, four channel PECL Terminators, connected to a 50 Ω input sampling 'scope.

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