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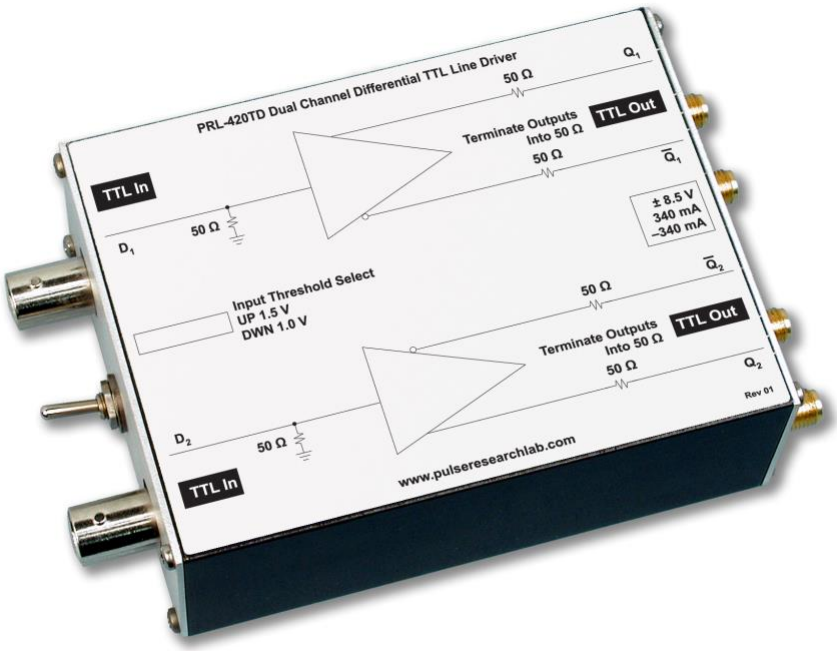
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PRL-420TD DUAL CHANNEL DIFFERENTIAL TTL LINE DRIVER

APPLICATIONS

- **Converting TTL/CMOS signals to Differential TTL Signals**
- **Converting TTL/CMOS Signals to RS422-compatible Signals**
- **High Speed Digital Communications Systems Testing**
- **Differential Long Line Drivers**



FEATURES

- **f_{max} > 250 MHz**
- **1.2 ns Typical Output Rise & Fall Times**
- **TTL Compatible 50 Ω Input**
- **1.5 V or 1.0 V Selectable Input Threshold**
- **Complementary 50 Ω Outputs**
- **BNC Input/SMA Output Connectors**
- **DC Coupled I/Os**
- **Self-contained 1.3 x 2.9 x 3.9-in. unit**
- **Includes AC/DC Adapter**

DESCRIPTION

The PRL-420TD is a dual channel single-ended input, differential output TTL Line Driver. Each channel has a 50 Ω TTL/CMOS compatible input and a pair of differential 50 Ω outputs for driving long lines, in excess of 100 ft, with or without 50 Ω terminations. The input threshold voltage can be selected between 1.5 V and 1 V using a front panel switch. The 1 V threshold makes easy interfacing with 3.3V TTL/CMOS devices.

The PRL-420TD is intended for use in testing and interfacing of high speed digital communication circuits, where conversion from single-ended TTL/CMOS level signals to differential signals is often required. The differential outputs are ideal for driving RS422 input circuits and for high speed ADCs where a differential clock input is often required. The PRL-420TD complements other PRL-series Level Translators, such as the PRL-420ND/PD, PRL-450ND/PD, and PRL-460NPD/PND, etc., in system integration applications where interconnections among different logic signals are often necessary.

The PRL-420TD is a ready-to-use functional module housed in a 1.3 x 2.9 x 3.9-in. extruded aluminum enclosure and is supplied with a ±8.5V AC/DC Adapter. BNC input and SMA output connectors are provided. A block diagram showing the equivalent input and output circuits of the PRL-420TD is shown in Fig. 1.

The PRL-420TD may be ordered without a power supply as "PRL-420TD-OEM" or with a NRTL-approved power supply (equivalent to PRL-765-1) as "PRL-420TD-NRTL".

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SPECIFICATIONS (0^0 C ≤ T_A ≤ 35^0C)

Unless otherwise specified, dynamic measurements are made with all outputs terminated into 50Ω.

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comments
R_{IN}	Input Resistance	49.5	50.0	50.5	Ω	
R_{OUT}	Output Resistance	49.5	50.0	50.5	Ω	
V_{TOSH}	Input Threshold Voltage (high)	1.4	1.5	1.6	V	
V_{TOSL}	Input Threshold Voltage (low)	0.9	1.0	1.1	V	
V_{IL}	TTL input Low Level	-0.5	0.0	0.5	V	
V_{IHH}	TTL input High Level	1.8	2.0	5.0	V	V_{TOSH}
V_{IHL}	TTL input High Level	1.2	1.3	5.0	V	V_{TOSL}
V_{OL}	TTL Output Low Level	-0.1	0.0	0.5	V	
V_{OH}	TTL Output High Level	2.0	2.5	2.6	V	
I_{DC1}	DC Input Current, +8.5 V		340	360	mA	
I_{DC2}	DC Input Current, -8.5 V	-360	-340		mA	
V_{DC}	DC Input Voltages	±7.5	±8.5	±12	V	
V_{AC}	AC/DC Adapter Input Voltage	103	115	127	V	
T_{PLH}	Propagation Delay to output ↑		2		ns	
T_{PHL}	Propagation Delay to output ↓		2		ns	
t_r/t_f	Rise/Fall Times (10%-90%)		1.2	1.4	ns	Note (1)
T_{SKEW}	Skew between any 2 outputs		150	400	ps	
f_{max}	Max Clock Frequency	250	300		MHz	Note (2)
	Size	1.3 x 2.9 x 3.9			in.	
	Weight	5			Oz	

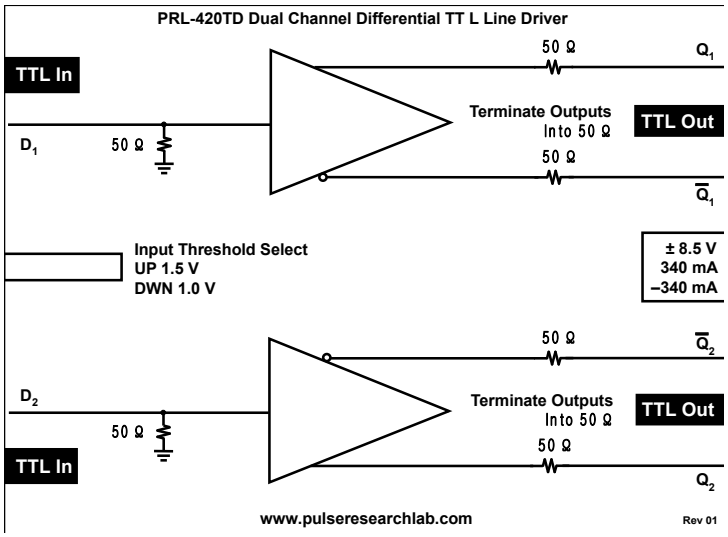


FIG. 1 PRL-420TD Block Diagram

Notes:

(1). The output rise and fall times are measured with both the Q and $\overline{Q}$ outputs terminated into 50 Ω. If an unused complementary output is left unterminated, a slight increase in rise and fall times will result.

(2). f_{MAX} is measured by connecting its inputs to the PRL-177A-500 clock generator, and its outputs to the sampling scope through a pair 26 dB attenuators. The input threshold voltage is set to 1.5 V.

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