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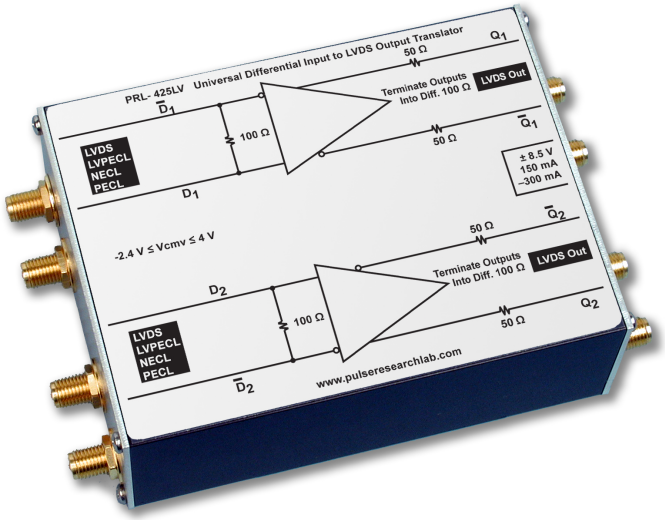
PRL-425LV DUAL CHANNEL, UNIVERSAL DIFFERENTIAL RECEIVER, LVDS OUTPUTS

APPLICATIONS

- Differential LVDS, LVPECL, NECL, PECL, RS422 or TTL to LVDS Logic Level Translation
- LVDS Line Driver
- Mini Modular Instrument for interfacing with High Speed Data Communications Equipment

FEATURES

- 500MHz maximum Clock Rate
- Floating 100 Ω Universal Differential Inputs Accept LVDS, LVPECL, NECL, PECL or TTL Inputs
- Differential 100 Ω Outputs for LVDS Interface
- Ready-to-Use 1.3 x 2.9 x 3.9-in. Modules include a ±8.5V/1.4A AC/DC Adapter



PRL-425LV, Universal Differential Receiver, LVDS Outputs

DESCRIPTION

The PRL-425LV is a dual channel, universal differential input to LVDS output translator. The floating 100 Ω inputs are designed for interfacing with differential signals within the common mode range of -2.4V to +4V. Therefore, they are compatible with LVDS, LVPECL, LVTTL/CMOS, NECL, PECL, RS422 or TTL differential input signals. The complementary 100 Ω outputs of the PRL-425LV are designed for driving LVDS input devices, and they will also drive other PRL-425 series modules. They are also long line drivers, designed specifically for use with high speed data communications applications. A functional block diagram of this device is shown in Fig. 1.

The standard unit is supplied with SMA input and output connectors. Models with Triax input and/or Triax output connectors are available by special order.

Each unit is supplied with a ±8.5 V/1.4 A AC/DC Adapter and housed in a 1.3 x 2.9 x 3.9-in. extruded aluminum enclosure. Available accessories include voltage distribution modules and brackets for mounting multiple units.

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*SPECIFICATIONS (0^{o} C ≤ T_A ≤ 35^{o}C)

SYMBOL	PARAMETER	Min	Typ	Max	UNIT
R_{inD}	Differential Input Resistance	95	100	105	Ω
R_{inC}	Common Mode Input Resistance		5K		Ω
I_{DC}	DC Input Current		165/-240	200/-260	mA
V_{DC}	DC Input Voltage	±7.5	±8.5	±12	V
V_{AC}	AC/DC Adapter Input Voltage	103	115	127	V
V_{OHNL}	Output Hi Level, No Load	2.75	3	3.3	V
V_{OHFL}	Output Hi Level, 124Ω load	1.8	2.0	2.2	V
V_{OLNL}	Output Lo Level, No Load	-1.2	-1	-0.8	V
V_{OLFL}	Output Lo Level, 124Ω Load	-0.2	0	0.2	V
t_{PLH}	Propagation Delay to output ↑		2200		ps
t_{PHL}	Propagation Delay to output ↓		2200		ps
t_r/t_f	Rise/Fall Times[1]		1000	1300	ps
fmax I	Max Clock Frequency, SMA[2]	500	580		MHz
fmax II	Max Clock Frequency, Triax[2]	350	450		MHz
t_{SKEW1}	Skew between outputs		250	500	ps
t_{SKEW2}	Skew from unit to units		500	1000	ps
VCM	Input Common Mode Voltage	-2.4		+4	V
	Size		1.3x2.9x3.9		in.
	Weight		5		Oz

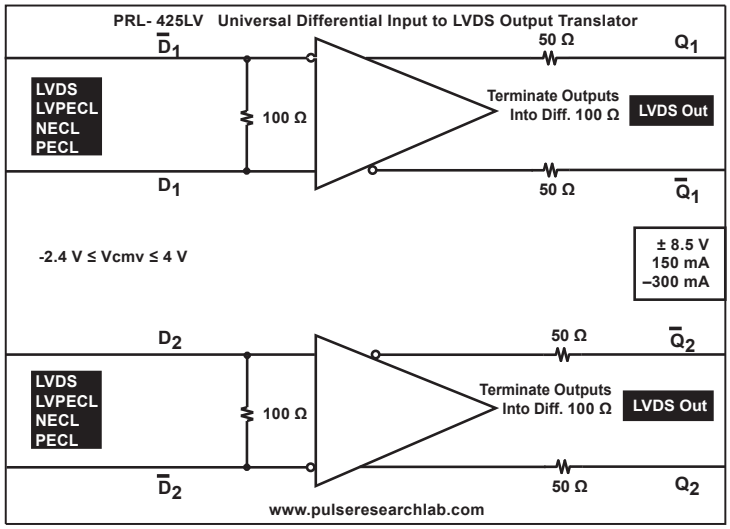


Fig. 1 PRL-425LV Block Diagram

Notes: (1). the output rise and fall times (10%-90%) of models with SMA output connectors are measured with both the Q and $\overline{Q}$ outputs terminated into ground referenced 50 Ω terminations. Rise and fall times for models with Triax output connectors are not measured.
(2). In fmax measurement, the module under test is connected between a driver PRL-425N and a receiver PRL-425N having the same interfacing connectors, SMA to SMA, Triax to Triax, etc. The outputs of the receiving PRL-425N are then connected to a PRL-255N frequency divider, and the outputs of the PRL-255N are measured using the PRL-550NQ4X NECL terminator connected to a sampling scope. The interconnecting cable for Triax I/O is the Trompeter PCGOW10PCG-36 shielded twisted pair cable.

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