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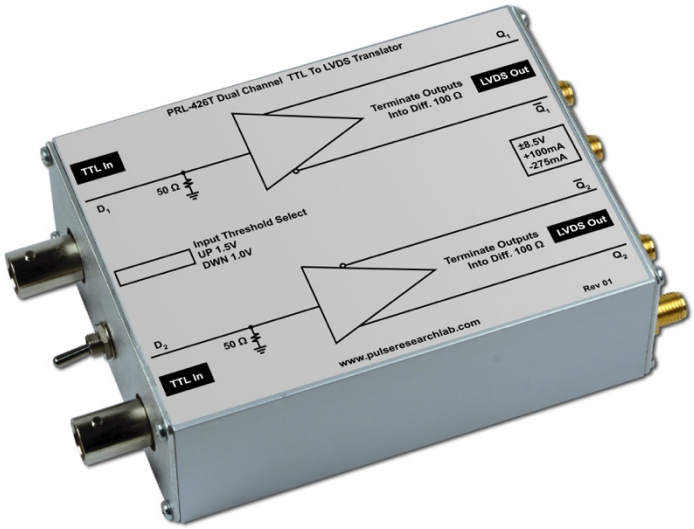
PRL-426T DUAL CHANNEL TTL TO LVDS TRANSLATOR

APPLICATIONS

- Converting TTL Signals to LVDS
- High Speed Digital Communications systems Testing
- High Speed SONET Clock Level Translation

FEATURES

- f_{max} > 300 MHz
- 1.1ns Typical Output Rise & Fall Times
- Switchable 1.5 V/1.0 V input threshold (TTL)
- Complementary 50 Ω LVDS Outputs
- BNC Input Connectors, SMA Output Connectors
- Triax Output Connector Option
- Two channels for CLK/DATA translation
- Self-contained 1.3 x 2.9 x 3.9-in. units include ±8.5V/1.8A AC/DC Adapters



PRL-426T, TTL to LVDS (SMA) Translator

DESCRIPTION

The PRL-426T is a TTL-to-LVDS Logic Level Translator. The PRL-426T input is single-ended, and a toggle switch controls the input threshold (1.5 V or 1.0 V into 50 Ω). The input connectors on the PRL-426T are BNC.

The differential outputs are 50 Ω back-terminated and are designed for driving floating 100 Ω loads, normally the configuration used in LVDS input circuits. The output swing is typically 600 mV with a common mode voltage of 1.2 V. Models with the "TR" suffix, e.g. PRL-426TTR, have Triax output connectors instead of the SMA connectors. These high speed translators facilitate testing of high speed digital communications circuits where conversion of TTL clock and data signals to LVDS level signals is often required.

The PRL-426T is designed to interface with TTL circuits. In cases where the signal source cannot drive TTL voltages into 50 Ω, the input threshold switch can be used to lower the triggering voltage to 1.0 V.

Each unit is supplied with a ±8.5 V/1.8 A AC/DC Adaptor and housed in a 1.3 x 2.9 x 3.9-in. extruded aluminum enclosure. Available accessories include voltage distribution modules for mounting multiple units.

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*SPECIFICATIONS (0^0 C ≤ T_A ≤ 35^0C)

Unless otherwise specified, dynamic measurements are made with all outputs terminated into floating 100 Ω loads.

		PRL-426T			
SYMBOL	**PARAMETER**	**Min**	**Typ**	**Max**	**UNIT**
R_{in}	Input Resistance	49.5	50.0	50.5	Ω
R_{out}	Output Resistance	49.5	50.0	50.5	Ω
V_{OL}	Output Low Level		0.9		V
V_{OH}	Output High Level		1.5		V
V_{CMV}	Common mode voltage[1]		1.2		
I_{DC1}	DC Input Current, +8.5 VDC		100	115	mA
I_{DC2}	DC Input Current, -8.5 VDC		-245	-265	mA
V_{DC}	DC Input Voltage	±7.5	±8.5	±12	V
V_{AC}	AC/DC Adapter Input Voltage	103	115	127	V
t_{PLH}	Propagation Delay to output ↑		2		ns
t_{PHL}	Propagation Delay to output ↓		2		ns
$t_{r/tf}$	Rise/Fall Times (10%-90%)[2]		1.00	1.25	ns
t_{SKEW}	Skew between any 2 outputs[3]		200	500	ps
f_{max}	Max Clock Frequency[4]	250	350		MHz
	Size	1.3 x 2.9 x 3.9			in.
	Weight	7			Oz

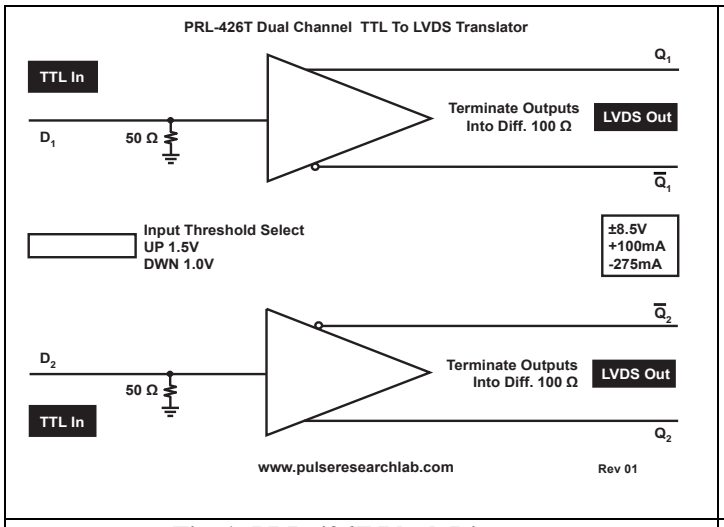


Fig. 1: PRL-426T Block Diagram

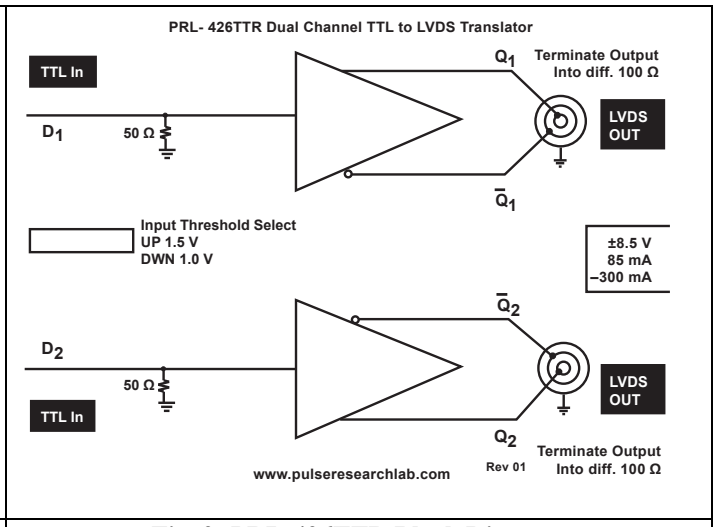


Fig. 2: PRL-426TTR Block Diagram

Notes:

(1) $V_{CMV} = (V_{OH}-V_{OL})/2$;

(2) Rise and Fall times are measured with SMA output connector units only and with ground-referenced 50 Ω loads.;

(3) Skew is measured at the output of a PRL-425N when driven by a PRL-426T ;

(4) f_{max} is measured using a PRL-425N with the corresponding input connectors as the receiver. The outputs of the PRL-425N are measured. f_{max} for the PRL-426T is currently limited by the lack of high frequency TTL drivers.

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