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Version 2.1A

4072, 4072A & 4073
DUAL PROGRAMMABLE RESISTANCE

PUBLICATION NO. 980753-501

RACAL INSTRUMENTS

Racal Instruments, Inc.
4 Goodyear St., Irvine, CA 92718-2002
Tel: (800) RACAL-ATE, (949) 859-8999, FAX: (949) 859-7309

Racal Instruments, Ltd.
480 Bath Road, Slough, Berkshire, SL1 6BE, United Kingdom
Tel: +44 (0) 1628 604455; FAX: +44 (0) 1628 662017

Racal Systems Electronique S.A.
18 Avenue Dutartre, 78150 LeChesnay, France
Tel: +33 (1) 3923 2222; FAX: +33 (1) 3923 2225

Racal Systems Elettronica Srl.
Strada 2-Palazzo C4, 20090 Milanofiori Assago, Milan, Italy
Tel: +39 (02) 5750 1796; FAX +39 (02) 5750 1828

Racal Elektronik System GmbH.
Frankenforster Strasse 21, 51427 Bergisch-Gladbach 1, Germany
Tel:+49 2204 92220; FAX: +49 2204 21491

Racal Australia Pty. Ltd.
3 Powells Road, Brookvale, NSW 2100, Australia
Tel: +61 (2) 9936 7000, FAX: +61 (2) 9936 7036

Racal Electronics Pte. Ltd.
26 Ayer Rajah Crescent, 04-06/07 Ayer Rajah Industrial Estate, Singapore 0513
Tel: +65 7792200, FAX: +65 7785400

Racal Instruments, Ltd.
Room 1213 Nan Fung Centre, Tsuen Wan, New Territories,Hong Kong
Tel: +852 2405 5500, FAX: +852 2416 4335

http://www.racalinst.com



PUBLICATION DATE: NOVEMBER 1994

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2. Product model number
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You may contact your customer service advisor by:

E-Mail:	Helpdesk@racalinstruments.com	
Telephone:	+1 800 722 3262	(USA)
	+44(0) 8706 080134	(UK)
	+852 2405 5500	(Hong Kong)
Fax:	+1 949 859 7309	(USA)
	+44(0) 1628 662017	(UK)
	+852 2416 4335	(Hong Kong)

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FOR YOUR SAFETY

Before undertaking any troubleshooting, maintenance or exploratory procedure, read carefully the **WARNING** and **CAUTION** notices.

This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.

If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earthed pole) of the power supply.

Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adaptor. This will defeat the protective feature of the third conductor in the power cord.

Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid "live" circuit points.

Before operating this instrument:

1. Ensure the instrument is configured to operate on the voltage at the power source. See Installation Section.

2. Ensure the proper fuse is in place for the power source to operate.

3. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until performance is checked by qualified personnel.

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Dual Programmable Resistance VXIbus Module

Model 4072 & 4072A & 4073

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4072 & 4073 - V2.1 - February 1993

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SECTION 1
INTRODUCTION

This manual provides the necessary information to install one or more of the Racal-Dana **4072 & 4072A & 4073** modules in a VXIbus compatible chassis and to operate it correctly.

The features and Ordering Information are given in this section.

The section 2 describes specifications of each model 4072, 4072A or 4073.

Some technical descriptions will be given to explain the theory of operation of the product in the section 6.

The section 7 describes SCPI syntax and commands.

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General Information

The **4072 & 4072A & 4073** Series is a range of C size, **VXI**bus compatible modules providing two individually programmable resistors.

Each Resistor can be programmed in a range of 4 decades.

The accuracy of the 4072 is 0.015 %, the accuracy of the 4072A is 0.05 %, the accuracy of the 4073 is 0.1 %. The maximum Power Dissipation for each programmable resistor of the 4072 is 1.1 W, the maximum Power Dissipation for each programmable resistor of the 4072A or 4073 is 3 W.

Each set of resistors can be wired in series to obtain one equivalent Resistor with 7 decades of Resolution for example. (407x-1-4 model: programmable value from 0 Ω to 999.9999 kΩ with a 0.1Ω of resolution).

The 4072 & 4072A & 4073 is a solution capable of high **precision resistance** for the following cases:
- high variable resolution resistor
- high accuracy
- variable resistor simulation with low residual resistance

The 4072 & 4072A & 4073 can be used with a current of 1A. An internal fuse can be selected to protect the internal resistance or deselected to obtain a higher precision.

A Self-Test is executed by user request. It checks the correct operation of the logic functions, the relays, the fuses and the correct values of all internal resistors.

As an outline, here are some applications of process control and industrial measurement requiring the 4072 & 4072A & 4073:

- Digitally Controlled potentiometer.
- Simulation of a temperature sensor (Pt 100 sensor).
- Bridge Method (Wheaston for example).
- Measurement of a current with high accuracy (using 4072 and a DVM)

The 4072 & 4072A & 4073 family is a message based module compatible with **VXI**bus revision 1.3, and IEEE 488.2 definitions. The commands and syntaxes are defined using SCPI standard.

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Features of 4072

- 2 Independent channels in a module.
- 4 Decades per channel
- 4 Ranges available from 999.9 Ω to 999.9 KΩ
- Maximum Power dissipation 1.1 W
- Resolution 0.01 %
- Precision 0.015 %
- High stability precision wirewound resistors
- Bounce-free Operation
- Total Self Test
- C-size simple width module
- Full VXIbus Revision 1.3 Compatibility
- SCPI Compatibility

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Features of 4072A

- 2 Independent channels in a module.
- 4 Decades per channel
- 2 Ranges available from 999.9 Ω to 9.999 KΩ
- Maximum Power dissipation 3 W
- Resolution 0.01 %
- Precision 0.05 %
- High stability wirewound silicone coated resistors, meet the requirements of MIL-R-26E, MIL-R26C, MIL-R-23379 specifications.
- Bounce-free Operation
- Total Self Test
- C-size simple width module
- Full VXIbus Revision 1.3 Compatibility
- SCPI Compatibility

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Features of 4073

- 2 Independent channels in a module.
- 4 Decades per channel
- 4 Ranges available from 999.9 Ω to 999.9 KΩ
- Maximum Power dissipation 3 W
- Resolution 0.01 %
- Accuracy 0.1 %
- High stability RW69 (MIL-R26E) resistors
- Total Self Test
- C-size simple width module
- Full VXIbus Revision 1.3 Compatibility
- SCPI Compatibility

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Models and Ordering Information

RACAL DANA's **VXI** model **4072 & 4073** offers two independent programmable Resistances with 10 000 steps of resolution.

Each Resistance can belong to one of these four ranges:

Range 1 (1K) : value from 0 to 999.9 Ω, resolution 0.1 Ω.

Range 2 (10K) : value from 0 to 9999 Ω, resolution 1 Ω.

Range 3 (100K) : value from 0 to 99.99 KΩ, resolution 10 Ω.

Range 4 (1000 K) : value from 0 to 999.9 KΩ, resolution 0.1 KΩ.

Each Resistance of the RACAL DANA's **VXI** model **4072A** can belong to one of these two ranges:

Range 1 (1K) : value from 0 to 999.9 Ω, resolution 0.1 Ω.

Range 2 (10K) : value from 0 to 9999 Ω, resolution 1 Ω.

Each 4072 & 4072A & 4073 model has two extensions to indicate the ranges of each Resistance. For example, the 4072-1-4 has a first Resistance of range 1 (1 KΩ) and a second Resistance with range 4 (1000 KΩ).

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ORDERING INFORMATION for 4072 Series

PART NUMBER	MODEL	OPTION	Description
33-1030-9999	4072&4073	ALL	Technical Documentation
33-1030-1400	4072	1 & 4	R1: 1 KΩ R2: 1000 KΩ
33-1030-1100	4072	1 & 1	R1: 1 KΩ R2: 1 KΩ
33-1030-1200	4072	1 & 2	R1: 1 KΩ R2: 10 KΩ
33-1030-1300	4072	1 & 3	R1: 1 KΩ R2: 100 KΩ
33-1030-2200	4072	2 & 2	R1: 10 KΩ R2: 10 KΩ
33-1030-2300	4072	2 & 3	R1: 10 KΩ R2: 100 KΩ
33-1030-2400	4072	2 & 4	R1: 10 KΩ R2: 1000 KΩ
33-1030-3300	4072	3 & 3	R1: 100 KΩ R2: 100 KΩ
33-1030-3400	4072	3 & 4	R1: 100 KΩ R2: 1000 KΩ
33-1030-4400	4072	4 & 4	R1: 1000 KΩ R2: 1000 KΩ
33-1030-1000	4072	1 & 0	R1: 1 KΩ R2: Not equiped
33-1030-2000	4072	2 & 0	R1: 10 KΩ R2: Not equiped
33-1030-3000	4072	3 & 0	R1: 100 KΩ R2: Not equiped
33-1030-4000	4072	4 & 0	R1: 1000 KΩ R2: Not equiped

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ORDERING INFORMATION for 4072A Series

PART NUMBER	MODEL	OPTION	Description
33-1030-9999	4072&4073	ALL	Technical Documentation
33-1031-1200	4072A	1 & 2	R1: 1 KΩ R2: 10 KΩ
33-1031-1100	4072A	1 & 1	R1: 1 KΩ R2: 1 KΩ
33-1031-2200	4072A	2 & 2	R1: 10 KΩ R2: 10 KΩ
33-1031-1000	4072A	1 & 0	R1: 1 KΩ R2: Not equiped
33-1031-2000	4072A	2 & 0	R1: 10 KΩ R2: Not equiped

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ORDERING INFORMATION for 4073 Series

PART NUMBER	MODEL	OPTION	Description
33-1030-9999	4072&4073	ALL	Technical Documentation
33-1040-1400	4073	1 & 4	R1: 1 KΩ R2: 1000 KΩ
33-1040-1100	4073	1 & 1	R1: 1 KΩ R2: 1 KΩ
33-1040-1200	4073	1 & 2	R1: 1 KΩ R2: 10 KΩ
33-1040-1300	4073	1 & 3	R1: 1 KΩ R2: 100 KΩ
33-1040-2200	4073	2 & 2	R1: 10 KΩ R2: 10 KΩ
33-1040-2300	4073	2 & 3	R1: 10 KΩ R2: 100 KΩ
33-1040-2400	4073	2 & 4	R1: 10 KΩ R2: 1000 KΩ
33-1040-3300	4073	3 & 3	R1: 100 KΩ R2: 100 KΩ
33-1040-3400	4073	3 & 4	R1: 100 KΩ R2: 1000 KΩ
33-1040-4400	4073	4 & 4	R1: 1000 KΩ R2: 1000 KΩ
33-1040-1000	4073	1 & 0	R1: 1 KΩ R2: Not equiped
33-1040-2000	4073	2 & 0	R1: 10 KΩ R2: Not equiped
33-1040-3000	4073	3 & 0	R1: 100 KΩ R2: Not equiped
33-1040-4000	4073	4 & 0	R1: 1000 KΩ R2: Not equiped

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SECTION 2
SPECIFICATIONS

This section contains specifications of:

- VXIbus Interface
- Commun Specifications
- Programmable Resistance:
    - 4072
    - 4072A
    - 4073

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SPECIFICATIONS

VXIbus Interface

Manufacturer ID:	**4091 (0FFB hex.): RACAL-DANA**
Model :	**1030 for 4072,**
	1031 for 4072A,
	1040 for 4073.
Logical Addressing:	**Dynamic or Static (1 to 254)**
Address Space:	**A16**
Device Class:	**Message Based Slave Device**
TTL Trigger line:	**Programmable**

WORD SERIAL PROTOCOL SUPPORTED

Byte Available

Byte Request

Write to logical address register

Asynchronous Mode Control

Begin Normal Operations Top

Control Response

Read Interrupter Line

Trigger

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COMMUN SPECIFICATIONS

Data rate in interactive mode:	**15 mS per value, without smoothing; 20 mS per value, with smoothing.**
Transition time (from a Trigger source):	**5 mS per channel, without smoothing; 10 mS per channel, with smoothing.**
Trigger source:	**Bus (GET) or 1 of 8 TTL Triggers (VXIbus).**
Trigger modes:	**IMMediate, ECOunt, COUNt.**
Self-Test time:	**< 5 seconds**
Self-Test Resistance Measurement Accuracy:	**4072 & 4072A: about 2 % ± 0.5 Ω 4073: about 2 % ± 1 Ω**
Self-Test coverage:	**99.8 % at 25°C**
Life Expectancy of relays :	**100 millions operations at 10 Vdc, 10 mA. 4072 & 4072A: 5 millions operations at 48 Vdc, 100 mA. 4073: 0.5 millions operations at 48 Vdc, 100 mA.**
MTBF:	**200 000 hours at 25°C, 160 000 hours at 35°C.**
User Connector:	**Two 9 pins sub D, RADIALL DPEZ-9P-S102**
Cooling (airflow backpressure):	**4.0 l/s, 0.5 mm H_2O.**
Operating Temperature:	**10 °C to 50 °C.**
Mounting Position:	**4072 & 4072A: Upright to within 30 ° of vertical. 4073: All position.**
Power Requirements:	
5 Vdc	**from 4.75 to 5.25 Vdc 2.5 A maximum, 3A peak internal protection by 3A temporized fuse.**
+24 Vdc	**from +22 Vdc to +26 Vdc 0.5 A typical, 1.5A peak internal protection by 1A temporized fuse.**
±12 Vdc	**from ±11 Vdc to ±13 Vdc 0.2 A typical, 1A peak internal protection by 1A temporized fuse**
Weight:	**about 2.5 kg (5.5 lbs)**

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SPECIFICATIONS - Resistance 4072

Number of channels:	**2**
Number of steps per channel:	**10 000 (or "4 decades")**
Initial Accuracy:	**± 0.015 % + 200 mΩ // 100 MΩ (23±3 °C) (RESistance1(or 2):PROTection OFF)**
Fuse Resistance:	**< 200 mΩ (RES1(or2):PROT ON)**
Resistance temperature coefficient:	**10 ppm / °C , from 10°C to 70 °C at Resistor Body.**
Thermal EMF: Above 4 KΩ	**< 0.5μV/°C Max.; < 0.2 μV/°C Typ.**
Below 4 KΩ	**< 1.8 μV/°C Max.; < 0.4 μV/°C Typ.**
Voltage Coefficient :	**< 1 ppm / Volt**
Maximum power dissipation : > 1 Ω	**1.1 W at 23 °C, 650 mW at 70 °C.**
< 1 Ω	**0.5 W at 23 °C, 300 mW at 70 °C.**
Recommended dissipation: > 1Ω	**850 mW at 23°C, 500 mW at 70 °C.**
< 1Ω	**300 mW at 23°C, 200 mW at 70 °C.**
Power dissipation coefficient:	**0.1 °C / mW**
Maximum working current:	**1 A (can be limited by internal fuse)**
Maximum working voltage:	**200 V DC or AC (at 70°C)**
Stability Load-Life (2000H, 500mW, 70°C):	**< 0.002%**
Stability Shelf-Life (-10°C to +30°C, no load):	**< 0.0015% after 1 year**
	< 0.003% after 3 years

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SPECIFICATIONS - Resistance 4072A

Number of channels:	**2**
Number of steps per channel:	**10 000 (or "4 decades")**
Initial Accuracy:	**± 0.05 % + 200 mΩ // 100 MΩ (23±3 °C) (RESistance1(or 2):PROTection OFF)**
Fuse Resistance:	**< 200 mΩ (RES1(or2):PROT ON)**
Resistance temperature coefficient: > 10 Ω	**20 ppm / °C , from 10°C to 70 °C at Resistor Body.**
< 10 Ω	**50 ppm / °C , from 10°C to 70 °C at Resistor Body.**
Maximum power dissipation :	**3 W at 23 °C, 2.5 W at 70 °C.**
Recommended dissipation:	**2 W at 23°C, 1.5 W at 70 °C.**
Short time overload:	**10 W, 5 seconds at 70 °C.**
Maximum working current:	**1 A (can be limited by internal fuse)**
Maximum working voltage:	**150 V DC or AC (at 70°C)**
Insulation relays protected voltage:	**250 V DC or AC (at 70°C)**
Stability Load-Life (2000H, 1 W, 70°C):	**< 0.005%**
Stability Shelf-Life (-10°C to +30°C, no load):	**< 0.003% after 1 year < 0.005% after 3 years**
Style of winding:	**Non-inductive (Aryton-Perry) winding.**
MIL specifications:	**Meet the requirements of MIL-R-26E, MIL-R26C, MIL-R-23379 specifications.**

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SPECIFICATIONS - Resistance 4073

Number of channels:	**2**
Number of steps per channel:	**10 000 (or "4 decades")**
Initial Accuracy:	**± 0.1 % + 800 mΩ // 100 MΩ (23±3 °C)** **(RESistance1(or 2):PROTection OFF)**
Fuse Resistance:	**< 200 mΩ (RES1(or2):PROT ON)**
Resistance temperature coefficient:	**10 ppm / °C from 10°C to 50 °C, at Resistor Body.**
Maximum power dissipation : > 2 Ω	**3 W at 23 °C.**
< 2 Ω	**1 W at 23 °C.**
Recommended dissipation: > 2 Ω	**1200 mW continuous at 23°C.**
< 2 Ω	**400 mW continuous at 23°C.**
Maximum working current:	**1 A (can be limited by internal fuse)**
Maximum working voltage:	**200 VDC or 200 V peak AC at 70°C**
Stability Load-Life (1000H, 500mW, 70°C):	**< 0.005%**
Stability Shelf-Life (at 25°C, no load):	**< 0.005 % after 1 year** **< 0.01 % after 3 years**
MIL specifications:	**Meet the requirements of MIL-R-26E, MIL-R26C, MIL-R-23379 specifications.**

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SECTION 3
INSTALLATION

This section describes the start-up phase before operation of the 4072 & 4072A & 4073 module:

- Unpacking and Inspection
- Reshipment Instructions
- Set up the logical address (dynamic and static configuration)
- Interrupt setting
- Power up
- Self-test.

The 4072 & 4072A must be mounted in vertical position (mercury wetted relays). The 4073 can be mounted in all position.

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Installation

Unpacking and Inspection

Before unpacking the 4072 & 4072A & 4073 module, check the exterior of the shipping box for any sign of damage. All irregularities should be noted on the shipping bill. Remove the instrument from its box, preserving the factory packaging as much as possible. Inspect the 4072 & 4072A & 4073 module for any defect or damage. Notify the carrier immediately if any damage is apparent.

Notify RACAL-DANA if the module appears damaged in any way. Do not attempt to install a damaged module into a VXI chassis.

Have a qualified person check the instrument for safety before use.

The 4072 & 4072A & 4073 module is shipped in a anti-static bag to prevent electrostatic damage to the module. Do not remove module from the anti-static bag unless in a static controlled area.

Reshipment Instructions

Use the original packing if it is necessary to return the 4072 & 4072A & 4073 module to RACAL-DANA for calibration or servicing. The original shipping box and the instrument's plastic foam will provide the necessary support for safe reshipment. If the original packing is unavailable, wrap the 4072 & 4072A & 4073 module in anti-static bag and use plastic spray foam to surround and protect the instrument. Reship in either the original or a new, sturdy shipping box.

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ADDRESS SWITCH SETTING

The 4072 & 4072A & 4073 Series dual programmable Resistance modules are installed in a C size VXIbus compatible chassis in any chassis slot (the leftmost slot is reserved for the controller).

One free address is required in the use of a 4072 & 4072A & 4073 Series module. The logical address is set by a DIP switch on the 4072 & 4072A & 4073.

The 4072 & 4072A & 4073 has an internal 8-position address switch used to determine dynamic or static configuration. It is located on the top of the module accessible through the case. Any setting other than 255 indicates static configuration.

Dynamic configuration is an alternative method for assigning Logical Address to VXIbus devices and is defined in section F of the VXIbus System Specification Revision 1.3.

The user can select any logical address from 1 to 254 for static configuration.

Logical address 0 is not allowed.

In the ON position the switch is set to the logical 1 and in the OFF position to the logical 0.

The switch 1 is the LSB, the switch 8 is the MSB.

VXIbus INTERRUPT HANDLER SETTING

One programmable interrupt line is provided on the 4072 & 4072A & 4073 module. This line is assigned by using the *assign interrupter* word serial protocol command (see page 183 in Rev 1.3 of the VXIbus specs). The *Int_ID* is set to 1.

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4072 & 4072A & 4073 to VXIbus MAINFRAME INSTALLATION

To install the 4072 & 4072A & 4073 in a C size VXI chassis, ensure power is not applied. Configurate the interrupt daisy chain on the backplane to bypass empty slots (VXIbus specs).

Remove the front cover of the VXI chassis and slide the 4072 & 4072A & 4073 into appropriate slot with the LED's towards the top.

The 4072 & 4072A can not be used with a horizontal chassis due to the polarization of mercury relays.

POWER UP INITIALIZATION

Before turning on the VXIbus mainframe, make sure that a slot 0 with resource manager is present.

Upon power up of the system the following sequence takes place:

- Board ID check.
- VXIbus Interface Initialization
- Power up Self-Test: Tests are performed on ROM, RAM, Non volatile Memory and the Timer to make sure that the logic components are operating correctly.
- Disable TTLTRG trigger functions.
- Relay Initialization (all Resistance channels are initialized to their maximum values, all ouput relays are open).

SELF-TEST

The Self-Test is called up by a TEST command (*TST?). Tests are performed on Ports, Relays, Fuses and measurement of value of each Resistance .

The Self-Test is performed in less than five seconds. It does not use external instrumentation or additional wiring. During the Self-Test, all output channels are disconnected.

All internal resistance values are measured independently, with an accuracy better than 2% ± 0.5 Ω for the 4072 & 4072A, or better than 2% ± 1 Ω for the 4073. A list of defects, if any, will be returned.

After the Self-Test, all Resistance channels are initialized to their maximum values and all output relays are disconnected.

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SECTION 4

OPERATION, CHECK and CALIBRATION

This section supplies the necessary information to operate, check and calibrate the 4072 & 4072A & 4073 Series Dual Programmable Resistance models.

Section 6 describes the theory of operation.

Section 7 describes the complete set of SCPI syntax commands.

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CONNECTORS:

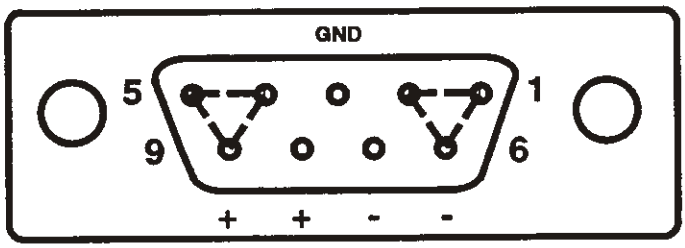
There are 2 connectors on the front panel of a 4072 & 4072A & 4073 module. Each connector corresponds to one Resistance channel, each having low contact resistance. Each one has 9 pins. 3 pins are used for each Resistance lead (group 1-2-6 and 4-5-9). Other pins can be used for 4-wire application. Pin 3 is the system ground.

Connect 1-2-6 together and 4-5-9 together in a 2-wire application.

For 4-wire measurement, use group (1-2-6) and (4-5-9) for sourcing, use pins 7 and 8 for sensing.

Channel 1 or 2

(9 pins connector viewed from the front panel)

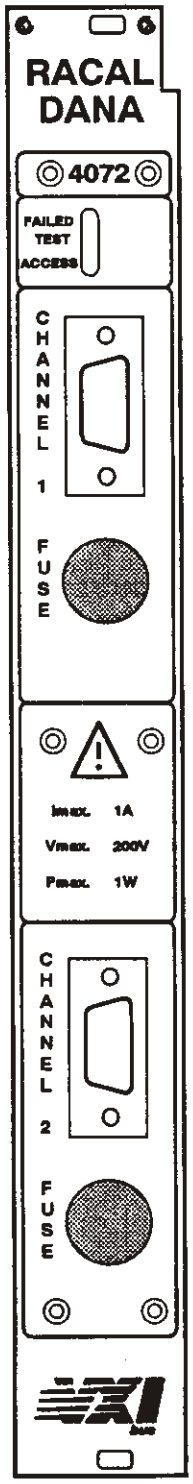


1	R-	OUTPUT 1 of the Resistance
2	R-	OUTPUT 1 of the Resistance
3	GND	Chassis ground
4	R+	OUTPUT 2 of the Resistance
5	R+	OUTPUT 2 of the Resistance
6	R-	OUTPUT 1 of the Resistance
7	R-m	OUTPUT 1 for 4-wires (Sense -)
8	R+m	OUTPUT 2 for 4-wires (Sense +)
9	R+	OUTPUT 2 of the Resistance

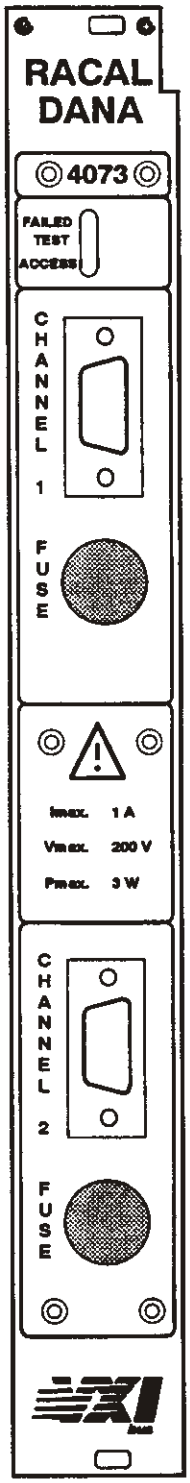
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FRONT PANEL of 4072 and 4072A



FRONT PANEL of 4073



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4.1 / CALIBRATION PROCEDURE ON THE MOTHERBOARD

Test equipment required :

- DC voltmeter (RACAL-DANA 4006 or 4009).
- A 4072 or 4073 module, a VXI chassis, a Slot 0 connected to a PC by a IEEE-488 bus or a built-in VXI Bus Computer.

Procedure

1) - Power up the motherboard during 5 minutes before starting calibration.

2) - Calibration must be done under normal cooling conditions of the module : that is to say calibrating the module inside the VXI chassis.

3) - Connect the voltmeter : positive terminal to pin 6 of U10, negative terminal to pin A20 of CN1 or CN2.
Adjust **PR1** to obtain 9V ± 5 mV.

4) - Connect the voltmeter : positive terminal to pin 2 of U14 (LM317T), negative terminal to pin A20 of CN1 or CN2.
Adjust **PR2** to obtain 18V ± 100 mV.

5) - Check serial number (*IDN?)

6) - Check options (*OPT?)

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4.2 / RESISTANCE MODULE CHECK PROCEDURE

Introduction:

The resistance module contains 4 decades. Each decade can provide a resistance value between 0 and 9 combining four elementary values : 1, 2, 3, 6. The 4072 & 4073 have an AUTOTEST function which measures all the elementary resistors with an accuracy better than 2 %. The AUTOTEST verifies all the internal relays for proper operation. The theorical Self-Test coverage is 99.8 % .

Test equipment required :

A 4072 or 4073 module, a VXI chassis, a Slot 0 connected to a PC by a IEEE-488 bus or a built-in VXI Bus Computer.

Test procedure :

1) - Send the command "*TST?". If answer is 0, then the resistance modules are correct and values of all elementary resistances are compliant with more than 2 %.

2) - If answer to "*TST?" is different from 0, then there are faulty components on resistance modules.
In order to know defects, send the command "TEST:RES1?" or "TEST:RES2?".

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4.3 / ACCURACY CHECK (complete device)

Introduction:

4072 & 4073 programmable resistances are highly accurate resistances, with a very low contact residual resistance. When measuring, you must use an ohmmeter with a better accuracy than 0.002 % connected to a "4 wire" mode according to indications mentionned on page 4-2 of the user manual.

Test equipment required :

- A "4 wire" input accuracy ohmmeter,
- A 4072 & 4073, a VXI chassis, a Slot 0 connected to a PC by IEEE-488 bus or a built-in PC.
- You can directly send the SCPI commands from the keyboard or use the "driver" for LabWindows which list is given in chapter 7 in the user manual.

Test procedure :

1) - Power up the 4072 & 4073 during 5 minutes before starting checking.

2) - Checking must be done under normal cooling conditions of the module : that is to say calibrating the module inside the VXI chassis.

3) - Control the output relays closure (Example: OUTPUT:RES1 ON). Control the protection fuse short circuit. (Example: RES1:PROT OFF). Control value 0 (Example: RES1 0) .
Check that the residual resistance value is inferior to the specified value.

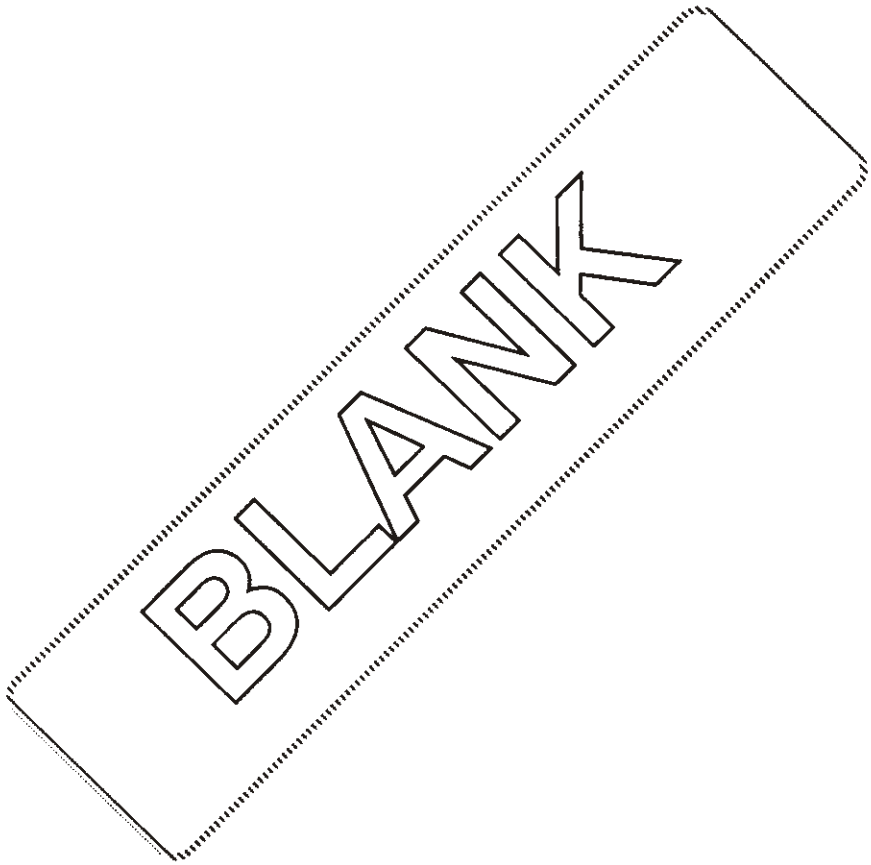
4) - Control the elementary values of each decade : 1, 2, 3, 6. (Example: RES1 100, RES1 200, RES1 300, RES1 600) .
Check that the real values are compliant with the specifications.

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SECTION 5

APPLICATIONS



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SECTION 6

TECHNICAL DESCRIPTION

6.1 Introduction and general view

6.1.1 4072

6.1.2 4072A

6.1.3 4073

6.1.4 General View and front panel connectors.

6.2 Block Diagram

6.3 Mother Board

6.3.1 Block Diagram

6.3.2 VXI-bus P1 and P2 connectors

6.3.3 Power supplies

6.3.4 Bus buffers and the memory extension

6.3.5 PLD

6.3.6 Self Test

6.4 Microprocessor and VXI Interface Board

6.4.1 Description

6.4.2 P100 Microprocessor bus Connector.

6.5 Resistance Board

6.5.1 Description

6.5.2 Internal CN1 and CN2 Connectors.

6.6 Mapping

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This Section describes the theory of operation of the 4072 & 4072A & 4073 Series.

This section begins with a 4072 & 4072A & 4073 model block diagram description then extends to the description of the circuit action at the component level:

6.1 Introduction and general view

6.2 Block Diagram

6.3 Mother Board

6.4 Microprocessor and VXI Interface Board

6.5 Resistance Board

The 4072 & 4072A & 4073 VXI model can be functionally and physically broken down to 4 sub assemblies (Final assebly, Mother board, Microprocessor & VXI Interface board, Resistance board.)

Section 8 gives the detailed schematics of each electronic sub assembly.

Section 9 gives the detailed drawings and PCB description of each sub assembly.

Section 10 gives the parts list of each sub assembly.

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6.1 Introduction and general view

6.1.1 4072

The 4072 model can be broken down into four physical blocks:

- **FS910304**: Final assembly (VXI C size box, front panel ...)

- **FS910301**: Mother board.

This board contains:
. Connectors P1 and P2 of the VXI bus.
. Power supply filters and Regulator.
. Buffers for Microprocessor buses (DATA, ADDRESS and CONTROL).
. Extension for RAM and EPROM.
. PLD (Programmable Logic Devices) for address decoder function.
. ADC (Analog to Digital Converter) and measurement system for Self Test.
. Glue logic.

- **FS910302**: Microprocessor and VXI Interface board.

This board contains:
. The 68000 Microprocessor and associated circuits.
. RAM, EPROM, NVRAM (Non volatile RAM)
. VXI Interface and Registers.
. Programmable Time base.

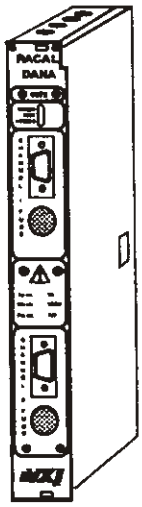
- **FS910303**: Resistance board.

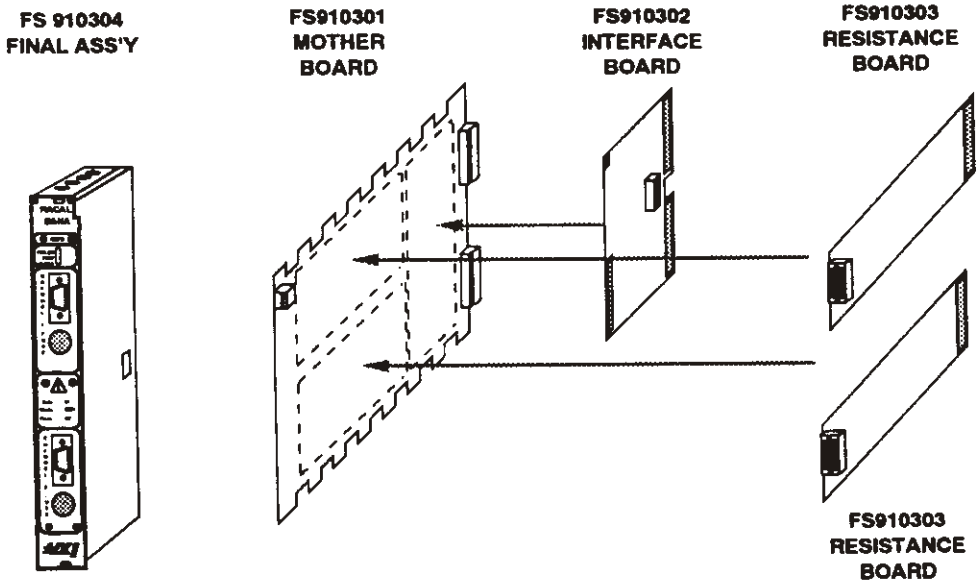
This board contains:
. Precision Resistances for 1 channel of 4 decades.
. Precision Relays
. Self Test switches.
. Glue logic.

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PHYSICAL BLOCK DIAGRAM

4072





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6.1.2 4072A

The 4072A model can be broken down into four physical blocks:

- **FS910304**: Final assembly (VXI C size box, front panel ...)

- **FS910301**: Mother board.

This board contains:
. Connectors P1 and P2 of the VXI bus.
. Power supply filters and Regulator.
. Buffers for Microprocessor buses (DATA, ADDRESS and CONTROL).
. Extension for RAM and EPROM.
. PLD (Programmable Logic Devices) for address decoder function.
. ADC (Analog to Digital Converter) and measurement system for Self Test.
. Glue logic.

- **FS910302**: Microprocessor and VXI Interface board.

This board contains:
. The 68000 Microprocessor and associated circuits.
. RAM, EPROM, NVRAM (Non volatile RAM)
. VXI Interface and Registers.
. Programmable Time base.

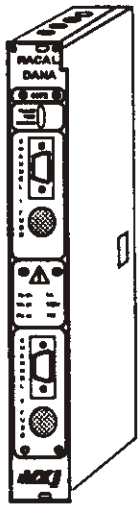
- **FS910503**: Resistance board.

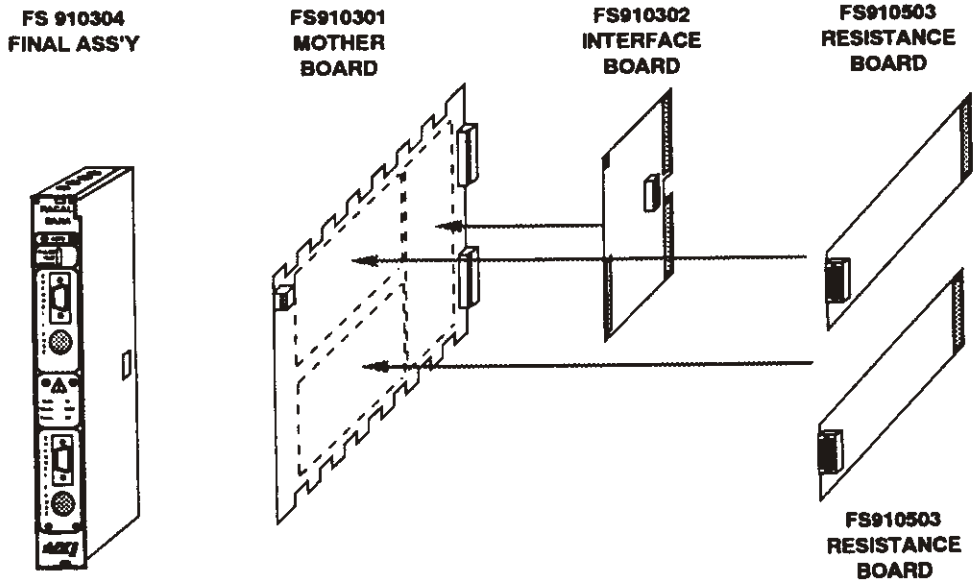
This board contains:
. Precision Resistances for 1 channel of 4 decades.
. Precision Relays
. Self Test switches.
. Glue logic.

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PHYSICAL BLOCK DIAGRAM

4072A





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6.1.3 4073

The 4073 model can be broken down into four physical blocks:

- **FS910404**: Final assembly (VXI C size box, front panel ...)

- **FS910301**: Mother board.

This board contains:
. Connectors P1 and P2 of the VXI bus.
. Power supply filters and Regulator.
. Buffers for Microprocessor buses (DATA, ADDRESS and CONTROL).
. Extension for RAM and EPROM.
. PLD (Programmable Logic Devices) for address decoder function.
. ADC (Analog to Digital Converter) and measurement system for Self Test.
. Glue logic.

- **FS910302**: Microprocessor and VXI Interface board.

This board contains:
. The 68000 Microprocessor and associated circuits.
. RAM, EPROM, NVRAM (Non volatile RAM)
. VXI Interface and Registers.
. Programmable Time base.

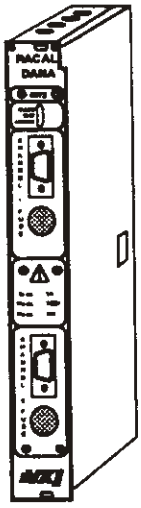
- **FS910403**: Resistance board.

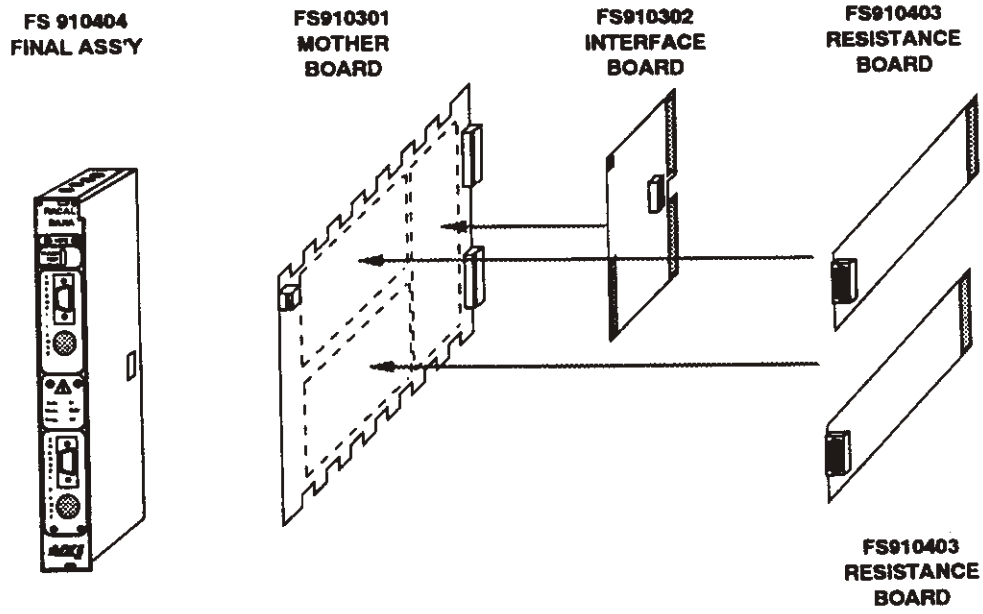
This board contains:
. Precision Resistances for 1 channel of 4 decades.
. Precision Relays
. Self Test switches.
. Glue logic.

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PHYSICAL BLOCK DIAGRAM

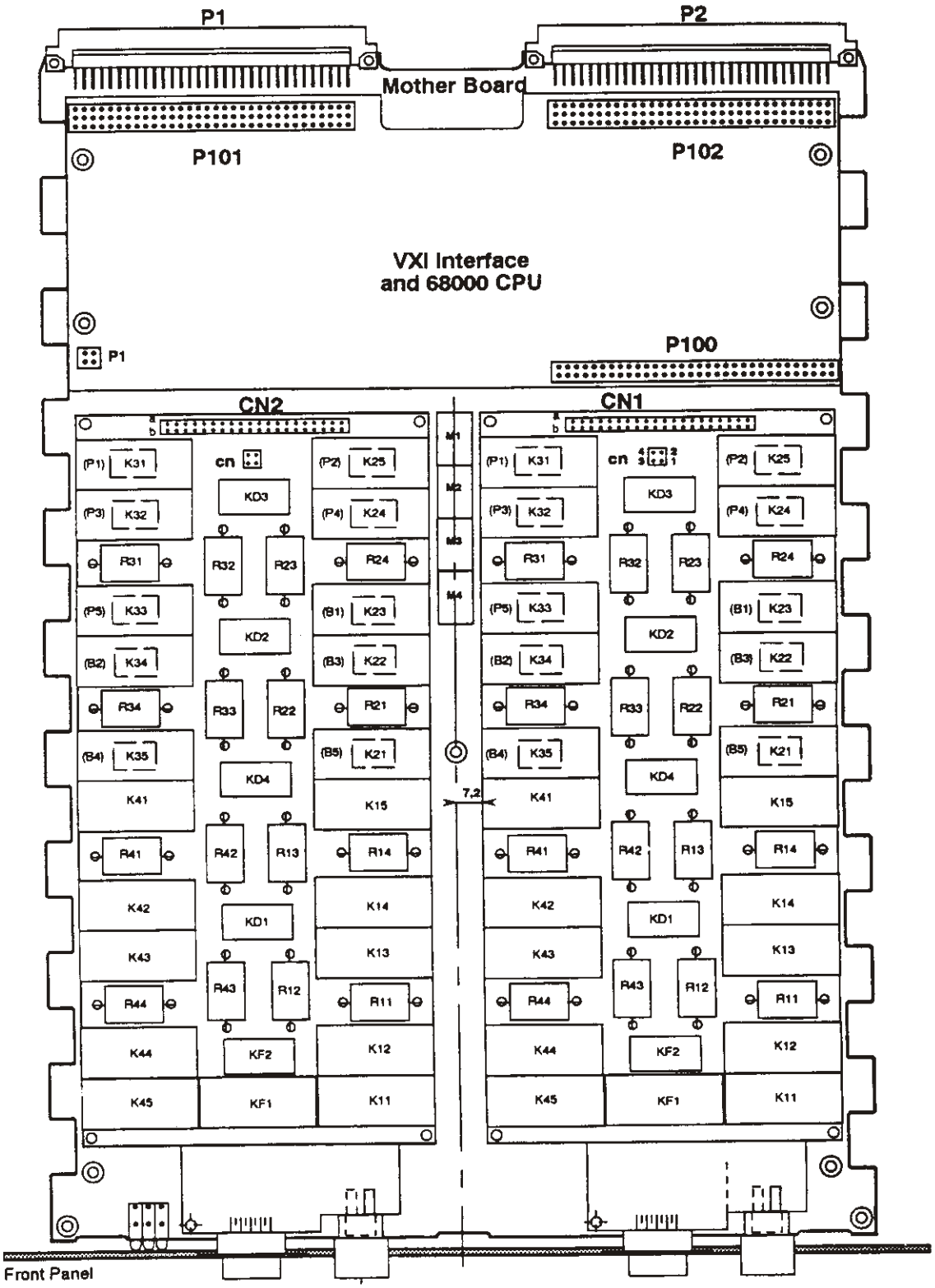
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6.1.4 General View



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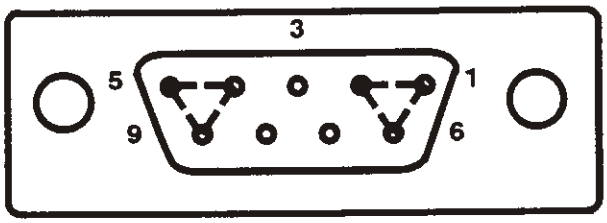
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CONNECTORS:

There are 2 connectors on the front panel of a 4072 & 4072A & 4073 module. Each connector corresponds to one Resistance channel, each having low contact resistance. Each one has 9 pins. 3 pins are used for one Resistance lead (group 1-2-6 and 4-5-9). Pin 3 is connected to the system ground. Other pins can be used for 4-wires application.

Channel 1 or 2

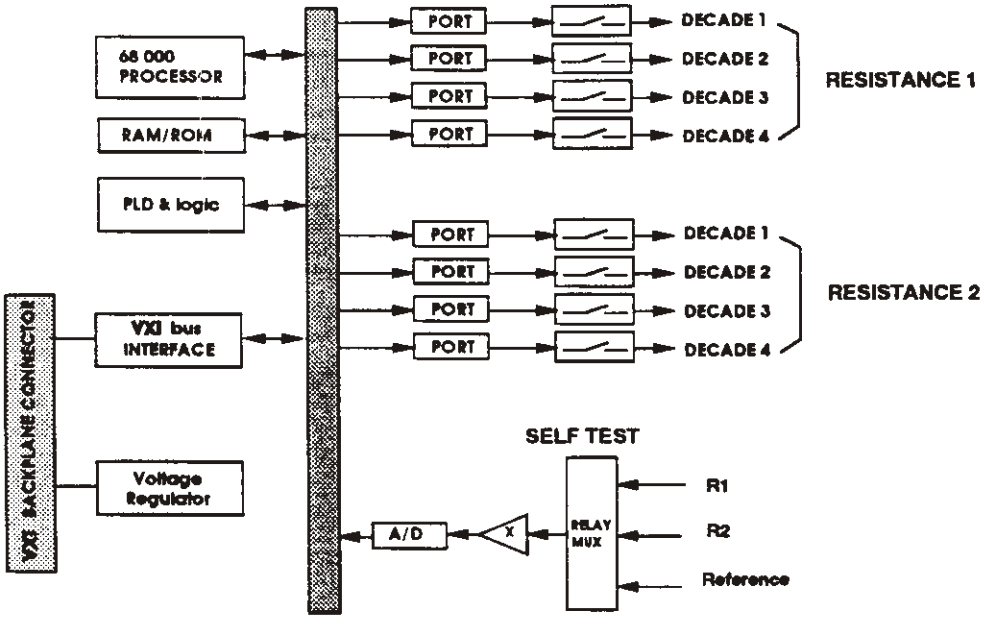
(9 pins connector viewed from the front panel)

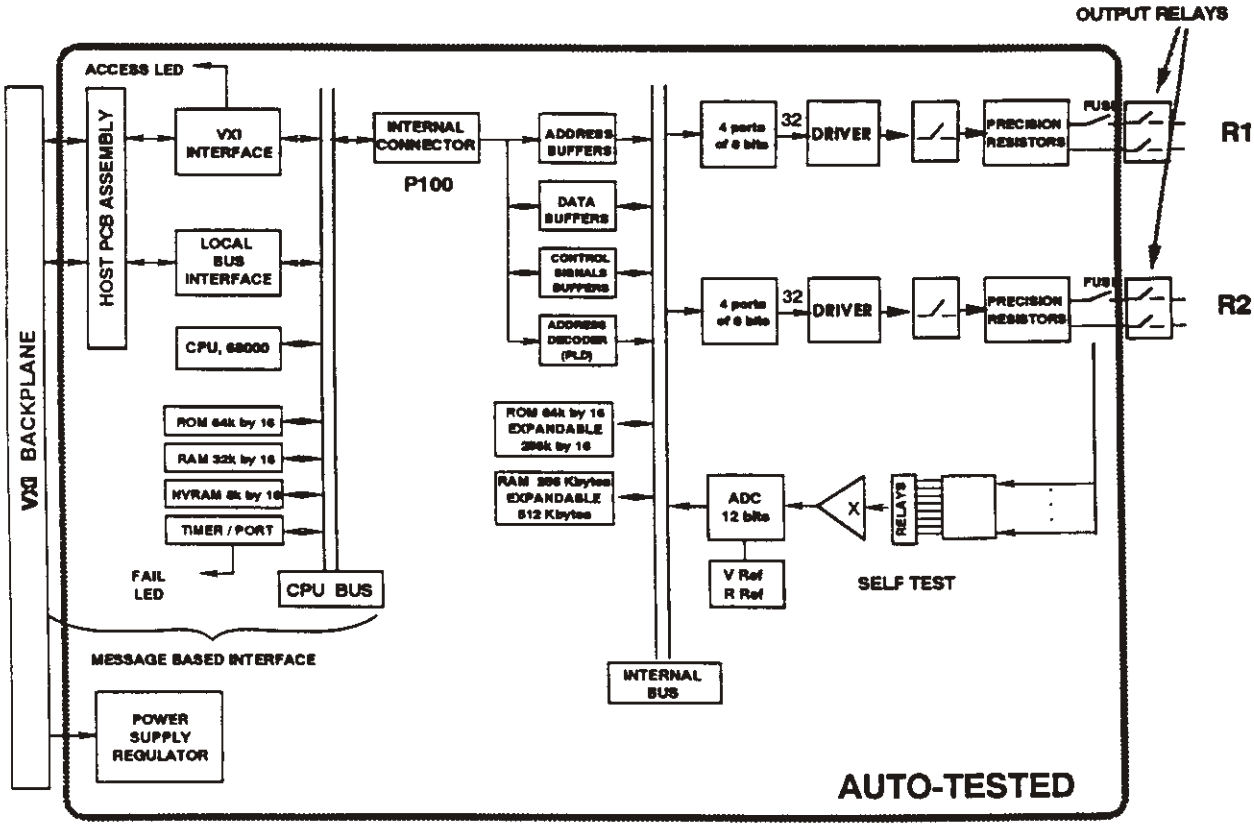


1	R-	OUTPUT 1 of the Resistance
2	R-	OUTPUT 1 of the Resistance
3	GND	Chassis ground
4	R+	OUTPUT 2 of the Resistance
5	R+	OUTPUT 2 of the Resistance
6	R-	OUTPUT 1 of the Resistance
7	R-m	OUTPUT 1 for 4-wires
8	R+m	OUTPUT 2 for 4-wires
9	R+	OUTPUT 2 of the Resistance

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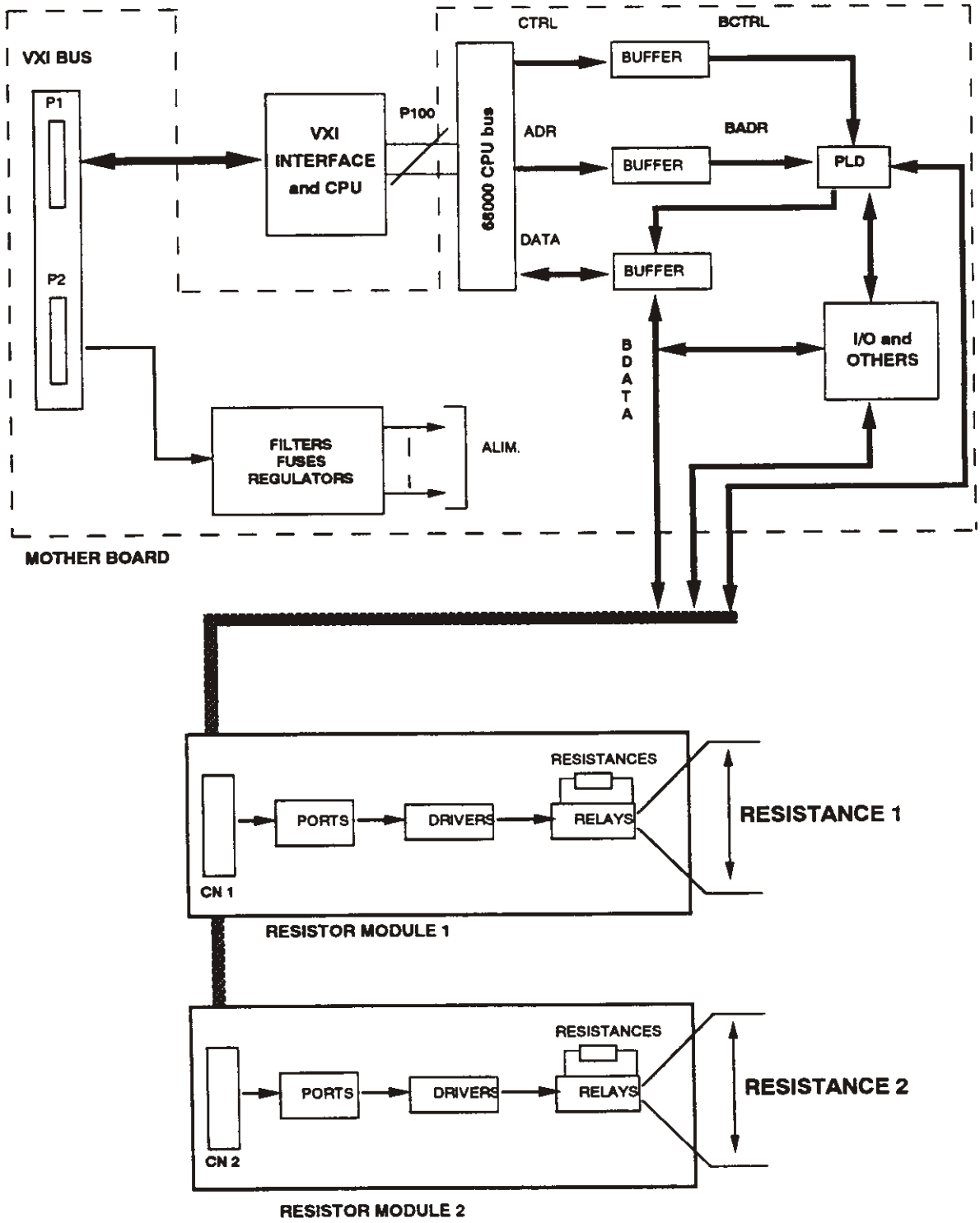
6.2 Block Diagrams





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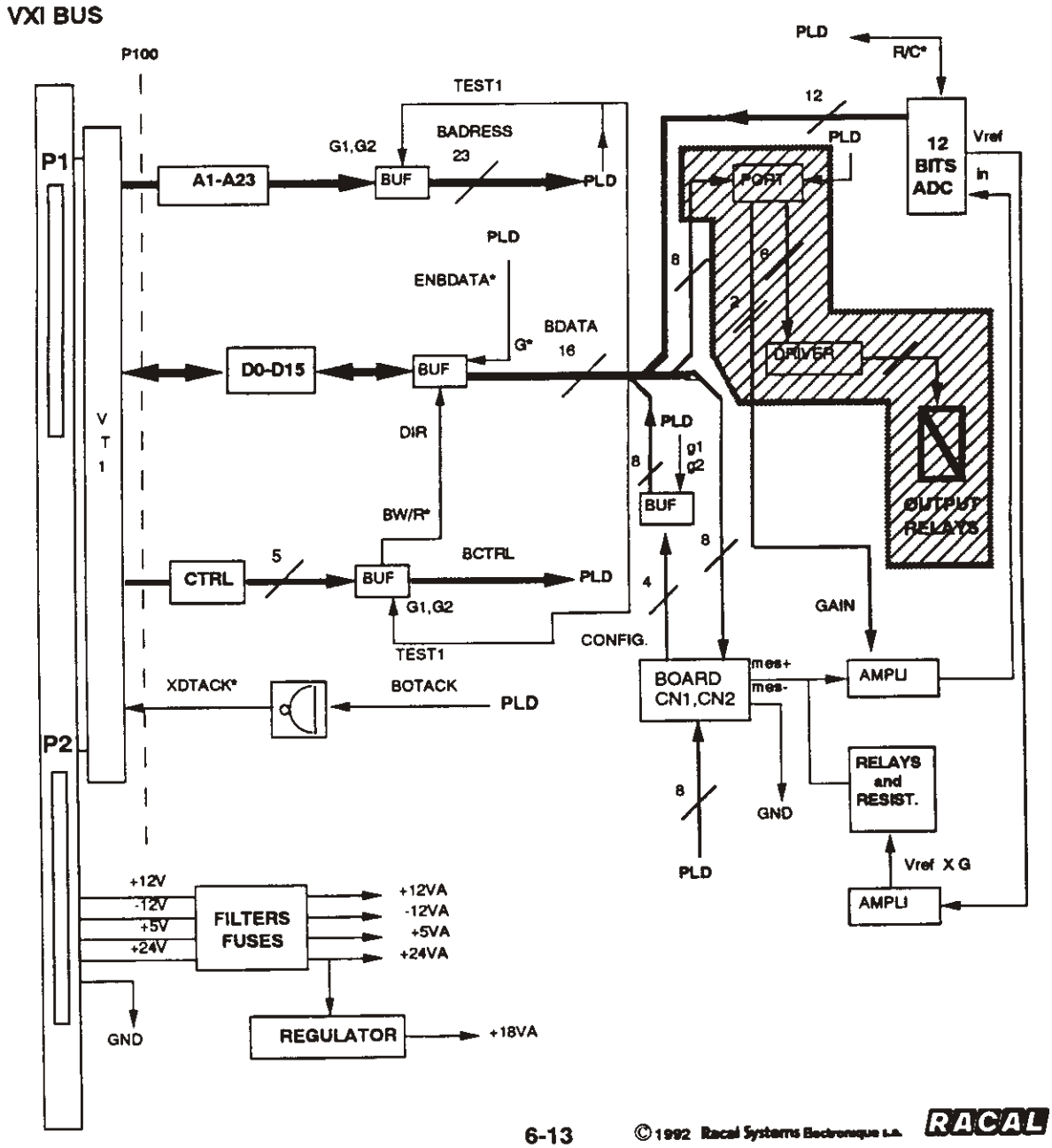
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6.3 Mother Board

6.3.1 Block Diagram
6.3.2 P1 and P2 connectors
6.3.3 Power supplies
6.3.4 Bus buffers and the memory extension
6.3.5 PLD
6.3.6 Self Test

6.3.1 Block Diagram



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6.3.2 Connectors P1 and P2 of the VXI bus.

P1:

N°	Row A	Row B	Row C	N°
1	D00	BBSY*	D08	1
2	D01	BCLR*	D09	2
3	D02	ACFAIL*	D10	3
4	D03	BG0IN*	D11	4
5	D04	BG0OUT*	D12	5
6	D05	BG1IN*	D13	6
7	D06	BG1OUT*	D14	7
8	D07	BG2IN*	D15	8
9	GND	BG2OUT*	GND	9
10	SYSCLK	BG3IN*	SYSFAIL*	10
11	GND	BG3OUT*	BERR*	11
12	DS1*	BR0*	SYSRESET*	12
13	DS0*	BR1*	LWORD*	13
14	WRITE*	BR2*	AM5	14
15	GND	BR3*	A23	15
16	DTACK*	AM0	A22	16
17	GND	AM1	A21	17
18	AS*	AM2	A20	18
19	GND	AM3	A19	19
20	IACK*	GND	A18	20
21	IACKIN*	SERCLK (1)	A17	21
22	IACKOUT*	SERDAT (1)	A16	22
23	AM4	GND	A15	23
24	A07	IRQ7*	A14	24
25	A06	IRQ6*	A13	25
26	A05	IRQ5*	A12	26
27	A04	IRQ4*	A11	27
28	A03	IRQ3*	A10	28
29	A02	IRQ2*	A09	29
30	A01	IRQ1*	A08	30
31	(-12V)	(+5V STDBY)	(+12V)	31
32	(+5V)	(+5V)	(+5V)	32

P2:

N°	Row A	Row B	Row C	N°
1	ECLTRG0	(+5V)	CLK10+	1
2	(-2V)	GND	CLK10-	2
3	ECLTRG1	RSV1	GND	3
4	GND	A24	(-5.2V)	4
5	LBUSA00	A25	LBUSC00	5
6	LBUSA01	A26	LBUSC01	6
7	(-5.2V)	A27	GND	7
8	LBUSA02	A28	LBUSC02	8
9	LBUSA03	A29	LBUSC03	9
10	GND	A30	GND	10
11	LBUSA04	A31	LBUSC04	11
12	LBUSA05	GND	LBUSC05	12
13	(-5.2V)	(+5V)	(-2V)	13
14	LBUSA06	D16	LBUSC06	14
15	LBUSA07	D17	LBUSC07	15
16	GND	D18	GND	16
17	LBUSA08	D19	LBUSC08	17
18	LBUSA09	D20	LBUSC09	18
19	(-5.2V)	D21	(-5.2V)	19
20	LBUSA10	D22	LBUSC10	20
21	LBUSA11	D23	LBUSC11	21
22	GND	GND	GND	22
23	TTLTRG0*	D24	TTLTRG1*	23
24	TTLTRG2*	D25	TTLTRG3*	24
25	(+5V)	D26	GND	25
26	TTLTRG4*	D27	TTLTRG5*	26
27	TTLTRG6*	D28	TTLTRG7*	27
28	GND	D29	GND	28
29	RSV2	D30	RSV3	29
30	MODID	D31	GND	30
31	GND	GND	(+24V)	31
32	SUMBUS	(+5V)	(-24V)	32

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6.3.3 Power supplies.

There are power supplies available on P1 and P2 connectors of the VXI bus:

* +5V (P1:15W, P2: 20W)
* +12V (P1:12W)
* -12V (P1:12W)
* +24V (P2:24W)
* -24V (P2:24W)
* -5.2V (P2:26W)
* -2V (P2:4W)

The DC power of the 4072 & 4072A & 4073 is derived from the VXI backplane via HF (high frequency) filters and fuses. The filters are π-type with high HF performance. The internal fuses are safety fuses that protect the VXI Mainframe.

The specific supplies used by the 4072 & 4072A & 4073 are:

* +5V : Supply voltage for Microprocessor, ADC and all of the logic on Mother board and on Resistance boards.

* ±12V: Supply voltage for ADC and associated components (U10 and U12, page 8-1-8).

* +24V:

- Supply voltage for power driver (U9) and the four relays used by the Self Test (M1 to M4, page 8-1-8).

- Supply voltage for power voltage regulator (U14, page 8-1-2) to produce a regulated 18 VDC (page 8-1-2). This voltage is used to supply the power drivers (B1 to B5, page 8-3-3) and all relay coil of the relays on the Resistance boards. A potentiometer PR2 on the mother board is used to adjust the required voltage to 18V.

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6.3.4 The Bus Buffers and the Memory Extension.

The J101 and J102 connectors connect the signals from P1 and P2 connectors of the VXI bus to the Microprocessor board. All signals of the 68000 Microprocessor are connected to the J100 connector on the mother board (page 9-2).

Three-state buffers are used to amplify the signals to/from the 68000 CPU:

- U1 to U3: buffers for ADDRESS bus (A01 to A23, page 8-1-3).
- U7: buffer for CONTROL bus (RESET*, AS*, R/W*, UDS* and LDS*, page 8-1-4)
- U4 and U5: bidirectional buffers for DATA bus (D00 to D15, page 8-1-5). The "enable" signal is controlled by a PLD(U22). The "direction" signal is controlled by the bufferized R/W* signal from the 68000 CPU.

CAV1 (page 8-1-3) is a special strap. It is used for Control and Test purposes. If this strap is open, then all buffers will be disabled and all bufferized signals will be in "high impedance" state.

U6 is a Input port that identifies the Ranges of Resistance Boards (pages 8-1-5 and 8-3-2) .

Mother board contains a memory extension capacity for future use:

- Four 32 KByte sockets for RAM (U15 to U18, page 8-1-6)
- Two 128 KByte sockets for EPROM (U19 and U20, page 8-1-7)

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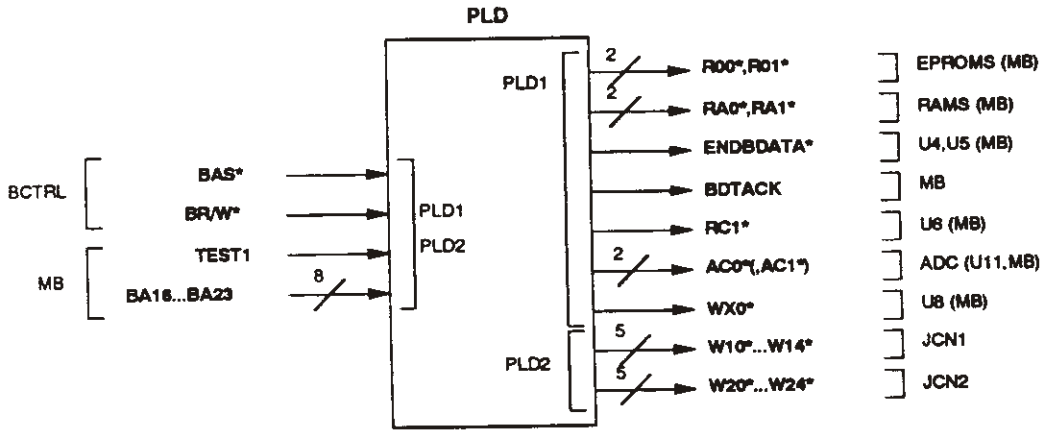
6.3.5 The PLDs.

The 4072 & 4073's mother board contains two 22V10 PLDs (U22 and U23, page 8-1-5).

The address decoding for a "Write to port" activity is performed by U23 to provide W10* to W24* signals. These signals control the "Latch" input of Output Ports implanted on the Resistance boards.

U24 provides RAM and EPROM control signals (chip select). This device also generates the necessary DTACK* signal for the 68000 microprocessor when a valid address is provided. The last function provided by U24 is to generate the control signal (AC0, page 8-1-5) for the Analog to Digital Converter.

Section 6.6 gives more detailed information on the mapping.



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6.3.6 The Self Test

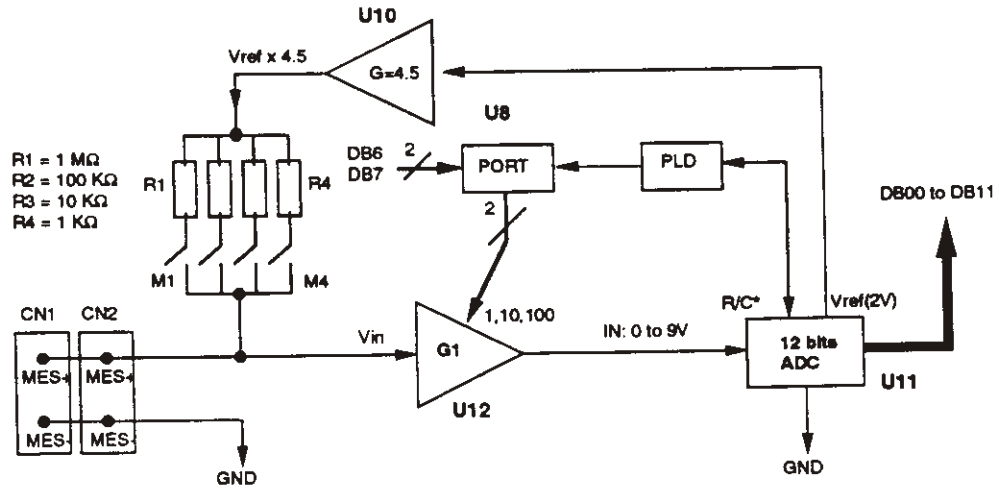
In the first place, we must point out that the purpose of the Self Test is not to measure the exact value of one Resistance, but rather to detect, as precisely as possible, components responsible for bad functioning of the system: for example, an overheated Resistor which causes a clear variation in its value, or a bad relay contact.

During the Self Test, output relays are open (see page 6-22).

Resistance to be tested is switched between MES- and MES+ points. The resistance value to be measured varies between 0.1Ω to 1 MΩ.

The ADC measures a voltage with about 10V full scale. (see page 8-1-8).
The ouput voltage of U10 is about 9 VDC.The software selects the value of the Resistance from R1 to R4 (by closing one relay from M1 to M4) and the amplifier Gain of U12 (by outputting a value to the U8 port) according to the value of the Resistance to be tested. The objective is to obtain a maximum voltage level at the input of the ADC:

* 100 KΩ to 1MΩ : R1 and Gain 1
* 10 KΩ to 100 KΩ : R2 and Gain 1
* 1 KΩ to 10 KΩ : R3 and Gain 1
* 100 Ω to 1 KΩ : R4 and Gain 1
* 10 Ω to 100 Ω : R4 and Gain 10
* 0.1 Ω to 10 Ω : R4 and Gain 100



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6.4 Microprocessor and VXI Inteface Board

6.4.1 Description
6.4.2 P100 Microprocessor bus Connector.

6.4.1 Description

The Microprocessor and VXI Interface board accept commands from the VXIbus, interpret the commands and send the required data to the appropriate Resistance board.

The microprocessor is a Motorola MC68000 operating at 8 MHz. This board also contains ROM, RAM, EEPROM, address decoding, interrupt logic, VXI interface, Local bus interface and a counter//timer.

The program memory consists of a U1 (page 8-2-4) EPROM. This device provides 64K by 16 bits of program memory.

The system RAM consists of two devices, U2 and U3. These devices provide 32K by 16 bits of memory.

The EEPROM consists of two devices, U5 and U6. These devices provide 8K by 16 bits of Non-volatile memory. U4D prevents false writes to the EEPROM during power up and power down sequences ensuring memory integrity.

General address decoding is performed by a 22V10 PLD, U12. This device provides the necessary logic to map the other devices into the microprocessor memory addressing space. This device also provides the DTACK signal required by the microprocessor. The last function provided by U12 is to detect an interrupt cycle from the states of FC0 and FC1 and drop the VPA line.

Address decoding for VXI registers is performed by a 74F138, U9.

System address decoding is performed by discret logic devices (page 8-2-9)

The microprocessor is configured so that it can support 8 TTL Trigger lines from the P2 connector of the VXI interface without requiring the polling of devices to determine the interrupt. These eight sources are encoded by U15, U16 and U21.

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The VXI interface consists of U28, U29, U32, U35 and U37,. The logic decoding is performed by a 22V10 PLD, U36.

The Local bus interface consists of discret logic devices (page 8-2-9). The Lbus interface state machine is implanted in a PAL, U45.

All signals of the 68000 Microprocessor are connected to the P100 connector (P100 will be connected to other buffers and logic devices on the mother board by J100).

6.4.2 P100 Microprocessor bus connector

N°	J100	J100	N°
1	**GND**	A1	2
3	A2	A3	4
5	A4	A5	6
7	A6	A7	8
9	A8	A9	10
11	A10	A11	12
13	A12	A13	14
15	A14	A15	16
17	A16	A17	18
19	A18	A19	20
21	A20	A21	22
23	A22	A23	24
25	**GND**	D15	26
27	D14	D13	28
29	D12	D11	30
31	D10	D9	32
33	D7	D8	34
35	D5	D6	36
37	D3	D4	38
39	D1	D2	40
41	VPA*	D0	42
43	BERR*	VMA*	44
45	**VREGENA***	ECLK	46
47	FC1	FC0	48
49	FC2	XDTACK*	50
51	IRQ4*	IRQ2*	52
53	BG*	**TTLTRIG**	54
55	BR*	BGACK*	56
57	RESET*	HALT*	58
59	R/W*	AS*	60
61	UDS*	LDS*	62
63	**(+5V)**	CPUCLK	64

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6.5 The RESISTANCE Board

6.5.1 Description

The 4072 & 4072A & 4073 model contains two Resistance boards. We describe the 4072 model.

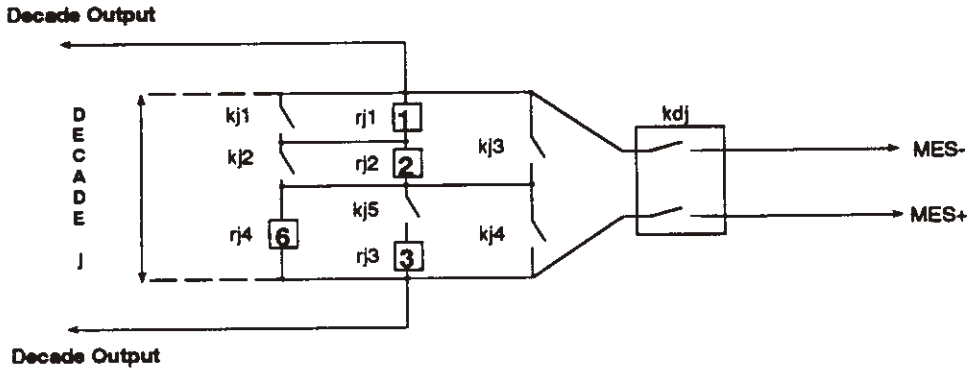
Each Resistance Board contains four "Decades of elementary Resistances". Elementary values chosed are: 1, 2, 3 and 6.

Each Decade uses a combination of parallel and serial mounted Resistances. Four precision Resistances (Rj1, Rj2, Rj3, Rj4) and Five special Relays (Kj1 to Kj5) form a Decade. Only zero, one or two relays are closed to obtain all values from 0 to 9. Each relay contact has a maximum of 40 mΩ of Resistance. Three contacts are connected in parallel to obtain a maximum error of 13 mΩ. So the total error Resistance per decade is limited to 26 mΩ.

F is a 1A fuse that limits the current in use. The error Resistance of the fuse is about one hundredth of mΩ. KF is a relay that can be used to by-pass the fuse when a high precision application is demanded.

The number of Resistances by Resistance board is 16. The number of Relays by Resistance board is 20. The total error resistance by channel is limited to 26 mΩ*4 + 13 mΩ (of KF) or < 120 mΩ.

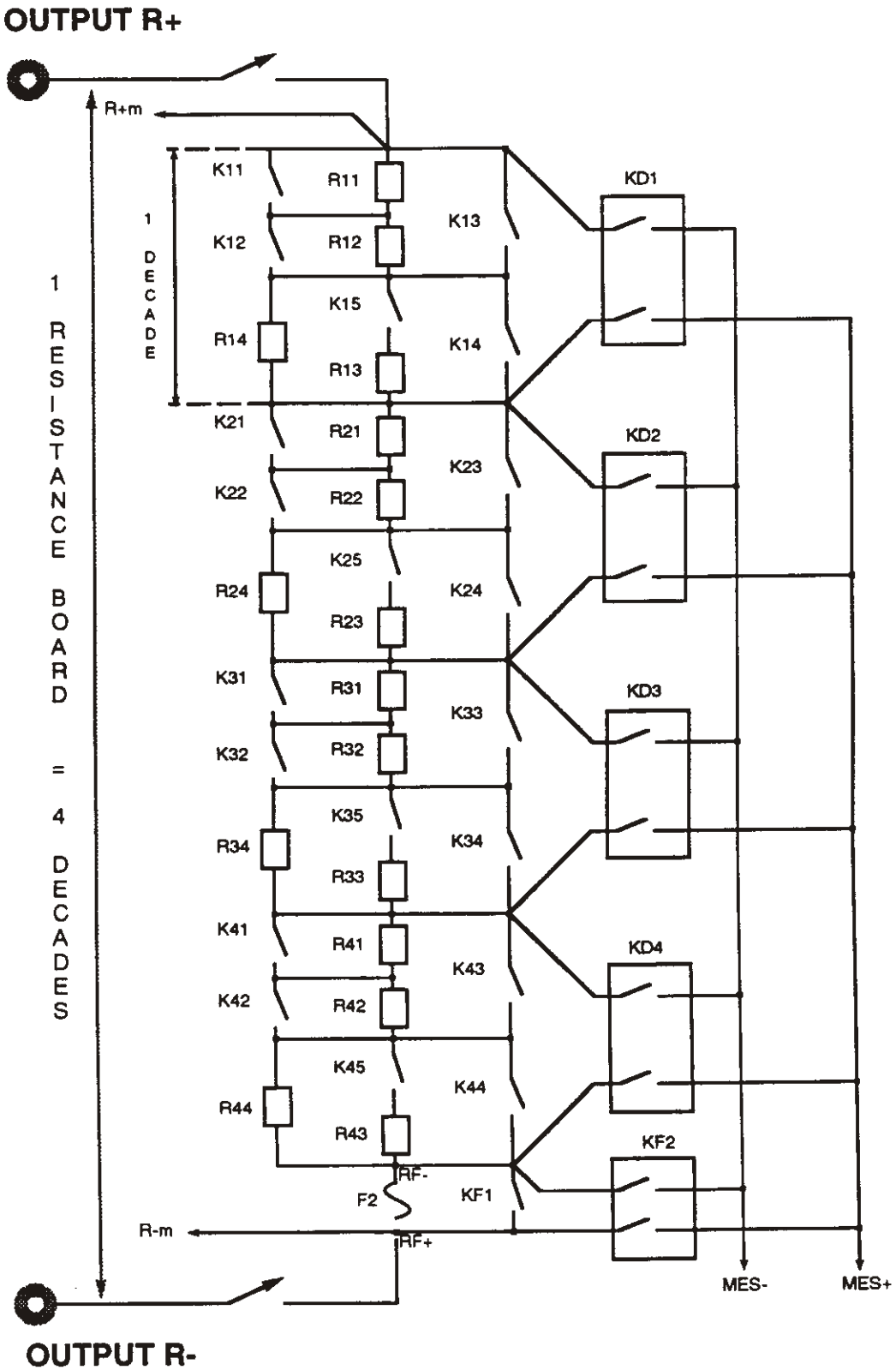
KD1 to KD4 are relays that switch each Decade to the measurement system used by the Self Test. KF is a relay that switches the fuse to the measurement system used by the Self Test.



VALUE	RELAYS CLOSED	Remarks
0	KJ3 KJ4	0 = 0
1	KJ2 KJ4	1 = 1
2	KJ1 KJ4	2 = 2
3	KJ4	3 = 1+2
4	KJ1 KJ5	4 = 2+ (6//3)
5	KJ5	5 = 1+2+(6//3)
6	KJ3	6 = 6
7	KJ2	7 = 1+6
8	KJ1	8 = 2+6
9		9 = 1+2+6

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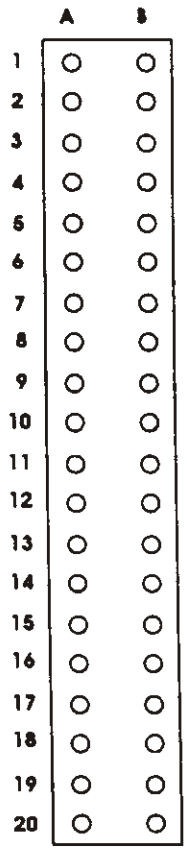
The 4072 & 4072A & 4073 module contains two Resistance boards. Each Resistance board is connected to the mother board by a 20 pin connector (CN1 or CN2, ***page 9-6***).

The **cn** connector is an identification connector. Two input bits (id0, id1) connected to cn indicate to the software the Range of the Resistance board (4 ranges are available: 1KΩ, 10KΩ, 100KΩ and 1MΩ).

Five output ports (P1 to P5, schematic, page 8-3-2) controlled by five Write signals (WP0 to WP4) are used for latching information from the Microprocessor Data Bus (BD00 to BD 07). B1 to B5 are current drivers that command the relay coils.

The relay coils are powered from a 18 VDC regulated voltage source.

6.5.2 CN1 and CN2 connectors:



A		B
GND	1	GND
GND	2	GND
5VA	3	5VA
18VA	4	18VA
18VA	5	18VA
GND	6	GND
BD00	7	BD01
BD02	8	BD03
BD04	9	BD05
BD06	10	BD07
WP0	11	WP1
WP2	12	WP3
TEST1	13	WP4
ID0	14	ID1
NC	15	NC
NC	16	NC
GND	17	GND
MES+	18	MES+
MES-	19	MES-
GND	20	GND

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6.6 Mapping

	ADDRESS	SYMBOLES	Type	Size (byte)	Remarks
ROM	00 0000 - 00 00FF	ROM	Read	256	Valeur d'exception
	00 0100 - 00 07FF	id	Read	1792	JMP Table
	00 0800 - 00 FFFF	id	Read	# 62K	VT-1 code
	01 0000 - 01 FFFF	**ROM**		64K	LIBRE (User on 27C1024)
	02 0000 - 1F FFFF	**ROM**	Read	2M-128K	Reserved for ROM USER
?	20 0000 - 3F FFFF	**Reserved**	?	2 M	RESERVED
RAM	40 0000 - 40 0FFF	RAM	Read, Write	4K	VT-1
	40 1000 - 40 1FFF	RAM	Read, Write	4K	LIBRE
	40 2000 - 40 2FFF	RAM	Read, Write	4K	Heap
	40 3000 - 40 DFFF	RAM	Read, Write	44K	LIBRE (user)
	40 E000 - 40 FFFF	RAM	Read, Write	8K	Stack
	41 0000 - 5F FFFF	**RAM**	Read, Write	2M- 64K	Reserved for RAM USER
NVRAM	60 0000 - 60 3FFF	NVRAM	Read, Write	16K	NVRAM 1
	60 4000 - 60 FFFF	NVRAM	Read, Write	48K	NVRAM 2
	61 0000 - 6F FFFF	**NVRAM**	Read, Write	960K	Reserved for NVRAM USER
	70 0000 - 71 FFFF	TIMER	Read, Write	128K	TIMER
	72 0000 - 77 FFFF	SERIAL	Read, Write	384K	Serial Interface
	78 0000 - 7B FFFF	LBUS	Read, Write	256K	I, O ports on local bus
VXI	7C 0000 - 7C 3FFF	REGENA	Read, Write	16K	VXI registers
	7C 4000 - 7C 7FFF	REGADDR	Read, Write	16K	VXI registers
	7C 8000 - 7C BFFF	RDVXIBLK	Read, Write	16K	VXI registers
	7C C000 - 7C FFFF	HOLDVXI	Read, Write	16K	VXI registers
	7D 0000 - 7D FFFF	RELVXI	Read, Write	64K	VXI registers
	7E 0000 - 7F FFFF	?	?	128K	Reserved
USER	800000 à FF FFFF	USER		8M	User (external decoder)

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	ADDRESS	SYMBOLES	Type	Size	Remarks	Used
PLD 1	80 0000-81 FFFF	RO0*	Read	128K	Extended EPROM	MB
	82 0000-83 FFFF	RO1*	Read	128K	id.	MB
	84 0000-8F FFFF			768K	Free	
	90 0000 - 90 FFFF	RA0*	Read/Write	64K	Extended RAM	MB
	91 0000 - 91 FFFF	RA1*	Read/Write	64K	id.	MB
	92 0000-9F FFFF			896K	Free	
	A0 xxxx	RC1*	Read	64K	Read System Config	MB
	A1 xxxx	AC0*	Read, word	64K	Read ADC	MB
	A2 xxxx	AC1*	Read, word	64K	RESERVED	MB
	A3 xxxx	WX0*	Write	64K	Ouput Port	MB
	A4 0000-AF FFFF			768K	Free	
PLD 2	B0 xxxx	W10*	Write	64K	Write to output port	JCN1
	B1 xxxx	W11*	Write	64K	id.	JCN1
	B2 xxxx	W12*	Write	64K	id.	JCN1
	B3 xxxx	W13*	Write	64K	id.	JCN1
	B4 xxxx	W14*	Write	64K	id.	JCN1
	B5 0000-BF FFFF			768K	Free	
	C0 xxxx	W20*	Write	64K	Write to output port	JCN2
	C1 xxxx	W21*	Write	64K	id.	JCN2
	C2 xxxx	W22*	Write	64K	id.	JCN2
	C3 xxxx	W23*	Write	64K	id.	JCN2
	C4 xxxx	W24*	Write	64K	id.	JCN2
	C5 0000-CF FFFF			768K	Free	
	D0 0000-FF FFFF			3 MB	RESERVED	

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SECTION 7
SOFTWARE & COMMANDS

7.1 List of commands and summary of syntax

7.2 "SYSTem" commands

7.3 Self Test

7.4 Environment commands

7.5 Commands for Immediate Resistance setting

7.6 Commands for Triggered Resistance setting

7.7 Principle Diagram of Trigger mode

7.8 Trigger commands

7.9 STATus registers

7.10 Example: Driver for LabWindows (National Instruments)

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7.1 LIST of COMMANDS

```
SYSTem          :PRESet
                |:VERSion?
                |:ERRor?

TEST            :RESistance1?
                |:RESistance2?

[SOURce]        :RESistance1        [:IMMediate]
                |:RESistance2       |:TRIGgered
                                    |:PROTection
                                    |:SMOothing

                                     :LIMIT          :HIGH
                                                     |:LOW
TRIGger         :RESistance1        [:IMMediate]
                |:RESistance2       |:COunt
                                    |:ECOunt
                                    |:SOURce

                 :TTLTrg            [:STATe]
                                    |:SELect

                 :BUS               [:STATe]

INITiate         :RESistance1
|ABORt          |:RESistance2

OUTPut           :TTLTrg            [:STATe]
                                     :SELect
                                     :SOURce

OUTPut          :RESistance1        [:STATe]
                |:RESistance2

STATus           :OPERation         [:EVENt]?
                                    |:CONDition?
                                    |:ENABle
                                    |:INSTrument
                                                    [:EVENt]?
                                                    |:CONDition?
                                                    |:ENABle
                                    |:RESistance1
                                                    [:EVENt]?
                                                    |:CONDition?
                                                    |:ENABle
                                    |:RESistance2
                                                    [:EVENt]?
                                                    |:CONDition?
                                                    |:ENABle
                                    |:PRESet

*CLS
*ESE, *ESE?, *ESR?
*OPC, *OPC?
*SRE, *SRE?
*STB?
*WAI
*RST
*TST?
*IDN?
*OPT?
*TRG
```


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Summary of SCPI syntax.

• An SCPI command (Program header) is made up of key words (<program mnemonic>) separated by ":" and possibly finished by a question mark if a reply is expected (Query form), the command is separated from the first parameter (if one exists) by one or several spaces (or more precisely"<White Space Character>"conforming to IEEE 488.2).

Example : "SOURce:RES1:LIMit:HIGH 10.0E3" or "RES1:LIMit:HIGH?"

•A complete message(<program message>:command + associated parameters) is ended either by an EOI, a <NL>(Line Feed:code ASCII 10,#H0A), or by a semi-colon, in this case several messages can be joined together on the same line.

Example : "RES1 2.5E03;RES2 1.35E02"

• A key word making up a command can be used just as well in a short form (capital letters in the description) as in a long form (capital and small letters), the rule being that the short form is made up of the first four characters of the long form, the last character being a vowel only if the long form has four characters or less.

Example : the key word SOURce can be written "source" (long form) or "sour" (short form), "RESistance" can be written "res" or "resistance", "DATA" is identical under the two forms.

• In the case of a key word with a channel rating, it will be associated as well with the long form as with the short form.

Example : the short form of "RESistance1" is "res1".

• The capital letters and the small letters can be used indifferently for the commands and parameters of string type.

Example : "SOurCe:Res1?" and "source:RESISTANCE1 ?" are correct.
• An expression contained within "[ ]" is optional.

Example : [SOURce]:RESistance1[:IMMediate] means that this command can be written "source:resistance1:immediate", "sour:res1", "res1", etc.....

• The symbol "|" is an "OR" and indicates a choice.

Example : "<ON|OFF>"indicates that for this, both ON and OFF are valid.

• The spaces (<White Space Character>) can be inserted at will between commands and parameters or between parameters but not within a command nor a parameter (string type).

Example : "re s1?"is not correct but " res1 2.5E02 ; " is correct.

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7.2 "SYSTem" commands

SYSTem:PRESet or ***RST**

Description : Initializes the module

• No Query form.

SYSTem:VERSion? ==> <num_val>

Description : Returns the System Software version number

SYSTem:ERRor? ==> <character_data>

Description : Returns an error message from the Queue (FIFO stack). The oldest error is the first transmitted. A transmitted error is suppressed from the Queue. When the Queue is empty, the "No error" message is transmitted. When the Queue is full, the message "-350, "Queue overflow"" is stored and no other message is stored until a message is read from the Queue.

***OPT? ==> <num_val1>, <num_val2>**

Description : Returns the Range of each Resistance sub module (unit: KΩ)

Results:

<num_val1> = Range of RESistance1

<num_val2> = Range of RESistance2

Example:

"*OPT?" ==> "1,100"

In that case the range of RESistance1 is 1 KΩ (0 to 999.9 Ω), and the range of RESistance2 is 100 KΩ (0 to 99.9 KΩ)

***IDN? ==> RACAL,1030, <serial_number>, <firmware_version>**

This is a case of one 4072.

***IDN? ==> RACAL,1040, <serial_number>, <firmware_version>**

This is a case of one 4073.

***TRG** Generates a Software Trigger which has the same effect as a "Word Serial Trigger"

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7.3 SELF TEST

TEST:RESistance1? ==> <char_data>{, <char_data>}
TEST:RESistance2? ==> <char_data>{, <char_data>}

Description : Executes the Self Test of the specified Resistance and returns the result.

Result :
1) "PASSED" if the test is OK
2) "FAILED, ..." with the list of faulty components.

Example :
If "TEST:RES1?" returns "FAILED, Fuse" then the fuse of the Resistance R1 is damaged or missing.
If "TEST:RES2?" returns "FAILED, R11, R34" then the Resistances R11 and R34 are faulty .

***TST? ==> <num_value>**

Description : Executes the Self Test of both Resistance R1 and R2, and returns the result. .

Result :
If **<num_value>** = 0, the Test is OK, otherwise the returned number (in binary form) identifies the faulty components :

*4096 : The Voltage reference(9V) used by Self Test is not correct.
*2048 : The configuration of R1 is faulty.
*1024 : The fuse of R1 is faulty.
*512 : The decade 1 of R1 is faulty.
*256 : The decade 2 of R1 is faulty.
*128 : The decade 3 of R1 is faulty.
*64 : The decade 4 of R1 is faulty.
*32 : The configuration of R2 is faulty.
*16 : The fuse of R2 is faulty.
*8 : The decade 1 of R2 is faulty.
*4 : The decade 2 of R2 is faulty.
*2 : The decade 3 of R2 is faulty.
*1 : The decade 4 of R2 is faulty.

Example :
If "*TST?" returns "16" then the fuse of R2 is faulty.
If "*TST?" returns "260" then the decade 2 of R1 and the decade 2 of R2 are faulty (because 260=256+4)

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7.4 Environment commands

OUTPut:RESistance1[:STATe] <ON|OFF>
OUTPut:RESistance2[:STATe] <ON|OFF>

Description :
Connects (ON) or disconnects (OFF) the specified Resistance.

• Query form :

OUTPut:RESistance1[:STATe]? => <ON|OFF>
OUTPut:RESistance2[:STATe]? => <ON|OFF>

[SOURce]:RESistance1:LIMit:HIGH <num_val>
[SOURce]:RESistance2:LIMit:HIGH <num_val>

Description :
Defines the upper limit of the Resistance. Setting a higher value will cause the Resistance to be clamped to the LIMit:HIGH value.

Parameter :
<num_val> is a numerical value, format <NRf> of IEEE 488.2 standard, the unit is **Ohm.**

Initialization : No limit.

Example :
"RES1:LIMIT:HIGH 10.0E3" for a maximum R1 value of 10 kΩ .
If "RES1 20.0E3" is requested later then the effective value will be 10 kΩ.

• Query form :

[SOURce]:RESistance1:LIMit:HIGH? => <num_val>
[SOURce]:RESistance2:LIMit:HIGH? => <num_val>

[SOURce]:RESistance1:LIMit:LOW <num_val>
[SOURce]:RESistance2:LIMit:LOW <num_val>

Description :
Defines the lower limit of the Resistance. Setting a lower value will cause the Resistance to be clamped to the LIMit:LOW value.

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Initialization : No limit.

• Query form :

[SOURce]:RESistance1:LIMit:LOW? => <num_val>
[SOURce]:RESistance2:LIMit:LOW? => <num_val>

[SOURce]:RESistance1:PROTection <ON|OFF>
[SOURce]:RESistance2:PROTection <ON|OFF>

Description :

If "ON", the fuse is connected to the Resistance; if "OFF", the fuse is strapped.

Initialization : ON

• Query form :

[SOURce]:RESistance1:PROTection? => <ON|OFF>
[SOURce]:RESistance2:PROTection? => <ON|OFF>

[SOURce]:RESistance1:SMOothing <ON|OFF>
[SOURce]:RESistance2:SMOothing <ON|OFF>

Description :

If "ON", the transition from one value of Resistance to another is "smoothing" by passing through intermediate values. In this mode, the transition time is **3 times** longer.

If "OFF", all relays of a Resistance board are switched simultaneously causing unexpected values of resistance to appear before complete establishment. In this mode, the transition time is shorter.

Initialization : ON

• Query form :

[SOURce]:RESistance1:SMOothing? => <ON|OFF>
[SOURce]:RESistance2:SMOothing? => <ON|OFF>

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7.5 Commands for Immediate Resistance setting

[SOURce]:RESistance1[:IMMediate] <num_val>
[SOURce]:RESistance2[:IMMediate] <num_val>

Description :
Sets immediately the specified Resistance value.

Parameter :
<num_val> is a numerical value, format <NRf> of IEEE 488.2 standard. The unit is **Ohm**. The effective value is the ***closest*** .

Initialization :
The maximum value .

Example :
"RES2 2.5E03" sets R2 to 2.5 kΩ .
If the range of R1 is 10 KΩ (0 to 9999 Ω, resolution 1Ω), "RES1 123.45E00" sets R1 to 123 Ω.

• **Query form :**

[SOURce]:RESistance1[:IMMediate]? => <num_val>
[SOURce]:RESistance2[:IMMediate]? => <num_val>

Description :
Returns the ***actual value*** of the Resistance.

Example :
If the Resistance range is 1MΩ (then the resolution is 100Ω), and the Command Message is "RES1 152.34" then the answer to "RES1?" will be "200".

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7.6 Commands for Triggered Resistance setting

[SOURce]:RESistance1:TRIGgered <num_val>
[SOURce]:RESistance2:TRIGgered <num_val>

Description :

Indicates that subsequent specification of a new resistance settings are to be transferred to the IMMediate value upon receipt of a trigger signal. (After a INITiate command).

Parameter :

<num_val> is a numerical value, format <NRf> of IEEE 488.2 standard. The unit is **Ohm**. The effective value is the ***closest*** possible value.

• Query form :

[SOURce]:RESistance1:TRIGgered? ==> <num_val>
[SOURce]:RESistance1:TRIGgered? ==> <num_val>

INITiate:RESistance1
INITiate:RESistance2

Description :

Validates the trigger conditions. When the trigger conditions are completed, the "triggered" settings are transferred.

• No Query form

ABORt:RESistance1
ABORt:RESistance2

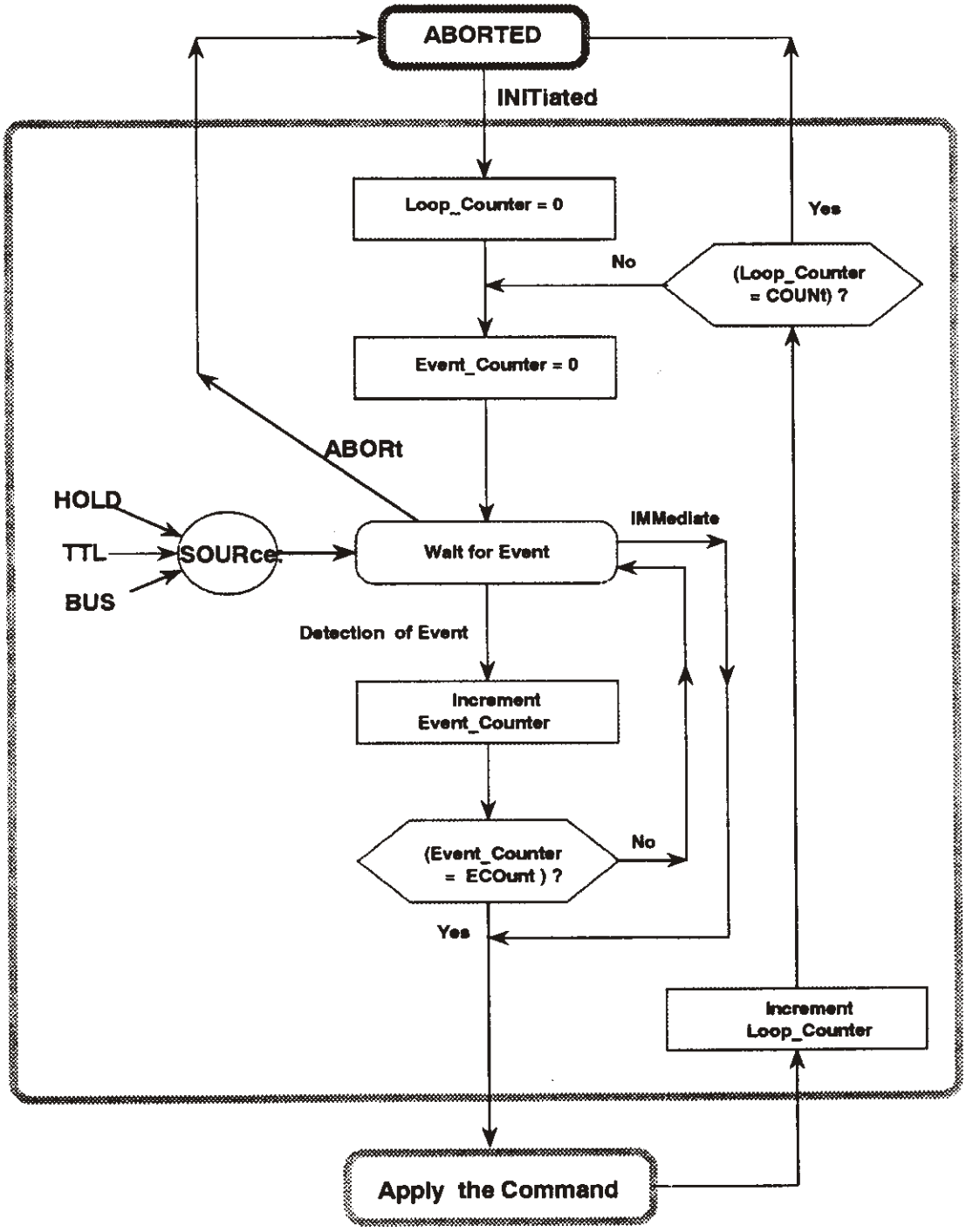
Description :

Aborts the trigger cycle. A new INITiate command is necessary to restart the cycle.

• No Query form

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7.7 Principle Diagram of Trigger mode



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7.8 Trigger commands

TRIGger:TTLTrg:SELect <num_value>

Description : Selects one TTL trigger line to be used (1 among the 8 TTL trigger lines available from the VXI bus). The implicit choice is TTL trigger line 0.

Parameters : **<num_value>** is an integer number from 0 to 7.

Examples : "trig:ttlt:sel 4" selects the TTLtrig number 4.

• Query form :

TRIGger:TTLTrg:SELect? ==> <num_value>

TRIGger:TTLTrg [:STATe] <ON|OFF>

Description : Enables (ON) or Disables (OFF) the interrupts from the selected TTL trigger line to be transmitted to the trigger conditions. The implicit value is ON.

• Query form :

TRIGger:TTLTrg [:STATe]? ==> <ON|OFF>

TRIGger:BUS[:STATe] <ON|OFF>

Description : Enables (ON) or Disables (OFF) the GET interrupts to be transmitted to the trigger conditions. The implicit value is ON.

• Query form :

TRIGger:BUS[:STATe]? ==> <ON|OFF>

TRIGger:RESistance1:SOURce <char_data>
TRIGger:RESistance2:SOURce <char_data>

Description : Selects the trigger source for a Resistance.

Parameter :
<char_data> can be:

HOLD : disables all trigger sources, only "TRIGger:RESistance[:IMMediate] " can make the triggered value to be transferred.

TTLTrg : the selected event is the TTL trigger line selected by TRIGger:TTLtrg:SELect.

BUS : the selected event is the reception of "Word Serial Trigger" message or "*TRG" command of IEEE 488.2 standard.

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Initialization : HOLD

• Query form :

TRIGger:RESistance1:SOURce? ==> <char_data>
TRIGger:RESistance2:SOURce? ==> <char_data>

TRIGger:RESistance1:ECOunt <num_value>
TRIGger:RESistance2:ECOunt <num_value>

Description :

Sets the number of events defined by "STARt:SOURce" to be counted before the TRIGger condition is completed.

Parameter :

<num_value> is an integer between 1 and 2 power 32 -1 (approximatively 4300 millions times).

Initialization : ECOunt=1

•Query form :

TRIGger:RESistance1:ECOunt? ==> <num_value>
TRIGger:RESistance2:ECOunt? ==> <num_value>

TRIGger:RESistance1[:IMMediate]
TRIGger:RESistance2[:IMMediate]

Description :

This command overcomes the TRIGger SOURce, the TRIGger ECOunt and accomplishes the TRIGger condition. To be taken in account, this command must be sent after a "INITiate" command. This command is useful when the "SOURce" is "HOLD" .

•No Query form.

TRIGger:RESistance1:COUNt <num_value>
TRIGger:RESistance2:COUNt <num_value>

Description :

Defines the loop number of TRIGgers to be completed after one "INITiate".

Parameter :

<num_value> is an integer between 0 and 2 power 32 -1 (approximatively 4300 millions times).

A zero value means an infinite loop (as long as an ABORt command is not received, the cycle continues).

Initialization : 0, the loop is infinite.

•Query form :

TRIGger[:GLOBal]:COUNt? ==> <num_value>

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OUTput:TTLTrg[:STATe] <ON|OFF>

Description :

Enables or Disables the emission of one pulse on the TTLtrig line selected by the "OUTPut:TTLTrig:SELect" command when a Resistance value is transferred.

Parameter :

ON : Enables the emission of a feedback trigger.
OFF : Disables the emission of a feedback trigger.

•Query form :

OUTPut:TTLTrg[:STATe]? ==> <ON|OFF>

OUTPut:TTLTrg:SELect <num_value>

Description :

Selects the trigger line on which the feedback trigger pulse will be emitted.

Parameter :

<num_value> is an integer from 0 to 7.

•Query form :

OUTPut:TTLTrg:SELect? ==> <num_value>

OUTPut:TTLTrg:SOURce <char_data>

Description :

Selects the origin of the pulse emission on a TTL trigger line.

Parameter:

<char_data> can be:

RESistance1 : The emission is due to R1 value transfer.

RESistance2 : The emission is due to R2 value transfer.

GLOBal : The emission is due to both R1 or R2 value transfer.

•Query form :

OUTPut:TTLtrg:SOURce? ==> <char_data>

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7.9 STATus Registers

- **7.9.1 General Description**
- **7.9.2 Description of STATus Register Contents**
- **7.9.3 CONDition Registers associated with EVENt Registers**
- **7.9.4 Status Command List**

7.9.1 General description

• IEEE 488.2 Standard prescribes two registers : **"Status Byte"** and **"Standard Event Status Register"**.

• The**"Status Byte"** gives global information on the system state in such a way that a user can select information to be reported (through Enable registers).

• The **"Standard Event Register"** reports Standard Events such as "Errors detection" or "Operation Complete" .

• Further SCPI registers are available, either CONDition, EVENt or ENABle registers.

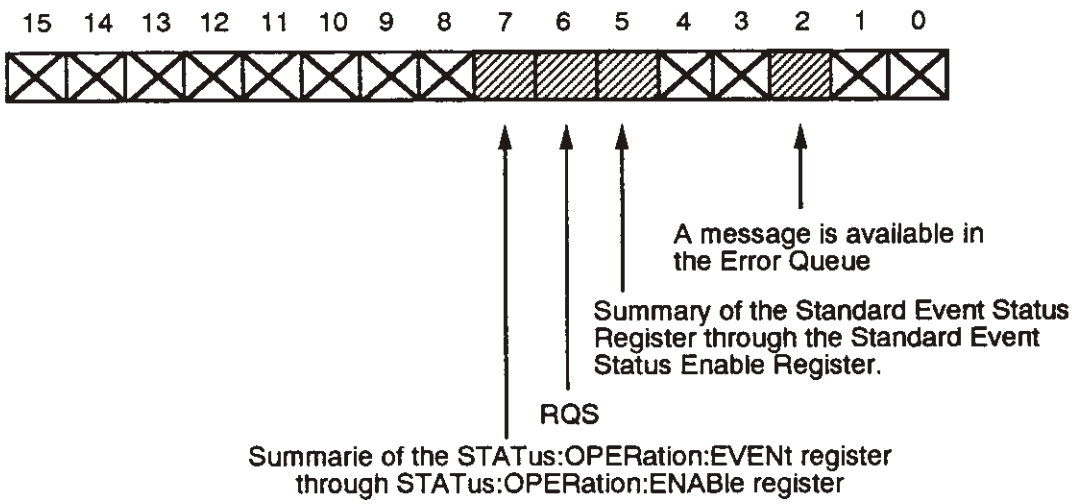
• A **CONDition** register gives information on specific device states, every change in a device state causes the associated CONDition register to be changed immediately while **EVENt** registers only capture changes in the corresponding condition register, they can be cleared only by reading them or by "*CLS" command.

• Some bits in an **EVENt** register may not reflect changes in the corresponding register, they summarize selected bits from another EVENt register, the bit selection is specified in the ENABle register.

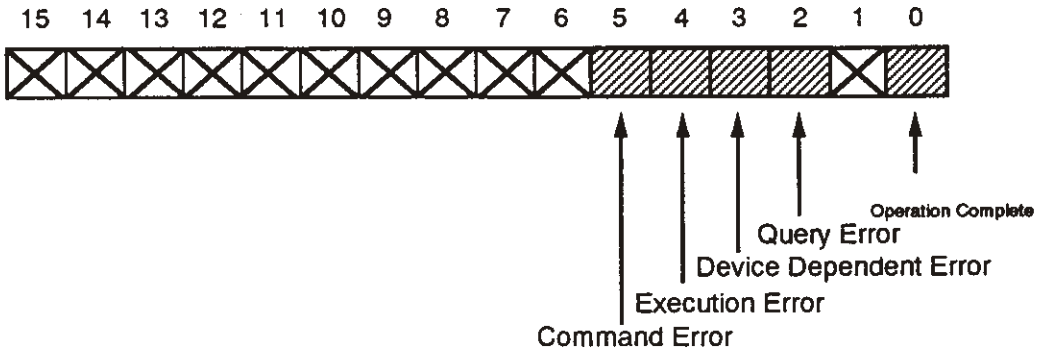
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7.9.2 Description of Status register Contents

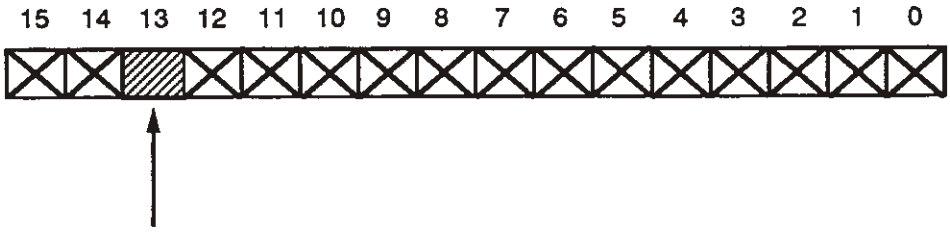
STATUS BYTE



STANDARD EVENT STATUS REGISTER

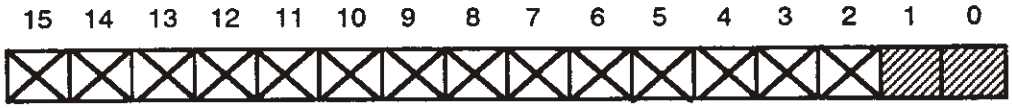


STATus:OPERation:EVENt register



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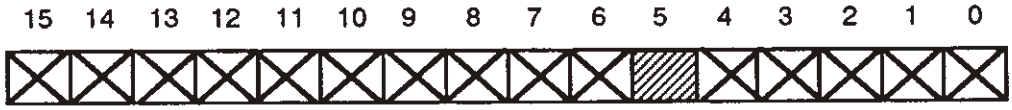
STATus:OPERation:INSTrument:EVENt register



Summary of the STATus:OPERation:RESistance2:EVENt register through the STATus:OPERation:RESistance2:ENABle register

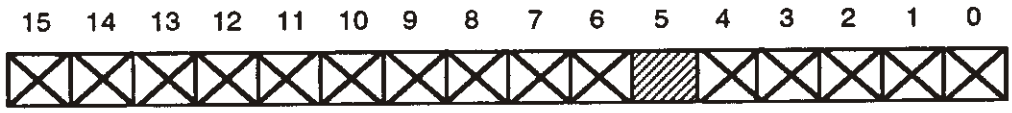
Summary of the STATus:OPERation:RESistance1:EVENt register through the STATus:OPERation:RESistance1:ENABle register

STATus:OPERation:RESistance1:EVENt register



End of the "Waiting for Trigger" state for RESistance1

STATus:OPERation:RESistance2:EVENt register

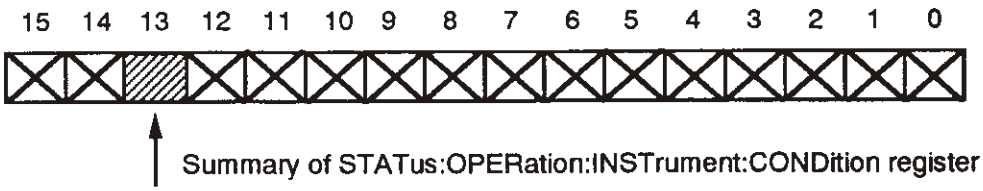


End of the "Waiting for Trigger" state for RESistance2

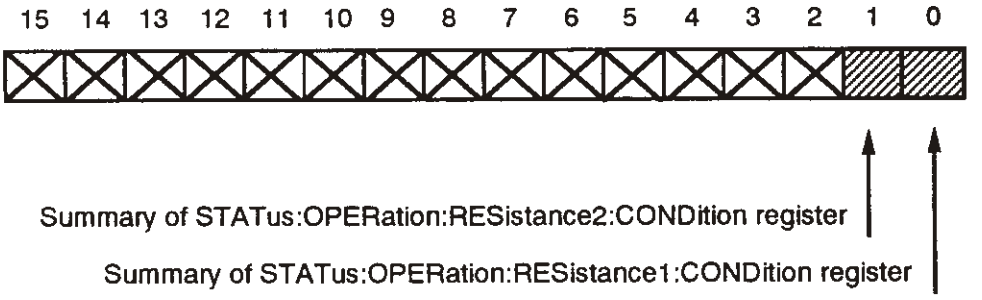
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7.9.3 CONDition registers associated with precedent EVENt registers

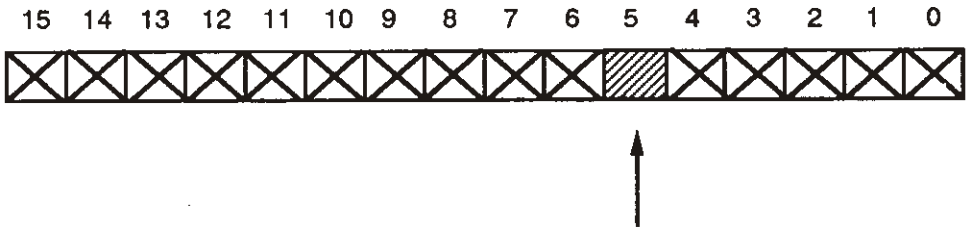
STATus:OPERation:CONDition register



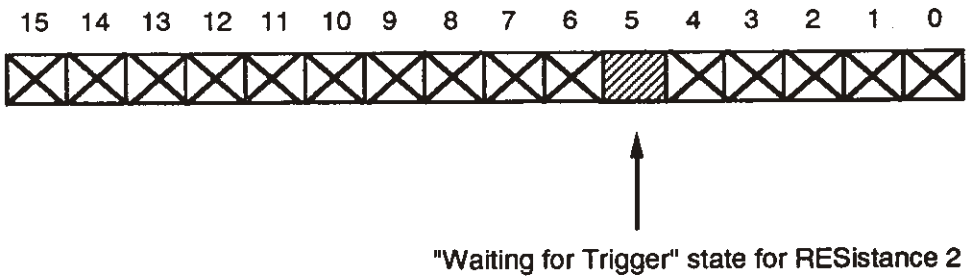
STATus:OPERation:INSTrument:CONDition register



STATus:OPERation:RESistance1:CONDition register



STATus:OPERation:RESistance2:CONDition register



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7.9.4 Status Command List

***CLS**

Description : Clears all event registers and empties the error queue.

***ESE <num_value>**

Description : Sets the Standard Event Status Enable Register bits.

Parameter : A bit set to one allows the corresponding bit in the Standard Event Status Register to be reported in bit 5 of Status Byte.

Initialization : 0, none bit of SESR is reported in SB.

Example : "*ESE 16" allows bit 5 of SB to be set every time an execution error occurs.

***ESE? ==> <num_value>**

Description : Returns the contents of the Standard Event Status Enable register.

***ESR? ==> <num_value>**

Description : Returns the contents of the Standard Event Status register, reading the SESR clears it.

***STB? ==> <num_value>**

Description : Returns the contents of the Status Byte.

Other commands available : ***OPC, *OPC?, *SRE, *SRE? et *WAI .**

SCPI commands of type "STATus:OPERation" are described below:

EVENt? : Returns the contents of the specified EVENt register, reading it clears it.

CONDition? : Returns the contents of the specified CONDition register.

ENABle : Sets the specified ENABle register.

ENABle? : Returns the contents of the specified ENABle register.

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STATus:PRESet

Description : Initializes all ENABle registers, **but** doesn't clear EVENt ones.

Remarks :

There are only two bits in the EVENt registers that really reflect changes in the device state, these are bits 5 of STATus:OPERation:RESistance1:EVENt and STATus:OPERation:RESistance2:EVENt, all the others are summaries.

Contrary to EVENt summaries which are dependent on ENABle registers, CONDition summaries are made without conditions.

At initialization (Power-on or STATus:PRESet) :

STATus:OPERation:ENABle = 0

Bit 13 (the only one used in this register) of STATus:OPERation:EVENt register is not reported in bit 7 of Status Byte register.

STATus:OPERation:INSTrument:ENABle = 3

Both bits 0 and 1 of STATus:OPERation:INSTrument:EVENt register are reported in bit 13 of STATus:OPERation:EVENt register.

STATus:OPERation:RESistance1:ENABle = 0
STATus:OPERation:RESistance2:ENABle = 0

Bits 5 of STATus:OPERation:RESistance1:EVENt and STATus:OPERation:RESistance2:EVENt registers are not reported in bits 0 and 1 of STATus:OPERation:INSTrument:EVENt register.

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7.10 Drivers for LabWindows (National Instruments)

Note: this program is given for example only. RACAL does not warrant that the operation of this program will meet your requirements or operate free from error.

```
'= RD4072 Instrument Module

REM     ' Version 1.04   3th August 1992


'=========================================================
REM = RD4072 Include File
'=========================================================

REM $INCLUDE: 'c:\LW\INCLUDE\LWSYSTEM.INC'
REM $INCLUDE: 'c:\LW\INCLUDE\GPIB.INC'
REM $INCLUDE: 'c:\LW\INCLUDE\FORMATIO.INC'

'=========================================================
' = GLOBAL FUNCTION DECLARATIONS
'=========================================================

DECLARE SUB RD4072.INIT  (p0%,p1%)
DECLARE SUB RD4072.RE1  (p0%,p1%,p2%,p3%,p4#,p5%,p6%)
DECLARE SUB RD4072.RE2  (p0%,p1%,p2%,p3%,p4#,p5%,p6%)
DECLARE SUB RD4072.TST  (p0%)
DECLARE SUB RD4072.CLOSE  ()

'=========================================================
' = GLOBAL VARIABLE DECLARATIONS
'=========================================================

COMMON SHARED /RD4072.err/ RD4072.err%
COMMON SHARED /mod1/ mod1#
COMMON SHARED /mod2/ mod2#
COMMON SHARED /conf1/ conf1$
COMMON SHARED /conf2/ conf2$
```


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```
'= RD4072 Instrument Module ================================================

'= RD4072 Instrument Module

REM    ' Version 1.04   3th August 1992

"= UTILITY ROUTINES ========================================================

DECLARE FUNCTION RD4072.device.closed% ()
DECLARE FUNCTION RD4072.read.data% (cmd$, v..cnt%)
DECLARE FUNCTION RD4072.write.data% (cmd$, v..cnt%)
DECLARE FUNCTION RD4072.invalid.real.range% (v..real.val#, v..min#, v..max#, v..err.code%)
DECLARE FUNCTION RD4072.invalid.integer.range% (v..int.val%, v..min%, v..max%, v..err.code%)
DECLARE FUNCTION RD4072.SYST.ERR%(cmd$)

'= LOCAL VARIABLES =========================================================

DIM SHARED bd AS INTEGER       ' bd contains the descriptor returned by OpenDev
DIM SHARED cmd AS STRING * 80   ' cmd is a buffer for GPIB I/O strings
DIM SHARED cm AS STRING * 80    ' cmd is a buffer for GPIB I/O strings

'============================================================================
' This functions opens the instrument, queries for ID, and initializes the
' instrument to a known state.
'============================================================================

SUB RD4072.init (pradd%,secadd%)


  STATIC n%,md1%,md2%


' Check for valid address

  IF RD4072.invalid.integer.range% (pradd%, 0, 30, -1) <> 0 THEN
    RD4072.err%=-1
    EXIT SUB
  END IF

  IF RD4072.invalid.integer.range% (secadd%, 0, 30, -1) <> 0 THEN
    RD4072.err%=-1
    EXIT SUB
  END IF

' If device has not been opened (bd <> 0), open it

  IF bd% <= 0 THEN
    n% = CloseInstrDevs("RD4072")
    bd% = OpenDev% ("", "RD4072")
    IF bd% <= 0 THEN
      RD4072.err% = 220
      EXIT SUB
    ELSE
      RD4072.err% = 0
    END IF
  END IF
```


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```
' Change the primary address of the device

  IF ilpad% (bd%, pradd%) < 0 THEN
     n% = CloseDev% (bd%)
     bd% = 0
     RD4072.err% = 233
     EXIT SUB
  END IF

' Change the secondary address of the device

  IF ilsad% (bd%, secadd%+96) < 0 THEN
     n% = CloseDev% (bd%)
     bd% = 0
     RD4072.err% = 234
     EXIT SUB
  END IF

' System Preset

     n%=Fmt(cmd$,"%s<%s","SYST:PRES")

     IF RD4072.write.data% (cmd$,NumFmtdBytes%) <> 0 THEN
              EXIT SUB
     END IF

' Read configuration

     n%=Fmt(cmd$,"%s<%s","*OPT?")

     IF RD4072.write.data% (cmd$,NumFmtdBytes%) <> 0 THEN
              EXIT SUB
     ENDIF

     IF RD4072.read.data% (cmd$,20) <> 0 THEN
              EXIT SUB
     ENDIF

          n%=Scan(cmd$,"%s[t44]>%d",md1%)

     SELECT CASE md1%
     CASE 1
          n%=Scan(cmd$,"%s>1,%d",md2%)
          conf1$="  999.9 Ω"
     CASE 10
          n%=Scan(cmd$,"%s>10,%d",md2%)
          conf1$="  9.999 kΩ"
     CASE 100
          n%=Scan(cmd$,"%s>100,%d",md2%)
          conf1$="  99.99 kΩ"
     CASE 1000
          n%=Scan(cmd$,"%s>1000,%d",md2%)
          conf1$="  999.9 kΩ"
     END SELECT

     SELECT CASE md2%
     CASE 1
          conf2$="  999.9 Ω"
     CASE 10
          conf2$="  9.999 kΩ"
     CASE 100
          conf2$="  99.99 kΩ"
     CASE 1000
          conf2$="  999.9 kΩ"
     END SELECT
```


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```
        n%=Fmt(mod1#,"%f<%d",md1%)
         n%=Fmt(mod2#,"%f<%d",md2%)

         mod1#=mod1#/10.0
         mod2#=mod2#/10.0

    IF  RD4072.SYST.ERR%(cmd$) <> 0 THEN
            EXIT SUB
    ENDIF


END SUB



'=============================================================================
' This instrument removes the instrument from the GPIB device table and
' sets bd to zero.
'=============================================================================

SUB RD4072.close

'  Check for device closed

   IF RD4072.device.closed% <> 0 THEN
      EXIT SUB
   END IF

'  Place device in local mode

   IF Illoc% (bd%) <= 0 THEN
      RD4072.err% = 234
      EXIT SUB
   END IF

'  Close the device

   IF CloseDev% (bd%) < 0 THEN
      RD4072.err% = 221
   ELSE
      RD4072.err% = 0
   END IF
   bd% = 0

 END SUB
```


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```
'=============================================================================
'=                    RESISTANCE 1
'=============================================================================

SUB RD4072.RE1 (dec11%,dec12%,dec13%,dec14%,val1#,prot1%,conn1%)

STATIC n%,fr#,dec%

' Write Protection Configuration

IF prot1% = 1 THEN

     n%=Fmt(cmd$,"%s<%s","RES1:PROT ON")

     IF RD4072.write.data% (cmd$,NumFmtdBytes%) <> 0 THEN
          EXIT SUB
     ENDIF
ELSE
     n%=Fmt(cmd$,"%s<%s","RES1:PROT OFF")

     IF RD4072.write.data% (cmd$,NumFmtdBytes%) <> 0 THEN
          EXIT SUB
     ENDIF
ENDIF

     IF  RD4072.SYST.ERR%(cmd$) <> 0 THEN
          EXIT SUB
     ENDIF

' Write Connection Configuration

IF conn1% = 1 THEN

     n%=Fmt(cmd$,"%s<%s","OUTP:RES1 ON")

     IF RD4072.write.data% (cmd$,NumFmtdBytes%) <> 0 THEN
          EXIT SUB
     ENDIF
ELSE
     n%=Fmt(cmd$,"%s<%s","OUTP:RES1 OFF")

     IF RD4072.write.data% (cmd$,NumFmtdBytes%) <> 0 THEN
          EXIT SUB
     ENDIF
ENDIF

     IF  RD4072.SYST.ERR%(cmd$) <> 0 THEN
          EXIT SUB
     ENDIF

' Convert data and send

     b$= "RES1 "

     dec%=(dec11%*1000)+(dec12%*100)+(dec13%*10)+dec14%

     n%=Fmt(fr#,"%f<%d",dec%)

     fr#=fr#*mod1#

     n%=Fmt(cmd$,"%s<%s%f",b$,fr#)

     IF RD4072.WRITE.DATA%(cmd$,NumFmtdBytes%) <> 0 THEN
          EXIT SUB
     ENDIF
```


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```
' Read value

IF conn1%=1 THEN

    n%=Fmt(cmd$,"%s<%s","RES1?")

    IF RD4072.write.data% (cmd$,NumFmtdBytes%) <> 0 THEN
            EXIT SUB
    ENDIF

    IF RD4072.read.data% (cmd$,20) <> 0 THEN
            EXIT SUB
    ENDIF


    ' Data conversion (String --> Real)

        n%=Fmt(val1#,"%f[p2]<%s",cmd$)

    IF  RD4072.SYST.ERR%(cmd$) <> 0 THEN
            EXIT SUB
    ENDIF
ELSE
    val1#=9.9999e99
ENDIF

END SUB


'=============================================================================
'=                    RESISTANCE 2
'=============================================================================


SUB RD4072.RE2 (dec21%,dec22%,dec23%,dec24%,val2#,prot2%,conn2%)

STATIC n%,fr#,dec%

' Write Protection Configuration

IF prot2% = 1 THEN

    n%=Fmt(cmd$,"%s<%s","RES2:PROT ON")

    IF RD4072.write.data% (cmd$,NumFmtdBytes%) <> 0 THEN
            EXIT SUB
    ENDIF
ELSE
    n%=Fmt(cmd$,"%s<%s","RES2:PROT OFF")

    IF RD4072.write.data% (cmd$,NumFmtdBytes%) <> 0 THEN
            EXIT SUB
    ENDIF
ENDIF
```


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```
    IF  RD4072.SYST.ERR%(cmd$) <> 0 THEN
            EXIT SUB
    ENDIF

' Write Disconnection Configuration

IF conn2% = 1 THEN

    n%=Fmt(cmd$,"%s<%s","OUTP:RES2 ON")

    IF RD4072.write.data% (cmd$,NumFmtdBytes%) <> 0 THEN
            EXIT SUB
    ENDIF
ELSE
    n%=Fmt(cmd$,"%s<%s","OUTP:RES2 OFF")

    IF RD4072.write.data% (cmd$,NumFmtdBytes%) <> 0 THEN
            EXIT SUB
    ENDIF
ENDIF

    IF  RD4072.SYST.ERR%(cmd$) <> 0 THEN
            EXIT SUB
    ENDIF

' Convert data and send

    b$= "RES2 "

    dec%=(dec21%*1000)+(dec22%*100)+(dec23%*10)+dec24%

    n%=Fmt(fr#,"%f<%d",dec%)

    fr#=fr#*mod2#

    n%=Fmt(cmd$,"%s<%s%f",b$,fr#)

    IF RD4072.WRITE.DATA%(cmd$,NumFmtdBytes%) <> 0 THEN
            EXIT SUB
    ENDIF

' Read value

IF conn2%=1 THEN

    n%=Fmt(cmd$,"%s<%s","RES2?")

    IF RD4072.write.data% (cmd$,NumFmtdBytes%) <> 0 THEN
            EXIT SUB
    ENDIF


    IF RD4072.read.data% (cmd$,20) <> 0 THEN
            EXIT SUB
    ENDIF


    ' Data conversion (String --> Real)

        n%=Fmt(val2#,"%f[p2]<%s",cmd$)

    IF  RD4072.SYST.ERR%(cmd$) <> 0 THEN
            EXIT SUB
    ENDIF
ELSE
  val2#=9.9999e99
ENDIF

END SUB
```


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```
'=============================================================================
'=                        TEST
'=============================================================================

SUB RD4072.TST(auto%)

STATIC n%

' Read test feedback


     n%=Fmt(cmd$,"%s<%s","*TST?")

     IF RD4072.write.data% (cmd$,NumFmtdBytes%) <> 0 THEN
               EXIT SUB
     ENDIF

' Change the time out limit

   IF iltmo% (bd%, 13) < 0 THEN
      n% = CloseDev% (bd%)
      bd% = 0
      RD4072.err% = 235
      EXIT SUB
   END IF


     IF RD4072.read.data% (cmd$,5) <> 0 THEN
               EXIT SUB
     ENDIF

     n%=Fmt(auto%,"%d<%s",cmd$)

' Change the time out limit

   IF iltmo% (bd%, 13) < 0 THEN
      n% = CloseDev% (bd%)
      bd% = 0
      RD4072.err% = 235
      EXIT SUB
   END IF

     IF  RD4072.SYST.ERR%(cmd$) <> 0 THEN
               EXIT SUB
     ENDIF

END SUB



'= UTILITY ROUTINES   ( FUNCTIONS ) ==================================


'=============================================================================
' This function checks wether the module has been initialized.  If the
' device has not been opened, a 1 is returned, 0 otherwise.
'=============================================================================
```


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```
FUNCTION RD4072.device.closed%

  IF bd% <= 0 THEN
     RD4072.err% = 232
     RD4072.device.closed% = 1
     EXIT FUNCTION
  END IF
  RD4072.device.closed% = 0
  EXIT FUNCTION

END FUNCTION

'=============================================================================
' This function checks wether an integer lies between a minimum and
' maximum value.  If the value is out of range, set the global error
' variable to the value err.code.  If the value is OK, error = 0.  The
' return value is equal to the global error value.
'=============================================================================

FUNCTION RD4072.invalid.integer.range% (int.val%, min%, max%, err.code%)

  IF int.val% < min% OR int.val% > max% THEN
     RD4072.err% = err.code%
     RD4072.invalid.integer.range% = 1
     EXIT FUNCTION
  END IF
  RD4072.invalid.integer.range% = 0
  EXIT FUNCTION

END FUNCTION

'=============================================================================
' This function checks wether a real number lies between a minimum and
' maximum value.  If the value is out of range, set the global error
' variable to the value err.code.  If the value is OK, error = 0.  The
' return value is equal to the global error value.
'=============================================================================

FUNCTION RD4072.invalid.real.range% (real.val#, min#, max#, err.code%)

  IF real.val# < min# OR real.val# > max# THEN
     RD4072.err% = err.code%
     RD4072.invalid.real.range% = 1
     EXIT FUNCTION
  END IF
  RD4072.invalid.real.range% = 0
  EXIT FUNCTION

END FUNCTION
```


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```
'=============================================================================
' This function reads a buffer of data from the GPIB interface.  If an error
' occurs, set the global error variable to 231, else set it to 0.  Return
' the error value.
'=============================================================================

FUNCTION RD4072.READ.DATA% (cmd$, cnt%)

   CALL FillBytes (cmd$,0,leng%,0)
   CALL FillBytes (cm$,0,leng%,0)

   IF iird% (bd%, cm$, cnt%) <= 0 THEN
      RD4072.ERR% = 231
   ELSE
      RD4072.ERR% = 0
   END IF
   RD4072.read.data% = RD4072.ERR%

   n%=Scan(cm$,"%s[w*]>%s",(ibcnt%),cmd$)


END FUNCTION



'=============================================================================
' This function writes a buffer of data to the GPIB interface.  If an error
' occurs, set the global error variable to 230, else set it to 0.  Return
' the error value.
'=============================================================================

FUNCTION RD4072.WRITE.DATA% (cm$, cnt%)

   IF iiwrt% (bd%, cm$, cnt%) <= 0 THEN
      RD4072.ERR% = 230
   ELSE
      RD4072.ERR% = 0
   END IF

   RD4072.WRITE.DATA% = RD4072.ERR%

   CALL FillBytes (cm$,0,ibcnt%,0)

END FUNCTION
```


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```
'=============================================================================
' This function checks if a system error occurs.Comment$ contains the error
' message from the RD4072 module.
'=============================================================================


FUNCTION RD4072.SYST.ERR%(cmd$)

    CALL FillBytes (cmd$,0,leng%,0)

    IF ilwrt% (bd%, "SYST:ERR?", 9) <= 0 THEN
      RD4072.ERR% = 230
    ELSE
      RD4072.ERR% = 0
    END IF

    IF ilrd% (bd%, cmd$, 80) <= 0 THEN
      RD4072.ERR% = 231
    ELSE
      RD4072.ERR% = 0
    END IF

    n%=Scan (cmd$,"%s>%l",er%)

    IF er%<>0 THEN
       PRINT cmd$
    ENDIF

    RD4072.ERR%=-er%
    RD4072.SYST.ERR%=-er%

END FUNCTION


END
```


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Racal Instruments

REPAIR AND CALIBRATION REQUEST FORM

To allow us to better understand your repair requests, we suggest you use the following outline when calling and include a copy with your instrument to be sent to the Racal Repair Facility.

Model_____Serial No._____Date_____

Company Name_____Purchase Order #_____

Billing Address_____

City

State/Province Zip/Postal Code Country

Shipping Address_____

City

State/Province Zip/Postal Code Country

Technical Contact_____Phone Number ( )_____
Purchasing Contact _____Phone Number ( )_____

1. Describe, in detail, the problem and symptoms you are having. Please include all set up details, such as input/output levels, frequencies, waveform details, etc.

2. If problem is occurring when unit is in remote, please list the program strings used and the controller type.

3. Please give any additional information you feel would be beneficial in facilitating a faster repair time (i.e., modifications, etc.)

4. Is calibration data required? Yes No (please circle one)

Call before shipping
Note: We do not accept "collect" shipments.

Ship instruments to nearest support office listed on back.

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Support Offices

Racal Instruments, Inc.
4 Goodyear Street
Irvine, CA 92718-2002
Phone: 1-949-859-8999
1-800-RACAL-ATE
1-800-722-2528
FAX: 1-949-859-7309

Racal Instruments Ltd
480 Bath Road
Slough, Berkshire
SL1 6BE, United Kingdom
Phone: +44 (0) 1628 604455
FAX: +44 (0) 1628 662017

Racal Systems Electronique
18 Avenue Dutartre
78150 LeChesnay, France
Phone: +33 (1) 3923 2222
FAX: +33 (1) 3923 2223

Racal Systems Elettronica Srl
Strada 2-Palazzo C4
20090 Milanofiori Assago
Milan, Italy
Phone: +39 (02) 5750 1796
FAX: +39 (02) 5750 1828

Racal Elektronik System GmbH
Frankenforster Strasse 21
51427 Bergisch-Gladbach ,1Germany
Phone: +49 2204 92220
FAX: +49 2204 21491

Racal Australia Pty Ltd
3 Powells Road
Brookvale, NSW 2100, Australia
Phone: +61 (2) 9936 7000
FAX: +61 (2) 9936 7036

Racal Electronics Pte Ltd
26 Ayer Rajah Crescent, 04-06/07
Ayer Rajah Industrial Estate, Singapore 0513
Phone: +65 7792200
FAX: +65 7785400

Racal Instruments Ltd.
Room 1213 Nan Fung Centre
Tsuen Wan, New Territories
Hong Kong
Phone: +852-2405 5500
FAX: +852 2416 4335

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