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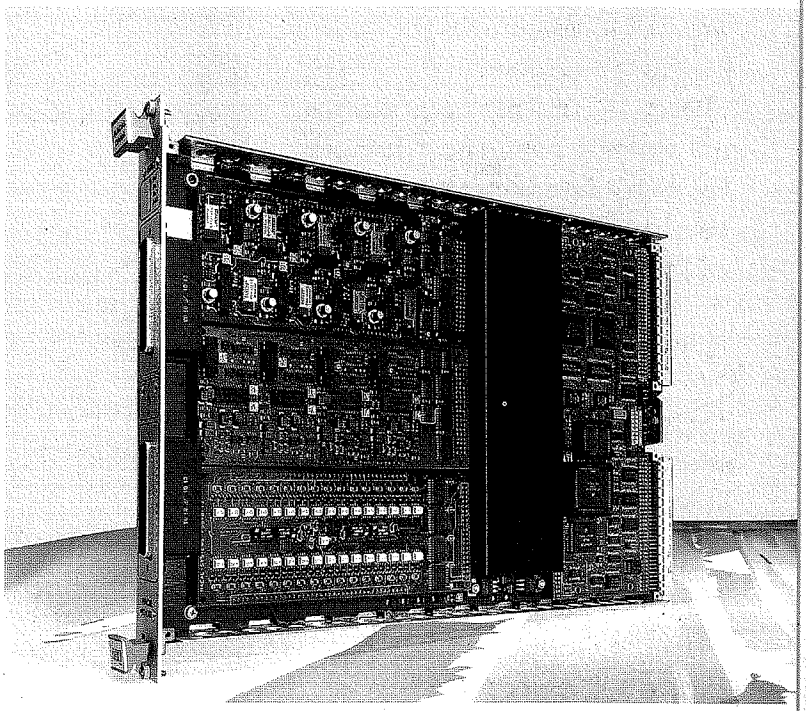
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Find the *EADS / Racal / Dana 6061A* at our website: ***Click HERE***

PRODUCT INFORMATION

Universal Analog & Digital Input / Output Modules
Models 6060 / 6061



- ❒ *Unique combination of analog and digital channels*
- ❒ *Fully isolated input / output channels on the 6061*
- ❒ *16 analog channels*
- ❒ *32 digital channels*
- ❒ *12 bits resolution*
- ❒ *Self test*
- ❒ *Internal memory for data storage*

INTRODUCTION

The 6060 and 6061 modules provide a unique combination of analog and digital channels in the same module. Different configurations are available according to the different versions A, B, C or D.

The A version includes 8 analog output channels, 8 analog input channels and 32 digital input/output channels.

APPLICATIONS

The 6060 and 6061 are able to cover a large range of applications in a VXI system, when a large number of analog input and output channels are required.

The internal memory with the Trace Mode capability allows the user to replace a large quantity of arbitrary function generators at low frequencies.

VXI SPECIFICATIONS

VXI message based instruments.
Word serial protocol.
1.3 compatibility.
SCPI compatibility.
Trigger capability
(TTL-TRG Ø to TRG 7).
Driver trigger capability
(TTL-TRG Ø to TRG 7).
Single slot.
C size.

RACAL INSTRUMENTATION

RACAL

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A high integration level

The 6060 and 6061 modules, based on a high integration of components offer today a unique combination of analog and digital channels in the same module. The 6060 and 6061 provide 16 analog channels and 32 digital channels.

Multiple configurations

The modular concept of the 6060 and 6061 gives a complete range of products with different types of inputs and outputs, analog or digital. The user has the possibility to choose between 8 different configurations to optimise his application.

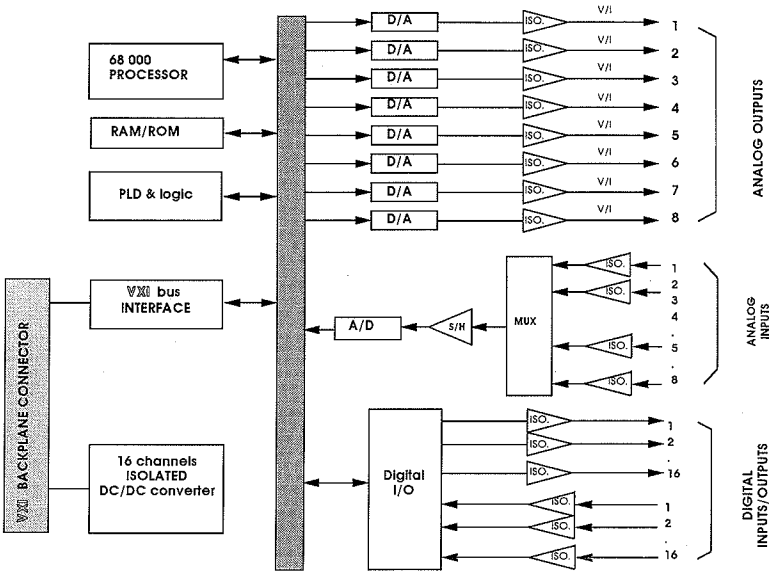


Figure 1: Architecture of 6061

Isolated channels

The 6061 is a fully isolated module providing 750 volts isolation between channels or between channel and ground.
The 6060 is the non isolated version.

Self test

An internal self test gives the user a high level of confidence. This feature is very important for systems applications (ATE).
The self test covers all channels, analog and digital.

SCPI capability

The 6060 and 6061 are message based VXI modules, fully compatible with the revision 1.3 . In addition these modules are SCPI compatible.

Powerful memory capability

The 256 Kbytes internal memory can be used to generate arbitrary waveform signals on the analog or digital outputs or to store data from the analog or digital inputs. The user himself can define the size and name for each channel.
As an option the memory can be extended to 512 Kbytes.

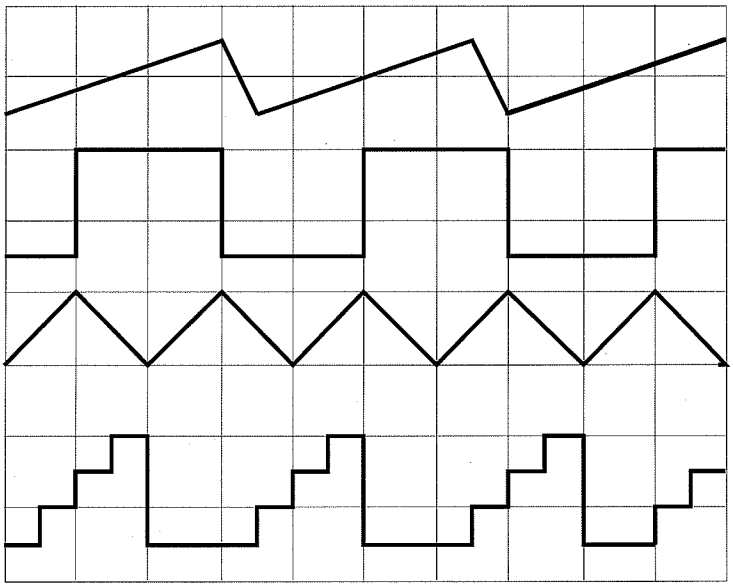


Figure 2 : Type of signal generated by output channel

Triggering capability

An internal programmable timer is used to control the rate on each channel. Additional triggering capability allows the module to be used as a multiple low frequency arbitrary waveform generator.

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Applications in the Automotive Industry.

The 6061 and 6060 models are much used in the automotive industry by cars and car equipments manufacturers .

The most important application concerns the simulation of the inputs and outputs of a car computer where the module is used as a multiple arbitrary low frequency and DC function generator. For example, an injection computer must control the opening of the carburator, engine rotation, oil pressure, temperature and battery voltage. For these signals, the D/A output may be used.

Similarly, the A/D input may be used to store the voltage generated by the calculator under test.

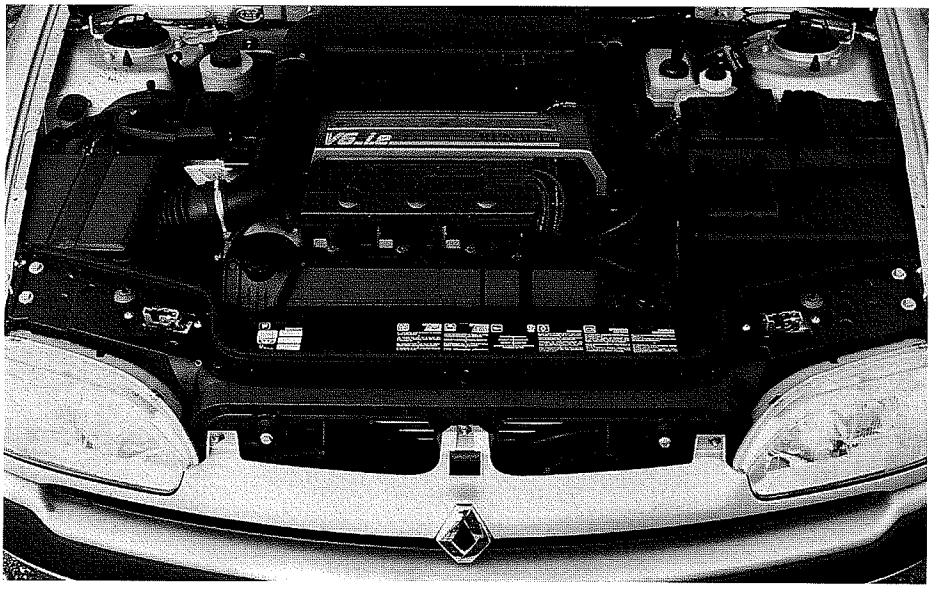


Photo fournie par la Régie Renault

Moreover, digital input - output ports are used to simulate gear speeds, binary sensors number of contacts or faulty lamps.

Controlling Device.

The 6060 or 6061 may be used as a VXI analog controlling device for test equipment built with DC motors or lasers.

For example, TTL channels may be used to control the frequency scan of the beam and the wave length and the absorption peak are measured with the A/D inputs.The alarms of the laser may also be monitored with the 6061.

Therefore, a voltage programmable device becomes a VXI programmable device.

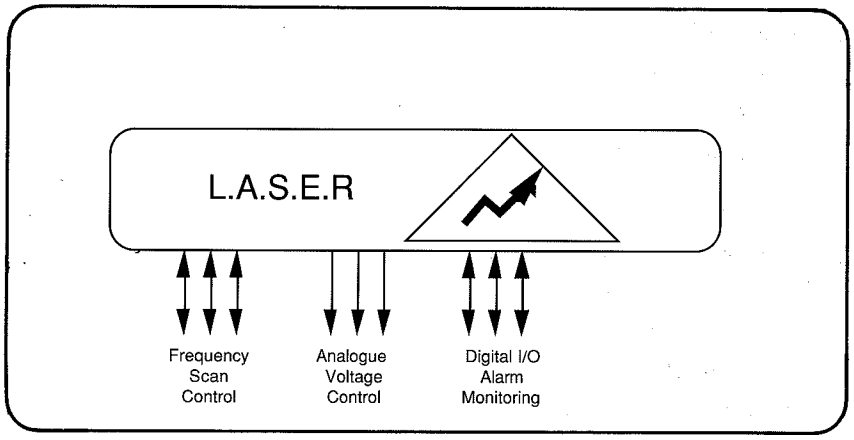


Figure 3 : Controlling a voltage programmable device

Configuration guide

Product Reference	Isolated Inputs/Outputs	Digital channels Inputs/Outputs	Analog Inputs	Analog Outputs
6060A	No	32	8	8
6060B	No	32	-	16
6060C	No	32	16	-
6060D	No	32	-	-
6061A	Yes	32	8	8
6061B	Yes	32	-	16
6061C	Yes	32	16	-
6061D	Yes	32	-	-

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TECHNICAL SPECIFICATIONS

Analog outputs

Number of channels	0, 8 or 16*
Ranges	1V,5V,10V,+/-1V,+/-5V,+/-10V
Resolution	12 bits
Linearity	0.01% FSR
Residual noise	2 mV rms, 10 mV pp (1V range) 5 mV rms, 30 mV pp (other ranges)
Setting time	20µS to 1%, 100µS to 0.1%
Slew rate	> 0.1V/µS
Output resistance	< 2Ω
Maximum current output	20mA (at 35°C)
Isolation voltage	750 V rms (50/60 Hz)**

Analog inputs

Number of channels	0, 8 or 16*
Ranges	1V,5V,10V,+/-1V,+/-5V,+/-10V
Resolution	12 bits
Linearity	0.03% FSR (5V and 10V ranges)
Residual noise	+/- 5mV
DC rejection	> 100 dB
AC rejection	> 80 dB
Input impedance	> 1 MΩ
Overvoltage protection	250 V rms (50/60 Hz)
Isolation voltage	750 V rms (50/60 Hz)**

Digital Outputs

Number of channels	16
Vhl high	3 to 35 V
Vhl low	< 1.3 V
Current sink max	50 mA
Slew rate	> 0.6 V/µS
Isolation	750V rms (50/60 Hz)**

Digital Inputs

Number of channels	16
Vhl high	3 to 35 V
Vhl low	2 V
Current sink max	5mA
Isolation	750 V rms (50/60 Hz)**

** Depending on version A/B/C/D*
*** 6061 version only*

Common Specifications

Data rate	
- interactive mode	< 10mS per logical group
- trace mode	130 µS + n x 30µS for digital and D/A channels 150 µS + n x 35µS for A/D channels where n is the number of channels used
Memory size	256 Kbytes
Trigger mode	SOURce, IMMediate, COUNt, ECOunt
Trigger source	Bus(GET),VXI trigger lines or Timer
Timer period	1 to 4 295 000 000 units 1 unit = 8 µs
Connectors	Two 78 pins high density
VXI compatibility	Revision 1.3, message based, SCPI
Cooling	4.0 l/S, 0.5 mm H_2O
Power requirements	5 VDC/2.5 A, +24 V/0.6 A, -24 V/0.1 A
Size	1 slot
Weight	2.5 Kg (5.5 lbs)

Option 01
16 Volts inputs/outputs

Ranges	1.6V, 8V, 16V,+/-1.6V, +/- 8V, +/- 16V
Residual noise	40 mV pp

Option 02
Digital TTL inputs/outputs

Outputs	
Vout high	> 2.4 V
Vout low	< 0.6 V
Transition time	< 20 nS(500/50 pf)
Inputs	
Vin max	6.5 V
Vin high	> 2V
Vin low	< 0.8 V

Option 03-4 or 03-8
Current outputs

Number of current outputs	4 or 8 (replace 4 or 8 voltage outputs)
Ranges	2mA, 10mA, 20mA,+/-2mA, +/-10mA, +/-20mA
Accuracy	0.2%FSR
Output resistance	>50KΩ

Option 04
Memory extension

Memory size	512 Kbytes

Option LW-01-6060/61
Labwindows 2.1 Driver for external PC

Option LW-02-6060/61
Labwindows 2.1 Driver for VXI PC and MXI.

RACAL INSTRUMENTATION RACAL

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The Racal policy is one of continuous development and consequently the equipment may vary in detail from the description and specification in this publication

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European Council Directive 89/336/CEE modified by the 92/31/CEE Directive and by the 93/68/CEE Directive.

Mr Antoine BARTOLI, legal responsible for

RACAL SYSTEMS ELECTRONIQUE S.A.
18 Av. Dutartre, 78150 Le Chesnay

DECLARES
that the VXI Racal Instrument **6060 / 6061** modules were designed, manufactured and commercialized to comply with the standards :

EN 55022-B
EN 50082-1

according to the Directive recommandations :

- 89/336/CEE "Electro Magnetic Compatibility"

Mr Antoine BARTOLI, Managing Director for

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78150 LE CHESNAY
Tél. 39.55.88.88 - Fax 39.55.67.35
S.A. au Capital de 30.000.000 F

At Le Chesnay, 12 December, 1995

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VXI bus

RACAL
The Electronics Group

MODEL 6060 & 6061

UNIVERSAL ANALOG&DIGITAL

INPUT/OUTPUT VXI MODULE

P/N: 33-1010-9999
Version : 1.1-C
August 1994

Release 1.1-C- August 1994

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PUBLICATION NO. 33-1010-9999

Model 6060 & 6061 Universal Analog & Digital Input / Output

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RACAL

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Items sold by Racal-Dana Instruments Inc. are warranted only as stated below:
Subject to the exceptions and upon the conditions specified below, Racal-Dana agrees to correct, either by repair, or, at its election, by replacement, any defects of material or workmanship which develop within one year after delivery of the instrument to the original purchaser by Racal-Dana or by an authorized representative, provided that investigation and factory inspection by Racal-Dana discloses that such defect developed under normal and proper use.

The exceptions and conditions mentioned above are the following:

a.) ***Some components and accessories by their nature are not intended to, and will not, function one year. If any such component or accessory manufactured by Racal-Dana and part of the item sold fails to give reasonable service for a reasonable period of time, Racal-Dana will, at its election, replace or repair such component or accessory. What constitutes reasonable service and what constitutes a reasonable period of time shall be determined solely by Racal-Dana after Racal-Dana is in possession of all the facts concerning operating conditions and other pertinent factors and after such component or accessory has been returned to Racal-Dana, transportation prepaid.***

b.) ***All items claimed defective must be returned to Racal-Dana, transportation changes prepaid, and will be returned to the customer with the transportation charges collect unless the item is found to be defective in which case Racal-Dana will pay the return transportation charges.***

c.) ***Racal-Dana makes no warranty concerning components or accessories not manufactured by it. However, in the event of the failure of any component or accessory not manufactured by Racal-Dana, Racal-Dana will give reasonable assistance to the purchaser in obtaining from the respective manufacturer whatever adjustment is reasonable in the light of the manufacture's own warranty.***

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FOR YOUR SAFETY

Before undertaking any troubleshooting, maintenance or exploratory procedure, read carefully the **WARNING** and **CAUTION** notices.

This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.

If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earthed pole) of the power supply.

Before operating the unit. ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adaptor. This will defeat the protective feature of the third conductor in the power cord.

Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid "live" circuit points.

Before operating this instrument:

1. Ensure the instrument is configured to operate on the voltage at the power source. See Installation Section.

2. Ensure the proper fuse is in place for the power source to operate.

3. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

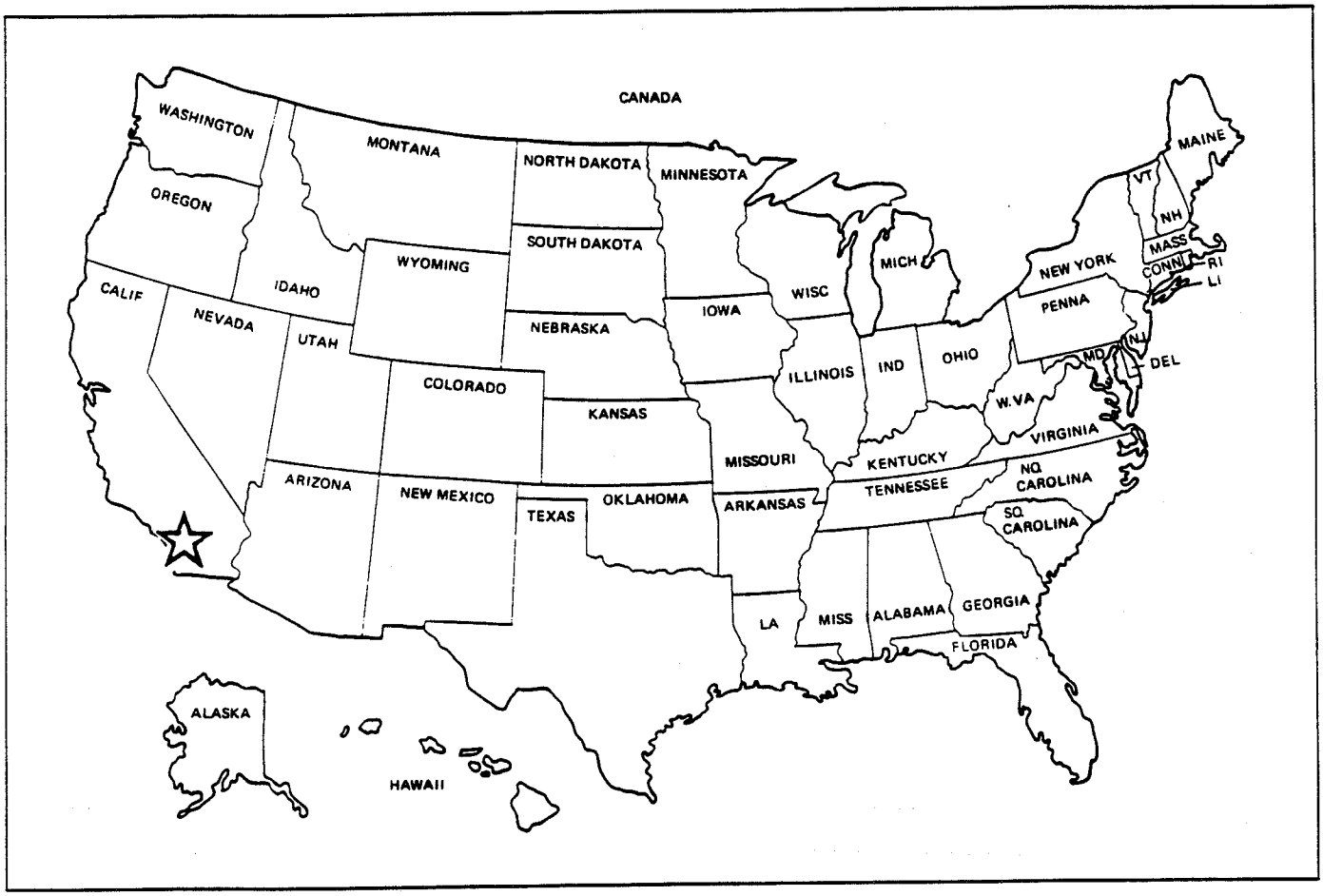
If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until performance is checked by qualified personnel.

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RACAL-DANA Instruments Inc.



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RACAL-DANA Instruments Inc. *4 Goodyear Street, Irvine, California 92718-2202*

REPAIR AND CALIBRATION REQUEST FORM

To allow us to better understand your repair requests, we suggest you use the following outline when calling and include a copy with your instrument to be sent to the Racal-Dana Repair Facility.

Model No_____ Serial No_____ Date_____

Company Name_____ P.O. No_____

Billing Address_____
City State Zip

Shipping Address_____
City State Zip

Technical Contact_____ Phone Number (___)_____

Purchasing Contact_____ Phone Number (___)_____

1. Describe, in detail, the problem and symptoms you are having. Please include all set up details, such as input/output levels, frequencies, waveform details, etc.

_____

_____

_____

_____

2. If problem is occurring when unit is in remote, please list the program strings used and the controller type.

_____

_____

_____

3. Please give any additional information you feel would be beneficial in facilitating a faster repair time (i.e., modifications, etc.).

_____

_____

_____

4. Is calibration data required? Yes No (circle one)

Call for RMA No. <u>before</u> shipping:

Customer Service
(714) 859-8999 x230 OR 1 (800) RAC-DANA

Ship instrument to:

Customer Service Department
Racal-Dana Instruments Inc.
4 Goodyear Street
Irvine, CA 92718

<u>Note</u>: We do not accept "collect" shipments.

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Universal Analog & Digital Input/Output VXIbus Module

Model 6060 & 6061

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SECTION 1

INTRODUCTION

This manual provides the necessary information to install one or more of the Racal-Dana **6060 & 6061A/B/C/D/E** modules in a VXIbus compatible chassis and to operate it correctly.

The **6060** series is a non isolated version of the **6061** series (all analog input/output signals are referenced to system ground, but all digital channels are isolated).

The **6061E** has his own application specific software and specific commands.

The description of the software and the SCPI commands list are given for the **6060 & 6061 A/B/C/D** versions.

The functional description describes only the **6061A** version.

The features and Ordering Information are given in this section.

The section 4 describes operation, check and calibration.

Some technical descriptions will be given to explain the theory of operation of the product in the section 6.

The section 7 is reserved for the Software syntax and command description.

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General Information

The **6060 & 6061** Series Universal Analog/Digital Input/Output modules are a range of C size, VXIbus compatible modules that generate and measure analog or digital signals.

A compact, multi-channel solution, the 6061 provides high isolation between channels for the following conditions:

- when ohmic isolation between signal source and the measuring system is necessary.
- when common-mode noise and voltage rejection requirements are > 80 dB.
- when it is necessary to process signals in the presence of high common-mode voltages.

The 6061 is therefore ideally suited to applications of industrial process control and measurement which require:

- signal measurement in the presence of common-mode noises and voltages.
- breaking ground loops and/or eliminating source ground connections. The 6061 provides full floating input, eliminating the need for connections to ground source, and thus allow ing two-wire hook-up to the signal source.
- isolation protection for electronic instruments/equipment. Large common-mode voltages occasionally cause electronic faults and damage.

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Features
(6061A version)

- 12 Bits Analog Input/Output Resolution
- 8 Isolated Voltage or Current Outputs
- 8 Isolated High Impedance Analog Inputs
- 32 Isolated Digital Inputs/Outputs
- 256 KBytes of data buffer (expandable to 512 KBytes)
- C-size simple width module
- Full VXIbus Revision 1.3 Compatibility
- SCPI Compatibility

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Models

The **6061** series is a isolated version: all analog and digital channels are isolated from channel to channel and from channel to the system ground.

The **6060** series is a non isolated version: all analog channels are referenced to the system ground, but all digital channels are isolated from channel to channel and from channel to the system ground (opto-isolator).

The **6061A** RACAL DANA **VXI** module offers eight isolated analog outputs with 12 bits resolution, eight isolated analog inputs with 12 bits resolution and thirty two isolated digital inputs/outputs.

The **6061B**: sixteen isolated analog outputs and thirty two isolated digital inputs/outputs.

The **6061C**: sixteen isolated analog inputs and thirty two isolated digital inputs/outputs.

The **6061D**: thirty two isolated digital inputs/outputs.

The **6061E** version is a 6061A with specific software and connectors, specially designed to be used in a VXI system to drive 4 power supplies.

The **6060A** RACAL DANA **VXI** module offers eight analog outputs with 12 bits resolution, eight analog inputs with 12 bits resolution and thirty two isolated digital inputs/outputs.

The **6060B**: sixteen analog outputs and thirty two isolated digital inputs/outputs.

The **6060C**: sixteen analog inputs and thirty two isolated digital inputs/outputs.

The **606D**: thirty two digital inputs/outputs.

The 6060 & 6061 family is a message based module compatible with **VXI**bus revision 1.3, and IEEE 488.2 definitions.

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OPTIONS

OPTION	DESCRIPTION
Option 01	Ranges 1.6, 8, 16 Volts instead 1,5,10 Volts (for 6060&6061A/B/C)
Option 02	Digital I/O with TTL compatible level (for 6060&6061A/B/C/D). With this Option, all Digital Input/Output are referenced to the system ground.
Option 03	Current outputs. (for 6060&6061A/B)
Option 04	Additional 256 Kbytes memory: Total 512 Kbytes (for 6060&6061A/B/C/D)

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ORDERING INFORMATION for 6061A Series

PART NUMBER	MODEL	OPTION	Description
33-1010-9999	6060&6061	ALL	Technical Documentation
33-1020-0000	6061A	STANDARD	8 Isolated 10V Analog Outputs 8 Isolated 10V Analog Inputs 16 O.C. Digital Outputs 16 Isolated Digital Inputs
33-1020-1000	6061A	01	8 Isolated 16V Analog Outputs 8 Isolated 16V Analog Inputs 16 O.C. Digital Outputs 16 Isolated Digital Inputs
33-1020-2000	6061A	02	8 Isolated 10V Analog Outputs 8 Isolated 10V Analog Inputs 32 Programmable TTL Digital Inputs/Outputs
33-1020-3000	6061A	03	8 Isolated Current Analog Outputs 8 Isolated 10V Analog Inputs 16 O.C. Digital Outputs 16 Isolated Digital Inputs
33-1020-4000	6061A	04	33-1020-0000 with additionnal 256 KBytes.
33-1020-1200	6061A	01 and 02	8 Isolated 16V Analog Outputs 8 Isolated 16V Analog Inputs 32 Programmable TTL Digital Inputs/Outputs
33-1020-2300	6061A	02 and 03	8 Isolated Current Analog Outputs 8 Isolated 10V Analog Inputs 32 Programmable TTL Digital Inputs/Outputs
33-1020-1400	6061A	01 and 04	33-1020-1000 with additionnal 256 KBytes.
33-1020-2400	6061A	02 and 04	33-1020-2000 with additionnal 256 KBytes.
33-1020-3400	6061A	03 and 04	33-1020-3000 with additionnal 256 KBytes.
33-1020-1240	6061A	01, 02, 04	33-1020-1200 with additionnal 256 KBytes.
33-1020-2340	6061A	02, 03, 04	33-1020-2300 with additionnal 256 KBytes.

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ORDERING INFORMATION for 6061B Series

PART NUMBER	MODEL	OPTION	Description
33-1010-9999	6060&6061	ALL	Technical Documentation
33-1021-0000	6061B	STANDARD	16 Isolated 10V Analog Outputs 16 O.C. Digital Outputs 16 Isolated Digital Inputs
33-1021-1000	6061B	01	16 Isolated 16V Analog Outputs 16 O.C. Digital Outputs 16 Isolated Digital Inputs
33-1021-2000	6061B	02	16 Isolated 10V Analog Outputs 32 Programmable TTL Digital Inputs/Outputs
33-1021-3000	6061B	03	16 Isolated Current Analog Outputs 16 O.C. Digital Outputs 16 Isolated Digital Inputs
33-1021-4000	6061B	04	33-1021-0000 with additionnal 256 KBytes.
33-1021-1200	6061B	01 and 02	16 Isolated 16V Analog Outputs 32 Programmable TTL Digital Inputs/Outputs
33-1021-2300	6061B	02 and 03	8 Isolated Current Analog Outputs 32 Programmable TTL Digital Inputs/Outputs
33-1021-1400	6061B	01 and 04	33-1021-1000 with additionnal 256 KBytes.
33-1021-2400	6061B	02 and 04	33-1021-2000 with additionnal 256 KBytes.
33-1021-3400	6061B	03 and 04	33-1021-3000 with additionnal 256 KBytes.
33-1021-1240	6061B	01, 02, 04	33-1021-1200 with additionnal 256 KBytes.
33-1021-2340	6061B	02, 03, 04	33-1021-2300 with additionnal 256 KBytes.

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ORDERING INFORMATION for 6061C Series

PART NUMBER	MODEL	OPTION	Description
33-1010-9999	6060&6061	ALL	Technical Documentation
33-1022-0000	6061C	STANDARD	16 Isolated 10V Analog Inputs 16 O.C. Digital Outputs 16 Isolated Digital Inputs
33-1022-1000	6061C	01	16 Isolated 16V Analog Inputs 16 O.C. Digital Outputs 16 Isolated Digital Inputs
33-1022-2000	6061C	02	16 Isolated 10V Analog Inputs 32 Programmable TTL Digital Inputs/Outputs
33-1022-4000	6061C	04	33-1022-0000 with additionnal 256 KBytes.
33-1022-1200	6061C	01 and 02	16 Isolated 16V Analog Outputs 32 Programmable TTL Digital Inputs/Outputs
33-1022-1400	6061C	01 and 04	33-1022-1000 with additionnal 256 KBytes.
33-1022-2400	6061C	02 and 04	33-1022-2000 with additionnal 256 KBytes.
33-1022-1240	6061C	01, 02, 04	33-1022-1200 with additionnal 256 KBytes.

ORDERING INFORMATION for 6061E Series

PART NUMBER	MODEL	OPTION	Description
33-1010-9999	6060&6061	ALL	Technical Documentation
33-1024-0000	6061E	STANDARD	8 Isolated 10V Analog Outputs 8 Isolated 50V Analog Inputs 16 O.C. Digital Outputs 16 Isolated Digital Inputs **Specific Software designed to drive Power Supplies.**

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ORDERING INFORMATION for 6060A Series

PART NUMBER	MODEL	OPTION	Description
33-1010-9999	6060&6061	ALL	Technical Documentation
33-1010-0000	6060A	STANDARD	8 10V Analog Outputs 8 10V Analog Inputs 16 O.C. Digital Outputs 16 Isolated Digital Inputs
33-1010-1000	6060A	01	8 16V Analog Outputs 8 16V Analog Inputs 16 O.C. Digital Outputs 16 Isolated Digital Inputs
33-1010-2000	6060A	02	8 10V Analog Outputs 8 10V Analog Inputs 32 Programmable TTL Digital Inputs/Outputs
33-1010-3000	6060A	03	8 Current Analog Outputs 8 10V Analog Inputs 16 O.C. Digital Outputs 16 Isolated Digital Inputs
33-1010-4000	6060A	04	33-1010-0000 with additionnal 256 KBytes.
33-1010-1200	6060A	01 and 02	8 16V Analog Outputs 8 16V Analog Inputs 32 Programmable TTL Digital Inputs/Outputs
33-1010-2300	6060A	02 and 03	8 Current Analog Outputs 8 10V Analog Inputs 32 Programmable TTL Digital Inputs/Outputs
33-1010-1400	6060A	01 and 04	33-1010-1000 with additionnal 256 KBytes.
33-1010-2400	6060A	02 and 04	33-1010-2000 with additionnal 256 KBytes.
33-1010-3400	6060A	03 and 04	33-1010-3000 with additionnal 256 KBytes.
33-1010-1240	6060A	01, 02, 04	33-1010-1200 with additionnal 256 KBytes.
33-1010-2340	6060A	02, 03, 04	33-1010-2300 with additionnal 256 KBytes.

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ORDERING INFORMATION for 6060B Series

PART NUMBER	MODEL	OPTION	Description
33-1010-9999	6060&6061	ALL	Technical Documentation
33-1011-0000	6060B	STANDARD	16 10V Analog Outputs 16 O.C. Digital Outputs 16 Isolated Digital Inputs
33-1011-1000	6060B	01	16 16V Analog Outputs 16 O.C. Digital Outputs 16 Isolated Digital Inputs
33-1011-2000	6060B	02	16 10V Analog Outputs 32 Programmable TTL Digital Inputs/Outputs
33-1011-3000	6060B	03	16 Current Analog Outputs 16 O.C. Digital Outputs 16 Isolated Digital Inputs
33-1011-4000	6060B	04	33-1011-0000 with additionnal 256 KBytes.
33-1011-1200	6060B	01 and 02	16 16V Analog Outputs 32 Programmable TTL Digital Inputs/Outputs
33-1011-2300	6060B	02 and 03	16 Current Analog Outputs 32 Programmable TTL Digital Inputs/Outputs
33-1011-1400	6060B	01 and 04	33-1011-1000 with additionnal 256 KBytes.
33-1011-2400	6060B	02 and 04	33-1011-2000 with additionnal 256 KBytes.
33-1011-3400	6060B	03 and 04	33-1011-3000 with additionnal 256 KBytes.
33-1011-1240	6060B	01, 02, 04	33-1011-1200 with additionnal 256 KBytes.
33-1011-2340	6060B	02, 03, 04	33-1011-2300 with additionnal 256 KBytes.

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ORDERING INFORMATION for 6060C Series

PART NUMBER	MODEL	OPTION	Description
33-1010-9999	6060&6061	ALL	Technical Documentation
33-1012-0000	6060C	STANDARD	16 10V Analog Inputs 16 O.C. Digital Outputs 16 Isolated Digital Inputs
33-1012-1000	6060C	01	16 16V Analog Inputs 16 O.C. Digital Outputs 16 Isolated Digital Inputs
33-1012-2000	6060C	02	16 10V Analog Inputs 32 Programmable TTL Digital Inputs/Outputs
33-1012-4000	6060C	04	33-1012-0000 with additionnal 256 KBytes.
33-1012-1200	6060C	01 and 02	16 16V Analog Inputs 32 Programmable TTL Digital Inputs/Outputs
33-1012-1400	6060C	01 and 04	33-1012-1000 with additionnal 256 KBytes.
33-1012-2400	6060C	02 and 04	33-1012-2000 with additionnal 256 KBytes.
33-1012-1240	6060C	01, 02, 04	33-1012-1200 with additionnal 256 KBytes.

ORDERING INFORMATION for 6060D Series

PART NUMBER	MODEL	OPTION	Description
33-1010-9999	6060&6061	ALL	Technical Documentation
33-1013-0000	6060D	STANDARD	16 O.C. Digital Outputs 16 Isolated Digital Inputs
33-1013-2000	6060D	02	32 Programmable TTL Digital Inputs/Outputs
33-1013-4000	6060D	04	33-1013-0000 with additionnal 256 KBytes.
33-1013-2400	6060D	02 and 04	33-1013-2000 with additionnal 256 KBytes.

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SECTION 2
SPECIFICATIONS

This section contains specifications of:

- VXIbus Interface
- Common Specifications
- Analog Outputs:
  - 10V, Voltage version (Standard)
  - 16V, Voltage version (Option 01)
  - Current version (Option 03)
- Analog Inputs:
  - 10V, Voltage version (Standard)
  - 16V, Voltage version (Option 01)
  - 50V, Voltage version (6061E)
- Digital Inputs/Outputs:
  - Open Collector (Standard)
  - TTL (Option 02)

DEFINITIONS:

The 6061 contains 20 logical groups:
- 16 analog channels, 2 bytes per channel (12 bits effective).
- 4 digital ports, 1 byte per port. Each port is a group of 8 bits. Each digital input or output bit is called a digital channel.

A standard version of 6061 contains 48 isolated channels:
- 16 analog channels.
- 32 digital channels.

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SPECIFICATIONS

VXIbus Interface

Manufacturer ID:	**4091 (0FFB hex.): RACAL-DANA**
6061A Model :	**1020**
6061B Model :	**1021**
6061C Model :	**1022**
6061D Model :	**1023**
6061E Model :	**1024**
6060A Model :	**1010**
6060B Model :	**1011**
6060C Model :	**1012**
6060D Model :	**1013**
Logical Addressing:	**Dynamic or Static (1 to 254)**
Address Space:	**A16**
Device Class:	**Message Based Slave Device**
Interrupt Levels:	**Programmable**
TTL Trigger line:	**Programmable**

WORD SERIAL PROTOCOL SUPPORTED

Byte Available
Byte Request
Write to logical address register
Asynchronous Mode Control
Begin Normal Operations Top
Control Response
Read Interrupter Line
Trigger

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COMMON SPECIFICATIONS (ALL VERSIONS)

Execution time in Interactive mode:	**< 10 mS per logical group .**
"Trace" Memory Size:	**256 KBytes (512 KBytes with Option 04)**
"Trace" commands:	**DEFine, CATalog, FREE, COPY, DELete, NAME**
Trigger source:	**Bus (GET), 1 of 8 TTL Triggers (VXIbus) or Timer.**
Trigger sequences for "Trace":	**START, STOP and STEP.**
Trigger modes:	**IMMediate, ECOunt, COUNt.**
Timer period:	**from 1 to 17 millions units(2E24-1), 1 unit is 8 µS. (maximum period # 2.2 minutes)**
Trace scanning rate:	**- about 130 µS + 30 µS per digital Input/Output or Analog Output logical group. - about 150 µS + 35 µS per Analog Input logical group.**
Self-Test coverage:	**65 % at 25 °C**
MTBF:	**56 000 hours at 25 °C, 44 000 hours at 35 °C**
User Connectors:	**Two 78 pins high density sub D, RADIALL HZ78POJ**
Cooling (airflow backpressure):	**4.0 l/s, 0.5 mm H_2O.**
Operating Temperature:	**10 °C to 50 °C.**
Power Requirements:	
5 Vdc	**from 4.75 to 5.25 Vdc 2.5 A typical, 4 A peak internal protection by 3A temporized fuse**
+24 Vdc	**from +22 Vdc to +26 Vdc 1 A typical, 3 A peak internal protection by 2.5 A temporized fuse**
-24 Vdc	**from −22 Vdc to −26 Vdc 0.1 A typical, 0.5 A peak internal protection by 1 A temporized fuse**
Weight:	**about 2.5 kg (5.5 lbs)**

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Timing Trigger Delay :

The basic timing trigger delay for 1 channel used is 400μs.

The additional delay for the number of channel is 50μs per additional channel.

The additional delay for the number position of the channel is 70μs per additional channel.

For example, the timing trigger delay for the channel number 8 used in a twelve channels configuration is:

400μs + (50μs x (12-1)) + (70μs x (8-1)) = 1440μs

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SPECIFICATIONS - Analog Outputs

10 V Voltage Outputs

(Standard for 6060A, 6060B, 6061A, 6061B)

Number of isolated channels	6060Aor 6061A: 8, 6060B or 6061B: 16
Resolution	12 bits
Voltage Range	1V, 5V, 10V, ±1V, ±5V, ±10V
Nonlinearity	0.1 % FSR
Offset & Gain Accuracy (23°C ± 5°C)	0.1 % FSR + 0.3 mV
Temperature coefficient	(0.01 % FSR + 0.1 mV) / °C typical, (0.02 % FSR + 0.2 mV) / °C max.
Settling time	50 µS to 1%, 100 µS to 0.1%
Signal Bandwidth	30 KHz
Slew Rate	> 0.1 V / µS
Ripple Voltage (20 Hz to 20 MHz)	range 1V or ±1V : 2 mV rms, 5 mV pp other ranges: 3 mV rms, 10 mV pp
Isolation Voltage	750 V rms (50/60 Hz)
DC Rejection	100 dB
AC Rejection (50/60 Hz)	80 dB
Isolation Resistance (DC)	> 100 MΩ
Leakage current (240 Vrms, 50/60 Hz)	< 10 µA rms
Output Resistance	< 2 Ω
Max Output Current	20 mA at ±10V per channel (at 35°C)

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SPECIFICATIONS - Analog Outputs

10 V Voltage Outputs (6061E)

Number of isolated channels	8
Resolution	12 bits
Voltage Range	0 to10V
Nonlinearity	0.1 % FSR
Offset & Gain Accuracy (23°C ± 5°C)	0.1 % FSR + 0.3 mV
Temperature coefficient	(0.01 % FSR + 0.1 mV) / °C typical, (0.02 % FSR + 0.2 mV) / °C max.
Settling time	50 µS to 1%, 100 µS to 0.1%
Signal Bandwidth	30 KHz
Slew Rate	> 0.1 V / µS
Ripple Voltage (20 Hz to 20 MHz)	3 mV rms, 10 mV pp
Isolation Voltage	750 V rms (50/60 Hz)
DC Rejection	100 dB
AC Rejection (50/60 Hz)	80 dB
Isolation Resistance (DC)	> 100 MΩ
Leakage current (240 Vrms, 50/60 Hz)	< 10 µA rms
Output Resistance	< 2 Ω
Max Output Current	20 mA at ±10V per channel (at 35°C)

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16 V Voltage Outputs

(Option 01 for 6060A, 6060B, 6061A and 6061B)

The Option 01 is available for 6060 & 6061 A/B. In standard version, the analog input / output ranges are: 0-1V, ±1V, 0-5V, ±5V, 0-10V, ±10V. With Option 01, the analog input / output ranges are: 0-1.6V, ±1.6V, 0-8V, ±8V, 0-16V, ±16V.

Number of isolated channels	6060A or 6061A: 8, 6060B or 6061B: 16
Resolution	12 bits
Voltage Range	1.6V, 8V, 16V, ±1.6V, ±8V, ±16V
Nonlinearity	0.1 % FSR
Offset & Gain Accuracy (23°C ± 5°C)	0.1 % FSR + 0.5 mV
Temperature coefficient	(0.015 % FSR + 0.15 mV) / °C typical, (0.030 % FSR + 0.3 mV) / °C max.
Settling time	80 µS to 1%, 150 µS to 0.1%
Signal Bandwidth	30 KHz
Slew Rate	> 0.1 V / µS
Ripple Voltage (20 Hz to 20 MHz)	range 1.6V or ±1.6V : 3 mV rms, 10 mV pp other ranges: 5 mV rms, 20 mV pp
Isolation Voltage	750 V rms (50/60 Hz)
DC Rejection	100 dB
AC Rejection (50/60 Hz)	80 dB
Isolation Resistance (DC)	> 100 MΩ
Leakage current (240 Vrms, 50/60 Hz)	< 10 mA rms
Output Resistance	< 2 Ω
Max Output Current	15 mA at ±16V per channel (at 35°C)

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Current Outputs

(Option 03 for 6060A, 6060B, 6061A and 6061B)

Number of isolated channels	6060A or 6061A: 8, 6060B or 6061B: 16
Resolution	12 bits
Current Range	0-2mA, 0-10mA, 0-20mA.
Nonlinearity	0.1 % FSR
Offset & Gain Accuracy (23° C ± 5° C)	0.2 % FSR + 2 μA
Temperature coefficient	(0.02 % FSR + 0.2 μA) / ° C typical, (0.04 % FSR + 0.4 μA) / ° C max.
Settling time	50 μS to 1%,100 μS to 0.1%
Signal Bandwidth	30 KHz
Slew Rate	> 0.1 mA/μS (range 0-20mA)
Ripple current (20 Hz to 20 MHz)	range 0-2mA: 10 μA rms, 50 μA pp other ranges: 20 μA rms, 100 μA pp
Isolation Voltage	750 V rms (50/60 Hz)
DC Rejection	100dB
AC Rejection (50/60 Hz)	80 dB
Isolation Resistance (DC)	> 100 MΩ
Leakage current (240 Vrms, 50/60Hz)	< 10 μA rms
Output Resistance	> 50 KΩ
Maximum load	300 Ω

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10 V Analog Inputs

(Standard for 6060A, 6060C, 6061A and 6061C)

Number of isolated channels	6060 or 6061A : 8, 6061C or 6061C: 16
Resolution	12 bits
Ranges	1V, 5V, 10V, ±1V, ±5V, ±10V
Nonlinearity	0.03 % FSR (range ±10V, 10V) 0.05 % FSR (range ±1V, 1V, ±5V, 5V)
Offset & Gain Accuracy (23° C ± 5° C)	0.1 % FSR (range ±10V) 0.15 % FSR (other ranges)
Temperature coefficient	(0.01 % FSR + 0.2 mV) / °C typical, (0.02 % FSR + 0.5 mV) / °C max.
Digitalization Noise	0.05 % FSR + 5 mV
Input Impedance (DC)	about 1 MΩ // 1nF
Overvoltage Protection	250V rms (50/60 Hz)
Small signal Bandwidth	> 10 KHz
Slew Rate	> 0.1 V / μS
Isolation Voltage	750 V rms (50/60 Hz)
DC Rejection	100 dB
AC Rejection (50/60 Hz)	70 dB
Isolation Resistance	> 100 MΩ
Leakage current (240 Vrms, 50/60 Hz)	10 μA rms

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16 V Analog Inputs
(Option 01 for 6060A, 6060C, 6061A and 6061C)

The Option 01 is available for 6060 & 6061 A/B. In standard version, the analog input / output ranges are: 0-1V, ±1V, 0-5V, ±5V, 0-10V, ±10V. With Option 01, the analog input / output ranges are: 0-1.6V, ±1.6V, 0-8V, ±8V, 0-16V, ±16V.

Number of isolated channels	6060 or 6061A : 8, 6061C or 6061C: 16
Resolution	12 bits
Ranges	1.6V, 8V, 16V, ±1.6V, ±8V, ±16V
Nonlinearity	0.03 % FSR (range ±16V, 16V) 0.05 % FSR (range ±1.6V, 1.6V, ±8V, 8V)
Offset & Gain Accuracy (23°C ± 5°C)	0.1 % FSR (range ±16V) 0.15 % FSR (other ranges)
Temperature coefficient	(0.015 % FSR + 0.3 mV) / °C typical, (0.03 % FSR + 1 mV) / °C max.
Digitalization Noise	0.05 % FSR + 8 mV
Input Impedance (DC)	about 1 MΩ // 1nF
Overvoltage Protection	250V rms (50/60 Hz)
Small signal Bandwidth	> 10 KHz
Slew Rate	> 0.1 V / μS
Isolation Voltage	750 V rms (50/60 Hz)
DC Rejection	100 dB
AC Rejection (50/60 Hz)	70 dB
Isolation Resistance	> 100 MΩ
Leakage current (240 Vrms, 50/60 Hz)	10 μA rms

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50 V Analog Inputs (6061E)

Number of isolated channels	8
Resolution	12 bits
Ranges	0 to + 50 V
Nonlinearity	0.05 % FSR
Offset & Gain Accuracy (23°C ± 5°C)	0.3 % FSR
Temperature coefficient	0.015 % FSR / °C typical, 0.03 % FSR / °C max.
Digitalization Noise	50 mV
Input Impedance (DC)	about 1 MΩ // 1nF
Overvoltage Protection	250V rms (50/60 Hz)
Small signal Bandwidth	> 10 KHz
Slew Rate	> 1 V / μS
Isolation Voltage	750 V rms (50/60 Hz)
DC Rejection	100 dB
AC Rejection (50/60 Hz)	70 dB
Isolation Resistance	> 100 MΩ
Leakage current (240 Vrms, 50/60 Hz)	10 μA rms

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Open Collector-Optoisolator Digital Inputs/Outputs (Standard for 6060 & 6061 A/B/C/D/E)

16 inputs and 16 outputs channels protected from polarity inversion, isolated by opto-couplers between channels and from channels to ground (isolation voltage = 750 Vrms, 50/60 Hz). Organization: 4 ports of 8 channels. Data buffer: 0 to 256 KWords of 8 bits.

Output : (Open Collector)

I sink max. = 50 mA
Vhl low (at I sink= 50 mA) ≤ 1.3 V
Vhl max. = 35 V
Vhl min. = 3 V
Slew Rate > 0.5 V/μs

Input : (Current Receiver)

Vhl high min. = 3 V
Vhl high max. = 35 V
Input current = auto regulated to 5 mA approximately (Vhl from 3V to 24V)
Vhl low max. = 2 V

TTL level compatible Digital Inputs/Outputs (Option 02 for 6060 & 6061 A/B/C/D/E)

32 programmable input/output channels referenced to system ground. Each channel can be programmed as input or output. Organization: 4 ports of 8 channels. Data buffer: 0 to 256 KWords of 8 bits.

Output :

Vout low < 0.6 V (I ol = + 5 mA)
Vout high > 2.4 V with I oh = - 50 μA, typical 4V no charge.
Maximum current low level: + 20 mA, high level: - 0.1 mA,
Output drive 10 ALS TTL loads
Transition Time < 50 ns (external 300 Ω pull-up to 5V // 50 pF)

Input : (type 74ALS563)

Vin max. = 5.5 V
Vin high > 2 V
Vin low < 0.8 V
High level input current < 20 μA (Vih = 2.7V)
Low level input current > - 0.1 mA (Vil = 0.4V)

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SECTION 3
INSTALLATION

This section describes the start-up phase before operating the 6060 & 6061 module:

- Unpacking and Inspection
- Reshipment Instructions
- Set up the logical address (dynamic and static configuration)
- Interrupt setting
- Power up
- Self-test.

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Unpacking and Inspection

Before unpacking the 6060 & 6061 module, check the exterior of the shipping box for any signs of damage. All irregularities should be noted on the shipping bill. Remove the instrument from its box, preserving the factory packaging as much as possible. Inspect the 6060 & 6061 module for any defect or damage. Notify the carrier immediately if any damage is apparent. Notify RACAL-DANA if the module appears damaged in any way. Do not attempt to install a damaged module into a VXI chassis.
Have a qualified person check the instrument for safety before use.

The 6061 module is shipped in a anti-static bag to prevent electrostatic damage to the module. Do not remove module from the anti-static bag unless in a static controlled area.

Reshipment Instructions

Use the original packing if it is necessary to return the 6060 & 6061 module to RACAL-DANA for calibration or servicing. The original shipping box and the instruments plastic foam will provide the necessary support for safe reshipment. If the original packing is unavailable, wrap the 6061 module in anti-static bag and use plastic spray foam to surround and protect the instrument. Reship in either the original or a new, sturdy shipping box.

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ADDRESS SWITCH SETTING

The 6060 & 6061 Series universal Analog/Digital Input/Output modules are installed in a C size VXIbus compatible chassis in any chassis slot (the leftmost slot is reserved for the controller).

One free address is required in the use of a 6060 & 6061 Series module. The logical address is set by a DIP switch on the 6060 &6061.

The 6060 & 6061 has an internal 8-position address switch, used to determine dynamic or static configuration. It is located on the top of the module accessible through the case. Any setting other than 255 indicates static configuration.

Dynamic configuration is an alternative method of assigning Logical Address to VXIbus devices and is defined in section F of the VXIbus System Specification Revision 1.3.

The user can select any logical address from 1 to 254 for static configuration.

Logical address 0 is not allowed.

In the ON position the switch is set to the logical 1 and in the OFF position to the logical 0.

The switch 1 is the LSB, the switch 8 is the MSB.

VXIbus INTERRUPT HANDLER SETTING

One programmable interrupt line is provided on the 6061 module. This line is assigned by using the *assign interrupter* word serial protocol command (see page 183 in Rev 1.3 of the VXIbus specs). The *Int_ID* is set to 1.

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6060 & 6061 to VXIbus MAINFRAME INSTALLATION

To install the 6060 & 6061 in a C size VXI chassis, ensure power is not applied. Configurate the interrupt daisy chain on the backplane to bypass empty slots (VXIbus specs). Remove the front cover of the VXI chassis and slide the 6060 & 6061 into appropriate slot with the LED's towards the top (or to the left in case of a horizontal chassis).

POWER UP INITIALIZATION

Before turning on the VXIbus mainframe, make sure that a slot 0 with resource manager is present.

Upon power up of the system, the following sequence takes place:

- Board ID check.
- VXIbus Interface Initialization
- Power up Self-Test: Tests are performed on ROM, RAM, Non volatile Memory and the Timer to make sure that the logic components are operating correctly.
- Disable TTLTRG trigger functions.
- Analog and Digital output Initialization.

SELF-TEST

The Self-Test is called up by a TEST command. Tests are performed on ADC, DAC, I/O Ports .

The Self-Test is performed in less than five seconds. It does not use external instrumentation or additional wiring.

During the Self-Test, all output channels are in indefinite states. After the Self-Test, all analog ouputs are initialized to 0 V and all digital outputs are initialized to "inactive" state (Open Collector - standard version: Output Transistor in high impedance, TTL version: low level).

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SECTION 4

OPERATION
CHECK and CALIBRATION

This Section supplies the information necessary to operate, check and calibrate the 6060 & 6061 Series Universal Analog & Digital Input & Output models.

The Section 6 describes the theory of operation.

The Section 7 gives the complete set of SCPI syntax commands.

Section 8 and Section 9 contain schematics and drawings.

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CONNECTORS:

There are 2 connectors on the front panel of a 6060 & 6061 module. Each one has 78 pins (type **high density sub D, RADIALL HZ78POJ)**

K1 : Analog Connector.

This connector corresponds to 2 internal Analog sub assemblies of the 6060 & 6061 called ANALOG1 and ANALOG2. Each Analog sub assembly defines the function of 8 analog channels.

- In the 6060 & 6061 A standard version, ANALOG1 is an 8 OUTPUTS module and ANALOG2 is an 8 INPUTS module.
- In the 6060 & 6061 B version, ANALOG1 and ANALOG2 are 8 OUTPUTS modules.
- In the 6060 & 6061 C version, ANALOG1 and ANALOG2 are 8 INPUTS modules.
- In the 6060 & 6061 D version, ANALOG1 and ANALOG2 are not equipped.

K2 : Digital Connector.

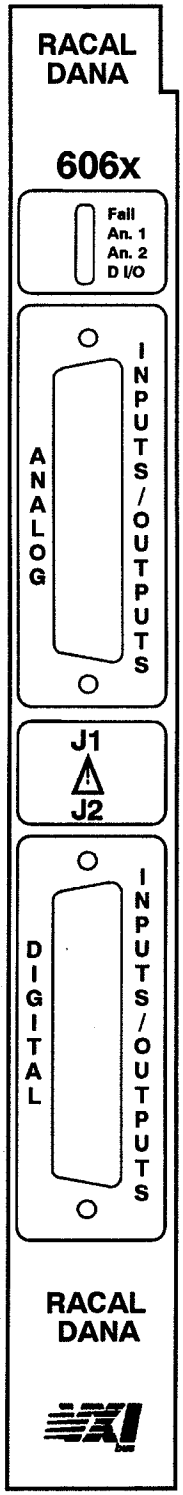
This connector corresponds to the Digital sub assembly of the 6060 & 6061 that contains 32 digital channels.

Normally the input state is read " on the fly". (Data on the input lines are read when the port is read from the VXI bus).
A HOLD auxiliary input gives the user the possibility to freeze input data with a clock signal. (At a later time, the input state can be read from the VXI bus).

In the 6060 & 6061 A, B, C, D version, isolated channels 1 to 16 are open collector outputs, and isolated channels 17 to 32 are inputs. An **isolated 5 VDC (50 mA max.)** is given on the K2 connector to the external application.

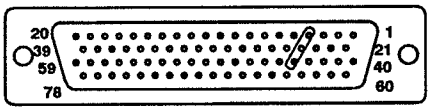
With a "TTL level Digital I/O" Option 02, each channel can be configured by the application software as input or output. All inputs/outputs are referenced to system ground. An **auxiliary 5 VDC (50 mA max.)** is given on the K2 connector to the external application.

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K1

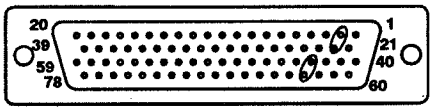


VERSION	ANALOG 1	ANALOG 2
6061A	Outputs 1 to 8	Inputs 1 to 8
6061B	Outputs 1 to 8	Outputs 1 to 8
6061C	Inputs 1 to 8	Inputs 1 to 8
6061D	Not used	Not used

ANALOG 1 group			ANALOG 2 group	
V1L	1		V9L	11
V1H	21		V9H	31
V1L	41		V9L	51
V2L	2		V10L	12
V2H	22		V10H	32
V2L	42		V10L	52
V3L	3		V11L	13
V3H	23		V11H	33
V3L	43		V11L	53
V4L	4		V12L	14
V4H	24		V12H	34
V4L	44		V12L	54
V5L	5		V13L	15
V5H	25		V13H	35
V5L	45		V13L	55
V6L	6		V14L	16
V6H	26		V14H	36
V6L	46		V14L	56
V7L	7		V15L	17
V7H	27		V15H	37
V7L	47		V15L	57
V8L	8		V16L	18
V8H	28		V16H	38
V8L	48		V16L	58

System ground: : 9, 10, 19, 20, 29, 30, 39, 40, 49, 50, 59, 60 to 78

K2



Notes:

- Standard (isolated) :
Channels 1 to 16: Outputs, Channels 17 to 32: Inputs.

- TTL option (Option 02) :
Each channel is programmable as Output or Input. All signals and auxiliary 5V output are referenced to system ground (VxL and GNDiso connected to SYSTEM GROUND).

DIGITAL INPUTS / OUTPUTS							
V1H	1	V9H	9	V17H	17	V25H	45
V1L	21	V9L	29	V17L	37	V25L	65
V2H	2	V10H	10	V18H	18	V26H	46
V2L	22	V10L	30	V18L	38	V26L	66
V3H	3	V11H	11	V19H	19	V27H	47
V3L	23	V11L	31	V19L	39	V27L	67
V4H	4	V12H	12	V20H	40	V28H	48
V4L	24	V12L	32	V20L	60	V28L	68
V5H	5	V13H	13	V21H	41	V29H	49
V5L	25	V13L	33	V21L	61	V29L	69
V6H	6	V14H	14	V22H	42	V30H	50
V6L	26	V14L	34	V22L	62	V30L	70
V7H	7	V15H	15	V23H	43	V31H	51
V7L	27	V15L	35	V23L	63	V31L	71
V8H	8	V16H	16	V24H	44	V32H	52
V8L	28	V16L	36	V24L	64	V32L	72
				+5Viso	56	GNDiso	76
HOLDH	54	HOLDL	74	+5Viso	57	GNDiso	77

System ground:: 20,59,73,75,78
ETRG1 (External Trigger Input): 55
ETRG2 (External Trigger Input): 53
TRGOUT (TTL Trigger Output): 58

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Check & Calibration Procedures :

4.1 / The motherboard (MB)

4.2 / DC/DC Converter module

4.3 / (ANO) Analog Output module

4.4 / (ANI) Analog Input module

4.5 / (DIO) Digital Inputs/Outputs module

ANNEX: Programs

A.1 / CALANO.BAS

A.2 / CONTRANO.BAS

A.3 / ANI.BAS

A.4 / ANI_6061E.BAS

A.5 / DIO.BAS

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4.1 CALIBRATION PROCEDURE ON THE MOTHERBOARD

Test equipment required :

- DC voltmeter, resolution 0.1 mV, range 20V (RACAL-DANA 4006 or 4009).

Procedure:

1) - Power up the motherboard during 5 minutes before starting calibration.

2) - Calibration must be done under normal cooling conditions of the module : that is to say calibrating the module inside the VXI chassis.

3) - Check that +15V is on pin 3 of U1, as well as -15V on pin 3 of U2, ground being connected on pin 2 of U1. Indicated values must be exactly at ±5% (±0,75V).

4) - Measure voltage between A17 and A18 (+ on A17), P1 potentiometer enables to ajust this voltage to 10V ± 1mV.

5) - Check supply voltages on the board between the ground (taken from CAV3 for example) and the concerned fuse. Measured values must be those indicated ±10%.

F1 : +12V
F3 : +24V
F4 : -24V
F5 : +5V

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4.2 DC/DC CONVERTER CHECK PROCEDURE

Introduction:

DC/DC converter receives 24 VDC and provides18 outputs ± 18V or ± 15V (according to the version). Outputs are isolated from one to another, to the input and to the system ground.

Test equipment required :

- Laboratory supply 24 VDC, 4 A.
- 2 resistors 300 Ω, 2 resistors 360 Ω,1W power.
- DC voltmeter, resolution 0.1mV on range 20V (RACAL-DANA 4006 or 4009).
- Multimeter on ohmmeter, 20 MΩ range.

Check procedure :

1) - The DC/DC converter being powered off, Gather : 3 points (+, -, 0) out of the 18 outputs groups, an d 2 input points24V. Check that these 19 groups and the ground are completely isolated from one to another. Isolating resistance must be greater than10 MΩ.

2) - Supply converter to 24 VDC ± 0.2 V, set up current limit to 4A.

3) - CASE "15V"
For each of the 18 outputs, check positive voltage and negative voltage unloaded and loaded by 300 Ω resistors (50 mA output current).
Voltages must be comprised between 14.4 V and15.6 V.

4) - CASE "18V"
For each of the 18 outputs, check positive voltage and negative voltage unloaded and loaded by 360 Ω resistors (50 mA output current).
Voltages must be comprised between 17.28 V and18.72 V.

5) - If only one of the channels is out of the indicated values, the converter is considered as defective.

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4.3 ANALOG OUTPUTS CALIBRATION PROCEDURE

Introduction:

The analog Output board contains 8 DAC of 12 bits and 8 isolated amplifiers. Each output has 2 set up potentiometers and 3 compensation resistances in the range. Each channel calibration guarantees accuracy on 1V, 5V, 10V, ±1V, ±5V, ±10V ranges.

Test equipment required :

- DC voltmeter, resolution 0.1 mV, on range 20V (RACAL-DANA 4006 or4009).
- A 6061A or 6060A, A VXI chassis, a Slot 0 connected to a IEEE-488 bus PC or a built-in PC.
- You can directly send SCPI commands from a keyboard or use the analog outputs calibration software (ANO.BAS , CONTRANO.BAS) which lists are given in annex : ANO.BAS in annex A.1, CONTRANO.BAS in annex A.2.

Test procedure :

1) - Power up the 6061 during 5 minutes before starting calibration.

2) - Calibration must be done under normal cooling conditions of the module : that is to say calibrating the module inside the VXI chassis.

3) - Follow indications of the ANO.BAS program for the 8 channels calibration. For channel number x (x = 1 to 8) :

POT x1 > Adjust unipolar and bipolar range gain.
POT x2 > Adjust general offset.

RE x1 > Balance between unipolar and bipolar ranges.
RE x2 > Adjust on 5V range gain.
RE x3 > Adjust -10V on ±10V range.

4) - Restart ajustment until right value.

5) - Control the board with the CONTRANO.BAS program.

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4.4 ANALOG INPUTS CALIBRATION PROCEDURE

Introduction:

The analog Inputs board contains 8 isolated amplifiers, one multiplexer and 1 ADC of 12 bits
Each channel calibration insures accuracy on 1V, 5V, 10V, ±1V, ±5V, ±10V ranges.

Test equipment required :

- DC voltmeter, resolution 0.1mV, range 20V (RACAL-DANA 4009 or 4006).
- Voltage calibrator 0 to ± 10V accuracy 0.01 % (FLUKE 5100B or EXACT 334)
- A 6061A or 6060A, a VXI chassis, a Slot 0 connected to a PC by IEEE-488 bus or built-in PC.
- You can directly send SCPI commands from a keyboard or use the analog inputs calibration software ANI.BAS which lists are given in annex A.3. For the 6061E, we use the ANI_6061E.BAS program in annex A.4.

Test procedure :

1) - Power up the 6061 during 5 minutes before starting calibration.
2) - Calibration must be done under normal cooling conditions of the module : that is to say calibrating the module inside the VXI chassis.
3) - Adjust voltage reference on the motherboard to +10,000V. (Measurement on A16 and A17 points of J200 or J300, adjustment by POT1 on motherboard).
4) - Configure the analog input board on ±10V.
5) - Short circuit all the input channels
6) - Short circuit C35 (close to U10).
7) - Adjust POT11 in order to read 0V ±5mV on the board. Suppress short circuit.
8) - Adjust POT1 to POT8 to read 0V ±5mV on all channels.
9) - Inject 1 a 9,500V voltage on channel 1.
10) - The resistance values RY1 to RY8 to install on the board (on the soldered side), are displayed on the screen.
11) - If RY values are inferior to15kΩ, adjust POT10 to modify the ADC gain.
12) - Note the average values for each channel.
13) - Remove the board from its socket, then solder RY1 to RY8 resistance to their respective place.
14) - Swith to 0-10V range, apply 9,950V to channel 1 input.
15) - Adjust POT9 to have the ADC indicate 9,950V ±5mV
16) - Switch to 0-5V ±5V 0-1V ±1V ranges.
17) - Apply respectively 2,500V 0V 0,500V 0V
You must read value to ±5mV ±5mV ±2mV ±3mV
18) - On the ±10V range, control linearity by 1V step.
19) - Leave inputs non connected, then verify that each channel reads 0V ± 5mV on each range.

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4.5 DIGITAL INPUT/OUTPUT BOARD CHECK PROCEDURE

Introduction:

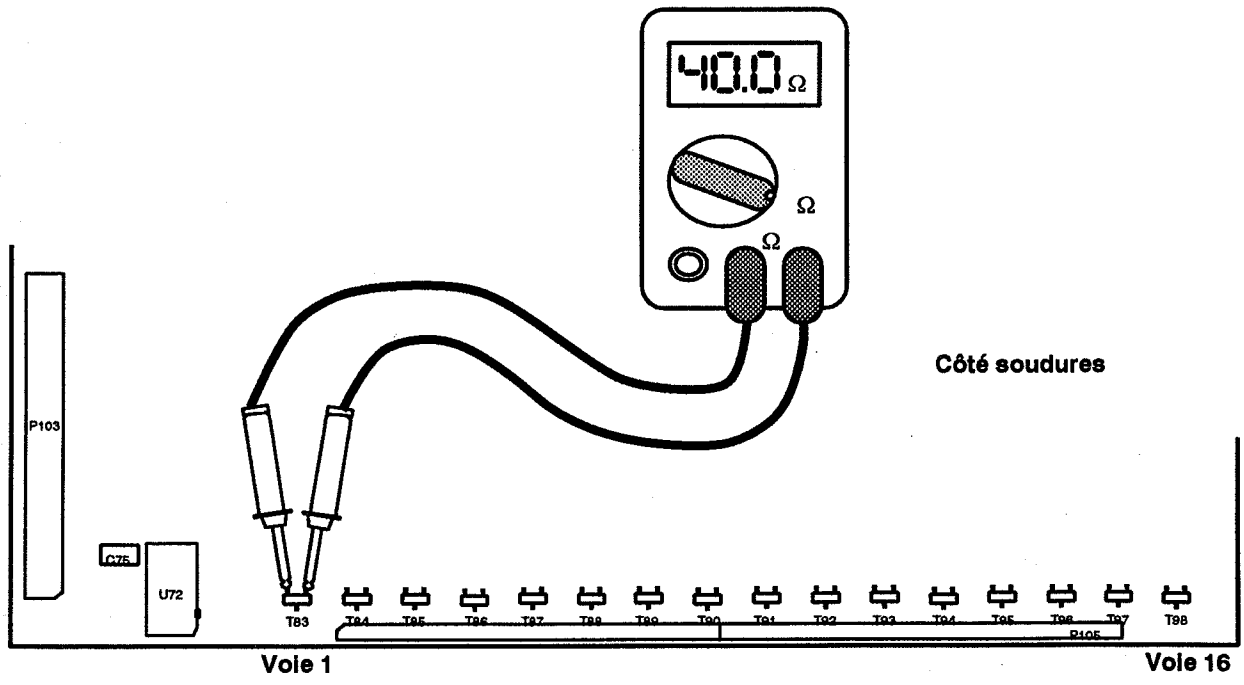
The digital Input/Output board contains 16 open collector outputs, isolated by Optocouplers and 16 isolated inputs by Optocouplers. Each input channel is powered from a 5 VDC, the consumption is about 5 mA. Each output channel can be powered towards 5 VDC by a 33O Ω resistance in series with a LED.

Test equipment required :

- Portable DVM (Fluke 23 or equivalent)
- Universal test box (Made by RACAL-DANA) or a 5 VDC power supply and LED+33O Ω.
- A 6061A or 6060A, a VXI chassis, a Slot 0 connected to a PC by IEEE-488 bus or built-in PC.
- You can directly send SCPI commands from a keyboard or use the software DIO.BAS which lists are given in annex A.5.

Check procedure :

- Connect the Universal box to the 6061
- Power up the VXI chassis
- Use the test software
- All the LED of the test box must lit up, except those correspond to the position of the digital input switch.
- If the switch "HOLD" is "ON", it does not interfere on the LED.
- If one (or several) LED never switches off, it can be a FET input transistor which value "Rds on" is too far from its nominal value. Then it is necessary to take the ohmic value in static measurement (unplugged board from its socket). This value must be 40Ω ±10Ω. Otherwise, replace the FET transistor which corresponds to the broken channel.



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Annexe A.1 CALANO.BAS

```
DEFINT A-Z
DECLARE SUB attend (n)

'       ********************************************************************
'       *                                                                  *
'       *               Programme de TEST 6060 & 6061                      *
'       *               Langage :       QuickBasic 4.0                     *
'       *               IBM PC + Interface IEEE-488 INES                   *
'       *               Version : 2.0   Création     : 8/8/1991            *
'       *                               modification : 25/1/93             *
'       *                                                                  *
'       ********************************************************************

adr$ = "736"     ' Adresse absolue de carte INES à 2E0H / PC-IBM
ap$ = "701+3"      ' 700 + adresse IEEE de l_instrument  P101

'       ------------------------------------------------------------------

'        MAIN PROGRAM

'       ------------------------------------------------------------------

CLS
p5$ = SPACE$(100)
compt% = 0

'====================================================================
rel:
SCREEN 9
LOCATE 10, 5
PRINT "CALIBRATION 6060/6061-Avec ou Sans Option 01 (16V)"
PRINT
LOCATE 15, 5: INPUT "OPTION 16V ? (O/N) ", a$
zz$ = UCASE$(a$)
IF zz$ <> "O" AND zz$ <> "N" THEN GOTO rel

'====================================================================

'       initialisation
'       --------------
deb:

GOSUB IE3INIT

cmd$ = "INIT " + adr$ + ",0,7,1"
GOSUB IE3DRV

cmd$ = "SET 7,1000,900,900"
GOSUB IE3DRV

m$ = "FORM ASC"
GOSUB wrtie3

p5$ = SPACE$(100)

CLS
```


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```
IF zz$ = "N" THEN

flag% = 0
ici:
CLS
LOCATE 2, 5: PRINT "POTX2 pour 0V"

m$ = "volt:range 5,(@1:8)"
GOSUB wrtie3

m$ = "volt 0.00,(@1:8)"
GOSUB wrtie3


LOCATE 4, 5: INPUT "OK ? (O/N) ", a$
a$ = UCASE$(a$)
IF a$ = "N" THEN GOTO ici

ici2:


CLS
LOCATE 2, 5: PRINT "POTX1 pour 10V"

m$ = "volt:range 5,(@1:8)"
GOSUB wrtie3

m$ = "volt 10.0,(@1:8)"
GOSUB wrtie3

LOCATE 4, 5: INPUT "OK ? (O/N) ", a$

a$ = UCASE$(a$)
IF a$ = "N" THEN GOTO ici2
IF flag% = 0 THEN flag% = 1: GOTO ici
IF flag% = 1 THEN GOTO ici3
IF flag% = 2 THEN GOTO ici6

ici3:

CLS
LOCATE 2, 5: PRINT "REX3 pour -10V"
m$ = "volt:range 6,(@1:8)"
GOSUB wrtie3

m$ = "volt -10.0,(@1:8)"
GOSUB wrtie3

LOCATE 4, 5: INPUT "OK ? (O/N) ", a$
a$ = UCASE$(a$)
IF a$ = "N" THEN GOTO ici3

ici4:

CLS
LOCATE 2, 5: PRINT "Retenez cette valeur"

m$ = "volt:range 5,(@1:8)"
GOSUB wrtie3

m$ = "volt 10.0,(@1:8)"
GOSUB wrtie3
```


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```
LOCATE 4, 5: INPUT "OK ? (O/N) ", a$
a$ = UCASE$(a$)
IF a$ = "N" THEN GOTO ici4

ici5:

CLS
LOCATE 2, 5: PRINT "REX1 pour équilibrer avec mesure précédente"

m$ = "volt:range 6,(@1:8)"
GOSUB wrtie3

m$ = "volt 10.0,(@1:8)"
GOSUB wrtie3

LOCATE 4, 5: INPUT "OK ? (O/N) ", a$
a$ = UCASE$(a$)
IF a$ = "N" THEN GOTO ici4

flag% = 2: GOTO ici2

ici6:

CLS
LOCATE 2, 5: PRINT "REX2 pour 5V"

m$ = "volt:range 3,(@1:8)"
GOSUB wrtie3

m$ = "volt 5.00,(@1:8)"
GOSUB wrtie3

LOCATE 4, 5: INPUT "OK ? (O/N) ", a$
a$ = UCASE$(a$)
IF a$ = "N" THEN GOTO ici6

ici7:

CLS
LOCATE 2, 5: PRINT "Contrôle 0V"

m$ = "volt:range 6,(@1:8)"
GOSUB wrtie3

m$ = "volt 0.0,(@1:8)"
GOSUB wrtie3

LOCATE 4, 5: INPUT "OK ? (O/N) ", a$

a$ = UCASE$(a$)
IF a$ = "N" THEN GOTO ici7

'=====================================================================

ELSE

'=====================================================================

flag% = 0

zici:
CLS
LOCATE 2, 5: PRINT "POTX2 pour 0V"
```


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```
m$ = "volt:range 5,(@1:8)"
GOSUB wrtie3

m$ = "volt 0.00,(@1:8)"
GOSUB wrtie3


LOCATE 4, 5: INPUT "OK ? (O/N) ", a$
a$ = UCASE$(a$)
IF a$ = "N" THEN GOTO zici

zici2:


CLS
LOCATE 2, 5: PRINT "POTX1 pour 16V"

m$ = "volt:range 5,(@1:8)"
GOSUB wrtie3

m$ = "volt 16.0,(@1:8)"
GOSUB wrtie3

LOCATE 4, 5: INPUT "OK ? (O/N) ", a$

a$ = UCASE$(a$)
IF a$ = "N" THEN GOTO zici2
IF flag% = 0 THEN flag% = 1: GOTO zici
IF flag% = 1 THEN GOTO zici3
IF flag% = 2 THEN GOTO zici6

zici3:

CLS
LOCATE 2, 5: PRINT "REX3 pour -16V"
m$ = "volt:range 6,(@1:8)"
GOSUB wrtie3

m$ = "volt -16.0,(@1:8)"
GOSUB wrtie3

LOCATE 4, 5: INPUT "OK ? (O/N) ", a$
a$ = UCASE$(a$)
IF a$ = "N" THEN GOTO zici3

zici4:

CLS
LOCATE 2, 5: PRINT "Il faut Retenir cette valeur"

m$ = "volt:range 5,(@1:8)"
GOSUB wrtie3

m$ = "volt 16.0,(@1:8)"
GOSUB wrtie3

LOCATE 4, 5: INPUT "OK ? (O/N) ", a$
a$ = UCASE$(a$)
IF a$ = "N" THEN GOTO zici4
```


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```
zici5:

CLS
LOCATE 2, 5: PRINT "REX1 pour équilibrer avec mesure précédente"

m$ = "volt:range 6,(@1:8)"
GOSUB wrtie3

m$ = "volt 16.0,(@1:8)"
GOSUB wrtie3

LOCATE 4, 5: INPUT "OK ? (O/N) ", a$
a$ = UCASE$(a$)
IF a$ = "N" THEN GOTO zici4

flag% = 2: GOTO zici2

zici6:

CLS
LOCATE 2, 5: PRINT "REX2 pour 8V"

m$ = "volt:range 3,(@1:8)"
GOSUB wrtie3

m$ = "volt 8.00,(@1:8)"
GOSUB wrtie3

LOCATE 4, 5: INPUT "OK ? (O/N) ", a$
a$ = UCASE$(a$)
IF a$ = "N" THEN GOTO zici6

zici7:

CLS
LOCATE 2, 5: PRINT "Contrôle 0V"

m$ = "volt:range 6,(@1:8)"
GOSUB wrtie3

m$ = "volt 0.0,(@1:8)"
GOSUB wrtie3

LOCATE 4, 5: INPUT "OK ? (O/N) ", a$

a$ = UCASE$(a$)
IF a$ = "N" THEN GOTO zici7

'=================================================================
END IF


CLS

LOCATE 24, 20: PRINT "Voulez-vous continuer (O/N) :     "

DO
a$ = UCASE$(INKEY$)
LOOP WHILE a$ = ""

IF a$ = "N" THEN END

GOTO deb

END
```


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```
'       ------------------------------------------------------------
        '--- INTERFACEPROGRAM FOR MS-BASIC COMPILER or QuickBasic 4.5
        '    USING THE 'CALL ABSOLUTE' STATEMENT:
        '                                TPL.RACAL-DANA SEF 5/4/1989
'       ------------------------------------------------------------


wrtie3:
        cmd$ = "output " + ap$ + ",'" + m$ + "'"
'        LOCATE 10, 10: PRINT cmd$
        GOSUB IE3DRV


RETURN

RD3:
        cmd$ = "enter " + ap$ + ", #5"
'        LOCATE 12, 10: PRINT cmd$
        GOSUB IE3DRV
        r$ = p5$
RETURN

'---- ieee488 - INTERFACE SUBROUTINE

IE3DRV:

CC$ = "PAR 5," + cmd$
CALL IEEE(P1%, P2%, P3%, P4$, p5$, CC$, ER%)

RETURN


IE3INIT:
        DEF SEG = 0: IEEESEG% = PEEK(&H182) + PEEK(&H183) * 256
        IF IEEESEG% = 0 THEN
          SHELL "c:\bat\ines":          ' test si driver INES chargé ?
          GOTO IE3INIT
        END IF
RETURN

END


'
SUB attend (n) STATIC

        FOR i% = 1 TO n
'          FOR n% = 1 TO 10
'          NEXT n%
        NEXT i%

END SUB
```


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Annexe A.2 CONTRANO.BAS

```
DECLARE SUB onetouch (y$)

DEFINT A-Z
DECLARE SUB attend (n)
'       ********************************************************************
'       *                                                                  *
'       *               Programme de TEST 6060 & 6061                      *
'       *               Langage :       QuickBasic 4.0                     *
'       *               IBM PC + Interface IEEE-488 INES                   *
'       *               Version : 2.0   Création : 2/10/1992               *
'       *                               Edition  : 21/1/93    TPL          *
'       *                                                                  *
'       ********************************************************************

adr$ = "736"     ' Adresse absolue de carte INES à 2E0H / PC-IBM
ap$ = "701+3"      ' 700 + adresse IEEE de l_instrument  P101
'       ------------------------------------------------------------------
'        MAIN PROGRAM
'       ------------------------------------------------------------------
CLS
p5$ = SPACE$(100)
compt% = 0

rel:
SCREEN 9
CLS
LOCATE 1, 10: PRINT "CONTROLE SORTIES ANALOGIQUES 6061, Version 2.0"
m$ = "SYST:VERS?"
GOSUB WRTIE3
GOSUB rd3
LOCATE 3, 28: PRINT "Version SOFT   : "; RTRIM$(r$)
r$ = ""
m$ = "*IDN?"
GOSUB WRTIE3
GOSUB rd3
LOCATE 4, 28: PRINT "Identification : "; RTRIM$(r$)
z1$ = MID$(r$, 7, 5)

r$ = ""
m$ = "*OPT?"
GOSUB WRTIE3
GOSUB rd3
LOCATE 5, 28: PRINT "Options        : "; RTRIM$(LTRIM$(r$))
Z2$ = MID$(r$, 1, 3)

LOCATE 6, 28: PRINT "MODEL          : "; z1$
z1$ = RIGHT$(z1$, 1)
LOCATE 7, 28
IF Z2$ <> "16V" THEN
PRINT "CALIBRE        : 10V"
ELSE
PRINT "CALIBRE        : 16V"
END IF

IF Z2$ = "16V" THEN
    zz$ = "O"
ELSE
    zz$ = "N"
END IF

CALL onetouch(a$)
```


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```
'       initialisation
'       --------------
deb:

GOSUB IE3INIT
cmd$ = "INIT " + adr$ + ",0,7,1"
GOSUB IE3DRV
cmd$ = "SET 7,1000,900,900"
GOSUB IE3DRV
m$ = "FORM ASC"
GOSUB WRTIE3
m$ = "poc #h9c0000,1"
GOSUB WRTIE3
p5$ = SPACE$(100)
'=================================================================
IF zz$ = "N" THEN

ici:

IF z1$ = "B" THEN
        v$ = "16"
ELSE
        v$ = "8"
END IF

LOCATE 10, 5: PRINT "GAMME: +/- 10 V"
m$ = "volt:range 6,(@1:" + v$ + ")"
GOSUB WRTIE3

LOCATE 12, 5: PRINT "                    ": LOCATE 12, 5: PRINT "- 9.95 V"
m$ = "volt -9.95,(@1:" + v$ + ")"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 12, 5: PRINT "                    ": LOCATE 12, 5: PRINT "0 V"
m$ = "volt 0.0,(@1:" + v$ + ")"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 12, 5: PRINT "                    ": LOCATE 12, 5: PRINT "+ 9.95 V"
m$ = "volt 9.95,(@1:" + v$ + ")"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 10, 5: PRINT "                     "
LOCATE 10, 5: PRINT "GAMME: 0 à 10 V"
m$ = "volt:range 5,(@1:" + v$ + ")"
GOSUB WRTIE3

LOCATE 12, 5: PRINT "                    ": LOCATE 12, 5: PRINT "+ 0.1 V"
m$ = "volt 0.1,(@1:" + v$ + ")"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 12, 5: PRINT "                    ": LOCATE 12, 5: PRINT "+ 9.95 V"
m$ = "volt 9.95,(@1:" + v$ + ")"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 10, 5: PRINT "                     "
LOCATE 10, 5: PRINT "GAMME: +/- 5 V"
m$ = "volt:range 4,(@1:" + v$ + ")"
GOSUB WRTIE3
```


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```
LOCATE 12, 5: PRINT "                    ": LOCATE 12, 5: PRINT "- 4.95 V"
m$ = "volt -4.95,(@1:" + v$ + ")"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 12, 5: PRINT "                    ": LOCATE 12, 5: PRINT "0 V"
m$ = "volt 0.0,(@1:" + v$ + ")"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 12, 5: PRINT "                    ": LOCATE 12, 5: PRINT "+ 4.95 V"
m$ = "volt 4.95,(@1:" + v$ + ")"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 10, 5: PRINT "                     "
LOCATE 10, 5: PRINT "GAMME: 0 à 5V"
m$ = "volt:range 3,(@1:" + v$ + ")"
GOSUB WRTIE3

LOCATE 12, 5: PRINT "                    ": LOCATE 12, 5: PRINT "+ 0.1V"
m$ = "volt 0.1,(@1:" + v$ + ")"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 12, 5: PRINT "                    ": LOCATE 12, 5: PRINT "+ 4.95V"
m$ = "volt 4.95,(@1:" + v$ + ")"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 10, 5: PRINT "                     "
LOCATE 10, 5: PRINT "GAMME: +/- 1 V"
m$ = "volt:range 2,(@1:" + v$ + ")"
GOSUB WRTIE3

LOCATE 12, 5: PRINT "                    ": LOCATE 12, 5: PRINT "- 0.95 V"
m$ = "volt -0.95,(@1:" + v$ + ")"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 12, 5: PRINT "                    ": LOCATE 12, 5: PRINT "0 V"
m$ = "volt 0.0,(@1:" + v$ + ")"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 12, 5: PRINT "                    ": LOCATE 12, 5: PRINT "+ 0.95 V"
m$ = "volt 0.95,(@1:" + v$ + ")"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 10, 5: PRINT "                     "
LOCATE 10, 5: PRINT "GAMME: 0 à 1V"

m$ = "volt:range 1,(@1:" + v$ + ")"
GOSUB WRTIE3
LOCATE 12, 5: PRINT "                    ": LOCATE 12, 5: PRINT "+ 0.10V"
m$ = "volt 0.1,(@1:" + v$ + ")"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 12, 5: PRINT "                    ": LOCATE 12, 5: PRINT "+ 0.95V"
m$ = "volt 0.95,(@1:" + v$ + ")"
GOSUB WRTIE3
CALL onetouch(a$)

ELSE
```


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```
LOCATE 10, 5: PRINT "                          "
LOCATE 10, 5: PRINT "GAMME: +/- 16 V"
m$ = "volt:range 6,(@1:8)"
GOSUB WRTIE3

LOCATE 12, 5: PRINT "                         ": LOCATE 12, 5: PRINT "- 15.95 V"
m$ = "volt -15.95,(@1:8)"
GOSUB WRTIE3:CALL onetouch(a$)

LOCATE 12, 5: PRINT "                         ": LOCATE 12, 5: PRINT "0 V"
m$ = "volt 0.0,(@1:8)"
GOSUB WRTIE3:CALL onetouch(a$)

LOCATE 12, 5: PRINT "                         ": LOCATE 12, 5: PRINT "+ 15.95 V"
m$ = "volt 15.95,(@1:8)"
GOSUB WRTIE3:CALL onetouch(a$)

LOCATE 10, 5: PRINT "                          "
LOCATE 10, 5: PRINT "GAMME: 0 à 16 V"
m$ = "volt:range 5,(@1:8)"
GOSUB WRTIE3

LOCATE 12, 5: PRINT "                         ": LOCATE 12, 5: PRINT "+ 0.1 V"
m$ = "volt 0.1,(@1:8)"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 12, 5: PRINT "                         ": LOCATE 12, 5: PRINT "+ 15.95 V"
m$ = "volt 15.95,(@1:8)"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 10, 5: PRINT "                          "
LOCATE 10, 5: PRINT "GAMME: +/- 8 V"
m$ = "volt:range 4,(@1:8)"
GOSUB WRTIE3

LOCATE 12, 5: PRINT "                         ": LOCATE 12, 5: PRINT "- 7.95 V"
m$ = "volt -7.95,(@1:8)"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 12, 5: PRINT "                         ": LOCATE 12, 5: PRINT "0 V"
m$ = "volt 0.0,(@1:8)"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 12, 5: PRINT "                         ": LOCATE 12, 5: PRINT "+ 7.95 V"
m$ = "volt 7.95,(@1:8)"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 10, 5: PRINT "                          "
LOCATE 10, 5: PRINT "GAMME: 0 à 8V"
m$ = "volt:range 3,(@1:8)"
GOSUB WRTIE3

LOCATE 12, 5: PRINT "                         ": LOCATE 12, 5: PRINT "+ 0.1V"
m$ = "volt 0.1,(@1:8)"
GOSUB WRTIE3
CALL onetouch(a$)

LOCATE 12, 5: PRINT "                         ": LOCATE 12, 5: PRINT "+ 7.95V"
m$ = "volt 7.95,(@1:8)"
GOSUB WRTIE3:CALL onetouch(a$)
```

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```
LOCATE 10, 5: PRINT "                          "
LOCATE 10, 5: PRINT "GAMME: +/- 1.6 V"
m$ = "volt:range 2,(@1:8)"
GOSUB WRTIE3

LOCATE 12, 5: PRINT "                        ": LOCATE 12, 5: PRINT "- 1.55 V"
m$ = "volt -1.55,(@1:8)"
GOSUB WRTIE3:CALL onetouch(a$)

LOCATE 12, 5: PRINT "                        ": LOCATE 12, 5: PRINT "0 V"
m$ = "volt 0.0,(@1:8)"
GOSUB WRTIE3:CALL onetouch(a$)

LOCATE 12, 5: PRINT "                        ": LOCATE 12, 5: PRINT "+ 1.55 V"
m$ = "volt 1.55,(@1:8)"
GOSUB WRTIE3:CALL onetouch(a$)

LOCATE 10, 5: PRINT "                          "
LOCATE 10, 5: PRINT "GAMME: 0 à 1.6 V"

m$ = "volt:range 1,(@1:8)"
GOSUB WRTIE3

LOCATE 12, 5: PRINT "                        ": LOCATE 12, 5: PRINT "+ 0.10V"
m$ = "volt 0.1,(@1:8)"
GOSUB WRTIE3:CALL onetouch(a$)

LOCATE 12, 5: PRINT "                        ": LOCATE 12, 5: PRINT "+ 1.55V"
m$ = "volt 1.55,(@1:8)"
GOSUB WRTIE3:CALL onetouch(a$)

'================================================================
END IF

PRINT CHR$(7);
LOCATE 24, 20: PRINT "Voulez-vous continuer? (O/N)     ";
CALL onetouch(a$)

a$ = UCASE$(a$)
IF a$ <> "N" AND a$ <> "n" THEN
        LOCATE 18, 10: PRINT "          "
        LOCATE 20, 10: PRINT "                          "
        LOCATE 24, 20: PRINT "                                    ";

        GOTO deb
END IF
END

'       ---------------------------------------------------------------
        '--- INTERFACEPROGRAM FOR MS-BASIC COMPILER or QuickBasic 4.5
        '    USING THE 'CALL ABSOLUTE' STATEMENT:
        '                                TPL.RACAL-DANA SEF 5/4/1989
'       ---------------------------------------------------------------
WRTIE3:
        cmd$ = "output " + ap$ + ",'" + m$ + "'"
        GOSUB IE3DRV

RETURN

rd3:
        r$ = ""
        p5$ = SPACE$(80)
        cmd$ = "enter " + ap$ + ", #5"
        GOSUB IE3DRV
        r$ = p5$
RETURN
```


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```
'---- ieee488 - INTERFACE SUBROUTINE

IE3DRV:

CC$ = "PAR 5," + cmd$
CALL IEEE(P1%, P2%, P3%, P4$, p5$, CC$, ER%)

RETURN



IE3INIT:
        DEF SEG = 0: IEEESEG% = PEEK(&H182) + PEEK(&H183) * 256
        IF IEEESEG% = 0 THEN
          SHELL "c:\bat\ines":          ' test si driver INES chargé ?
          GOTO IE3INIT
        END IF
RETURN

END

'
SUB attend (n) STATIC

        FOR i% = 1 TO n
'          FOR n% = 1 TO 10
'          NEXT n%
        NEXT i%

END SUB

SUB onetouch (y$)
DO
 y$ = INKEY$
LOOP WHILE y$ = ""
END SUB
```


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Annexe A.3 ANI.BAS

```
DEFINT A-Z
DECLARE SUB attend (n)

'       ********************************************************************
'       *                                                                  *
'       *               Programme de TEST 6060 & 6061                      *
'       *               Langage :       QuickBasic 4.0                     *
'       *               IBM PC + Interface IEEE-488 INES                   *
'       *               Version : 1.0   Création : 8/8/1991                *
'       *                               Edition  : 25/9/92 TPL             *
'       *                                                                  *
'       ********************************************************************
dl% = 5000      ' délai
adr$ = "736"    ' Adresse absolue de carte INES à 2E0H / PC-IBM
ap$ = "701+3"   ' 700 + adresse IEEE de l_instrument  P101
'       ------------------------------------------------------------------
'        MAIN PROGRAM
'       ------------------------------------------------------------------
p5$ = SPACE$(80)

'       initialisation
'       --------------
GOSUB IE3INIT
cmd$ = "INIT " + adr$ + ",0,7,1"
GOSUB IE3DRV
cmd$ = "SET 7,1000,900,900"
GOSUB IE3DRV

m$ = "FORM ASC"
GOSUB WRTIE3

p5$ = SPACE$(80)

SCREEN 9
CLS
LOCATE 1, 25: PRINT "ENTREES ANALOGIQUES Version 2.0"

m$ = "SYST:VERS?"
GOSUB WRTIE3
GOSUB RD3
COLOR 12
LOCATE 5, 10: PRINT "Version SCPI    : "; r$

m$ = "*IDN?"
GOSUB WRTIE3
GOSUB RD3
LOCATE 6, 10: PRINT "Identification : "; r$
z1$ = MID$(r$, 11, 1)

m$ = "*OPT?"
GOSUB WRTIE3
GOSUB RD3
LOCATE 7, 10: PRINT "Options        : "; r$
z2$ = MID$(r$, 1, 3)
```


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```
m$ = "poc #h9c0000,1"
GOSUB WRTIE3
ici:

COLOR 15
LOCATE 10, 10: PRINT "Entrez le calibre (1 à 6) :                    "
DO
     clav$ = INKEY$
LOOP WHILE VAL(clav$) < 1 OR VAL(clav$) > 6

IF z2$ <> "16V" THEN
SELECT CASE VAL(clav$)
        CASE 1
        range$ = "0-1 V"
        CASE 2
        range$ = "±1 V"
        CASE 3
        range$ = "0-5 V"
        CASE 4
        range$ = "±5 V"
        CASE 5
        range$ = "0-10V"
        CASE 6
        range$ = "±10 V"
END SELECT

ELSE
SELECT CASE VAL(clav$)
        CASE 1
        range$ = "0-1.6 V"
        CASE 2
        range$ = "±1.6 V"
        CASE 3
        range$ = "0-8 V"
        CASE 4
        range$ = "±8 V"
        CASE 5
        range$ = "0-16V"
        CASE 6
        range$ = "±16 V"
END SELECT
END IF

LOCATE 10, 37: PRINT SPACE$(15)
LOCATE 10, 39: PRINT range$

IF z1$ = "C" THEN
LOCATE 12, 1: PRINT "Voies: 1"; TAB(16); "2"; TAB(26); "3"; TAB(36); "4"; TAB(46);
"5"; TAB(56); "6"; TAB(66); "7"; TAB(76); "8"
END IF

LOCATE 18, 1: PRINT "Voies: 9"; TAB(16); "10"; TAB(26); "11"; TAB(36); "12";
TAB(46); "13"; TAB(56); "14"; TAB(66); "15"; TAB(76); "16"

IF z1$ <> "C" THEN
        m$ = "SENSE:VOLT:RANG " + clav$ + ",(@9:16)"
ELSE
        m$ = "SENSE:VOLT:RANG " + clav$ + ",(@1:16)"
END IF
```


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```
GOSUB WRTIE3

DO
  IF z1$ <> "C" THEN
  FOR t% = 1 TO dl%: NEXT t%: ' Attendre pour Lecture
  END IF

  IF z1$ = "C" THEN
    m$ = "MEAS:VOLT? (@1:8)"
    GOSUB WRTIE3
    GOSUB RD3
    b$ = ""
    col% = 1
    FOR i% = 1 TO LEN(r$)
        a$ = MID$(r$, i%, 1)
        b$ = b$ + a$
        IF a$ = "," THEN
            LOCATE 14, col%: PRINT USING "###.### V"; VAL(b$)
        IF VAL(b$) > 9 AND VAL(b$) < 10 THEN
            LOCATE 16, col%: PRINT USING "###.## kΩ"; .1 / ((9.5 / VAL(b$)) - 1)
        END IF
            col% = col% + 10
            b$ = ""
        END IF
    NEXT i%
    LOCATE 14, col%: PRINT USING "###.### V"; VAL(b$)
        IF VAL(b$) > 9 AND VAL(b$) < 10 THEN
            LOCATE 16, col%: PRINT USING "###.## kΩ"; .1 / ((9.5 / VAL(b$)) - 1)
        END IF
  END IF

    m$ = "MEAS:VOLT? (@9:16)"
    GOSUB WRTIE3
    GOSUB RD3

    b$ = ""
    col% = 1

    FOR i% = 1 TO LEN(r$)
        a$ = MID$(r$, i%, 1)
        b$ = b$ + a$
        IF a$ = "," THEN
            LOCATE 20, col%: PRINT USING "###.### V"; VAL(b$)
        IF VAL(b$) > 9 AND VAL(b$) < 10 THEN
            LOCATE 22, col%: PRINT USING "###.## kΩ"; .1 / ((9.5 / VAL(b$)) - 1)
        END IF
            col% = col% + 10
            b$ = ""
        END IF
    NEXT i%
    LOCATE 20, col%: PRINT USING "###.### V"; VAL(b$)
        IF VAL(b$) > 9 AND VAL(b$) < 10 THEN
            LOCATE 22, col%: PRINT USING "###.## kΩ"; .1 / ((9.5 / VAL(b$)) - 1)
        END IF

LOOP WHILE INKEY$ = ""

LOCATE 14, 1: PRINT SPACE$(80)
```


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```
LOCATE 16, 1: PRINT SPACE$(80)
LOCATE 20, 1: PRINT SPACE$(80)
LOCATE 22, 1: PRINT SPACE$(80)
LOCATE 10, 33: PRINT " "
GOTO ici

END
'       ---------------------------------------------------------------
        '--- INTERFACEPROGRAM FOR MS-BASIC COMPILER or QuickBasic 4.5
        '    USING THE 'CALL ABSOLUTE' STATEMENT:
        '                                TPL.RACAL-DANA SEF 5/4/1989
'       ---------------------------------------------------------------
WRTIE3:
        cmd$ = "output " + ap$ + ",'" + m$ + "'"
        GOSUB IE3DR
RETURN

RD3:
        attend (dl%)
        r$ = ""
        p5$ = SPACE$(80)
        cmd$ = "enter " + ap$ + ", #5"
        GOSUB IE3DRV
        r$ = RTRIM$(LTRIM$(p5$))
RETURN

'---- ieee488 - INTERFACE SUBROUTINE

IE3DRV:

CC$ = "PAR 5," + cmd$
CALL IEEE(P1%, P2%, P3%, P4$, p5$, CC$, ER%)

RETURN

IE3INIT:
        DEF SEG = 0: IEEESEG% = PEEK(&H182) + PEEK(&H183) * 256
        IF IEEESEG% = 0 THEN
          GOTO IE3INIT
        END IF
RETURN

END

'
SUB attend (n) STATIC

        FOR i% = 1 TO n
        NEXT i%

END SUB
```


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Annexe A.4 ANI_6061E.BAS

```
DEFINT A-Z
DECLARE SUB attend (n)
'       ********************************************************************
'       *                                                                  *
'       *               Programme de TEST 6061 E                           *
'       *               Langage :       QuickBasic 4.0                     *
'       *               IBM PC + Interface IEEE-488 INES                   *
'       *               Version : 1.0   Création : 8/8/1992                *
'       *                               Edition  : 20/2/93                 *
'       *                                                                  *
'       ********************************************************************
adr$ = "736"     ' Adresse absolue de carte INES à 2E0H / PC-IBM
ap$ = "701+3"     ' 700 + adresse IEEE de l_instrument  P101
'       ------------------------------------------------------------------
'        MAIN PROGRAM
'       ------------------------------------------------------------------
CLS
p5$ = SPACE$(50)
compt% = 0
'       initialisation
'       --------------
GOSUB IE3INIT
cmd$ = "INIT " + adr$ + ",0,7,1"
GOSUB IE3DRV
cmd$ = "SET 7,1000,900,900"
GOSUB IE3DRV
SCREEN 9
LOCATE 1, 20: PRINT "ENTREES ANALOGIQUES 6061E"
LOCATE 3, 1
PRINT " Voie1     Voie2     Voie3     Voie4     Voie5     Voie6     Voie7     Voie
LOCATE 24, 20: PRINT "Tapez une touche pour sortir";
DO
        m$ = "MEAS:PSUP1?"
        GOSUB WRTIE3
        GOSUB RD3
        LOCATE 5, 1: PRINT r$
        m$ = "MEAS:PSUP2?"
        GOSUB WRTIE3
        GOSUB RD3
        LOCATE 5, 11: PRINT r$
        m$ = "MEAS:PSUP3?"
        GOSUB WRTIE3
        GOSUB RD3
        LOCATE 5, 21: PRINT r$
        m$ = "MEAS:PSUP4?"
        GOSUB WRTIE3
        GOSUB RD3
        LOCATE 5, 31: PRINT r$

        m$ = "MEAS:VOLT1?"
        GOSUB WRTIE3
```

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```
        GOSUB RD3
        LOCATE 5, 41: PRINT r$
        m$ = "MEAS:VOLT2?"
        GOSUB WRTIE3
        GOSUB RD3
        LOCATE 5, 51: PRINT r$
        m$ = "MEAS:VOLT3?"
        GOSUB WRTIE3
        GOSUB RD3
        LOCATE 5, 61: PRINT r$
        m$ = "MEAS:VOLT4?"
        GOSUB WRTIE3
        GOSUB RD3
        LOCATE 5, 71: PRINT r$
LOOP WHILE INKEY$ = ""

END
'       ---------------------------------------------------------------
        '--- INTERFACEPROGRAM FOR MS-BASIC COMPILER or QuickBasic 4.5
        '    USING THE 'CALL ABSOLUTE' STATEMENT:
        '                                    TPL.RACAL-DANA SEF 5/4/1989
'       ---------------------------------------------------------------
WRTIE3:
        cmd$ = "output " + ap$ + ",'" + m$ + "'"
        GOSUB IE3DRV
RETURN

RD3:
        cmd$ = "enter " + ap$ + ", #5"
        GOSUB IE3DRV
        r$ = LTRIM$(RTRIM$(p5$))
RETURN

'---- ieee488 - INTERFACE SUBROUTINE
IE3DRV:
 CC$ = "PAR 5," + cmd$
 CALL IEEE(P1%, P2%, P3%, P4$, p5$, CC$, ER%)
RETURN

IE3INIT:
        DEF SEG = 0: IEEESEG% = PEEK(&H182) + PEEK(&H183) * 256
        IF IEEESEG% = 0 THEN
          SHELL "c:\bat\ines":          ' test si driver INES chargé ?
          GOTO IE3INIT
        END IF
RETURN

END

SUB attend (n) STATIC

        FOR i% = 1 TO n
        NEXT i%
END SUB
```


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Annexe A.5 DIO.BAS

```
DEFINT A-Z
DECLARE SUB attend (n)

'       ********************************************************************
'       *                                                                  *
'       *               Programme de TEST 6060 & 6061                      *
'       *               Langage :       QuickBasic 4.0                     *
'       *               IBM PC + Interface IEEE-488 INES                   *
'       *               Version : 1.0   Création : 8/8/1991                *
'       *                               Edition  :                         *
'       *                                                                  *
'       ********************************************************************

adr$ = "736"     ' Adresse absolue de carte INES à 2E0H / PC-IBM
ap$ = "701+3"      ' 700 + adresse IEEE de l_instrument  P101

'       ------------------------------------------------------------------
'        MAIN PROGRAM
'       ------------------------------------------------------------------
CLS
p5$ = SPACE$(50)
compt% = 0

'       initialisation
'       --------------

GOSUB IE3INIT
cmd$ = "INIT " + adr$ + ",0,7,1"
GOSUB IE3DRV
cmd$ = "SET 7,1000,900,900"
GOSUB IE3DRV
SCREEN 9
'       ------------------------------------------------------------------
'        PROCEDURE DIGITAL INPUTS/OUTPUTS
'       ------------------------------------------------------------------

dio:
LOCATE 1, 20: PRINT "Brancher le connecteur avec LEDS"
LOCATE 23, 25: PRINT "Tapez 'S' pour sortir"
DO
a$ = INKEY$
IF a$ = "S" OR a$ = "s" THEN
        m$ = "DOGL 65535;"
        GOSUB WRTIE3
        END
END IF

p5$ = "    "
        m$ = "MEAS:DIP3?;"
        GOSUB WRTIE3
        GOSUB RD3
        m$ = "DOP1 " + p5$ + ";"
        GOSUB WRTIE3
p5$ = "     "
        m$ = "MEAS:DIP4?;"
```

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```
        GOSUB WRTIE3
        GOSUB RD3
        m$ = "DOP2 " + p5$ + ";"
        GOSUB WRTIE3
LOOP

END


'       ---------------------------------------------------------------
        '--- INTERFACEPROGRAM FOR MS-BASIC COMPILER or QuickBasic 4.5
        '    USING THE 'CALL ABSOLUTE' STATEMENT:
        '                                TPL.RACAL-DANA SEF 5/4/1989
'       ---------------------------------------------------------------

WRTIE3:
        cmd$ = "output " + ap$ + ",'" + m$ + "'"
'        LOCATE 10, 10: PRINT cmd$
        GOSUB IE3DRV
RETURN


RD3:
        cmd$ = "enter " + ap$ + ", #5"
'        LOCATE 12, 10: PRINT cmd$
        GOSUB IE3DRV
        r$ = p5$
RETURN

'---- ieee488 - INTERFACE SUBROUTINE

IE3DRV:
 CC$ = "PAR 5," + cmd$
 CALL IEEE(P1%, P2%, P3%, P4$, p5$, CC$, ER%)
RETURN


IE3INIT:
        DEF SEG = 0: IEEESEG% = PEEK(&H182) + PEEK(&H183) * 256
        IF IEEESEG% = 0 THEN
          SHELL "c:\bat\ines":          ' test si driver INES chargé ?
          GOTO IE3INIT
        END IF
RETURN

END

'
SUB attend (n) STATIC

        FOR i% = 1 TO n
'          FOR n% = 1 TO 10
'          NEXT n%
        NEXT i%

END SUB
```


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SECTION 5

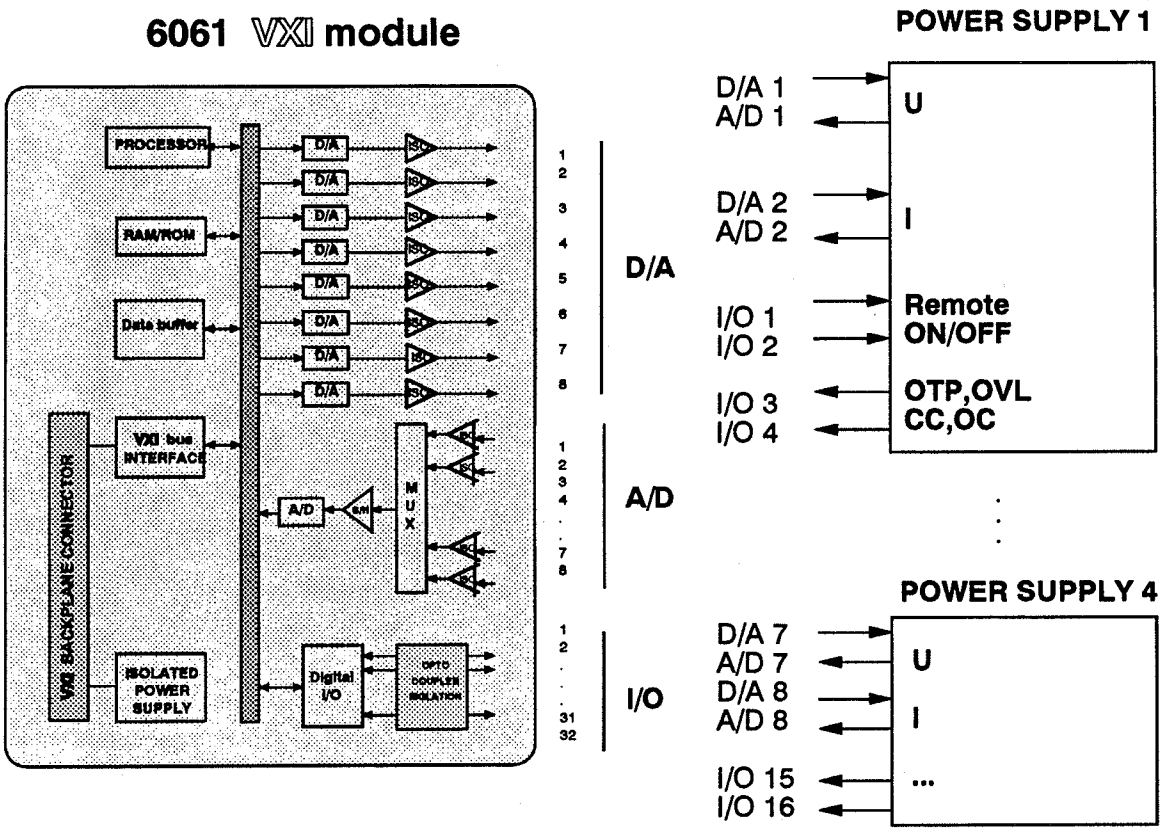
APPLICATIONS

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APPLICATION EXAMPLE

One 6061A can be used in a VXI system for driving 4 power supplies.

(The 6061E includes a specific software for this example).



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```
'=================================================

REM    Version 1.0  February 1992

'=================================================

REM Copyright RACAL DANA, RACAL SYSTEMS Electronique S.A.
REM All Rights Reserved

'=================================================

dim shared retour as string * 100
dim shared ritour as string * 100
dim shared envoi as string * 17
y% = InitVXIlibrary
cls
rem----------------------HEIDEN 1109-16-------------------------------
rem
rem--------------Range+Remote mode-----------------------------------
          y% = WSwrt (24, "volt:rang 6,(@1)", 16&, 3, all&)
          y% = WSwrt (24, "volt:rang 6,(@2)", 16&, 3, all&)
          y% = WSwrt (24, "volt:rang 3,(@3)", 16&, 3, all&)
          y% = WSwrt (24, "volt 5.0,(@3)", 13&, 3, all&)
print""
print"       Driving the Heiden 1109-16 Power Supply by RACAL 6061 VXI
module"
print""
      input "      Output Voltage ? (0-16v) : ",Uin#
      Uinap# = Uin#/1.600
      input "      Current Limit ? (0-4A) : ",Iin#
      Iinap# = Iin#*2.500
print""

rem-------------Send commands to 6061-----------------
rem-------- Write Voltage by Analog Output n° 1 --------
rem-------- Write Current by Analog Output n° 2 --------

 n% = Fmt(envoi$,"%s<volt %f[w6p3],(@1)",Uinap#)
 y% = WSwrt (24, envoi$, 16&, 3, all&)
 n% = Fmt(envoi$,"%s<volt %f[w6p3],(@2)",Iinap#)
 y% = WSwrt (24, envoi$, 16&, 3, all&)

call delay(0.5#)
rem-------- Read Voltage by Analog Input n° 9 --------
rem-------- Return the effective Voltage -----------------

  y% = WSwrt (24, "meas:volt? (@9)", 15&, 3, all&)
  y% = WSrd (24, retour$, 100&, 1, ret& )
  n% = Scan(retour$,"%s>%f",lectvolt#)
  print "      Effective Voltage = ",lectvolt# *1.600, "Volt"

rem-------- Read Current by Analog Input n° 10 --------
rem-------- Return the effective Current -----------------

  y% = WSwrt (24, "meas:volt? (@10)", 16&, 3, all&)
  y% = WSrd (24, ritour$, 100&, 1, ret& )
  n% = Scan(ritour$,"%s>%f",lectamp#)
  afficour#=lectamp#/2.500
  print "      Effective Current = ",afficour#,"Amp"

end
```


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SECTION 6

TECHNICAL DESCRIPTION

This section describes the theory of operation of a 6061 Series.

The 6061A is used as the reference designators for the circuit descriptions given in this section.

This section begins with a block diagram description of the 6061A module then extends to the description of the circuit action at the component level:

6.1 Introduction

6.2 Block Diagram

6.3 Mother Board

6.4 Microprocessor and VXI Interface Board

6.5 DC/DC Converter

6.6 Digital Inputs/Outputs Board

6.7 Analog Inputs Board

6.8 Analog Outputs Board

Section 8 gives schematics of each electronic sub assembly.

Section 9 gives drawings and PCB description of each sub assembly.

Section 10 gives parts list of each sub assembly.

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6.1 INTRODUCTION

The 6061 model can be physically broken down in seven physical blocks:

- **FS910107**: Final assembly (VXI C size box, front panel ...)

- **FS910101**: Mother board with logic extensions.

This board contains:
. Connectors P1 and P2 of the VXI bus.
. Power supply filters and internal fuses.
. Buffers for Microprocessor buses (DATA, ADDRESS and CONTROL).
. Extension for RAM and EPROM.
. PLD (Programmable Logic Devices) for address decoder function.
. High precision Voltage Reference for Digital to Analog Converters.
. Glue logic.

- **FS910105**: Microprocessor and VXI Interface board.

This board contains:
. The 68000 Microprocessor and associated circuits.
. RAM, EPROM, NVRAM (Non volatile RAM)
. VXI Interface and Registers.
. Programmable Time base.
. Connector P100 of the Microprocessor bus.

- **FS910106**: multi channel Isolated DC/DC Converters.

This shielded board contains 18 independent DC/DC converters (Input 24VDC, Outputs ± 15VDC).

- 16 isolated converters are used by Analog Inputs/Outputs Boards,
- 1 isolated converter is used to supply power for Option 02 (Digital I/O with TTL compatible level)
- 1 reserved DC/DC converter for maintenance purpose.

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- **FS910102**: 32 channels Digital I/O board.

This board contains:
. Four 8 bits Ouput ports.
. Four 8 bits Input ports.
. Optocouplers for digital ouputs.
. Optocouplers and constant current regulators for digital inputs.

- **FS910103**: 8 isolated channels Analog Outputs board.

This board contains 8 identical channels. Each channel contains:
. 12-bits DAC.
. 6-Ranges Electronic (0 to 1V, 0 to 5V, 0 to 10V, ±1V, ±5V, ±10V).
. Isolated amplifier.
. Ouput active filter and amplifier.
. Voltage to Current Converter (Option 03).
. Glue logic.

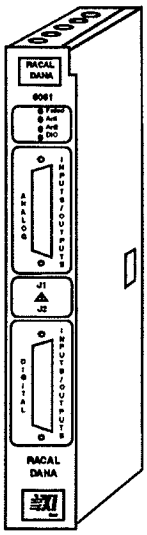
- **FS910103**: 8 isolated channels Analog Inputs board.

This board contains one common electronic and 8 identical isolated channels. The common electronic contains:
. One 12-bits ADC
. One 8 channel analog multiplexer.
. 6-Ranges Electronic (0 to 1V, 0 to 5V, 0 to 10V, ±1V, ±5V, ±10V).

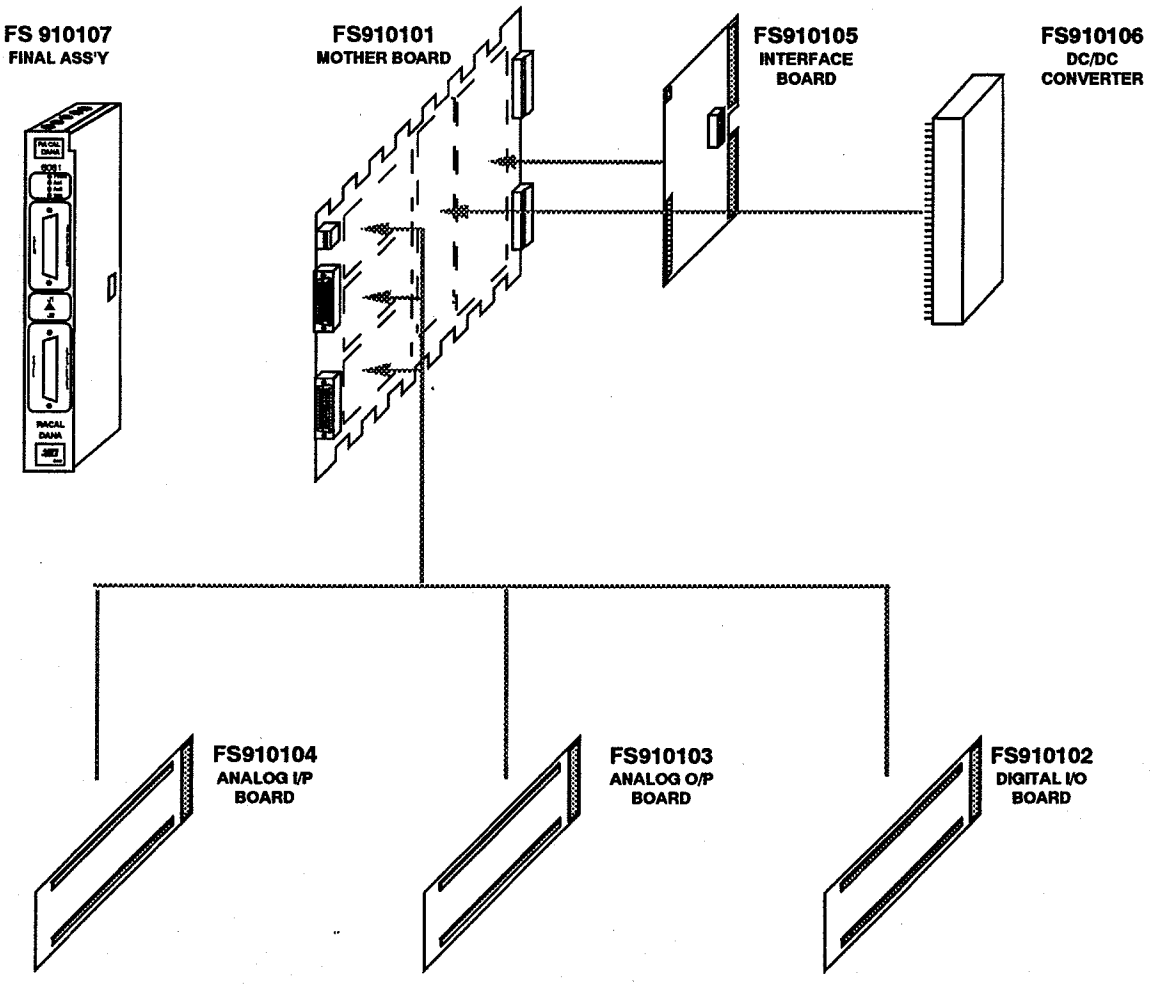
Each isolated channel contains:
. Overvoltage protection and high impedance input amplifier.
. Gain-programmable Amplifier.
. Isolated amplifier and active filter.
. Glue logic.

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PHYSICAL BLOCK DIAGRAM

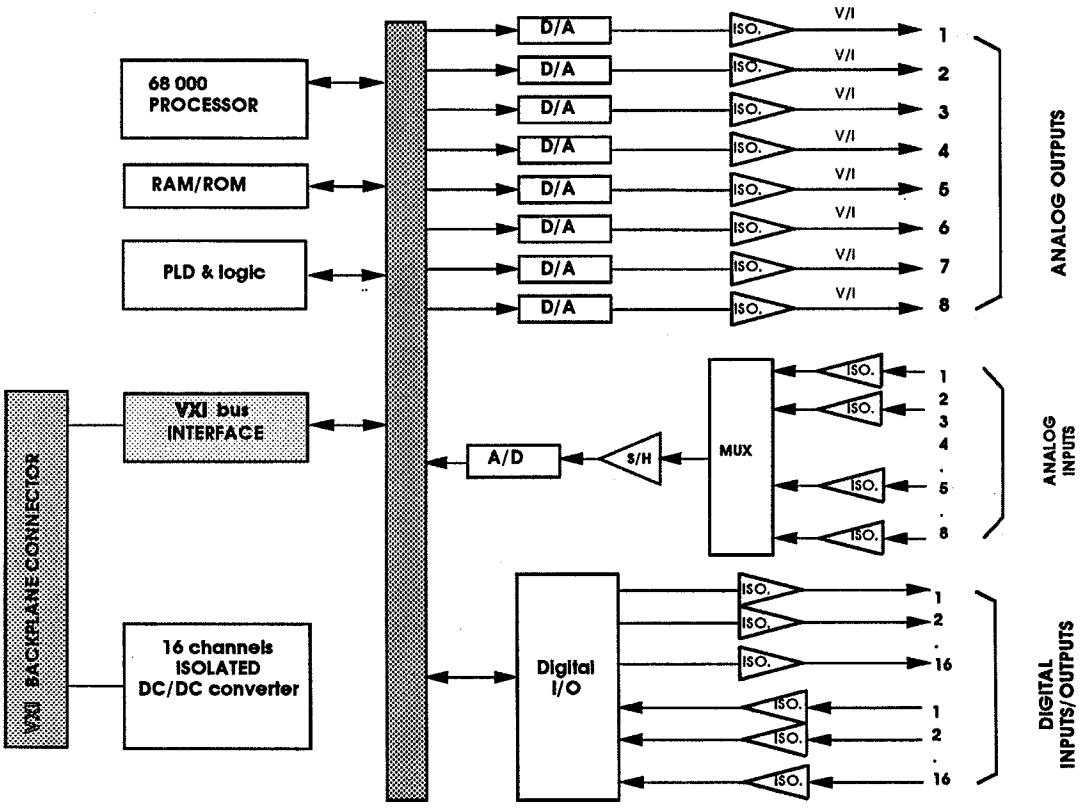


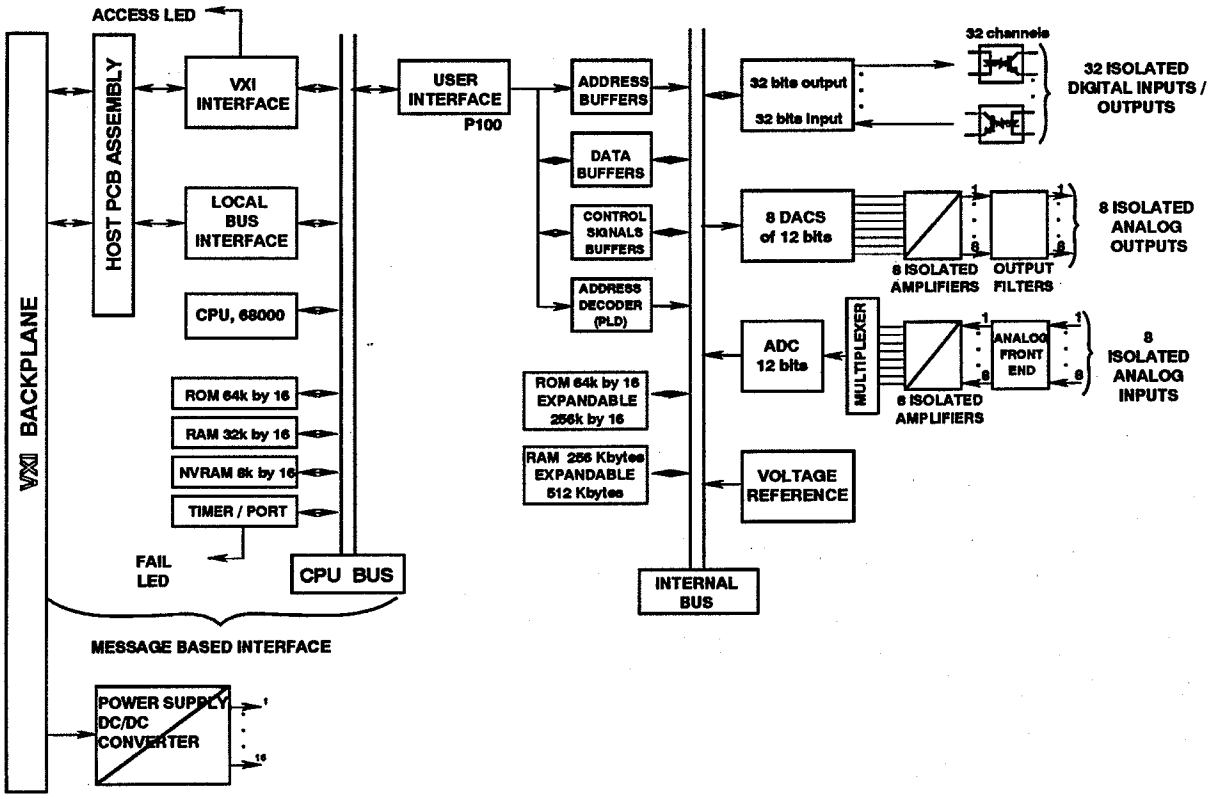
6061



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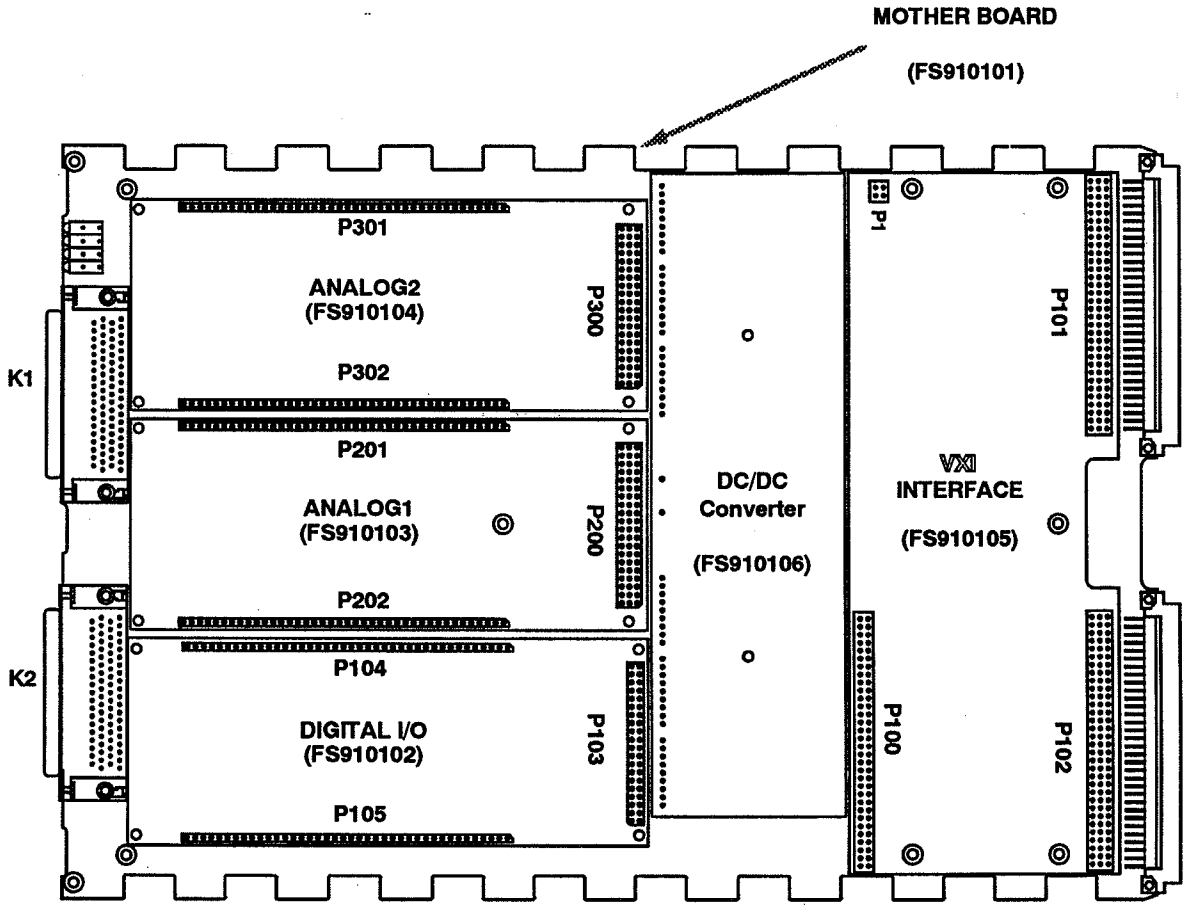
6.2 BLOCK DIAGRAM and GENERAL VIEW





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6061A: GENERAL VIEW



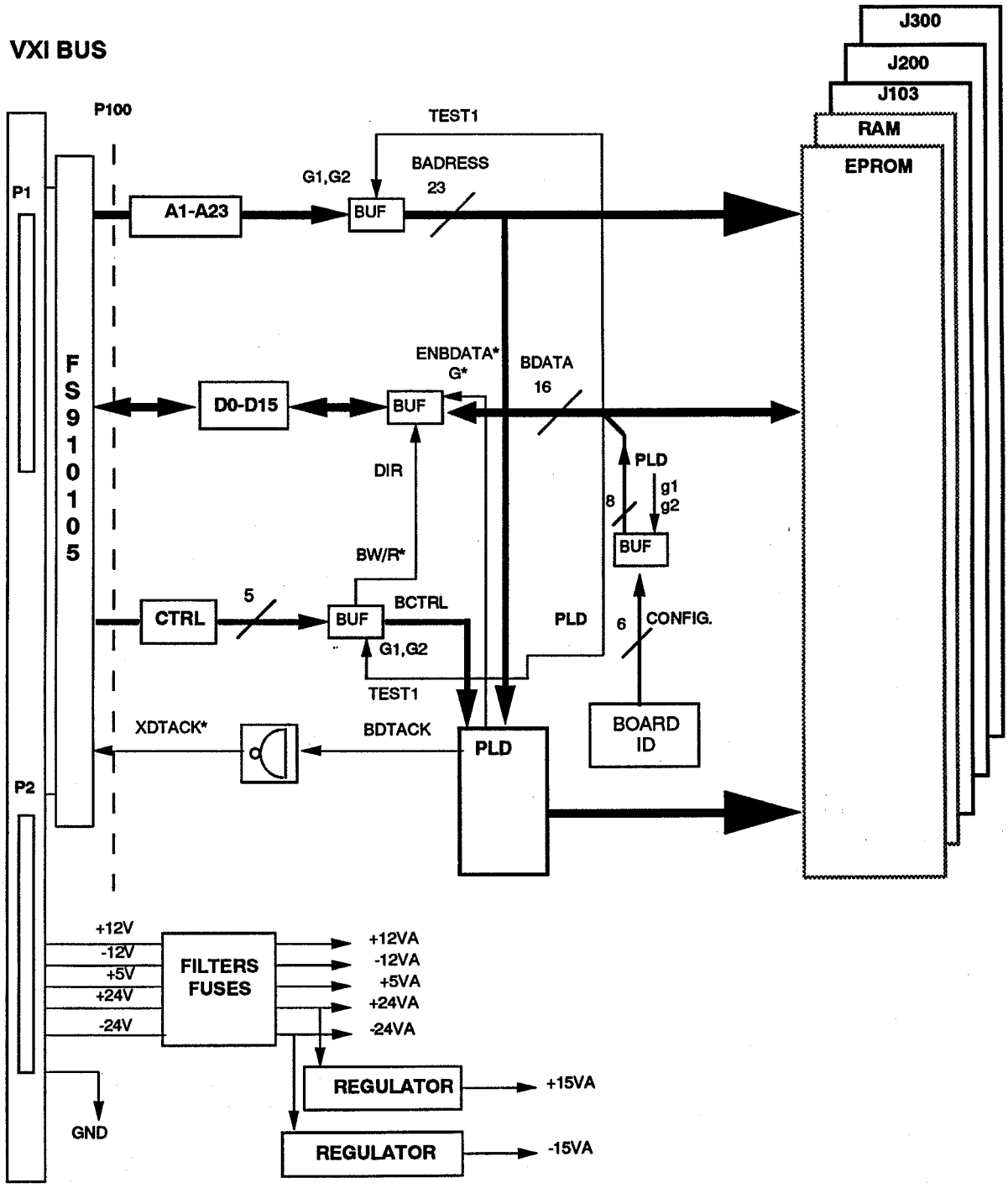
VERSION	ANALOG1	ANALOG2
6061A	OUTPUT	INPUT
6061B	OUTPUT	OUTPUT
6061C	INPUT	INPUT
6061D	-	-
6061E	OUTPUT	INPUT

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6.3 Mother Board

6.3.1 Block diagram of the Mother Board
6.3.2 P1 and P2 connectors (from VXI bus)
6.3.3 K1 and K2 connectors (on the front panel)
6.3.4 Power supplies
6.3.5 Bus buffers and the memory extension
6.3.6 PLD
6.3.7 Voltage Reference

6.3.1 Block Diagram of the Mother Board



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6.3.2 Connectors P1 and P2 of the VXI bus.

P1:

N°	Row A	Row B	Row C	N°
1	D00	BBSY*	D08	1
2	D01	BCLR*	D09	2
3	D02	ACFAIL*	D10	3
4	D03	BG0IN*	D11	4
5	D04	BG0OUT*	D12	5
6	D05	BG1IN*	D13	6
7	D06	BG1OUT*	D14	7
8	D07	BG2IN*	D15	8
9	GND	BG2OUT*	GND	9
10	SYSCLK	BG3IN*	SYSFAIL*	10
11	GND	BG3OUT*	BERR*	11
12	DS1*	BR0*	SYSRESET*	12
13	DS0*	BR1*	LWORD*	13
14	WRITE*	BR2*	AM5	14
15	GND	BR3*	A23	15
16	DTACK*	AM0	A22	16
17	GND	AM1	A21	17
18	AS*	AM2	A20	18
19	GND	AM3	A19	19
20	IACK*	GND	A18	20
21	IACKIN*	SERCLK (1)	A17	21
22	IACKOUT*	SERDAT (1)	A16	22
23	AM4	GND	A15	23
24	A07	IRQ7*	A14	24
25	A06	IRQ6*	A13	25
26	A05	IRQ5*	A12	26
27	A04	IRQ4*	A11	27
28	A03	IRQ3*	A10	28
29	A02	IRQ2*	A09	29
30	A01	IRQ1*	A08	30
31	(-12V)	(+5V STDBY)	(+12V)	31
32	(+5V)	(+5V)	(+5V)	32

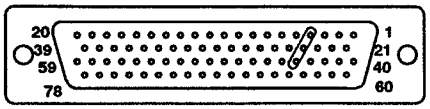
P2:

N°	Row A	Row B	Row C	N°
1	ECLTRG0	(+5V)	CLK10+	1
2	(-2V)	GND	CLK10-	2
3	ECLTRG1	RSV1	GND	3
4	GND	A24	(-5.2V)	4
5	LBUSA00	A25	LBUSC00	5
6	LBUSA01	A26	LBUSC01	6
7	(-5.2V)	A27	GND	7
8	LBUSA02	A28	LBUSC02	8
9	LBUSA03	A29	LBUSC03	9
10	GND	A30	GND	10
11	LBUSA04	A31	LBUSC04	11
12	LBUSA05	GND	LBUSC05	12
13	(-5.2V)	(+5V)	(-2V)	13
14	LBUSA06	D16	LBUSC06	14
15	LBUSA07	D17	LBUSC07	15
16	GND	D18	GND	16
17	LBUSA08	D19	LBUSC08	17
18	LBUSA09	D20	LBUSC09	18
19	(-5.2V)	D21	(-5.2V)	19
20	LBUSA10	D22	LBUSC10	20
21	LBUSA11	D23	LBUSC11	21
22	GND	GND	GND	22
23	TTLTRG0*	D24	TTLTRG1*	23
24	TTLTRG2*	D25	TTLTRG3*	24
25	(+5V)	D26	GND	25
26	TTLTRG4*	D27	TTLTRG5*	26
27	TTLTRG6*	D28	TTLTRG7*	27
28	GND	D29	GND	28
29	RSV2	D30	RSV3	29
30	MODID	D31	GND	30
31	GND	GND	(+24V)	31
32	SUMBUS	(+5V)	(-24V)	32

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6.3.3 Connectors K1 and K2 on the front panel.

K1

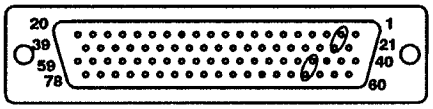


VERSION	ANALOG 1	ANALOG 2
6061A	Outputs 1 to 8	Inputs 1 to 8
6061B	Outputs 1 to 8	Outputs 1 to 8
6061C	Inputs 1 to 8	Inputs 1 to 8
6061D	Not used	Not used

ANALOG 1 group			ANALOG 2 group	
V1L	1		V9L	11
V1H	21		V9H	31
V1L	41		V9L	51
V2L	2		V10L	12
V2H	22		V10H	32
V2L	42		V10L	52
V3L	3		V11L	13
V3H	23		V11H	33
V3L	43		V11L	53
V4L	4		V12L	14
V4H	24		V12H	34
V4L	44		V12L	54
V5L	5		V13L	15
V5H	25		V13H	35
V5L	45		V13L	55
V6L	6		V14L	16
V6H	26		V14H	36
V6L	46		V14L	56
V7L	7		V15L	17
V7H	27		V15H	37
V7L	47		V15L	57
V8L	8		V16L	18
V8H	28		V16H	38
V8L	48		V16L	58

System ground: : 9, 10, 19, 20, 29, 30, 39, 40, 49, 50, 59, 60 to 78

K2



Notes:

- Standard (isolated) :
Channels 1 to 16: Outputs, Channels 17 to 32: Inputs.

- TTL option (Option 02) :
Each channel is programmable as Output or Input. All signals and auxiliary 5V output are referenced to system ground (VxL and GNDiso connected to SYSTEM GROUND).

DIGITAL INPUTS / OUTPUTS							
V1H	1	V9H	9	V17H	17	V25H	45
V1L	21	V9L	29	V17L	37	V25L	65
V2H	2	V10H	10	V18H	18	V26H	46
V2L	22	V10L	30	V18L	38	V26L	66
V3H	3	V11H	11	V19H	19	V27H	47
V3L	23	V11L	31	V19L	39	V27L	67
V4H	4	V12H	12	V20H	40	V28H	48
V4L	24	V12L	32	V20L	60	V28L	68
V5H	5	V13H	13	V21H	41	V29H	49
V5L	25	V13L	33	V21L	61	V29L	69
V6H	6	V14H	14	V22H	42	V30H	50
V6L	26	V14L	34	V22L	62	V30L	70
V7H	7	V15H	15	V23H	43	V31H	51
V7L	27	V15L	35	V23L	63	V31L	71
V8H	8	V16H	16	V24H	44	V32H	52
V8L	28	V16L	36	V24L	64	V32L	72
				+5Viso	56	GNDiso	76
HOLDH	54	HOLDL	74	+5Viso	57	GNDiso	77

System ground:: 20,59,73,75,78
ETRG1 (External Trigger Input): 55
ETRG2 (External Trigger Input): 53
TRGOUT (TTL Trigger Output): 58

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6.3.4 Power supplies.

There are power supplies available on P1 and P2 connectors of the VXI bus:

* +5V (P1:15W, P2: 20W)
* +12V (P1:12W)
* -12V (P1:12W)
* +24V (P2:24W)
* -24V (P2:24W)
* -5.2V (P2:26W)
* -2V (P2:4W)

The DC power of the 6061 is derived from the VXI backplane via HF (high frequency) filters and fuses. The filters are π-type with high HF performance. The internal fuses are security fuses that protect the VXI Mainframe.

The specific supplies used by the 6061 are:

* + 5V : Supply voltage for Microprocessor and all of the logic on Mother board and on all other boards.

* + 24V: Supply voltage for DC/DC converters.

* ± 24V: Supply voltage for power voltage regulator (U1 and U2 on mother board, see page 8-1-24) to produce a regulated ± 15 VDC. These voltages are used to supply a precision Voltage Reference. A potentiometer POT1 on the mother board is used to adjust the required voltage to 10 V (page 8-1-3).

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6.3.5 Bus Buffers and Memory Extension.

The J101 and J102 connectors connect the signals from P1 and P2 connectors of the VXI bus to the Microprocessor board (pages 8-1-9 and 8-1-10). All signals of the 68000 Microprocessor are connected to the J100 connector on the mother board (page 8-1-11).

Three-state buffers are used to amplify the signals to/from the 68000 CPU:

- U13 to U15: buffers for ADDRESS bus (A01 to A23, page 8-1-5).
- U11: buffer for CONTROL bus (RESET*, AS* and R/W*, page 8-1-4)
- U9 and U10: bidirectional buffers for DATA bus (D00 to D15, page 8-1-4). The "enable" signal is controlled by a PLD(U16, page 8-1-21). The "direction" signal is controlled by the bufferized R/W* signal from the 68000 CPU.

CAV4 (page 8-1-5) is a special strap. It is used for Control and Test purposes. If this strap is open, then all buffers will be disabled and all bufferized signals will be in "high impedance" state.

U22 is a Input port that identifies the type of internal sub-assemblies (pages 8-1-21).

Mother board contains a memory extension capacity for future use:

- Four 32 KByte sockets for xC256 RAM (U41 to U44, page 8-1-6)
- Two 128 KByte or 256 KByte sockets for 27C1024/2048 EPROM (U5 and U6, page 8-1-7)

6.3.6 PLDs.

The 6061's mother board contains five 22V10 PLDs (U16 to U19 and U21, page 8-1-21).

U16 provides RAM and EPROM control signals (chip select). This device also generates the necessary DTACK* signal for the 68000 microprocessor when a valid address is provided. The last function provided by U16 is to generate the control signal (ENBDATA) for the Data bus bidirectional buffers.

The address decoding for a "Read/Write from/to Digital port" activity is performed by U17.

The address decoding for a "Read/Write from/to Analog port" activity is performed by UU18 , U19 and U21.

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6.3.7 Voltage Reference.

The 6061's mother board contains a high precision Voltage Reference (U3, page 8-1-3, 10 ppm/°C max.). An operational amplifier (U4, page 8-1-3) mounted in voltage-follower configuration supplies this reference voltage to all digital to analog converters.

POT1 is an adjust potentiometer.

U3 and U4 are powered from a ± 15V sources (U1 and U2, high precision Voltage Regulators).

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6.4 Microprocessor and VXI Interface Board

6.4.1 Description

6.4.2 P100 Microprocessor bus Connector.

6.4.1 Description

The Microprocessor and VXI Interface board accept commands from the VXIbus, interpret the commands and send the required data to the appropriate analog or digital board.

The microprocessor is a Motorola MC68000, U10 operating at 8 MHz. This board also contains ROM, RAM, EEPROM, address decoding, interrupt logic, VXI interface, local bus interface and a counter//timer.

The program memory consists of a U1 (page 8-2-4) EPROM. This device provides 64K by 16 bits of program memory.

The system RAM consists of two devices, U2 and U3 (pages 8-2-4 and 8-2-5). These devices provide 32K by 16 bits of memory.

The EEPROM consists of two devices, U5 and U6 (pages 8-2-5and 8-2-6). These devices provide 8K by 16 bits of Non-volatile memory. U4D prevents false writes to the EEPROM during power up and power down sequences ensuring "non volatile memory" integrity.

General address decoding is performed by a 22V10 PLD, U12 (page 8-2-3). This device provides the necessary logic to map the other devices into the microprocessor memory addressing space. This device also provides the DTACK signal required by the microprocessor. The last function provided by U12 is to detect an interrupt cycle from the states of FC0 and FC1 and drop the VPA line.

Address decoding for VXI registers is performed by a 74F138, U9 (page 8-2-3).

System address decoding is performed by discrete logic devices (page 8-2-9)

The microprocessor is configured so that it can support 8 TTL Trigger lines from the P2 connector of the VXI interface without requiring the polling of devices to determine the interrupt. These eight sources are encoded by U15, U16 and U21 (page 8-2-6).

Counter/Timer function is performed by a MC68230, U19 (page 8-2-6).

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The VXI interface consists of U28, U29, U32, U35 and U37. The logic decoding is performed by a 22V10 PLD, U36 (page 8-2-8).

The Local bus interface consists of discrete logic devices (page 8-2-10). The Lbus interface state machine is implanted in a PAL, U45.

All signals of the 68000 Microprocessor are connected to the P100 connector (P100 will be connected to other buffers and logic devices on the mother board by J100).

6.4.2 P100 Microprocessor bus connector

N°	J100	J100	N°
1	**GND**	A1	2
3	A2	A3	4
5	A4	A5	6
7	A6	A7	8
9	A8	A9	10
11	A10	A11	12
13	A12	A13	14
15	A14	A15	16
17	A16	A17	18
19	A18	A19	20
21	A20	A21	22
23	A22	A23	24
25	**GND**	D15	26
27	D14	D13	28
29	D12	D11	30
31	D10	D9	32
33	D7	D8	34
35	D5	D6	36
37	D3	D4	38
39	D1	D2	40
41	VPA*	D0	42
43	BERR*	VMA*	44
45	**VREGENA***	ECLK	46
47	FC1	FC0	48
49	FC2	XDTACK*	50
51	IRQ4*	IRQ2*	52
53	BG*	**TTLTRIG**	54
55	BR*	BGACK*	56
57	RESET*	HALT*	58
59	R/W*	AS*	60
61	UDS*	LDS*	62
63	**(+5V)**	CPUCLK	64

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6.5 DC/DC CONVERTER

The DC/DC converter receives +24 VDC from the VXI power supply. It supplies 18 independent and isolated sources of ±15 VDC.

- 16 isolated converters are used by Analog Input/Output Boards,
- 1 isolated converter is used to supply power for Option 02 (Digital I/O with TTL compatible level)
- 1 reserved DC/DC converter for maintenance purpose.

The 24 VDC input voltage is filtered by a π-filter that rejects the HF interferences (L1, and C109 to C112, page 8-3-2).

Two PWM Regulators (Pulse Width Modulation) with VMOS Power FET (Field Effect Transistor) are used (MX1, MX2, Q37 and Q38, page 8-3-2). Each PWM regulator system is connected to 3 transformers. In total, six transformers are used (T1 to T6).

Each transformer provides power for 3 output sources (see page 8-3-3 for example).

Each output channel uses two rectifiers and two precision voltage regulators and provides a dual voltage of ±15 VDC.

The DC/DC Converter is shielded by a 6-facets metal box (page 9-9).

The design of the DC/DC Converter assumes an isolation of 1 KV rms from channel to channel, from channel to ground and from channel to input.

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6.6 Digital Inputs/Outputs Board

This board contains:

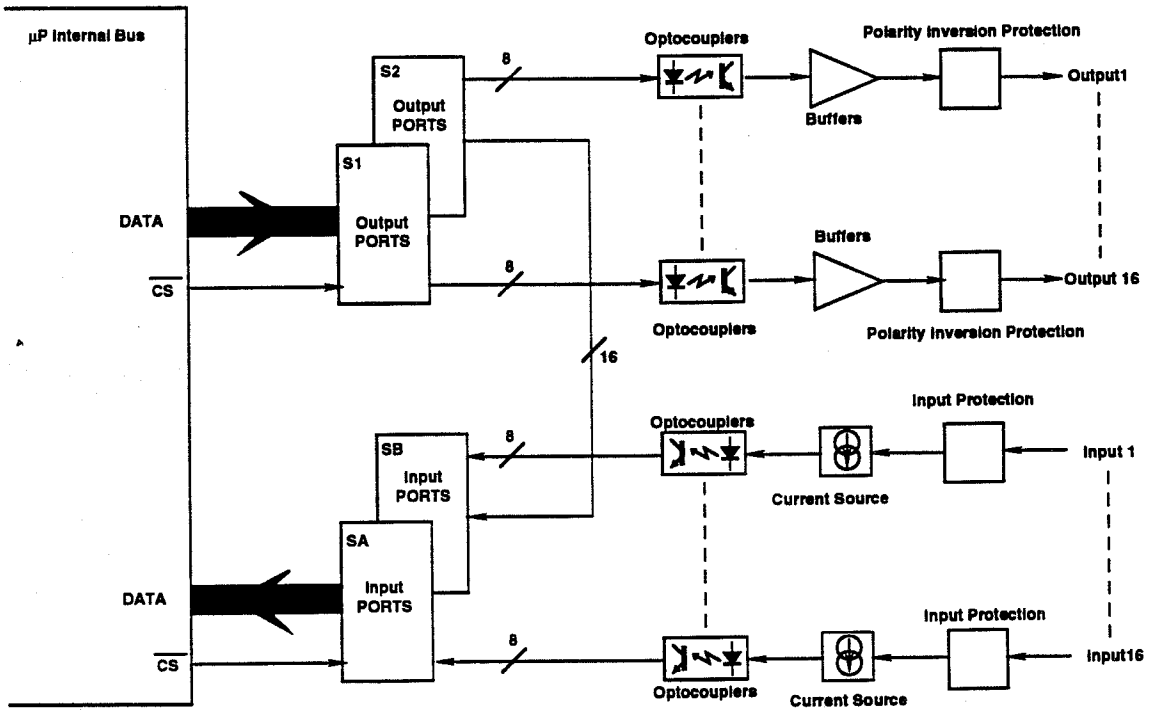
- Four 8 bits output ports with Optocouplers,
- Four 8 bits input ports with Optocouplers and constant current regulators.

This board is connected to the mother board by 3 connectors (page 9-13):

- P103: bufferized data bus from Microprocessor and "chip select" signals from PLD decoders.
- P104 and P105: input/output signals.

Output ports use Integrated circuits type 74ALS574 (U65, U67, U69 and U71, page 8-6-8 to 8-6-11). Optocoupler U1 transfers digital information with isolation to a output transistor T1. The transistor functions on "Open Collector" mode. A Schottky diode D1 protects electronic component against polarity inversion (page 8-6-6).

Input ports use Integrated circuits type 74ALS563 (U66, U68, U70 and U72, page 8-6-8 to 8-6-11). The constant current regulator is formed by the FET T67 and a resistor R2. Optocoupler U2 transfers digital information with isolation to a input transistor T2 (page 8-6-6).



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6.7 Analog Inputs Board

This board contains:

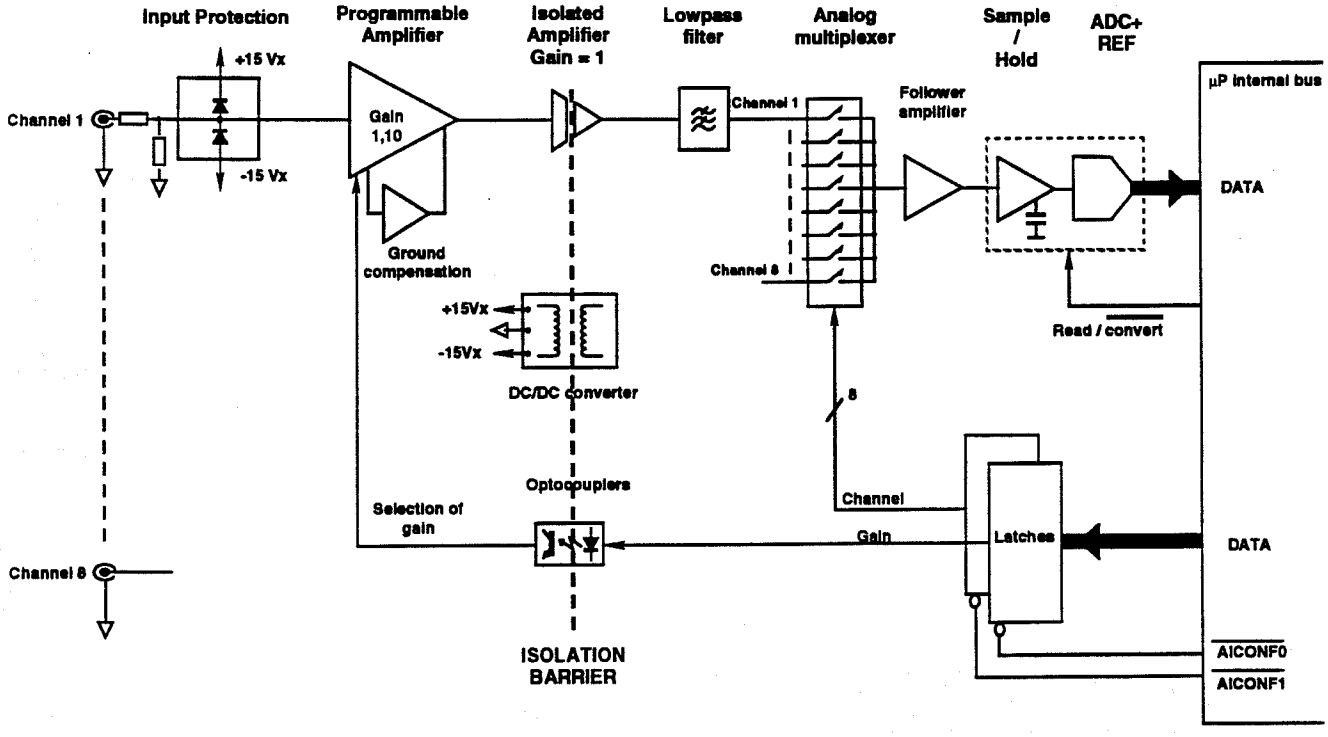
- Eight overvoltage protection / programmable-gain amplifiers (U1, U2 and U5, page 8-4-2),
- Eight isolation amplifiers and active low-pass filters (U3 and U6, page 8-4-2),
- One 8-channel analog multiplexer (U7 and U8, page 8-4-12),
- One 12 bits sampling Analog to Digital Converters (U11, page 8-4-12),
- One 6-range analog system (1, 5 or 10V; unipolar or bipolar; U60 to U63, page 8-4-12),
- Glue logic (page 8-4-10).

This board is connected to the mother board by 3 connectors (page 9-11):

- P300: bufferized data bus from Microprocessor and "chip select" signals from PLD decoders.
- P301 and P302: analog input signals from the K1 connector of the front panel (page 4-4).

Each isolated component group (U1 to U5, page 8-4-2) is powered by one isolated ± 15V power supply from the FS910103 DC/DC Converter.

The 12-bit A/D Converter is a fast sampling - successive approximation converter. The ADC is specified no missing codes, 1/2 LSB integral linearity error over temperature.



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6.8 Analog Outputs Board

This board contains 8 identical channels and 1 common logic.

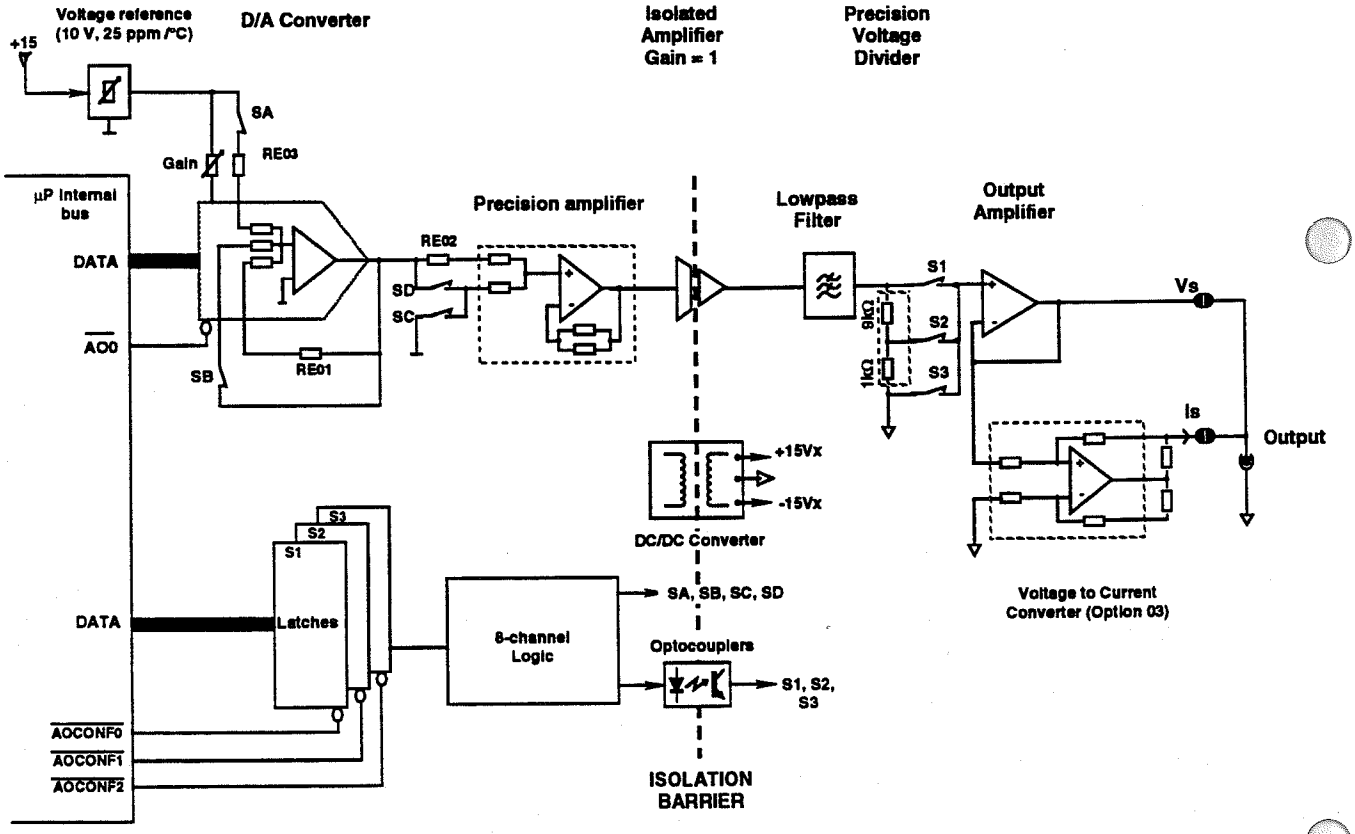
The common electronic contains:
- Three output latches (U1 to U3, page 8-5-26),
- One voltage comparator for auto-test (UG, page 8-5-28).

Each channel contains:
- One microprocessor-compatible 12-bits Digital to Analog Converter (UA, page 8-5-2),
- One 10V or 20V full-scan / unipolar or bipolar selection (SA&SB orSW100, page 8-5-2),
- One precision voltage follower or 1/2 divider (UB, INA105, page 8-5-2),
- Oneisolated amplifier (UC, page 8-5-2),
- One active low-pass filter (UD, page 8-5-2),
- One output voltage follower or 1/10 voltage divider (SW10 and UE, page 8-5-2),
- One voltage to current converter with option 03 (UF, page 8-5-2).

This board is connected to the mother board by 3 connectors (page 9-12):
- P200: bufferized data bus from Microprocessor and "chip select" signals from PLD decoders.
- P201 and P202: analog output signals to the K1 connector of the front panel (page 4-4).

Each isolated component group (UC to UFand SW10, page 8-5-2) is powered by one isolated ± 15V power supply from the FS910103 DC/DC Converter.

The 12-bit D/A Converter is specified monotonic and 1/2 LSB nonlinearity error over temperature.



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July 21th, 1994

VXI MODEL 6060 &6061
Universal Input / Output

SOFTWARE USER MANUAL

Description of commands

Firmware version ≥ 3.02

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Option 02 (TTL Digital I/Os), Additionnal Commands

Since all 4 Digital I/O ports can be configured as Input or Output, following commands are available for TTL option :

SOURce	:DOPort3	[:DATA]	
	|:DOPort4	|:HIGH	
		|:LOW	
		|:TRACe	[:NAME]
			|:INDIce?
			|:COUNt
MEASure	:DIPort1	[:DATA]?	
	|:DIPort2	|:HIGH?	
		|:LOW?	
SENse	:DIPort1	:TRACe	[:NAME]
	|:DIPort2		|:INDIce?
			|:COUNt
TRIGger	:DOPort3	:STEP	[:IMMediate]
	|:DOPort4		|:ECOunt
	|:DIPort1		
	|:DIPort2		

No further explanation is necessary for these new commands since there are described for the other ports in the manual.

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Really new commands :

OUTPut:DOGLobal[:STATe] <ON|OFF>, <channel_list>

Description : Allows to set the configuration of TTL digital I/Os. If a channel is configured as an Input, any further Source command concerning it will be ineffective.

Parameters :

<ON|OFF> : If "ON", the listed channels are configured as Outputs.
<channel_list> : from 1 to 32.

Initialization : All 32 digital I/Os are configured as Inputs (OFF).

Example :

"outp:dogl on, (@1:16)" configures I/Os 1 to 16 as Outputs.

OUTPut:DOPort1[:STATe] <ON|OFF>, <channel_list>
OUTPut:DOPort2[:STATe] <ON|OFF>, <channel_list>
OUTPut:DOPort3[:STATe] <ON|OFF>, <channel_list>
OUTPut:DOPort4[:STATe] <ON|OFF>, <channel_list>

Description : These commands are identical to the previous one, except that they only concern one digital I/O port, also the channels are numbered from 1 to 8.

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6061 OPTION 03
CURRENT ANALOG OUTPUTS

• "**VOLTage**" mnemonic must be **replaced** by "**CURRent**" in any SCPI command.

Ranges are as follows :

1 : 0-2 mA
3 : 0-10 mA
5 : 0-20 mA

Ranges 2,4 and 6 are not allowed.

• For the "[SOURce]:CURRent[:**LEVel**]" command the **unit** is **1 mA.**

Examples :

"CURR:RANG 3,(@5:8)" for a 0-10 mA range on Analog Output channels 5 to 8.

"CURR 5.1,(@5); CURR 3.33,(@7)" for 5.1 mA on channel 5 and 3.33 mA on channel 7.

"CURR:TRAC Trace_1,(@1)" associates "Trace_1" with Output Channel 1.

∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞

Here is the list of all the specific commands of the 6061 option 03 :

[SOURce]	:**CURRent**	[:LEVel] :DATA :RANGe	
		:TRACe	[:NAME] :INDice? :COUNt
TRIGger	:**CURRent**	:STEP	[:IMMediate] :ECOunt

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I) Summary of SCPI syntax.

I.1) Conventions used in description

- An expression contained within "[]" is optional.

Example : [SOURce]:VOLTage[:LEVel] means that this command can be written

"source:voltage:level", "volt:lev", "sour:volt", "volt", etc.....

- The symbol "|" is an "OR" and indicates a choice.

Example : "<ON|OFF>"indicates that in this case, both ON and OFF are valid.

- An expression contained within "{ }" is optional and can be repeated.

•Example : <0|1>{,<0|1>} can be used to described "0,1,0,0,0,1,0"

I.2) General Rules for syntax

- The spaces (<White Space Character>) can be inserted at will between commands and parameters or between parameters but not within a command nor a parameter (string type).

Example : "mea s:digl?"is not correct but " inp:digl:state ON, (@ 1 ,2) ; " is correct.

- The capital letters and the small letters can be used indifferently for the commands and parameters of string type.

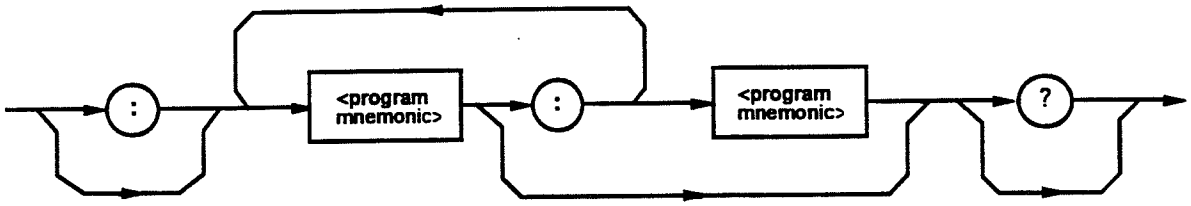
Example : "MeaS:VOlt:DatA? (@1:5)" and "Form BIn" are correct.

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I.3) Description of commands (Program Header)

- An SCPI command (Program header) is made up of key words (<program mnemonic>) separated by ":" and eventually finished by a question mark if a reply is expected (Query form), the command is separated from the first parameter (if one exists) by one or several spaces (or more precisely"<White Space Character>"conforming to IEEE 488.2)



Example : "input:diglobal:state" or"measure:volt:level?"

- A key word making up a command can be used just as well in a short form (capital letters in the description) as in a long form (capital and small letters), the rule being that the short form is made up of the first four characters of the long form, the last character being a vowel only if the long form has four characters or less.

Example : the key word SOURce can be written "source" (long form) or "sour" (short form), "LEVel" can be written "lev" or "level", "DATA" is identical under the two forms.

- In the case of a key word with a channel rating, it will be associated just as well with the long form as with the short form.

Example : the short form of "DOPort1" is "dop1".

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I.4) Parameters and Separators

- The parameters are separated by commas",", a complete message(<program message>:command + associated parameters) is ended either by an EOI, either by a <NL>(Line Feed:code ASCII 10,#H0A), either by a semi-colon, in this case several messages can be joined together on the same line.

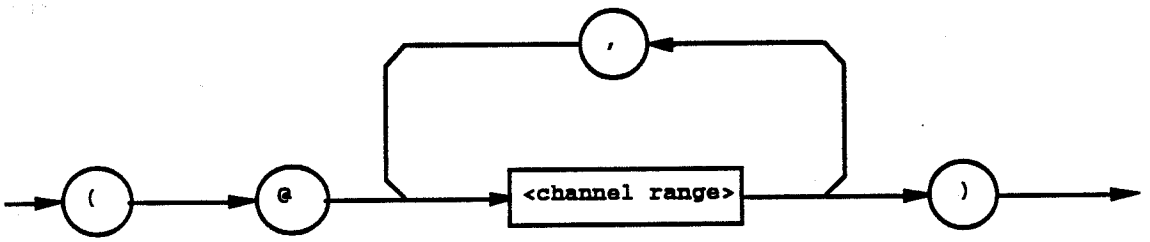
Example : "sens:volt:rang 1,(@10:13,16);meas:volt? (@10)"

- These same rules are also valid for parameters of string type (<char_data>).

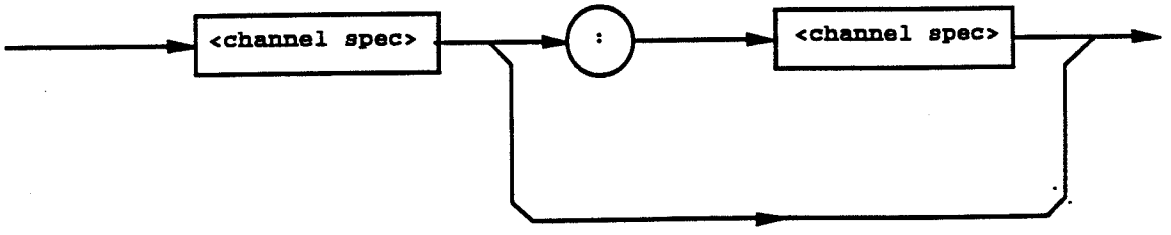
Example : the short form of the "HEXadecimal" parameter is "hex".

I.5) Channel List

- A "<channel_ list>" is a list of channels to which the command is applied, the syntax is as follows:



Where <channel range> is defined as



Example : "volt 2.5, (@4:7, 11, 13:16)" generates 2.5 V on the channels 4 to 7, 11 and 13 to 16.

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I.6) Linked commands

- When the commands are linked on the same line and separated by ";" certain rules allow the description of commands to be reduced in a tree structure. In effect, the first command of the line causes branching out from the root level, the following commands may omit the levels already described by the previous command.

Example :

"**trig:dop1:start:count 2 ; sour bus**" is equivalent to
"**trig:dop1:start:count 2 ; trig:dop1:start:sour bus**"

- It is possible to go directly from the root level by putting a ":" in front of the first keyword.

Example :

"**volt 2,(@1) ; trace t_1,1,2,3,4**" will be interpreted as
"volt 2,(@1) ; volt:trace t_1,1,2,3,4" and will generate an error message (too many parameters for the second command) but
"**volt 2,(@1) ; :trace t_1,1,2,3,4**" is correct.

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II) Description of Inputs/Outputs

II.1) Keywords

DOGLobal : "Digital Output Global" concerns the commands which can simultaneously reach all the digital outputs (within the 32 I/O).

DIGLobal: "Digital Input Global" concerns the commands which can simultaneously reach all the digital inputs (within the 32 I/O).

DOPort1, DOPort2 : "Digital Output Port" concerns the commands which can simultaneously reach eight outputs of a port of 8 digital I/O .

DIPort3, DIPort4 : "Digital Input Port"concerns the commands which can simultaneously reach eight inputs of a port of 8 digital I/O.

VOLTage: concerns the commands of analog Inputs and Outputs. The analog I/O are numbered from 1 to 16.

DATA: is used when the value sent or read on the analog I/O is represented by an Integer number without unit.

LEVel: is used when the value sent or read is exactly the same as the tension or current of the present range.

II.2) Configuration

- The software automatically recognizes the configuration (analog input or output, tension or current, digital I/O TTL or Open Collector) of the module and adapts the error messages to this configuration.

  This documentation is written for a **standard configuration**:

16 Digital outputs open collector : from 1 to 16

16 Digital inputs : from 17 to 32

8 Analog outputs Tension : from 1 to 8

8 Analog inputs High Impedance: from 9 to 16

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II.3) Ranges

For the analog I/O, the ranges are categorized by number:

Range		STANDARD	OPTION 01	OPTION 03
1	:	0 - 1 V	0-1.6V	0-2 mA
2	:	± 1V	±1.6V	Not available
3	:	0 - 5 V	0-8V	0-10 mA
4	:	± 5 V	±8V	Not available
5	:	0 - 10 V	0-16V	0-20 mA
6	:	± 10 V	±16V	Not available

II.4) Direct writing and reading on I/O

- The keyword **SOURce** precedes all the commands concerning the Outputs.
- The keyword **SENse** precedes all the commands which concern the configuration (range, trace,...) of the inputs.
- The keyword **MEASure** precedes all the direct commands of input measurement.
- All the commands which do not refer to Triggers are interpreted and carried out immediately.

Examples:

"source:volt 1,(@1:4)" generates 1V on the analog outputs 1 to 4.
"source:dop1 0" puts the digital outputs 1 to 8 to earth.
"measure:volt? (@9,11)" reads the analog inputs 9 and 11, the user can therefore read the values in the reader buffer module.

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II.5) Reading andWriting from memory on I/O

II.5.a) Principles of operation

- For the **Outputs** :

The values to be written on the outputs are remotely loaded in the memory by the user,via the bus, then written automatically in time with a soft trigger, an internal timer or a TTLtrig line on the specified outputs.

- For the **Inputs** :

The values read at the specified Inputs are stocked automatically in the memory, at a trigger rhythm chosen by the user, who can then transfer the values to the bus to read them.

II.5.b) Traces

- Traces are **memory zones** with length and format defined by the user and two functions :

1) to contain **raw data** which the user, via the bus, will control remotely; data intended to be **written at an output channel,** at the trigger rhythm.

2) to receive **data read at the Input channel** at the trigger rhythm, data stocked in the memory is therefore read finally by the user via the bus.

- A trace is an independent entity which can be handled like a data file, it has a name defined by the user, it is not linked to any particular I/O channel when it's created; the user runs himself the exchanges between traces and I/O channels, the only restraint being the format of the data which must be the same for the two entities. A trace can be linked simultaneously for example with several output channels or contain data read on an input channel and which can be then written on an output channel, etc...

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II.5.c) Triggers

- A trigger is in fact a combination of three triggers :

1) a trigger **STARt** which launches the exchanges between the I/O channel and the associated TRACe, the trigger STARt is set up by the command INITiate.

2) a trigger **STEP** which runs the exchanges between the I/O channels and the TRACes, this trigger applies only after the trigger STARt has been ended.

3) a trigger **STOP** which stops the exchanges between the I/O channels and the TRACes, this trigger applies only after the trigger STARt has been ended.

- The command **ABORt** totally stops the trigger cycle launched by **INITiate**, this cycle can only be relaunched by an other INITiate command.

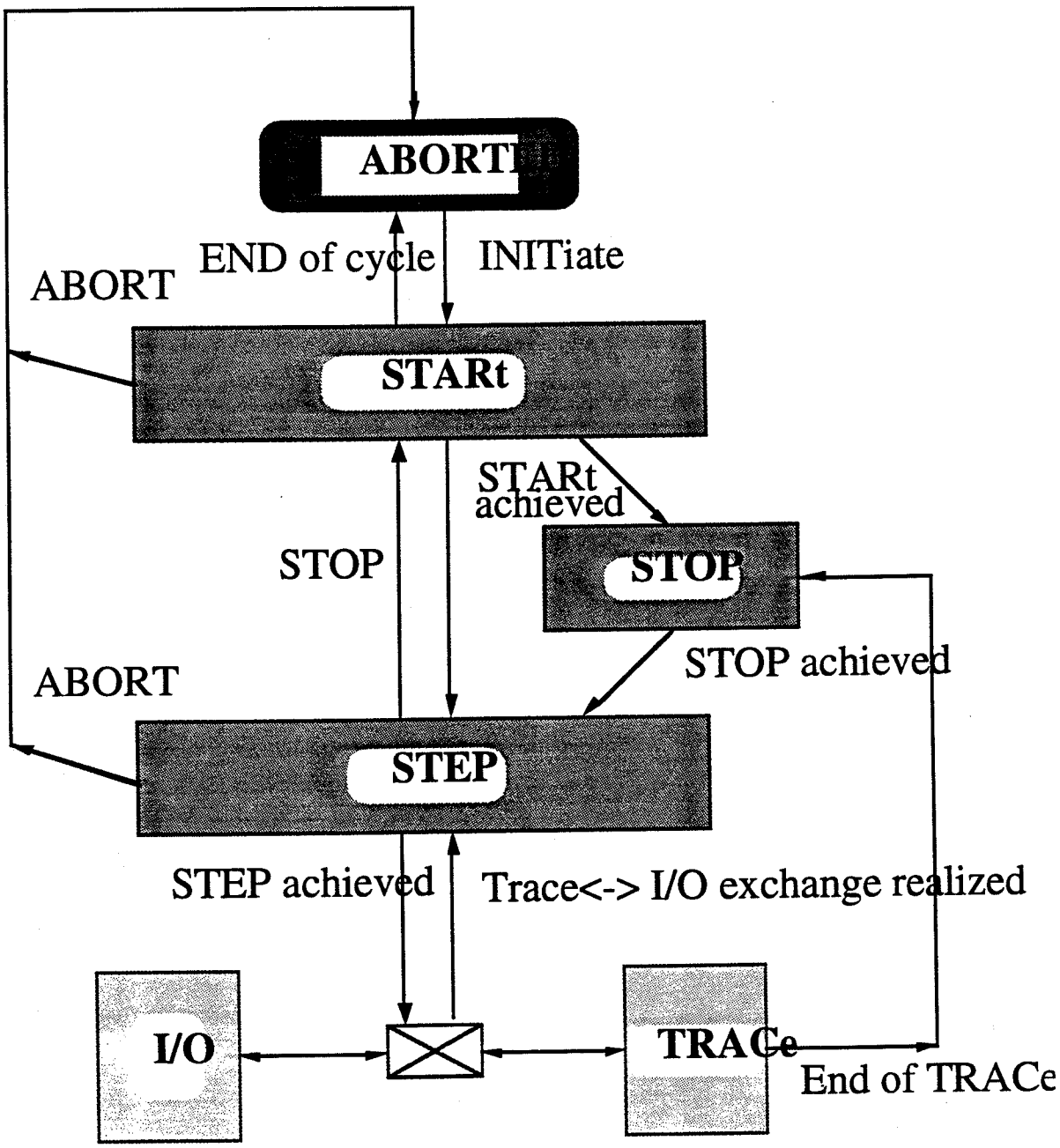
- For each TRACe the **DATA pointer** is set up at the beginning of the TRACe the first time that the process enters in STARt, then it is incremented after each exchange with I/O channels. The loop back at the beginning of the TRACe occurs automatically after reading or writing the last data, at this time an event EOT (End Of Trace) is generated and can be used as SOURce by the STOP trigger.

- The diagram of the following page summarizes a trigger cycle, the three following diagrams summarize the functioning of the three triggers STARt, STOP and STEP.

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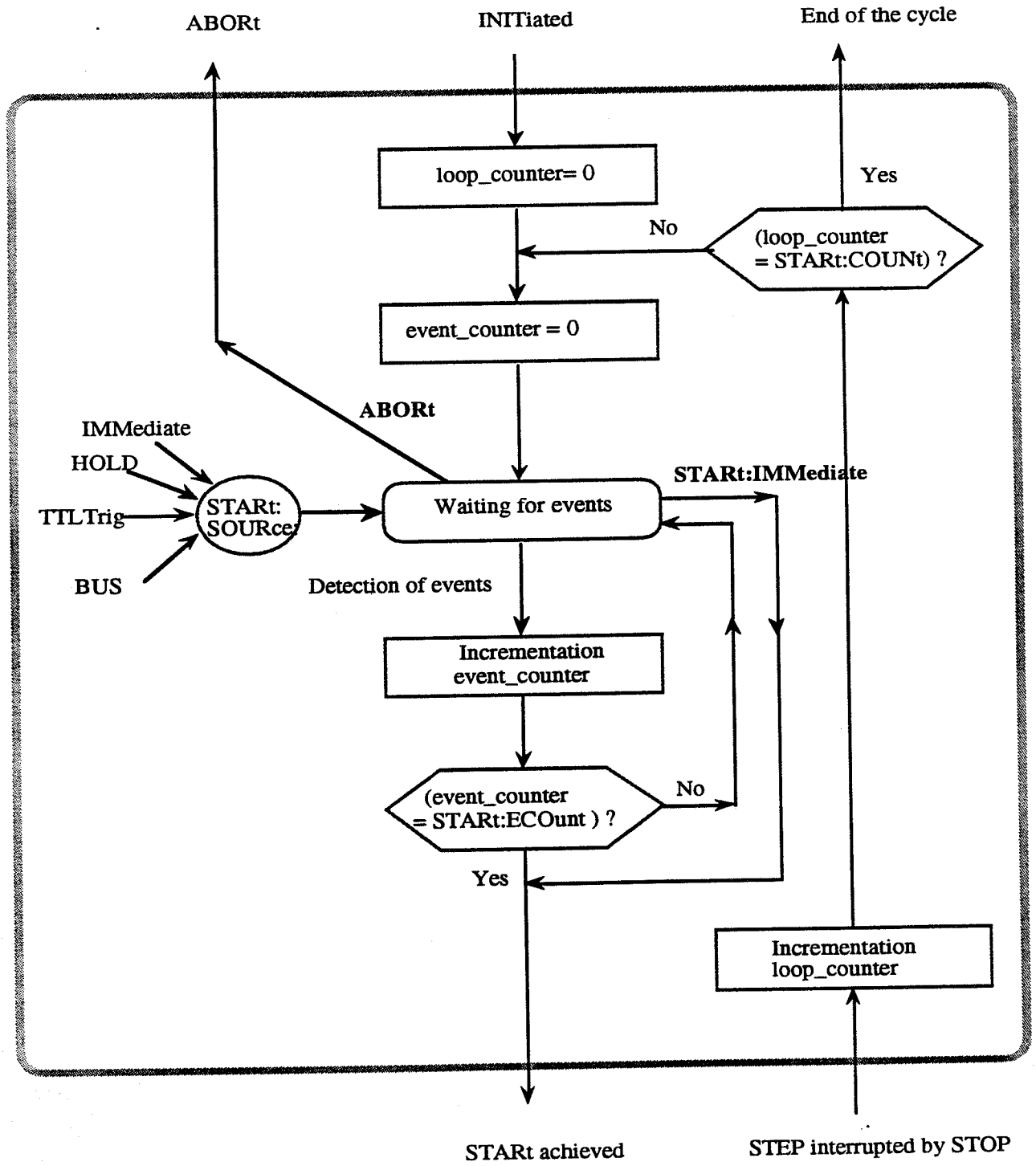
SYNOPTIC DIAGRAM OF TRIGGER CYCLE



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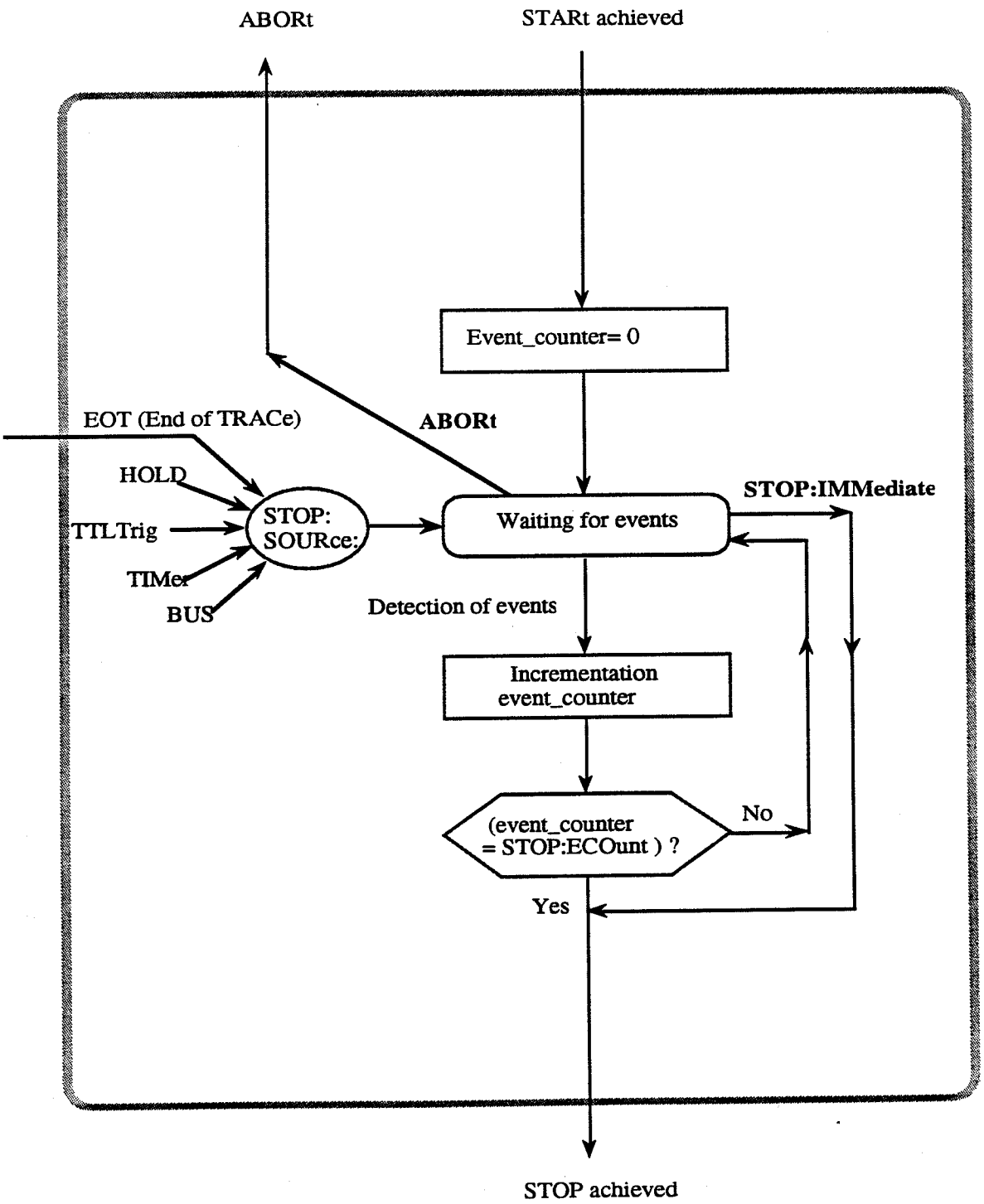
SYNOPTIC DIAGRAM OF START TRIGGER



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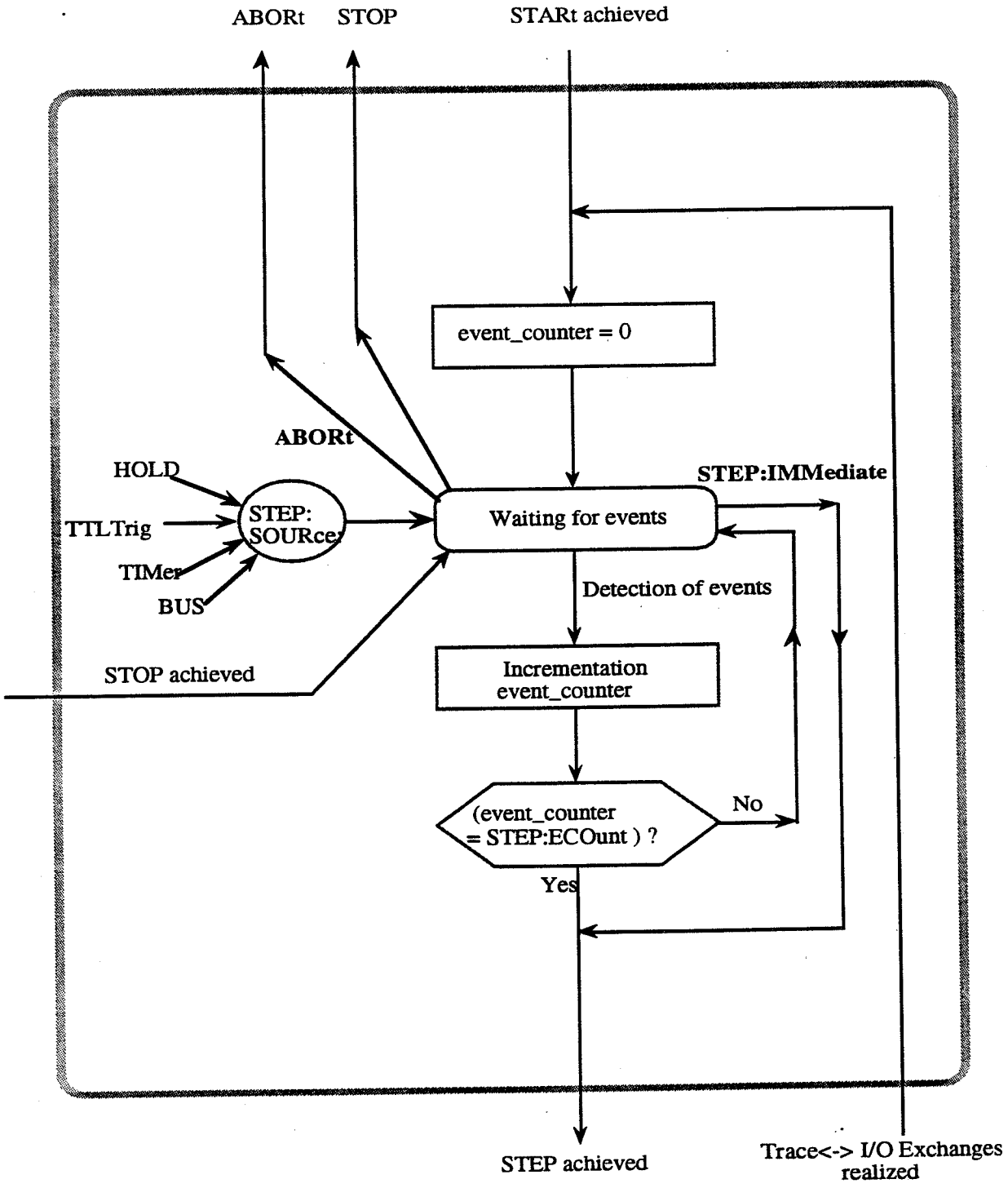
SYNOPTIC DIAGRAM OF STOP TRIGGER



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SYNOPTIC DIAGRAM OF STEP TRIGGER



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III) SUMMARY OF COMMANDS

SCPI (those commands preceded by a "»" are SCPI 1991.0 confirmed commands) :

»FORMat			
»TRACe	[:DATA]		
»	|:CATalog?		
»	|:DEFine		
»	|:DELete	[:NAME]	
»		:ALL	
»	|:POINts		
»	|:FREE?		
	|:HANDle?		
[SOURce]	:DOGLobal	[:DATA]	
	|:DOPort1	|:HIGH	
	|:DOPort2	|:LOW	
»[SOURce]	:VOLTage	[:LEVel]	
		|:DATA	
»		|:RANGe	
»SENSE	:VOLTage	:RANGe	
MEASure	:DIGLobal	[:DATA]?	
	|:DIPort3	|:HIGH?	
	|:DIPort4	|:LOW?	
»MEASure	:VOLTage	[:LEVEL]?	
		|:DATA?	
SOURce	:DOPort1	:TRACe	[:NAME]
	|:DOPort2		|:INDice?
	|:VOLTage		|:COUNt
SENSe	:DIPort3	:TRACe	[:NAME]
	|:DIPort4		|:INDice?
	|:VOLTage		|:COUNt

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TRIGger	:TIMer	[:STATe] |:PERiod	
	:EOT	[:STATe] :NAME	
	:TTLTrg |:ETRG1 |:ETRG2 |:BUS	[:STATe]	
	[:GLOBal]	[:STARt]	[:IMMediate] |:COUNt |:ECOunt |:SOURce
		:STOP	[:IMMediate] |:ECOunt |:SOURce
		:STEP	[:IMMediate] |:SOURce
	:DOPort1 |:DOPort2 |:DIPort3 |:DIPort4 |:VOLTage	:STEP	[:IMMediate] |:ECOunt
INITiate |ABORt	[:GLOBal]		
OUTPut	:VINTerrupt |:TTLTrg	:SEQuence<n>	[:STATe] |:ECOunt |:SOURce
	:VINTerrupt	:SEQuence<n>	:EVENt
	:TTLTrg	:SEQuence<n>	:LINE
FETCh	:VINTerrupt |:TTLTrg	:SEQuence<n>	[:DATA]?

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»SYSTem	:PRESet		
»	|:VERSion?		
»	|:ERRor?		
»STATus	:OPEration	[:EVENt]?	
»		|:CONDition?	
»		|:ENABle	
		:TRIGger	[:EVENt]?
			|:CONDition?
			|:ENABle
»	:PRESet		

IEEE 488.2 :

*RST
*IDN?
*OPT?
*TST?
*CLS
*ESE
*ESE?
*ESR?
*OPC
*OPC?
*SRE
*SRE?
*STB?
*WAI
*TRG

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IV) Detailed description of commands

IV.1) Format of exchanged data

FORMat <char_data>

Description : defines the present format of certain exchanged data (Integer).The format can be forced independently of the usual format by using the prefixes "#A" for ASCii, "#H"for HEXadecimal and "#B" for BINary. Each parameter concerned by this command and without prefix will be considered as described within this format. Each response concerned by this command will be described, without a prefix, in this format.

Parameters : **<char_data>** can be "ASCii", "HEXadecimal" or "BINary".

ASCii : base 10, decimal.
HEXadecimal : base 16, hexadecimal
BINary : base 2, binary.

Initialization : ASCii

Example : "form hex" will set the format by default in hexadecimal, so that "dogl 100" will have the same effect as "dogl #H100" or "dogl #A256" and "dogl?" will return "100".

•Query form :

FORMat? ==><char_data>

In the rest of this document:
the usual FORMat applies to each parameter preceded by a "*".

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IV.2) Setting digital outputs

[SOURce]:DOGLobal[:DATA] *<num_value>[, *<mask]

Description : Defines the state of digital outputs, this command does not affect the inputs.

Parameters :

<num_value> is an Integer value from 0 to #HFFFF (0 to 65535), the LSB corresponds to the digital output 1.

<mask> allows the command to affect only one part of the outputs; in order to have one output to be affected by <num_value>, the corresponding bit of <mask> must be set to 1, <mask> can therefore take Integer values from 0 to #HFFFF, if no mask is specified, all the outputs are affected by <num_value> (this is equivalent to <mask>=#HFFFF).

Initialization : the 16 digital outputs are in a high state (open collector).

Examples :
"DOGL#HFF00" sets the outputs 1 to 8 at the low state, 9 to 16 at the high state.
"DOGL 0,#HFF00" sets the outputs 9 to 16 at the low state, and keeps the others at their initial state.

•Query form :

[SOURce]:DOGLobal[:DATA]? ==>*<num_value>

Response : <num_value> (0 à #HFFFF) represents the effective instruction of the outputs.

Example : "FORM HEX ; DOGL? ==> 0100" the output 9 is at the high state, the others at the low state.

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[SOURce]:DOPort1[:DATA] *<num_value>[, *<mask>]
[SOURce]:DOPort2[:DATA] *<num_value>[, *<mask>]

Description : these commands are identical to the preceding one but concern only a port of 8 I/O.

Parameters : **<num_value>** and **<mask>** can take Integer values from 0 to #HFF.

Examples :
"DOP1 #H55" sets the outputs 1, 3, 5, 7 of port 1 at the high state and 2, 4, 6, 8 at the low state.
"DOP2 0, #H30" sets the outputs 5 and 6 of port 2 (then 13 and 14)at the low state.
"DOP1 #B11110000" sets the outputs 1 to 4 of port 1 at the low state, 5 to 8 at the high state.
"FORM BIN ; DOP1 1010, 1100" sets the output 3 of port 1 at the low state, the output 4 at the high state, the other outputs keep their initial states.

•Query form :

[SOURce]:DOPort1[:DATA]? ==> *<num_value>
[SOURce]:DOPort2[:DATA]? ==> *<num_value>

Example : "FORM ASC ; DOP2?" => "36" the inputs 3 and 6 of port 2 (then 11 and 13) are at the high state, the others at the low state.

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[SOURce]:DOGLobal:HIGH <channel_list>
[SOURce]:DOGLobal:LOW <channel_list>

Description : These commands offer an alternative to the preceding commands, for some applications, by describing each digital I/O as separated "channel".

Example : "DOGL:HIGH (@5:10)" sets the outputs 5 to 10 at the high state.

•Query form :

[SOURce]:DOGLobal:HIGH? <channel_list> ==> <0|1>{, <0|1>}
[SOURce]:DOGLobal:LOW? <channel_list> ==> <0|1>{, <0|1>}

Response : 1 if the corresponding output is in the specified state (HIGH or LOW), 0 at the contrary.

Examples :
"DOGL:LOW? (@6,15)" ==> "0,1" the output 6 is at the high state, the output 15 at the low state.
"DOGL:HIGH (@9:12)" ==> "1,1,1" the outputs 9 and 12 are at the high state.

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[SOURce]:DOPort1:HIGH <channel_list>
[SOURce]:DOPort2:HIGH <channel_list>
[SOURce]:DOPort1:LOW <channel_list>
[SOURce]:DOPort2:LOW <channel_list>

Description : Identical to the commands above, except that it works only on a port of 8 digital I/O.

Examples :
"DOP2:LOW (@3:6, 8)" sets the outputs 3 to 6 and 8 of port 2, then 11 to 14 and 16 at the low state.

•Query form :

[SOURce]:DOPort1:HIGH? <channel_list> ==> <0|1>{, <0|1>}
[SOURce]:DOPort2:HIGH? <channel_list> ==> <0|1>{, <0|1>}
[SOURce]:DOPort1:LOW? <channel_list> ==> <0|1>{, <0|1>}
[SOURce]:DOPort2:LOW? <channel_list> ==> <0|1>{, <0|1>}

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MEASure:DIGLobal[:DATA]? ==> *<num_value>

Description : Measurement of the digital inputs.

Response : **<num_value>** is an integer from 0 to #HFFFF, the LSB corresponds to the input 17.

Example :
"FORM HEX ; MEAS:DIGL?" ==> "FF00" the inputs 25 to 32 are at the high state, the others (17 to 23) at the low state.
"MEAS:DIGL?" ==> "3840" (if FORMat = ASC) the inputs 25 to 28 are at the high state, the others at the low state.

MEASure:DIPort3[:DATA]? ==> *<num_value>
MEASure:DIPort4[:DATA]? ==> *<num_value>

Description : similar to the above commands except that it concerns only a port of 8 I/O.

Example :
"FORM HEX ; MEAS:DIP3?" ==> "61" the inputs 1, 6 and 7 of port 3 (then 17, 22 and 23) are at the high state, the others at the low state.
"FORM BIN ; MEAS:DIP4?" ==> "1100000"the inputs 6 and 7 of port 4 (then 22 and 23) are at the high state, the others at low state.

MEASure:DIGLobal:HIGH? <channel_list> ==> <0|1>{, <0|1>}

Description : Measures immediately the state of the digital inputs specified in the "channel-list".

Response : A succession of "0" (low state) and of "1" (high state) separated by commas corresponding to the states of specified inputs and in the "channel_list" order.

Example : "MEAS:DIGL:HIGH? (@25,27:30)" ==> "0,1,1,1,0" the inputs 25 and 30 are at the low state, the inputs 27, 28 and 29 at the high state.

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MEASure:DIGLobal:LOW? <channel_list> ==> <0|1>{, <0|1>}

__Description__ : Similar to the preceding command except that a "1" is resent for the low states and a "0" for the high states.

MEASure:DIPort3:HIGH? <channel_list> ==> <0|1> {, <0|1>}
MEASure:DIPort4:HIGH? <channel_list> ==> <0|1> {, <0|1>}

__Description__ : Measures immediately the state of digital inputs specified in the "channel_list" for the port of specified digital I/O.

__Example__ :
"MEAS:DIP4:HIGH? (@2,5,8)" ==> "0,0,1" the inputs 2 and 5 of port 4 (then 26 and 29) are at the low state, the input 8 of port 4 (then 32) at the high state.

MEASure:DIPort3:LOW? <channel_list> ==> <0|1> {, <0|1>}
MEASure:DIPort4:LOW? <channel_list> ==> <0|1> {, <0|1>}

__Description__ : Similar to the preceding command except that a "1" is resent for the low states and a "0" for the high states.

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IV.4) Setting analog output ranges

[SOURce]:VOLTage:RANGe <num_value>, <channel_list>

Description : This command sets the range of the outputs specified in the "channel_list". **Each output concerned by the change in the range is systematically set to OV.**

Parameters : **<num_value>** is an Integer value from 1 to 6.

Initialization : range 1 (0-1V) for the analog outputs.

Example : "VOLT:RANG 3,(@1:8)" sets the range of outputs 1 to 8 to (0-5 V), after this command the 8 outputs are set to 0V whatever their initial states.

•Query form :

[SOURce]:VOLTage:RANGe? <channel_list> ==> <num_value>{, <num_value>}

Response : the ranges of the channels of specified outputs in the <channel_list> order.

IV.5) Commands for setting analog Output voltages

[SOURce]:VOLTage[:LEVel] <num_value>, <channel_list>

Description : sets the voltage of analog outputs listed in the "channel_list".

Parameters : **<num_value>** gives the value of the voltage expressed in VOLT in the format <NRf> of the standard IEEE 488.2, if the value is over the high or low limits of the usual range, the corresponding limit is applied.

Initialization : 0V on the 8 analog outputs.

Example :
"VOLT 2.55, (@1,5:7)" sets to 2.55V the analog outputs 1, 5, 6 and 7.
"VOLT 10.0E-3, (@3)" sets to 10 mV the analog output 3.

•Query form :

[SOURce]:VOLTage[:LEVel]? <channel_list> ==> <num_value>{, <num_value>}

Response : requested output voltages specified in the <channel_list> order.

Example : "VOLT? (@5:7)" ==> "2.5000,1.0000,-9.60000" the output voltages are 5: 2.5V, 6: 1V and 7: 9.6V.

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[SOURce]:VOLTage:DATA *<num_value>, <channel_list>

Description : sets the voltage of analog outputs listed in the "channel_list".

Parameters : contrary to the commands of LEVel type, this command allows the digital -> analog converters of analog outputs to be directly controlled, **<num_value>** is an integer value from 0 to #HFFF (0 to 4095), the resulting voltage depends on the chosen range.

Example :

"VOLT:DATA #H800,(@1:8)" sets the output voltage in the middle of the range for the outputs 1 to 8.

"VOLT:RANG 5,(@1) ; FORM ASC ; VOLT:DATA 1024,(@1)" sets the output voltage of the channel 1 at 2.5V.

•Query form:

[SOURce]:VOLTage:DATA? <channel_list> ==> *<num_value>{, *<num_value>}

Response : the voltages of the output channels specified in the <channel_list> order.

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IV.6) Setting analog Input ranges

SENSe:VOLTage:RANGe <num_value>, <channel_list>

Description : This command sets the range of analog inputs listed in the "channel_list".

Parameters : **<num_value>** is an Integer value from 1 to 6.

Initialization : range 6 (±10V) for the 8 analog inputs.

•Query form :

SENSe:VOLTage:RANGe? <channel_list> ==> <num_value>{, <num_value>}

Response : the ranges of input channels listed in the <channel_list>.

IV.7) Measuring analog Input voltages

MEASure:VOLTage[:LEVel]? <channel_list> ==> <num_value>{,<num_value>}

Description : immediately measures the voltage of the analog inputs listed in the "channel-list".

Response : The voltage values in Volt with format <NRf>, separated by commas in the order of the "channel_list".

Example :
"MEAS:VOLT? (@9,13)" ==> "7.324, 0.4883"the voltage measured on the input 9 is 7.324 V and 488.3 m V on input 13.

MEASure:VOLTage:DATA? <channel_list> ==>*<num_value>{,*<num_value>}

Description : Identical to the above command except that the value read is not converted into VOLT according to the current range but corresponds to the raw data (0 to #HFFF) read at the output of the analog->digital converter.

Example :

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"SENS:VOLT:RANG 6,(@9:16) ; FORM ASC ; MEAS:VOLT:DATA? (@9:10)" ==> "1024, 3072"
then analog input 9 voltage is -5.0V and analog input 10 voltage is +5.0V.

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TRACe:DEFine <trace_name_1>, (<trace_name_2>|<n_points>)[, <format>]

Description : Opening of a TRACe, a memory zone is put aside, it could contain data coming from measurements on Input channels or data stored by user in order to be transfered to Output channels.

Parameters :

<trace_name_1> is the name of the trace to be created (12 characters max, indifferently capitals and small letters).

<trace_name_2> is the name of an already existing trace, <trace_name_1> will be then a true copy (size and data) of <trace_name_2>.
OR

<n_points> is the amount of data of format "<format>" that is reserved for <trace_name_1>.
<format> is the data format, INTeger8 or INTeger16, if omitted the format is INTeger16.

Examples :
"TRAC:DEF T_1, 100, INT8" opens the TRACe "t_1" which can contain 100 data in INTeger8 (that is to say 100 bytes of memory).
"TRAC:DEF TRACE_16,1000" opens the TRACe "TRACE_16" which can contain 1000 data of INTeger16 format (that is to say 16 kbytes of memory).
"TRAC:DEF T_2, T_1" opens the TRACe "T_2" which is a true copy of "T_1".

•no query form

TRACe:POINts <trace_name>, <n_points>

Description : Modifies the amount and the format of the data reserved for the specified TRACe.

Parameters :
<trace_name> is the name of an existing TRACe.
<n_points> is the new amount of data reserved for the TRACe.

Example :
"TRAC:DEF T_1,200" opens a TRACe "T_1" which can contain 200 data of format INTeger16.
"TRAC:POIN T_1,10" modifies the memory space reserved for "T_1"so it can contain 10 data of format INTeger16.

•query form :

TRACe:POINts? <trace_name> ==> <n_points>, <format>

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TRACe:CATalog? ==> [<trace_name>]{, <trace_name>}

Description : Returns the list of the existing TRACes separated by commas.

Examples :
"TRAC:CAT?" ==> "T_1, TRACE_16, T_2"

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TRACe:FREE? ==> <bytes_available>, <bytes_in_use>

Description : Returns the available memory space and the memory space used in numbers of octets.

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TRACe:DELete[:NAME] <trace_name>

Description : Deletes the TRACe "<trace_name>" of the TRACe list and releases the memory space reserved for <trace_name> data.

Examples : "TRAC:DEL T_1" deletes the TRACe "T_1" of the list.

•No query form.

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TRACe:DELete:ALL

Description : Deletes all the TRACes of the list and releases the memory space reserved for TRACe data.

•No query form.

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TRACe[:DATA] <t_name>, (<block>|*<num_value>{ ,*<num_value>})

Description : Fills up the memory zone reserved for TRACe "<trace_name>" with listed data, data can be transfered either as a list of ASCII data separated by commas or as a block of raw integer data.

Parameters :

<t_name> is the name of an existing TRACe.

<block> is a block of raw integers (INTeger8 or INTeger16 according to the TRACe format), the block is identified by "**#0**" prefixe, then data follow byte after byte, in case of an INTeger16 format upper byte is first.

INTeger8 : "#0<data1><data2><data3>....<dataN>"
INTeger16 : "#0<MSbyte.data1><LSbyte.data1><MSbyte.data2>...<MSbyte.dataN><LSbyte.dataN>"

<num_value> is an Integer value compatible with "<trace_name>" data size.

Examples :

"TRAC:DEF T_1,6,INT8" opens "T_1" for containing 6 INTeger8 data.
"FORM HEX ; TRAC T_1,AA,55,AA,55,AA,55" fills up "T_1" alternately with "#HAA" and "#H55".

"TRAC:DEF SINUS,1024" opens "SINUS" for containing 1024 INTeger16 data
"TRAC SINUS,#0<><><><><><><><><><><><>...<><><>" fills up "SINUS" with raw data.

•query form :

TRACe[:DATA]? <t_name>[,<fmt>] ==> (<block>|*<num_value>{, *<num_value>})

<fmt> is the format of the expected data

if this parameter is given it overrides the currently specified "FORMat".

"ASCii", "HEXadecimal", "BINary" = the same as "FORMat" parameter

"INTeger" = the TRACe content is returned byte after byte (without prefixe) as a **block** of raw integer data.

INTeger8 : "<data1><data2>...<dataN>"
INTeger16 : "<MSbyte.data1><LSbyte.data1><MSbyte.data2>...<MSbyte.dataN><LSbyte.dataN>"

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TRACe:HANDle? <trace_name> ==> <num_value>

Description: Returns a number linked to the specified trace. This number is necessary in the using of the pseudo-register.

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<start_ind> is the indice of the first data to be taken from/written to <trace_name>
<stop_ind> is the indice of the last data to be taken from/written to <trace_name>
The absolute first data of <trace_name> has an indice of 1.
If <start_ind> is omitted then the start indice is 1
If <stop_ind> is omitted then the stop indice is the absolute last indice of <trace_name>

[SOURce]:DOPort1:TRACe[:NAME] <trace_name>[, <start_ind>[, <stop_ind>]]
[SOURce]:DOPort2:TRACe[:NAME] <trace_name>[, <start_ind>[, <stop_ind>]]

Description : Associates the TRACe "<trace_name>" with 8 digital I/O of an output port, the data contained in <trace_name> will be transfered to outputs at the TRIGger STEP rhythm

Parameters :
<trace_name> is a TRACe containing data of INTeger8 format, **<trace_name> = NULL dissociates DOPortX from all TRACes.**

Initialization : NULL, no TRACe is associated with DOPort1 and DOPort2.

Examples :
"TRAC:DEF T_1, 100, INT8" opens "T_1"
"TRAC T_1#H200,#H201,#H200,........" fills up "T_1"
"DOP1:TRAC T_1" associates the digital port 1 to "T_1"
"DOP2:TRAC NULL" disassociates the digital port 2 from all TRACe.

•query form :

[SOURce]:DOPort1:TRACe[:NAME]? ==> <trace_name>, <start_ind>, <stop_ind>
[SOURce]:DOPort2:TRACe[:NAME]? ==> <trace_name>, <start_ind>, <stop_ind>

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SENSe:DIPort3:TRACe[:NAME] <trace_name>[, <start_ind>[, <stop_ind>]]
SENSe:DIPort4:TRACe[:NAME] <trace_name>[, <start_ind>[, <stop_ind>]]

Description : Associates <trace_name> to 8 digital I/O of Input ports, <trace_name> will be filled up with the values measured on this port at the TRIGger STEP rhythm.

Parameters :
<trace_name> is a TRACe containing data of INTeger8 format, **<trace_name> = NULL dissociates DIPortX from all TRACes.**

Initialization : NULL, no TRACe is associated with DIPort1 and DIPort2.

•query form:

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SENSe:DIPort3:TRACe[:NAME]? ==> <trace_name>, <start_ind>, <stop_ind>
SENSe:DIPort4:TRACe[:NAME]? ==> <trace_name>, <start_ind>, <stop_ind>

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[SOURce]:VOLTage:TRACe[:NAME] <trace_name>[, <start_ind>[, <stop_ind>]],<channel_list>

Description : Associates <trace_name> with the analog outputs listed in the <channel_list>, the data enclosed in <trace_name> will be transfered to these outputs at the rhythm of the TRIGger STEP.

Parameters :
<trace_name> is a TRACe containing data of INTeger16 format.

Initialization : NULL, no TRACe is associated with any analog Output channel.

Examples :
"TRAC:DEF T_SINUS, 1000" opens "T_SINUS" of 1000 INTeger16
"TRAC T_SINUS,0,0,1,1,3,4,......." fills up "T_SINUS"
"VOLT:TRAC T_SINUS, (@1,5)" associates "T_SINUS" to the analog outputs 1 and 5.

•query form:

[SOURce]:VOLTage:TRACe[:NAME]? <channel_list> ==> <trace_name>, <start_ind>, <stop_ind>{, <trace_name>, <start_ind>, <stop_ind>}

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SENSe:VOLTage:TRACe[:NAME] <trace_name>[, <start_ind>[, <stop_ind>]], <channel_list>

Description : Associates <trace_name> with the analog inputs specified in the <channel_list>, <trace_name> will be filled up with values measured on these inputs at the rhythm of the TRIGger STEP.

Parameters :
<trace_name> is a TRACe containing data of INTeger16 format.

Initialization : NULL, no TRACe is associated with any analog Input channel.

Examples :
"SENS:VOLT:TRAC T_1,(@9)" associates "T_1" with the analog input 9.

•query form:

SENSE:VOLTage:TRACe[:NAME]? <channel_list> ==> <trace_name>, <start_ind>, <stop_ind>{, <trace_name>, <start_ind>, <stop_ind>}

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[SOURce]:DOPort1:TRACe:INDice? ==> <num_value>
[SOURce]:DOPort2:TRACe:INDice? ==> <num_value>
SENSe:DIPort3:TRACe:INDice? ==> <num_value>
SENSe:DIPort4:TRACe:INDice? ==> <num_value>
[SOURce]:VOLTage:TRACe:INDice? <channel_list> ==> <num_value>,{,<num_value>}
SENSe:VOLTage:TRACe:INDice? <channel_list> ==> <num_value>,{,<num_value>}

Description : These commands allow the user to know the current position of the TRACe pointer associated with the specified I/O channel. They can be sent during the exchanges or after they have been stopped in order to know which datum has been read or written last.

Response :
<num_value> is an Integer value from 1 to 4294967295, it is the indice of the datum which is (or was) about to be be read or written, so before the exchanges have began the indice is 1.

Example :

"trac:def t_1,100,int8"
"trac t_1,1,2,3,4,64,128,....."
"trac:def t_2,50"
"dop1:trac t_1"
"sens:volt:trac t_2,(@9)"
"trig:bus on; step:sour bus"
"trig:volt:step:eco 2,(@9)"
"init"
"*trg; *trg; *trg; *trg; *trg; *trg"
"dop1:trac:ind?" ==> "7"
"sens:volt:trac:ind? (@9)" ==> "4"

[SOURce]:DOPort1:TRACe:COUNt <num_value>
[SOURce]:DOPort2:TRACe:COUNt <num_value>
SENSe:DIPort3:TRACe:COUNt <num_value>
SENSe:DIPort4:TRACe:COUNt <num_value>
[SOURce]:VOLTage:TRACe:COUNt <num_value>, <channel_list>
SENSe:VOLTage:TRACe:COUNt <num_value>, <channel_list>

Description : Sets the number of times that the TRACe associated with the specified I/O channel must be scaned for that channel.

Parameter :

<num_value> is in the range from 0 to 4294967295, a value of 0 means that the TRACe is scaned indefinitely until a STOP trigger occurs or an ABORt command.

Initialization : 0

Query form : Yes

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IV.10) Trigger commands

IV.10.a) General

***TRG** is an IEEE 488.2 command which generates a trigger equivalent to a GET (Word Serial Trigger).

TRIGger:TIMer:PERiod <num_value>

Description : Sets the period of the timer.

Parameters :
<num_value> is a Integer value, the time unit is 1µs, the minimum accepted value is 100, but in fact this minimum value depends on the number and type of the I/O channels associated with a TRACe. The maximum value is 134217720. The Timer period resolution is 8 µs, then any value which is not a multiple of 8 will be rounded to the nearest multiple of 8.

Initialization: 1000000 that means 1 s.

Examples :
"TRIG:TIM:PER 800" , each 800 µs, the timer generates an interruption which will be taken into account provided that a trigger has TIMer as SOURce, and that it has been allowed by "TRIGger:TIMer[:STATe] ON".

• query form :

TRIGger:TIMer:PERiod? ==> <num_value>

TRIGger:TIMer[:STATe] <ON|OFF>

Description : Enables (ON) or disables (OFF) the Timer.

Initialization : ON

• query Form :

TRIGger:TIMer[:STATe]? ==> <ON|OFF>

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TRIGger:EOT[:STATe] <ON|OFF>

Description : Enables (ON) or disables (OFF) the EOT trigger .

Initialization : ON

• query form :

TRIGger:EOT[:STATe]? ==> <ON|OFF>

TRIGger:EOT:NAME <trace_name>

Description : sets the name of the TRACe which generates a EOT Trigger when its last datum is encountered during TRACe to I/O or I/O to TRACe process.

Parameter :

<trace_name> is the name of an existing or non existing TRACe, if <trace_name> is **"ALL"** then **every** End Of Trace encountered must generate a EOT trigger.

• query form :

TRIGger:EOT:NAME? ==> <trace_name>

TRIGger:TTLTrg[:STATe] <ON|OFF>

Description : Enables (ON) or disables (OFF) the selected TTLtrig.

Initialization : ON

• query form :

TRIGger:TTLTrg[:STATe]? ==> <ON|OFF>

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TRIGger:BUS[:STATe] <ON|OFF>

Description : Enables (ON) or disables (OFF) the Word Serial or IEEE 488.2 "*TRG" trigger.

Initialization : ON

•query form : TRIGger:BUS[:STATe]? ==> <ON|OFF>

TRIGger:ETRG1[:STATe] <ON|OFF>

Description : Enables (ON) or disables (OFF) the external Trigger 1.

Initialization : ON

•query form : TRIGger:ETRG1[:STATe]? ==> <ON|OFF>

TRIGger:ETRG2[:STATe] <ON|OFF>

Description : Enables (ON) or disables (OFF) the external Trigger 2.

Initialization : ON

•query form : TRIGger:ETRG2[:STATe]? ==> <ON|OFF>

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IV.10.b) STARt trigger

TRIGger[:GLOBal][:STARt]:SOURce <char_data>

Description : Sets the origin of the trigger which has to be counted so that the exchanges between I/O channels and TRACes can begin.

Parameters :
<char_data> can take the values :

IMMediate : No waiting for any event; as soon as the command INITiate is received, the exchanges I/O <-> TRACes begin at the rhythm of trigger STEP.

HOLD : The STEP and STOP triggers can only be launched by the command "TRIGger[:GLOBal][:STARt][:IMMediate]".

ETRG1 : External trigger 1
ETRG2 : External trigger 2

TTLTrg0, TTLTrg1, TTLTrg2, TTLTrg3, TTLTrg4, TTLTrg5, TTLTrg6, TTLTrg7: The event to be taken into account is the activation of the specified TTLtrig line (if allowed by "TRIGger:TTLT[:STATe] ON").

BUS : The event to be taken into account is the receipt of "Word Serial Trigger" or of the command IEEE 488.2 "*TRG" (if allowed by "TRIGger:BUS[:STATe] ON").

Initialization : IMMediate

•query form :

TRIGger[:GLOBal][:STARt]:SOURce? ==> <char_data>

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TRIGger[:GLOBal][:STARt]:ECOunt <num_value>

Description : Gives the number of times that the event of GLOBal:STARt:SOURce type has to be detected before the trigger STARt can be considered as completed.

Parameters : **<num_value>** is an integral value from 1 to 4294967295.

Initialization : 1

Query form : TRIGger[:GLOBal][:STARt]:ECOunt? ==> <num_value>

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TRIGger[:GLOBal][:STARt][:IMMediate]

Description : Whatever SOURce has been selected for STARt trigger and whatever ECOunt number of events chosen, the trigger STARt is considered as completed as soon as this command has been received. It is of course necessary to have launched the TRIGger by the command INITiate, otherwise this command would have no effect. This command is usually used when the SOURce is HOLD.

Examples :

"TRIG:SOUR HOLD"

"INIT" sets up the cycle of GLOBal triggers

"TRIG" launches the exchanges between I/O and TRACes at the rhythm of STEP and stopped by STOP

•No query form :

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TRIGger[:GLOBal][:STARt]:COUNt <num_value>

Description : Sets the number of global cycles (STARt + STOP) which have to be carried out without sending a command INITiate.

Parameters :

<num_value> is an Integer value from 0 to 4294967295, **a 0 value signifies that the number of loop backs is undefined**, as long as an ABORt command is not received, the cycle is restarted automatically.

Initialization: 1, the cycle is realized just one time.

Query form:

TRIGger[:GLOBal][:STARt]:COUNt? ==> <num_value>

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IV.10.c) STOP trigger

TRIGger[:GLOBal]:STOP:SOURce <char_data>

Description : Sets the origin of the trigger which has to be taken into account to stop the exchanges between I/O channels and TRACes, the STOP SOURce is taken into account only when the trigger STARt is completed.

Parameters :
<char_data> can take the values :

EOT : for "End Of Trace", as soon the selected TRACe(s) has reached its end, an event is taken into account.

HOLD : no event is taken into account, STEP trigger can only be stopped by the command "TRIGger[:GLOBal]:STOP[:IMMediate]" (or "ABORT").

ETRG1 : External trigger 1
ETRG2 : External trigger 2

TTLTrg0, TTLTrg1, TTLTrg2, TTLTrg3, TTLTrg4, TTLTrg5, TTLTrg6, TTLTrg7: the event to be taken into account is the activation of the specified TTLtrig line (if allowed by "TRIGger:TTLT[:STATe] ON").

TIMer : the event to be taken into account is the top of TIMer generated at a period specified by TRIGger:TIMer:PERiod (if allowed by "TRIGger:TIMer:[:STATe] ON").

BUS : The event to be taken into account is the receipt of "Word Serial Trigger" (GET) or of the command IEEE 488.2 "*TRG" (if allowed by "TRIGger:BUS[:STATe] ON").

Initialization: HOLD, the STOP can only be caused by IMMediate

•query form :

TRIGger[:GLOBal]:STOP:SOURce? ==> <char_data>

TRIGger[:GLOBal]:STOP:ECOunt <num_value>

Description : Gives the number of times that the event of GLOBal:STOP:SOURce type has to be detected before the STOP trigger can be considered as completed.

Parameters :
<num_value> is an integral value from 1 to 4294967295.

Initialization : 1

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Query form :

TRIGger[:GLOBal]:STOP:ECOunt? ==> <num_value>

TRIGger[:GLOBal]:STOP[:IMMediate]

Description : Whatever SOURce of trigger has been selected for STOP trigger and whatever the ECOunt number of events, the STOP trigger is considered as completed as soon as this command is received. This command is usually used when the SOURce is HOLD.

•No query form :

IV.10.d) STEP trigger

TRIGger[:GLOBal]:STEP:SOURce <char_data>

Description : Sets the origin of the trigger which must be taken into account in order to cause the exchanges between I/O channels and TRACes, the STEP SOURce is taken into account only if the trigger STARt is completed.

Parameters :
<char_data> can take the values :

HOLD : no event is taken into account, exchanges between I/O and TRAces can only be caused by the command "TRIGger[:GLOBal]:STEP[:IMMediate]" .

ETRG1 : External trigger 1
ETRG2 : External trigger 2

TTLTrg0, TTLTrg1, TTLTrg2, TTLTrg3, TTLTrg4, TTLTrg5, TTLTrg6, TTLTrg7: the event to be taken into account is the activation of the specified TTLtrig line (if allowed by "TRIGger:TTLT[:STATe] ON").

TIMer : the event to be taken into account is the top of TIMer generated at a period specified by TRIGger:TIMer:PERiod (if allowed by "TRIGger:TIMer:[:STATe] ON").

BUS : the event to be taken into account is the receipt of "Word Serial Trigger" or of the command IEEE 488.2 "*TRG" (if allowed by "TRIGger:BUS[:STATe] ON").

Initialization : HOLD

•query form:

TRIGger[:GLOBal]:STEP:SOURce? ==> <char_data>

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TRIGger:DOPort1:STEP:ECOunt <num_value>
TRIGger:DOPort2:STEP:ECOunt <num_value>
TRIGger:DIPort3:STEP:ECOunt <num_value>
TRIGger:DIPort4:STEP:ECOunt <num_value>
TRIGger:VOLTage:STEP:ECOunt <num_value>, <channel_list>

Description : sets the number of times that the GLOBal:STEP:SOURce event should be detected before the TRIGger:GLOBal:STEP can be considered as completed **for the specified channel(s)**. It means that the exchanges between the TRACes and the I/O channels can be asynchronous.

Parameters :
<num_value> is an Integer number from 1 to 424967295.

Initialization : 1

•query Form :

TRIGger:DOPort1:STEP:ECOunt? ==> <num_value>
TRIGger:DOPort2:STEP:ECOunt? ==> <num_value>
TRIGger:DIPort3:STEP:ECOunt? ==> <num_value>
TRIGger:DIPort4:STEP:ECOunt? ==> <num_value>
TRIGger:VOLTage:STEP:ECOunt? <channel_list> ==> <num_value>{,<num_value>]

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TRIGger[:GLOBal]:STEP[:IMMediate]

Description : whatever SOURce for STEP trigger and whatever the ECOunt numbers of events, the STEP trigger is considered as completed for all I/O channels as soon as this command is received. This command is generally used when the SOURce is HOLD.

• No query form:

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TRIGger:DOPort1:STEP[:IMMediate]
TRIGger:DOPort2:STEP[:IMMediate]
TRIGger:DIPort3:STEP[:IMMediate]
TRIGger:DIPort4:STEP[:IMMediate]
TRIGger:VOLTage:STEP[:IMMediate] <channel_list>

Description : whatever the SOURce for STEP trigger and whatever the ECOunt numbers of events, the STEP trigger is considered as completed for the specified channel(s) as soon as this command is received. This command is generally used when the SOURce is HOLD.

• No query form:

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IV.10.e) Initiating and Abandoning

INITiate:[GLOBal]

Description : this command sets up all the TRACe pointers associated with I/O channels at the beginning of **TRACe** and validates the conditions of TRIGger **STARt** , although the two other TRIGgers STEP and STOP are not set up and validated until the TRIGger STARt is completed.
The TRIGger cycle only concerns those channels which have an associated TRACe, the other channels are not concerned and remain in the state resulting from the direct commands.

No query form :

∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞∞

ABORt:[GLOBal]

Description : this command causes the trigger cycle to be totally abandoned.

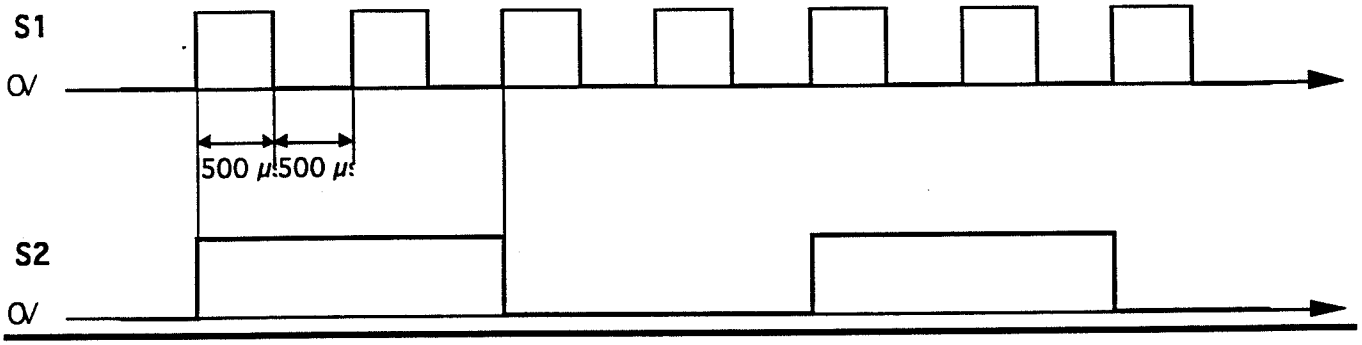
•No query form

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IV.10.f) Examples and real cases

Real Case N° 1



Purpose : **To generate S1 and S2 on the digital outputs 1 and 2, the other port outputs remaining in Open Collector, during one hour.**

List of commands to be sent to the module :

TRAC:DEF T_1, 8, INT8
Opening of the TRACe "T_1" which will contain the description of S1 and S2.

FORM HEX
By default the exchanged data are in hexadecimal

TRAC T_1,FF,FE,FF,FE,FD,FC,FD,FC
Remote control of the data (in hexadecimal) in the TRACe "T_1", only the two LSB vary, they describe S1 and S2 signals, other bits are set to one, which corresponds to the Open Collector state of associated outputs.

DOP1:TRAC T_1
Creates an link between the TRACe "T_1" and the port 1 of digital outputs.

TRIG:TIM:PER 500; STAT ON
The period of the TIMer is 62*8 µs that means 496 µs (the nearest of 500)

TRIG:STEP:SOUR TIM ; STOP:SOUR TIM ; ECO 45000000
The TIMer is a SOURce for the TRIGger STEP and STOP.
The TRIGger STEP is completed after each occurrence of the TIMer, that means that a value is read each 500 µs in "T_1" and applied to DOP1.
The TRIGger STOP is completed after 45000000 occurrences of the TIMer, that is to say 1H, at the moment the cycle is ending.

INIT
The TRIGger STARt is IMMediate by default, the exchanges from "T_1" to Digital Port 1 start as soon as this command is given. The process will end automatically after one hour.

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Real case N° 2

Purpose : **To generate S1 on the digital output 1, and S2 on the digital output 9, the other digital outputs remaining in Open Collector, for an undetermined period.**

List of the commands to be sent to the module :

TRAC:DEF T_1, 2, INT8
Declaration of the TRACe associated to S1 and S2

FORM HEX
TRAC T_1,FF,FE
Two values are enough to describe S1 and S2.

DOP1:TRAC T_1
DOP2:TRAC T_1
T_1 is associated to the port 1 and the port 2

TRIG:TIM:PER 500; STAT ON

TRIG:STEP:SOUR TIM ; DOP2:STEP:ECO 4
The TIMer is the STEP SOURce, at each occurrence of the Timer a value is transfered from T_1 to Digital Port 1 whilst only one each four occurrences for Digital Port 2.

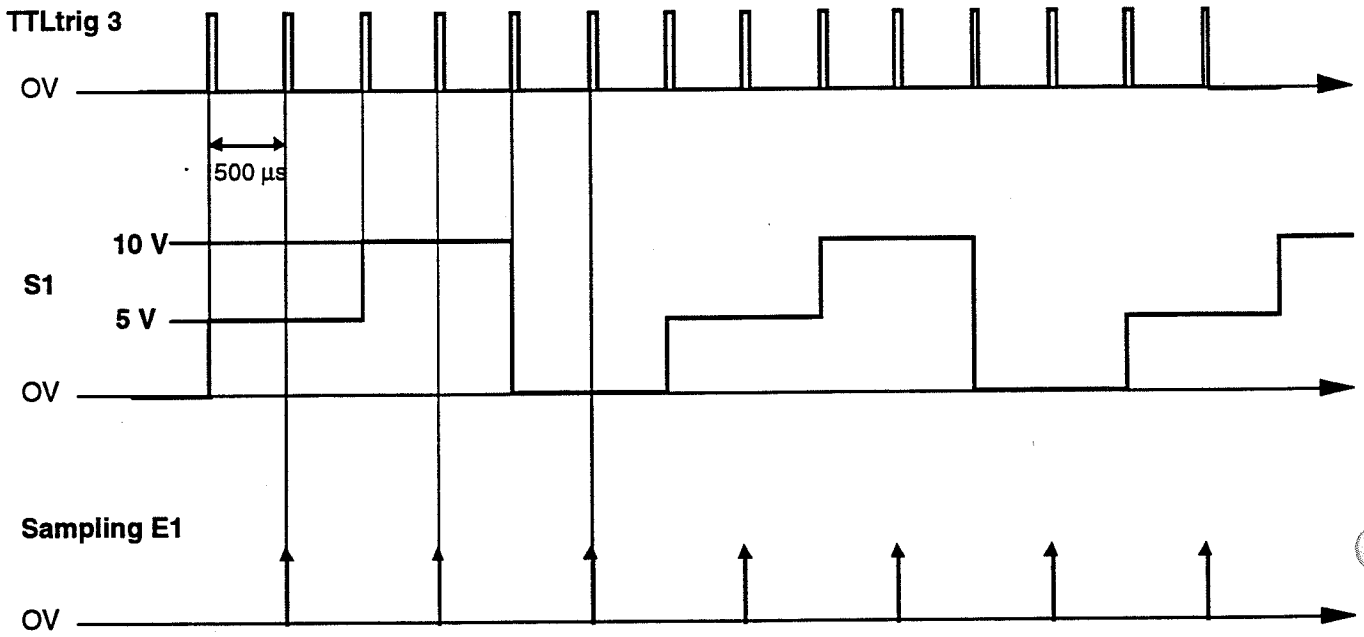
INIT

ABORT

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Real case N° 3



Purpose :

To generate S1 on the analog output N° 1 and read 120 samples of an analog signal E1 (in range 0-5V) on the analog Input 9, synchronized by the TTLtrig3.

List of the commands to be sent to the module :

FORM HEX ; TRAC:DEF T_1,6 ; DATA T_1,0,0,7FF,7FF,FFF,FFF
Opening of the TRACe "T_1" containing the description of the signal S1 and the remote control loading of corresponding data.

TRAC:DEF T_2,120
Opening of the TRACe "T_2" whose purpose is to receive the sampled data of the signal E1.

VOLT:TRAC T_1,(@1)
Link between TRACe "T_1" and the analog output 1.

SENS:VOLT:TRAC T_2,(@9)
Link between TRACe "T_2" and the analog input 9.

TRIG:STEP:SOUR TTLT3; VOLT:STEP:ECO 2, (@9)
The TTLtrig line 3 is chosen as a SOURce for the TRIGger STEP. In order to respect the chronogramme output channel 1 receives a datum measured on analog Input 9 every time the TTLtrig occurs while a datum is tranfered from T_1 to analog Output 1 only every second time.

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TRIG:STOP:SOUR EOT
The event chosen to stop the process is the end of "T_2".

VOLT:RANG 5,(@1)
The analog Output 1 is in the range 0-10V

SENS:VOLT:RANG 3,(@9)
The analog Input 9 is in the range 0-5V

TRIG:TTLT ON
TTLtrig is allowed to run the STEP trigger.

INIT
The process will stop automatically after TRACe "T_2" has been filled.

TRAC? T_2
Reading, after the end of the process, of the samples stocked in "T_2".

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IV.11) VXI interrupter capabilities

- Nine sequences are available (n in <1,9>), each sequence is completely independent , it has its own source conditions, its own VXI event and its own Event COunt.

OUTPut:VINTerrupt:SEQuence<n>:SOURce <source>[, *<num_val>[, <condt>]]

Description : Sets the source of the specified sequence.

Parameters :

<source> :

TIMer : the internal timer (Timer must be ON)
ETRG1 : the external trigger 1
ETRG2 : the external trigger 2
EOT : the End Of the selected Trace(s) (with "TRIGger:EOT[:NAME]" command)

DIPort<n> : the selected Digital Port is tested each time the **Timer** occurs (Timer must be ON)

<num_val> is from 0 to 255 and is a **mask**
<condt> is "AND", "NAND", "OR" or "NOR"

"**data**" being the data measured on digital Port, an Event is counted if :

AND	(data AND mask) EQual 0
NAND	(data AND mask) Not Equal 0
OR	(data OR mask) EQual 255
NOR	(data OR mask) Not Equal 255

Default values : <num_val> = 0, <condt> = "NOR"

AINPut<n> : the selected Analog Input Channel is tested each time the **Timer** occurs (Timer must be ON)

<num_val> is from 0 to 4095 and is a **threshold**
<condt> is "OVER" or "UNDer"

"**data**" being the data measured on analog channel, an Event is counted if :

OVER	(data > threshold)
UNDER	(data < threshold)

Default values : <num_val> = 4095, <condt> = "OVER"

Query form :

OUTPut:VINTerrupt:SEQuence<n>:SOURce? ==> <source>[, *<num_val>, <condt>]

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OUTPut:VINTerrupt:SEQuence<n>:EVENt *<num_val>

Description : Sets the event number (VXI bus specification E.4 "protocol events") that is written in the Status/Id word during the VXI interrupt acknowledgement process.

Parameter :

<num_val> is a "User Defined" Event from 0 to #H3F.

Initialization : 0

Query form : Yes

OUTPut:VINTerrupt:SEQuence<n>:ECOunt <num_val>

Description : Sets the number of times that the specified Source Event must be detected before the VXI Interrupt is asserted.

Parameter : a <NR1> value from 1 to 4294967295

Initialization : 1

Query form : Yes

OUTPut:VINTerrupt:SEQuence<n>[:STATe] <ON|OFF>

Description : If "ON" the selected sequence becomes effective.

Initialization : "OFF"

Query form : Yes

FETCh:VINTerrupt:SEQuence<n>[:DATA]? ==> <num_value>

Description : When "DIPort<n>" or "AINPut<n>" source is used, returns the last measurement that has been counted as an Event (so the condition was true).

Examples :

VXI Interrupt with Event "1" is asserted after 5 External Trigger 1
"OUTP:VINT:SEQ1:SOUR ETRG1; ECO 5; EVEN 1; STAT ON"

VXI Interrupt with Event "2" is asserted each time Digital Input 2 of Port 3 is at a high level (1ms resolution)
"OUTP:VINT:SEQ2:SOUR DIP3,2,NAND; EVEN 2; STAT ON"

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IV.12) TTLtrigger generation

• Nine sequences are available (n in <1,9>), each sequence is completely independent , it has its own source conditions, its own associated TTLtrig line and its own Event COunt.

OUTPut:TTLTrg:SEQuence<n>:SOURce <source>[, *<num_val>[, <condt>]]

Description : Sets the source of the specified sequence.

Parameters :

<source> :

TIMer : the internal timer (Timer must be ON)
ETRG1 : the external trigger 1
ETRG2 : the external trigger 2
EOT : the End Of the selected Trace(s) (with "TRIGger:EOT[:NAME]" command)

DIPort<n> : the selected Digital Port is tested each time the **Timer** occurs (Timer must be ON)

<num_val> is from 0 to 255 and is a **mask**
<condt> is "AND", "NAND", "OR" or "NOR"

"**data**" being the data measured on digital Port, an Event is counted if :

AND	(data AND mask) EQual 0
NAND	(data AND mask) Not Equal 0
OR	(data OR mask) EQual 255
NOR	(data OR mask) Not Equal 255

Default values : <num_val> = 0, <condt> = "NOR"

AINPut<n> : the selected Analog Input Channel is tested each time the **Timer** occurs (Timer must be ON)

<num_val> is from 0 to 4095 and is a **threshold**
<condt> is "OVER" or "UNDer"

"**data**" being the data measured on analog channel, an Event is counted if :

OVER	(data > threshold)
UNDER	(data < threshold)

Default values : <num_val> = 4095, <condt> = "OVER"

Query form :

OUTPut:TTLTrg:SEQuence<n>:SOURce? ==> <source>[, *<num_val>, <condt>]

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OUTPut:TTLTrg:SEQuence<n>:LINE <num_val>

Description : Sets the number of the TTL trigger line associated with the specified sequence

Parameter :

<num_val> is from 0 to 7

Initialization : 0

Query form : Yes

OUTPut:TTLTrg:SEQuence<n>:ECOunt <num_val>

Description : Sets the number of times that the specified Source Event must be detected before the TTL trigger is generated.

Parameter : a <NR1> value from 1 to 4294967295

Initialization : 1

Query form : Yes

OUTPut:TTLTrg:SEQuence<n>[:STATe] <ON|OFF>

Description : If "ON" the selected sequence becomes effective.

Initialization : "OFF"

Query form : Yes

FETCh:TTLTrg:SEQuence<n>[:DATA]? ==> <num_value>

Description : When "DIPort<n>" or "AINPut<n>" source is used, returns the last measurement that has been counted as an Event (so the condition was true).

Example :

TTLtrig line 5 is generated each 100 occurences of the internal timer
"OUTP:TTLT:SEQ1:SOUR TIM; ECO 100; LINE 5; STAT ON"

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IV.13) SYSTem

SYSTem:PRESet or *RST

Description : Resets the module at the starting level

•No Query form

SYSTem:VERSion? ==> <num_val>

Description : Returns the SCPI revision number for which the instrument complies.

SYSTem:ERRor? ==> <character_data>

Description : Returns an error message from the Error Output Queue (FIFO type). The oldest error is the first transmitted, a transmitted error is canceled out of the queue, when the queue is empty the message "0, No error" is sent. If an error occurs and no place is available in the Error Queue to store the corresponding message, then the message "-350,"Queue overflow"" is stored instead of it, any error occurring later on will not be noted.

***IDN? ==> RACAL,<Model_number>,<Serial_number>,<Firmware_level>**

***OPT? ==> <char_data>{, <char_data>}**

Response :

If no option is installed, only character <NULL> (ASCII 0X00) is returned.
else

"16V" :	Analog Outputs are 16V versions.
"TTL" :	Digital Inputs/Outputs are TTL compatible.
"CURRent" :	Analog Outputs are current versions.
"AMEMory" :	256 k of Additionnal MEMory is installed.

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***TST? ==> <num_value>**

Response : if **<num_value>** = 0, the Test is OK, otherwise the returned number identifies the faulty components:

*16 : The configuration is not OK.
*8 : TRACE memory fails.
*4 : The analog I/O board 1 is faulty.
*2 : The analog I/O board 2 is faulty.
*1 : The digital I/O board is faulty.

Example:

If "*TST?" returns "6" (4+2) then the two analog I/O board are faulty.
If "*TST?" returns "17" (16+1) then the configuration is not correct and the digital I/O board is faulty.

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IV.14) STATus

General Description

- IEEE 488.2 standard imposes two registers : "**Status Byte**" and "**Standard Event Status Register**".

- The"**Status Byte**" gives global information on the system state in such a way that user can select (through Enable registers) which information is desired.

- The "**Standard Event Status Register**" reports Standard Events such as "Errors detection" or "Operation Complete" .

- SCPI has added some more registers which report more specific states and events of the instrument, three registers are available at the same level :

A **CONDition** register reports some device states, every change in a device state causes the associated CONDition register to be changed immediately.

An **EVENt** register captures the changes in the associated CONDition register, when a change has been captured it remains in the EVENt register even if the CONDition register changes to its previous state.

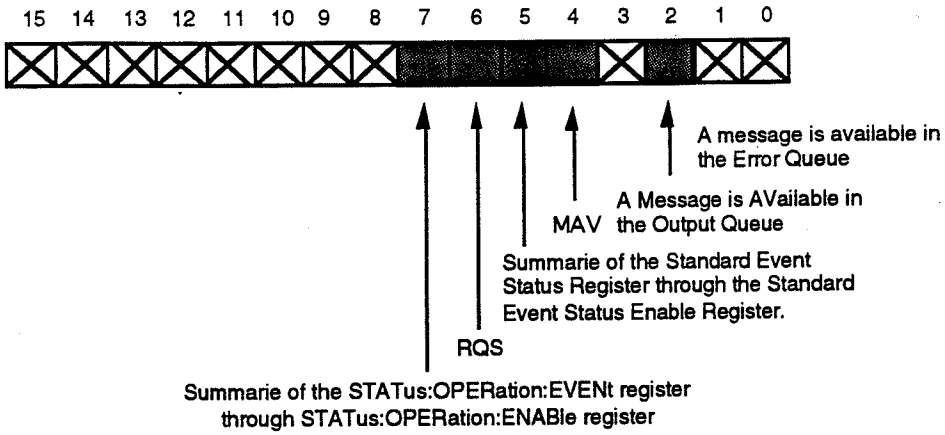
Some bits in an **EVENt** register may not reflect changes in the corresponding CONDition register, they summarize selected bits from another EVENt register, the bit selection is specified in the **ENABle** register.

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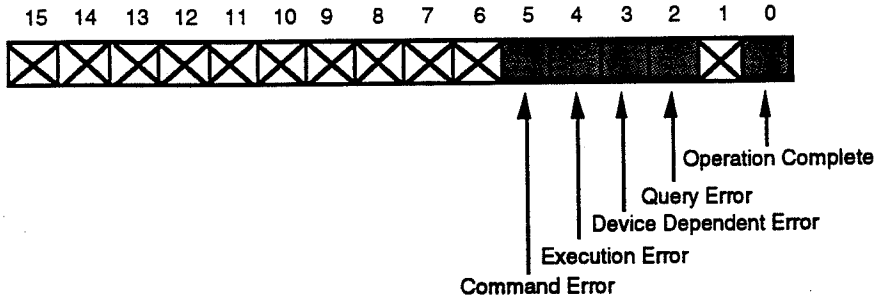
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Description of status register contents

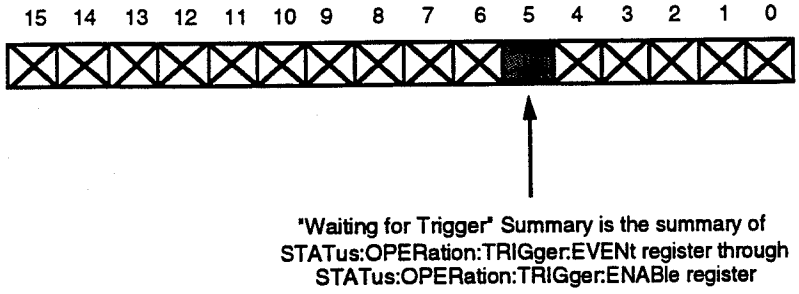
STATUS BYTE



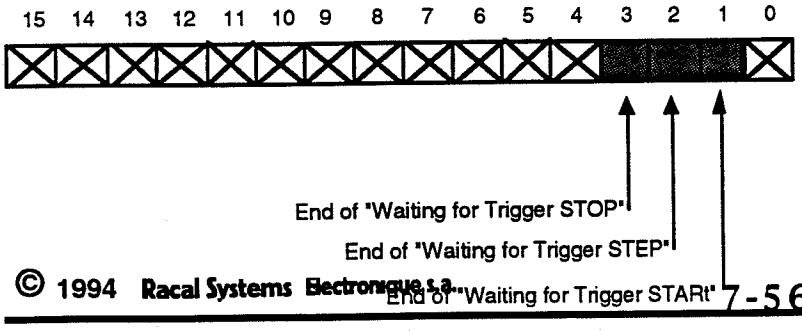
STANDARD EVENT STATUS REGISTER



STATus:OPERation:EVENt register



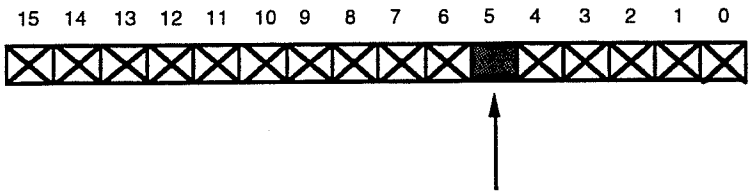
STATus:OPERation:TRIGger:EVENt register



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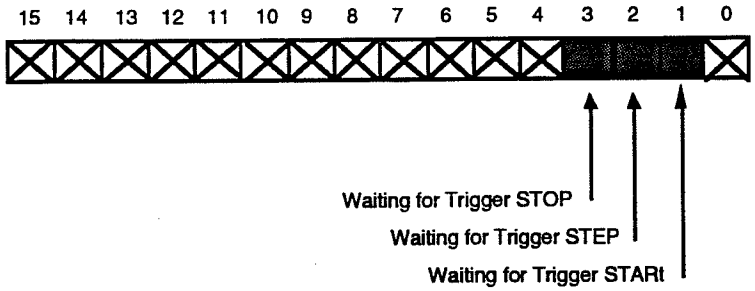
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STATus:OPERation:CONDition register



"Waiting for Trigger" Summary is the summary of
STATus:OPERation:TRIGger:CONDition

STATus:OPERation:TRIGger:CONDition register



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***CLS**

Description : Clears all event registers and clears the error queue.

***ESE <num_value>**

Description : Sets the Standard Event Status Enable Register for reporting in bit 5 of Status Byte.

Initialization : 0, no reporting from SESR in Status Byte.

***ESE? ==> <num_value>**

Description : returns the content of the Standard Event Status Enable Register.

***ESR? ==> <num_value>**

Description : returns the content of the Standard Event Status Register, reading the SESR clears it.

***STB? ==> <num_value>**

Description : returns the content of the Status Byte.

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STATus:OPERation[:EVENt]? ==> <num_value>
STATus:OPERation:TRIGger[:EVENt]? ==> <num_value>

Description : returns the content of the specified EVENt register, reading an EVENt register clears it.

∞∞

STATus:OPERation:CONDition? ==> <num_value>
STATus:OPERation:TRIGger:CONDition? ==> <num_value>

Description : Returns the content of the specified CONDition.

∞∞

STATus:OPERation:ENABle <num_value>
STATus:OPERation:TRIGger:ENABle <num_value>

Description : Sets the specified ENABle register.

Initialization :
STATus:OPERation:ENABle is set to 0 so that no bit from STATus:OPERation:EVENt is allowed to be reported in bit 7 of Status Byte.

STATus:OPERation:TRIGger:ENABle is set to #H000E so that the three active bits of STATus:OPERation:TRIGger:EVENt are allowed to be reported in bit 5 of STATus:OPERation:EVENt.

Query form :

STATus:OPERation:ENABle? ==> <num_value>
STATus:OPERation:TRIGger:ENABle? ==> <num_value>

∞∞

STATus:PRESet

Description : Initializes the two SCPI STATus ENABle registers, **but doesn't clear the EVENt registers**.

∞∞

Remarks : ENABle registers only apply to EVENt registers, reporting of CONDition registers is made regardless of ENABle registers.

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V) THE "PSEUDO REGISTER BASED" OPERATION

V.1) Overview

To provide performance levels closer to those of a register based design, the new software version 3.00 of the 6061 module has included a Pseudo Register Based mode of operation.
The pseudo register based software consists of some very short software routines to do simple and quick data transfers for the user.
The message based software coexists with the pseudo register based software. This means the user can use whichever approach is most advantageous, even to the point of mixing message based and pseudo register based operations.

The register map for message based devices has half of the registers designated as device dependent registers (as specified in VXIbus standard). The pseudo register based software takes advantage of these device dependent registers to increase the data transfer rates. To be able to use the pseudo register based software, the user only needs to be able to read and write in these registers.

To use the new software routines, the user has to write or read to the first 5 of device dependent registers. Refer to the Register Map.

V.2) Address Calculation

To make device dependent register accesses, it is necessary to reference the proper address.The VXI standard places all VXI registers in the upper quadrant of the A16 address space. The part of the address that is dependent on the device's VXI address is called the base address. The base address is calculated as follows:

BASE ADDRESS = DEVICE'S VXI ADDRESS * 64 + 49152

In hexadecimal:
BASE ADDRESS = DEVICE'S VXI ADDRESS * 40_{16} + $C000_{16}$

Refer to the Register Map. The numbers along the left side are offsets from the BASE ADDRESS (in Hex).
The access address is calculated like this:

ACCESS ADDRESS = BASE ADDRESS + Offset

Example:

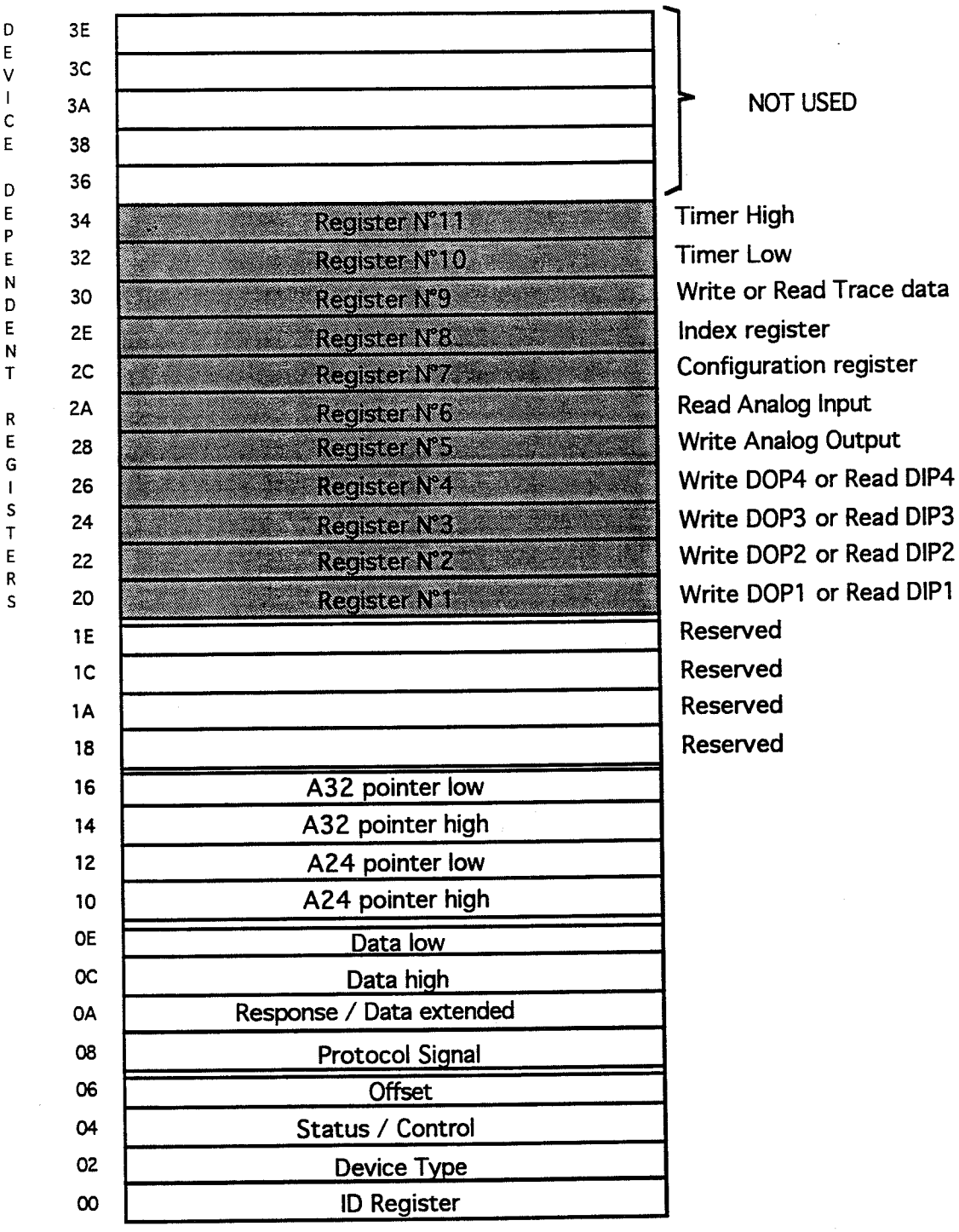
DEVICE'S VXI ADDRESS = 2 (the number we multiply by 40_{16} or 64 decimal).
Access the dependent device register n°1: offset 20_{16} or 32 decimal.

ACCESS ADDRESS (in decimal) = 2 * 64 + 49152 + 32 = 49312
ACCESS ADDRESS (in hex) = 2 * 40_{16} + $C000_{16}$ + 20_{16} = $C0A0_{16}$

With LABWINDOWS, the user can use library functions to make data transfers. These routines witch perform the data transfers are an input routine VXIinREG(...) and an output routine VXIoutREG(...).

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REGISTER MAP

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V.3) Applications

In the rest of this document, the DEVICE'S VXI ADDRESS is '2'.

V.3.a) Input/Ouptut

Write to Digital Output Port 1: offset = 20_{16}
Write to Digital Output Port 2: offset = 22_{16}
Write to Digital Output Port 3: offset = 24_{16}
Write to Digital Output Port 4: offset = 26_{16}

Description: A write to the appropriate access address simply causes a write to the output port.

Similar to the SCPI command:
"[SOURce]:DOPort1[:DATA] *<num_value>[, *<mask>]"

Content of the access address:

MSB

8 bits	8 bits
Mask	Data

<Mask> and <Data> can take values from 0 to #HFF.
<Mask> allows to affect only one part of the outputs; in order to have one output to be affected by <Data>, the corresponding bit of <Mask> must be set to '1'. If all the outputs are affected by <Data> , the <Mask> value is #HFF.

Example:

Bit n°0 of port1 sets to '0' then sets to '1':
Access address = $2*40_{16} + C000_{16} + 20_{16} = C0A0_{16}$
$(C0A0_{16})$ = #H0100 sets bit n°0 of port 1 to '0'
$(C0A0_{16})$ = #H0101 sets bit n°0 of port 1 to '1'

The upper 4 bits of port 2 sets to '1'
Access address = $2*40_{16} + C000_{16} + 22_{16} = C0A2_{16}$
$(C0A2_{16})$ = #HF0F0

Execution_time:

The write on digital output ports takes **#80 µsec.**

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Read from Digital Input Port 1: offset = 20_{16}
Read from Digital Input Port 2: offset = 22_{16}
Read from Digital Input Port 3: offset = 24_{16}
Read from Digital Input Port 4: offset = 26_{16}

Decription: Measures the digital input port. A read from a device dependent register returns data from a previous read. For the user to be guaranteed current data on a read, two reads are necessary. The first read will update the register and the second will return the updated value.

Two simply read on the Access Address returns the data presents on the selected input port.

Similar to the SCPI command:
"MEASure:DIPort3[:DATA]? ==> *<num_value>"

Example:

Reads the content of digital input port 3:
Access address = $2*40_{16} + C000_{16} + 24_{16} = C0A4_{16}$
$(C0A4_{16})$? ==> #HXX , previous value
$(C0A4_{16})$? ==> #H33 , the input 1 and 6 of port 3 are at the high state, the others are at the low state.

Execution time:

The read of a digital input port takes **#110 µsec**, corresponding to two access on the device register. So the user can scrutinize a input port all **#55 µsec** (he just reads the previous data).

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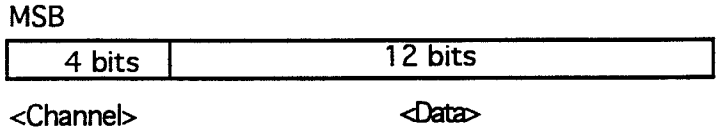
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Write on Analog Output: offset = 28_{16}

Description: The writting on the specific register sets the voltage of the specified analog output.

Similar to the SCPI command:
"[SOURce]:VOLTage:DATA *<num_value>, <channel_list>" excepts that the user can access only one channel.

Content of the access address:



<Channel> : the bits 12 to 15 give the number of the channel. '0' selects the channel 1, '7' selects the channel 8. If the 6061 module is fitted out two analog output boards, it can access the channels 9 to 16 by writting in <Channel> area '8' to '15' (in decimal).

<Data> can take value from 0 to #H0FFF (0 to 4095 in decimal), the resulting voltage depends on the chosen range.

Example:

Sets the output channel 4 in the middle of the range:
Access Address = $2*40_{16}+ C000_{16} + 28_{16} = C0A8_{16}$
$(C0A8_{16})$ = #H3800
Sets the output channel 8 to earth if the channel range is '1', '3' or '5'.
$(C0A8_{16})$ = #H7000

Execution time:

The writing on an output analog takes **#90 µsec**, in comparison with the SCPI command "VOLT 2.5, (@1)" which takes 7 ms. This represents almost a factor 80 improvement over the message base transfers.

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Read of Analog Input: offset = $2A_{16}$

Description: Immediately measures the voltage of the selected analog input.
Two operations are necessary: a write to the specific device dependent register to select the channel then a read to the same register to measure the channel.

Similar to the SCPI command:
"MEASure:VOLTage:DATA? <channel_list> ==> *<num_value>" excepts that the user can access only one
channel.

Content of the access address:

MSB

4 bits	12 bits
<Channel>	<Not used in writting and returns Data in reading>

<Channel> : the bits 12 to 15 give the number of the channel. '8' selects the channel 9, '15' (in decimal).selects the channel 16 If the 6061 module is fitted out two analog input boards, it can access the channels 1 to 8 by writting in <Channel> area '0' to '7'.

After a reading, the register returns the measure value of the input channel.
The returned Data can take values from 0 to #H0FFF (0 to 4095.). The user must convert this data in the chosen range to know the voltage.

Example:

Measure the input channel 16:
Access Address = $2*40_{16} + C000_{16} + 2A_{16} = C0AA_{16}$
Writing: $(C0AA_{16})$ = #HFXXX ; selects the channel 16.
Reading: $(C0AA_{16})$? ==> #H0FFF, the voltage measured on the input 16 is 10 V (on the range 6).

Execution time:

The reading on input analog takes **#120 µsec.**

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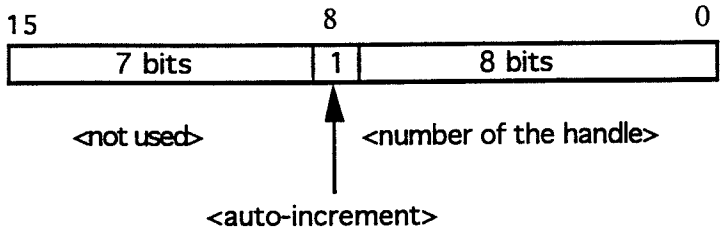
V.3.b) Trace mode

The trace mode using the pseudo-registers allows to monitor the trace data more quickly than with the SCPI commands.

Configuration register: offset = $2C_{16}$

Description:

Content of the access address:



<number of the handle> :This field (one byte) specifies the handle's number of the trace on which the user wants to make transfers. This number is returned by the SCPI command "TRACe:HANDle? <trace_name>"

<auto-increment> : If the bit 8 is set, at every writing or reading on the specified trace, the address pointer is automatically incremented.
If the bit is not activated, the writing or the reading on the specified trace is always made on the same address.

The seven upper bits are not used.

Example:

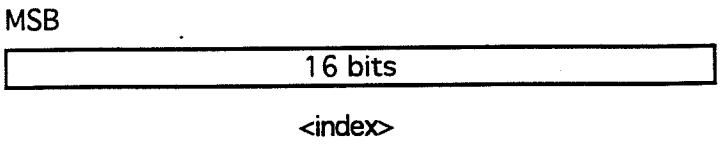
Access Address = $2*40_{16}+ C000_{16} + 2C_{16} = C0AC_{16}$
$(C0AC_{16})$ = #H0102 the auto-increment bit is set and the handle's number is 2.

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Index register: offset = $2E_{16}$

Description: Allows to set the data index for the trace specified in the configuration register.

Content of the access address:



<index> : sets the index of the first data to be read from/writen to the specified trace. It can take value from 1 to $FFFF_{16}$. To start transfers at the beginning of the trace, the value of <index> is 1.

The default value of <index> is 1.

Example:

Access Address = $2*40_{16}+ C000_{16} + 2E_{16} = C0AE_{16}$
$(C0AE_{16})$ = #H0200 the number of the field <index> is 2000_{16}

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Write data to Trace: offset = 30_{16}

Description: A writing to this device-dependent register stores the transmitted value in the location given by the index register.

Content of the access address:

MSB



<not used>	<data>	for a byte transfer
< data >		for a word transfer

<data> : sets the data which is transfered to the pointed address on the memory trace zone.
For a byte transfer, only the 8 lower bits are useful.

Access Address = $2*40_{16}+ C000_{16} + 30_{16} = C0B0_{16}$

Read data from Trace : offset = 30_{16}

Description: A reading from this device-dependent register retrieves the content from the pointed address on the memory zone reserved for the specified trace.
A simply read on the Access Address returns the pointed data (a byte or a word allowing to the type of the transfer).

MSB



<not used>	<returned data>	for a byte transfer
< returned data >		for a word transfer

Access Address = $2*40_{16}+ C000_{16} + 30_{16} = C0B0_{16}$

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Examples of using:

- Download 5 words, in auto-increment mode, on the memory zone reserved by the trace "T_2".

SCPI commands:

TRAC:DEF T_1,2,int8
Opening of the TRACe "T_1" (size : 2 bytes).

TRAC:DEF T_2,10
Opening of the TRACe "T_2" (size : 10 words).

TRAC:HAND? T_2
response ==> "2" : the handle number associated with the trace "T_2".

Pseudo-register commands: (DEVICE'S VXI ADDRESS is '2')

Register of configuration:
($C0AC_{16}$) = #H0102 , the auto-increment bit is set and the handle's number is 2.

Register of index:
($C0AE_{16}$) = #H0005 the downloading begins at the fifth position in the trace T_2.

Write to trace data:
($C0B0_{16}$) = #HA00A downloading of 5 consecutive values.
($C0B0_{16}$) = #HB00B
($C0B0_{16}$) = #HC00C
($C0B0_{16}$) = #HD00D
($C0B0_{16}$) = #HE00E

Before the sequence, the trace T_2 was equal to:
0,0,0,0,0,0,0,0,0,0

After:
0,0,0,0,0,#HA00A,#HB00B,#HC00C,#HD00D,#HE00E
only the last five values of the trace have been modified.

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- Retrieve the content of the trace T_1 from the position 4 to 6 in auto-increment mode

SCPI command:

FORM HEX ; TRAC:DEF T_1,8,int8 ; DATA T_1,B0,0F,A0,FF,78,5E,55,CE
Opening of the TRACe "T_1" and loading of corresponding data.

TRAC:HAND? T_1
response ==>"1"

Pseudo register commands:

(C0AC16) = #H0101 , the auto-increment bit is set and the handle's number is 1

Register of index:
(C0AE16) = #H0004 the data transfer begins at the fourth position in the trace T_1

Read from trace data:

First reading of the trace:
(C0B016) = #HFF, it is the first value pointed in the trace (fourth position).

Second reading of the trace:
(C0B016) = #H78, it is the second value pointed in the trace (fifth position).

Third reading of the trace:
(C0B016) = #H5E, it is the third value pointed in the trace (sixth position).

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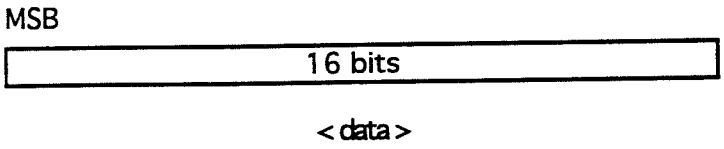
V.3.c) Timer

This routine has been created to change the timer period more quickly than with the SCPI command "TRIGger:TIMer PERiod".
The period is given in microseconds. If the period is fewer than 65536 µsec, the user can write only in the timer low register. In the opposite case, he has to write in the timer high and low registers (see the example).
The lowest period is 100 µsec and the highest period is 134217745 µsec ($7FFFFFF_{16}$)

Timer low: offset = 32_{16}

Description: Sets the timer low period.

Content of the access address:



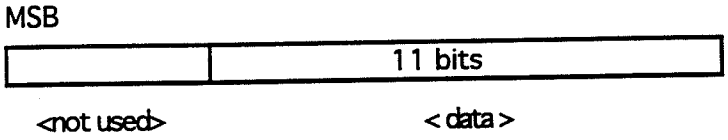
<data> : this field can take values from 100 to 65535 (in decimal).
The lowest period is 100 µsec.

Access Address = $2*40_{16}+ C000_{16} + 32_{16} = C0B2_{16}$

Timer high: offset = 34_{16}

Description: Sets the timer high period in conjunction with the timer low register. **The timer high register must be set before the timer low register.**

Content of the access address:



<data> : this field can take value from 0 to $7FF_{16}$.

The five upper bits are not used.

Access Address = $2*40_{16}+ C000_{16} + 34_{16} = C0B4_{16}$

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Examples:

- Sets the timer period to 300 µsec.

Write to timer low register:
$(C0B2_{16})$ = #H012C

- Sets the timer period to 1 second

Write to timer high register then to timer low register:
$(C0B4_{16})$ = #HF sets the timer high register.
$(C0B2_{16})$ = #H423E sets the timer low register.

($F423E_{16} = 10^6$ µsec)

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Description of errors:

1- No error

Error Number	Error description [description/explanation/examples]
0	No error [The queue is competely empty. Every error/event in the queue has been read or the queue was purposely cleared by power-on.]

2- Command error

Error Number	Error description [description/explanation/examples]
-101	Invalid Character [A syntactic element contains a character which is invalid for that type.]
-102	Syntax error [An unrecognised command or data type was encountered; for example, a string was received when the device does not accept strings.]
-108	Parameter not allowed [More parameters was received than expected for the header; for example the *SRE common command only accepts one parameter, so receiving *SRE 180,34 is not allowed.]
-109	Missing parameter [Fewer parameters were received than required for the header; for example, the *SRE common command requires one parameter, so receiving *SRE is not allowed.]
-112	Program mnemonic too long [The program mnemonic contains more that twelve characters (see IEEE 488.2, 7.6.1.4.1).]
-113	Undefined header [The header is syntactically correct, but it is undefined for this specific device; for example, *XYZ is not defined for any device.]

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-120 Numeric data error
[This error, as well as error -121, are generated when parsing a data element which apprears to be numeric, including the nondecimal numeric types.
This particular error message should be used if the device cannot detect a more specific error.]

or

Invalid character data
[An invalid character for the <char_data> type was encountered.]

-121 Invalid character in number
[An invalid character for the data type being parsed was encountered; for example, an alpha in a decimal numeric.]

-144 Character data too long
[The <char_data> element contains more than twelve characters (see IEEE 488.2, 7.7.1.4).]

-161 Invalid block data
[A block data element was expected, but was invalid for some reason (see IEEE 488.2, 7.7.6.2); for example, an END message was received before the length was satisfied.]

3- Execution error

Error Number **Error description [description/explanation/examples]**

-200 Execution error
[This is a generic syntax error for devices that cannot detect more specific erors. This code indicates only an Executiion Error as defined in IEEE 488.2, 11.5.1.1.5 has occured.]

-210 Trigger error

-211 Trigger ignored
[Indicates that a GET, *TRG, or triggering signal was received and recognized by the device but was ignored because of device timing considerations; for example, the device was not ready to respond.]

-213 Init ignored
[Indicates that an initiate command was ignored as another one was already in progress.]

-221 Settings conflict
[Indicates that a legal program data element was parsed but could not be executed due to the current device state.]

-222 Data out of range
[Indicates that a legal program data element was parsed but could not be executed because the interpreted value was outside the legal range as defined by the device.]

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-223 Too much data
[Indicates that a legal program data element of block, expression, or string type was received that contained more data than the device could handle due to memory or related device-specific requirements.

-224 Illegal parameter value
[Used where exact value, from a list of possibles, was expected. For example, the "TRIG:BUS HOLD" command generates an error because the parser expected the value ON or OFF in place of HOLD.]

-241 Hardware missing
[Indicates that a legal program command or query could not be executed because of missing device hardware; for example an option was not installed or the user wants to set a voltage on a specific channel as the channel is in current mode.]

4- Device-specific error

Error Number	Error description [description/explanation/examples]

-300 Device-specific error
[Indicates only that a Device-Dependent Error as defined in IEEE 488.2, 11.5.1.1.6 has occured. For example, the autozero calibration was aborted.]

-350 Queue overflow
[A specific code entered into the queue in lieu of the code that caused the error. This code indicates that there is no room in the queue and an error occured but was not recorded.]

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VXIbus WORD SERIAL COMMANDS

All of the following commands are supported by this module:

- Abort Normal Operation
- Assign Interrupter Line
- Asynchronous Mode Control
- Begin Normal Operation
- Byte Available
- Byte Request
- Clear
- Control Event
- End Normal Operation
- Read Interrupter Line
- Read Interrupters
- Read Protocol
- Read Protocol Error
- Read STB
- Trigger

1 - Abort Normal Operation

This command is used to cause a device to cease normal operation. Upon receipt of this command the device returns to its default configuration, aborting all operation. The aborted state is defined as follows: pending interrupts are unasserted, no new bus requests or interrupts may be asserted. The device is in inactive state and is ready to accept commands.

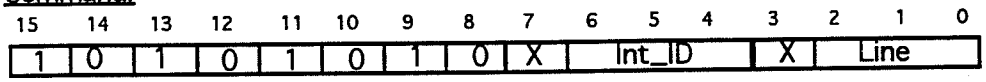
Command: $C8FF_{16}$

The response data is placed in the Data Low Register
Response: $FFFE_{16}$

2 - Assign Interrupter Line

This command is used to assign a VMEbus IRQ line to a particular Interrupter in the servant device.

Command:



- X: Don't care
- Int_ID: This is a unique identifier of the particular Interrupter being assigned. For this module the field 'Int_ID' must take value '001'.
- Line: This is the VMEbus IRQ line number. A value of zero indicates that the Interrupter is to be disconnected.

Action: if Int_ID = 001 save value of 'Line'

The response data is placed in the Data Low Register.
Response: if Int_ID = 001 --> $FFFE_{16}$
else --> $7FFE_{16}$

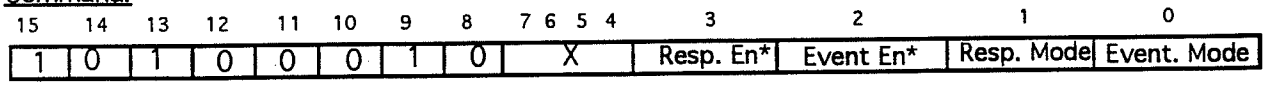
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3 - Asynchronous Mode Control

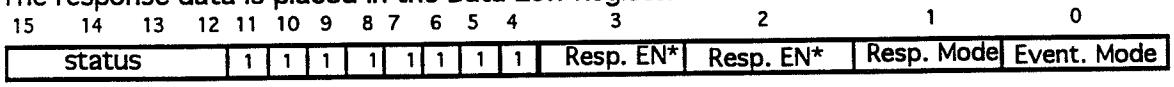
This command is used by a commander to direct path of events and responses.

Command:



- X: don't care
- Resp. En*: a zero (0) enables generation of responses. A one (1) disables generation of responses.
- Event En*: a zero (0) enables generation of events. A one (1) disables generation of events.
- Resp. Mode: A one indicates that responses should be sent as signals. A zero indicates that responses should be sent as interrupts.
- Event. Mode: A one indicates that events should be sent as signals. A zero indicates that events should be sent as interrupts.

The response data is placed in the Data Low Register



- Status: This field indicates the execution status of the command
  - F_{16}: The command successfully completed as expected.
  - 7_{16}: Command failed. A requested option is not supported.
- Resp. En*: a zero indicates that the generation of responses is enabled. A one indicates that the generation of responses is disabled.
- Event En*: a zero indicates that the generation of events is enabled. A one indicates that the generation of events is disabled.
- Resp. Mode: A one indicates that responses are being sent as signals. A zero indicates that responses are being sent as interrupts.
- Event. Mode: A one indicates that events are being sent as signals. A zero indicates that events are being sent as interrupts.

4 - Begin Normal Operation

This command notifies the device that it can begin normal operation now.

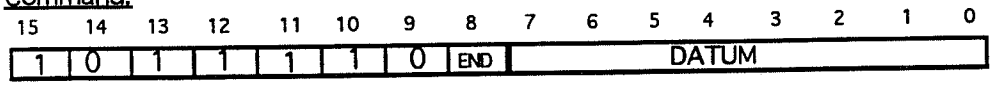
Command: $FCFF_{16}$ or $FDFE_{16}$

The response data is placed in the Data Low Register: $FFFE_{16}$

5 - Byte Available

This command is used by a commander to send a byte of data to a servant device. The END field identifies that this is the last byte of the message.

Command:



Response: none

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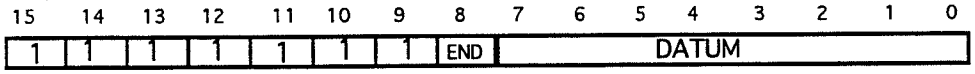
6 - Byte request

This command is used by a commander to read a byte of data from a servant device.

Command: $AEFF_{16}$

The response data is placed in the Data Low Register. The END field is used to indicate the last byte of the message.

Response:



7 - Clear

This command is used by a commander to cause a servant device to clear the VXIbus interface and any pending operations. Any initiated operations in the receiving device are undisturbed.

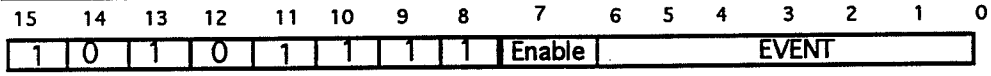
Command: $FFFF_{16}$

Response: none

8 - Control Event

This command is used by a commander to selectively enable the generation of events by a servant. A one in the enable field enables the generation of the specific event. A zero in the enable field disablles the generation of the specific event.

Command:



• Event: These bits (6 <- 0) are the identifying bits (14 <- 8) of the event being enabled/disabled. See Section E.4, "Protocol Events", for further information.

The response data is placed in the Data Low Register.

Responses:

- $FFFE_{16}$: the command successfully completed.
- $7FFE_{16}$: command failed. The event referenced is not generated by this device.

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9 - End Normal Operation

This command is used to cause a commander to cease normal operation in an orderly manner. Upon receipt of this command the commander issues the *End Normal Operation* command to all of its Message Based Servants. The commander is responsible for halting all its servants. The "ended" state is defined as follows: pending interrupts are unasserted, no new bus requests or interrupts may be asserted. The device is in inactive state and is ready to accept commands.

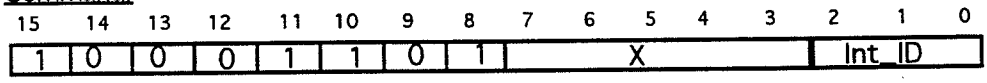
Command: $C9FF_{16}$

The response data is placed in the Data Low Register.
Response: $FFFE_{16}$

10 - Read Interrupter Line

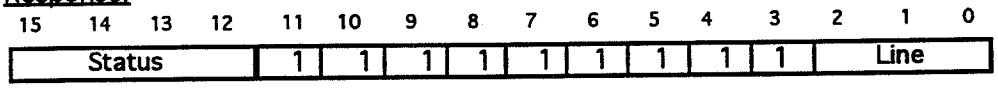
This command is used to determine to which VMEbus IRQ line a particular interrupter in the servant device is connected.

Command:



- X: Don't care
- Int_ID: This is a unique identifier of the particular Interrupter being queried. For this module the field 'Int_ID' must take value '001'.

The VMEbus IRQ line number is placed in the Data Low Register.
Response:



- Status: This field indicates the execution status of the command.
  - F_{16}: The command successfully completed.
  - 7_{16}: Command failed; the Interrupter referenced in the Int_ID field is unknown to this device.
- Line: This is the VMEbus IRQ line number. A value of zero indicates that the Interrupter is to be disconnected.

11 - Read Interrupters

This command is used to determine the number of Interrupters within a servant device.

Command: $CAFF_{16}$

The number of Interrupters is placed in the Data Low Register.
Response: $FFF9_{16}$ (one interrupter).

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12- Read Protocol

This command is used by a commander to find out what protocols in addition to the Word Serial protocol that the servant supports.

Command: $DFFF_{16}$

The protocol support word is placed in Data Low Register.
Response: $FC2B_{16}$

13- Read Protocol Error

This command is used by a commander to tell a servant device to report its current error state as the 16 bit response to this command. After responding to this command, the servant will reset its current error state to "No Error".

Command: $CDFF_{16}$

The error codes are placed in the Data Low Register.
Several responses are possible:

No error: $FFFF_{16}$

Multiple Queries: $FFFD_{16}$
The device was requested to overwrite previous unread response data.

Unsupported command: $FFFC_{16}$
This device has received a command that it does not implement.

DIR violation: $FFFB_{16}$
This device has received a command that violates the DIR handshake.

DOR violation: $FFFA_{16}$
This device has received a command that violates the DOR handshake.

Read Ready violation: $FFF9_{16}$
This device has received a command that violates the Read Ready handshake.

Write Ready violation: $FFF8_{16}$
This device has received a command that violates the Write Ready handshake.

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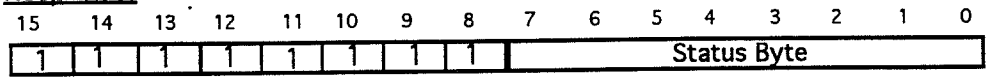
14- Read STB

This command is used by a commander to read the status word from a servant device.

Command: $CFFF_{16}$

The status byte is placed in the Data Low Register.

Response:



15- Trigger

This command is used by a commander to cause a servant device to trigger any previously armed operation.

Command: $EDFF_{16}$

Response: none

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SECTION 8

SCHEMATICS

8-1	**F2910101**	Schematic, MOTHER Board
8-2	**F2910105**	Schematic, VXI INTERFACE Board
8-3	**F2910106**	Schematic, DC/DC CONVERTER Board
8-4	**F2910104**	Schematic, ANALOG INPUTS Board
8-5	**F2910103**	Schematic, ANALOG OUTPUTS Board
8-6	**F2910102**	Schematic, DIGITAL INPUTS/OUTPUTS Board

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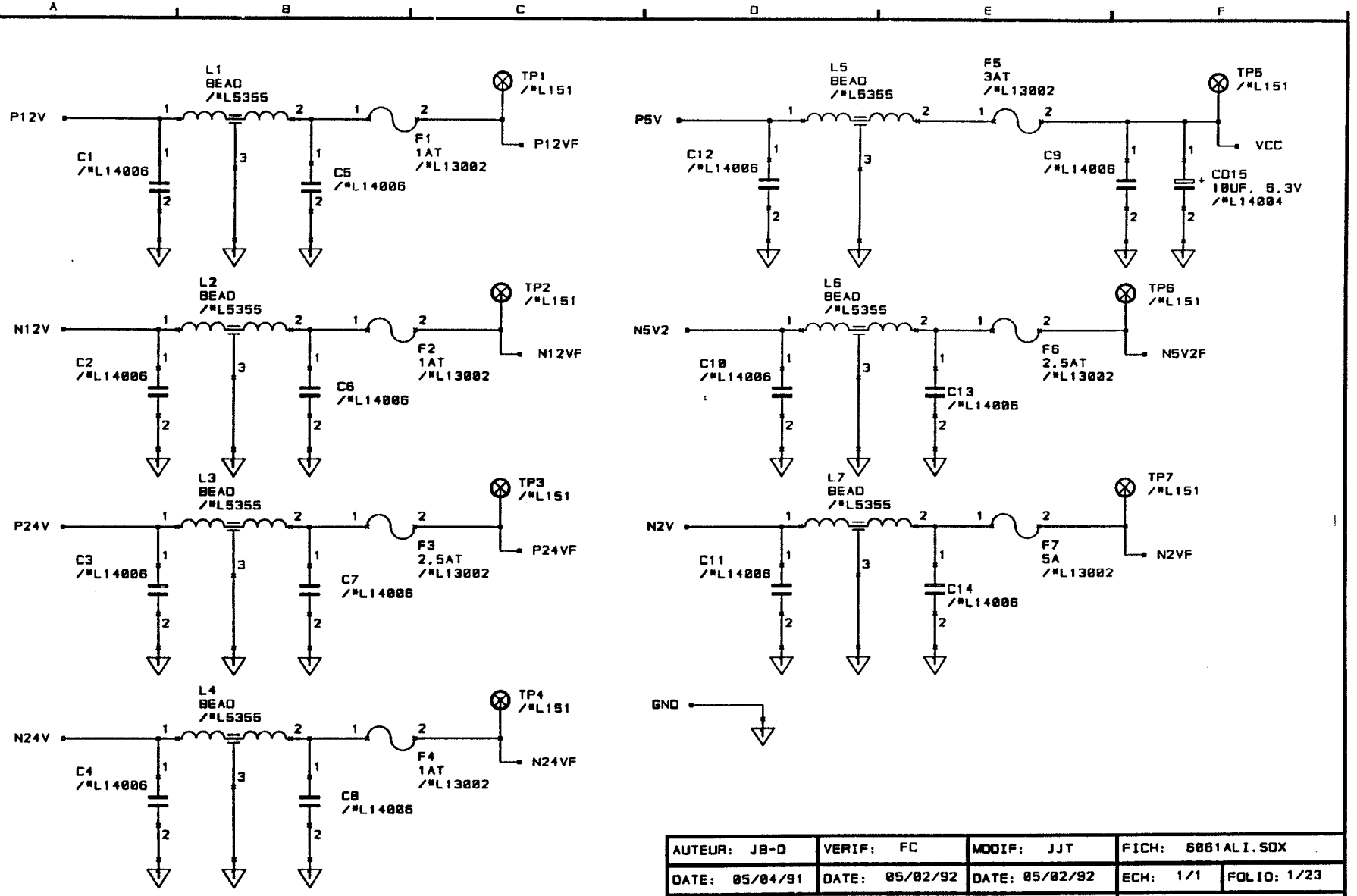
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SECTION 8-1

F2910101

SCHEMATICS of the MOTHER BOARD

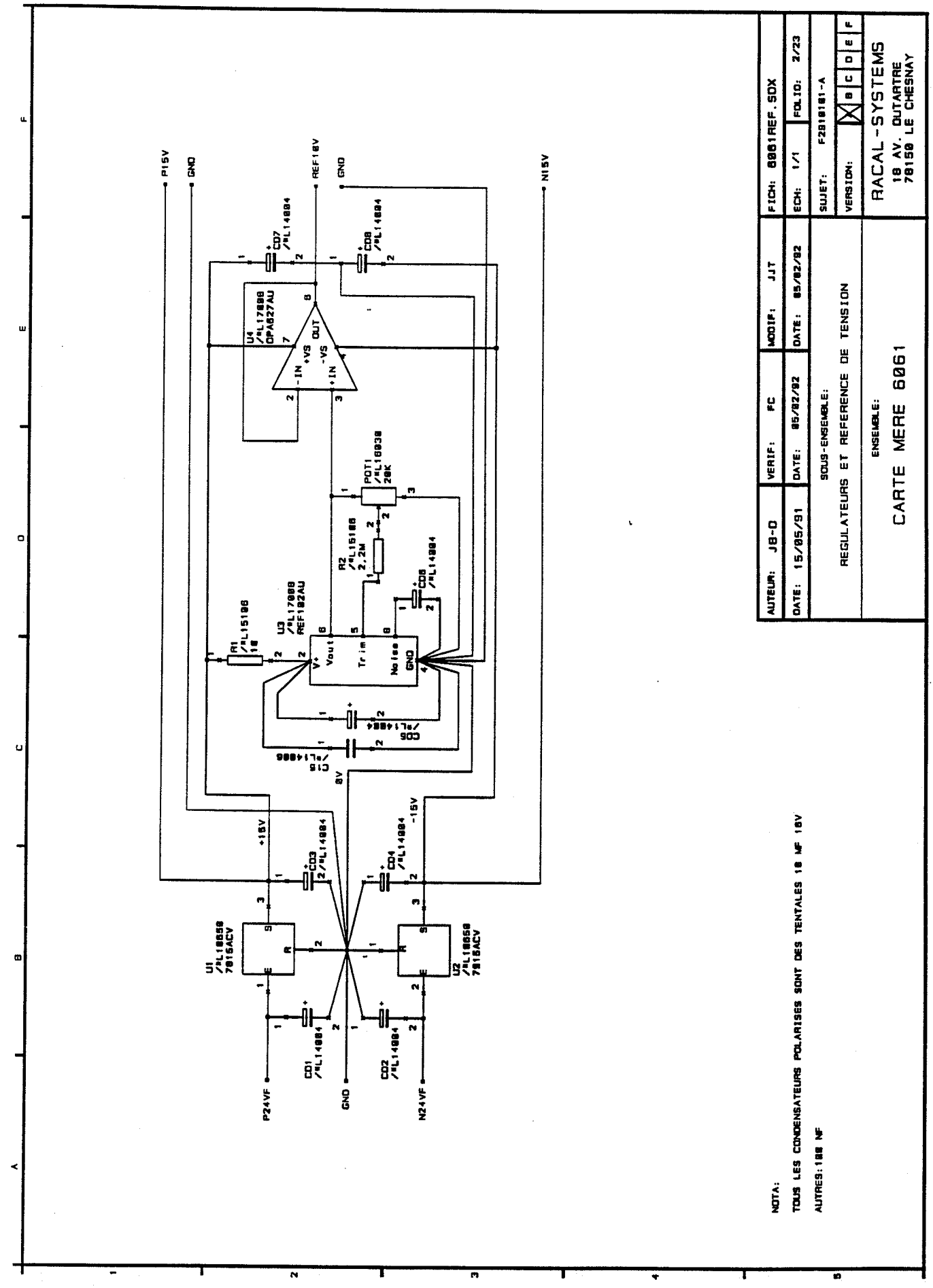
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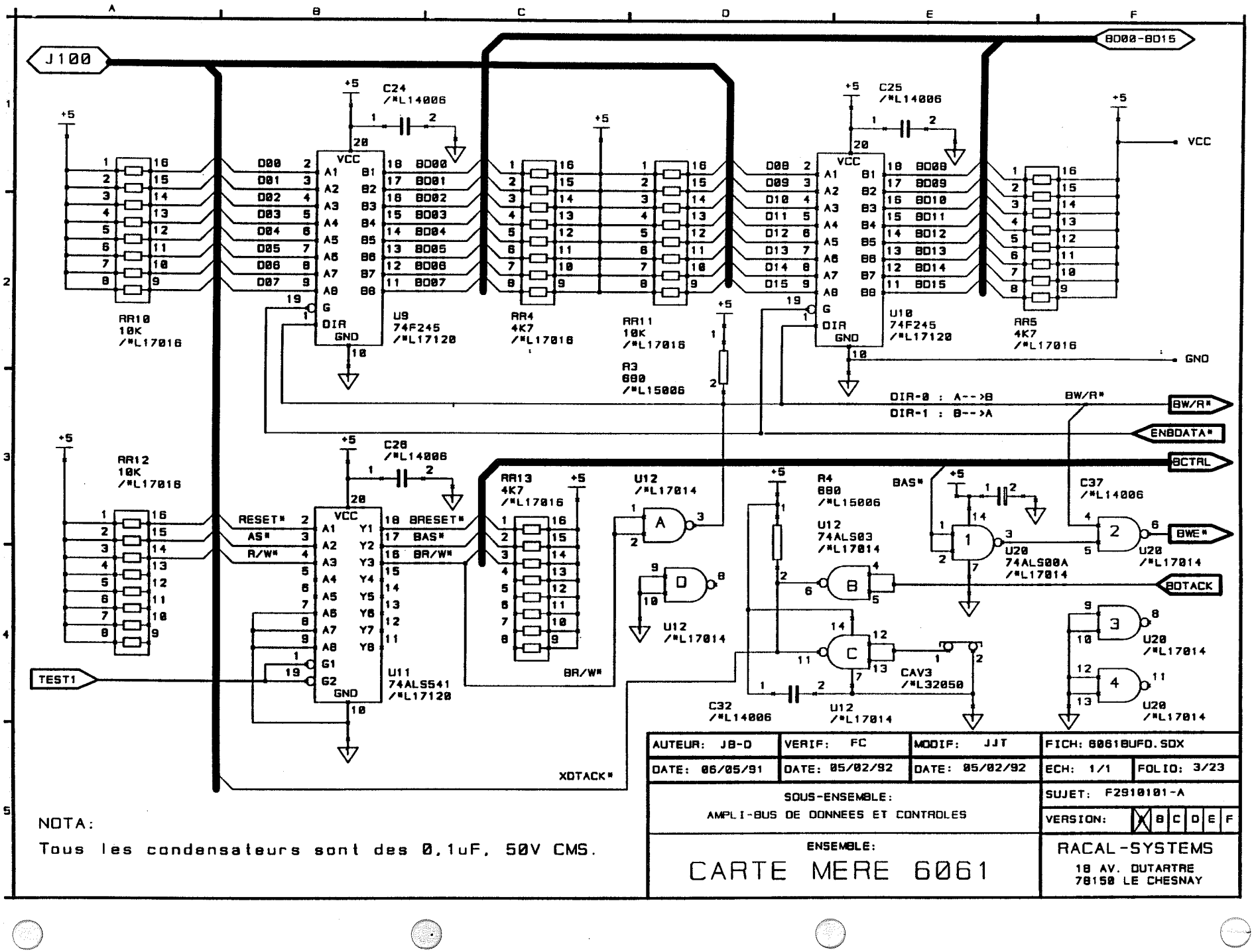
NOTA : TOUS LES CONDENSATEURS SONT DES DES CHIPS CMS
0,1uF, 50V, SAUF INDICATIONS CONTRAIRES.

AUTEUR: JB-D	VERIF: FC	MODIF: JJT	FICH: 6061ALI.SOX	
DATE: 05/04/91	DATE: 05/02/92	DATE: 05/02/92	ECH: 1/1	FOLIO: 1/23
SOUS-ENSEMBLE: FILTRES - FUSIBLES			SUJET: F2910101-A	
			VERSION: X B C D E F	
ENSEMBLE: CARTE MERE 6061			RACAL-SYSTEMS 18 AV. OUTARTRE 78150 LE CHESNAY	

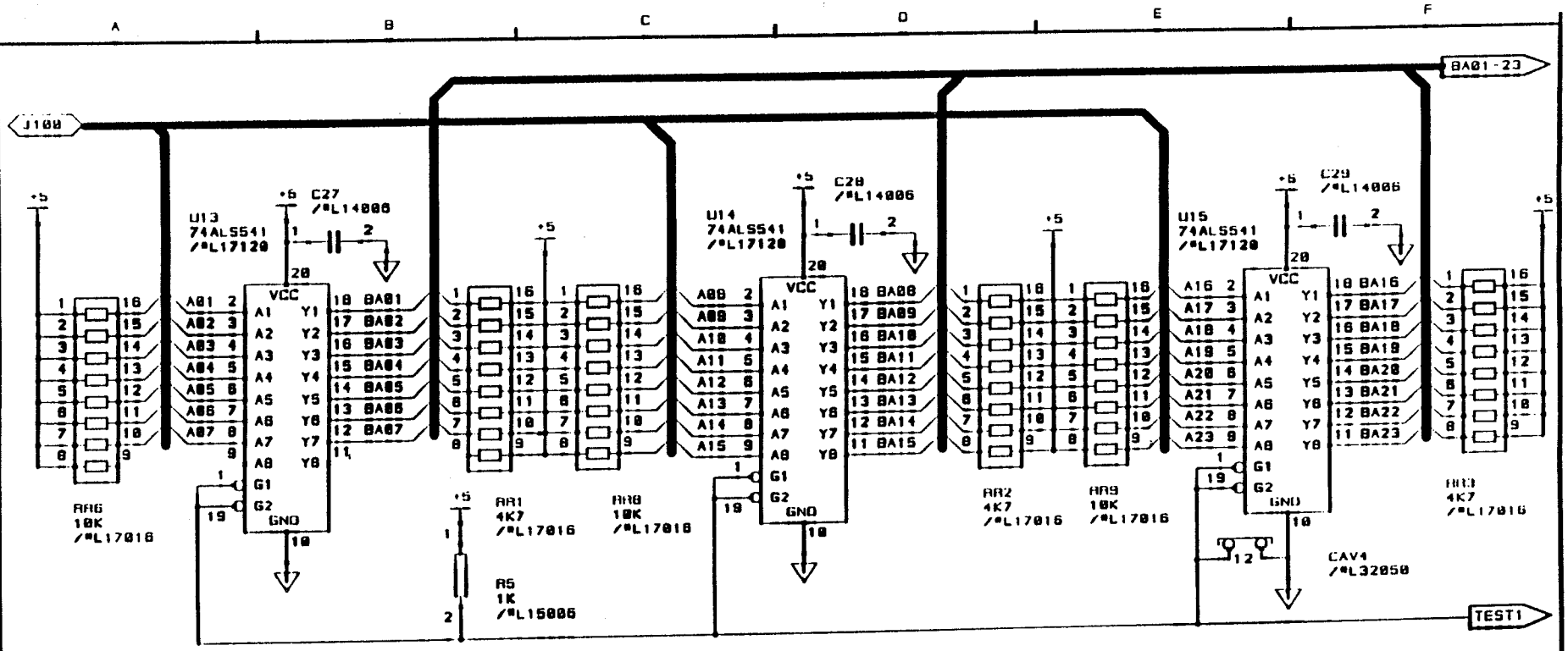
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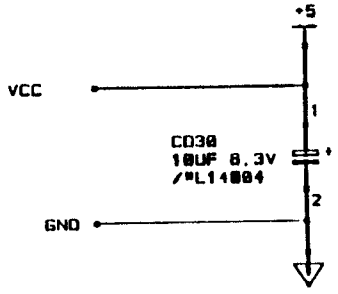


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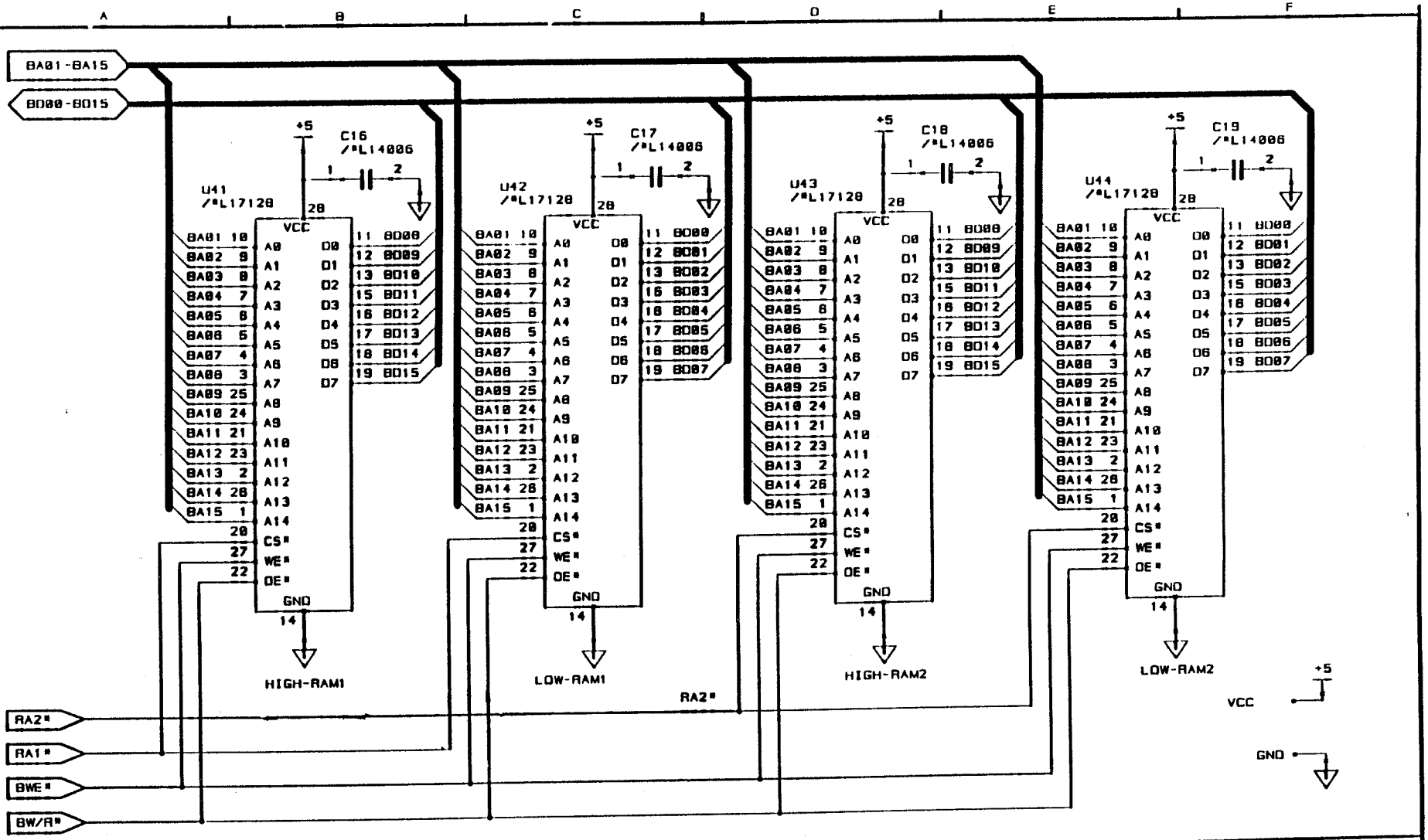
NOTA : TOUS LES CONDENSATEURS SONT DE 0.1uF, 50V
SAUF INDICATIONS CONTRAIRES

MODIF JJT	DATE 05/02/92	
MODIF FC	DATE 24/06/91	COMMENTAIRES

AUTEUR: JB-D	VERIF: FC	FICH: 6061BUFA.SDX
DATE: 25/04/91	DATE: 05/02/92	ECH: 1/1 FOLIO: 4/23
SOUS-ENSEMBLE: AMPLI BUS ADRESSES		SUJET: F2910101-A
ENSEMBLE: CARTE MERE 6061		VERSION: X B C D E F

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NOTA : HIGH-RAM2 ET LOW-RAM2 IMPLANTEES MAIS NON EQUIPEES

RAM : 32K*8

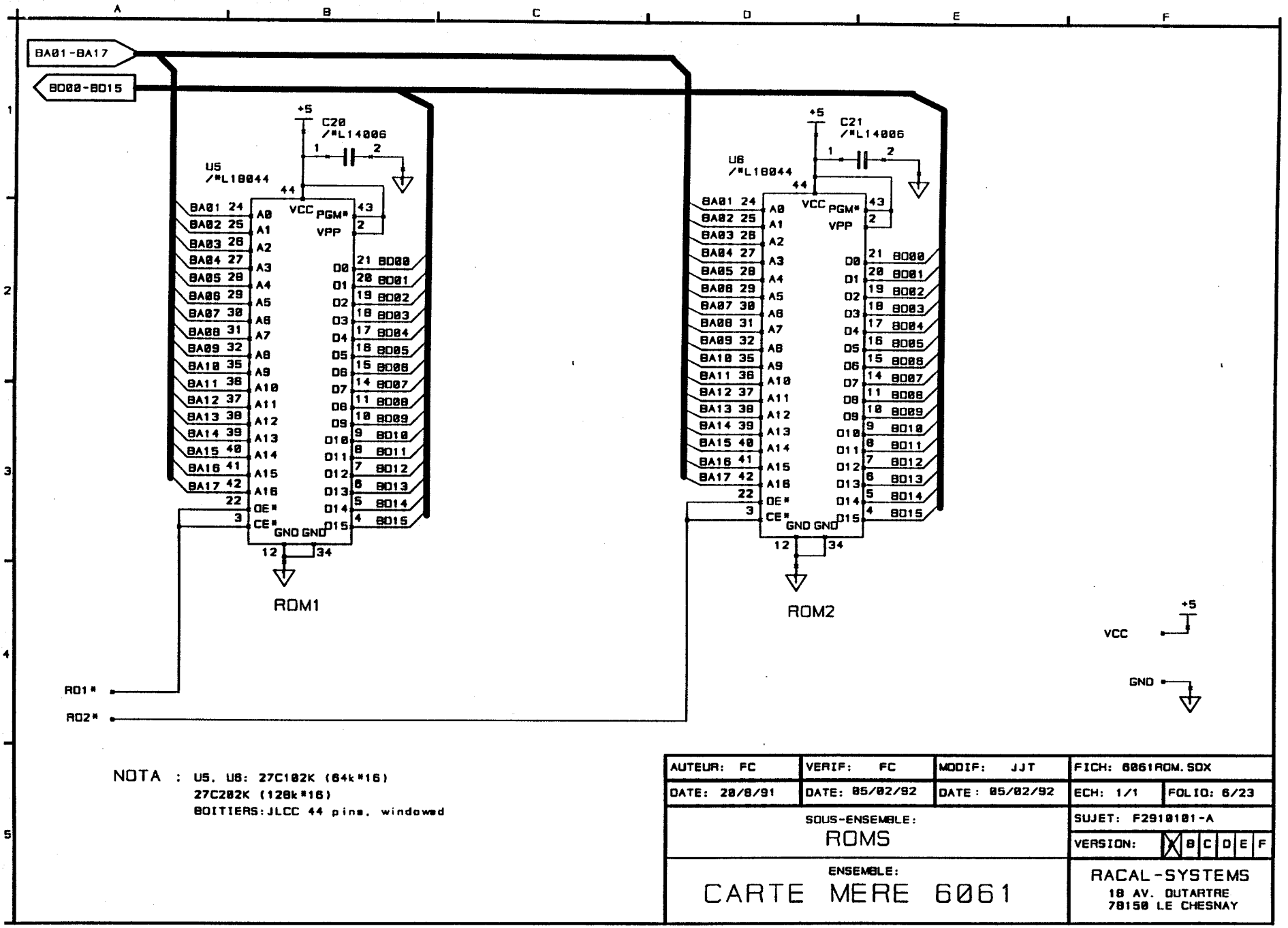
TYPE

HM 62256-LFP-12T
KM 62256 ALG-10
MSM5278S

BOITIERS: SOIC 28

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DATE: 05/04/91	DATE: 05/02/92	DATE: 05/02/92	ECH: 1/1 FOLIO: 5/23
SOUS-ENSEMBLE: RAMS			SUJET: F2910101-A
			VERSION: X B C D E F
ENSEMBLE: CARTE MERE 6061			RACAL-SYSTEMS 18 AV. DUTARTRE 78150 LE CHESNAY

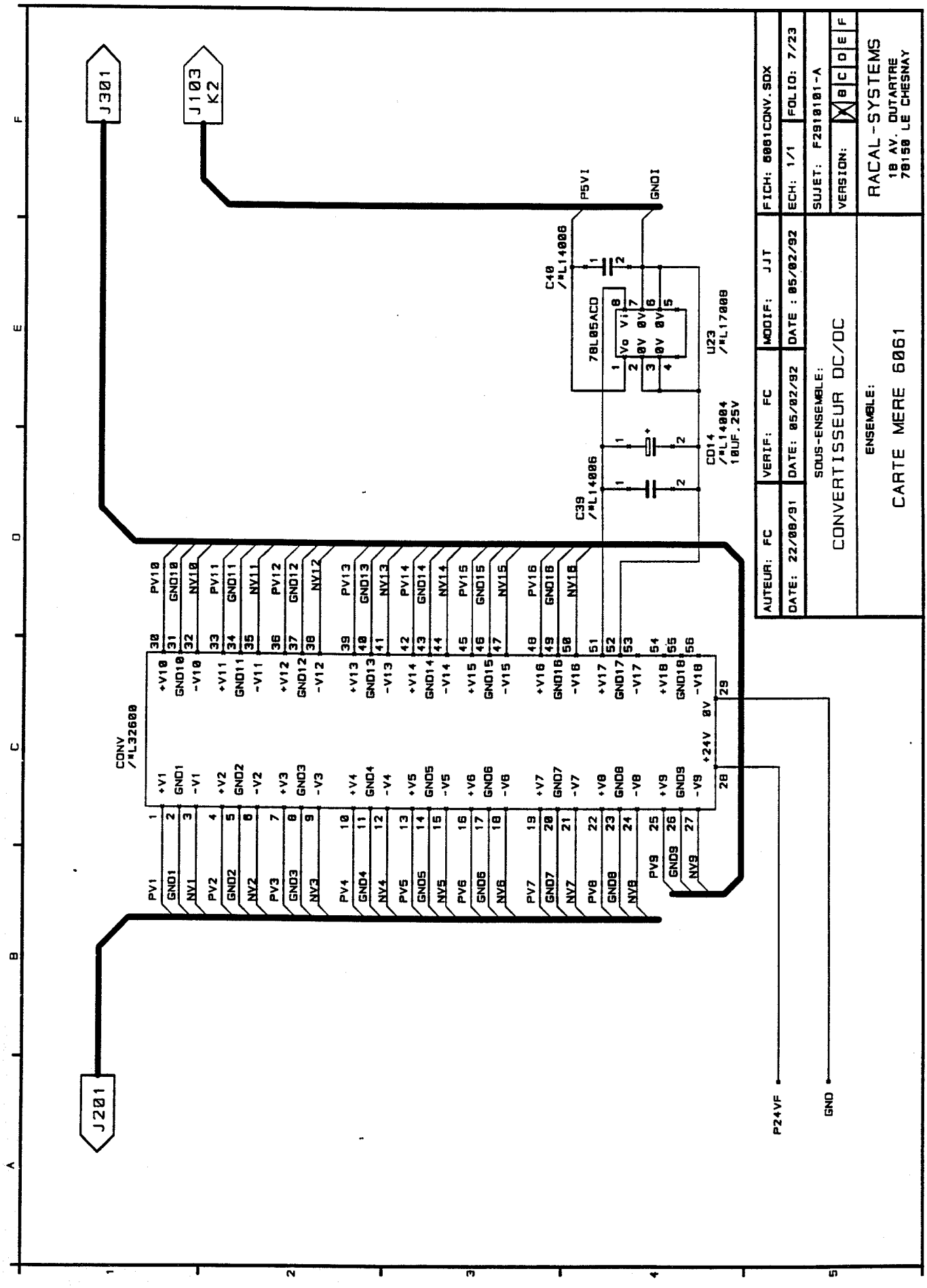
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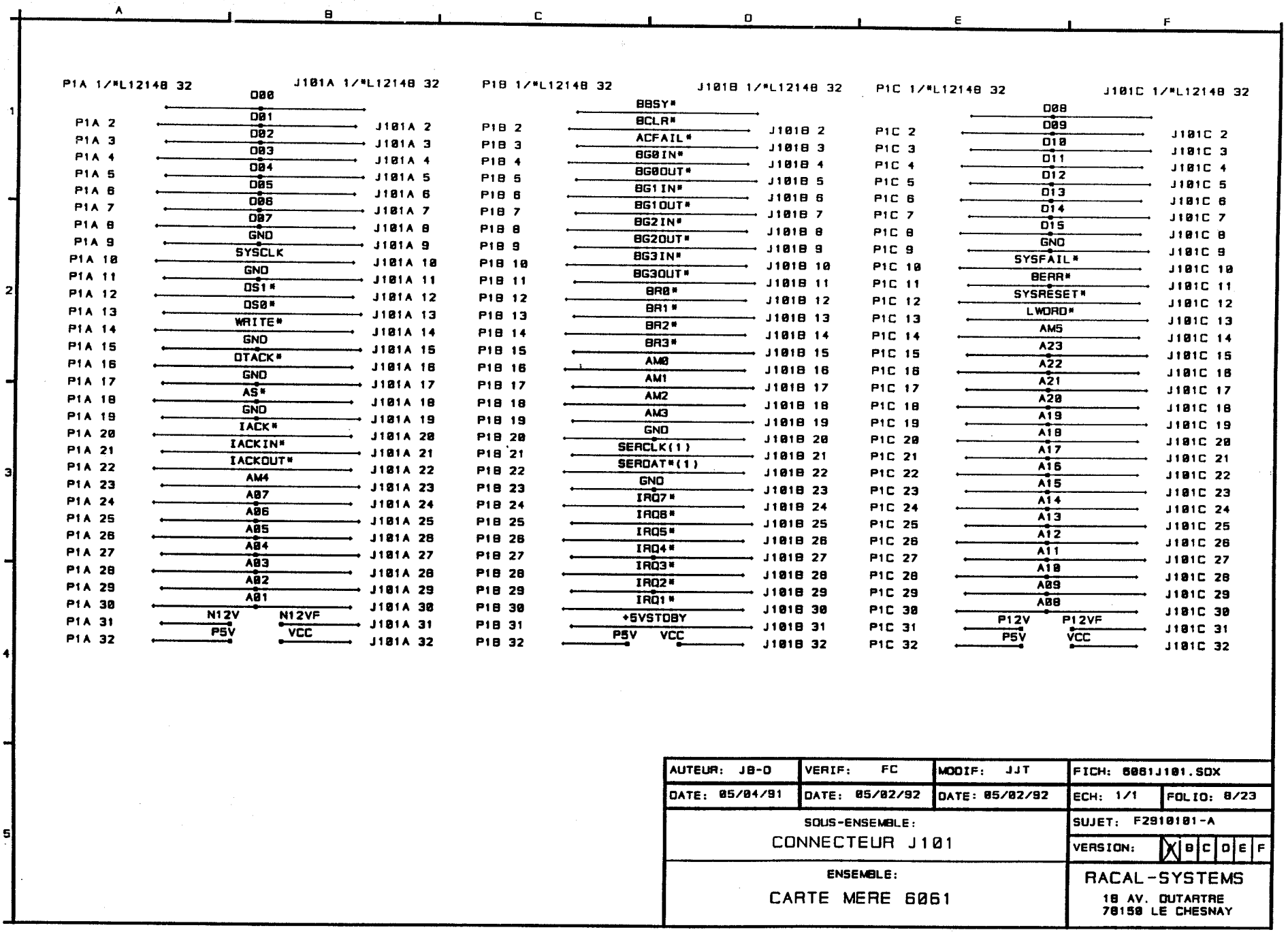
NOTA : U5, U6: 27C102K (64k*16)
27C202K (128k*16)
BOITIERS:JLCC 44 pins, windowed

AUTEUR: FC	VERIF: FC	MODIF: JJT	FICH: 6061ROM.SOX
DATE: 20/8/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 FOLIO: 6/23
SOUS-ENSEMBLE: ROMS			SUJET: F2910101-A
			VERSION: X B C D E F
ENSEMBLE: CARTE MERE 6061			RACAL-SYSTEMS 18 AV. OUTARTRE 78150 LE CHESNAY

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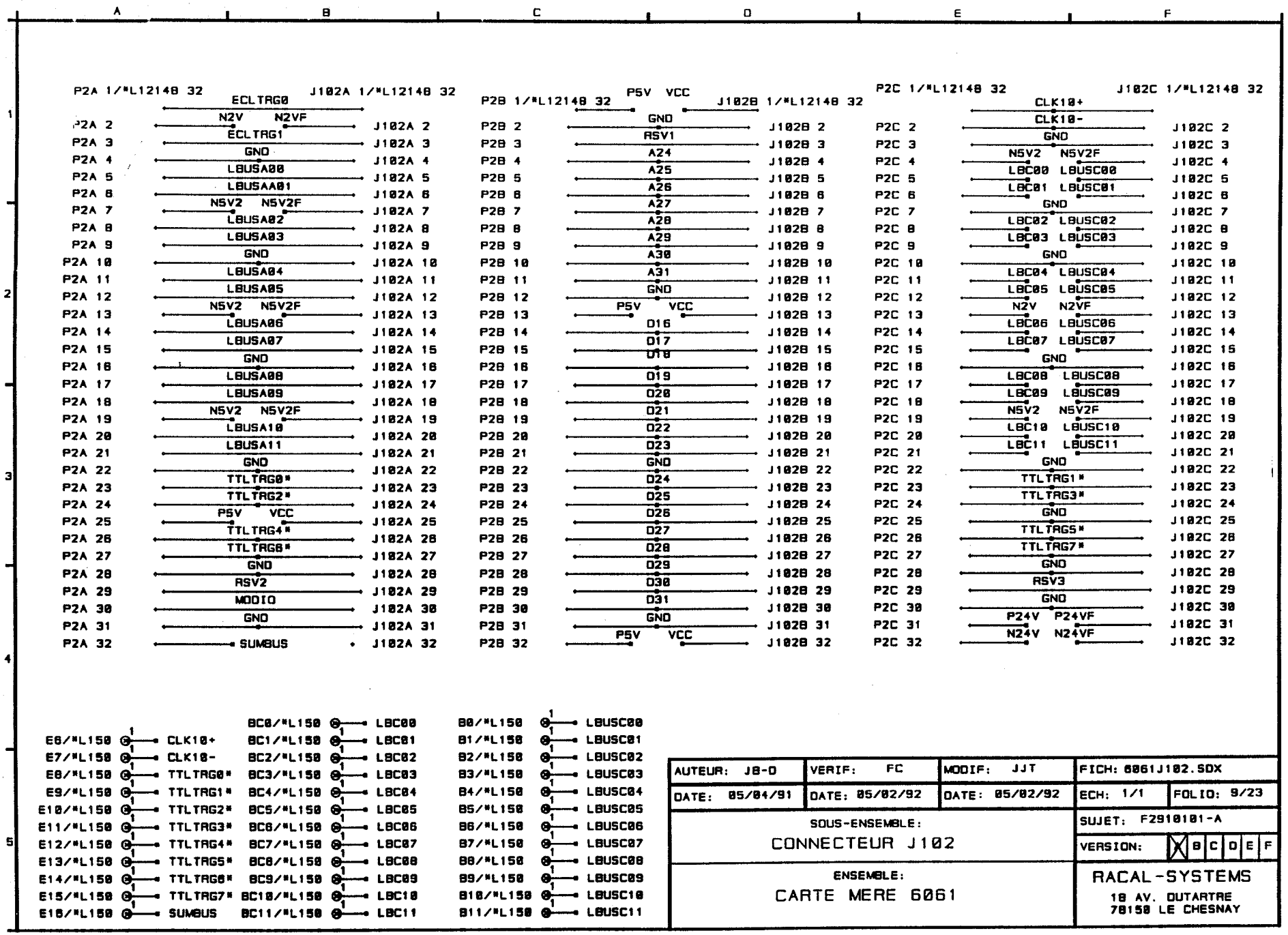


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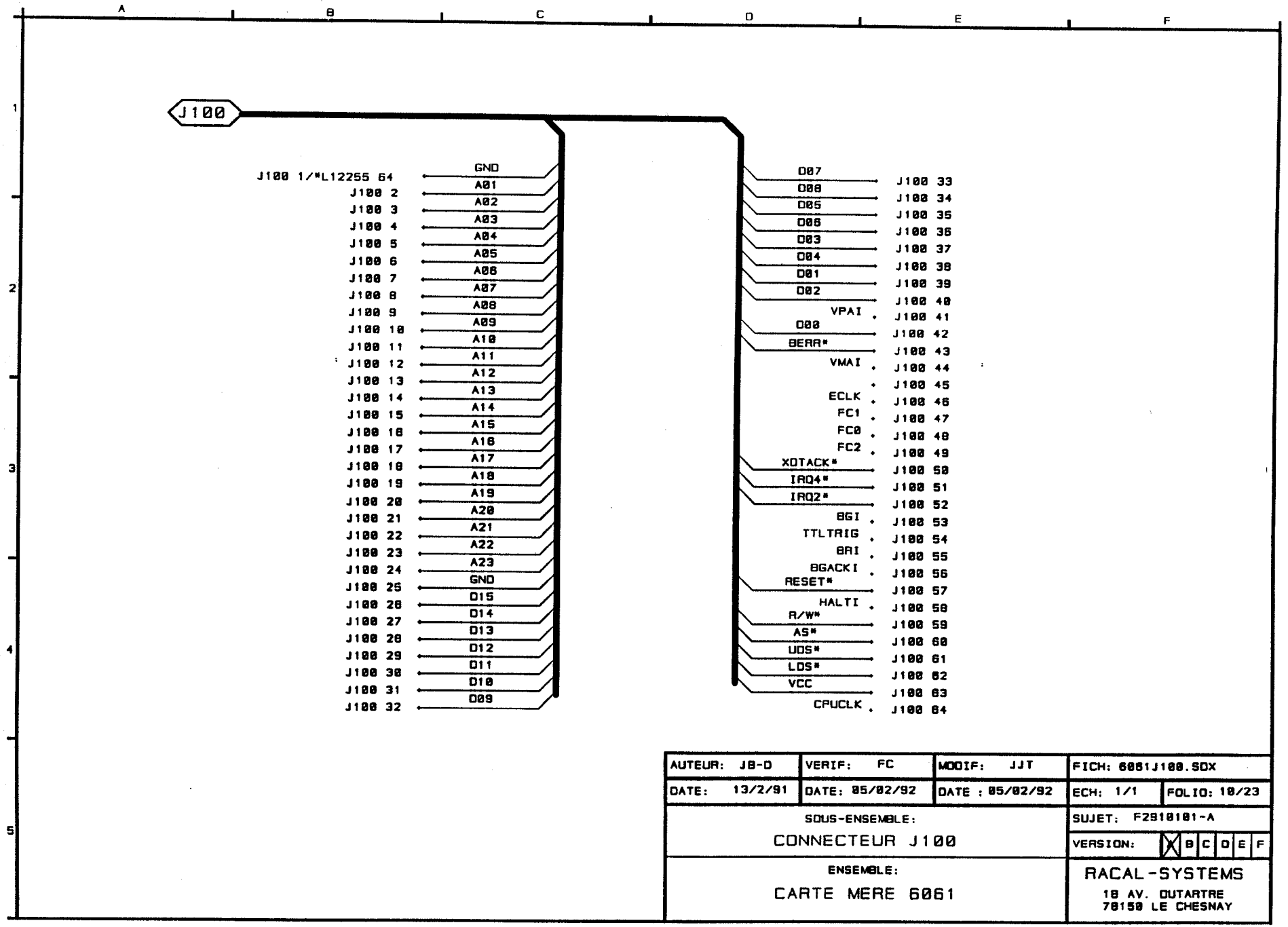


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SOUS-ENSEMBLE: CONNECTEUR J101			SUJET: F2910101-A
			VERSION: X B C D E F
ENSEMBLE: CARTE MERE 6061			RACAL-SYSTEMS 18 AV. DUTARTRE 78150 LE CHESNAY

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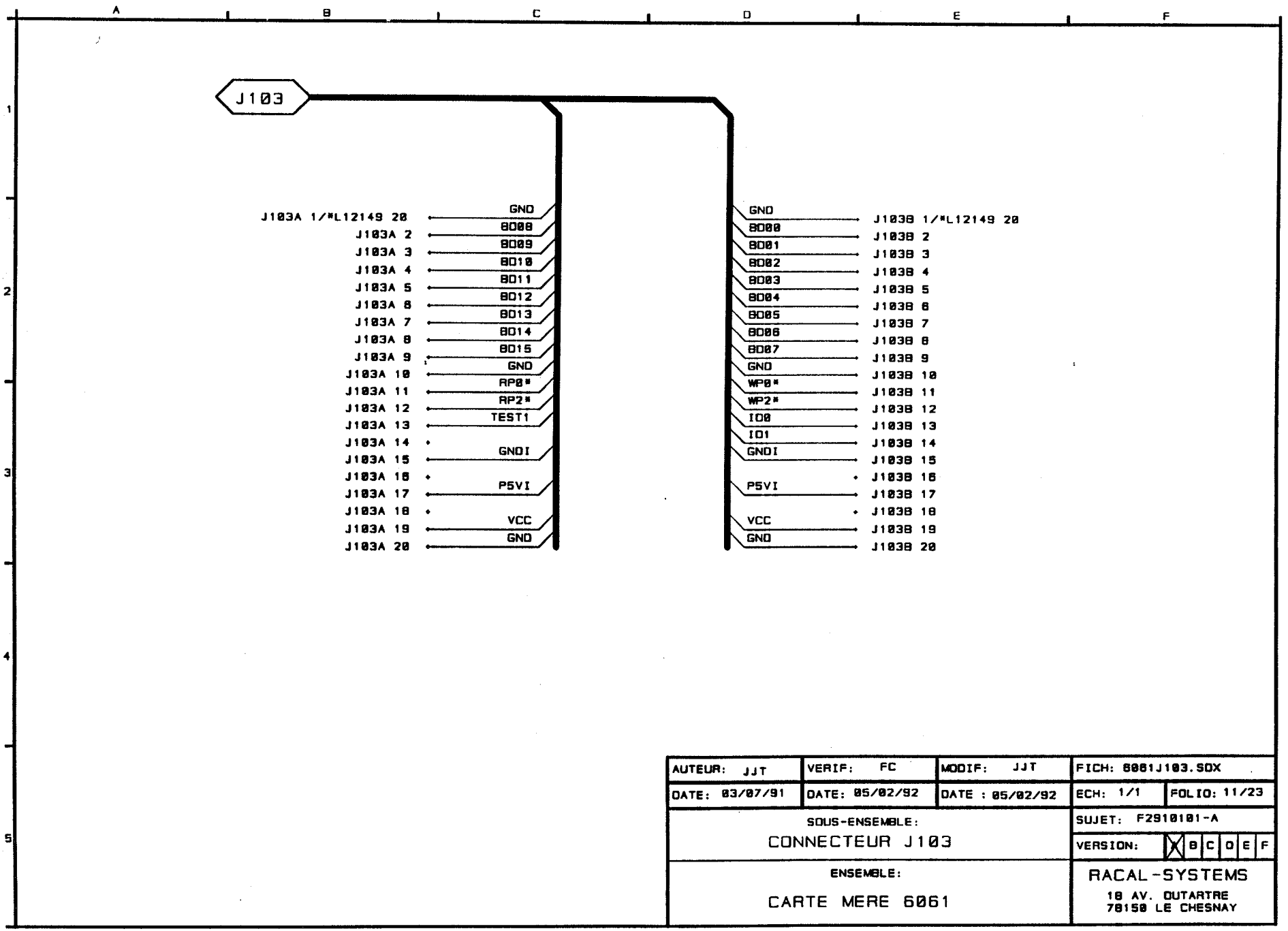


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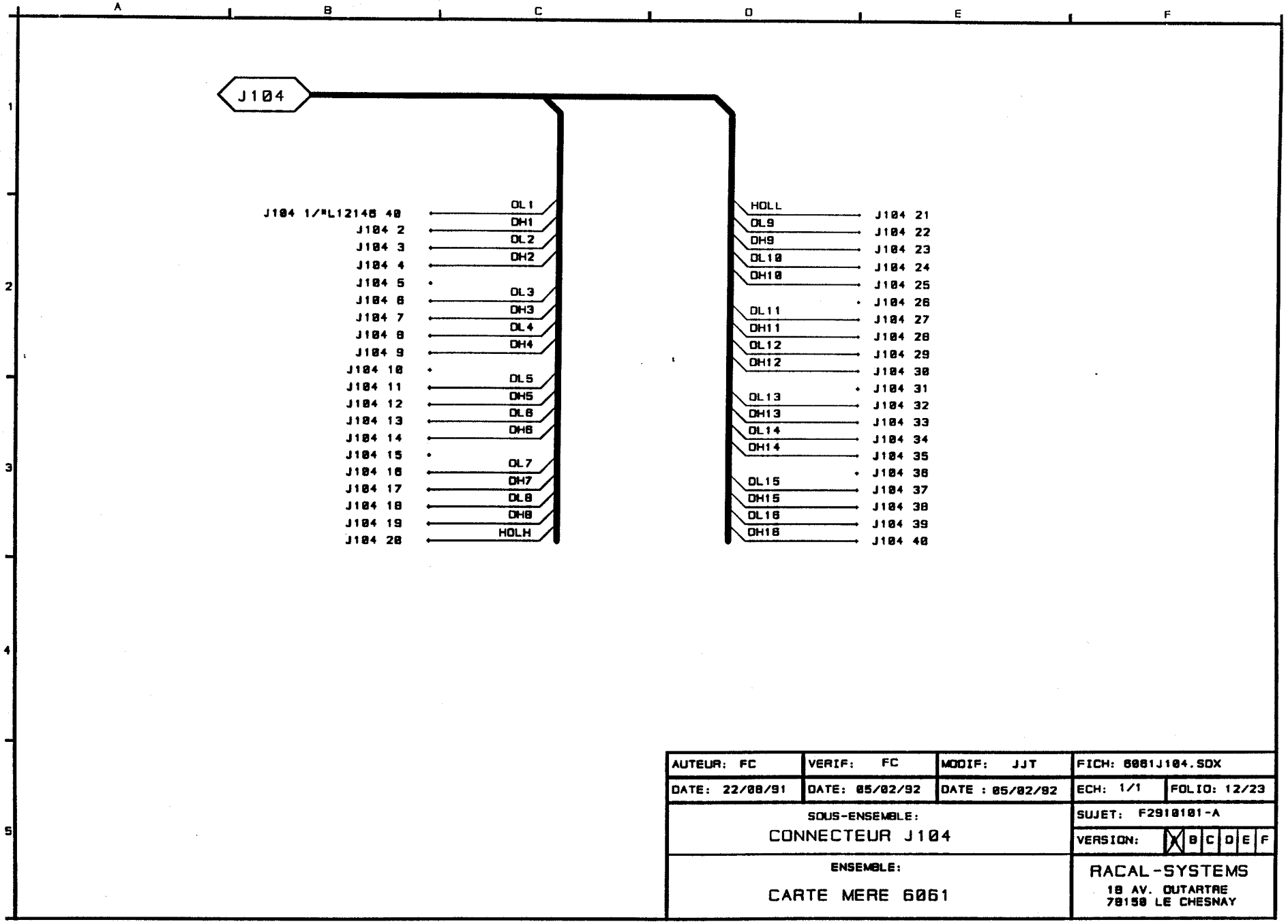
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DATE: 13/2/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 FOLIO: 10/23
SOUS-ENSEMBLE: CONNECTEUR J100			SUJET: F2S10101-A
			VERSION: [X] A B C D E F
ENSEMBLE: CARTE MERE 6061			RACAL-SYSTEMS 18 AV. OUTARTRE 78150 LE CHESNAY

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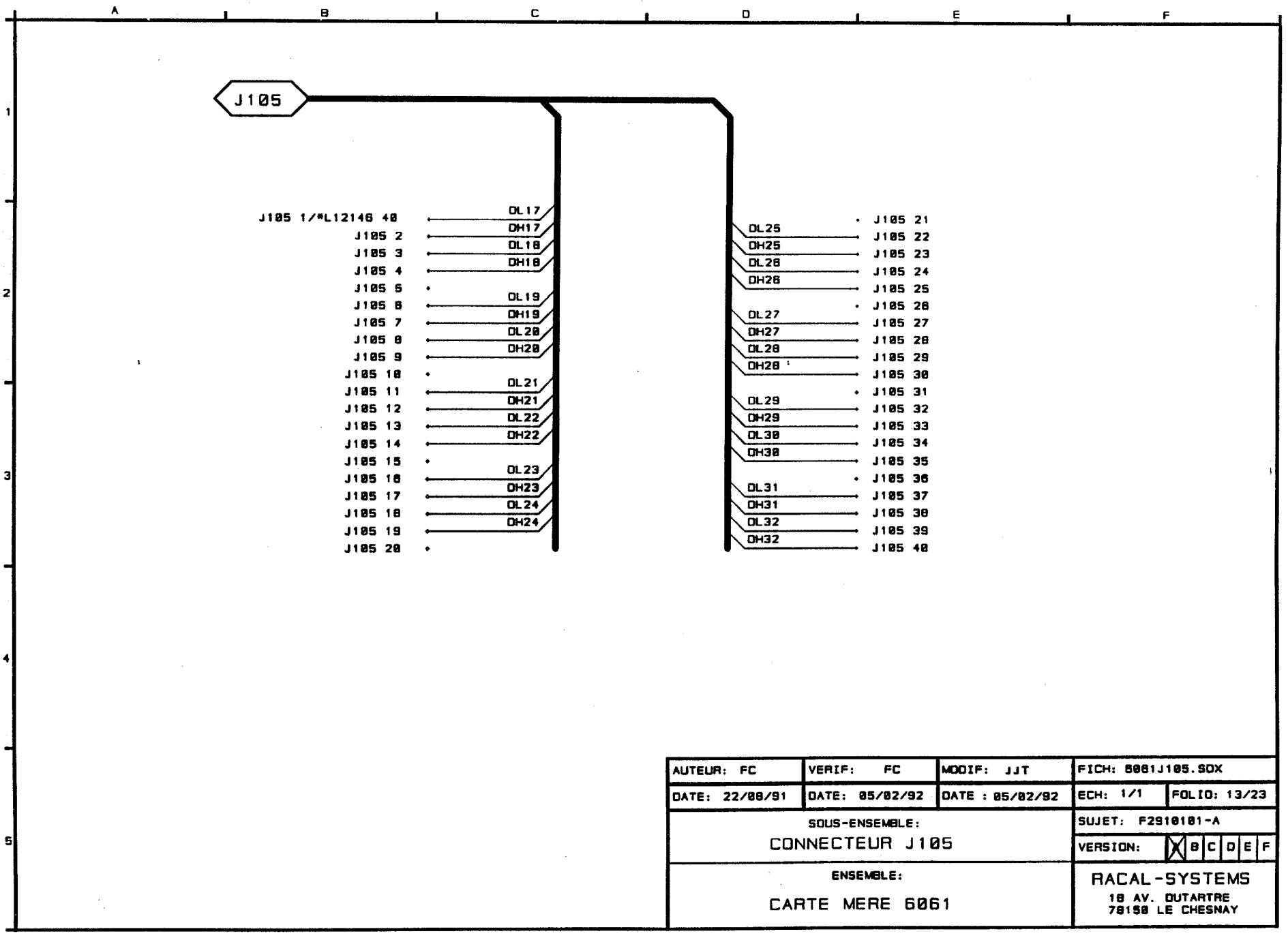
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DATE: 03/07/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 FOLIO: 11/23
SOUS-ENSEMBLE: CONNECTEUR J103			SUJET: F2910101-A VERSION: X B C D E F
ENSEMBLE: CARTE MERE 6061			RACAL-SYSTEMS 18 AV. OUTARTRE 78150 LE CHESNAY

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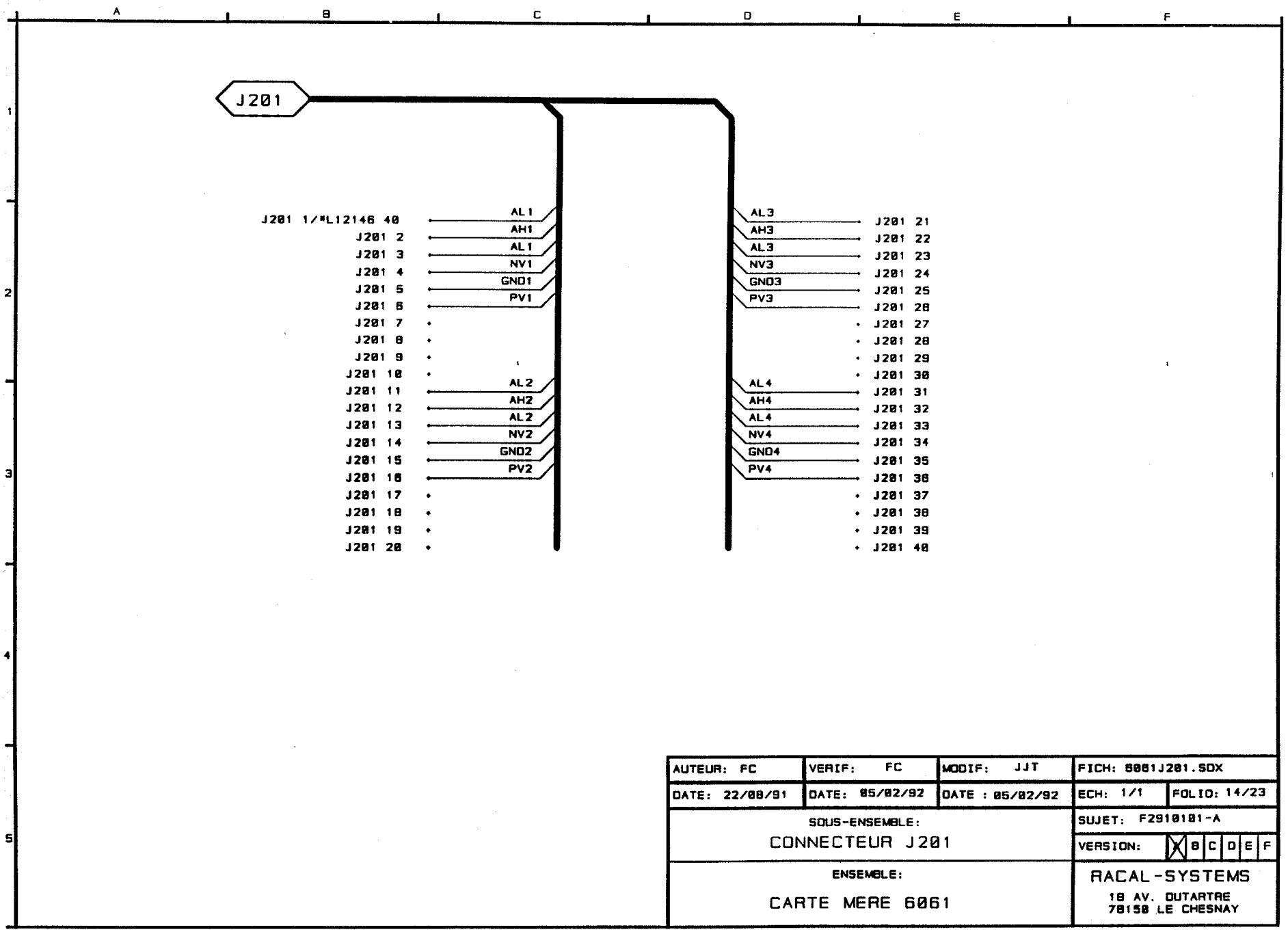
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SOUS-ENSEMBLE: CONNECTEUR J104			SUJET: F2910101-A
			VERSION: [X] B C D E F
ENSEMBLE: CARTE MERE 6061			RACAL-SYSTEMS 18 AV. OUTARTRE 78150 LE CHESNAY

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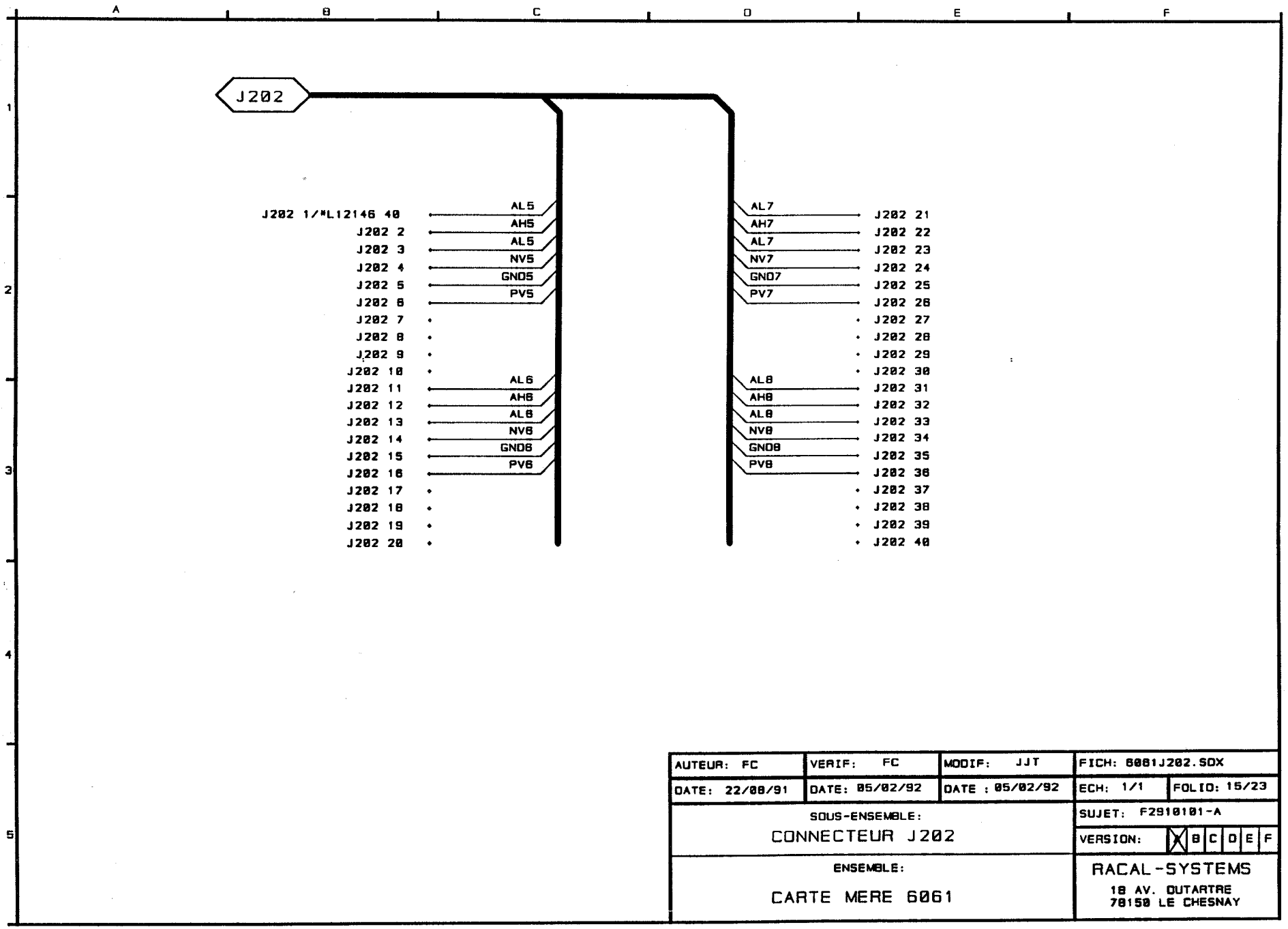
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SOUS-ENSEMBLE: CONNECTEUR J105			SUJET: F2910101-A
			VERSION: X B C D E F
ENSEMBLE: CARTE MERE 6061			RACAL-SYSTEMS 18 AV. DUTARTRE 78150 LE CHESNAY

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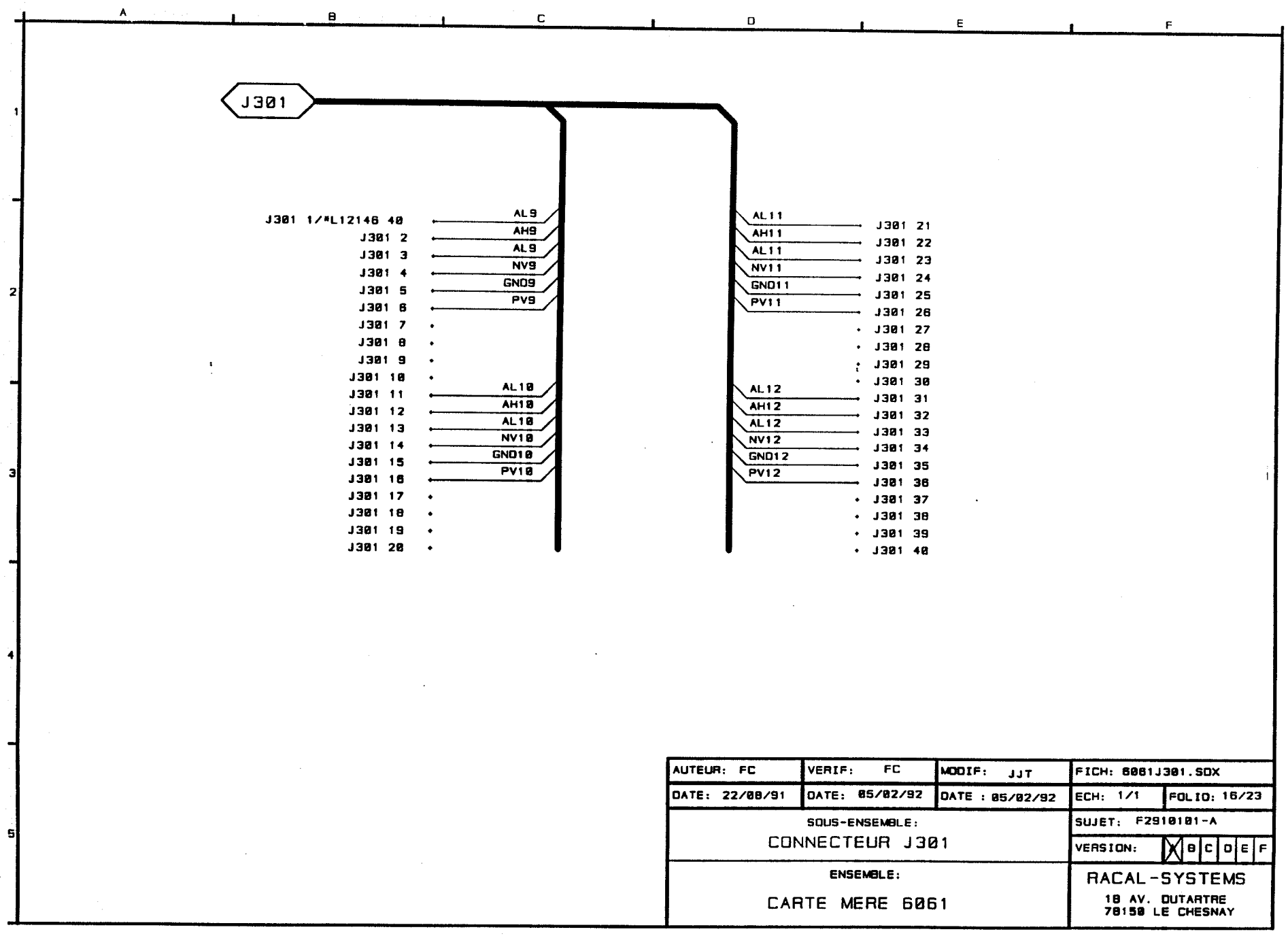
AUTEUR: FC	VERIF: FC	MODIF: JJT	FICH: 6061J201.SDX
DATE: 22/08/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 — FOLIO: 14/23
SOUS-ENSEMBLE: CONNECTEUR J201			SUJET: F2910101-A
			VERSION: [X] A B C D E F
ENSEMBLE: CARTE MERE 6061			RACAL-SYSTEMS 18 AV. OUTARTRE 78150 LE CHESNAY

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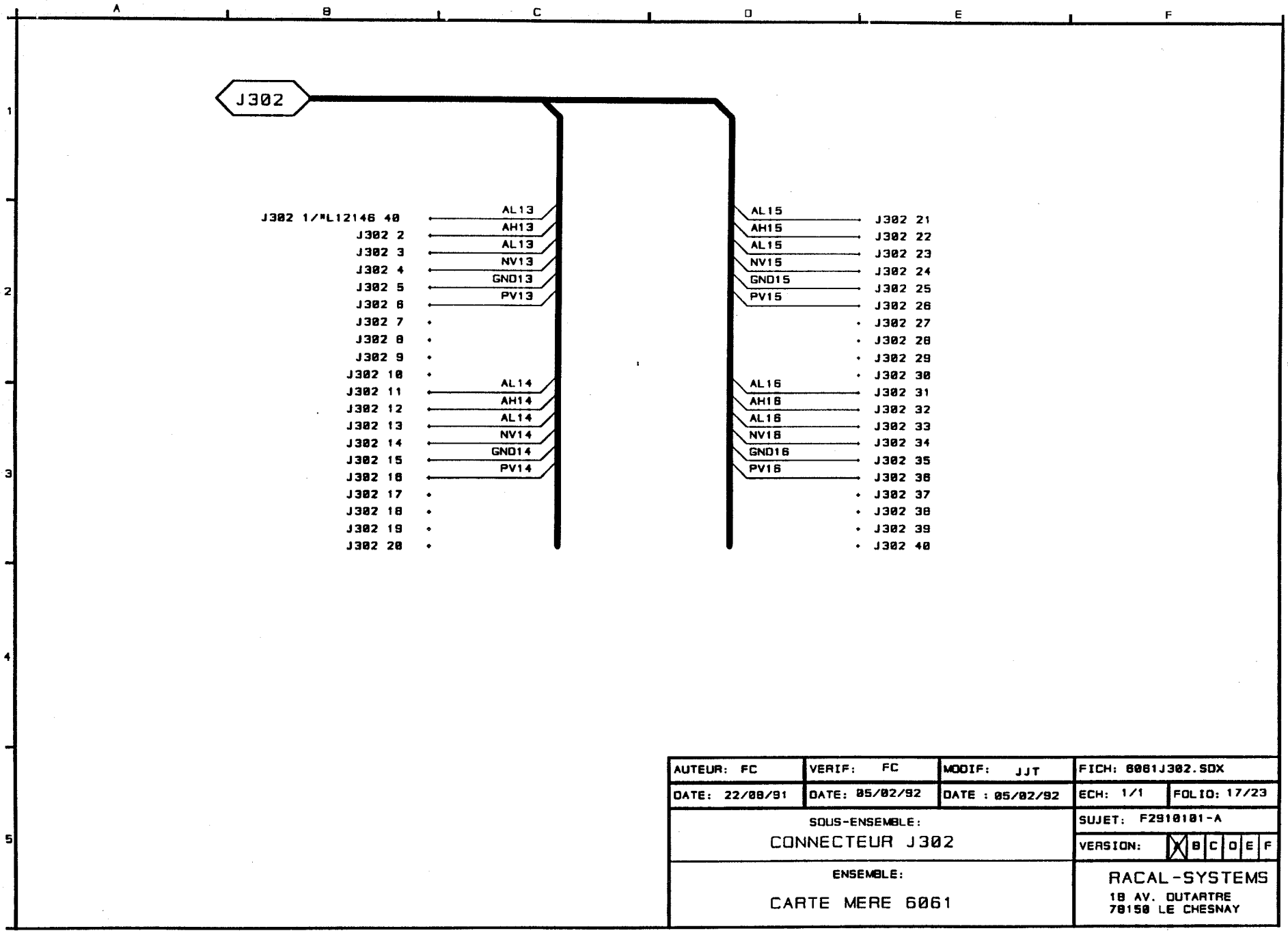
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DATE: 22/08/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 FOLIO: 15/23
SOUS-ENSEMBLE: CONNECTEUR J202			SUJET: F2910101-A
			VERSION: X B C D E F
ENSEMBLE: CARTE MERE 6061			RACAL-SYSTEMS 18 AV. OUTARTRE 78150 LE CHESNAY

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AUTEUR: FC	VERIF: FC	MODIF: JJT	FICH: 6061J301.SDX
DATE: 22/08/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 FOLIO: 16/23
SOUS-ENSEMBLE: CONNECTEUR J301			SUJET: F2910101-A
			VERSION: X B C D E F
ENSEMBLE: CARTE MERE 6061			RACAL-SYSTEMS 18 AV. DUTARTRE 78150 LE CHESNAY

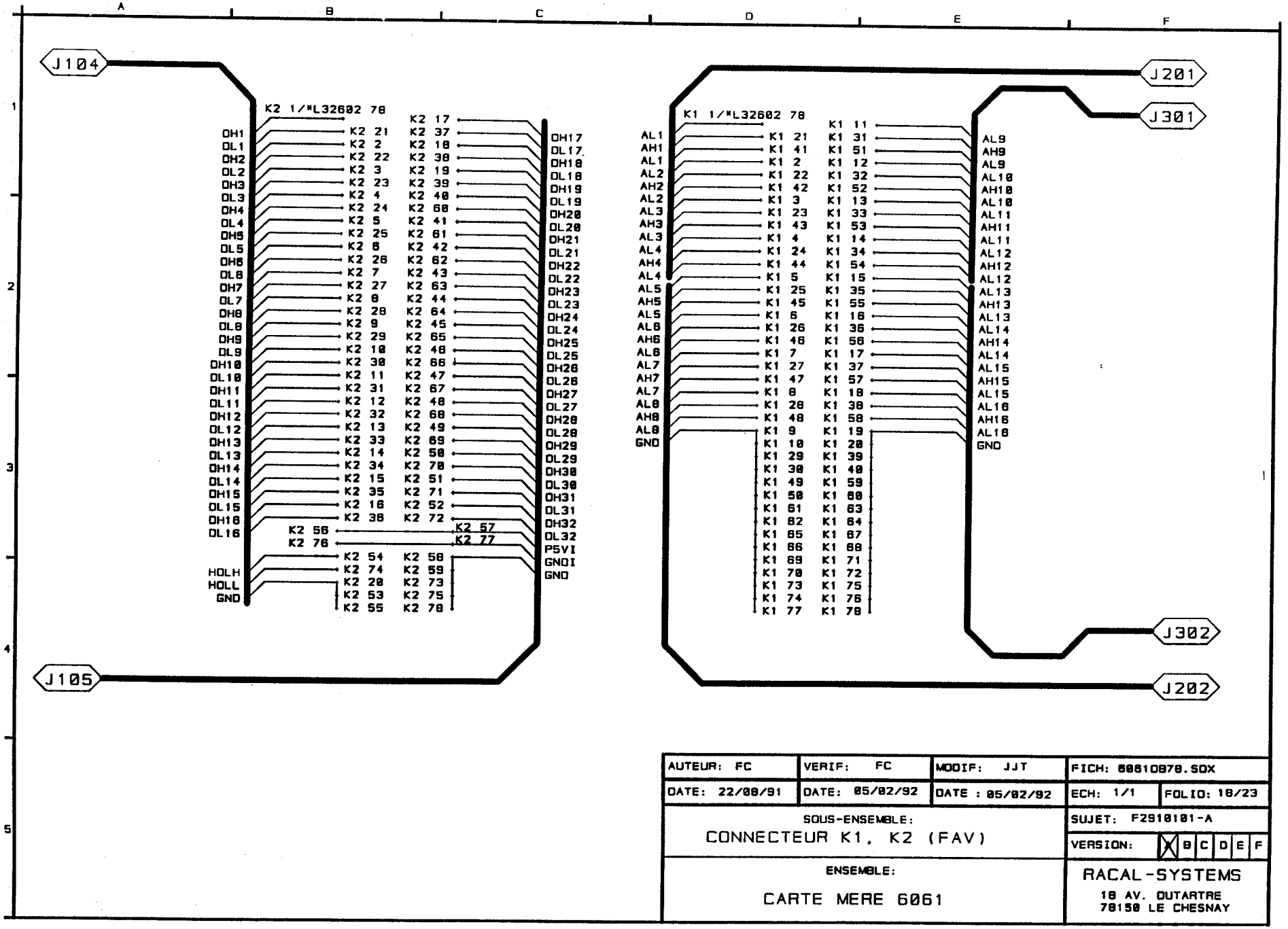
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AUTEUR: FC	VERIF: FC	MODIF: JJT	FICH: 6061J302.SDX
DATE: 22/08/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 FOLIO: 17/23
SOUS-ENSEMBLE: CONNECTEUR J302			SUJET: F2910101-A
			VERSION: X B C D E F
ENSEMBLE: CARTE MERE 6061			RACAL-SYSTEMS 18 AV. DUTARTRE 78150 LE CHESNAY

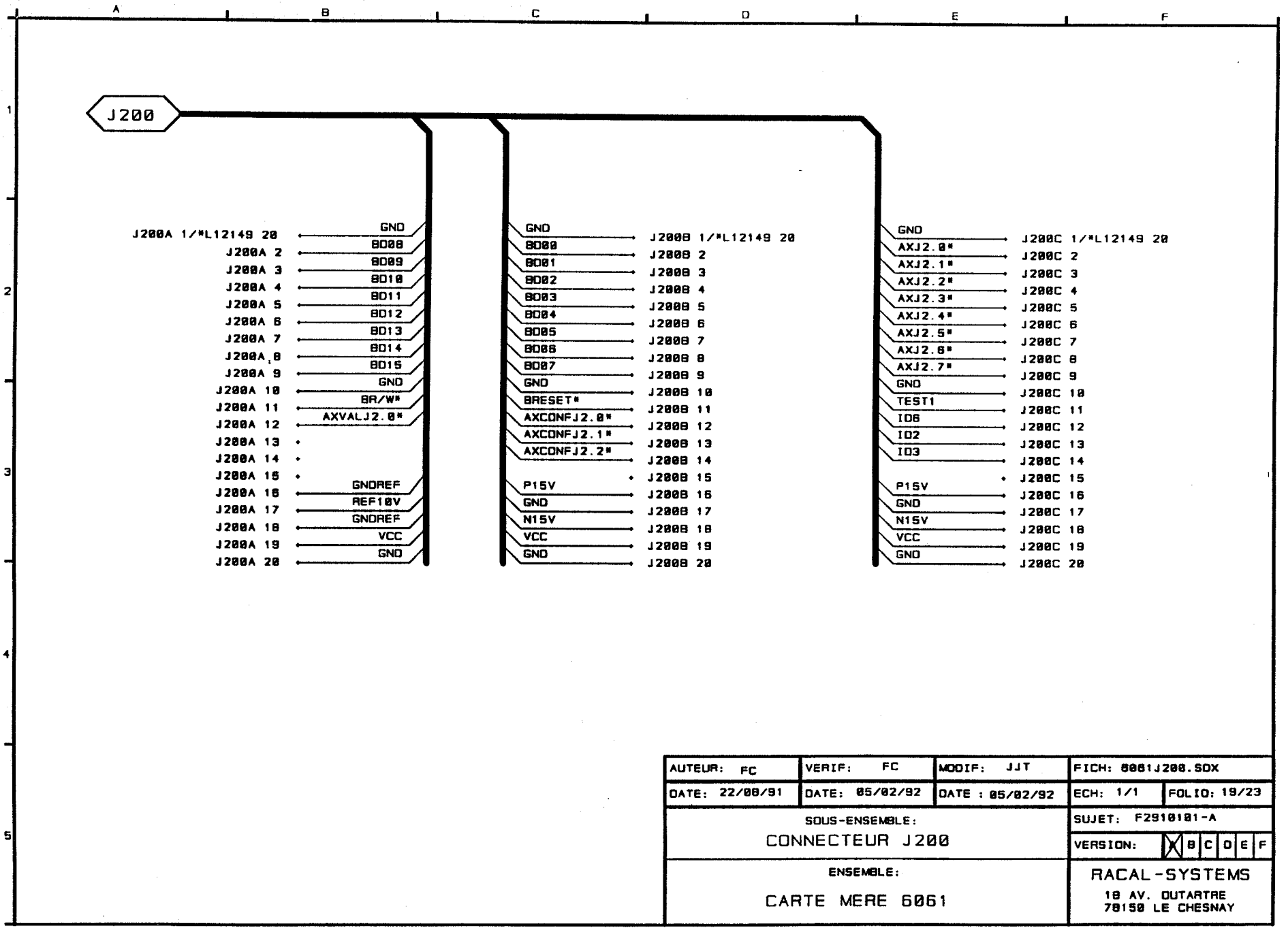
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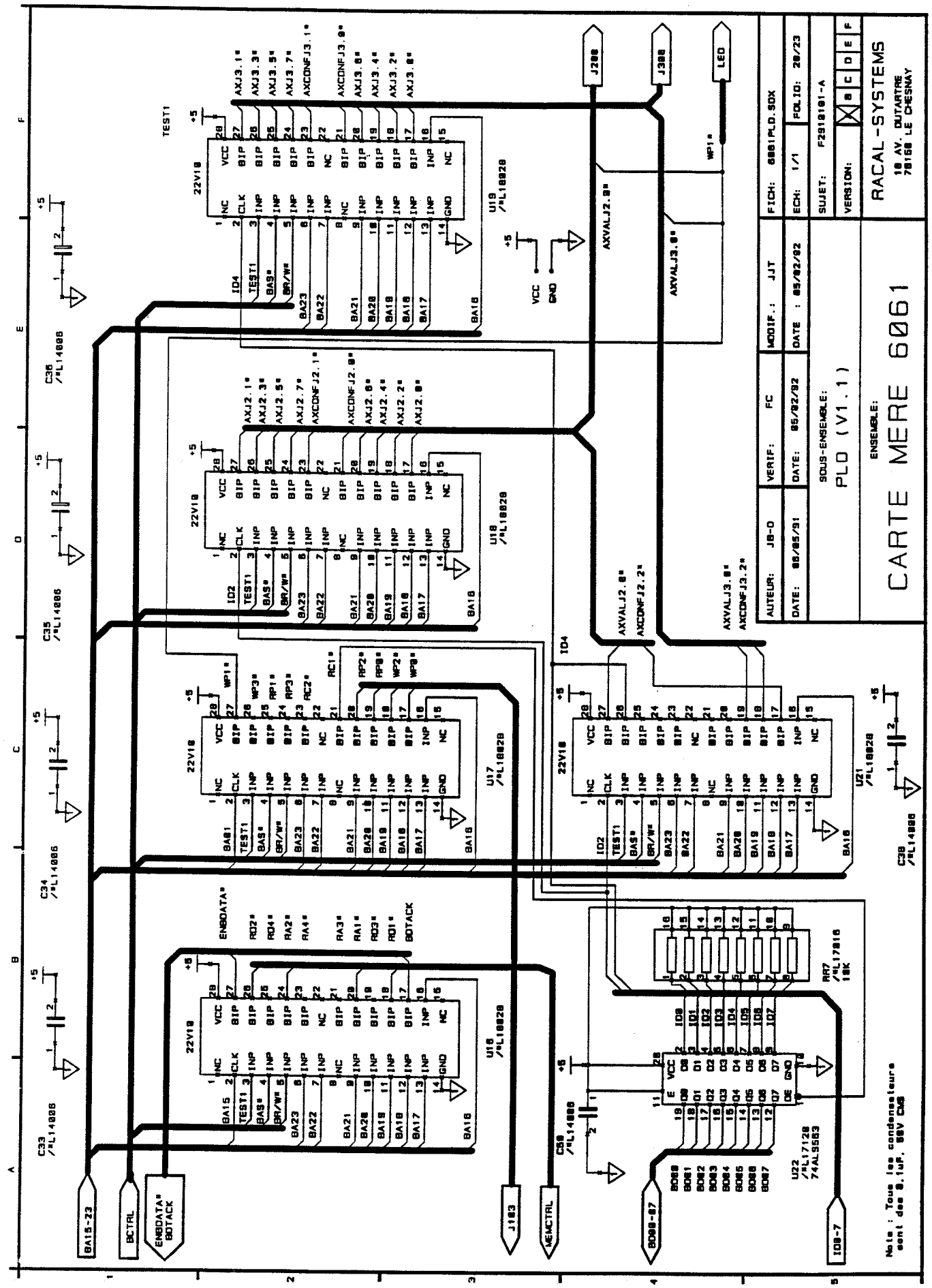
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DATE: 22/08/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 FOLIO: 18/23
SOUS-ENSEMBLE: CONNECTEUR K1, K2 (FAV)			SUJET: F2910101-A
			VERSION: X B C D E F
ENSEMBLE: CARTE MERE 6061			RACAL-SYSTEMS 18 AV. OUTARTRE 78150 LE CHESNAY

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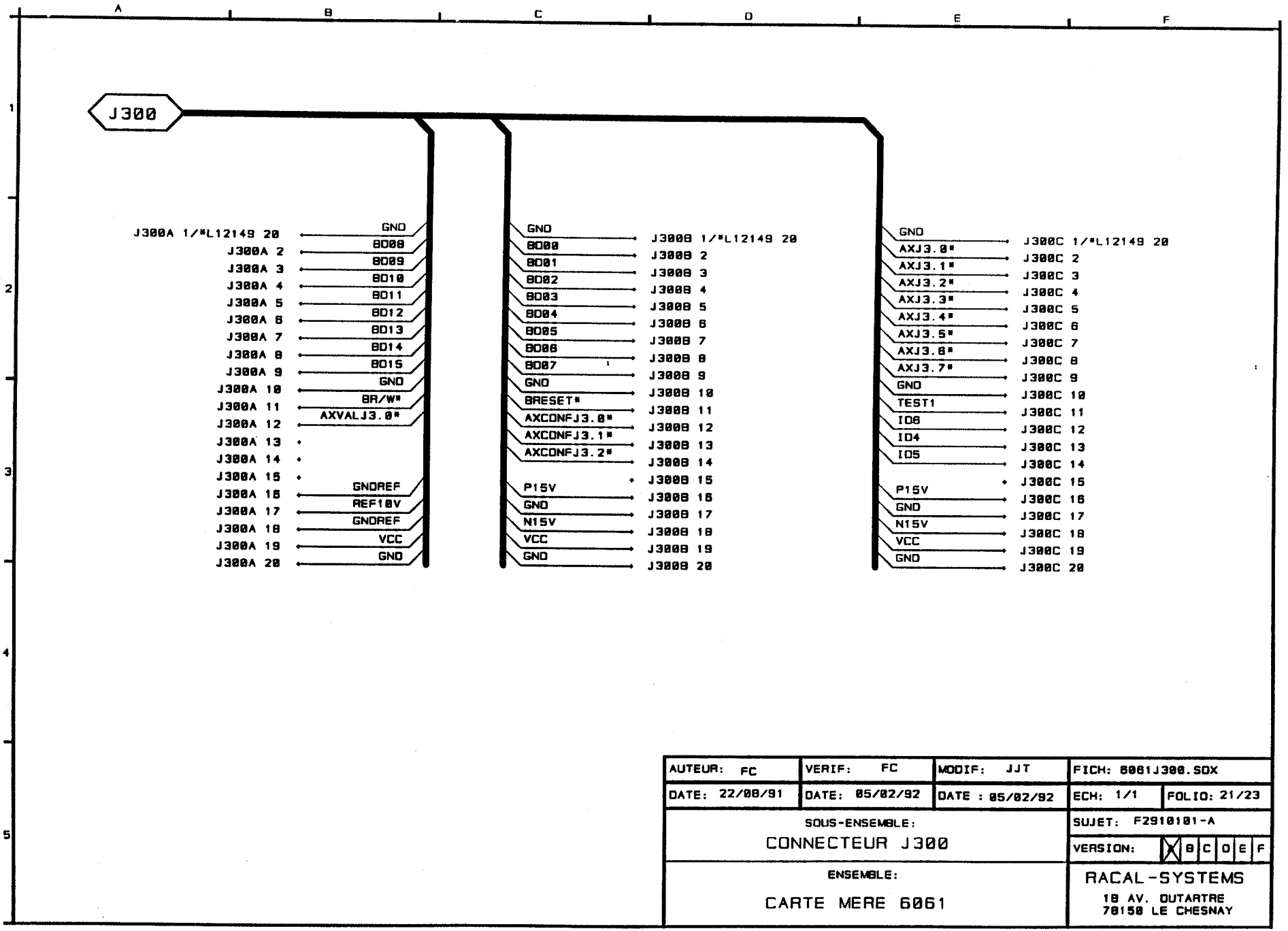


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DATE: 22/08/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 FOLIO: 19/23
SOUS-ENSEMBLE: CONNECTEUR J200			SUJET: F2910101-A
			VERSION: X B C D E F
ENSEMBLE: CARTE MERE 6061			RACAL-SYSTEMS 18 AV. OUTARTRE 78150 LE CHESNAY

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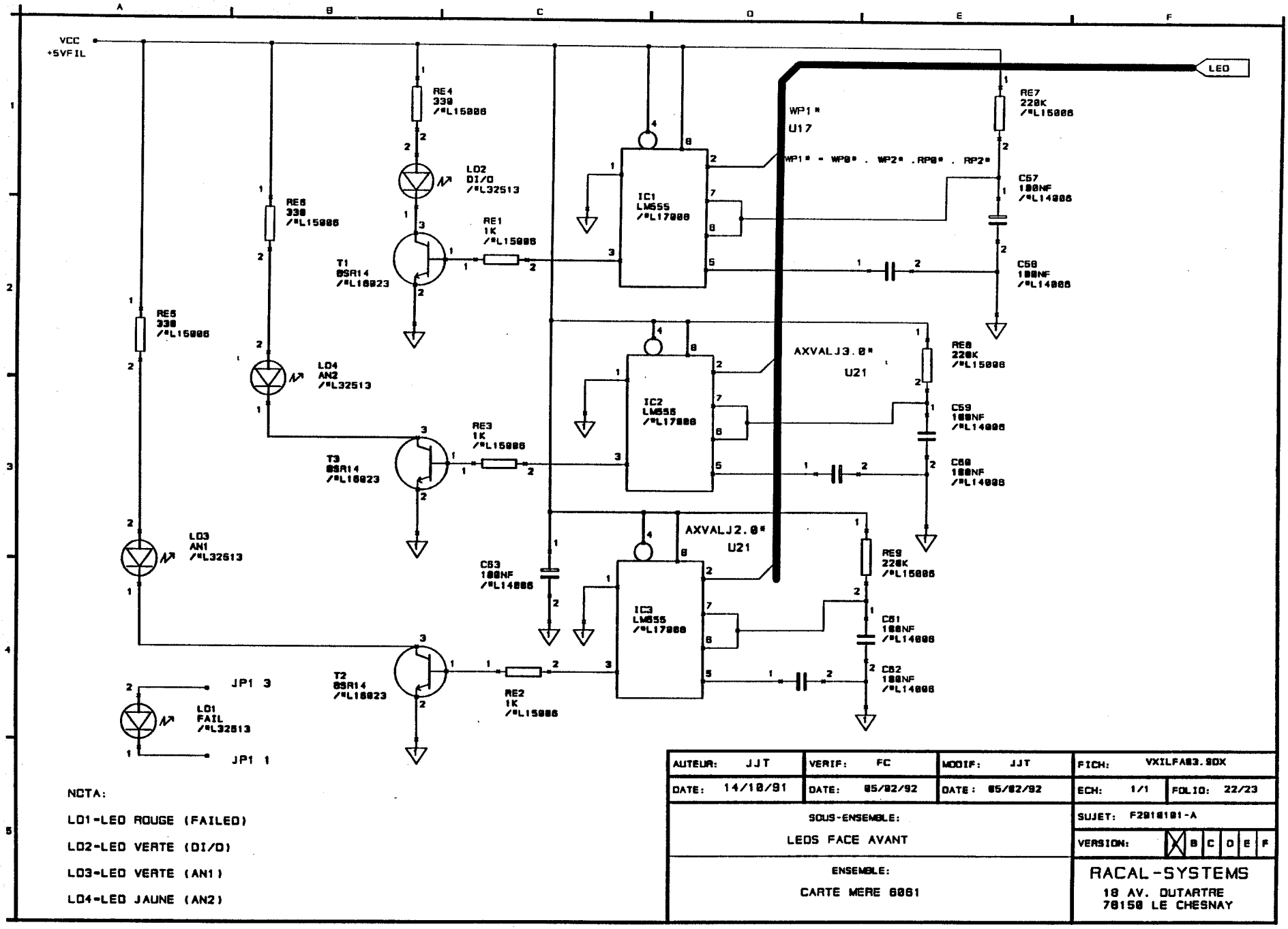


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AUTEUR: FC	VERIF: FC	MODIF: JJT	FICH: 6061J300.SOX
DATE: 22/08/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 FOLIO: 21/23
SOUS-ENSEMBLE: CONNECTEUR J300			SUJET: F2910101-A
			VERSION: X B C D E F
ENSEMBLE: CARTE MERE 6061			RACAL-SYSTEMS 18 AV. OUTARTRE 78150 LE CHESNAY

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NOTA:

LD1=LED ROUGE (FAILED)

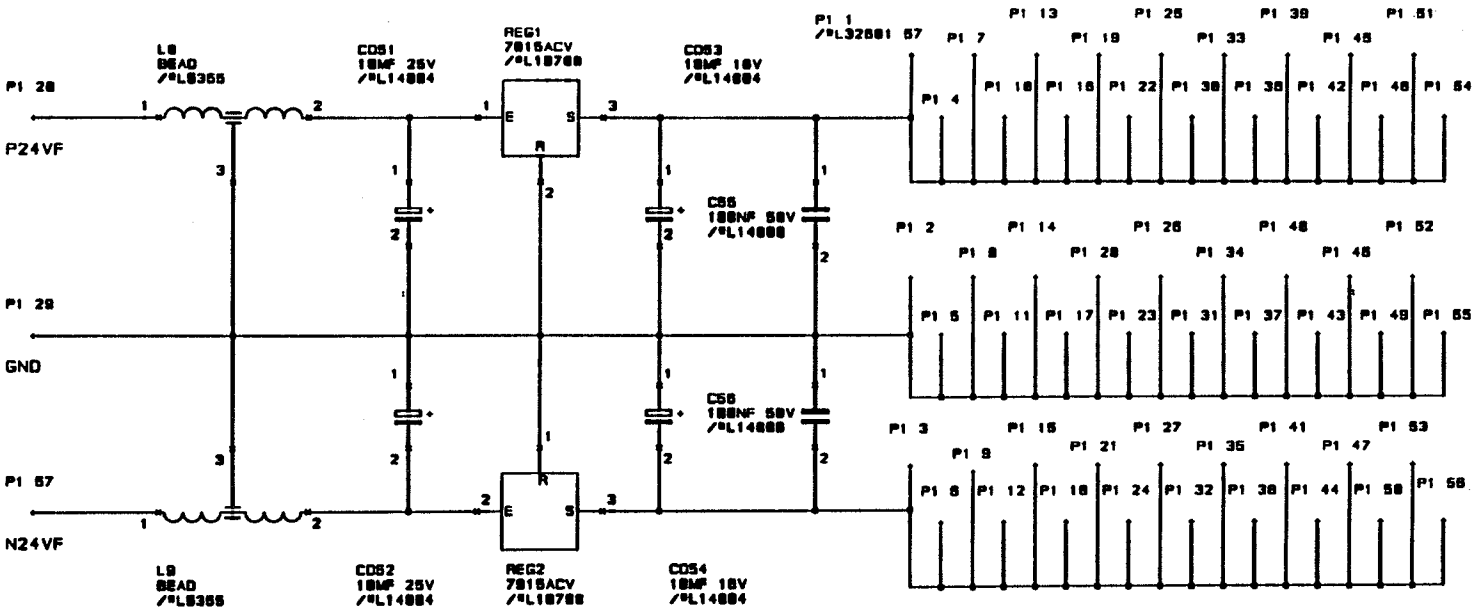
LD2=LED VERTE (DI/D)

LD3=LED VERTE (AN1)

LD4=LED JAUNE (AN2)

AUTEUR: JJT	VERIF: FC	MODIF: JJT	FICH: VXILFA83.SDX
DATE: 14/10/91	DATE: 05/02/92	DATE: 05/02/92	ECH: 1/1 FOLIO: 22/23
SOUS-ENSEMBLE: LEDS FACE AVANT			SUJET: F2918101-A
			VERSION: X B C D E F
ENSEMBLE: CARTE MERE 6061			RACAL-SYSTEMS 18 AV. DUTARTRE 78150 LE CHESNAY

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NOTA:

LES REG 1 ET 2 SONT A MONTER SUR UN RADIATEUR
PROFILE ALUMINIUM WA498

AVEC 1 KIT TO220

AUTEUR: JJT	VERIF: FC	MODIF: JJT	FICH: VXICONVS.SCH		
DATE: 11/10/91	DATE: 05/02/92	DATE: 05/02/92	ECH: 1/1	FOLIO: 23/23	
SOUS-ENSEMBLE: CONVERTISSEUR NON ISOLE			SUJET: F2916101-A		
			VERSION:	X A B C D E F	
ENSEMBLE: CARTE MERE 6061			RACAL-SYSTEMS 18 AV. DUTARTRE 78150 LE CHESNAY		

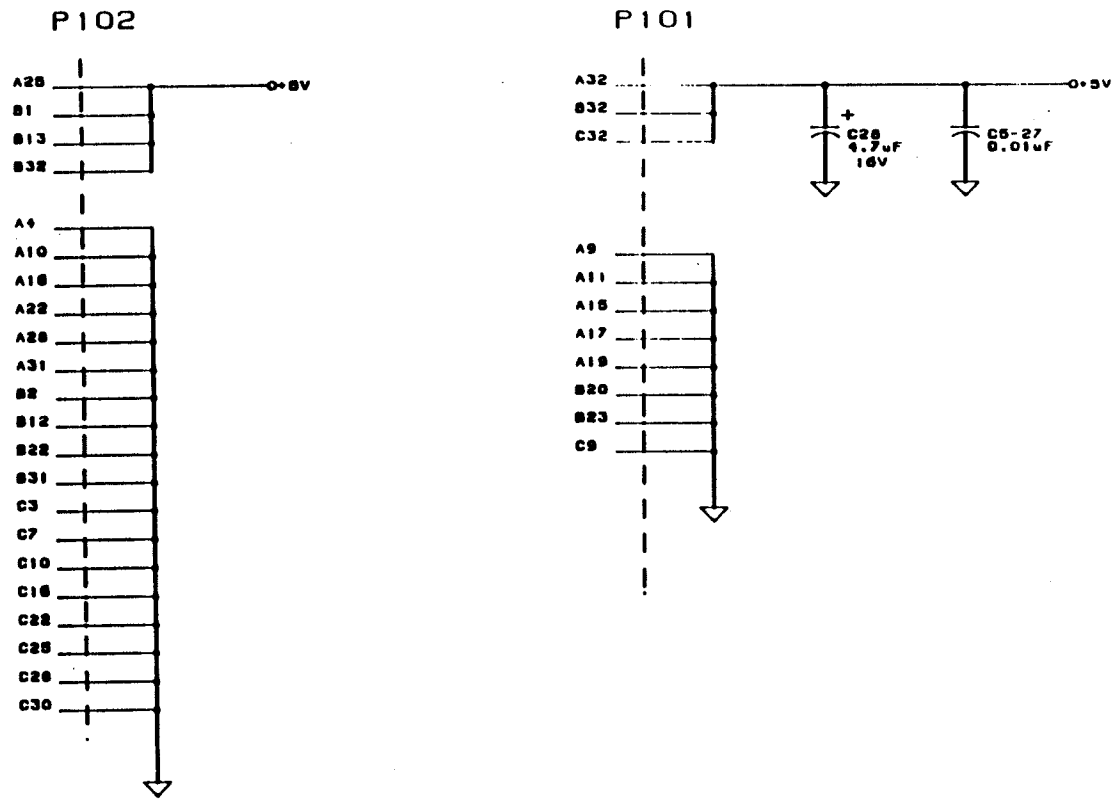
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SECTION 8-2

F2910105

SCHEMATICS of the MICROPROCESSOR and VXI INTERFACE BOARD

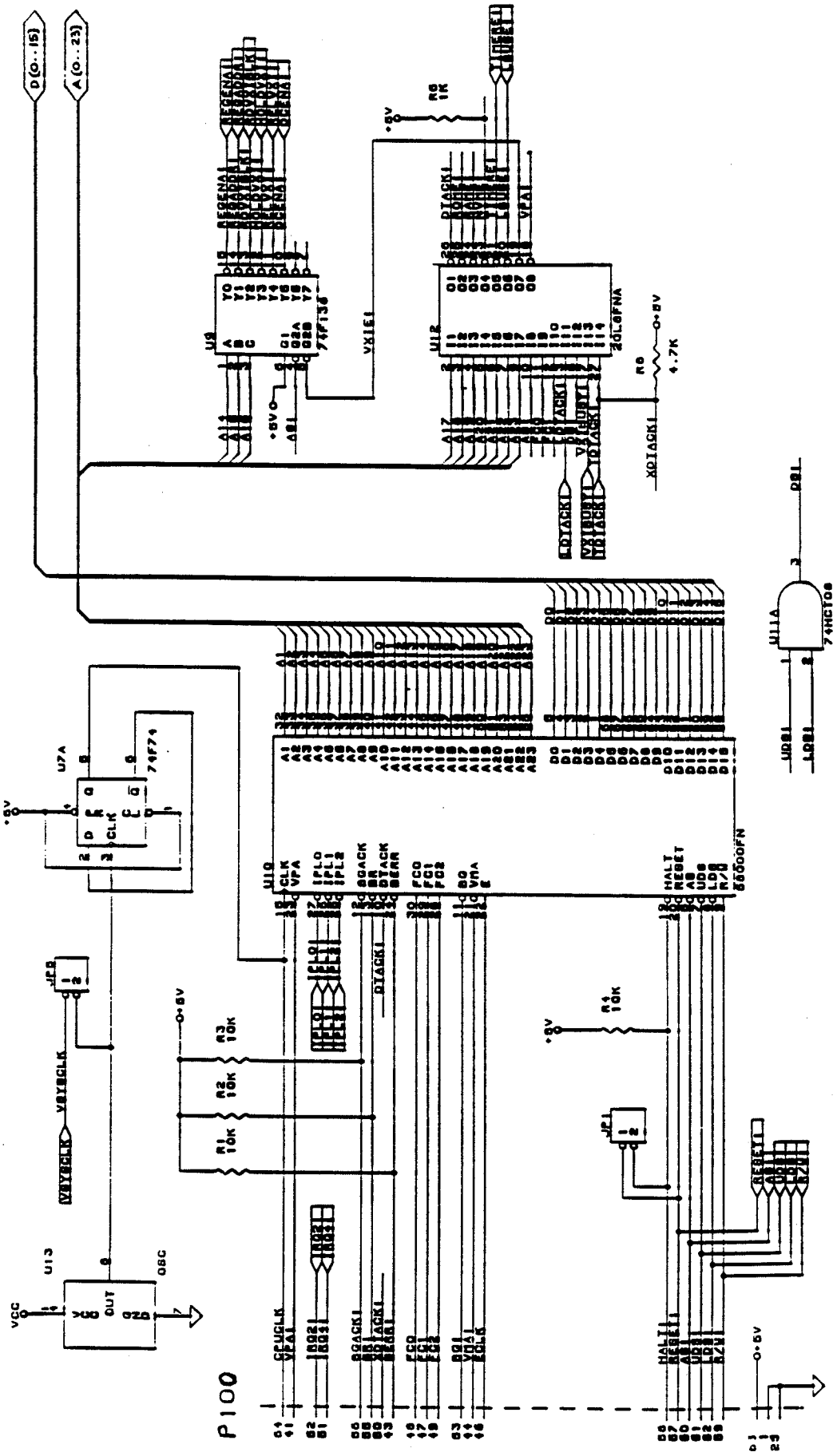
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5. U13 AND JP5 ARE INSTALLED ON 12.5 MHz UNITS ONLY
4. INSTALL JP2 FOR 256K X 16 EPROM
   DELETE JP2 FOR 64K X 16 AND 128K X 16 EPROM
3. INSTALL JP3 AND JP4 FOR 32K X 8 NVM
   DELETE JP3 AND JP4 FOR 8K X 8 NVM
2. ALL CAPACITORS ARE 20% 50V
1. ALL RESISTORS ARE 5% 1/8 WATT

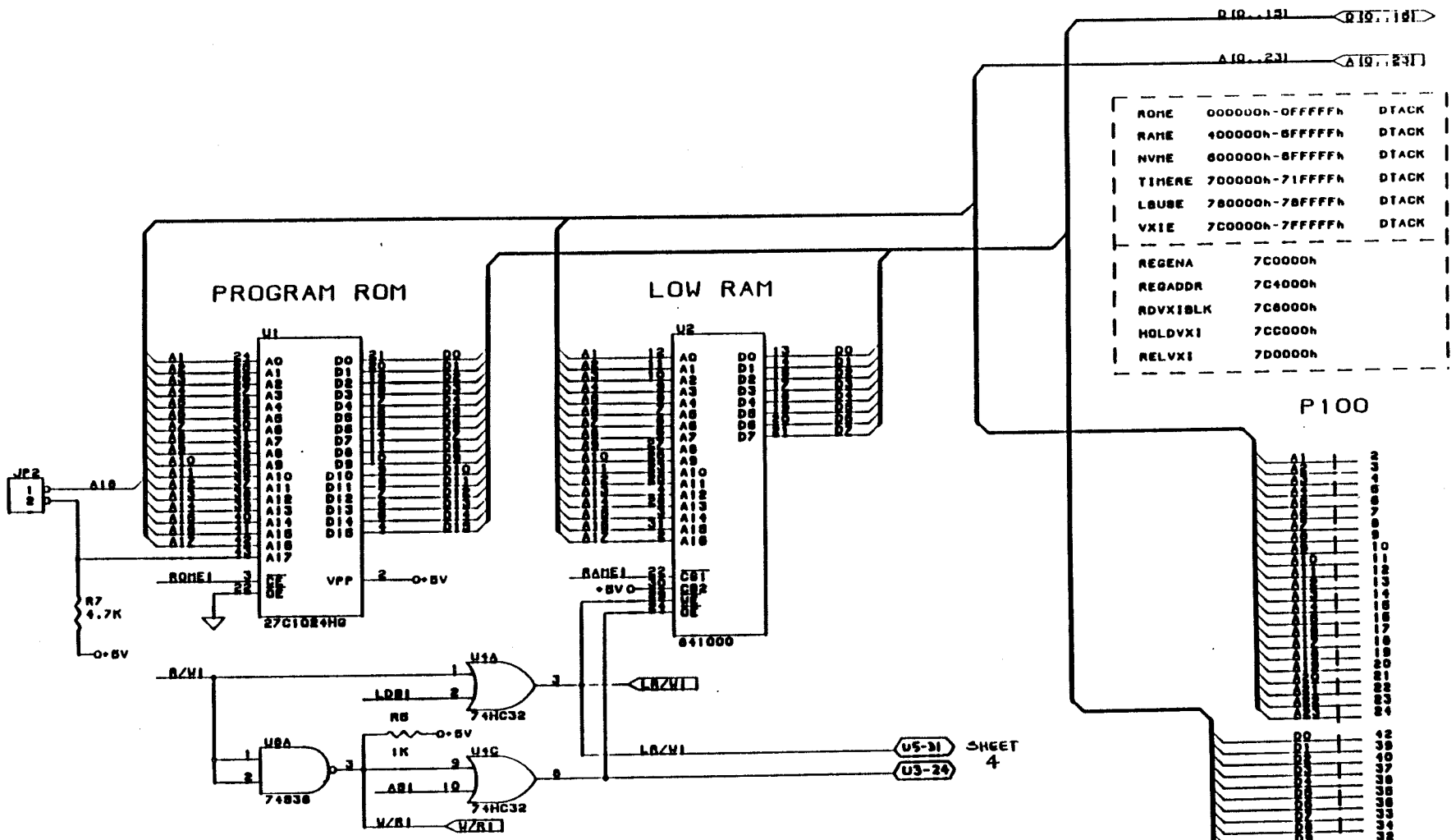
NOTES: UNLESS OTHERWISE SPECIFIED

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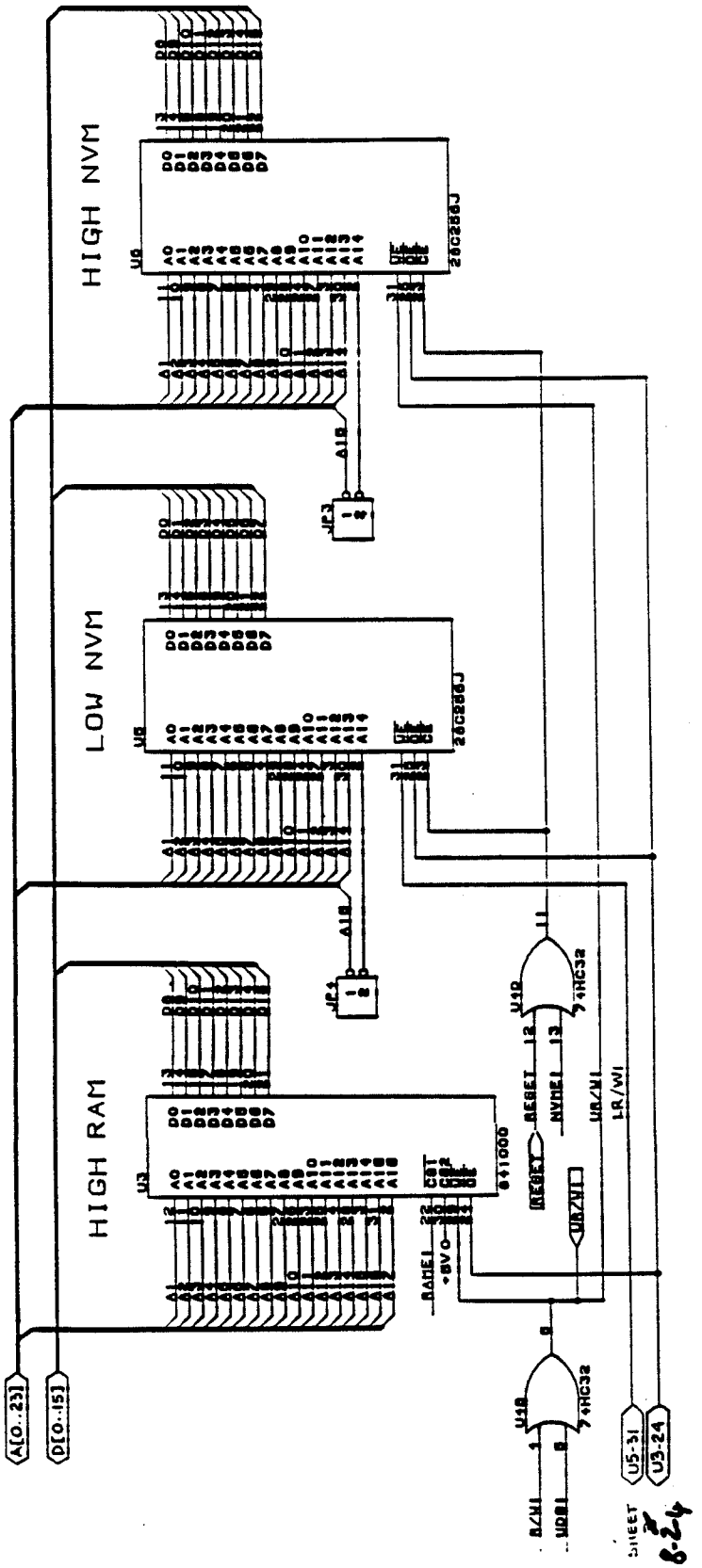


RACAL

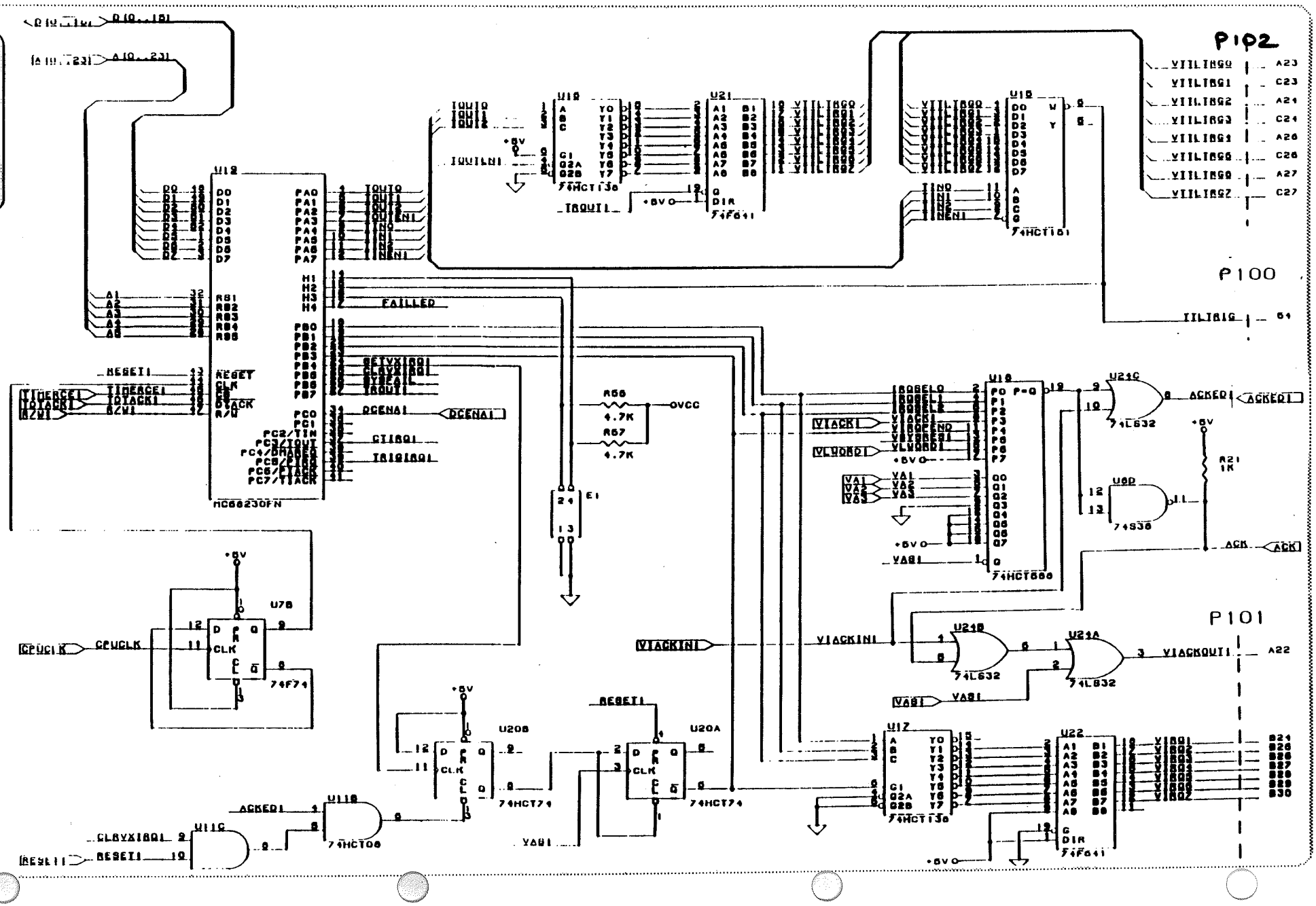
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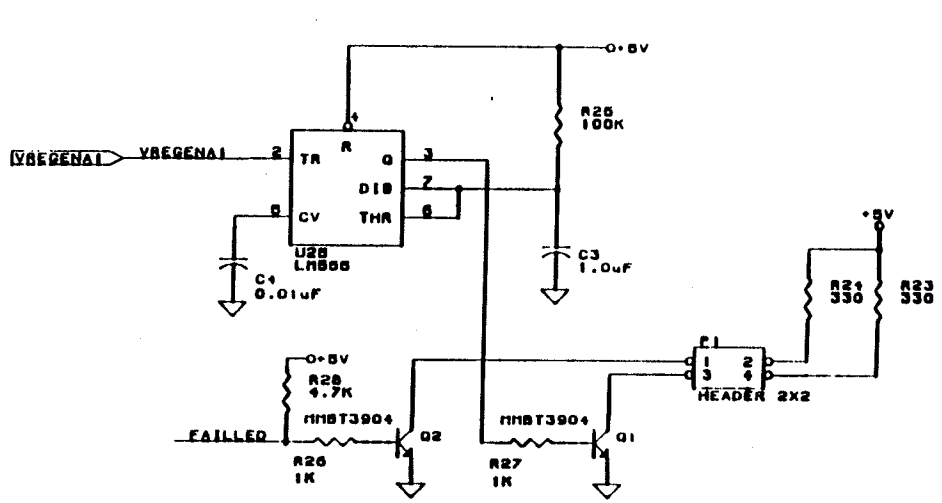
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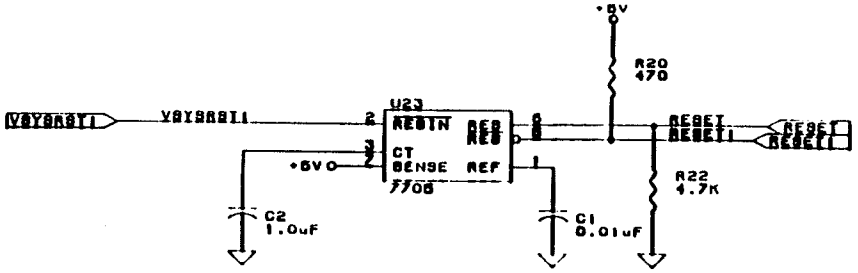


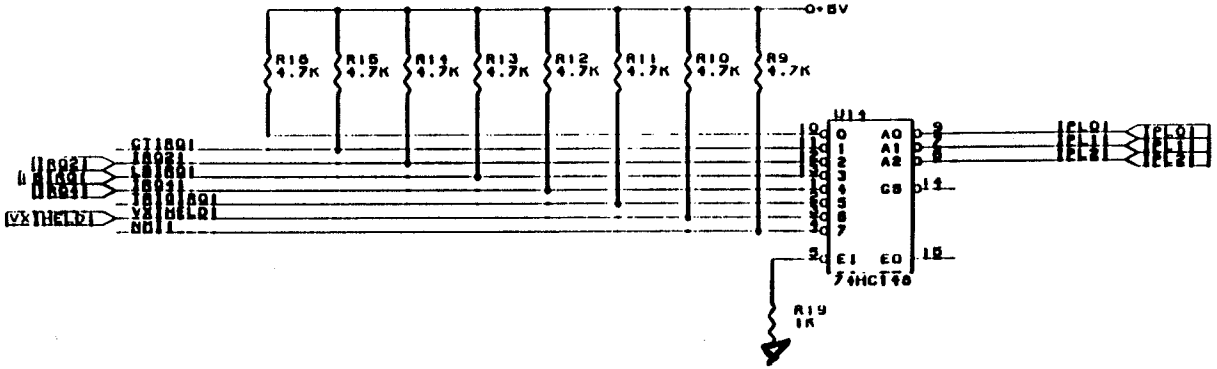
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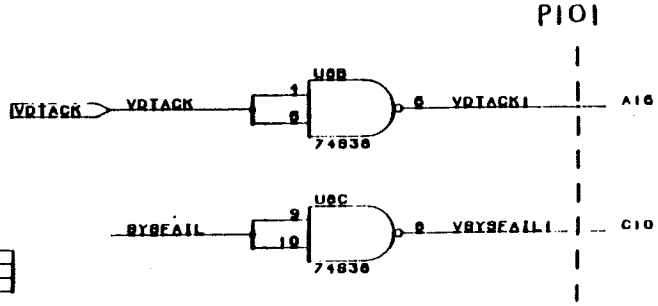


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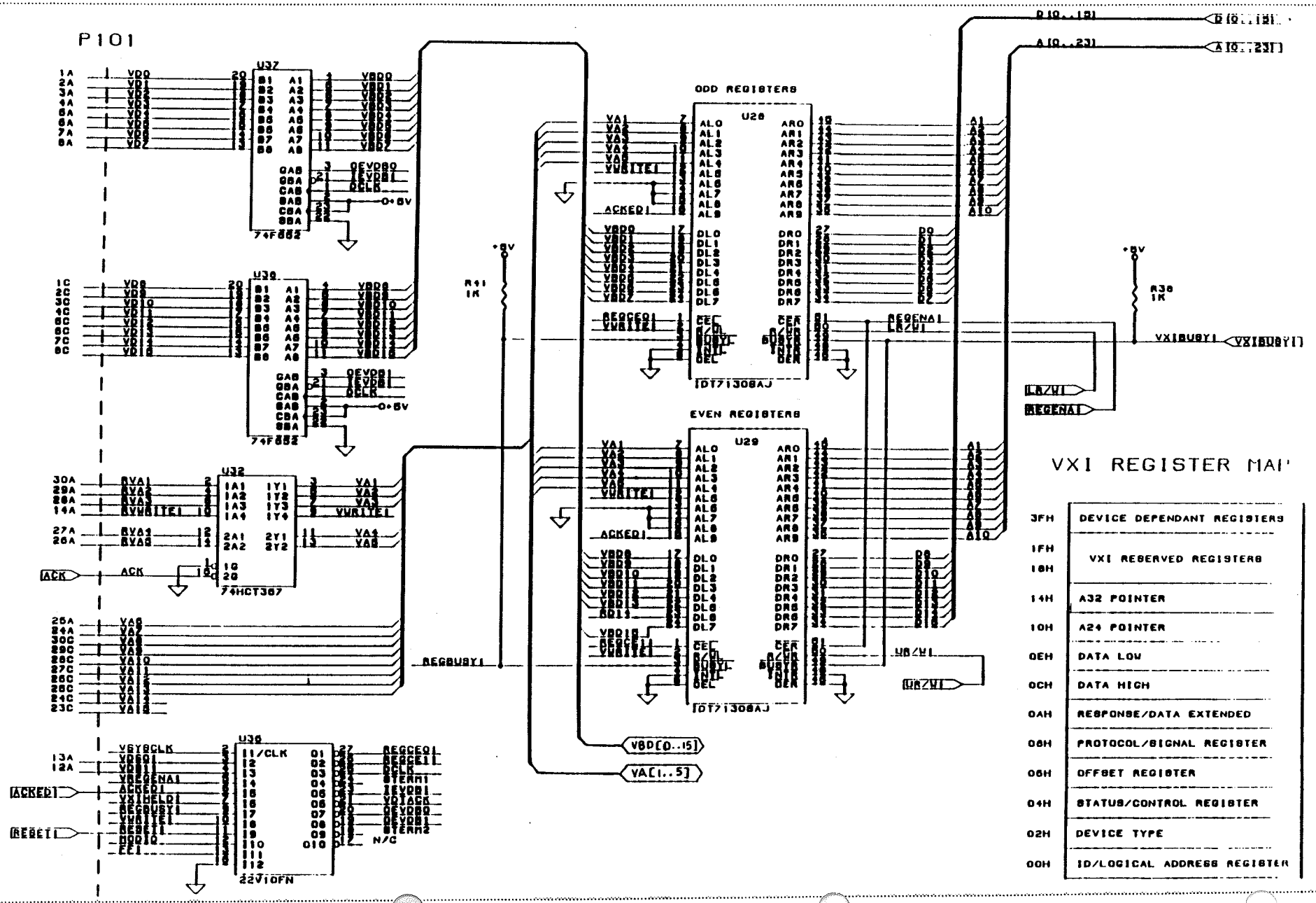




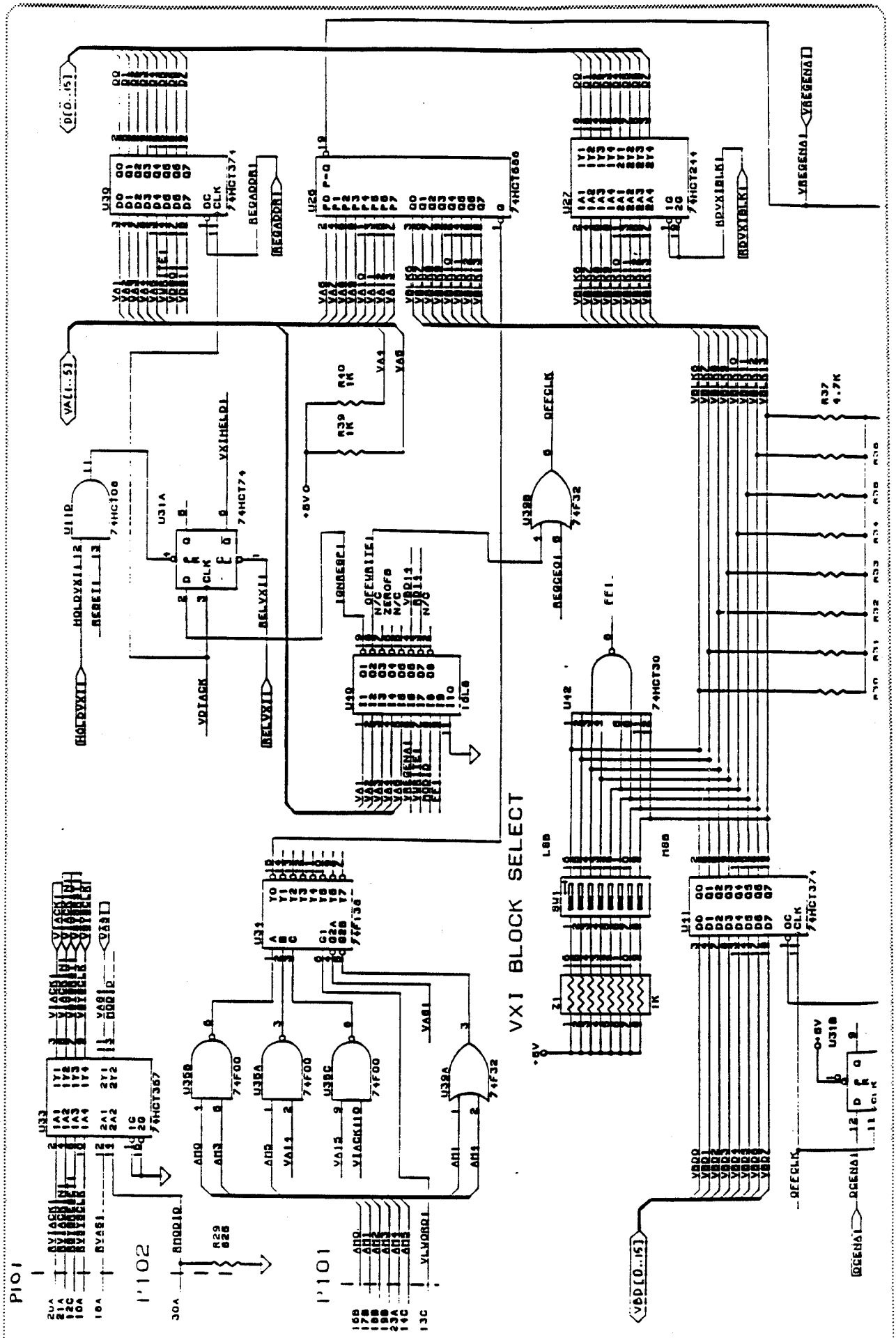


RACAL

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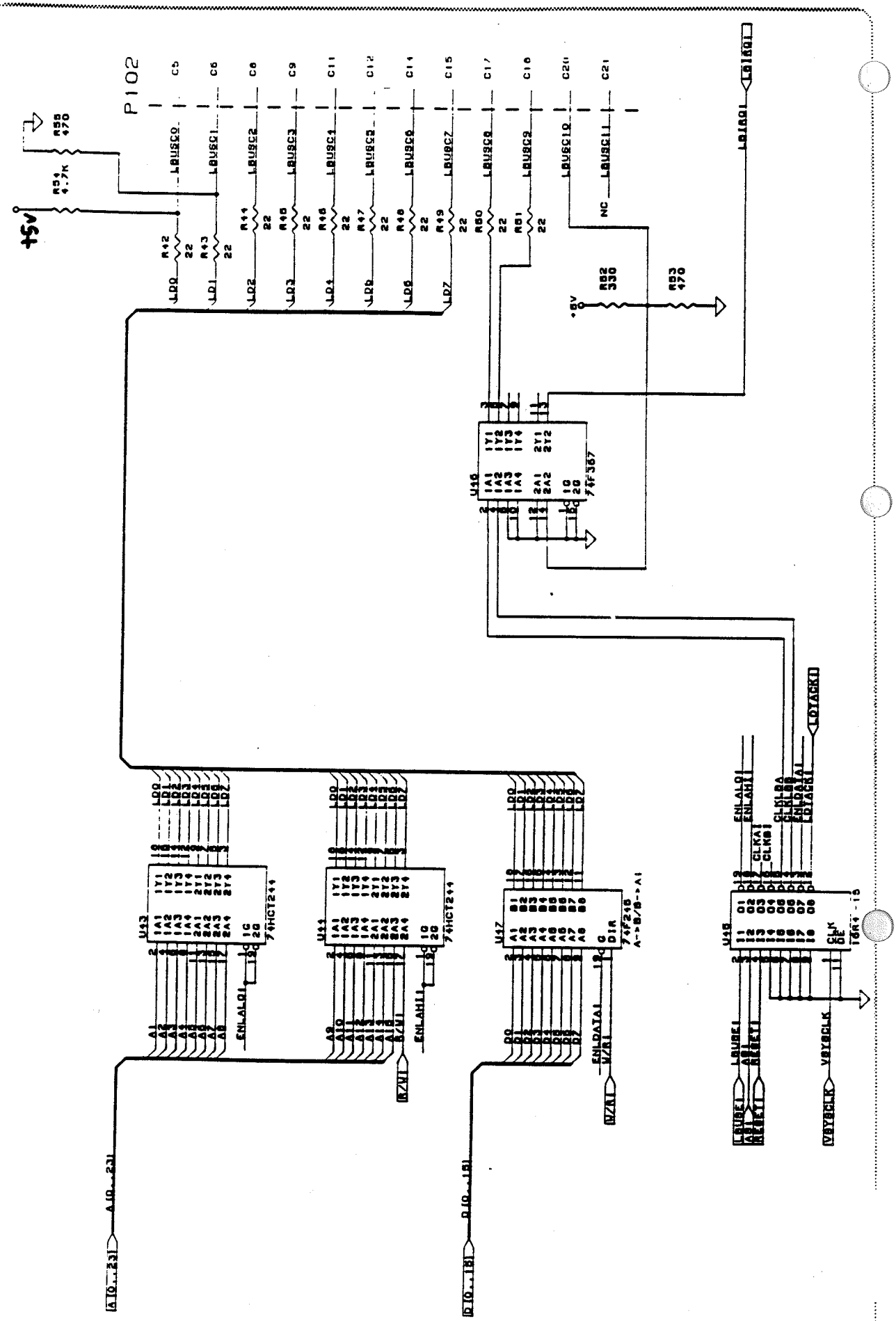


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RACAL

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RACAL

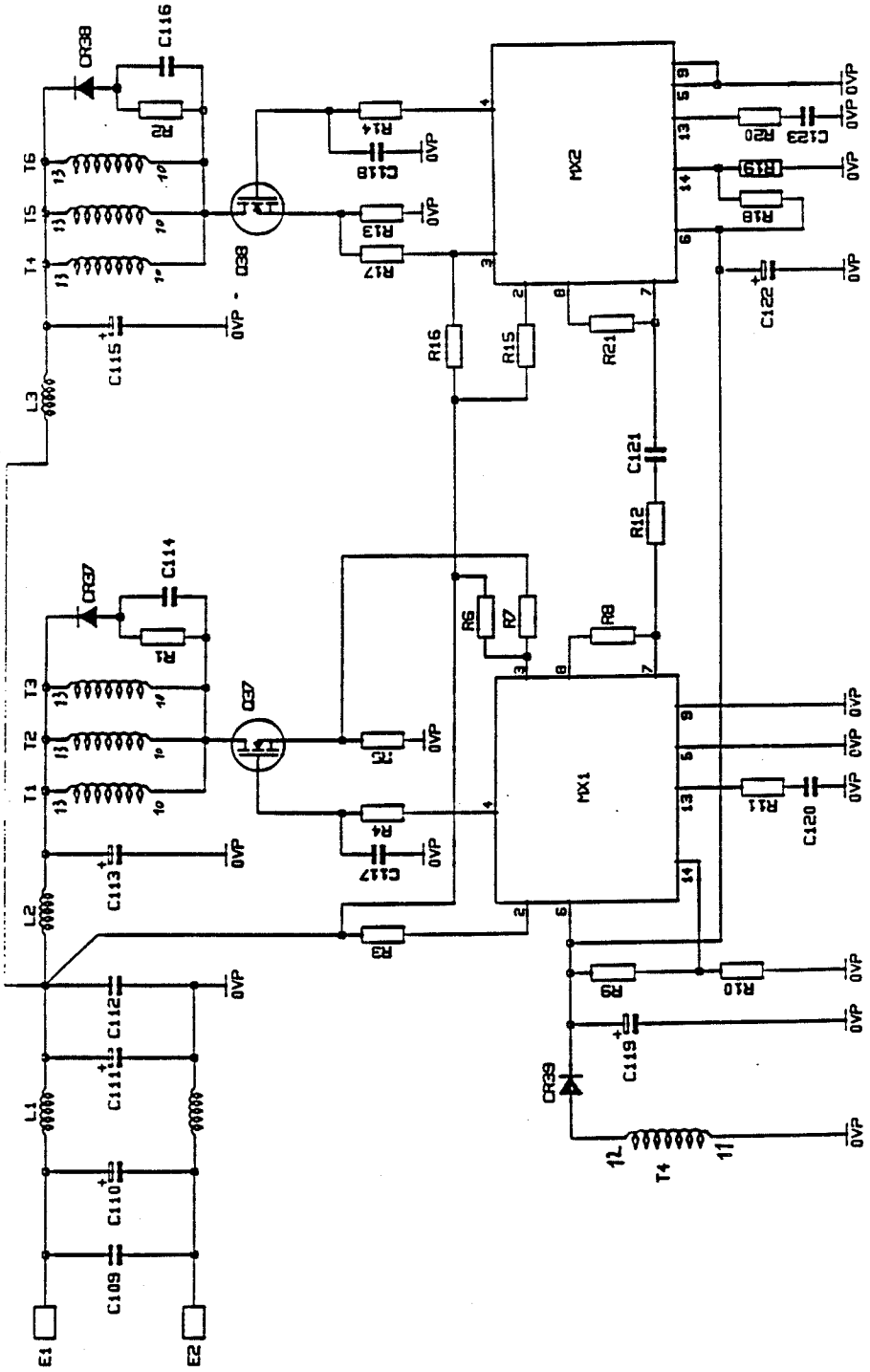
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SECTION 8-3

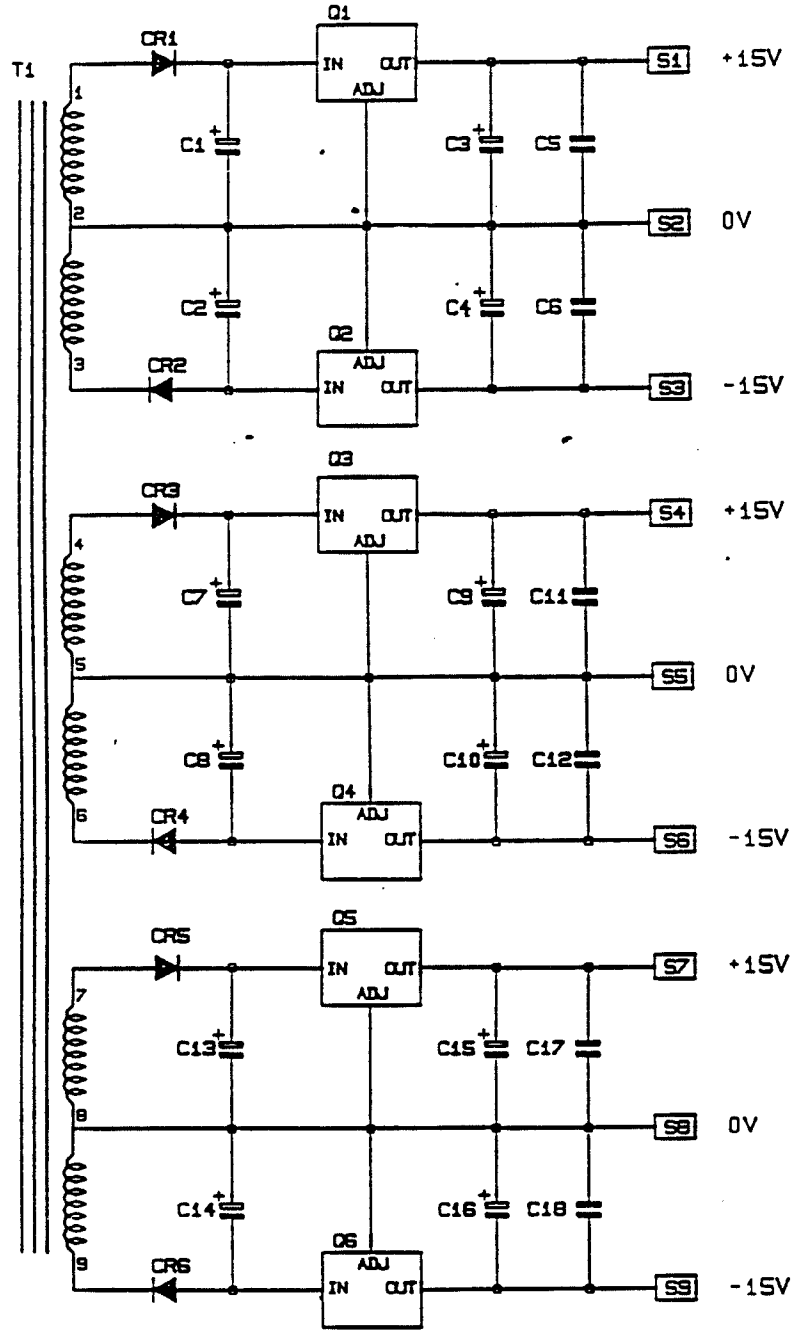
F2910106

SCHEMATICS
of the
DC / DC CONVERTER
BOARD

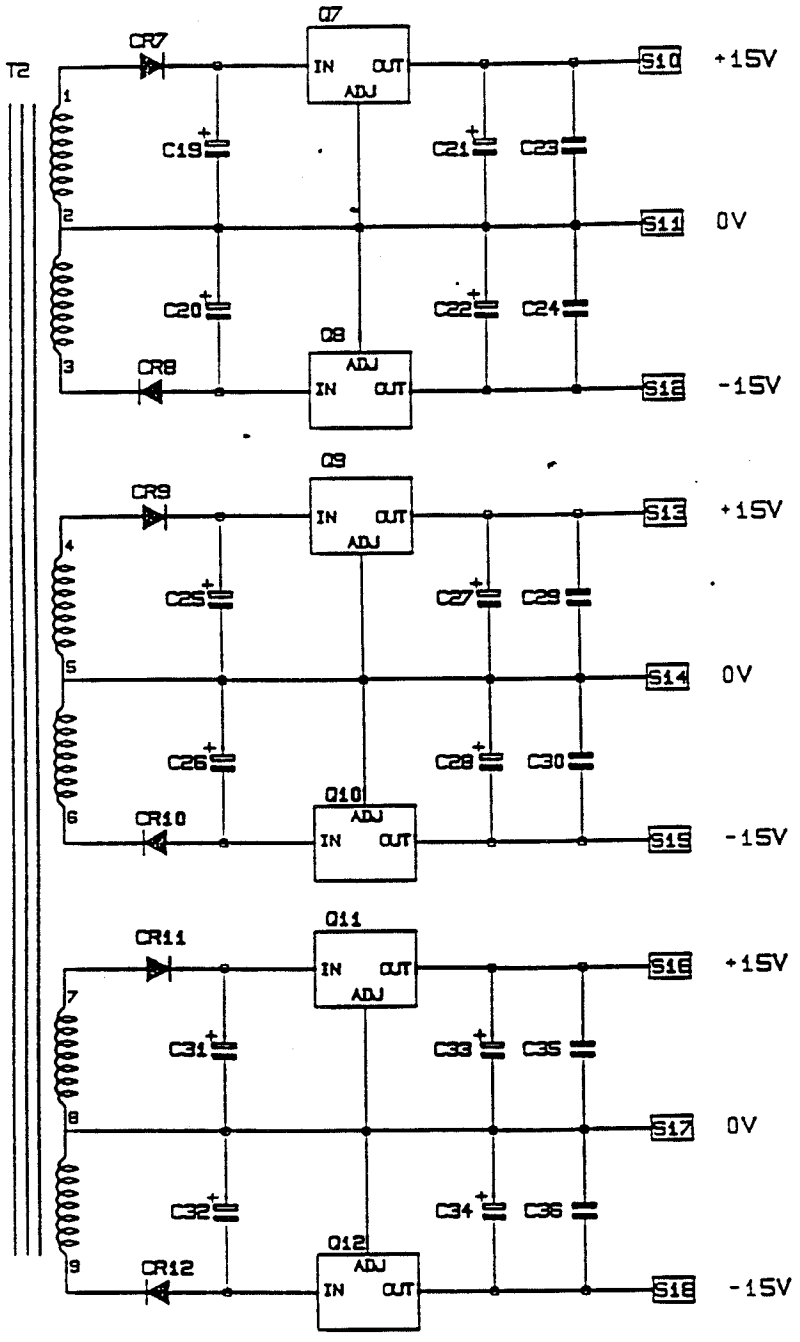
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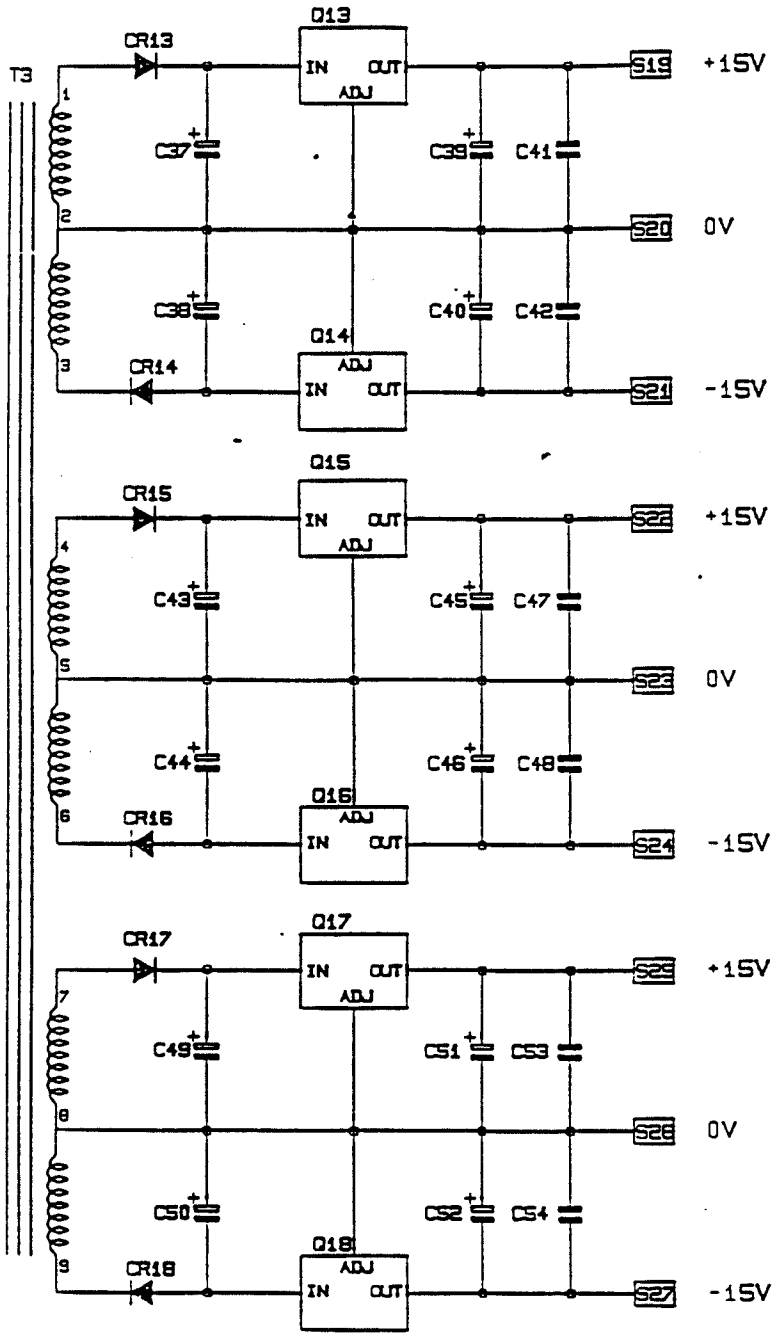
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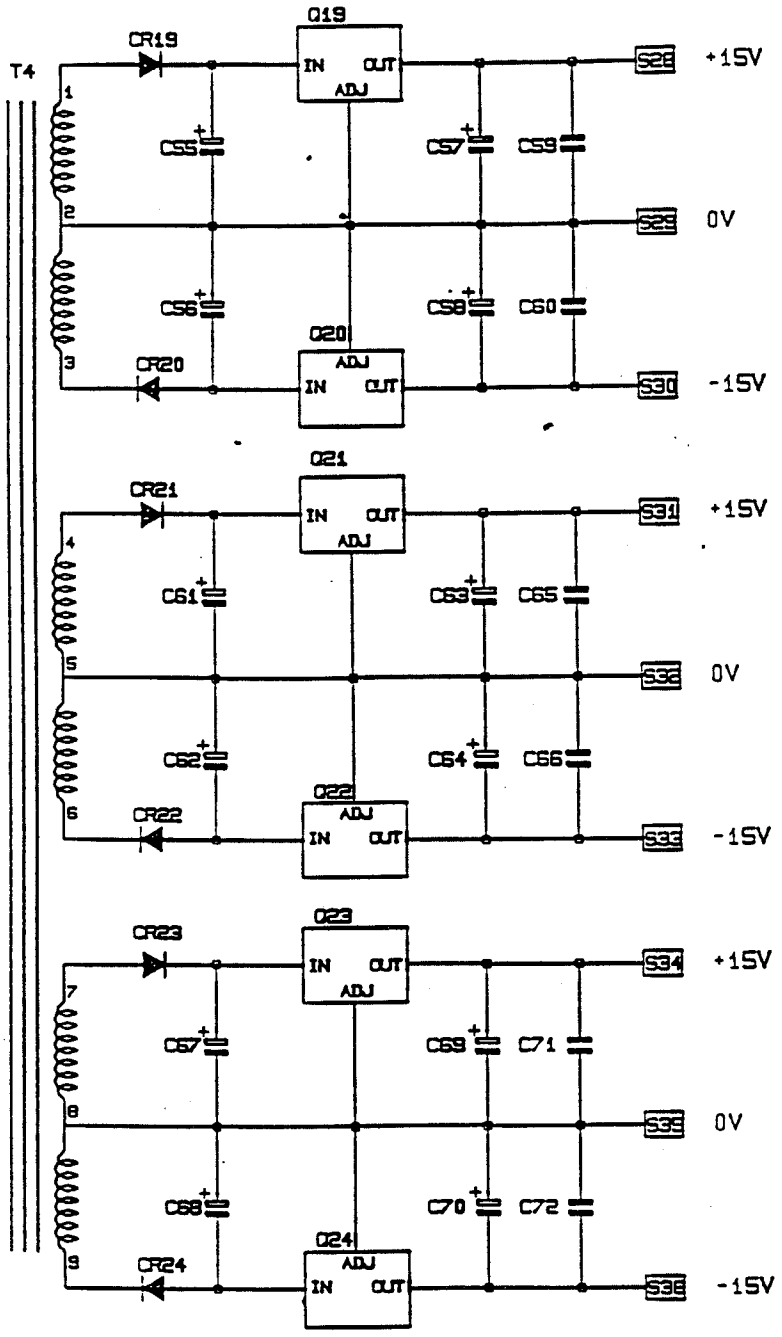
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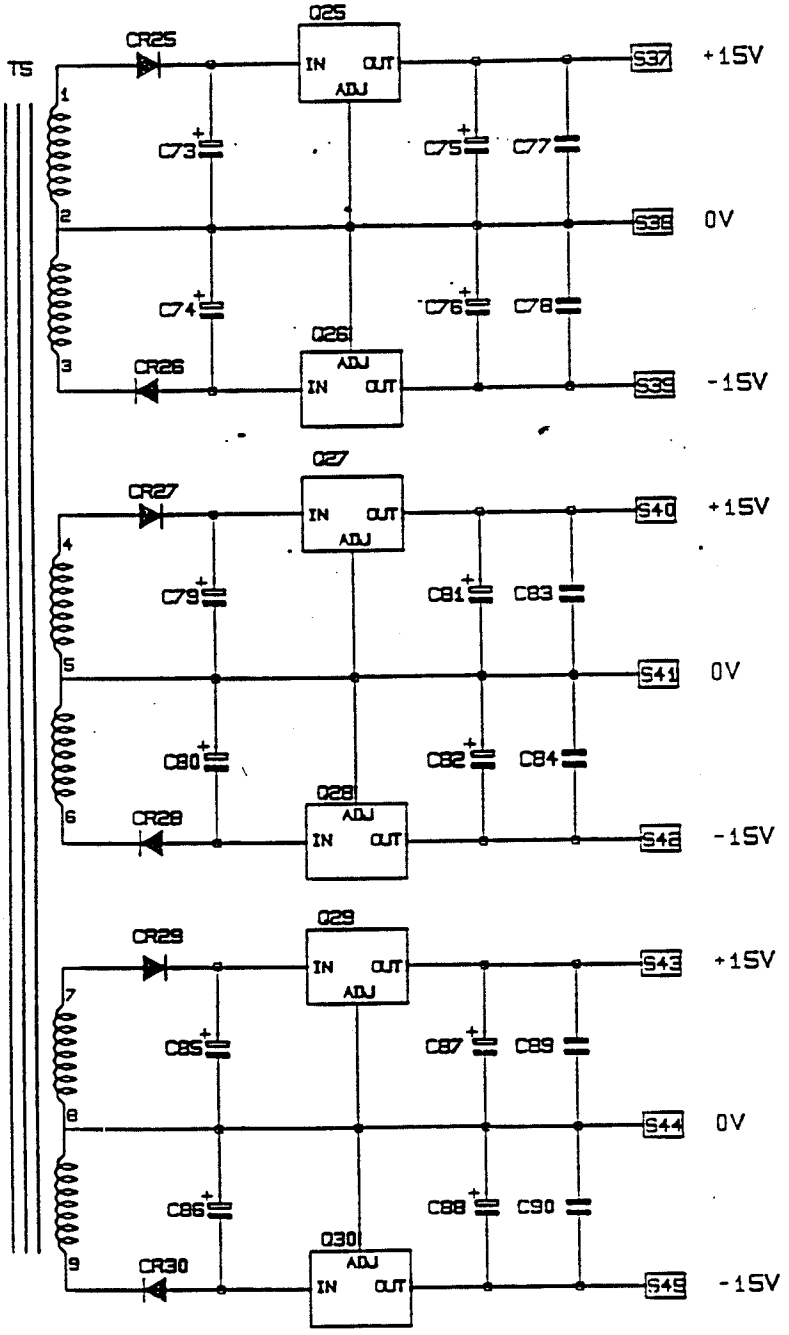
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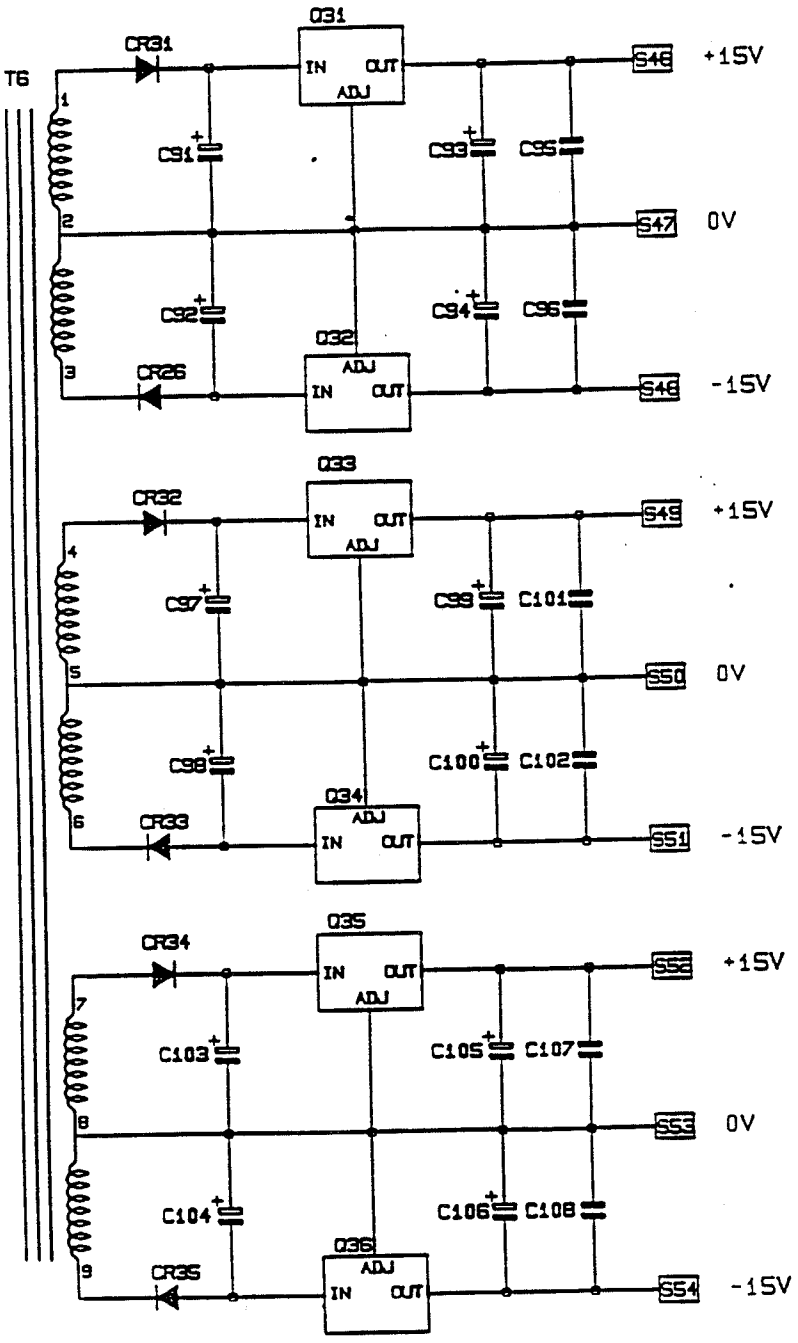


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RACAL

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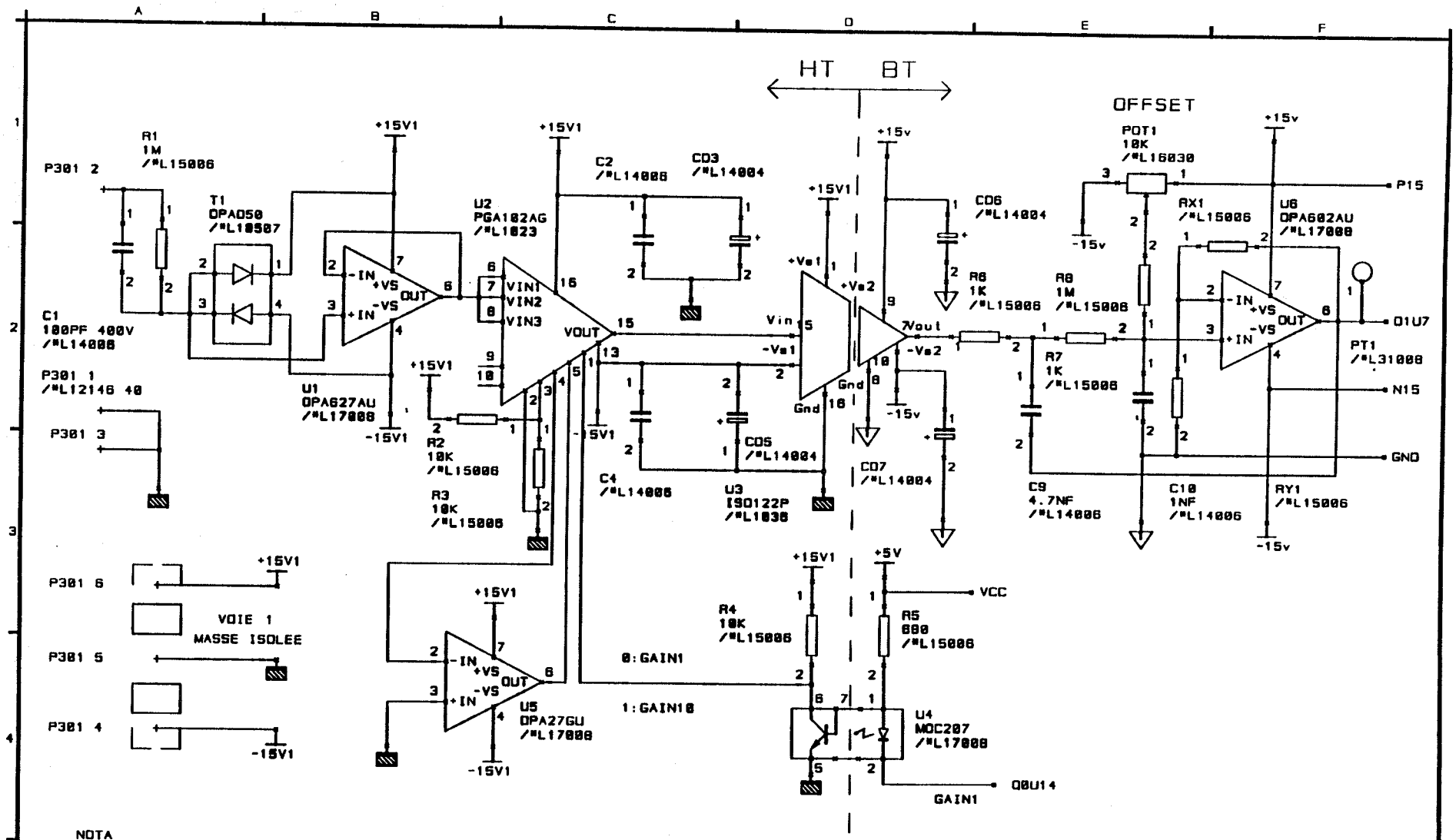
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SECTION 8-4

F2910104

SCHEMATICS
of the
ANALOG INPUTS
BOARD

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NOTA

TOUS LES CONDENSATEURS POLARISES SONT DE 10MF 16V

TOUS LES CONDENSATEURS NON POLARISES SONT DE 100NF

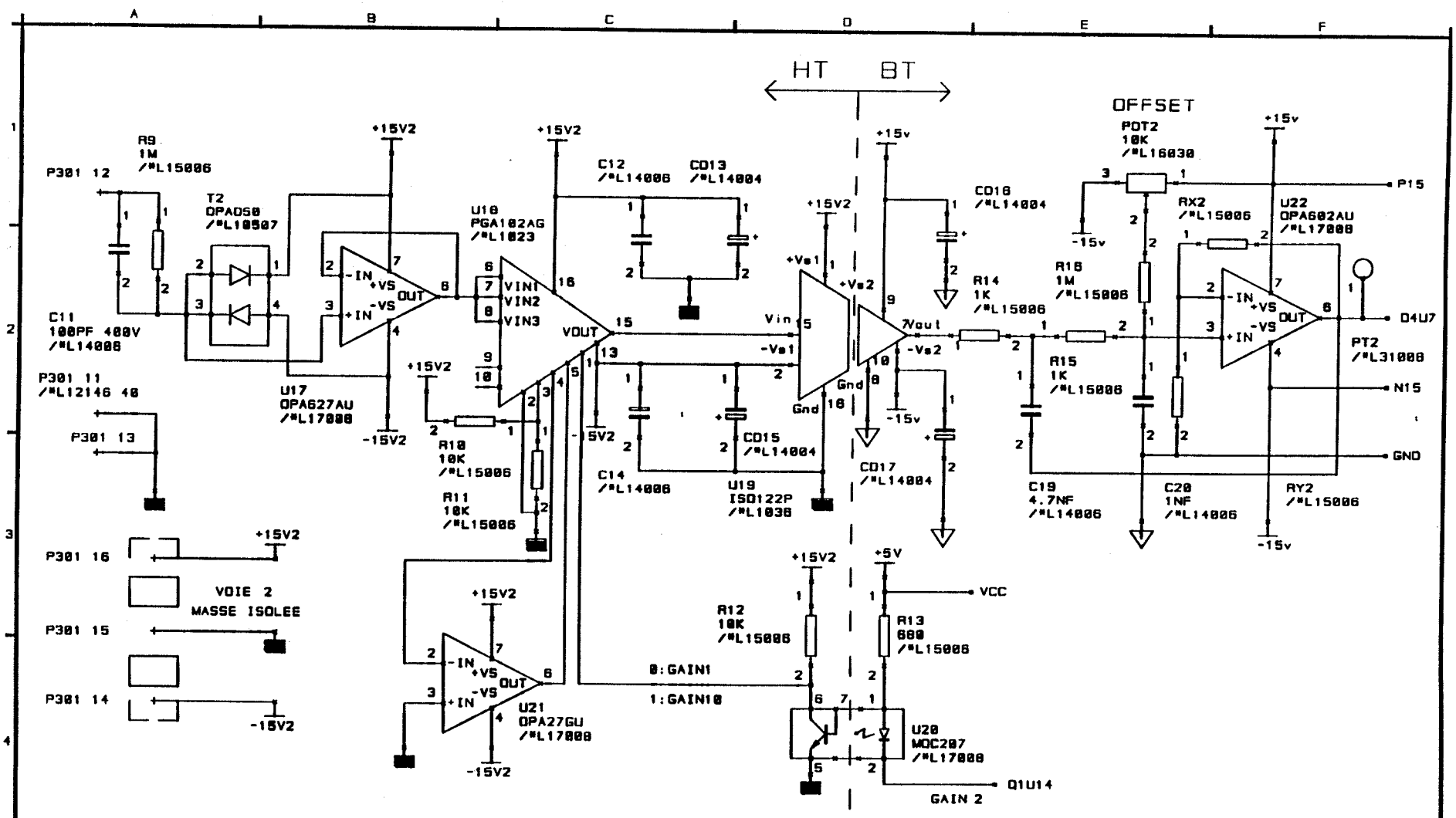
SAUF INDICATION CONTRAIRE

RX1 = 100R

RY1 = RESISTANCE A CALIBRER (SUR LES HUIT VOIES)

AUTEUR: JJT	VERIF: FC	MODIF.: JJT	FICH: MODANA10.SOX
DATE: 15/06/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 FOLIO: 1/12
SOUS-ENSEMBLE: ENTREES ISOLEES ANALOG INPUTS			SUJET: F2910103
			VERSION: X B C D E F
ENSEMBLE: 6061			RACAL-SYSTEMS 10 AV. QUATARTRE 78150 LE CHESNAY

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NOTA

TOUS LES CONDENSATEURS POLARISES SONT DE 10MF 16V

TOUS LES CONDENSATEURS NON POLARISES SONT DE 100NF

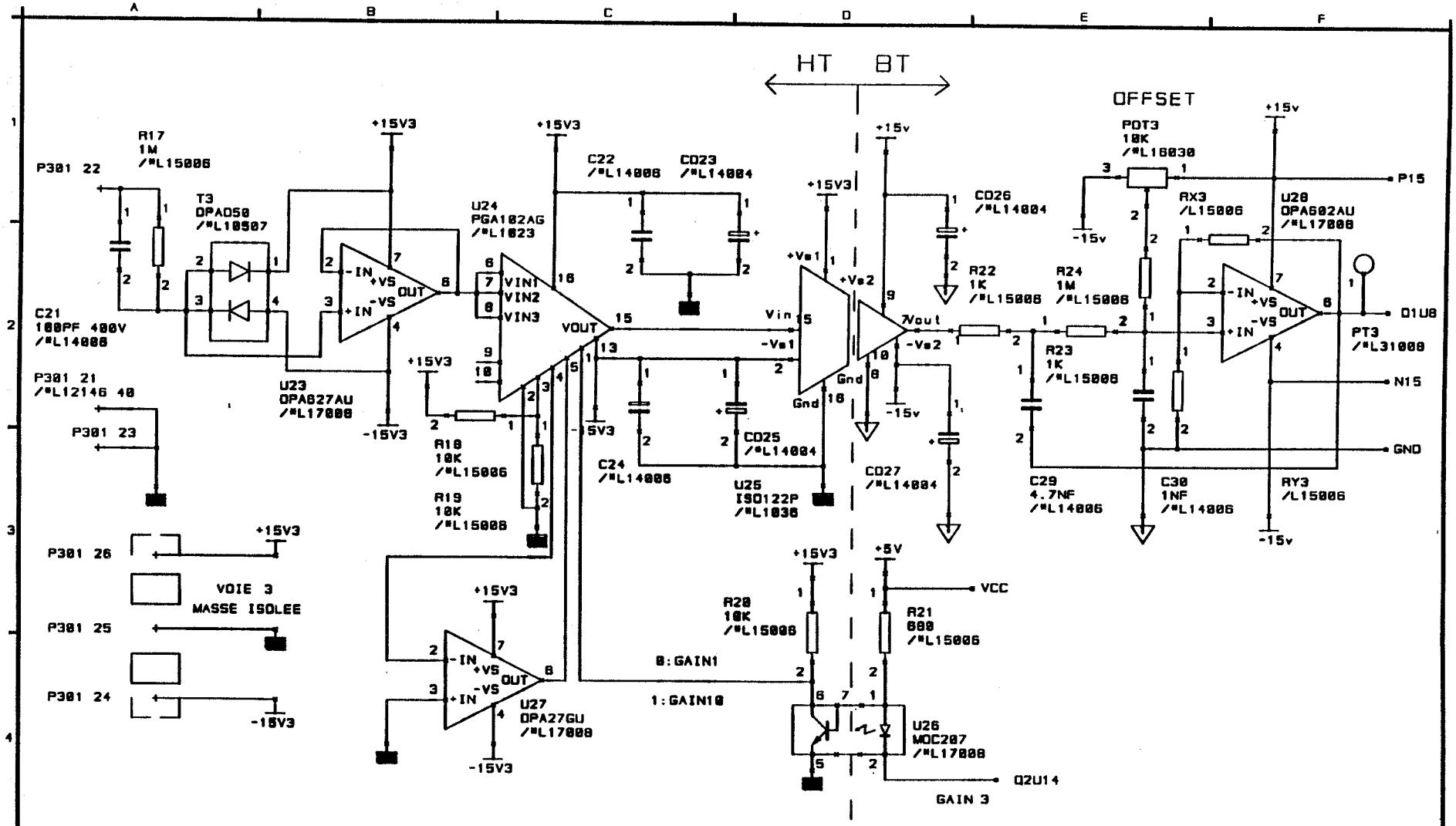
SAUF INDICATION CONTRAIRE

RX2 = 100R

RY2 = RESISTANCE A CALIBRER (SUR LES HUIT VOIES)

AUTEUR: JJT	VERIF: FC	MODIF: JJT	FICH: MODANA28.SOX	
DATE: 15/06/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1	FOLIO: 2/12
SOUS-ENSEMBLE: ENTREES ISOLEES ANALOG INPUTS			SUJET: F2910103	
			VERSION: X A B C D E F	
ENSEMBLE: 6061			RACAL-SYSTEMS 10 AV. OUTARTRE 78150 LE CHESNAY	

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NOTA

TOUS LES CONDENSATEURS POLARISES SONT DE 10MF 16V

TOUS LES CONDENSATEURS NON POLARISES SONT DE 100NF

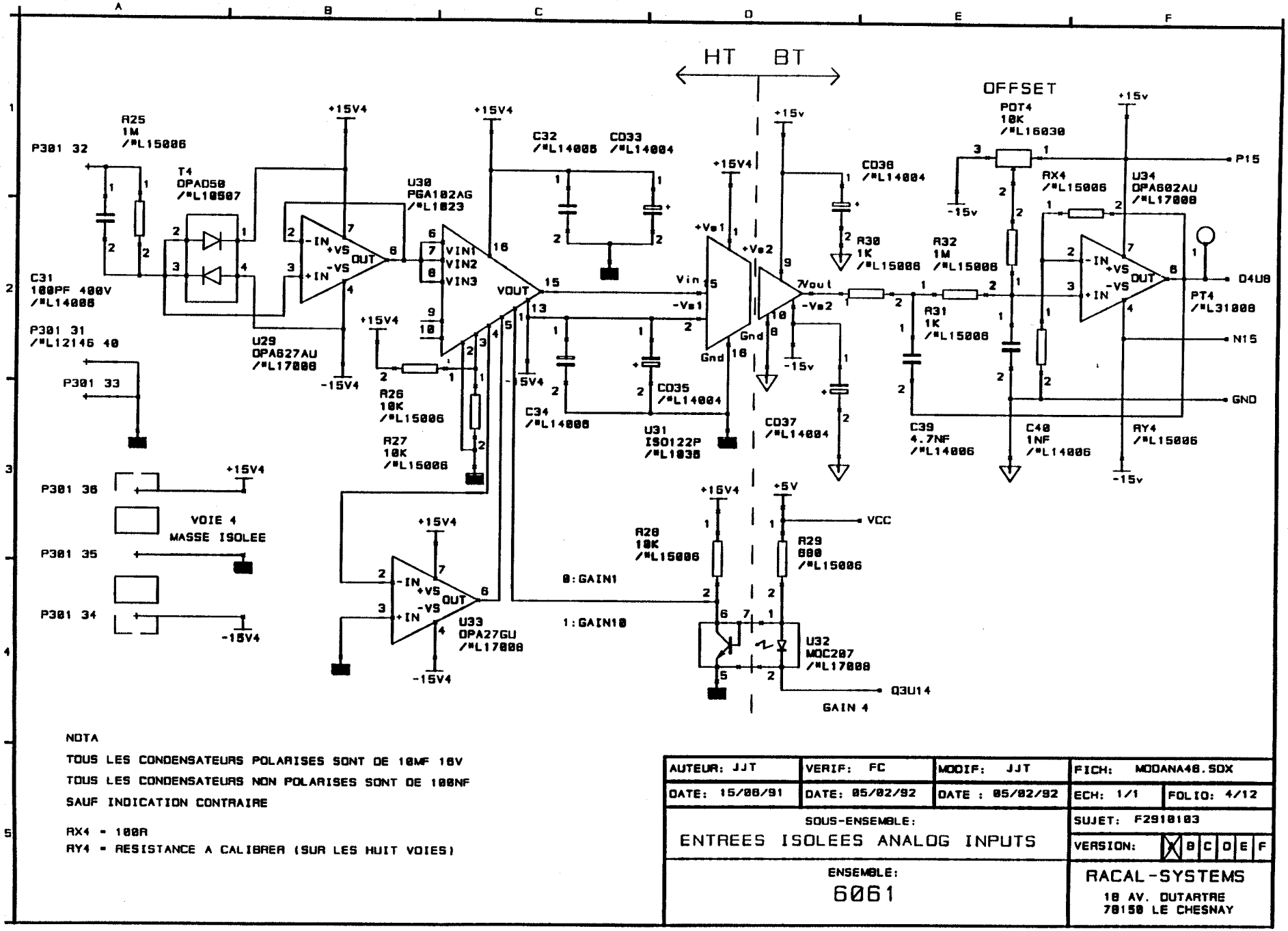
SAUF INDICATION CONTRAIRE

RX3 = 100R

RY3 = RESISTANCE A CALIBRER (SUR LES HUIT VOIES)

AUTEUR: JJT	VERIF: FC	MODIF: JJT	FICH: MODANA36.SDX
DATE: 15/06/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 FOLIO: 3/12
SOUS-ENSEMBLE: ENTREES ISOLEES ANALOG INPUTS			SUJET: F2910103
			VERSION: X B C D E F
ENSEMBLE: 6061			RACAL-SYSTEMS 18 AV. DUTARTRE 78150 LE CHESNAY

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NOTA

TOUS LES CONDENSATEURS POLARISES SONT DE 10MF 16V

TOUS LES CONDENSATEURS NON POLARISES SONT DE 100NF

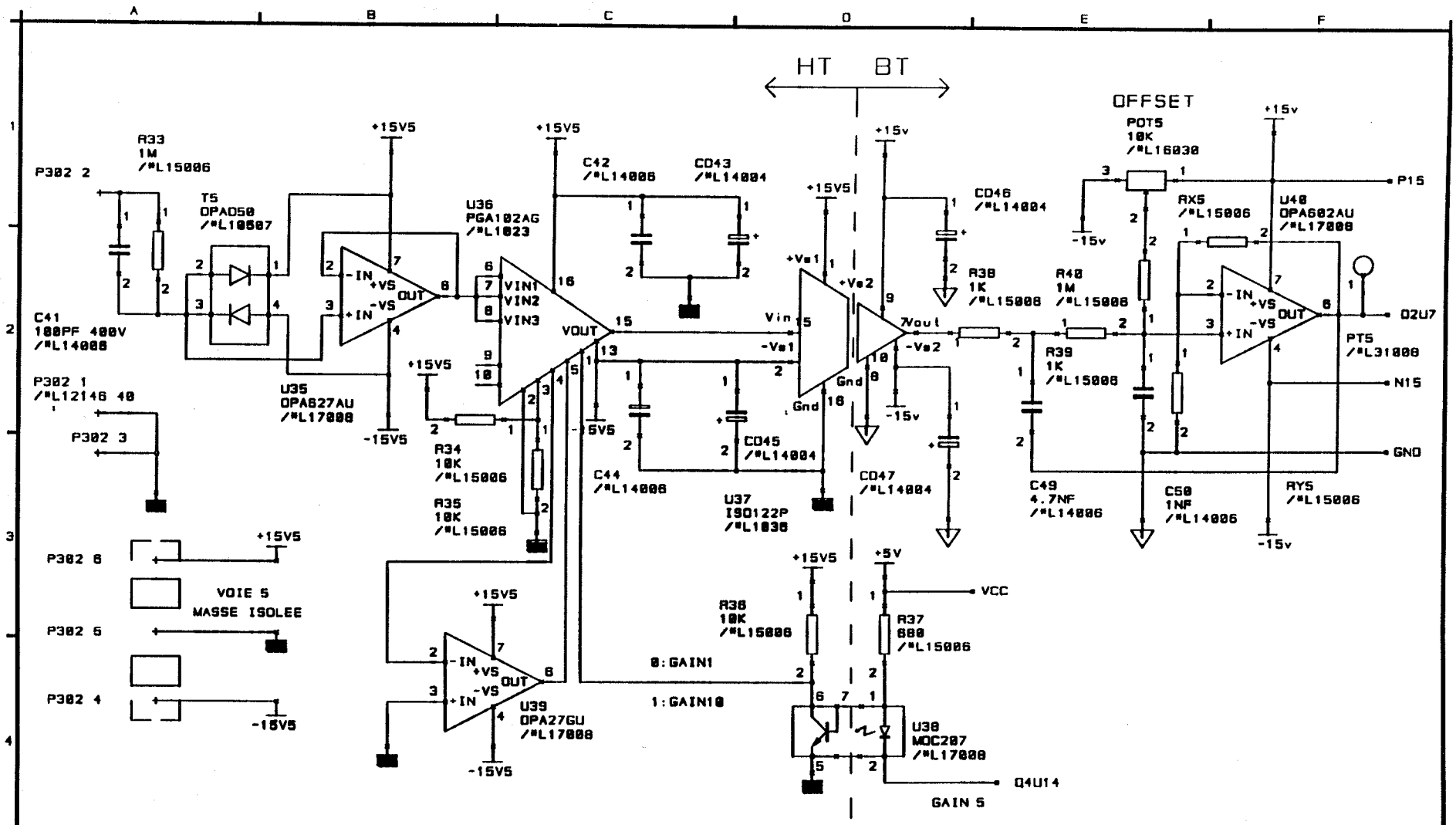
SAUF INDICATION CONTRAIRE

RX4 = 100R

RY4 = RESISTANCE A CALIBRER (SUR LES HUIT VOIES)

AUTEUR: JJT	VERIF: FC	MODIF: JJT	FICH: MODANA48.SDX
DATE: 15/08/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 FOLIO: 4/12
SOUS-ENSEMBLE: ENTREES ISOLEES ANALOG INPUTS			SUJET: F2910103
			VERSION: X B C D E F
ENSEMBLE: 6061			RACAL-SYSTEMS 18 AV. DUTARTRE 78150 LE CHESNAY

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NOTA

TOUS LES CONDENSATEURS POLARISES SONT DE 10MF 16V

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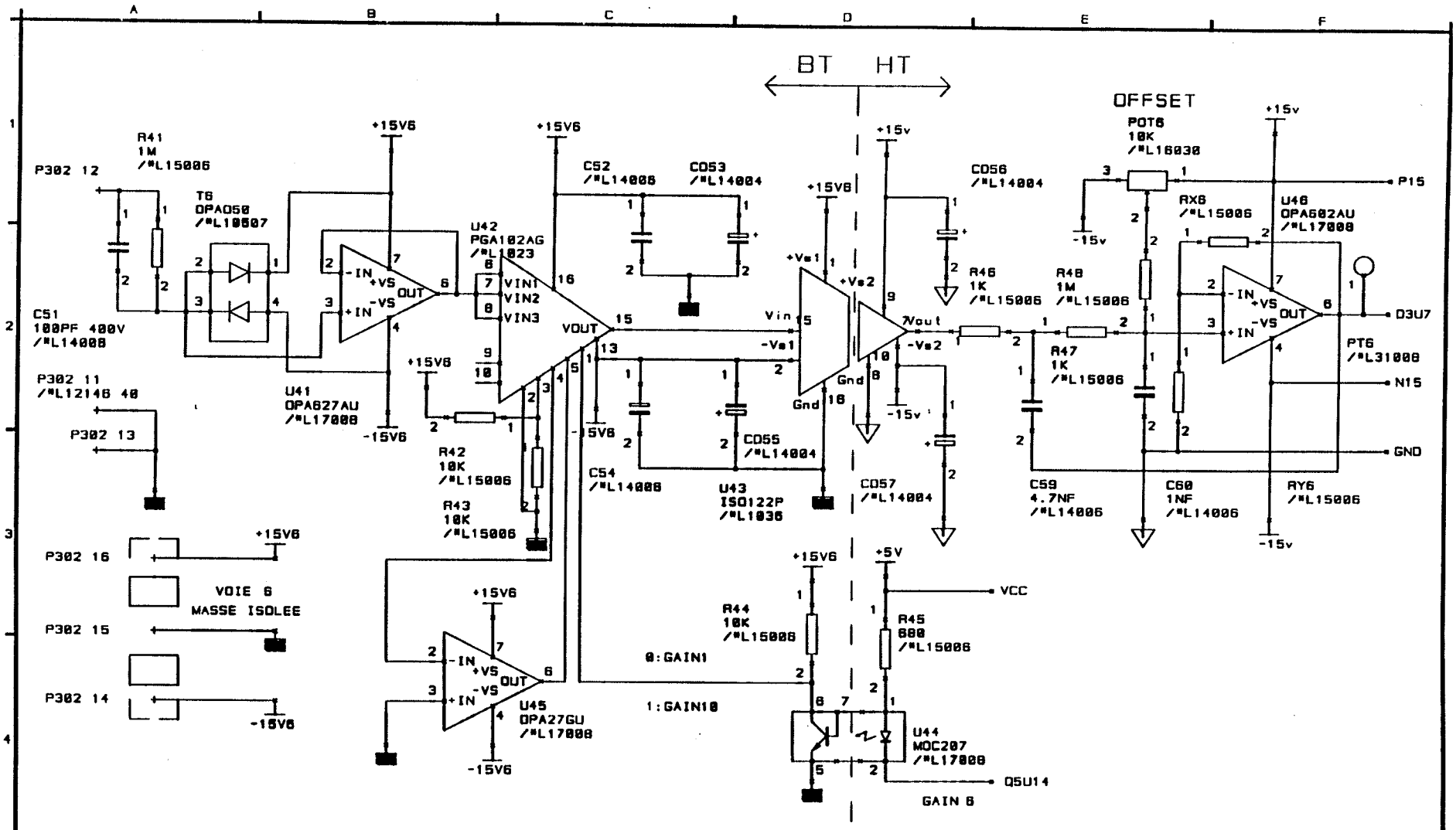
SAUF INDICATION CONTRAIRE

RX5 = 100R

RY5 = RESISTANCE A CALIBRER (SUR LES HUIT VOIES)

AUTEUR: JJT	VERIF: FC	MODIF: JJT	FICH: MODANA68.SOX
DATE: 15/08/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 FOLIO: 5/12
SOUS-ENSEMBLE: ENTREES ISOLEES ANALOG INPUTS			SUJET: F2910103
			VERSION: X B C D E F
ENSEMBLE: 6061			RACAL-SYSTEMS 10 AV. DUTARTRE 78150 LE CHESNAY

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NOTA

TOUS LES CONDENSATEURS POLARISES SONT DE 10MF 16V

TOUS LES CONDENSATEURS NON POLARISES SONT DE 100NF

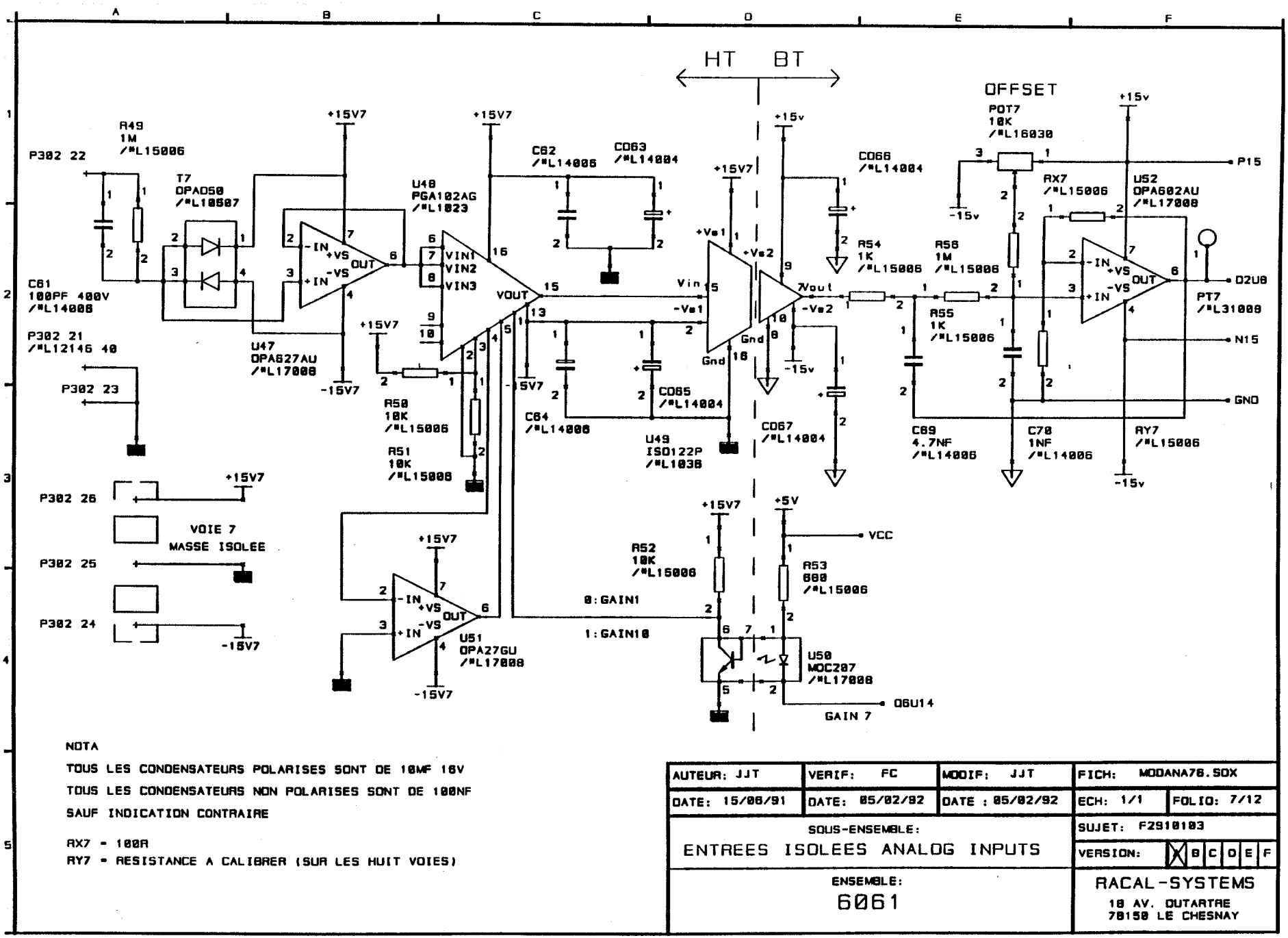
SAUF INDICATION CONTRAIRE

RX6 = 100R

RY6 = RESISTANCE A CALIBRER (SUR LES HUIT VOIES)

AUTEUR: JJT	VERIF: FC	MODIF: JJT	FICH: MDOANA86.SDX
DATE: 15/06/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 FOLIO: 6/12
SOUS-ENSEMBLE: ENTREES ISOLEES ANALOG INPUTS			SUJET: F2910103
			VERSION: X B C D E F
ENSEMBLE: 6061			RACAL-SYSTEMS 10 AV. DUTARTRE 78150 LE CHESNAY

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NOTA

TOUS LES CONDENSATEURS POLARISES SONT DE 10MF 16V

TOUS LES CONDENSATEURS NON POLARISES SONT DE 100NF

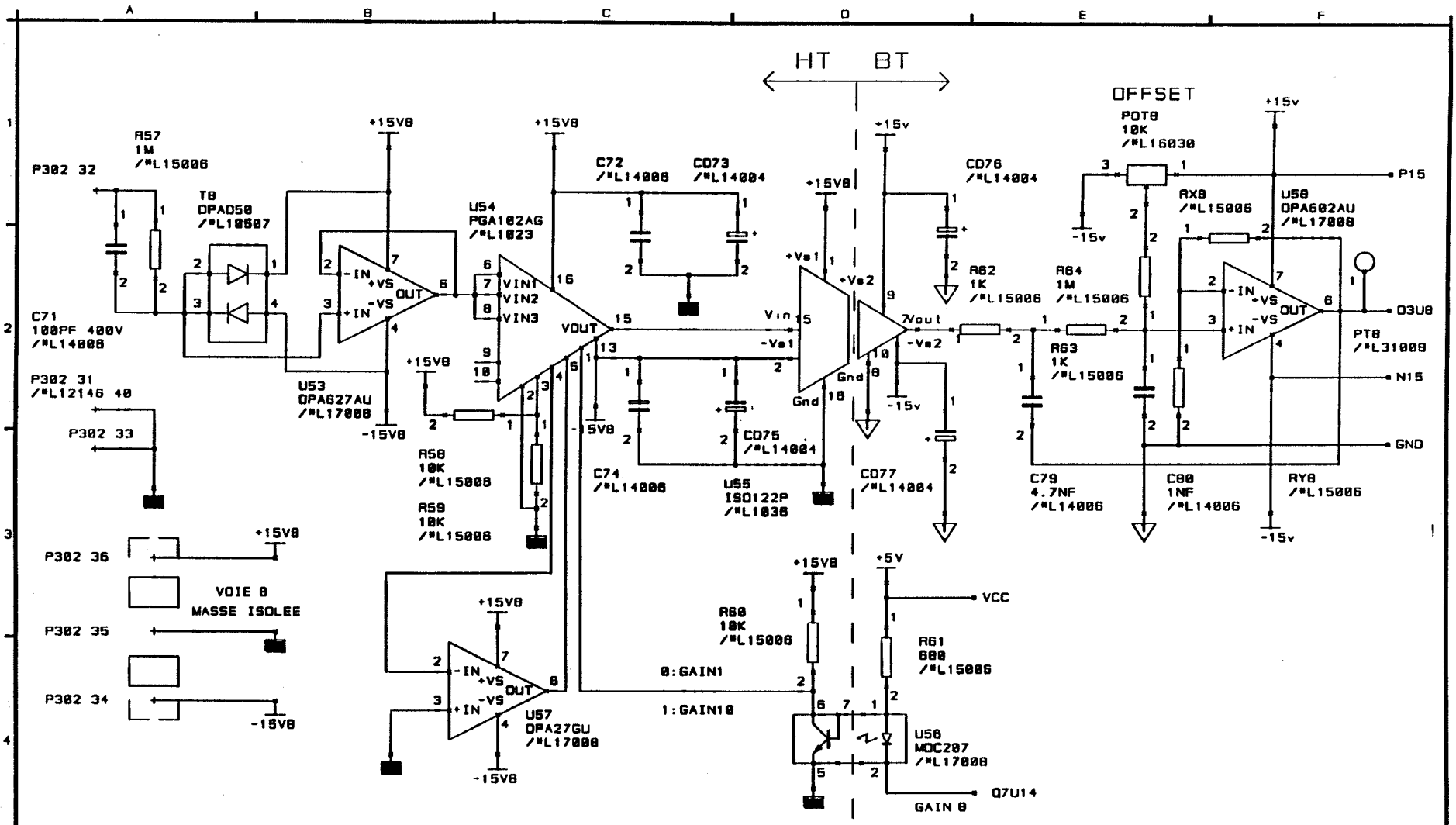
SAUF INDICATION CONTRAIRE

RX7 = 100R

RY7 = RESISTANCE A CALIBRER (SUR LES HUIT VOIES)

AUTEUR: JJT	VERIF: FC	MODIF: JJT	FICH: MODANA76.SOX
DATE: 15/06/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 — FOLIO: 7/12
SOUS-ENSEMBLE: ENTREES ISOLEES ANALOG INPUTS			SUJET: F2910103
			VERSION: X B C D E F
ENSEMBLE: 6061			RACAL-SYSTEMS 18 AV. DUTARTRE 78150 LE CHESNAY

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NOTA

TOUS LES CONDENSATEURS POLARISES SONT DE 10MF 16V

TOUS LES CONDENSATEURS NON POLARISES SONT DE 100NF

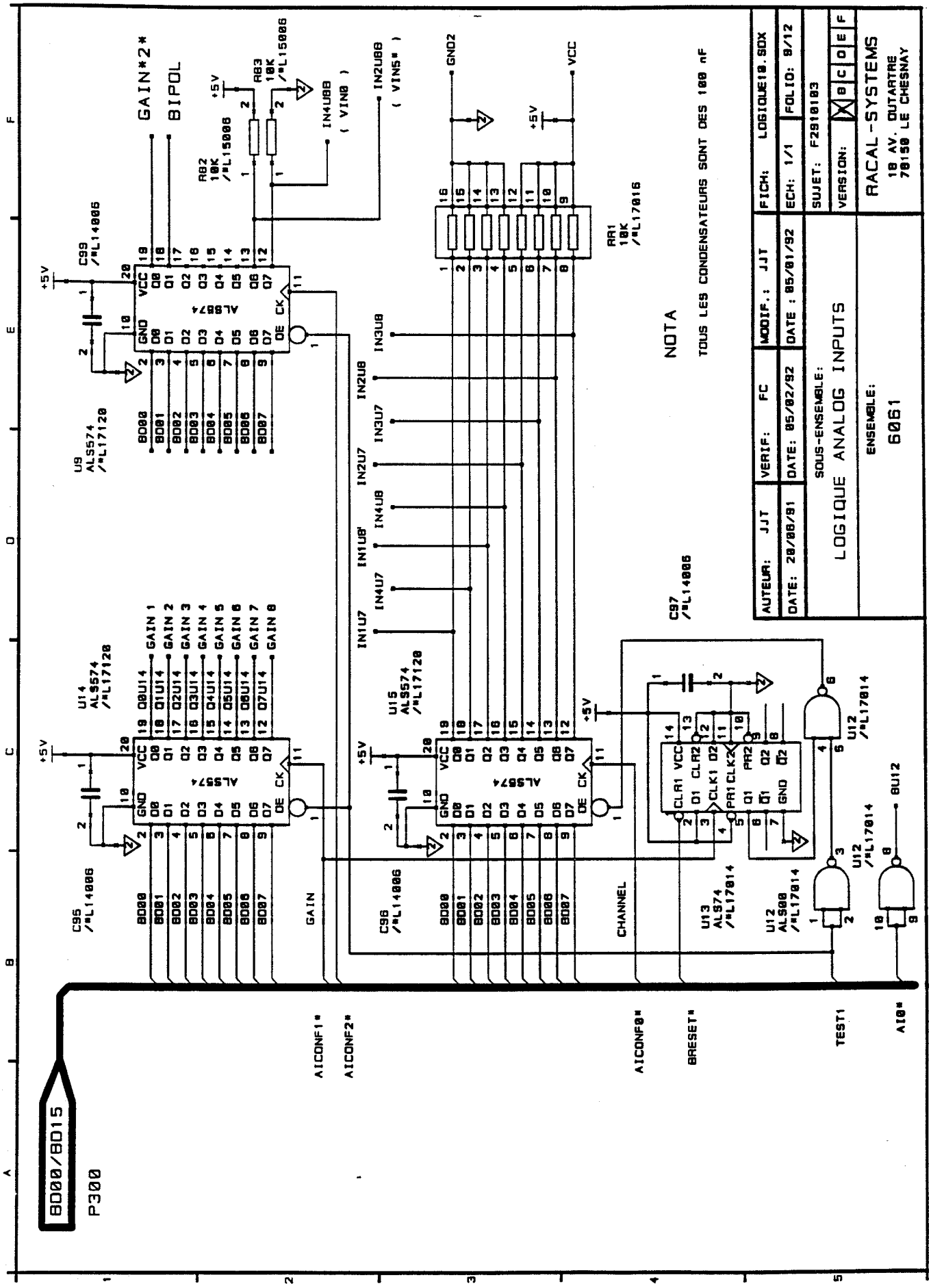
SAUF INDICATION CONTRAIRE

RX8 = 100R

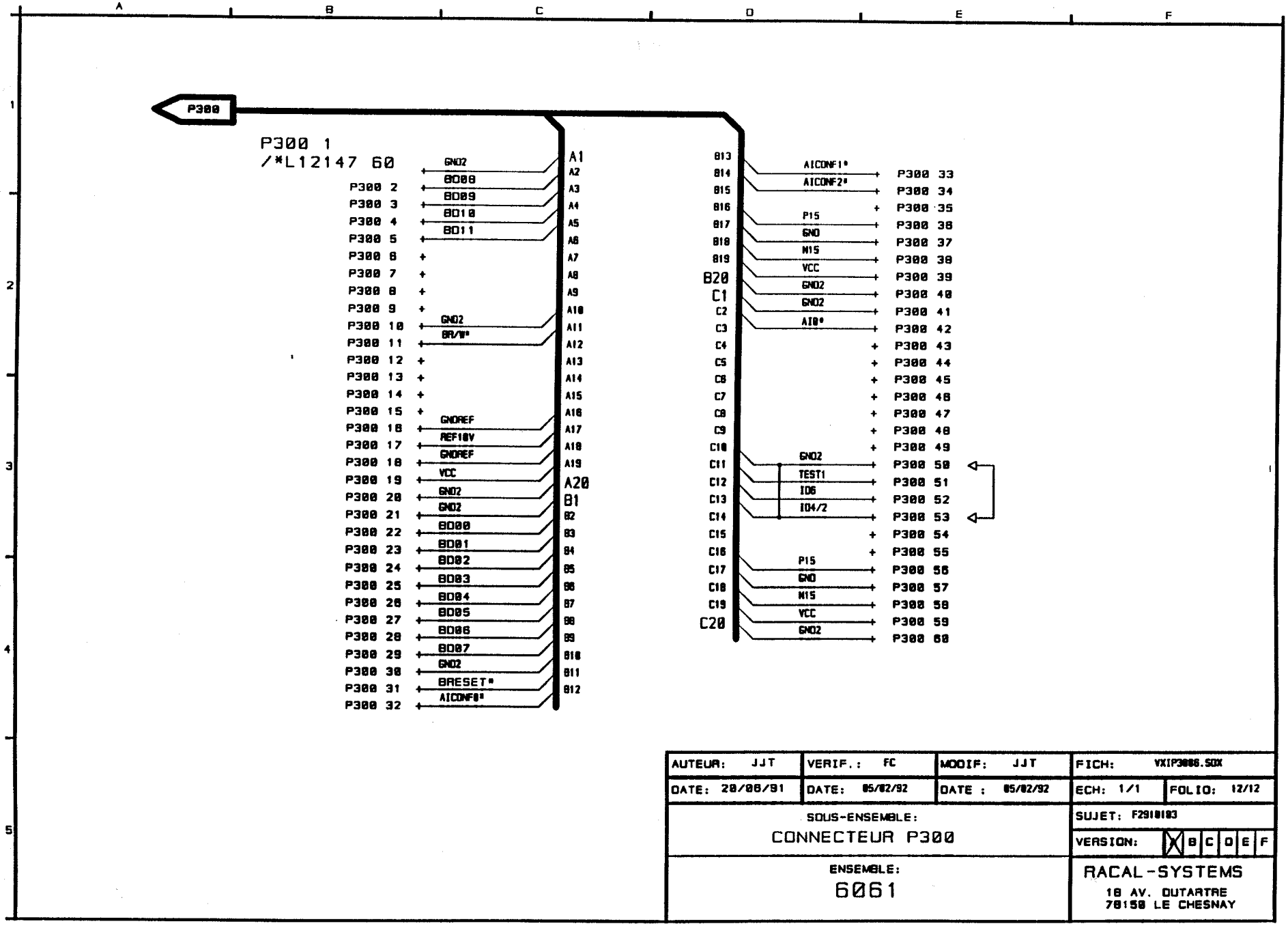
RY8 = RESISTANCE A CALIBRER (SUR LES HUIT VOIES)

AUTEUR: JJT	VERIF: FC	MODIF: JJT	FICH: MODANA08.SDX
DATE: 15/08/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 FOLIO: 8/12
SOUS-ENSEMBLE: ENTREES ISOLEES ANALOG INPUTS			SUJET: F2910103
			VERSION: X A B C D E F
ENSEMBLE: 6061			RACAL-SYSTEMS 10 AV. OUTARTRE 78150 LE CHESNAY

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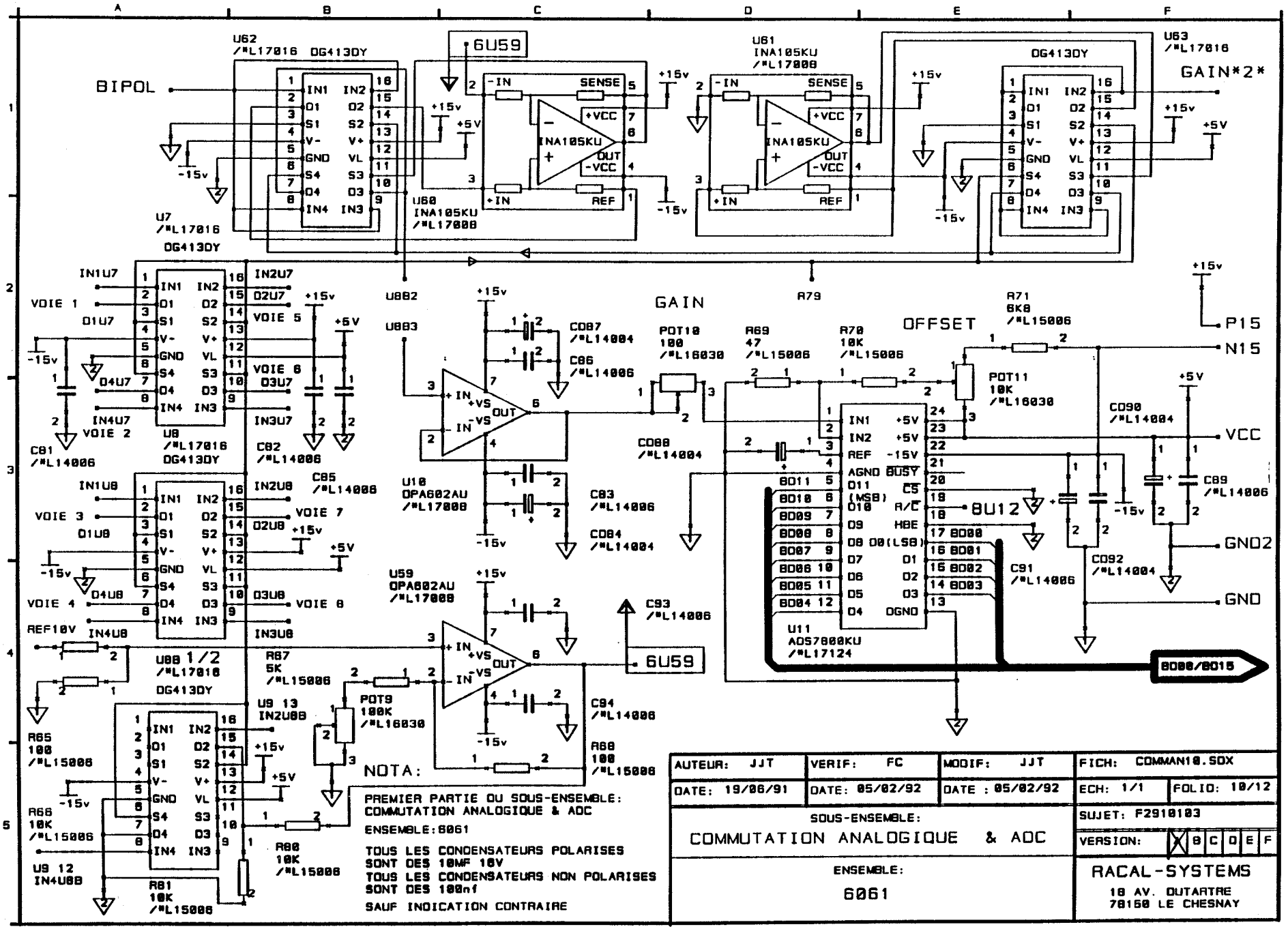


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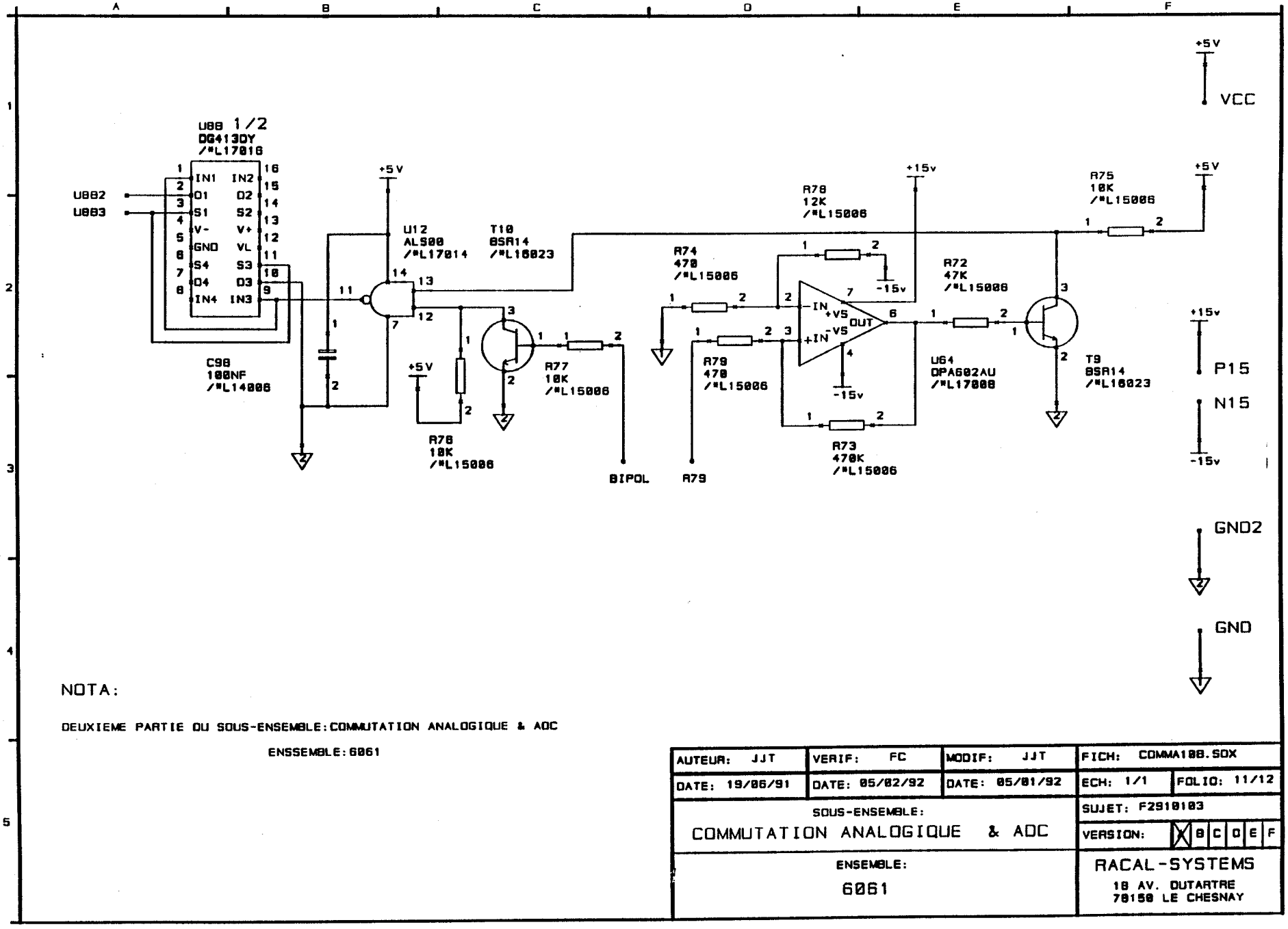


AUTEUR: JJT	VERIF.: FC	MODIF: JJT	FICH: VXIP3000.SOX
DATE: 20/08/91	DATE: 05/02/92	DATE : 05/02/92	ECH: 1/1 FOLIO: 12/12
SOUS-ENSEMBLE: CONNECTEUR P300			SUJET: F2910103
			VERSION: X B C D E F
ENSEMBLE: 6061			RACAL-SYSTEMS 10 AV. DUTARTRE 78150 LE CHESNAY

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NOTA:

DEUXIEME PARTIE DU SOUS-ENSEMBLE:COMMUTATION ANALOGIQUE & ADC

ENSSEMBLE:6061

AUTEUR: JJT	VERIF: FC	MODIF: JJT	FICH: COMMA100.SOX
DATE: 19/06/91	DATE: 05/02/92	DATE: 05/01/92	ECH: 1/1 FOLIO: 11/12
SOUS-ENSEMBLE: COMMUTATION ANALOGIQUE & ADC			SUJET: F2910103
			VERSION: X B C D E F
ENSEMBLE: 6061			RACAL-SYSTEMS 18 AV. DUTARTRE 78150 LE CHESNAY

8-4-13

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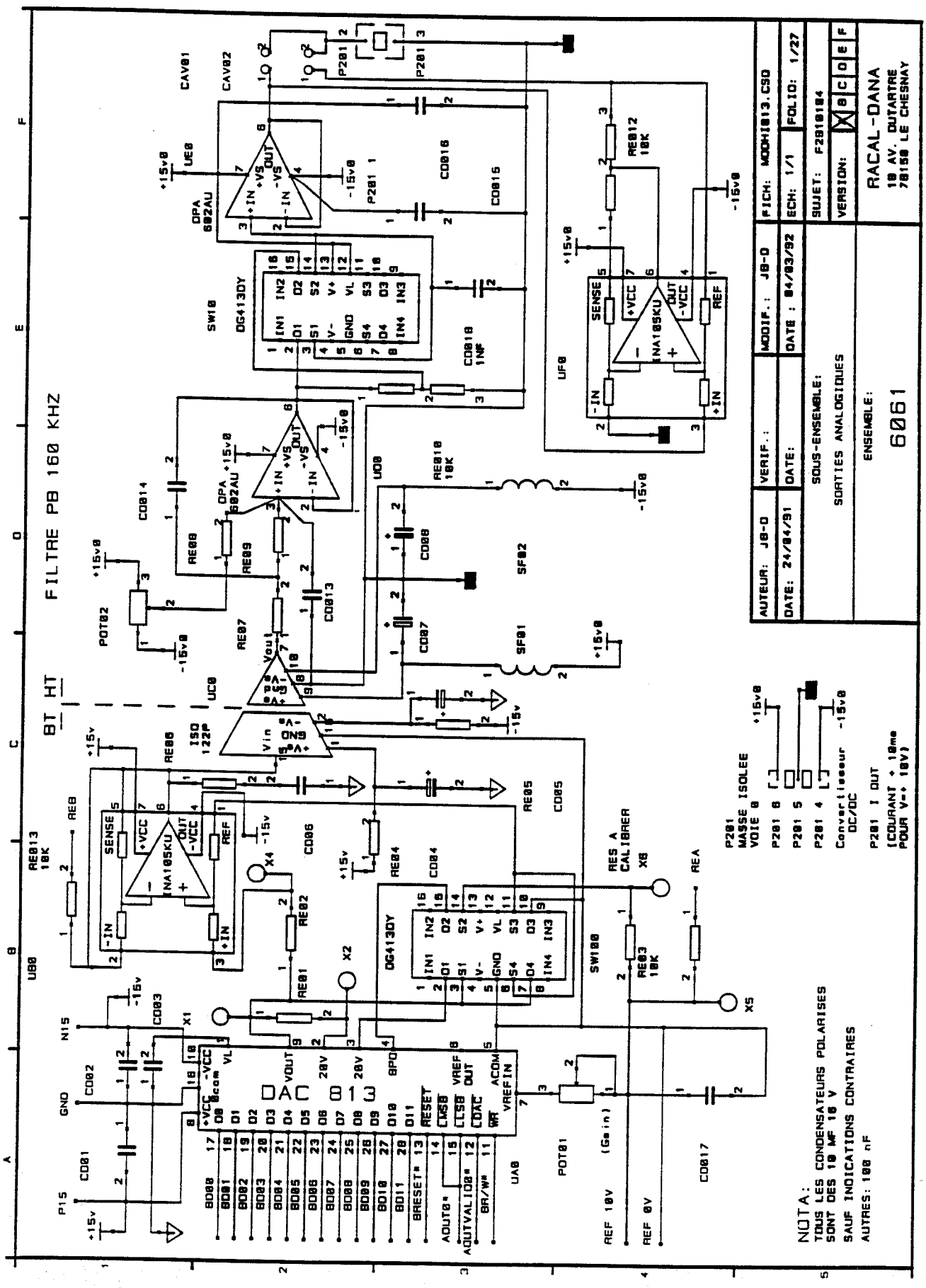
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SECTION 8-5

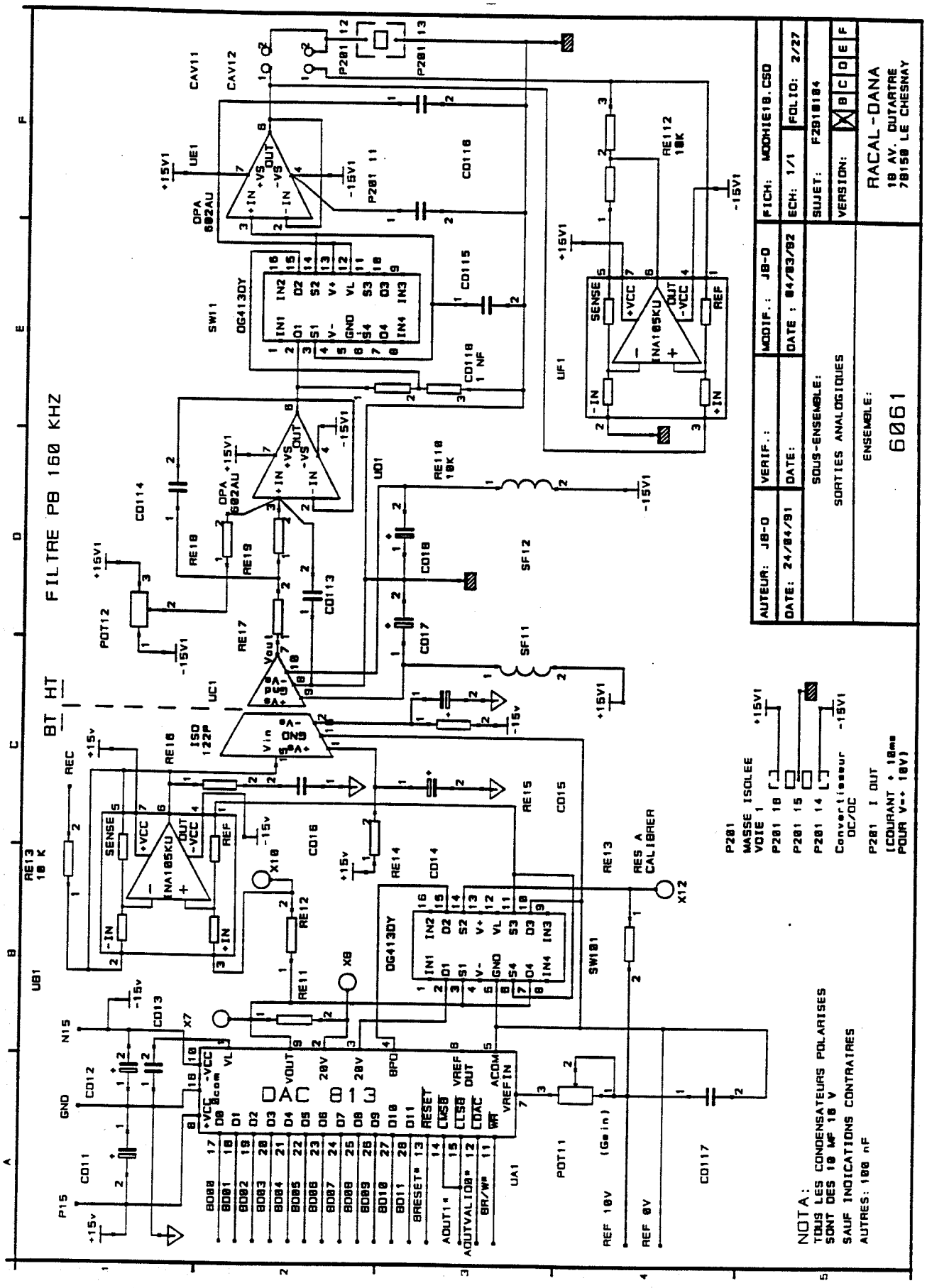
F2910103

SCHEMATICS
of the
ANALOG OUTPUTS
BOARD

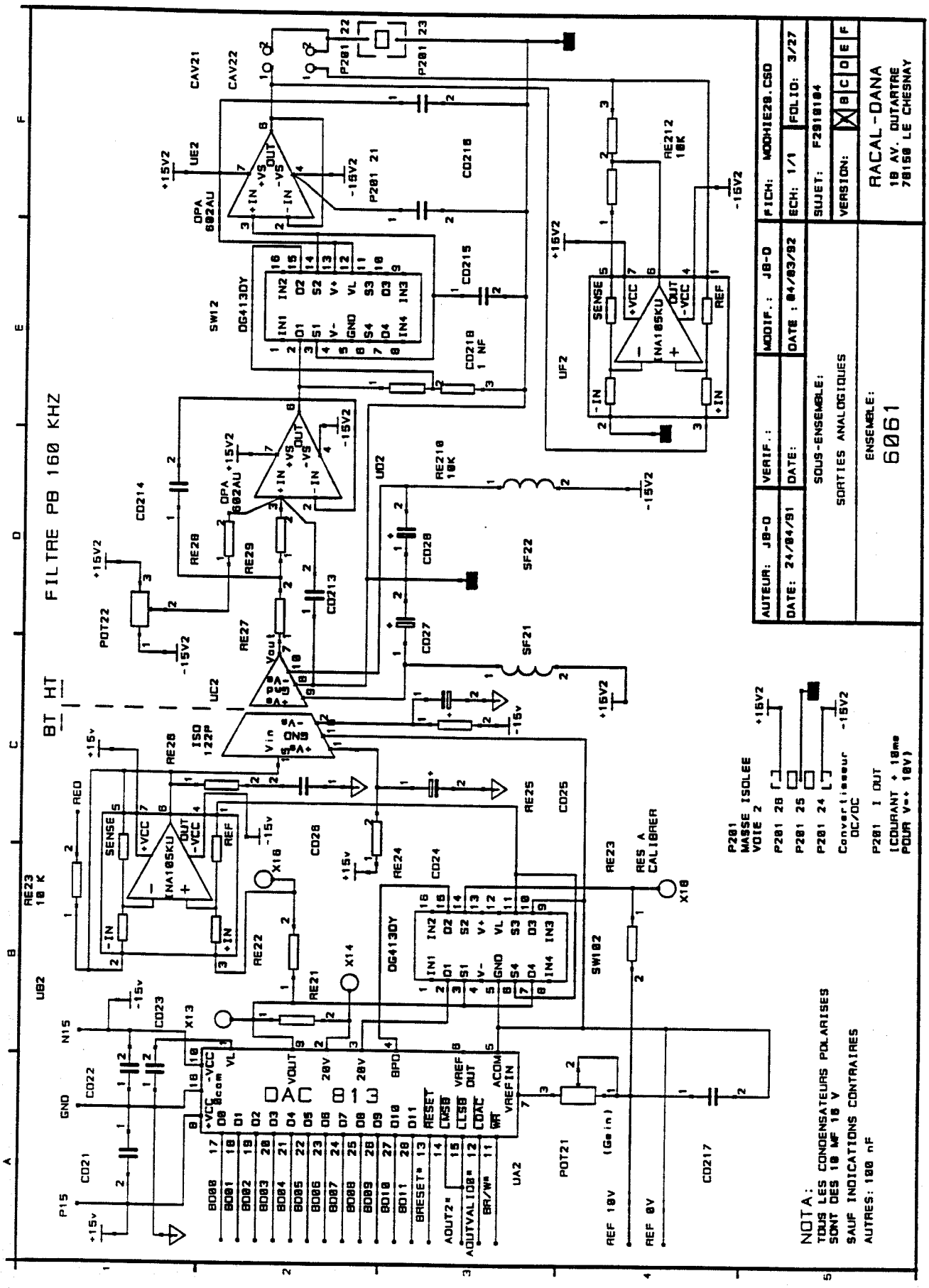
Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com



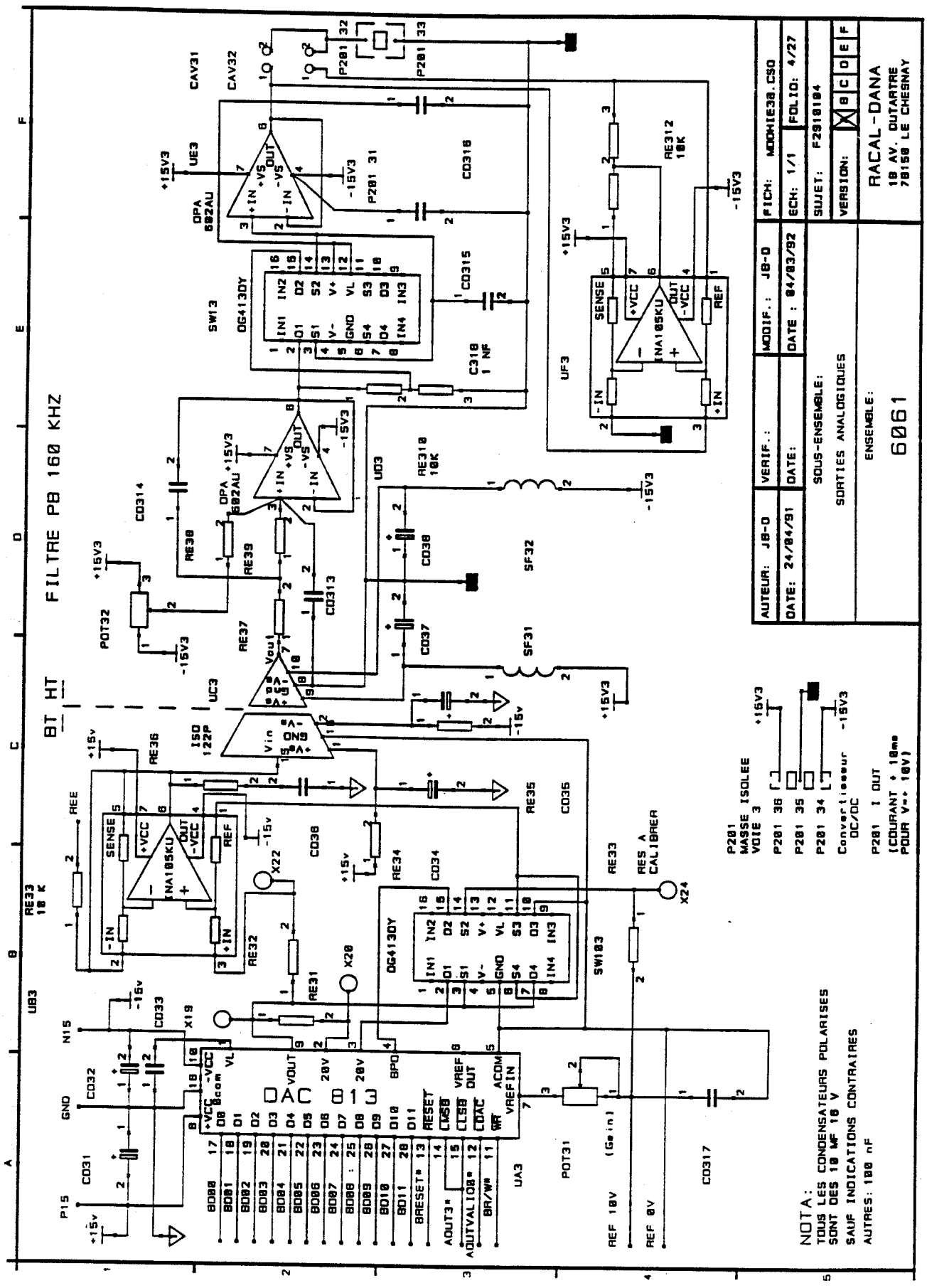
Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com



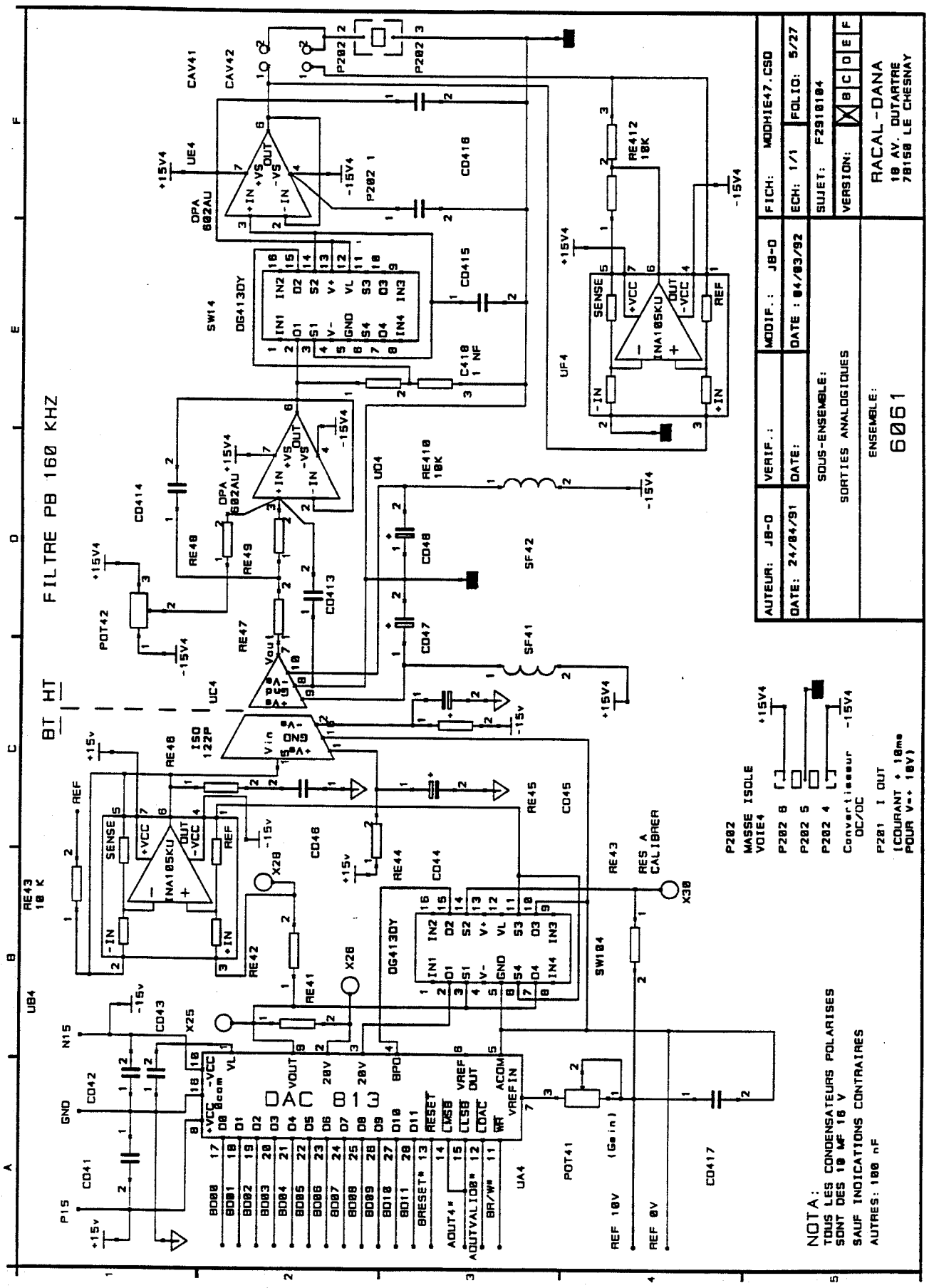
Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com



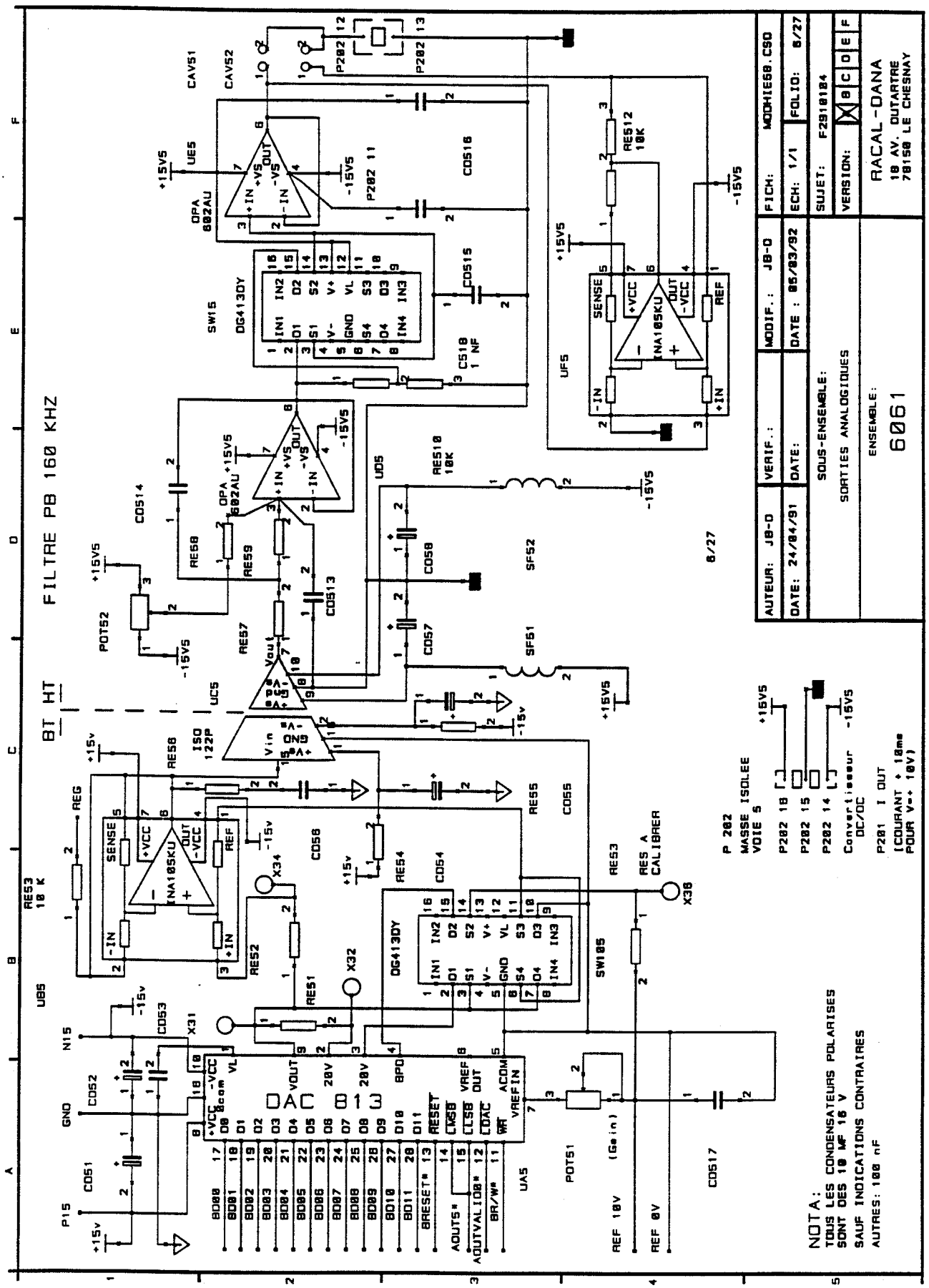
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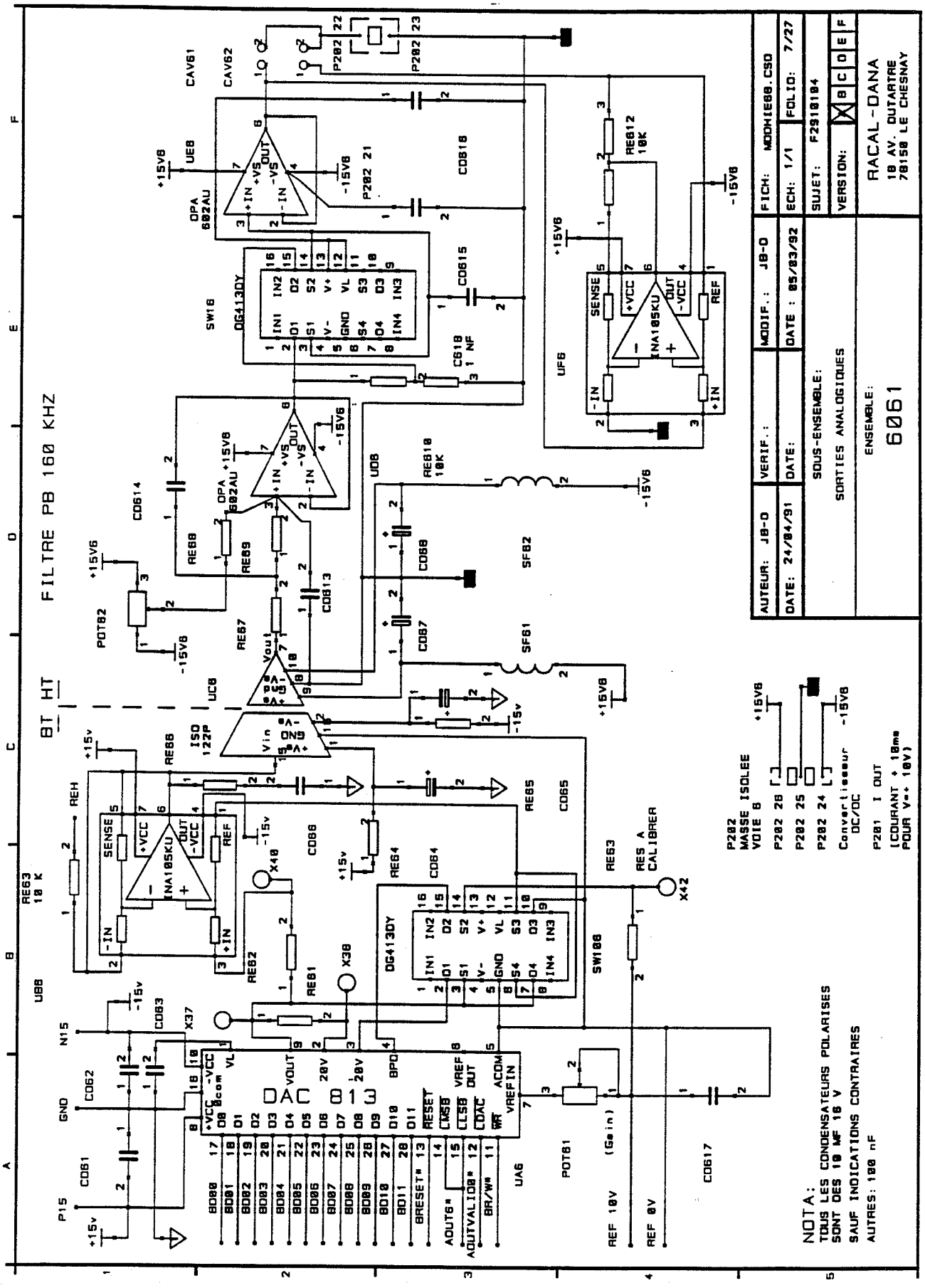
Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com



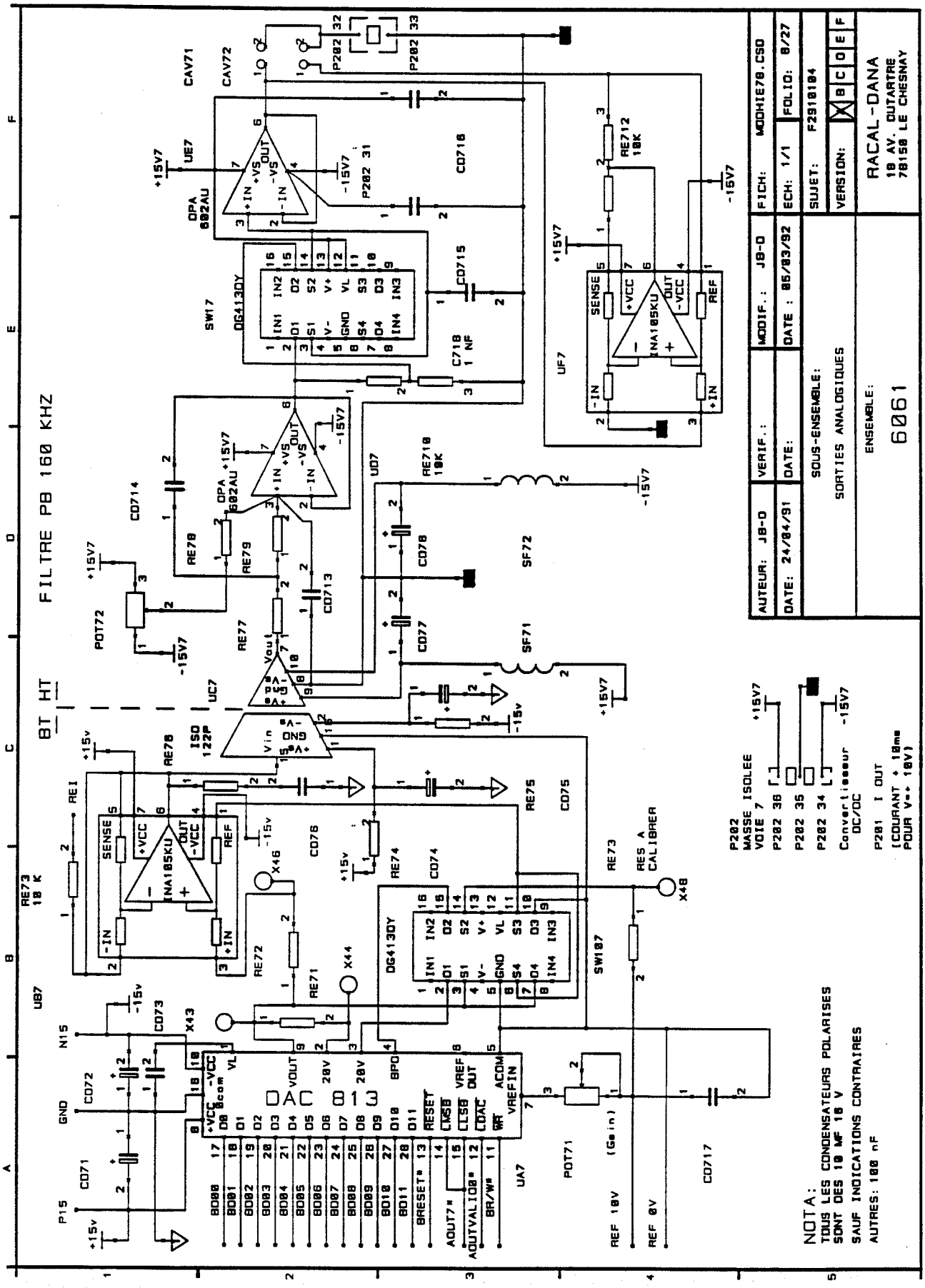
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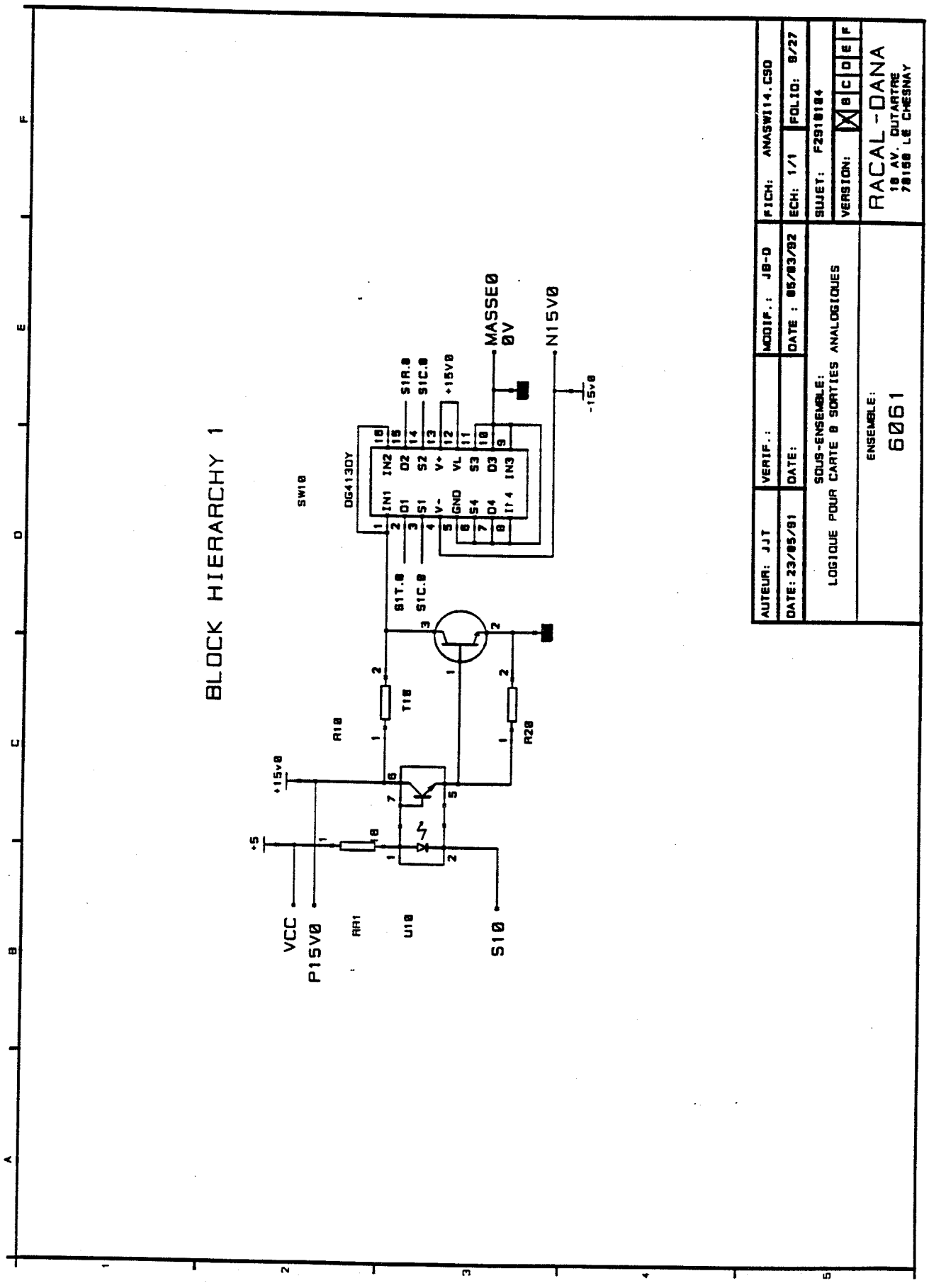
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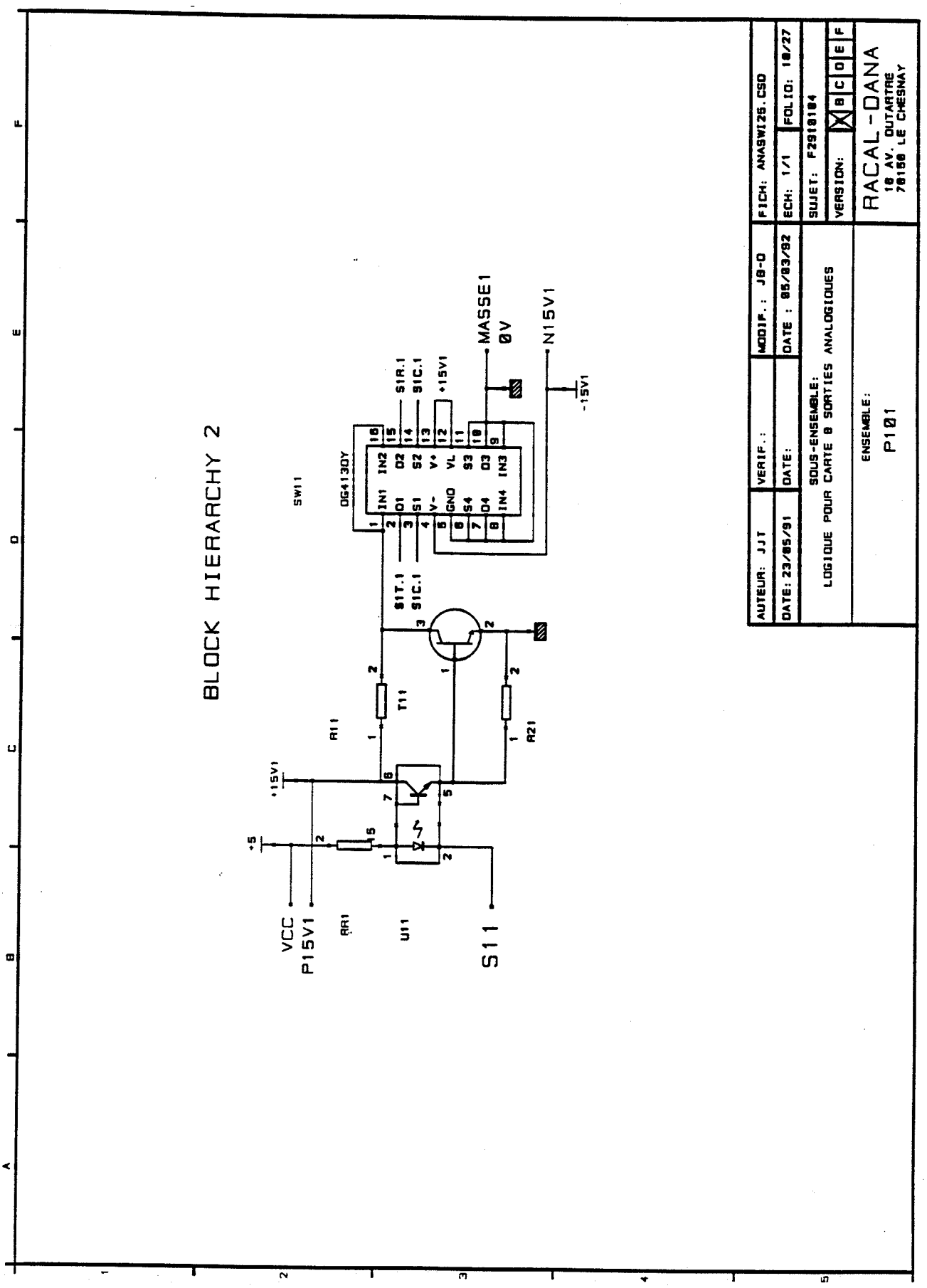
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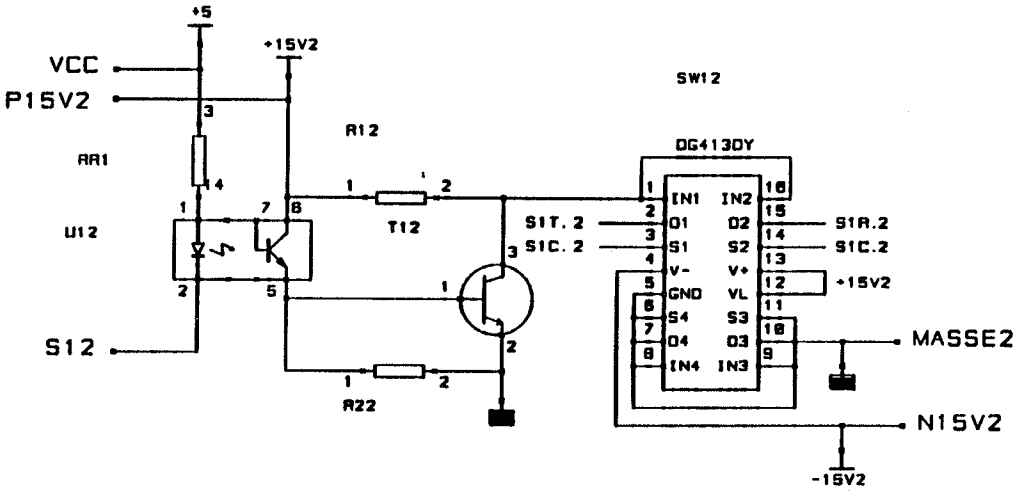


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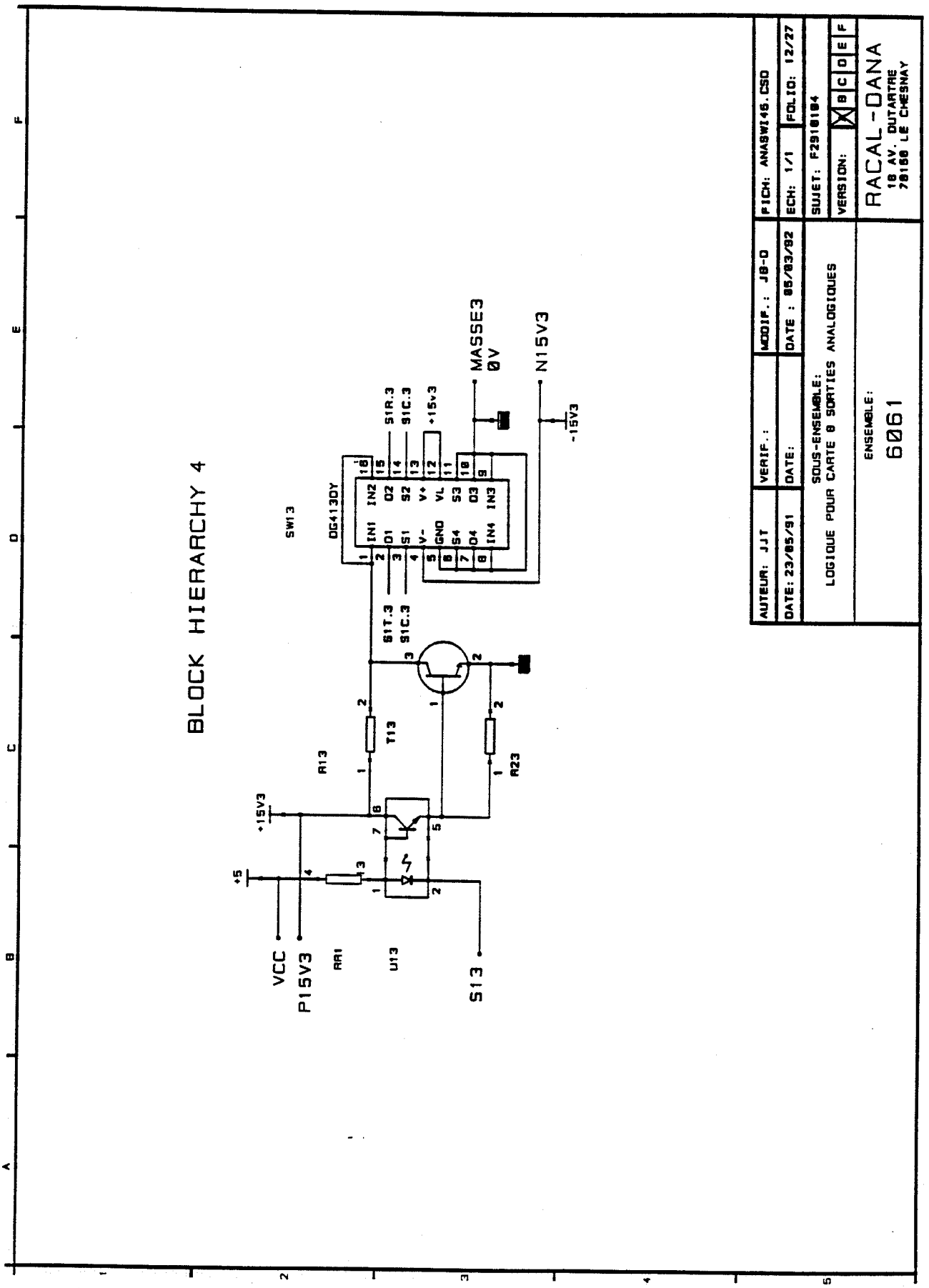
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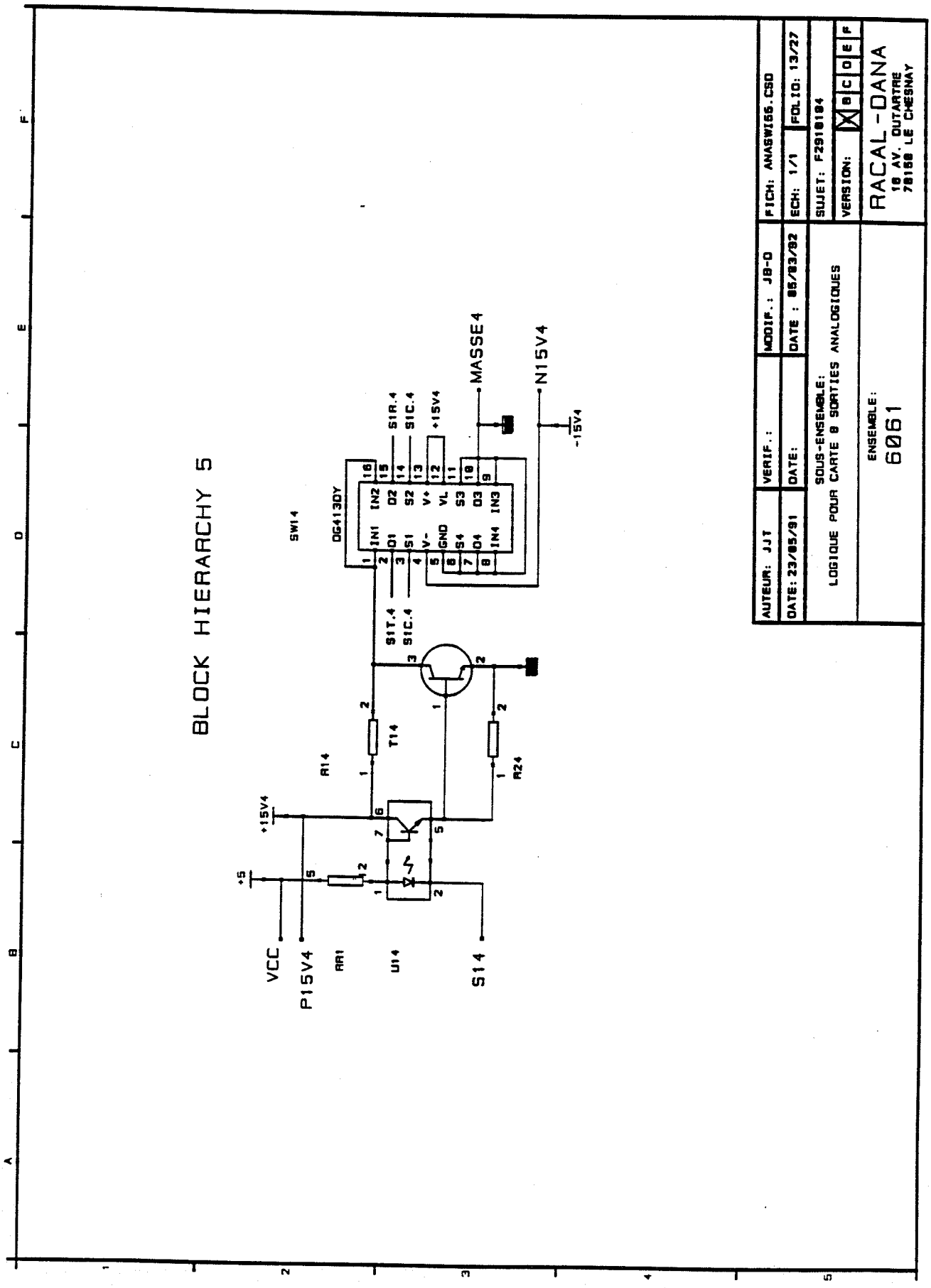


AUTEUR: JJT	VERIF.:	MODIF.: JB-D	FICH: ANASWI36.CSD
DATE: 23/05/91	DATE:	DATE : 05/03/92	ECH: 1/1 FOLIO: 11/27
SOUS-ENSEMBLE: LOGIQUE POUR CARTE 8 SORTIES ANALOGIQUES			SUJET: F2918184
			VERSION: X B C D E F
ENSEMBLE: 6061			RACAL-DANA 10 AV. DUTARTRE 78150 LE CHESNAY

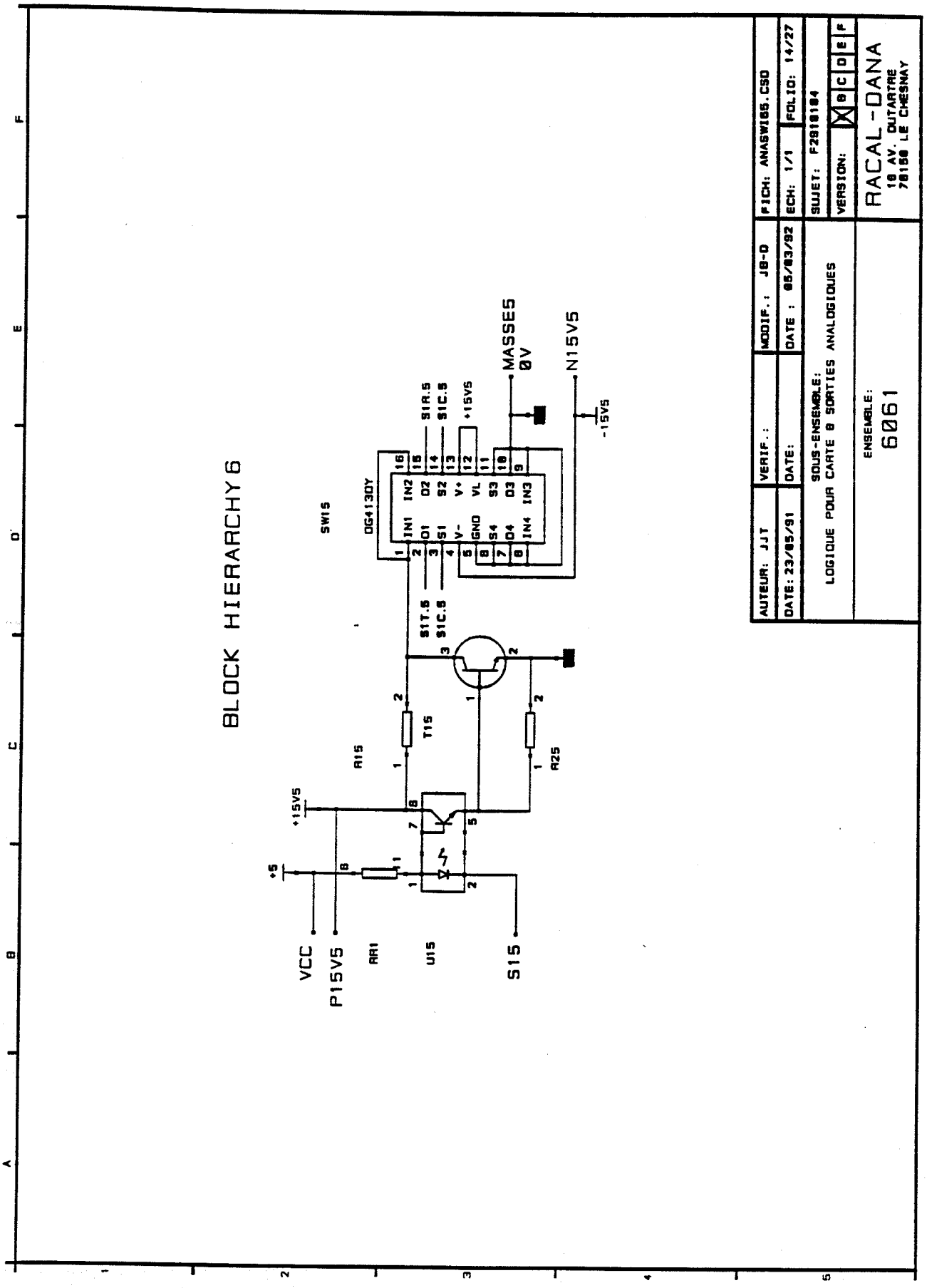
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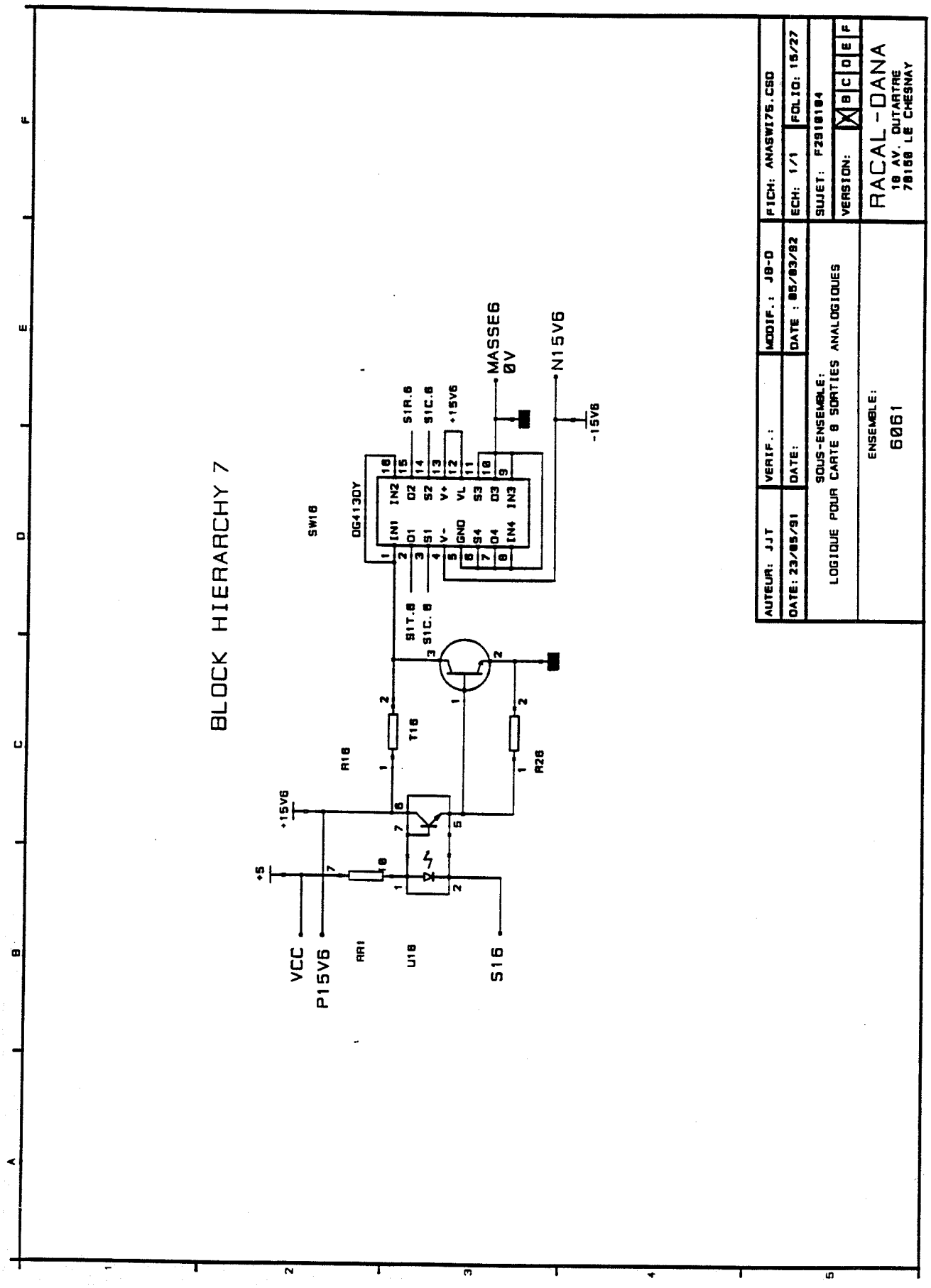
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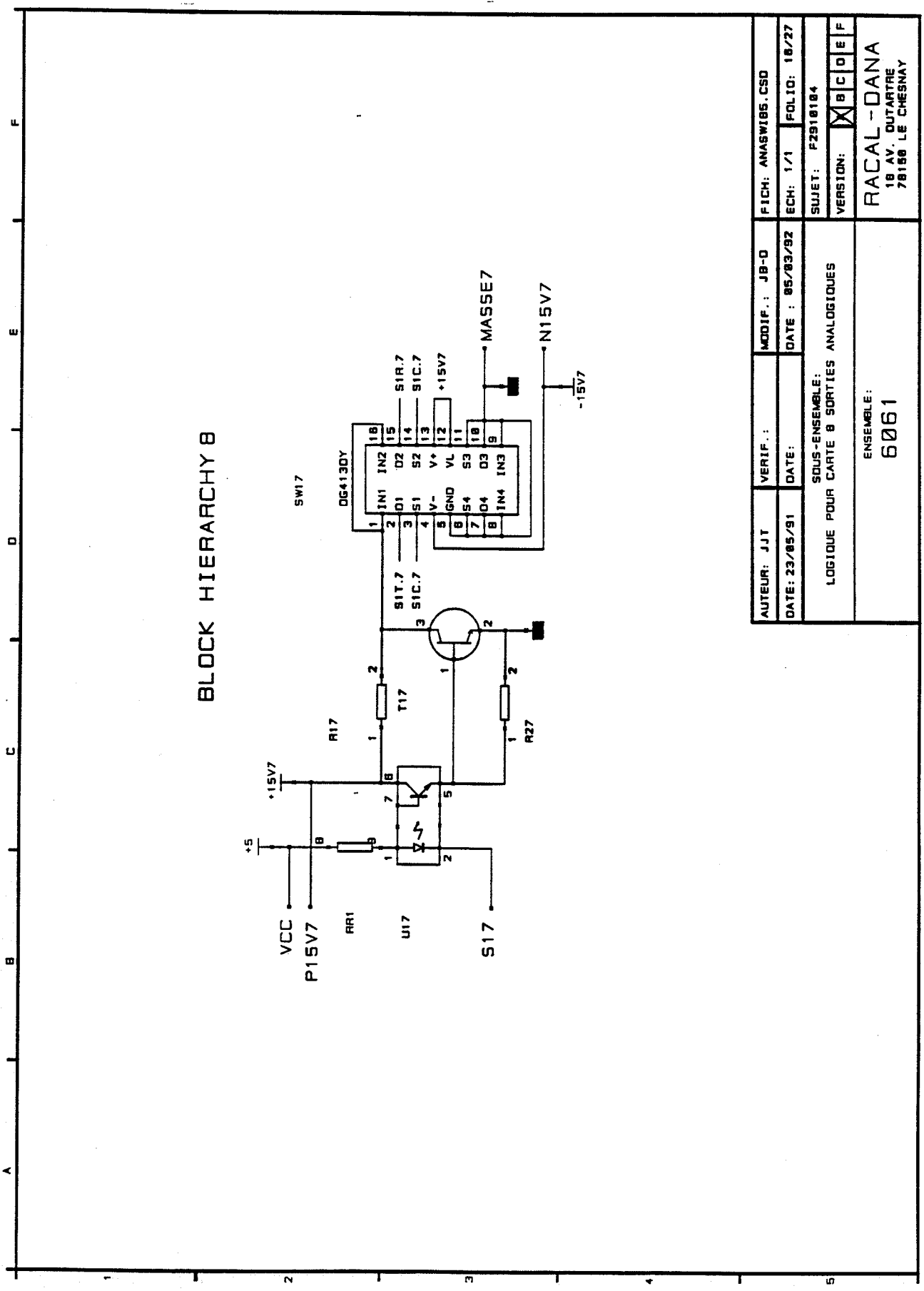
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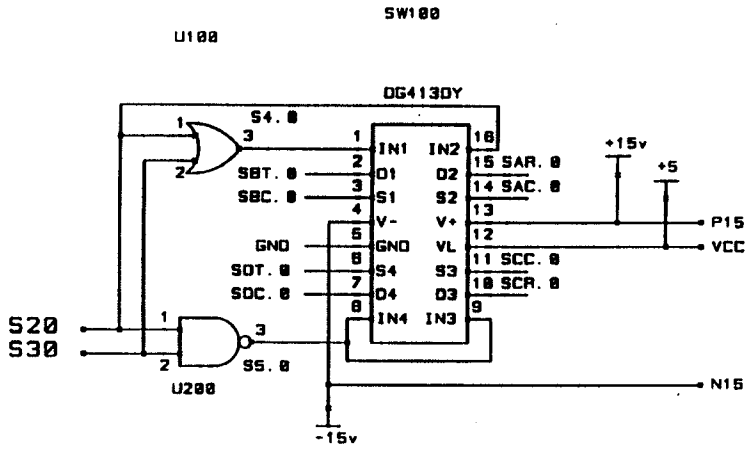


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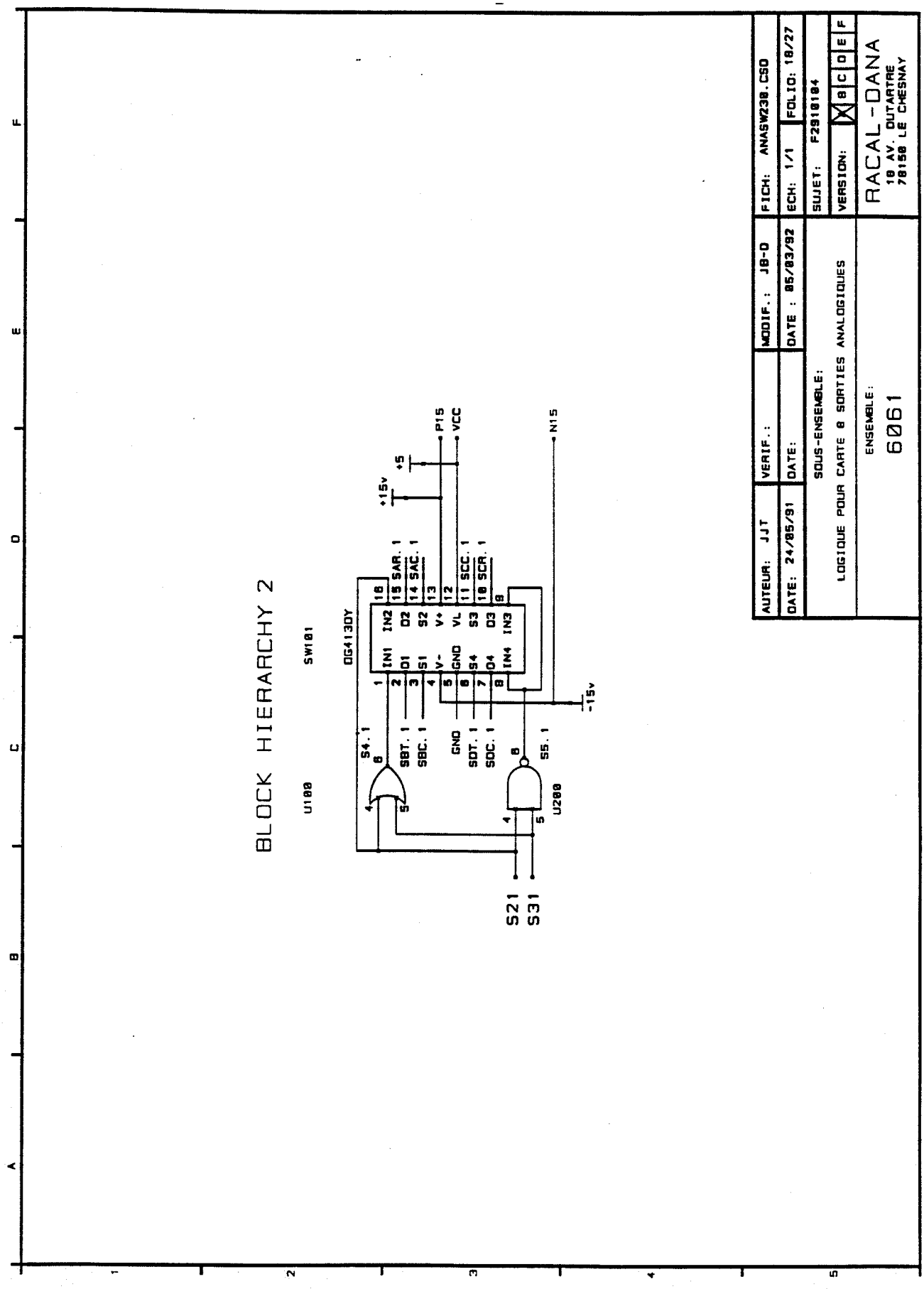
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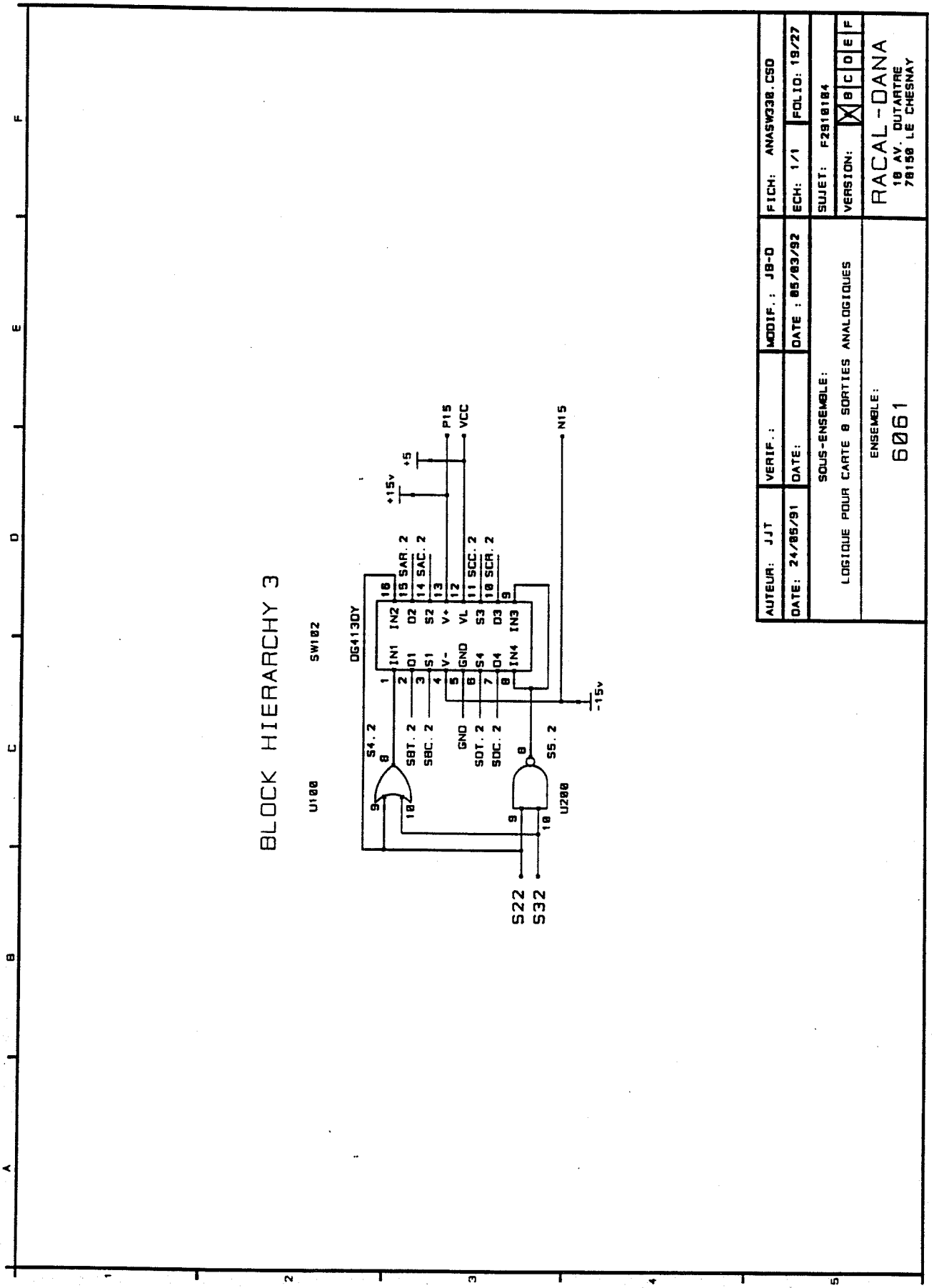


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DATE: 24/05/91	DATE:	DATE : 05/03/92	ECH: 1/1 — FOLIO: 17/27
SOUS-ENSEMBLE: LOGIQUE POUR CARTE 8 SORTIES ANALOGIQUES			SUJET: F2910104
			VERSION: [X] B C D E F
ENSEMBLE: 6061			RACAL-DANA 18 AV. DUTARTRE 78150 LE CHESNAY

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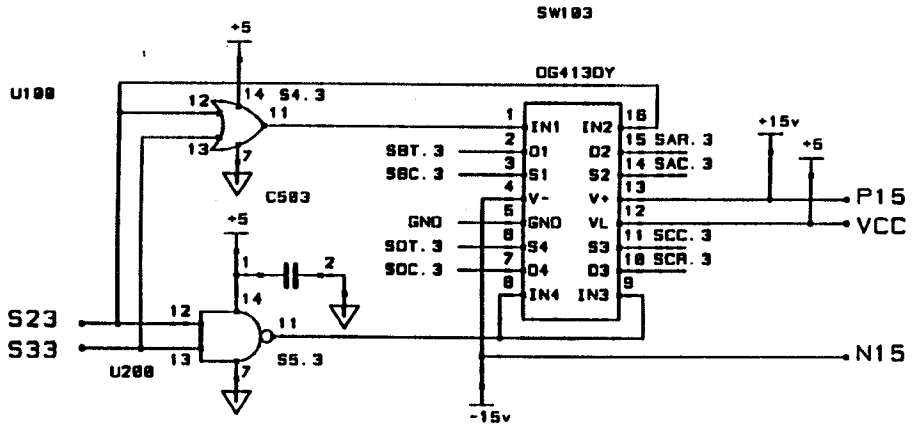
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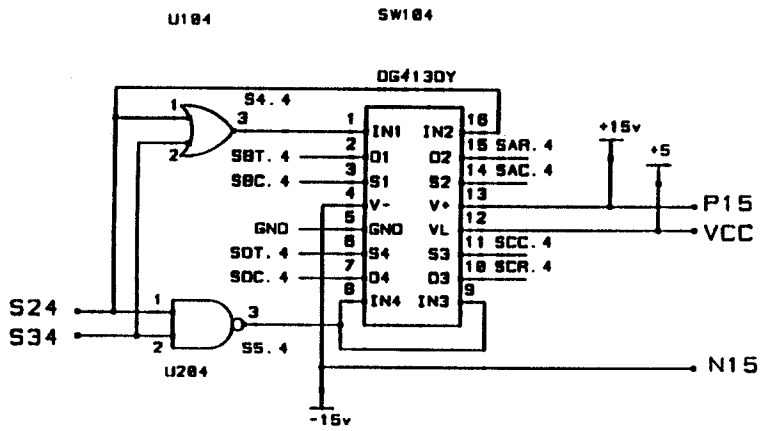
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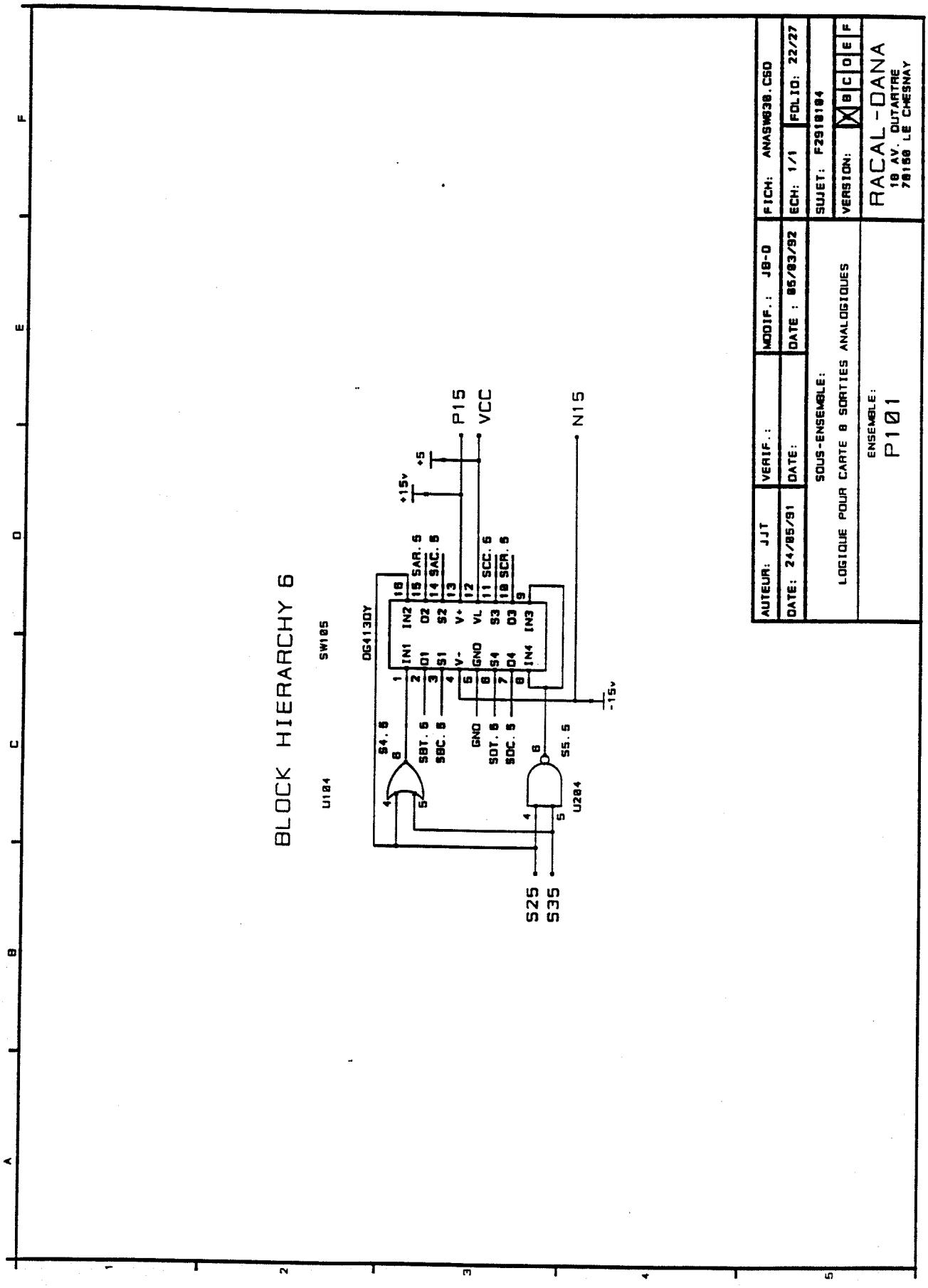
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DATE: 24/05/91	DATE:	DATE : 05/03/92	ECH: 1/1	FOLIO: 26/27
SOUS-ENSEMBLE: LOGIQUE POUR CARTE 8 SORTIES ANALOGIQUES			SUJET: F2918104	
			VERSION: X B C D E F	
ENSEMBLE: 6061			RACAL-DANA 10 AV. DUTARTRE 78150 LE CHESNAY	

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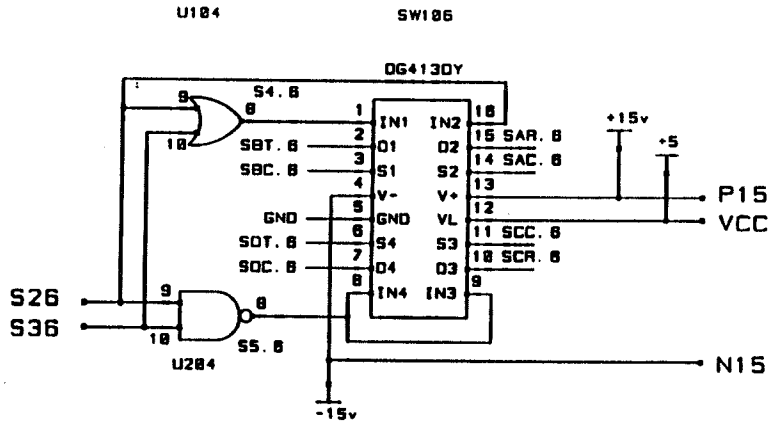
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DATE: 24/05/91	DATE:	DATE : 05/03/92	ECH: 1/1 FOLIO: 21/27
SOUS-ENSEMBLE: LOGIQUE POUR CARTE 8 SORTIES ANALOGIQUES			SUJET: F2910184
			VERSION: X B C D E F
ENSEMBLE: 6061			RACAL-DANA 10 AV. DUTARTRE 78150 LE CHESNAY



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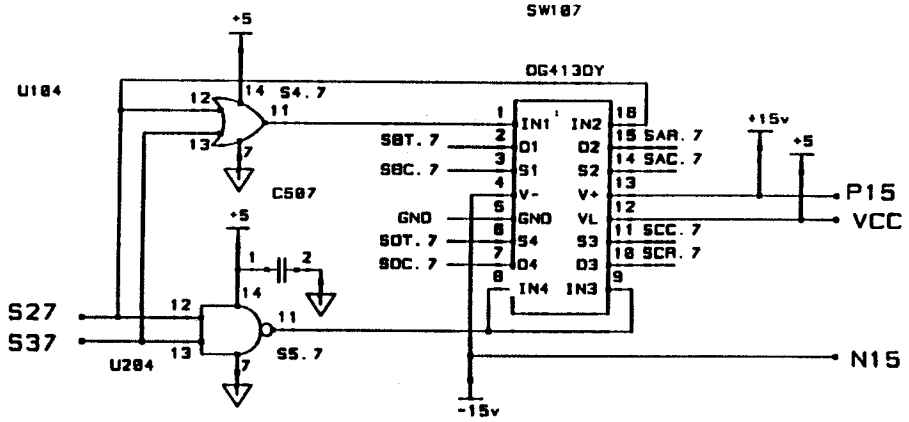


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DATE: 24/05/91	DATE:	DATE : 05/03/92	ECH: 1/1 FOLIO: 23/27
SOUS-ENSEMBLE: LOGIQUE POUR CARTE 8 SORTIES ANALOGIQUES			SUJET: F2918184
			VERSION: X B C D E F
ENSEMBLE: 6061			RACAL-DANA 10 AV. QUTARTRE 78150 LE CHESNAY

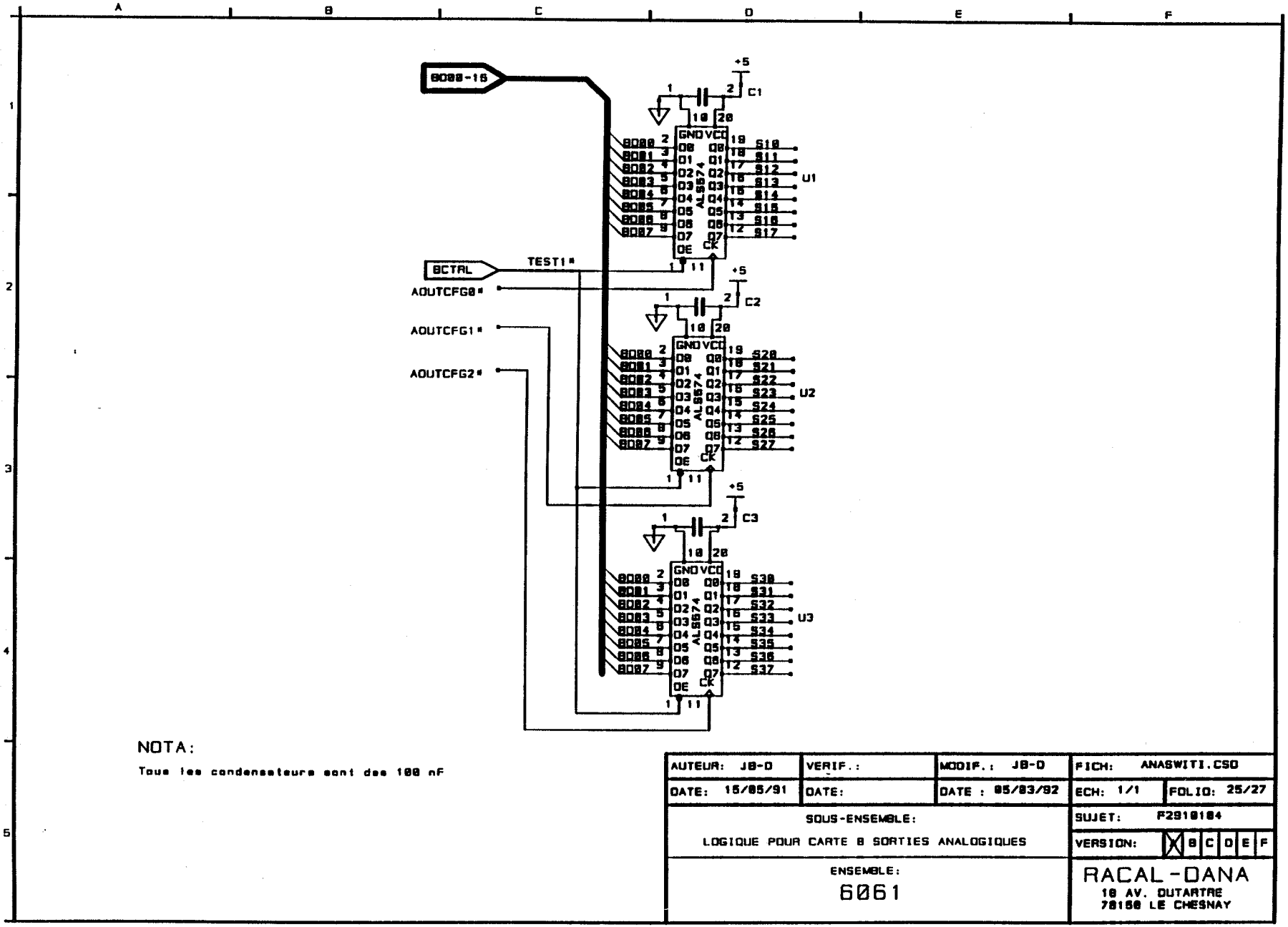
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8-5-25

BLOCK HIERARCHY 8



AUTEUR: JJT	VERIF.:	MODIF.: JB-D	FICH: ANASW848.CSD
DATE: 24/05/91	DATE:	DATE : 05/03/92	ECH: 1/1 FOLIO: 24/27
SOUS-ENSEMBLE: LOGIQUE POUR CARTE 8 SORTIES ANALOGIQUES			SUJET: F2918104
			VERSION: X B C D E F
ENSEMBLE: 6061			RACAL-DANA 10 AV. DUTARTRE 78150 LE CHESNAY

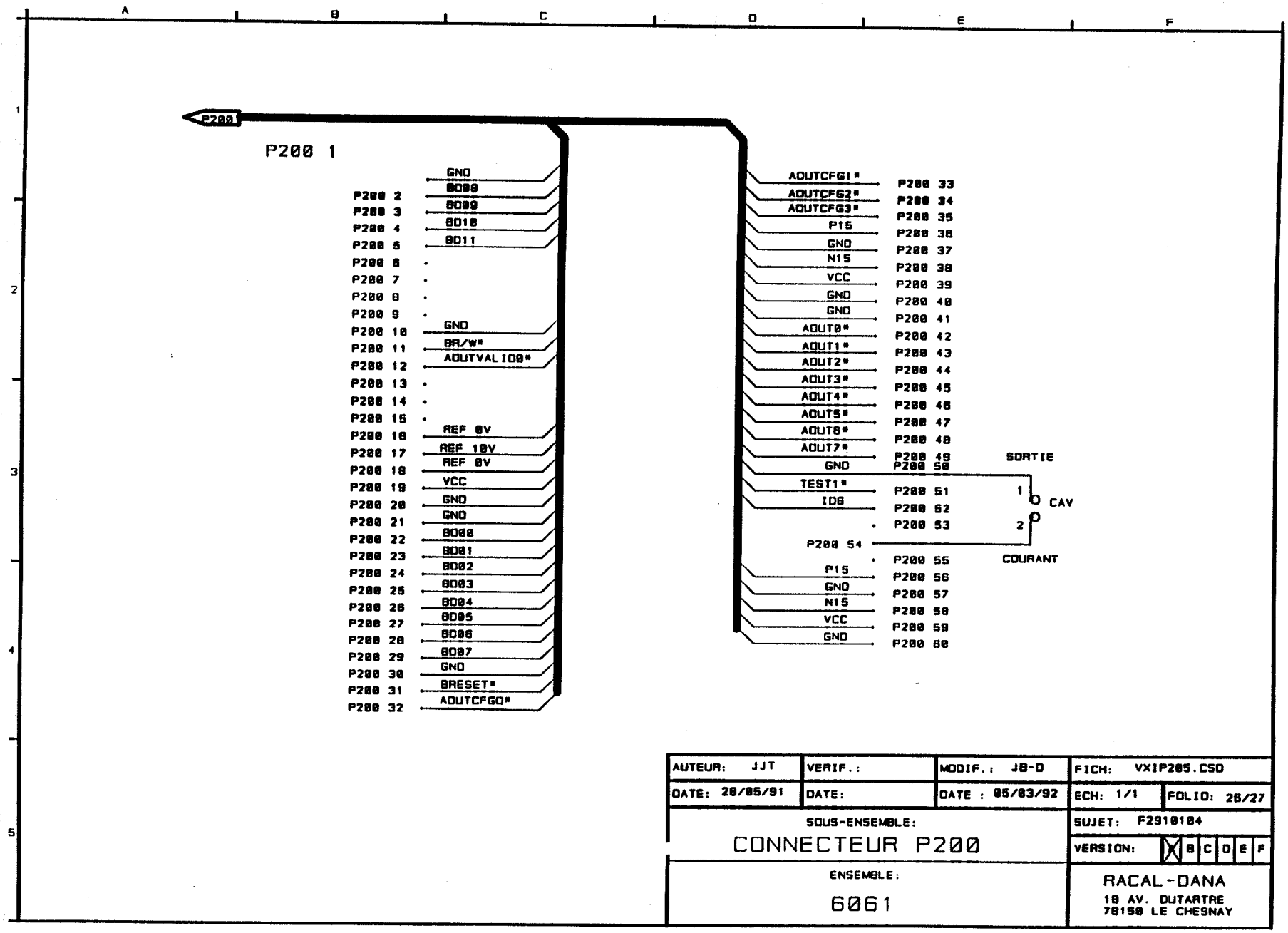


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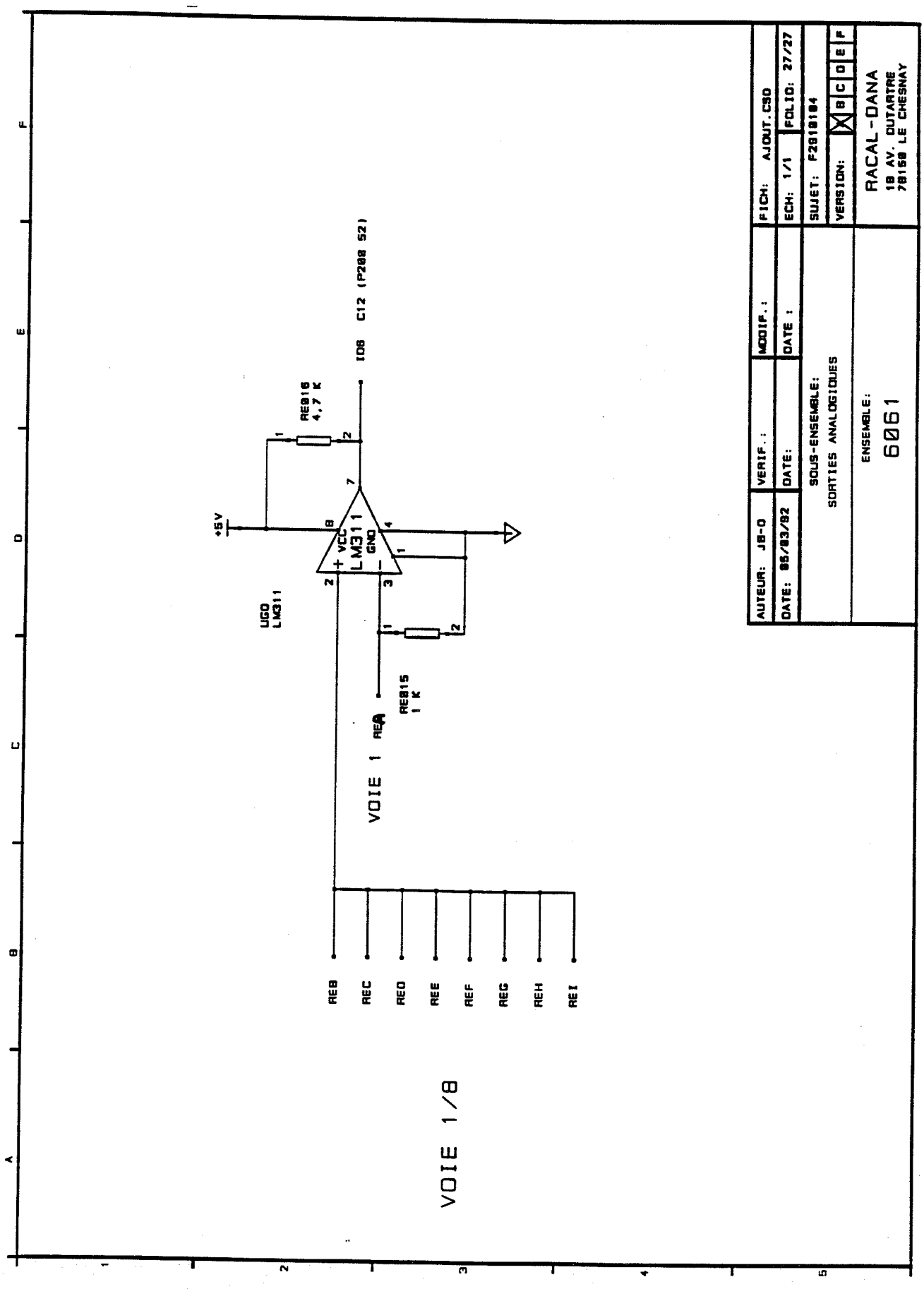
Tous les condensateurs sont des 100 nF

AUTEUR: JB-D	VERIF.:	MODIF.: JB-D	FICH: ANASWITI.CSD
DATE: 15/05/91	DATE:	DATE : 05/03/92	ECH: 1/1 FOLIO: 25/27
SOUS-ENSEMBLE: LOGIQUE POUR CARTE 8 SORTIES ANALOGIQUES			SUJET: F2910184
			VERSION: X B C D E F
ENSEMBLE: 6061			RACAL-DANA 10 AV. DUTARTRE 78150 LE CHESNAY

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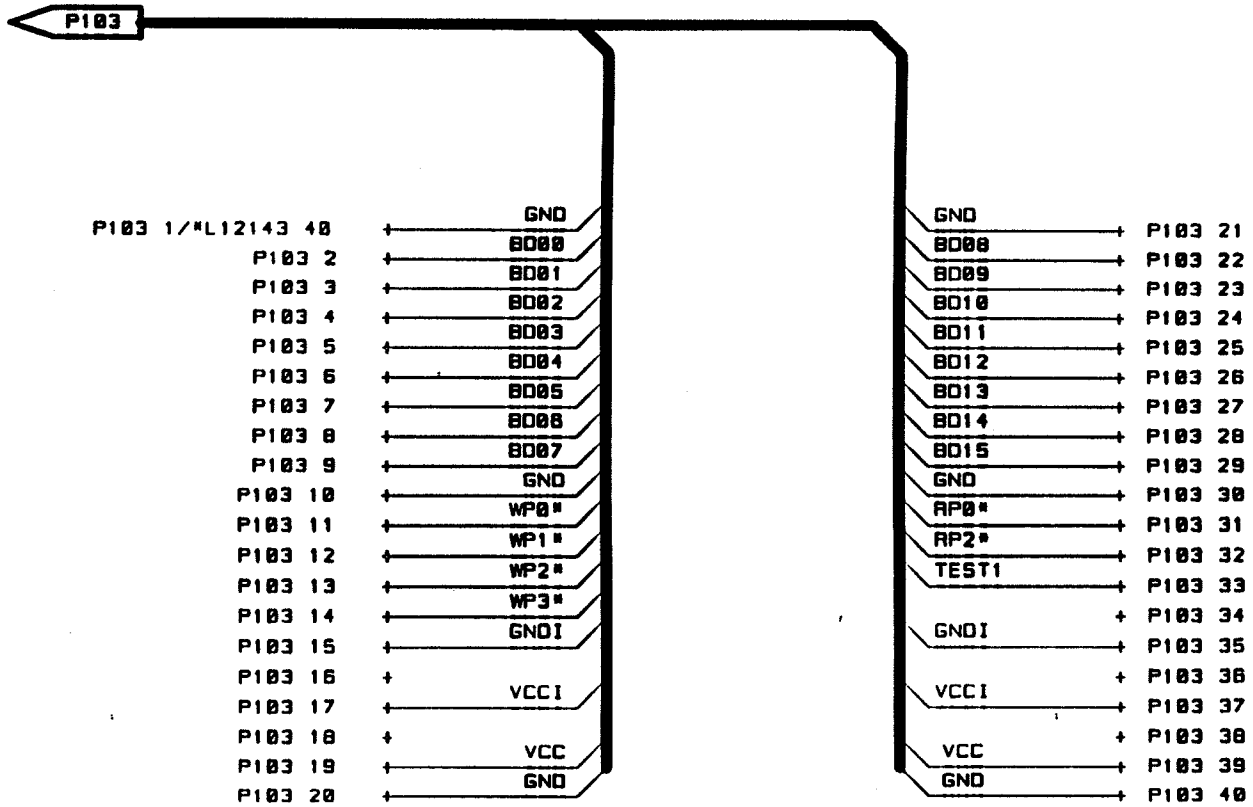
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SECTION 8-6

F2910102

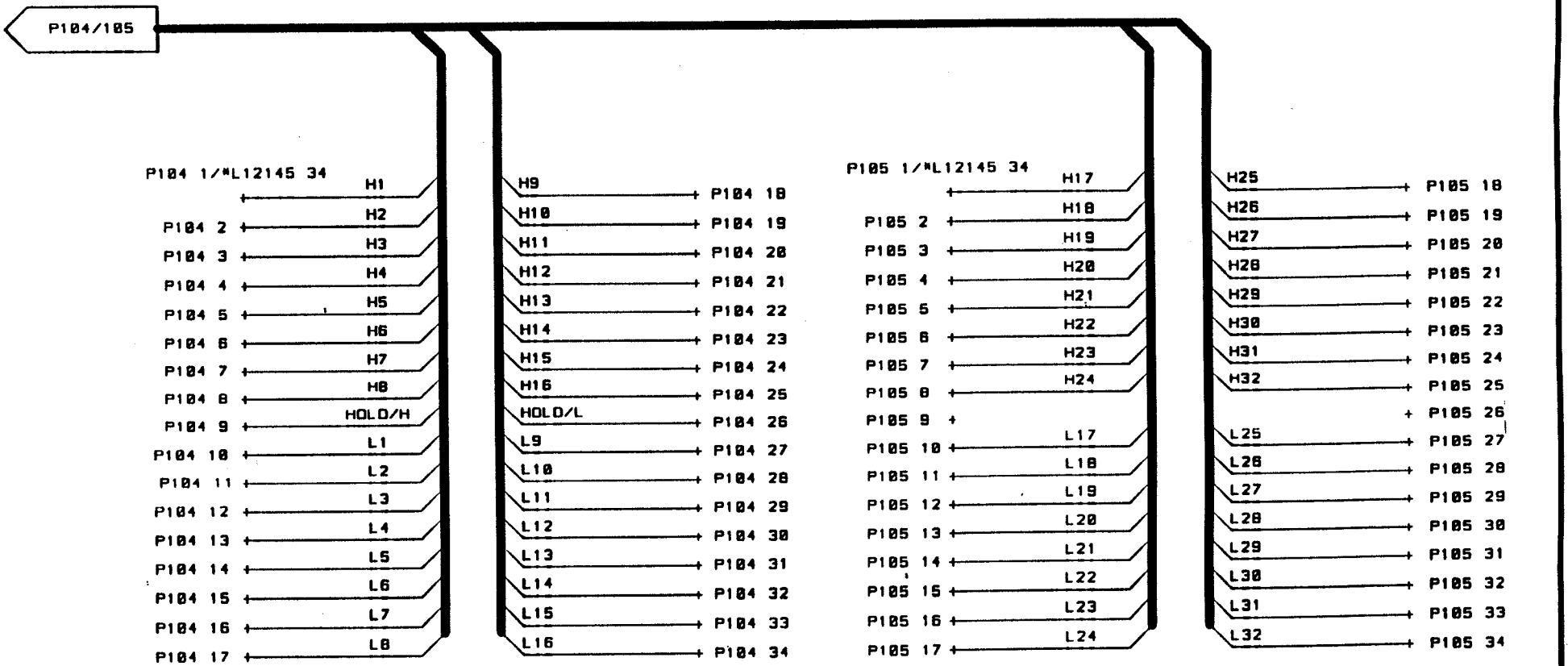
SCHEMATICS
of the
DIGITAL
INPUTS / OUTPUTS
BOARD

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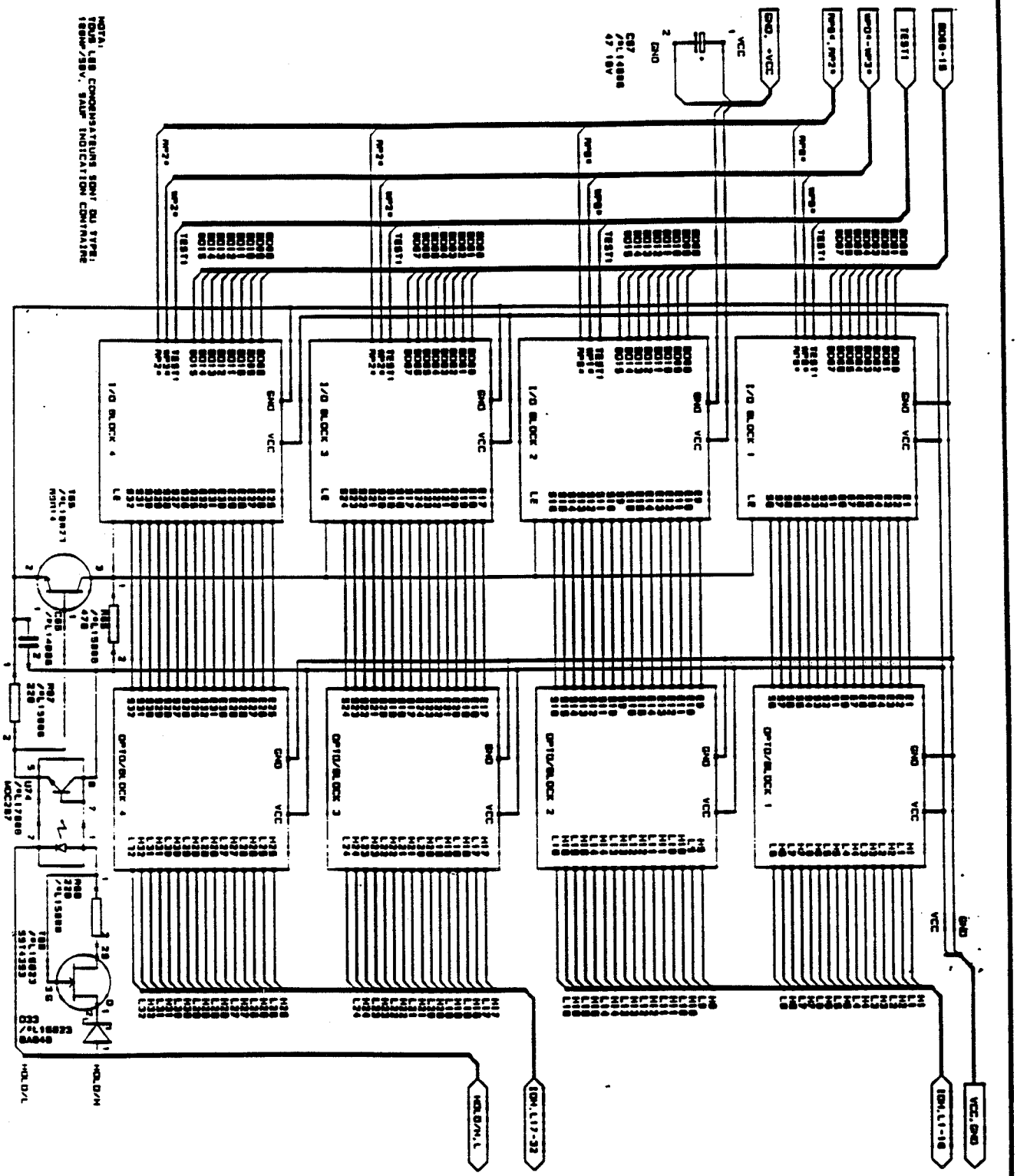
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DATE: 12/02/92	DATE: 13/02/92							FOLIO: 42/43
AUTEUR: JB-D	FICH: P103.SDX	X	B	C	D		ENSEMBLE: 6861	RACAL-SYSTEMS 18 AV. DUTARTRE 78150 LE CHESNAY
DATE: 15/02/91	ECH: 1/1	E	F	G	H			

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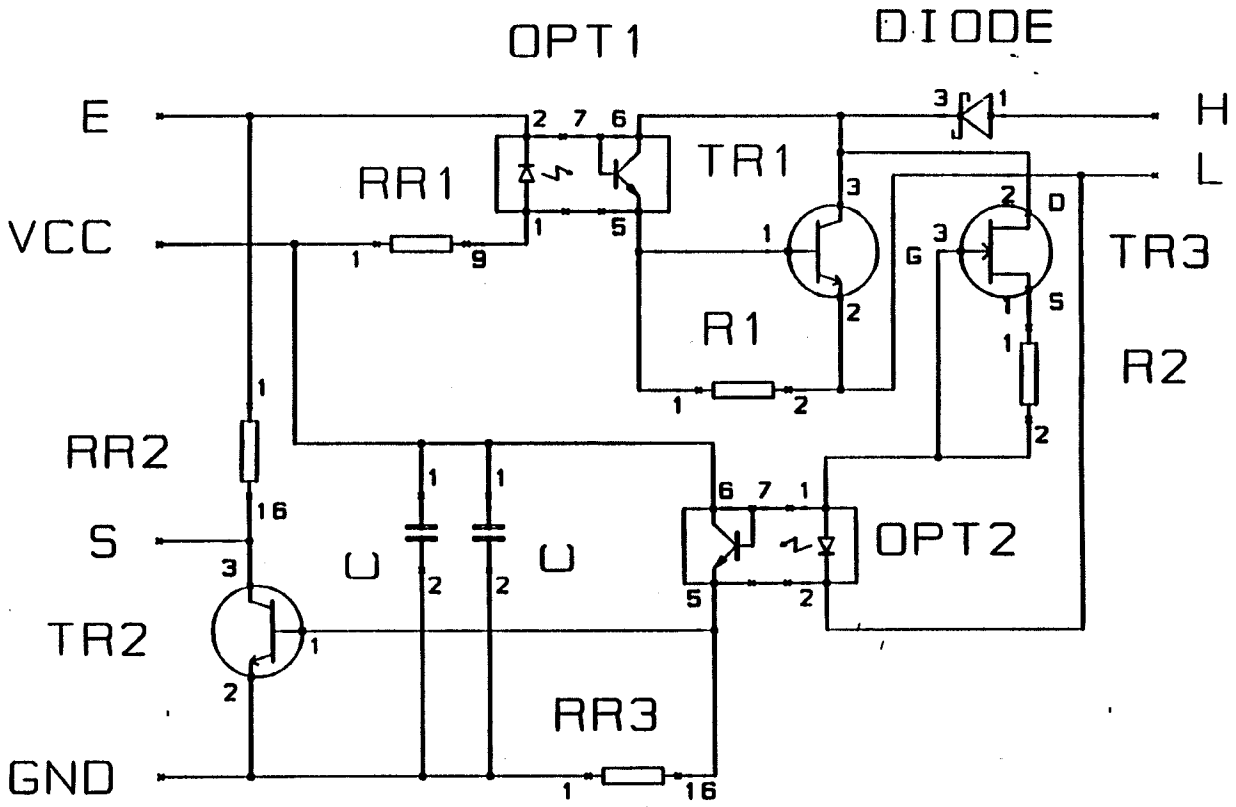
VERIF: FC	MODIF: JJT	VERSION:				SOUS-ENSEMBLE: DIGITAL INPUTS/OUTPUTS	CODE: F2910102
DATE: 12/02/92	DATE: 13/02/92						FOLIO: 43/43
AUTEUR: JB-D	FICH:P104/05.SDX	X	B	C	D	ENSEMBLE: 6061	RACAL-SYSTEMS 18 AV. DUTARTRE 78150 LE CHESNAY
DATE: 28/02/91	ECH: 1/1	E	F	G	H		

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VERIF: FC	MODIF: JJT	VERSION:					SOUS-ENSEMBLE: DIGITAL INPUTS/OUTPUTS	CODE: F2918182
DATE: 2/02/82	DATE: 11/02/82							FOLIO: 1/43
AUTEUR: FC	FICH: DIO.SOX	X	B	C	D		ENSEMBLE: 8881	RACAL-SYSTEMS 18 AV. OUTARTRE 78180 LE CHESNAY
DATE: 15/02/81	ECH: 1/1	E	F	G	H			

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NOTA :

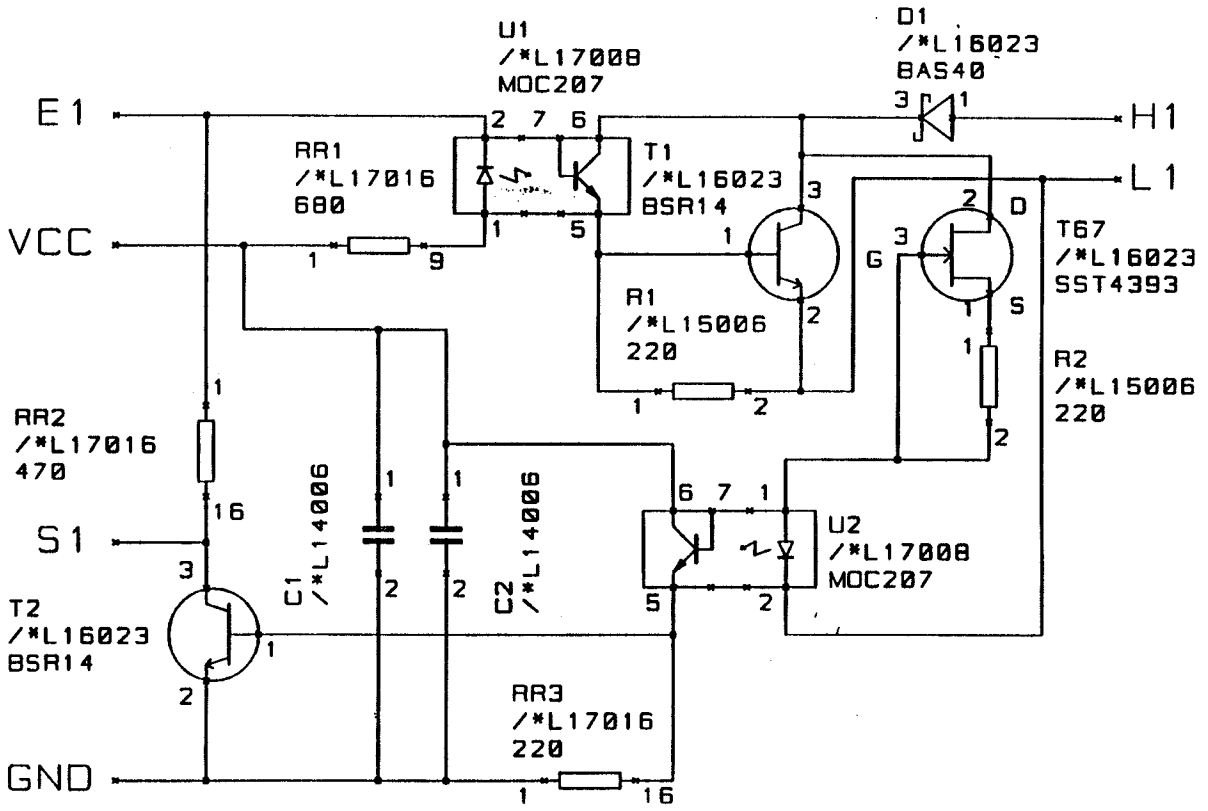
DIO.SDX

LES 32 VOIES SONT IDENTIQUES

(EX: PAGE 1)

VERIF: FC	MODIF: JJT	VERSION:				SOUS-ENSEMBLE: DIGITAL INPUTS/OUTPUTS	CODE: F2918102
DATE: 18/02/92	DATE: 18/02/92						FOLIO: 8/43
AUTEUR: JJT	FICH: EXEMPLE.CSD	X	B	C	D	ENSEMBLE: 6981	RACAL-SYSTEMS 18 AV. DUTARTRE 78150 LE CHESNAY
DATE: 18/02/92	ECH: 1/1	E	F	G	H		

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NOTA : DIO.SOX
OPTO/BLOCK1
OP81.CSO
OL1.CSO

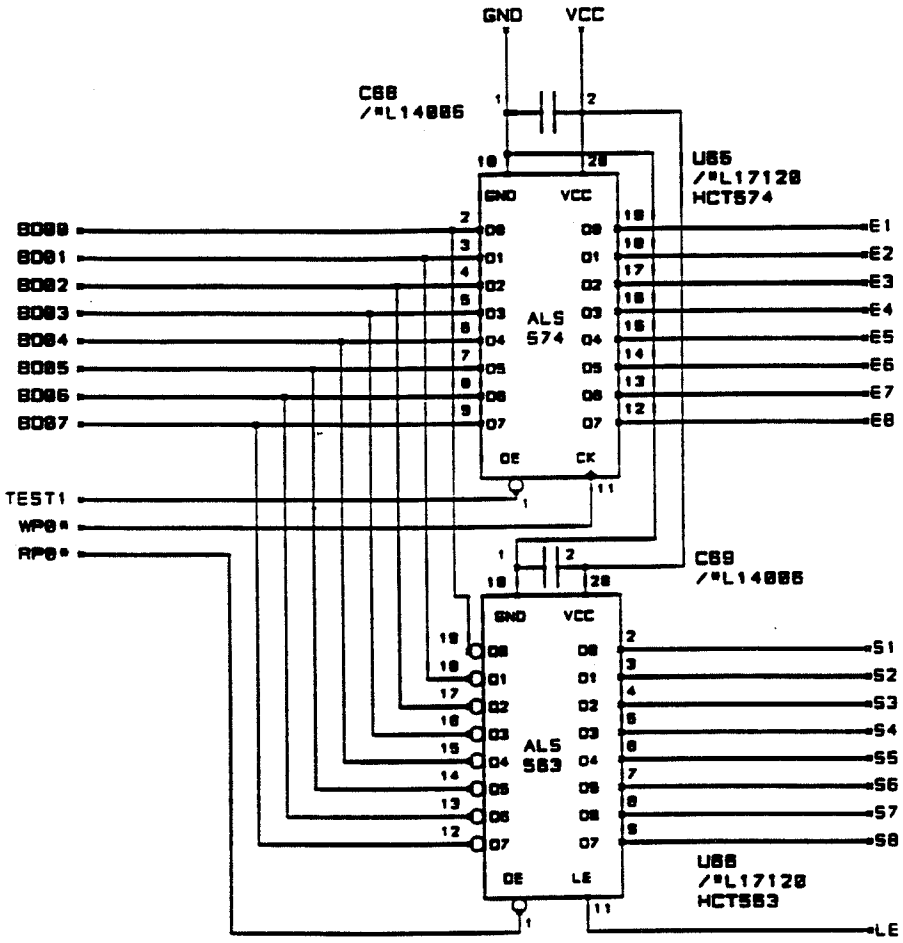
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DATE: 12/02/92	DATE: 11/02/92						FOLIO: 7/43
AUTEUR: FC	FICH: OL1.CSO	A	B	C	D	ENSEMBLE: 6061	RACAL-SYSTEMS 18 AV. DUTARTRE 78150 LE CHESNAY
DATE: 15/02/91	ECH: 1/1	E	F	G	H		

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6061: DIGITAL INPUTS / OUTPUTS

CHANNEL	OPT1 MOC207	OPT2 MOC207	DIODE BAS40	TR1 BSR14	TR2 BSR14	TR3 SST4393	RR1 680Ω	RR2 470Ω	RR3 220Ω	C 100nF	R1 220Ω	R2 220Ω	INPUT	OUTPUT	HIGH	LOW	VCC	GND
1	U1	U2	D1	T1	T2	T67	RR1	RR2	RR3	C1,C2	R1	R2	E1	S1	H1	L1	Vcc	GND
2	U3	U4	D2	T3	T4	T68	RR1	RR2	RR3	C4	R3	R4	E2	S2	H2	L2	Vcc	GND
3	U5	U6	D3	T5	T6	T69	RR1	RR2	RR3	C6	R5	R6	E3	S3	H3	L3	Vcc	GND
4	U7	U8	D4	T7	T8	T70	RR1	RR2	RR3	C8	R7	R8	E4	S4	H4	L4	Vcc	GND
5	U9	U10	D5	T9	T10	T71	RR1	RR2	RR3	C10	R9	R10	E5	S5	H5	L5	Vcc	GND
6	U11	U12	D6	T11	T12	T72	RR1	RR2	RR3	C12	R11	R12	E6	S6	H6	L6	Vcc	GND
7	U13	U14	D7	T13	T14	T73	RR1	RR2	RR3	C14	R13	R14	E7	S7	H7	L7	Vcc	GND
8	U15	U16	D8	T15	T16	T74	RR1	RR2	RR3	C16	R15	R16	E8	S8	H8	L8	Vcc	GND
9	U17	U18	D9	T17	T18	T75	RR4	RR5	RR6	C17,C18	R17	R18	E9	S9	H9	L9	Vcc	GND
10	U19	U20	D10	T19	T20	T76	RR4	RR5	RR6	C20	R19	R20	E10	S10	H10	L10	Vcc	GND
11	U21	U22	D11	T21	T22	T77	RR4	RR5	RR6	C22	R21	R22	E11	S11	H11	L11	Vcc	GND
12	U23	U24	D12	T23	T24	T78	RR4	RR5	RR6	C24	R23	R24	E12	S12	H12	L12	Vcc	GND
13	U25	U26	D13	T25	T26	T79	RR4	RR5	RR6	C26	R25	R26	E13	S13	H13	L13	Vcc	GND
14	U27	U28	D14	T27	T28	T80	RR4	RR5	RR6	C28	R27	R28	E14	S14	H14	L14	Vcc	GND
15	U29	U30	D15	T29	T30	T81	RR4	RR5	RR6	C30	R29	R30	E15	S15	H15	L15	Vcc	GND
16	U31	U32	D16	T31	T32	T82	RR4	RR5	RR6	C32	R31	R32	E16	S16	H16	L16	Vcc	GND
17	U33	U34	D17	T33	T34	T83	RR7	RR8	RR9	C33,C34	R33	R34	E17	S17	H17	L17	Vcc	GND
18	U35	U36	D18	T35	T36	T84	RR7	RR8	RR9	C36	R35	R36	E18	S18	H18	L18	Vcc	GND
19	U37	U38	D19	T37	T38	T85	RR7	RR8	RR9	C38	R37	R38	E19	S19	H19	L19	Vcc	GND
20	U39	U40	D20	T39	T40	T86	RR7	RR8	RR9	C40	R39	R40	E20	S20	H20	L20	Vcc	GND
21	U41	U42	D21	T41	T42	T87	RR7	RR8	RR9	C42	R41	R42	E21	S21	H21	L21	Vcc	GND
22	U43	U44	D22	T43	T44	T88	RR7	RR8	RR9	C44	R43	R44	E22	S22	H22	L22	Vcc	GND
23	U45	U46	D23	T45	T46	T89	RR7	RR8	RR9	C46	R45	R46	E23	S23	H23	L23	Vcc	GND
24	U47	U48	D24	T47	T48	T90	RR7	RR8	RR9	C48	R47	R48	E24	S24	H24	L24	Vcc	GND
25	U49	U50	D25	T49	T50	T91	RR10	RR11	RR12	C49,C50	R49	R50	E25	S25	H25	L25	Vcc	GND
26	U51	U52	D26	T51	T52	T92	RR10	RR11	RR12	C52	R51	R52	E26	S26	H26	L26	Vcc	GND
27	U53	U54	D27	T53	T54	T93	RR10	RR11	RR12	C54	R53	R54	E27	S27	H27	L27	Vcc	GND
28	U55	U56	D28	T55	T56	T94	RR10	RR11	RR12	C56	R55	R56	E28	S28	H28	L28	Vcc	GND
29	U57	U58	D29	T57	T58	T95	RR10	RR11	RR12	C58	R57	R58	E29	S29	H29	L29	Vcc	GND
30	U59	U60	D30	T59	T60	T96	RR10	RR11	RR12	C60	R59	R60	E30	S30	H30	L30	Vcc	GND
31	U61	U62	D31	T61	T62	T97	RR10	RR11	RR12	C62	R61	R62	E31	S31	H31	L31	Vcc	GND
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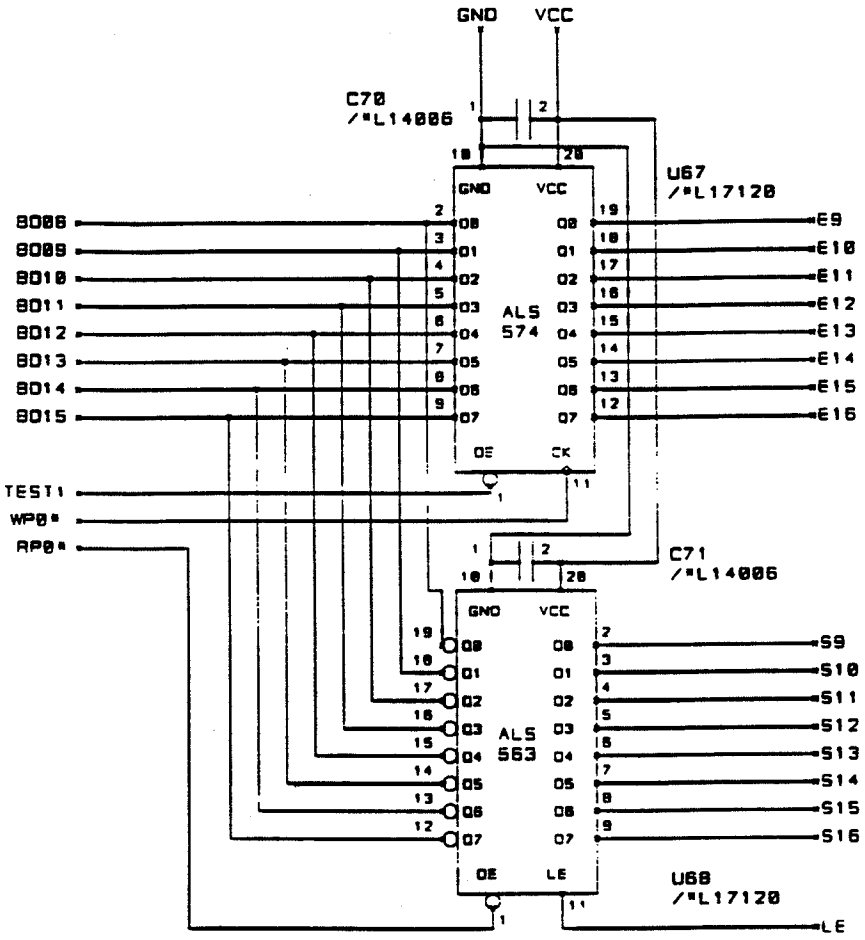
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NOTA : 010.SOX
I/O BLOCK1
081.CSD

VERIF: FC	MODIF: JJT	VERSION:				SOUS-ENSEMBLE: DIGITAL INPUTS/OUTPUTS	CODE: F2910102
DATE: 12/02/92	DATE: 11/02/92						FOLIO: 2/43
AUTEUR: FC	FICH: 081.CSD	A	B	C	D	ENSEMBLE: 6661	RACAL-SYSTEMS 18 AV. OUTARTRE 78150 LE CHESNAY
DATE: 15/02/91	ECH: 1/1	E	F	G	H		

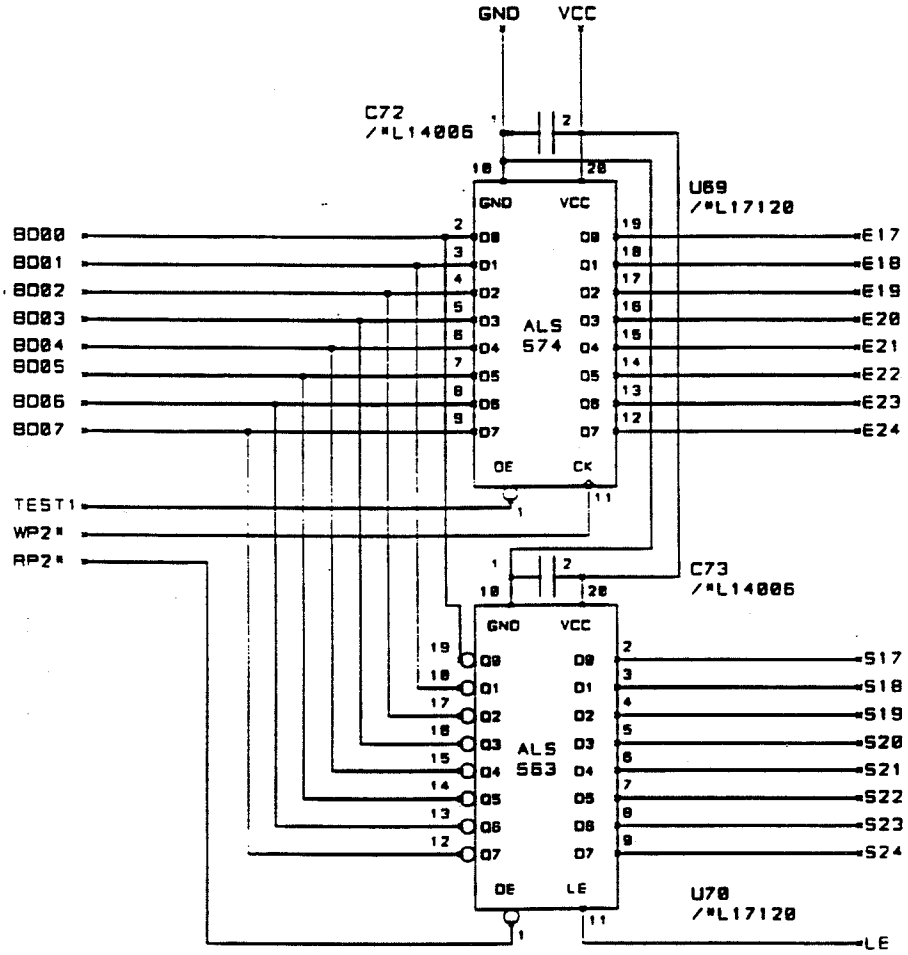
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NOTA : DIO.SOX
I/O BLOCK2
D02.CSD

VERIF: FC	MODIF: JJT	VERSION:				SOUS-ENSEMBLE: DIGITAL INPUTS/OUTPUTS	CODE: F2910102
DATE: 12/02/92	DATE: 11/02/92						FOLIO: 3/43
AUTEUR: FC	FICH: D02.CSD	A	B	C	D	ENSEMBLE: 8051	RACAL-SYSTEMS 18 AV. OUTARTRE 78150 LE CHESNAY
DATE: 15/02/91	ECH: 1/1	E	F	G	H		

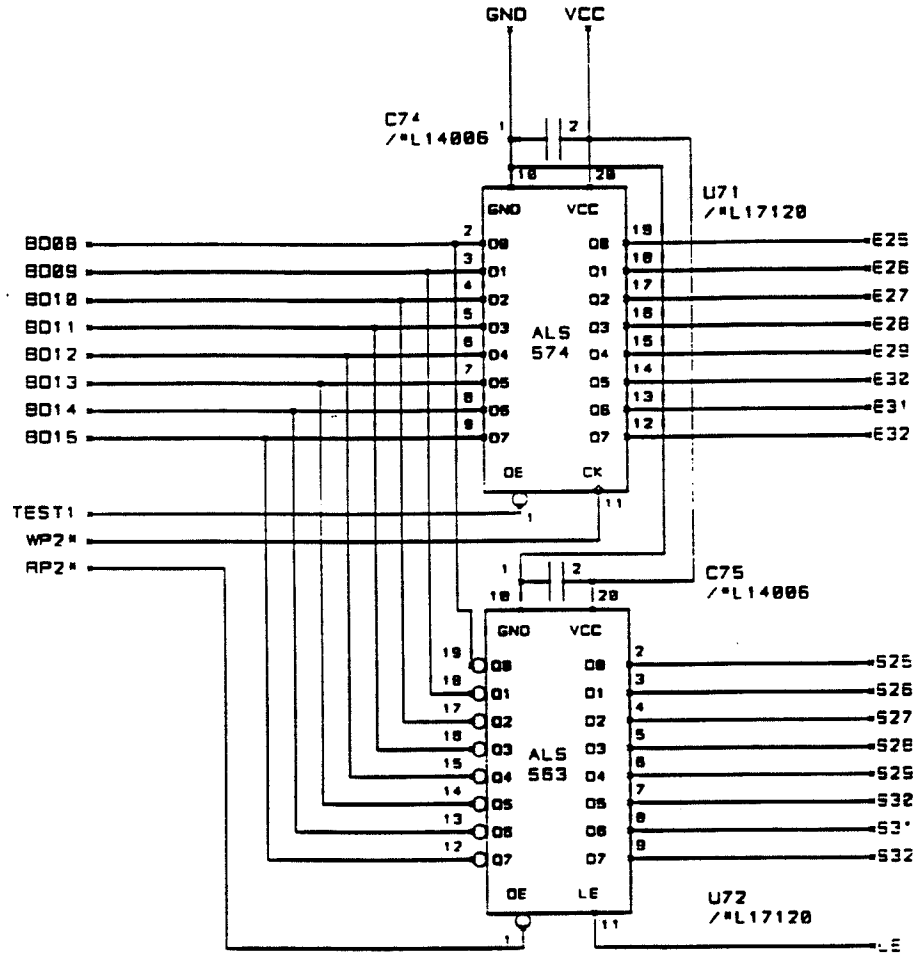
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NOTA : DIO.SOX
I/O BLOCK3
003.CSD

VERIF: FC	MODIF: JJT	VERSION:				SOUS-ENSEMBLE:	CODE: F2910102
DATE: 12/02/92	DATE. 11/02/92					DIGITAL INPUTS/OUTPUTS	FOLIO: 4/43
AUTEUR: FC	FICH: 003.CSD	X	B	C	D	ENSEMBLE:	RACAL-SYSTEMS
DATE: 15/02/91	ECH: 1/1	E	F	G	H	8861	18 AV. OUTARTRE 78150 LE CHESNAY

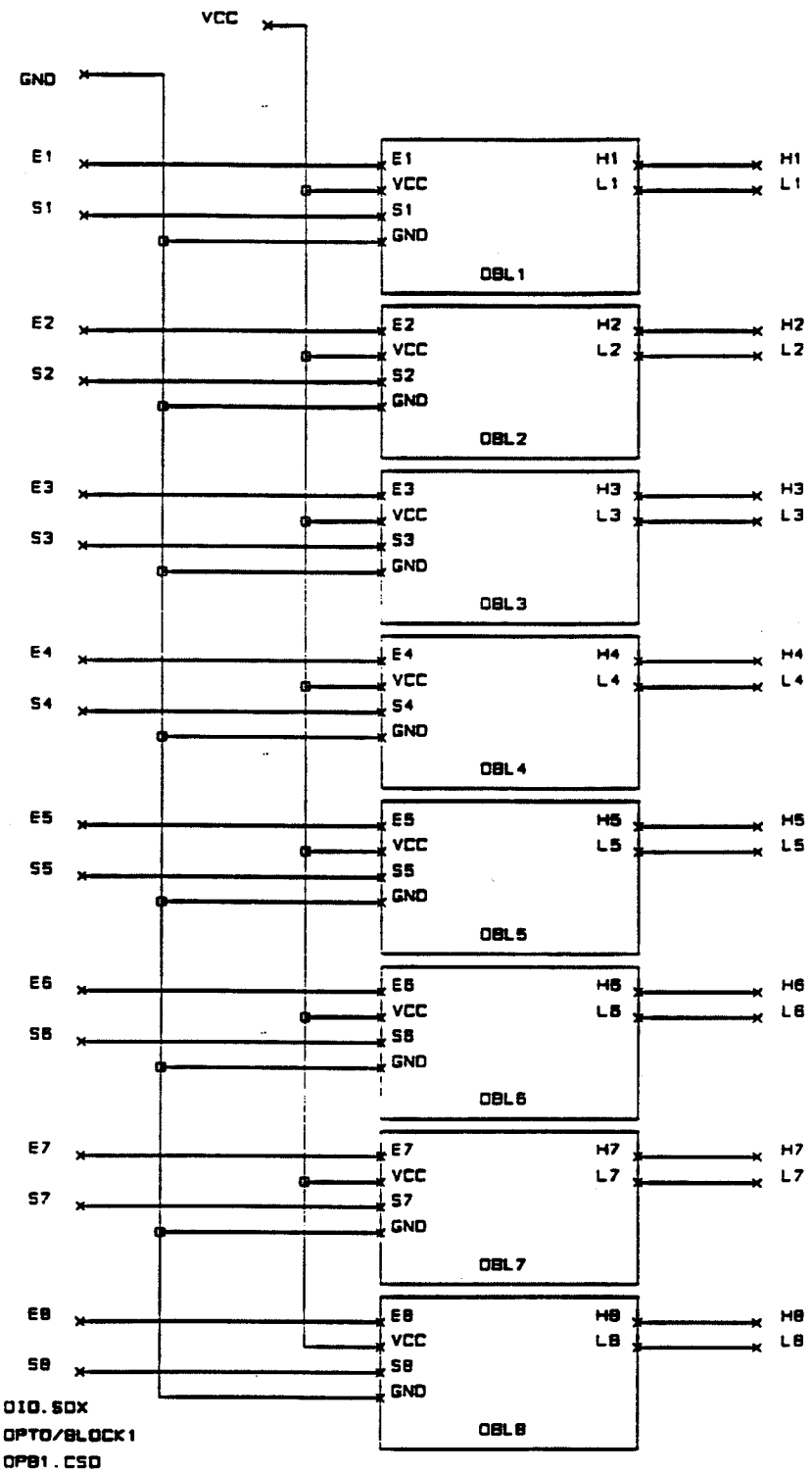
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NOTA : DIO.SOX
I/O BLOCK4
D04.CSD

VERIF: FC	MODIF: JJT	VERSION:				SOUS-ENSEMBLE:	CODE: F2910102
DATE: 12/02/92	DATE: 11/02/92					DIGITAL INPUTS/OUTPUTS	FOLIC. 5/43
AUTEUR: FC	FICH: D04.CSD	A	B	C	D	ENSEMBLE:	RACAL-SYSTEMS
DATE: 15/02/91	ECH: 1/1	E	F	G	H	6061	18 AV. OUTARTRE 78150 LE CHESNAY

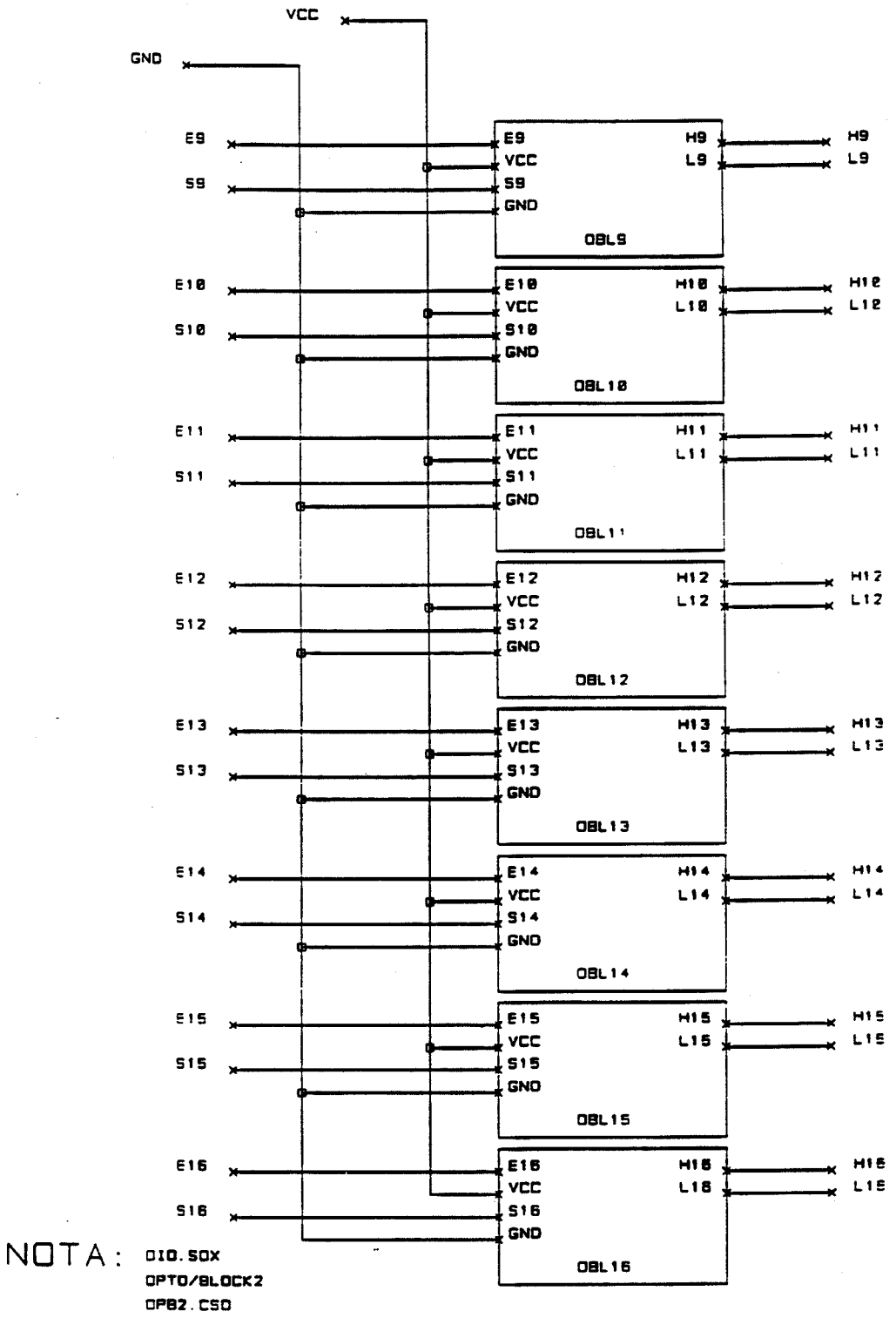
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NOTA : OIO.SOX
OPTO/BLOCK1
OPB1.CSD

VERIF: FC	MODIF: JJT	VERSION:				SOUS-ENSEMBLE:	CODE: F2910102
DATE: 12/02/92	DATE: 11/02/92					DIGITAL INPUTS/OUTPUTS	FOLIO: 6/43
AUTEUR: FC	FICH: OPB1.CSD	A	B	C	D	ENSEMBLE:	RACAL-SYSTEMS
DATE: 15/02/91	ECH: 1/1	E	F	G	H	6881	18 AV. OUTARTRE 78150 LE CHESNAY

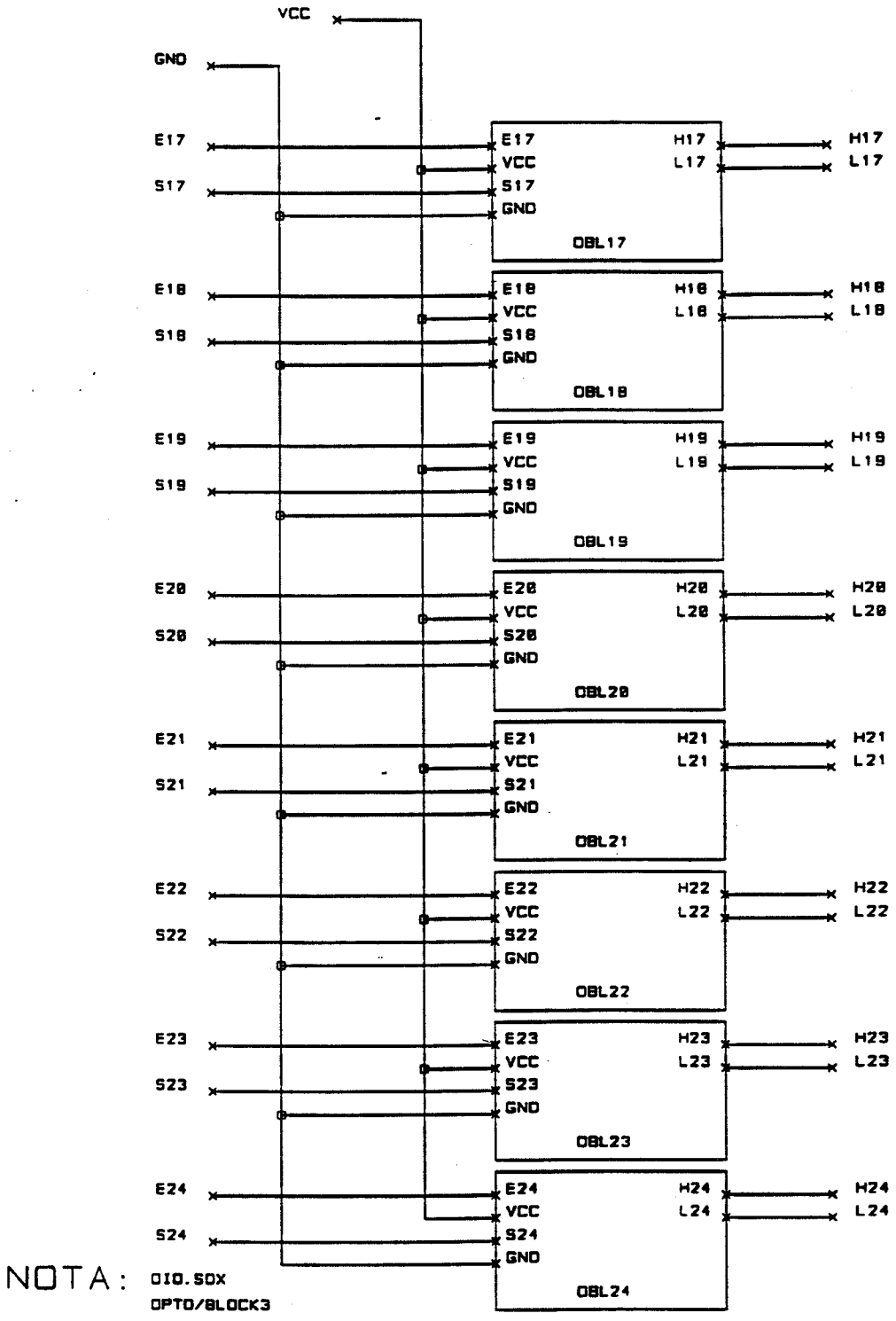
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NOTA : DIO.SOX
OPTO/BLOCK2
OPB2.CSO

VERIF: FC	MODIF: JJT	VERSION:				SOUS-ENSEMBLE:	CODE: F2910102
DATE: 12/02/92	DATE: 11/02/92					DIGITAL INPUTS/OUTPUTS	FOLIC 15/43
AUTEUR: FC	FICH: OPB2.CSO	A	B	C	D	ENSEMBLE:	RACAL-SYSTEMS
DATE: 15/02/91	ECH: 1/1	E	F	G	H	6881	18 AV. OUTARTRE 78150 LE CHESNAY

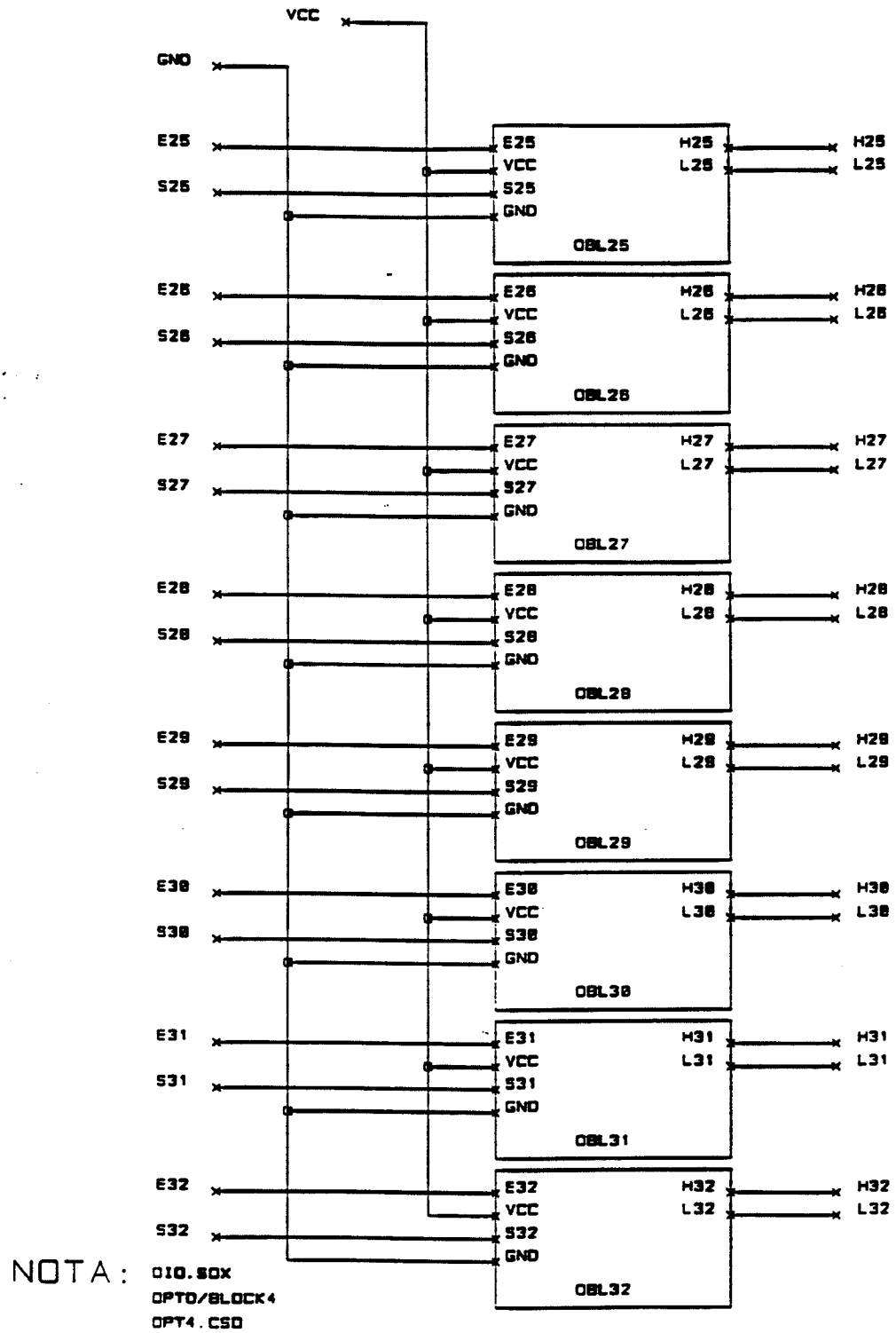
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NOTA : DIO.SOX
OPTO/BLOCK3
OP83.CSD

VERIF.: FC	MODIF: JJT	VERSION:				SOUS-ENSEMBLE:	CODE: F2910102
DATE: 12/02/92	DATE: 11/02/92					DIGITAL INPUTS/OUTPUTS	FOLIO: 24/43
AUTEUR: FC	FICH: OP83.CSD	A	B	C	D	ENSEMBLE:	RACAL-SYSTEMS
DATE: 15/02/91	ECH: 1/1	E	F	G	H	6881	18 AV. DUTARTRE 78150 LE CHESNAY

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NOTA : DIO.SOX
OPTO/BLOCK4
OPT4.CSD

VERIF: FC	MODIF: JJT	VERSION:				SOUS-ENSEMBLE:	CODE: F2818182
DATE: 12/02/92	DATE: 11/02/92					DIGITAL INPUTS/OUTPUTS	FOLIO: 33/43
AUTEUR: FC	FICH: OPT4.CSD	A	B	C	D	ENSEMBLE:	RACAL-SYSTEMS
DATE: 15/02/91	ECH: 1/1	E	F	G	H	6861	18 AV. OUTARTRE 78150 LE CHESNAY

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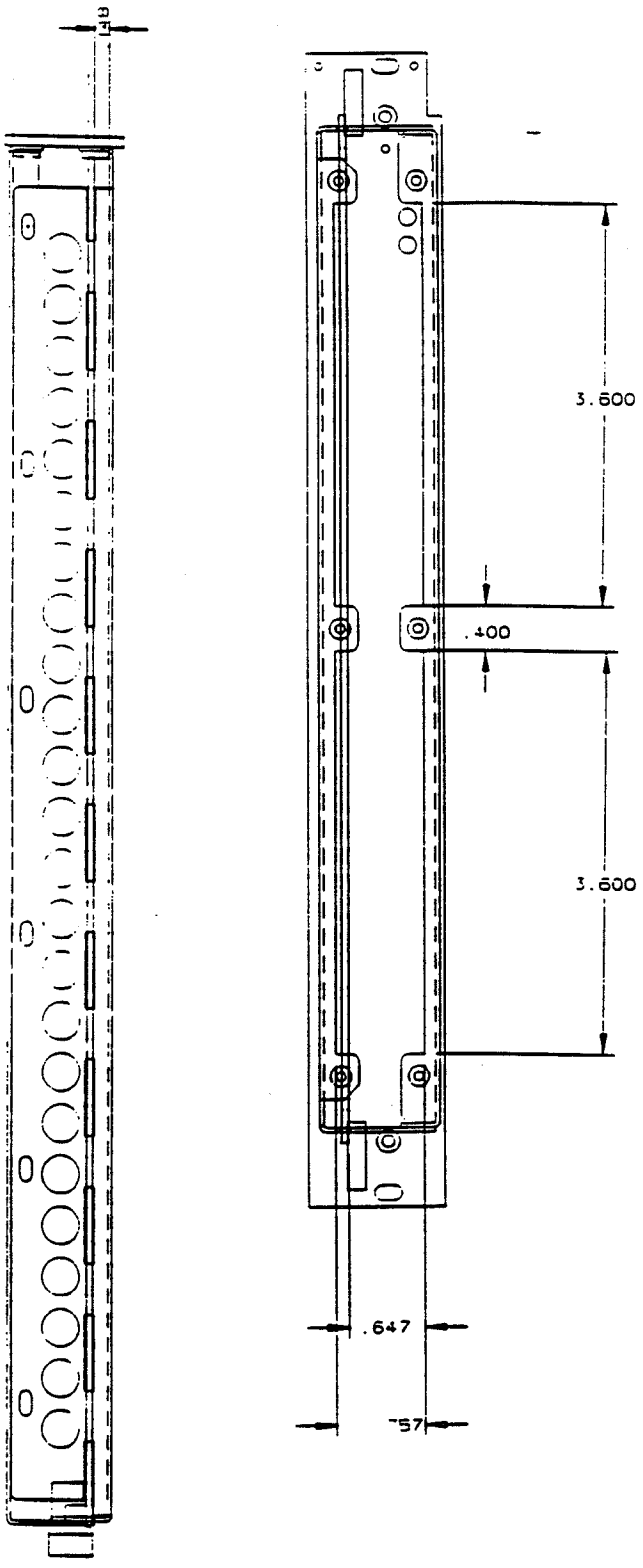
SECTION 9

DRAWINGS

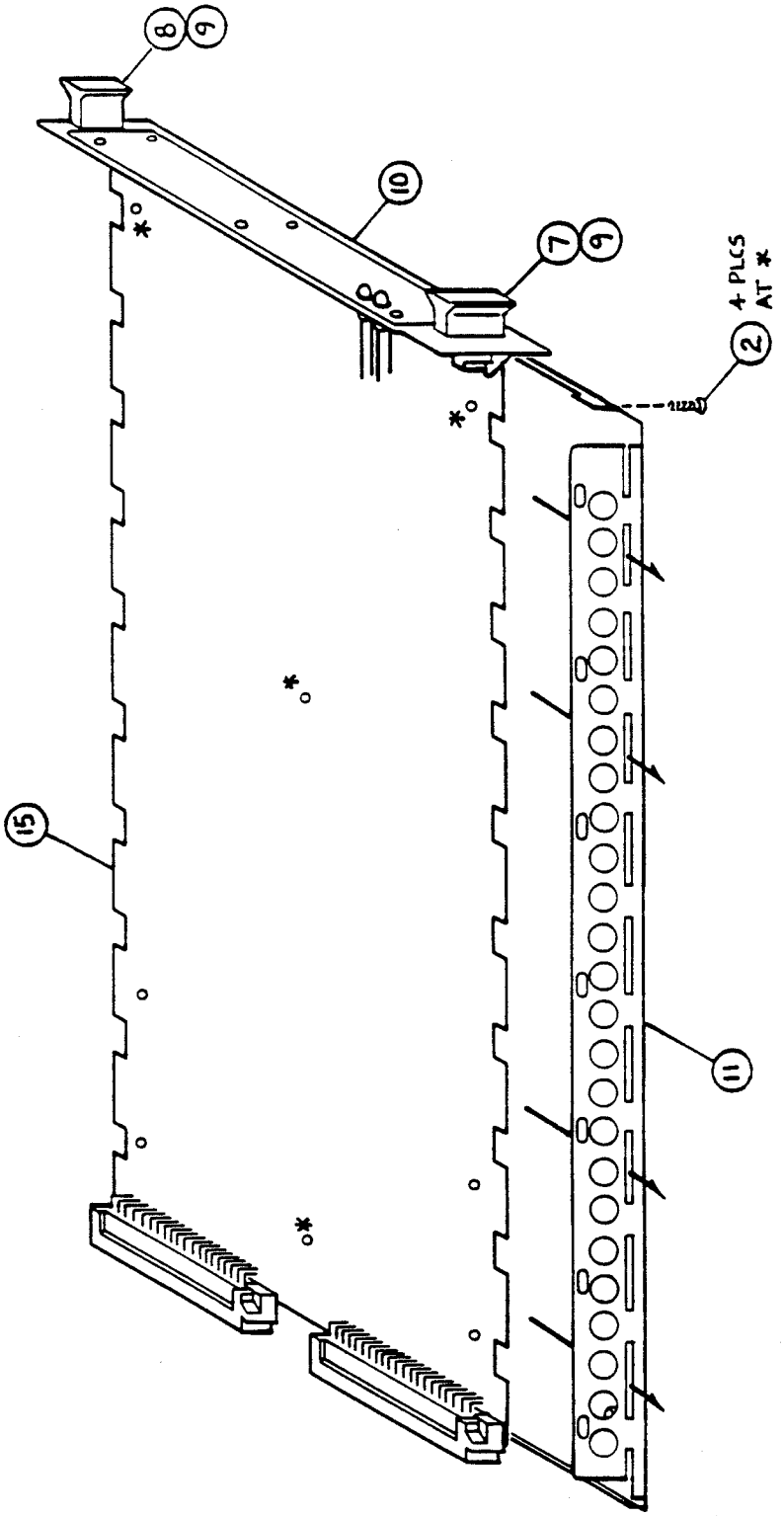
MODEL 6061

FS910107	FINAL ASSEMBLY
F4910101	PCB Assy., MOTHER Board
F4910105	PCB Assy., VXI INTERFACE Board
F4910106	PCB Assy., DC/DC CONVERTER Board
F4910104	PCB Assy., ANALOG INPUTS Board
F4910103	PCB Assy., ANALOG OUTPUTS Board
F4910102	PCB Assy., DIGITAL INPUTS/OUTPUTS Board.

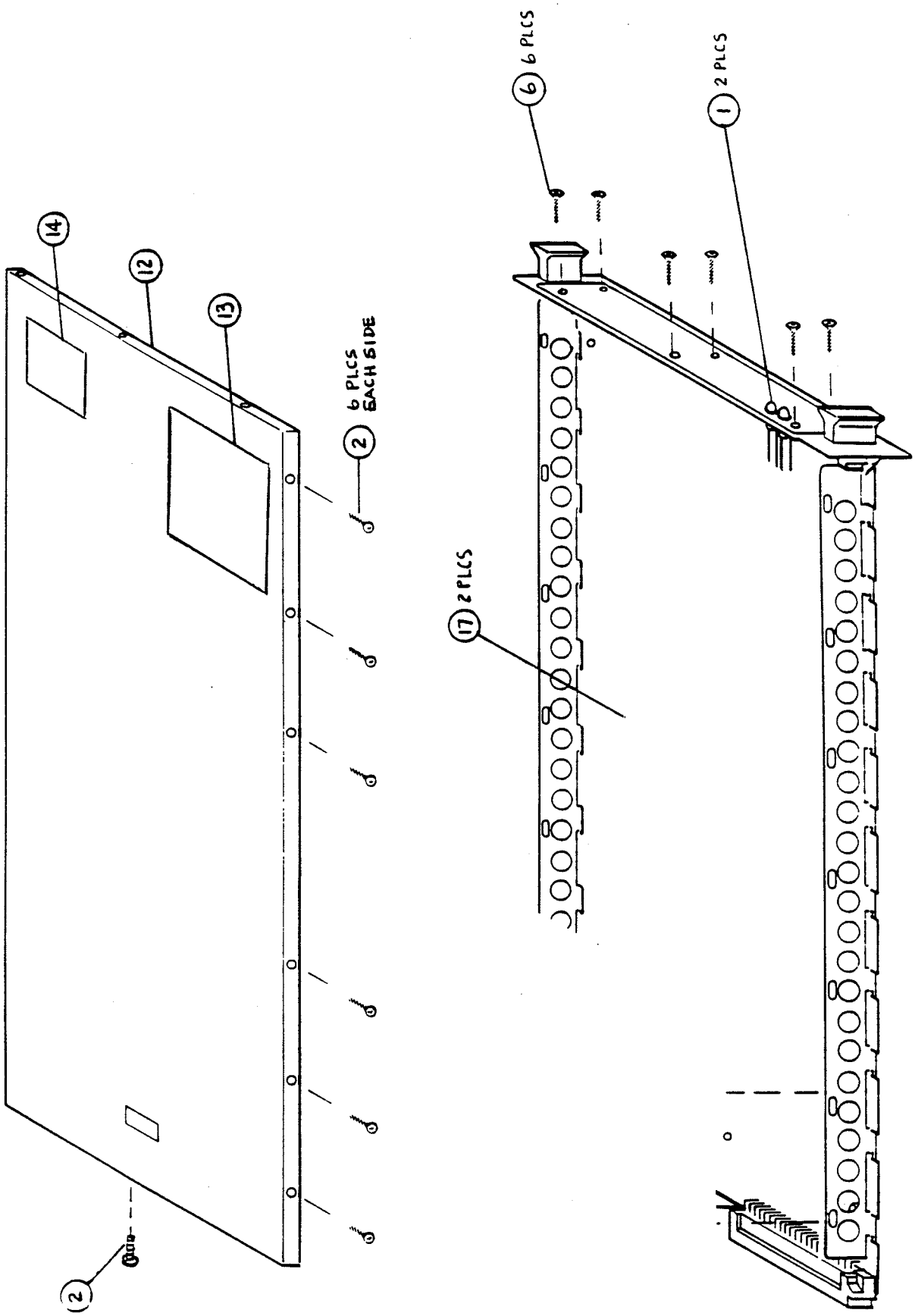
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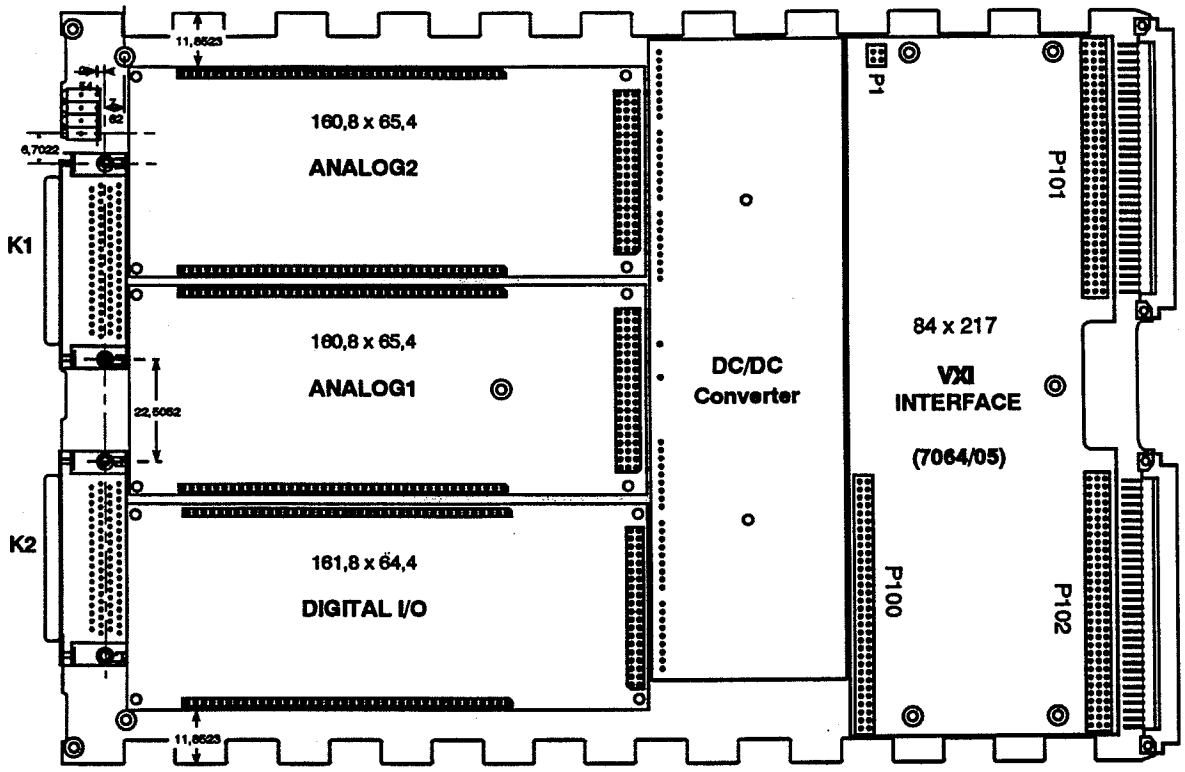


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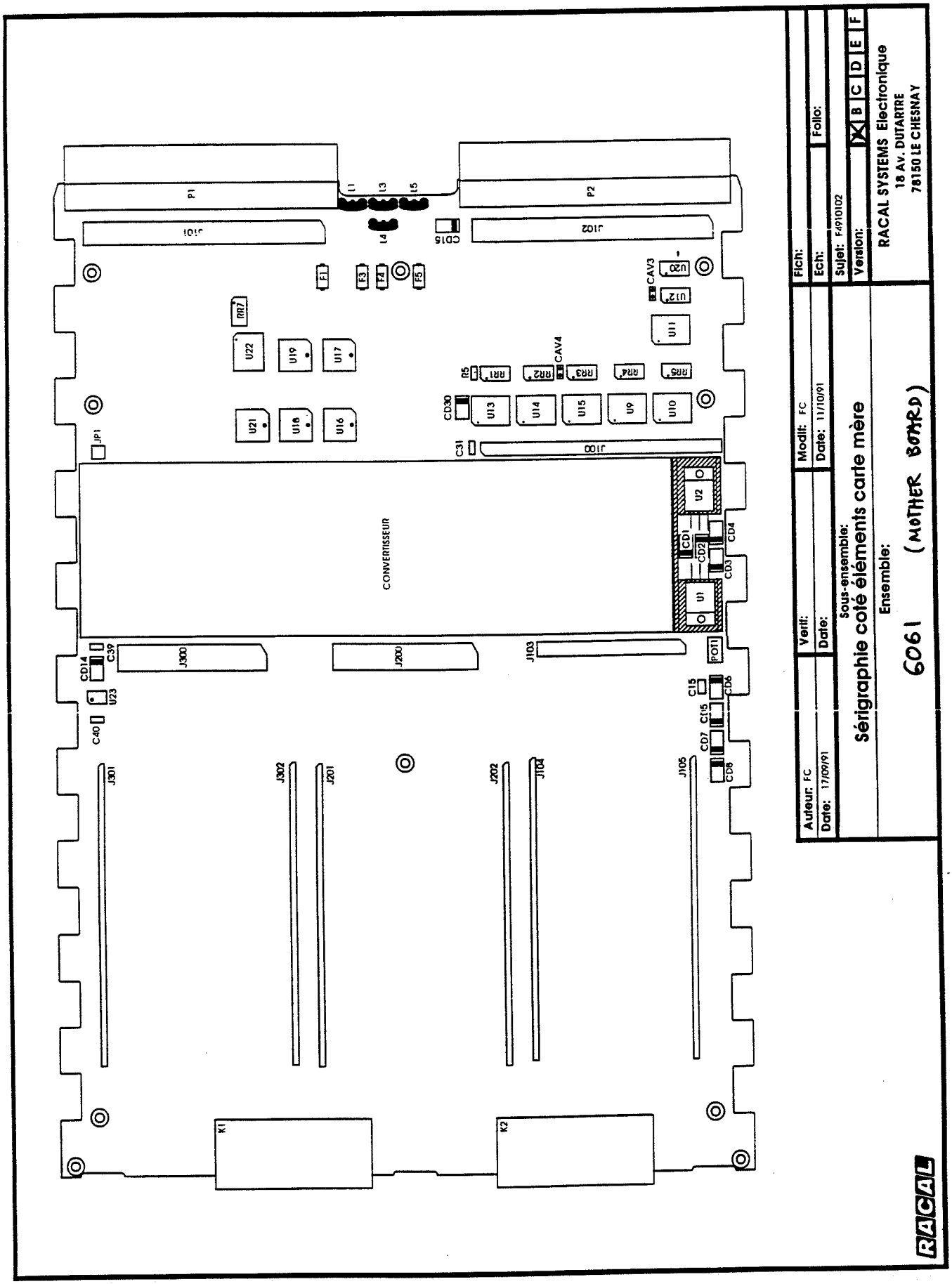
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PCB-Mother Board ASSY

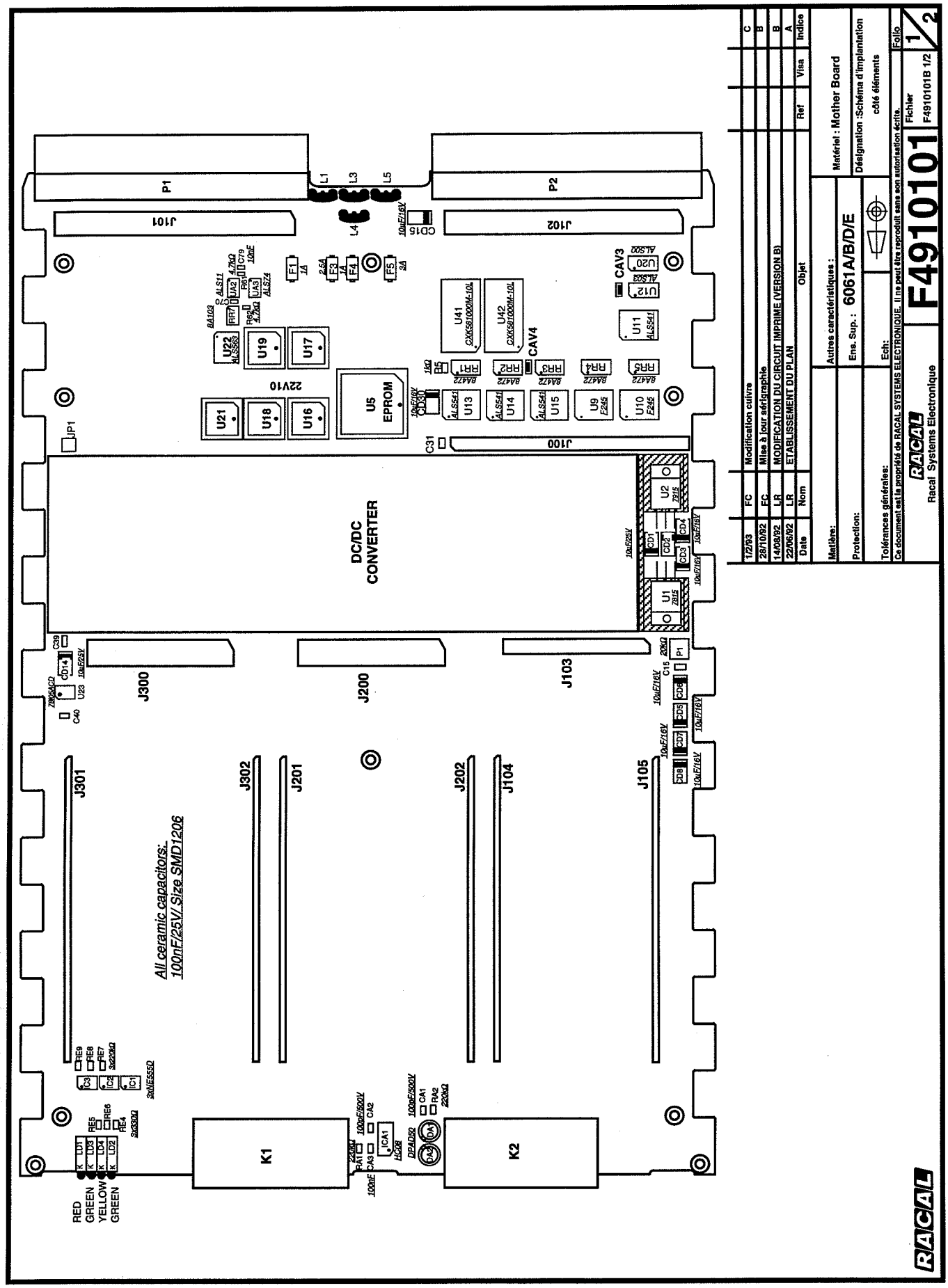


VERSION	ANALOG1	ANALOG2
6061A	OUTPUT	INPUT
6061B	OUTPUT	OUTPUT
6061C	INPUT	INPUT
6061D	-	-
6061E	OUTPUT	INPUT

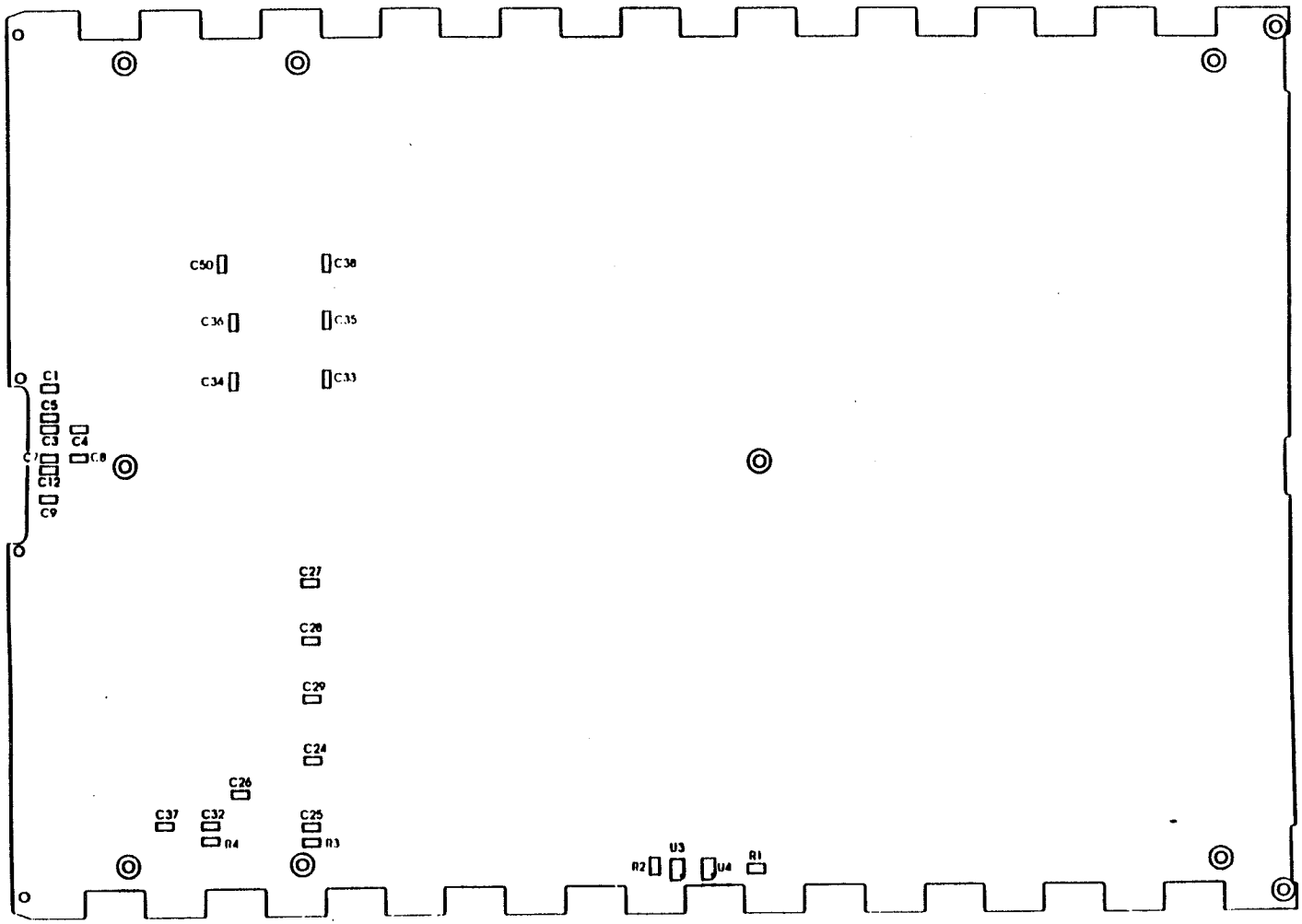
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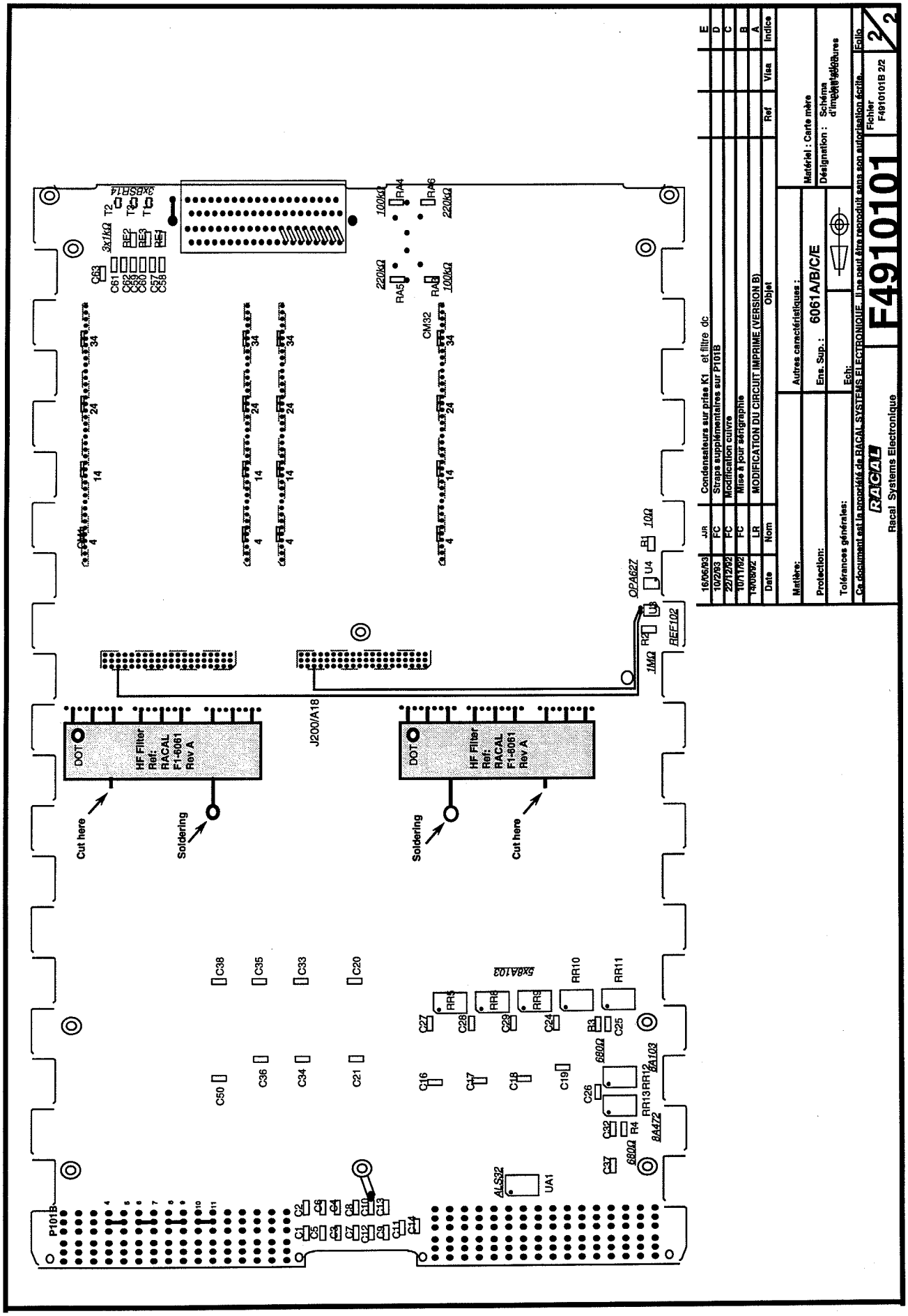
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Auteur: FC	Verif:	Modif: FC	Fich:	
Date: 17/09/91	Date:	Date: 11/10/91	Ech:	Folio:
Sous-ensemble: Sérigraphie coté soudures carte mère			Sujet: F4910101	
			Version: X B C D E F	
Ensemble: 6061 (MOTHER BOARD)			RACAL SYSTEMS Electronique 18 Av. DUTARTRE 78150 LE CHESNAY	

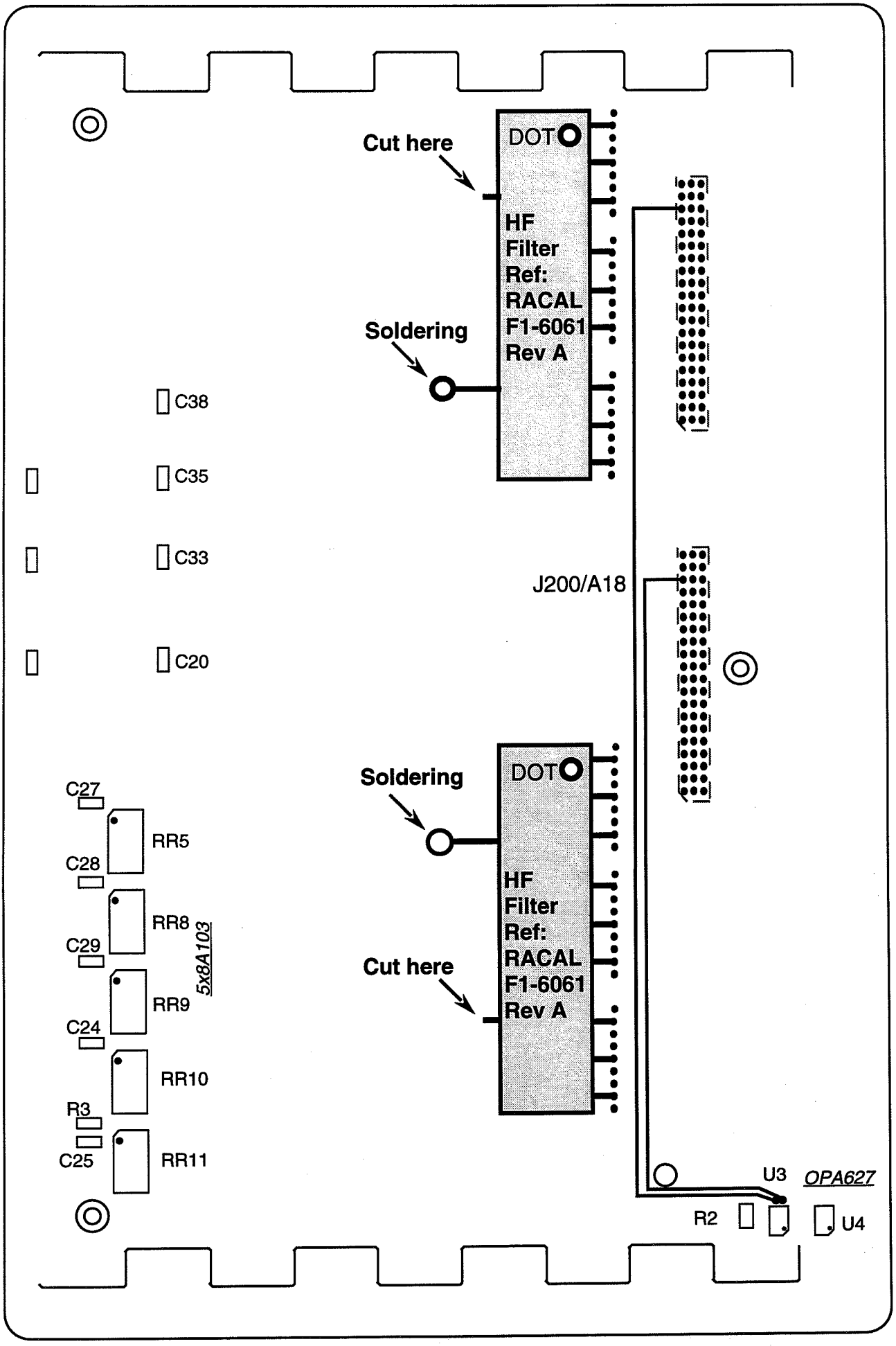
RACAL

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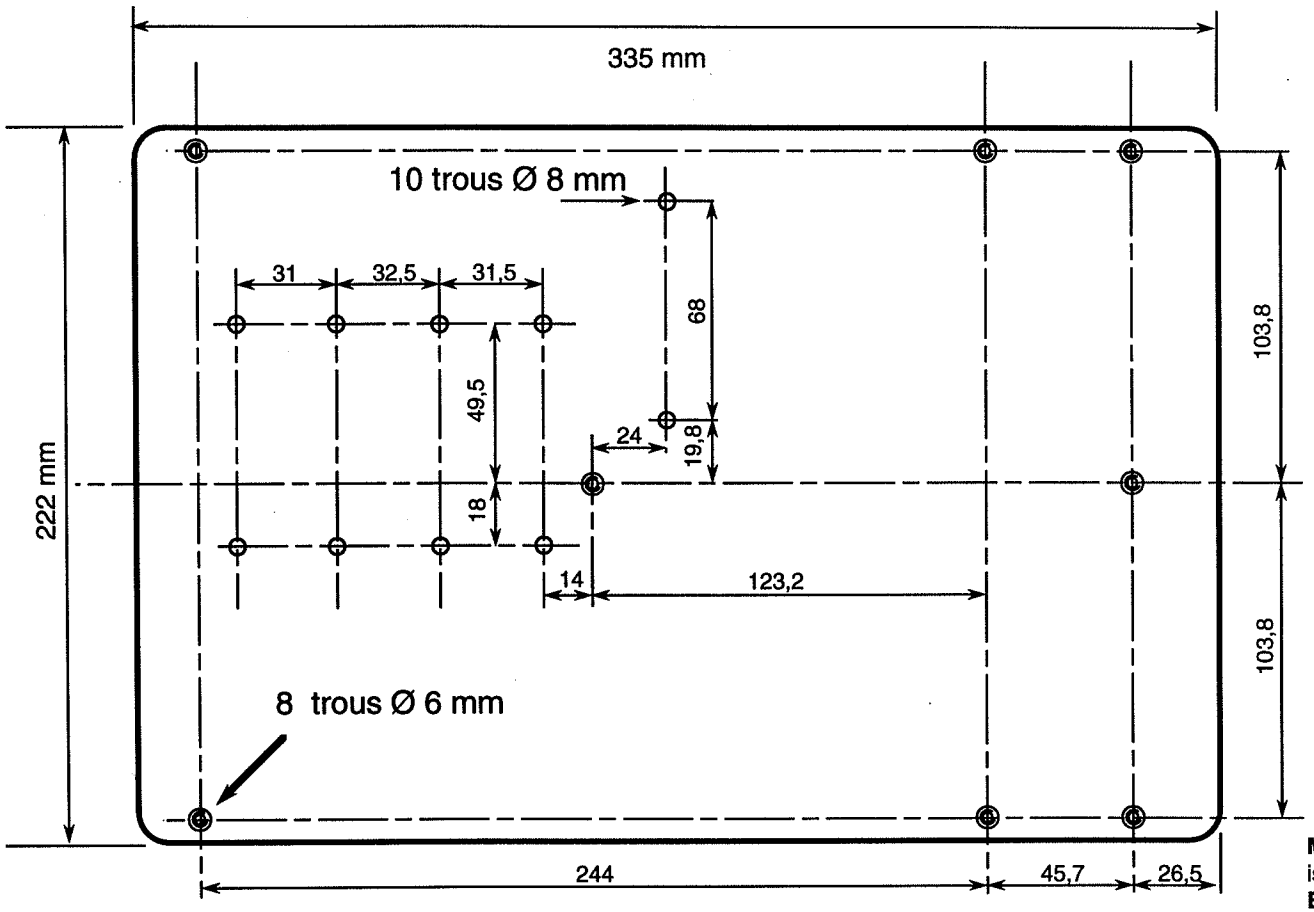
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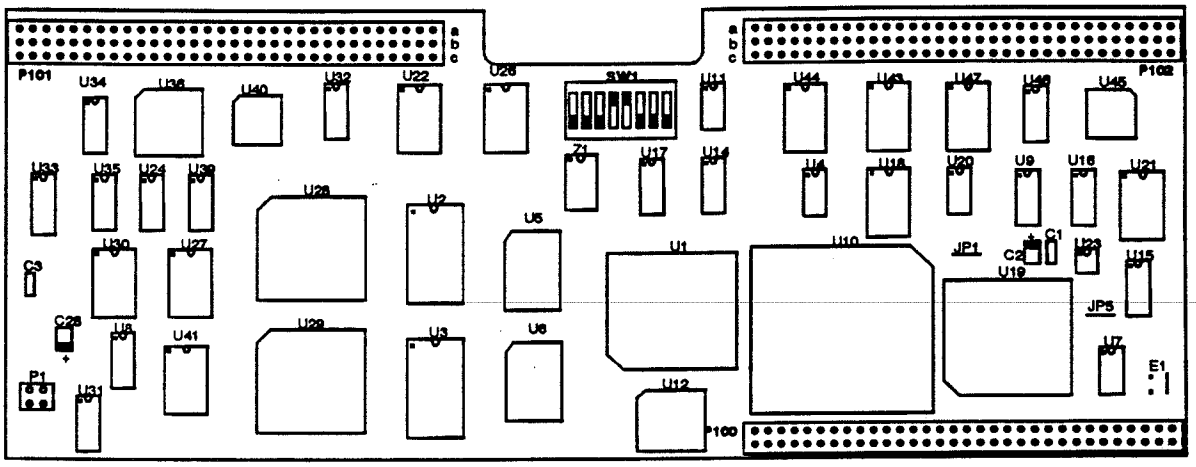


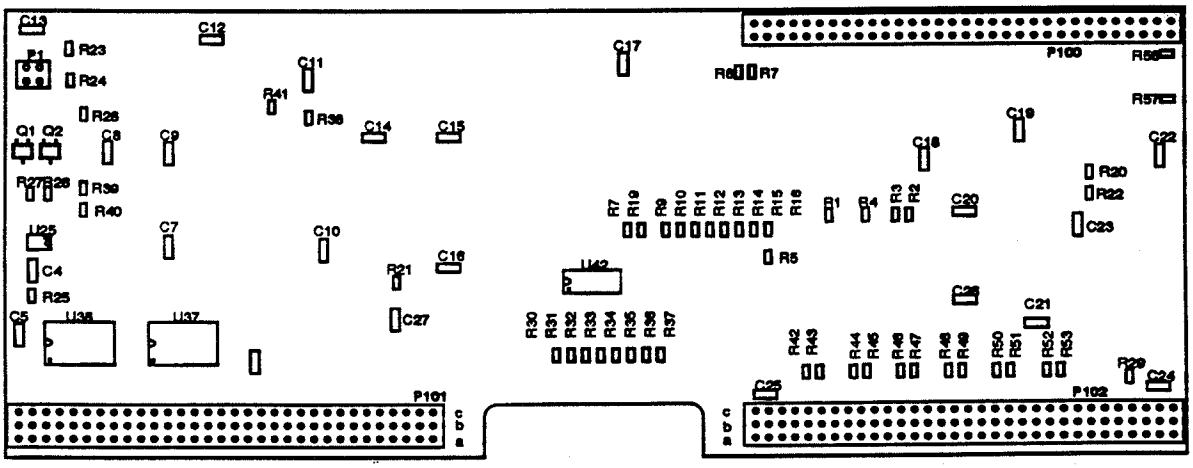
MATIERE : Polycarbonate, isolement > 1KV à 125°C
EPAISSEUR : 0,25 mm
COTATION : en mm
TOLERANCE : ± 0,2 mm

Verif:	**Modif:**	**Version:**	**Sous-ensemble:** Protection Capot inf.	**Code:** F8910190
Date:	**Date:**			**Folio:** 1
Auteur: TPL	**Fich:**	A B C D	**Ensemble:** 6061	**RACAL-SYSTEMS** Electronique 18 Av. Dutartre 78150 le Chesnay
Date: 23/9/93	**Ech:** 1/2	E F G H		

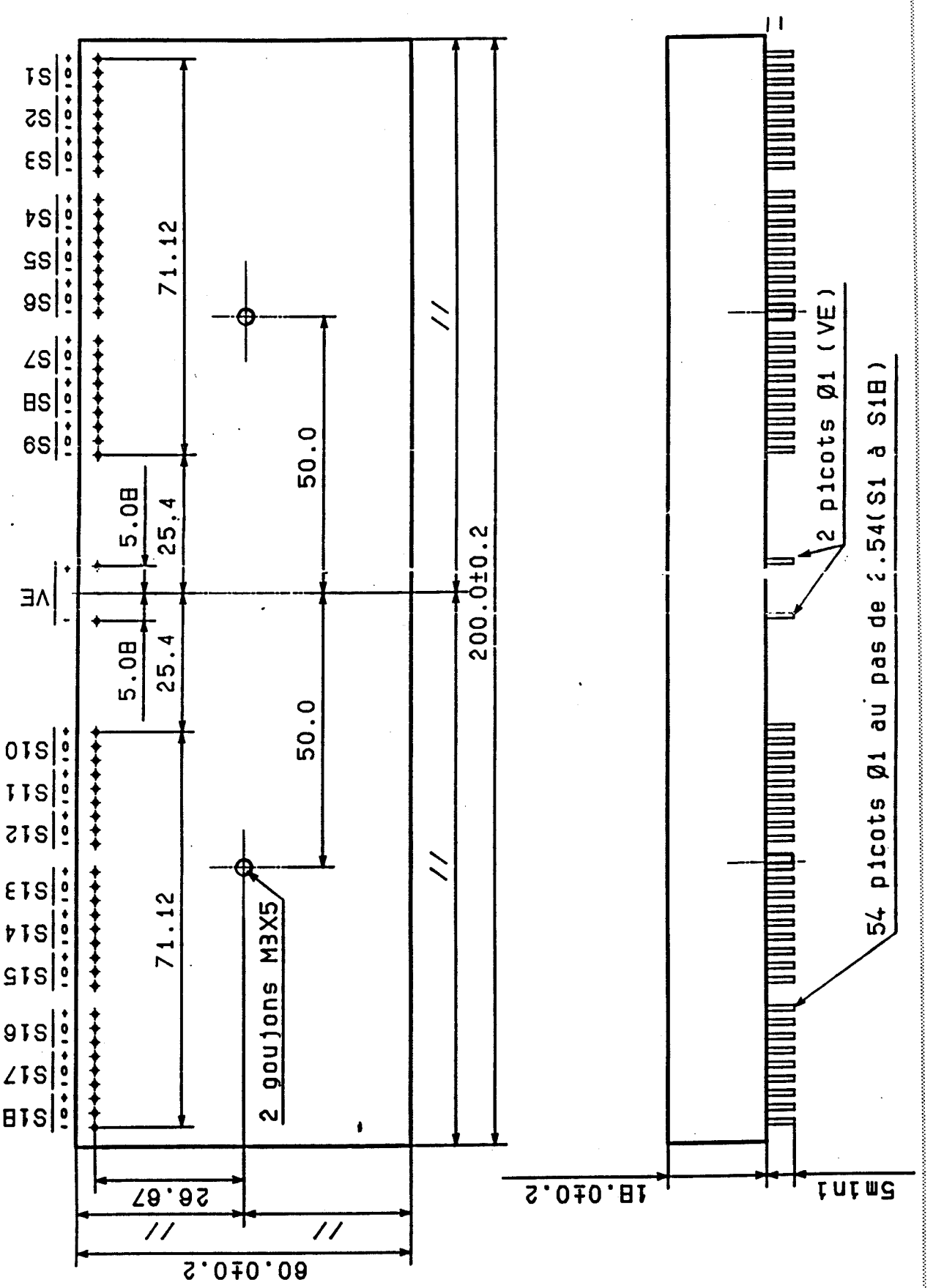
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PCB-VXI INTERFACE ASSY





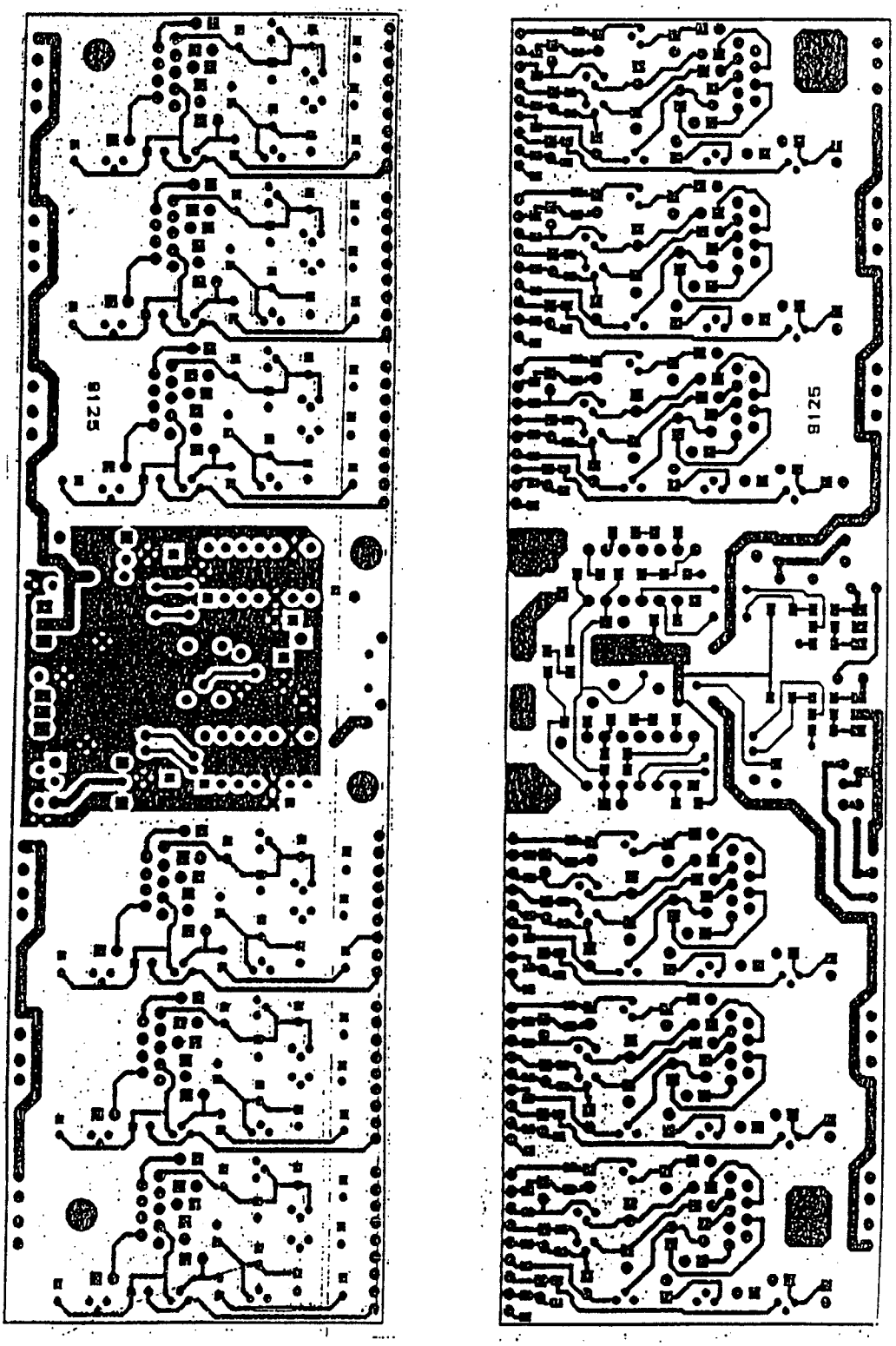
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8081-V1.0 - February 1992

RACAL

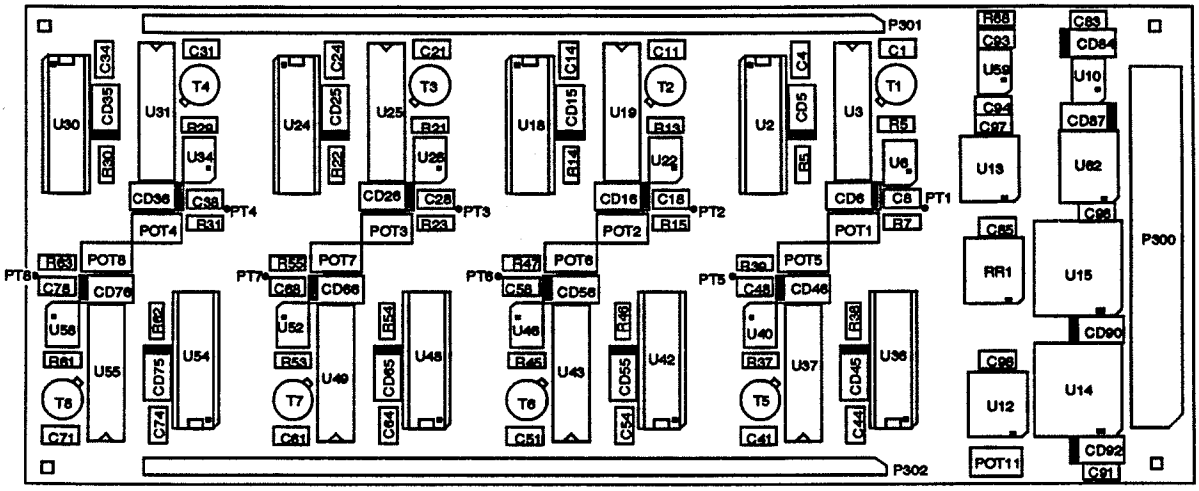
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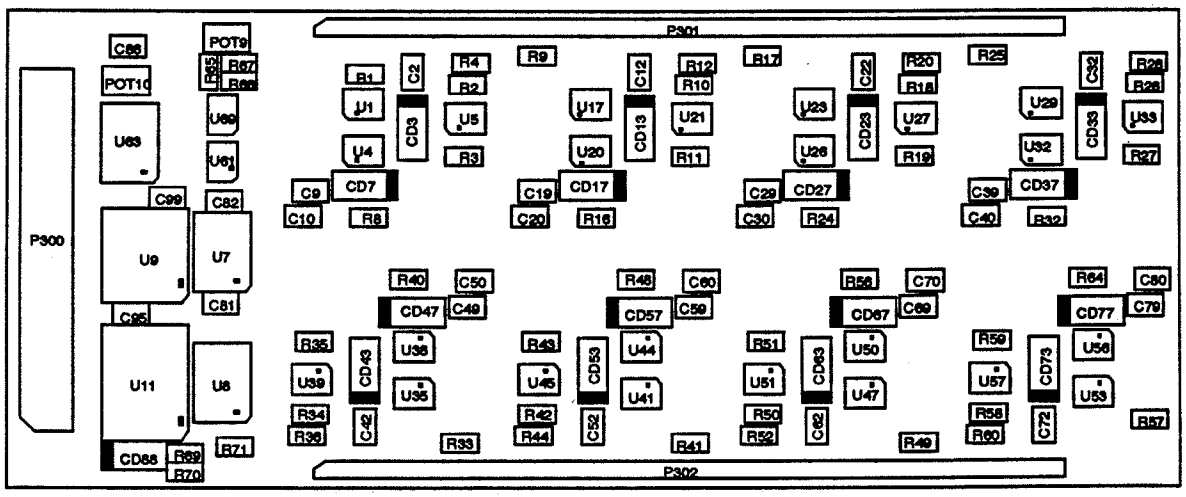


9125 CLICHE FACE SOUDURES

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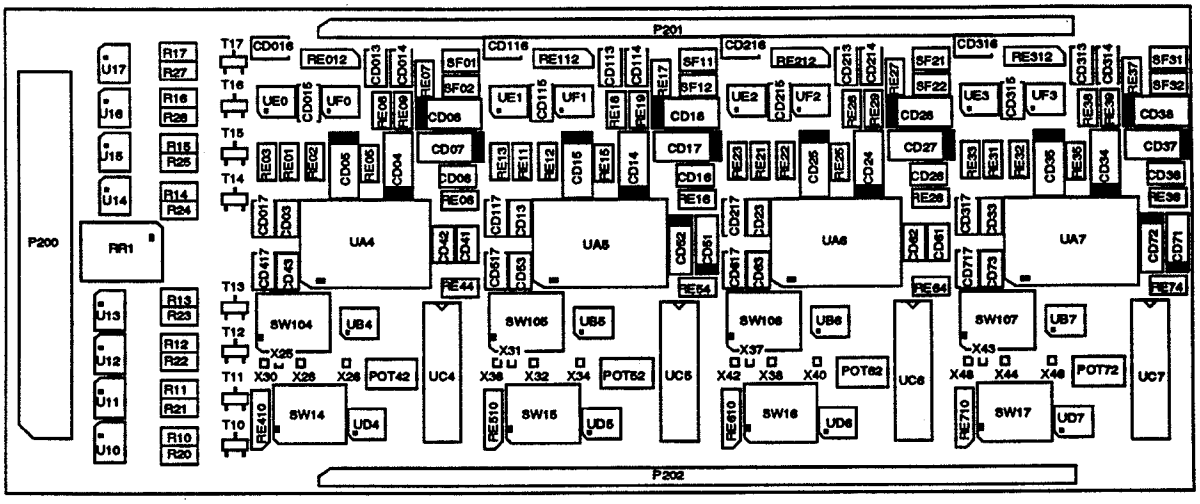
PCB-Analog Input ASSY

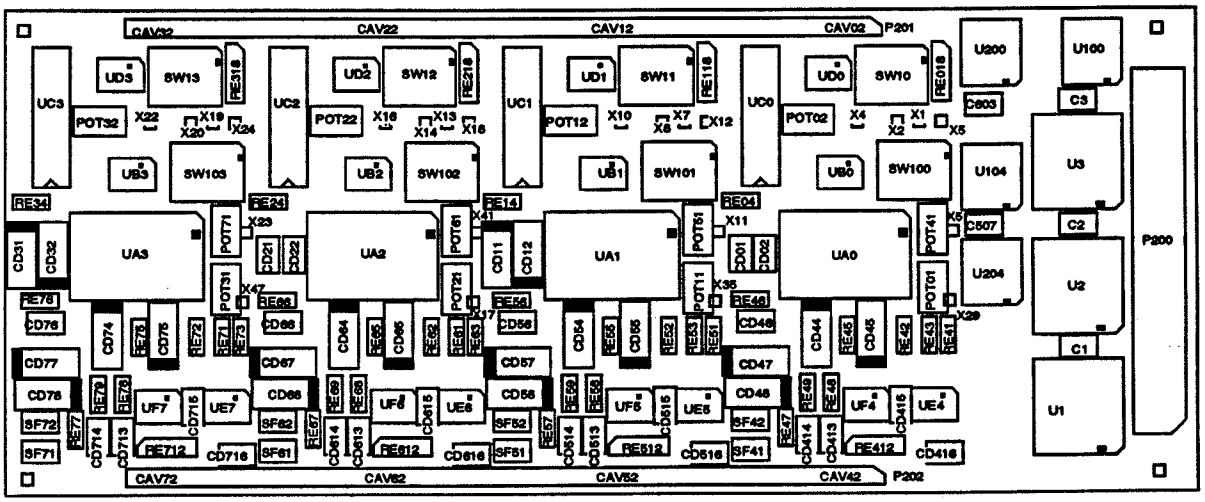




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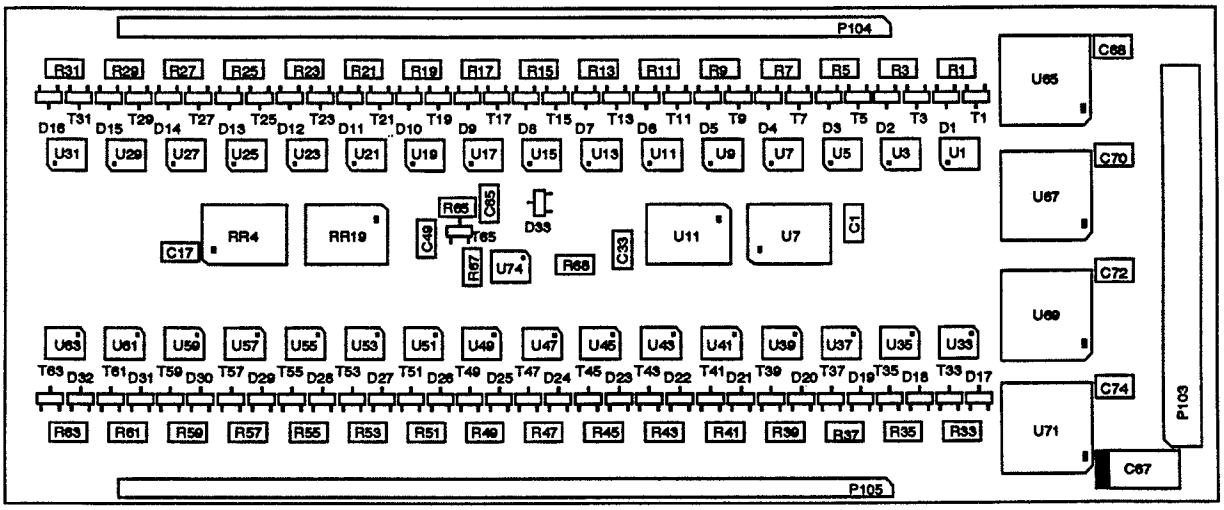
PCB-Analog Output ASSY

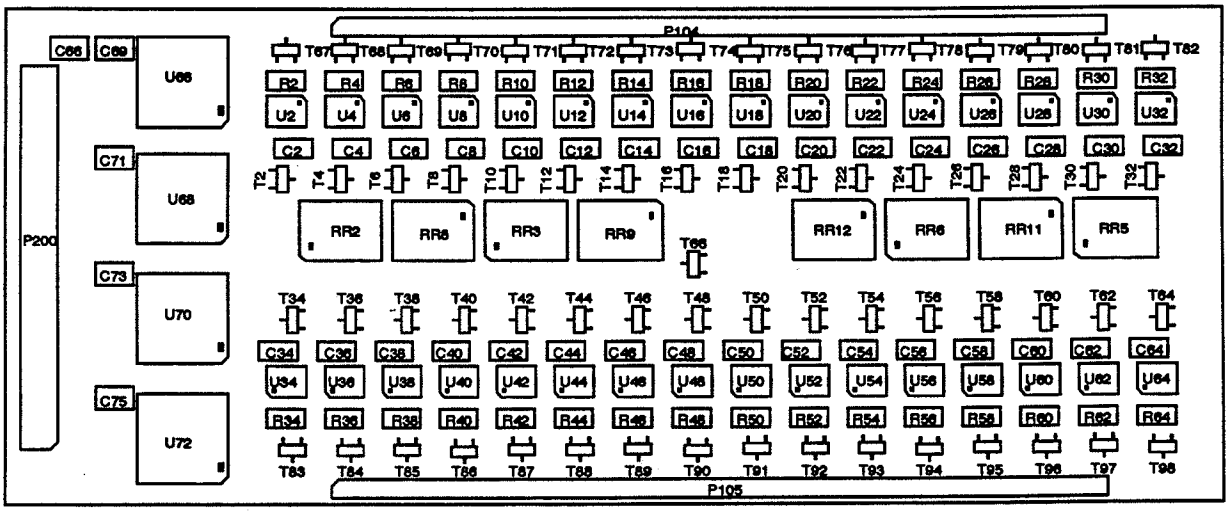




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DIGITAL INPUT/OUTPUT





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SECTION 10

Part Lists

MODEL 6061

F3910107	FINAL ASSEMBLY
F3910101	PCB Assy., MOTHER Board
F3910105	PCB Assy., VXI INTERFACE Board
F3910106	PCB Assy., DC/DC CONVERTER Board
F3910104	PCB Assy., ANALOG INPUTS Board
F3910103	PCB Assy., ANALOG OUTPUTS Board
F3910102	PCB Assy., DIGITAL INPUTS/OUTPUTS Board.

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PARTS LIST FOR FINAL ASSY

Part Number	Description	Qty	Reference	Remark
140T88208	Accesory K1a,2a	2	T88208	K1b,2b
80P101001	Base and cover, VXI, C size, single	1	F8910107/3,4	
80P101002	front panel, VXI, C size, single	1	F8910107/1,2	
80P101008	Spacer for VT1	1	F8910101/3	
80P101005	Spacer	1	F8910101/4 (4 & 4)	
80P101006	Cover for digital/analog plugs T88208	2	2 PIECES	
80P101007	Screw M2,5	1	F8910101/6 (12)	
680000006	VXI Extractor handle, Top, Grey	1	20817-328	
680000007	VXI Extractor handle, Bottom, Grey	1	20817-327	
810000010	Label , Static Warning	1		
810000011	Label, RACAL Serial & Model Number	1		
F8910190	Isolator for Base Plate	1	F8910190	
670910028	Washer	2	21100-464	
670910027	Screw	2	21100-379	
850001023	Screw	4	M2,5x10 PBaZ	
850000018	Screw for Extractor handle	2	M2,5x6 PFaZ	
850001002	Screw for VT1	4	M3x12 PBaZ	
850001024	Special Screw	12	M2,5x15 PBaZ	
860000005	Washer, Split lock	4	M2,5 DIN 137A	
860000003	Washer, Flat for extractor handle	2	3,2 EXT 8	
860000004	Washer, Plastic, Flat	24	2,5 EXT 6	87-8889-H
660100029	Grounding accesory	2	519	
530000007	Noise Filter for DC/DC converter	2	F1-6061, Rev A	

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PARTS LIST FOR MOTHERBOARD

Part Number	Description	Qty	Reference	Case
INTEGRATED CIRCUITS				
47000F245	Octuple buffers (SMD)	2	U9,10	SOIC20
47000LS03	Quad NAND open collectors (SMD)	1	U12	SOIC14
4700ALS00	Quad NAND (SMD)	1	U20	SOIC14
470ALS541	Octuple buffers (SMD)	4	U11,13-15	SOIC20
470ALS563	Octuple D-Latches (SMD)	1	U22	SOIC20
470022V10	PAL (SMD)	5	U16-19,21	PLCC 28
427815ACV	Precision voltage regulator (2%)	1	U1	TO220
427915ACV	Precision voltage regulator (2%)	1	U2	TO220
470REF102	Precision voltage reference (10V)	1	U3	SOIC8
470OPA627	Low noise operational amplifier	1	U4	SOIC8
478L05ACD	Voltage regulator (SMD)	1	U23	SOIC8
470NE555D	Timer (SMD)	3	IC1-3	SOIC8
RESISTORS				
240000005	Resistor (SMD)	2	R3,4	1206
240000007	Resistor (SMD)	3	RE4-6	1206
240000008	Resistor (SMD)	3	RE7-9	1206
240000017	Resistor (SMD)	4	R5,RE1-3	1206
240000024	Resistor (SMD)	2	R2,R2bis	1206
240000010	Resistor (SMD)	1	R1	1206
280000004	Resistor array (SMD)	5	RR1-5	SOIC16
280000005	Resistor array (SMD)	7	RR6,7,8-12	SOIC16
POTENTIOMETERS				
200000203	Potentiometer 1 turn, 20kΩ (SMD)	1	POT1	
CAPACITORS				
380000001	Ceramic capacitor (SMD)	33	C1,3-5,7-9,12,15,24-26 C27-29,31,32-40,50,57-63	1206
380000005	Tantalum capacitor (SMD)	9	CD3-8,14,15,30	C size
380000009	Tantalum capacitor (SMD)	2	CD1,2	D size
FILTERS				
530000002	Ceramic EMI Filter	4	L1,L3-L5	
CONNECTORS				
140096096	C size connector 96/96	2	P1,P2	DIN 41612
140S316G2	Board/board 3x16 socket	4	J101,J102	
140S216G2	Board/board 2x16 socket	2	J100	
140S220G2	Board/board 2x20 socket	1	J103	
140S320G2	Board/board 3x20 socket	2	J200,J300	
140S120G2	Board/board 1x20 socket	12	J104,5,201,2,301,2	
140S202G2	Board/board 2x2 socket	1	JP1	
14HV78S7J	Digital/Analog I/O sockets	2	K1,2	HD Sub D
14HZ78POJ	Digital/Analog I/O plugs	2	K1,2	HD Sub D
MISCELLANEOUS				
170000001	Fuse 1A delayed (SMD)	2	F1,F4	
170000002	Fuse 2.5A delayed (SMD)	1	F3	
170000003	Fuse 3A delayed (SMD)	1	F5	
46HPLM132	Red LED (Front panel)	1	LD1	Ø 3mm
46HPLM152	Green LED (Front panel)	2	LD2,LD3	Ø 3mm
46HPLM142	Yellow LED (Front panel)	1	LD4	Ø 3mm
4300BSR14	Transistor (SMD)	3	T1-3	SOT 23
12P101M0B	Printed board	1		
140T88208	Cover for digital/Analog I/O plugs	2	K1,2	Metalic
490000001	Heatsink	1		
490000002	Hardware kit TO220	2	For U1,U2	
49PLCC28S	PLCC socket for 22V10	5	U16,17,18,19	PLCC 28 pin
52P101001	DC/DC CONVERTER 18 x ±15V	1	Conv	
80P101001	19" CASE ASS'Y	1	Top & bottom covers	
80P101002	Front panel & overlay	1	Front panel	
80P101003	Heatsink ASS'Y.	1		
910000001	ASS'Y,PCB VXI interface module 8 Mhz	1		
680000006	Extractor handle, top	1		
680000007	Extractor handle, bottom	1		
680000008	Hardware kit	1		

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PARTS LIST FOR VXI INTERFACE & CPU BOARD

Part Number	Description	Qty	MF Code	Reference	Case
Printed board (unloaded)					
33-0011-000	PCB, VXI interface module	1		see (48)	
Semi-conductors					
15-0010-005	IC, INT.	1	TL7705	U23	SO8
17-0010-032	IC, DIGITAL	1	74LS32	U24	SO14
17-0010-148	IC, DIGITAL	1	74LS148	U14	SO16
17-0011-000	IC, DIGITAL	1	74F00	U35	SO14
17-0011-032	IC, DIGITAL	1	74F32	U39	SO14
17-0011-074	IC, DIGITAL	1	74F74	U7	SO14
17-0011-138	IC, DIGITAL	2	74F138	U9,34	SO16
17-0011-245	IC, DIGITAL	1	74F245	U47	SO20
17-0011-367	IC, DIGITAL	1	74F367	U46	SO16
17-0011-641	IC, DIGITAL	2	74F641	U21,22	SO20
17-0011-652	IC, DIGITAL	2	74F652	U37,38	SO24
17-0012-008	IC, DIGITAL	1	74HCT08	U11	SO14
17-0012-030	IC, DIGITAL	1	74HCT30	U42	SO14
17-0012-074	IC, DIGITAL	2	74HCT74	U20,31	SO14
17-0012-138	IC, DIGITAL	2	74HCT138	U16,17	SO16
17-0012-151	IC, DIGITAL	1	74HCT151	U15	SO16
17-0012-244	IC, DIGITAL	3	74HCT244	U25,43,44	SO20
17-0012-367	IC, DIGITAL	2	74HCT367	U32,33	SO16
17-0012-374	IC, DIGITAL	2	74HCT374	U30,41	SO20
17-0012-688	IC, DIGITAL	2	74HCT688	U18,26	SO20
17-0013-032	IC, DIGITAL	1	74HC32	U4	SO14
17-0014-038	IC, DIGITAL	1	74S38	U8	SO14
17-0015-000	IC, MICROPROCESSOR	1	MC68000FN-8	U10	
17-0016-000	IC, TIMER	1	MC68230FN-8	U19	
19-0010-001	IC, MEMORY, EPROM	1	M5M27C102JK-15	U1	
19-0011-000	IC, MEMORY, RAM	2	KM62256ALG-10	U2,3	
19-0013-000	IC, MEMORY, EEPROM	2	NQ28C64-200	U5,6	
19-0014-000	IC, MEMORY, DUAL PORT RAM	2	IDT7130SAJ	U28,29	
21-0010-001	IC, PAL	1	22V10FN-25	U36	
21-0011-001	IC, PAL	1	16L8AFN-15	U40	
21-0012-001	IC, PAL	1	16R4AFN-15	U45	
21-0013-001	IC, PAL	1	20L8AFN-25	U12	
Resistors					
01-0011-102	CHIP Resistor 5PCT (SMD)	10	1KΩ, 0.06W	R5,6,19,21,26,27,38-41	805
01-0011-103	CHIP Resistor 5PCT (SMD)	4	10KΩ, 0.06W	R1-4	805
01-0011-104	CHIP Resistor 5PCT (SMD)	1	100KΩ, 0.06W	R25	805
01-0011-220	CHIP Resistor 5PCT (SMD)	10	22Ω, 0.06W	R42-51	805
01-0011-331	CHIP Resistor 5PCT (SMD)	3	330Ω, 0.06W	R23,24,52	805
01-0011-471	CHIP Resistor 5PCT (SMD)	2	470Ω, 0.06W	R20,53	805
01-0011-472	CHIP Resistor 5PCT (SMD)	22	4.7KΩ, 0.06W	R7-16,22,28,30-37,56,57	805
01-0013-825	CHIP Resistor 1PCT (SMD)	1	825Ω, 0.06W	R29	805
01-0018-102	NETWORK Resistor 2PCT	1	1KΩ	Z1	
Capacitors					
05-0010-103	Mono. capacitor (SMD)	26	0.01uF / 50V	C1,3-27	1206
05-0012-336	Tantalum capacitor (SMD)	2	3.3uF /16V	C2,28	
Connectors, plugs & sockets					
27-0011-032	Connector, pin strip	5	P101A,B,C;P102A,C		32 PINS
27-0013-004	Connector, right angle	1	P1		4 PINS
27-0013-064	Connector, right angle	1	P100		64 PINS
27-0014-044	PLCC socket	1	see (45)		44 PINS
27-0014-068	PLCC socket	1	see (46)		68 PINS

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PARTS LIST FOR DC / DC CONVERTER

Description	Qty	MF Code	Reference	Case
Semi-conductors				
Diode 1A 90V = 1N9600	36	BYS21.90	CR1-36	
Diode 3A 600V	2	BYW36	CR37,38	
Signal diode	1	1N4448	CR39	
Rectifier diode	1	1N4004	CR40	
MOS FET Canal N 100V 52A	2	BUK456 100A	Q37,38	TO220
Integrated circuits				
Voltage regulator 15V 100MA	18	LM78L15ACZ	Q1,3,5,7,9,11,13,15,17,19,21,23,25,27,29 Q31,33,35	TO92
Voltage regulator -15V 100MA	18	LM79L15ACZ	Q2,4,6,8,10,12,14,16,18,20,22,24,26,28 Q30,32,34,36	TO92
Controller	2	SI 9112	MX1,2	
Resistors				
Carbon resistor	2	100KΩ 1/4W 5%	R1,2	
Resistor (SMD)	2	22Ω 1/8W 5%	R3,15	1206
Resistor (SMD)	2	6.8Ω 1/8W 5%	R4,14	1206
Carbon resistor	2	0.22Ω 1/4W 5%	R5,13	
Carbon resistor	2	1Ω 1/4W 5%	R5,13	
Resistor	2		R6,16	
Resistor (SMD)	2	1kΩ 1/8W 5%	R7,17	1206
Resistor (SMD)	1	75kΩ 1/8W 5%	R8	1206
Resistor (SMD)	2	22kΩ 1/8W 5%	R9,18	1206
Resistor (SMD)	2	10KΩ 1/8W 5%	R10,19	1206
Resistor (SMD)	2	4.7KΩ 1/8W 5%	R11,20	1206
Resistor (SMD)	1	2.7KΩ 1/8W 5%	R12	1206
Resistor (SMD)	1	90.9KΩ 1/8W 1%	R21	1206
Resistor (SMD)	2	100KΩ 1/8W 5%	R22,23	1206
Inductors				
Inductor 3E2	1	N°974	L1	Diam. 14
Inductor 15MH	2	TSL0707-150	L2,3	
Capacitors				
Electro. capacitor SMEVB	36	100MF 25V 6.3X11	C1,2,7,8,13,14,19,20,25,26,31,32,37 C38,43,44,49,50,55,56,61,62,67,68,73 C74,79,80,85,86,91,92,97,98,103,104	
Electro. capacitor SRAVB	36	22MF 40V 6.3X7	C3,4,9,10,15,16,21,22,27,28,33,34,39 C40,45,46,51,52,57,58,63,64,69,70,75 C76,81,82,87,88,93,94,99,100,105,106	
Ceramic capacitor (SMD)	38	100NF 50V 10%	C5,6,11,12,17,18,23,24,29,30,35,36,41,42 C47,48,53,54,59,60,65,66,71,72,77,78,83 C84,89,90,95,96,101,102,107,108,120,123	1206
Poly. capacitor MKT 2P	2	100NF 100V 10%	C109,112	
Electro. capacitor CE-UST	1	10MF 63V 6.5X16	C110	
Electro. capacitor SMEVB	3	47MF 63V 8X11.5	C111,113,115	
Ceramic capacitor CN72	2	1NF 100V 10% 5.08	C114,116	
Capacitor	2		C117,118	
Electro. capacitor SRAVB	2	4.7MF 35V 4X7	C119,122	
Ceramic capacitor (SMD)	1	1NF 50V 10%	C121	1206
Miscellaneous				
PCB DFTM 16/10° CU35u	1	9125		
Transformer	6	N°970	T1-6	
SILPAD 60*40	1			

TOTAL : **239**

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PARTS LIST FOR ANALOG INPUTS

Part Number	Description	Qty	Reference	Case
SEMI-CONDUCTORS				
470MOC207	Optocoupler (SMD)	8	U4,20,26,32,38,44,50,56	SOIC 8
450DPAD50	Pico-diode (Protection)	8	T1-T8	T0 66 mod.
4300BSR14	Bipolar transistor (SMD)	1	T9	SOT23
INTEGRATED CIRCUITS				
420ISO122	Isolated amplifier	8	U3,16,25,31,37,43,49,55	DIP16
420PGA102	Digitally controled amplifier	8	U2,17,24,30,36,42,48,54	DIP16
4700OPA27	OPA (SMD)	8	U5,21,27,33,39,45,51,57	SOIC 8
470OPA602	OPA (SMD)	11	U6,10,22,28,34,40,46,52,58,59,64	SOIC 8
470OPA627	OPA (SMD)	8	U1,17,23,29,35,41,47,53	SOIC 8
47ADS7800	Analog to digital conv. (SMD)	1	U11	SOIC 24
470INA105	Precision OPA (SMD)	2	U60,61	SOIC 8
4700DG413	Analog switches (SMD)	4	U7,8,62,63	SOIC 16
470ALS574	Octuple D (SMD)	3	U9,14,15	SOIC 20
4700ALS00	4 nand (SMD)	1	U12	SOIC 14
4700ALS74	2 D Latch (SMD)	1	U13	SOIC 14
RESISTORS				
240000001	Resistor (SMD)	1	R69	1206
240000018	Resistor (SMD)	10	R65,68,RX1-RX8	1206
240000003	Resistor (SMD)	1	R74	
240000005	Resistor (SMD)	8	R5,13,21,29,37,45,53,61	1206
240000017	Resistor (SMD)	16	R6,7,14,15,22,23,30,31,38,39 R46,47,54,55,62,63	1206
240000026	Resistor (SMD)	1	R67	1206
240000025	Resistor (SMD)	1	R71	1206
240000004	Resistor (SMD)	26	R2-4,10-12,18-20,26-28,34-36 R42-44,50-52,58-60,66,70	1206
240000027	Resistor (SMD)	1	R72	1206
240000028	Resistor (SMD)	1	R73	1206
240000023	Resistor (SMD)	8	R1,9,17,25,33,41,49,57	1206
240000024	Resistor (SMD)	8	R8,16,24,32,40,48,56,64	1206
RESISTOR ARRAYS				
280000005	Resistor array (SMD)	1	RR1	SOIC16
POTENTIOMETERS				
200000101	1 turn, 100Ω (SMD)	1	POT10	
200000103	1 turn, 10kΩ (SMD)	9	POT1-8,11	
200000104	1 turn, 100kΩ (SMD)	1	POT9	
CAPACITORS				
380000006	Ceramic capacitor (SMD)	8	C10,20,30,40,50,60,70,80	1206
380000000	Ceramic capacitor (SMD)	8	C9,19,29,39,49,59,69,79	1206
380000012	Ceramic capacitor (SMD)	8	C1,11,21,31,41,51,61,71	1206
380000001	Ceramic capacitor (SMD)	30	C2,4,12,14,22,24,32,34,42,44 C52,54,62,64,72,74,81,82,83 C85,86,89,91,93-99	1206
380000005	Tantalum capacitor (SMD)	37	CD3,5,6,7,13,15,16,17,23,25, 26,27,33,35,36,37,43,45,46,47, 53,55,56,57,63,65,66,67,73,75, 68,67,73,75	C size
CONNECTORS, PLUGS & SOCKETS				
140T320GR	Board to board 3x20 connector	1	P300	
14BBL120G	Board to board 1x20 connector	4	P301,302	
MISCELLANEOUS				
12P101ANI	Printed board circuit	1	E5910103	
	TOTAL	**263**		

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PARTS LIST FOR ANALOG OUTPUTS

Part Number	Description	Qty	Reference	Case
SEMI-CONDUCTORS				
4300BSR14	Bipolar transistor (SMD)	8	T10 - T17	SOT 23
470MOC207	Optocoupler (SMD)	8	U10 - U17	SOIC 8
INTEGRATED CIRCUITS				
420ISO122	Isolated amplifier	8	UC1-UC8	DIP 16
4700DG413	Analog switches (SMD)	8	SW10 - SW17	SOIC 16
470DAC813	Digital to Analog Converter (SMD)	8	UA1 - UA8	SOIC28
470INA105	OPA (SMD)	16	UB1-UB8, UF1-UF8	SOIC 8
470OPA602	OPA (SMD)	16	UD1-UD8, UE1-UE8	SOIC 8
4700ALS00	4 nand (SMD)	2	U200,201	SOIC 14
4700ALS32	4 or (SMD)	2	U100,101	SOIC 14
470ALS574	Octuple D (SMD)	3	U1,U2,U3	SOIC 20
RESISTORS				
	Calibrated resistor (SMD)	24	REX1,X2,X3 ...	1206
23009K001	Precision resistor	8	REX10 ...	TAS280
23001K001	Precision resistor	8	REX12 ...	TAS209
240000003	Resistor (SMD)	16	REX7,X9 ...	1206
240000010	Resistor (SMD)	16	REX4,X5 ...	1206
240000017	Resistor (SMD)	8	R20-R27	1206
240000018	Resistor (SMD)	8	REX6 ...	1206
240000021	Resistor (SMD)	8	REX8 ...	1206
240000022	Resistor (SMD)	8	R10-R17	1206
280000001	Resistor array (SMD)	1	RR1	SOIC 16
POTENTIOMETERS				
200000102	1 turn 1kΩ (SMD)	8	POTX1...	
200000103	1 turn 10kΩ (SMD)	8	POTX2...	
CAPACITORS				
380000000	Ceramic capacitor (SMD)	8	CDX14 ...	1206
380000001	Ceramic capacitor (SMD)	59	CDX3,X9,X10,X15,X16, CDX17...	1206
380000005	Tantalum capacitor (SMD)	56	CDX1,X2,X4,X5,X7,X8, CDX11,12...	C size
380000006	Ceramic capacitor (SMD)	8	CDX13 ...	1206
380000007	Ceramic capacitor (SMD)	8	CDX6 ...	1206
CONNECTORS, PLUGS & SOCKETS				
140T320GR	Board to board 3x20 connector	1	P200	
14BBL120G	Board to board 1x20 connector	4	P201,202	
MISCELLANEOUS				
53LQH3C10	Choke inductor 10µH (SMD)	16	SFX1, SFX2 ...	
12P101ANO	Printed board	1	E5910102	

TOTAL **361**

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PARTS LIST FOR DIGITAL I/O

Part Number	Description	Qty	Reference	Case
SEMI-CONDUCTORS				
4300BSR14	Bipolar transistor (SMD)	65	T1 - T65	SOT 23
44SST4393	FET transistor (SMD)	33	T66 - T98	SOT 23
470MOC207	Optocoupler (SMD)	65	U1 - U64,U74	SOIC8
4500BAS40	Schottky diode (SMD)	33	D1 - D33	SOT 23
INTEGRATED CIRCUITS				
470ALS574	Octuple D latche (SMD)	4	U65,67,69,71	SOIC20
470ALS563	Octuple latches (SMD)	4	U66,68,70,72	SOIC20
RESISTORS				
240000002	resistor (SMD)	66	R1 - R64,67,68	1206
240000003	resistor (SMD)	1	R65	1206
280000001	Resistor array (SMD) 680Ω	4	RR1,4,7,10	SOIC16
280000002	Resistor array (SMD) 470Ω	4	RR2,5,8,11	SOIC16
280000003	Resistor array (SMD) 220Ω	4	RR3,6,9,12	SOIC16
CAPACITORS				
380000001	Ceramic capacitor (SMD)	45	C1 - C65, C68 - C75	1206
380000005	Tantalum capacitor (SMD)	1	C67	C size
CONNECTORS				
14BDL120G	Board to board connector 2x20 pins	1	P103	
14BBL120G	Board to board connector 1x20 pins	4	P104, P105	
MISCELLANEOUS				
12P101DIO	Printed board	1	E5910101	

TOTAL **335**

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