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PROMENTUM™

COMPUTE PROCESSING MODULE REFERENCE

ATCA-4300
ATCA-4310



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Release history

Release	Date	Description
-0000	March 2007	First release.
-0001	September 2007	Added information about reprogramming the Crosspoint switch and the Ethernet controller. Added new software features in version 2.2.
-0002	January 2008	Added the ATCA-4310 model and removed the standard FRU information tables. Updated hardware information.
-0003	May 2008	Removed the software information, because it was incorporated into other manuals. Added pressure drop curves.
-0004	August 2008	Minor updates.
-0005	January 2009	Revised to explain ekey daemon configuration file modification for AMC cards.

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PREFACE

About this manual

This manual describes the Promentum™ ATCA-4300 and ATCA-4310 compute processing modules (CPMs). The CPM is fully compliant with the PICMG® ATCA® standard and is designed to be incorporated into high-availability (HA) systems such as the Promentum platforms SYS-6006 and SYS-6010.

Use this manual as a reference for the operation and the maintenance of the CPM. The material presented here is not introductory; the assumption is you are already familiar with the intended use of the CPM in your organization's ATCA platform, as well as the role of the ATCA platform within the local-area or wide-area network.

The simplified terms "CPM" and "module" may be used in place of "ATCA-4300 and ATCA-4310" throughout the rest of the manual.

Related Promentum manuals

The following software and hardware manuals are available to help you use the MRM:

- *ATCA-4300/ATCA-4310 Compute Processing Module Installation Guide.* The installation guide provides the steps for installing the module into a shelf and completing the initial configuration.
- *Software Guide for Management Processors and General Purpose Computing Processors*. The *Software Guide* introduces and describes the software RadiSys provides to manage the CPM. The guide includes an overview of the supported operating systems, software interfaces, configuration procedures, and supplied Linux packages. It supplies conceptual, reference, and usage information.
- *CLI Reference*. This reference manual for the command line interface describes the master CLI and its command modes. It serves as a reference for command syntax and options.

Where to get more product information

Please visit the RadiSys Web site at www.radisys.com for product information and other resources. Downloads (manuals, release notes, software, etc.) are available via the Technical Support Library product links at www.radisys.com/support or the product pages at www.radisys.com/products.

Standards information

For information about the PCI Industrial Computer Manufacturers Group (PICMG) and the ATCA standard, consult the PICMG Web site, www.picmg.org.

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Related documents

PICMG 3.0 Revision 2.0 *AdvancedTCA® Base Specification*, ECN-002, PCI Industrial Computer Manufacturers Group, May 19, 2006.

PICMG 3.1 R1.0 *Ethernet/Fibre Channel over PICMG 3.0,* PICMG

PICMG AMC.0 R2.0 *Advanced Mezzanine Card Base Specification, PCI Industrial Computer Manufacturers Group, November 15, 2006.*

PICMG AMC.1 R1.0 *PCI Express and Advanced Switching on AdvancedMC,* PCI Industrial Computer Manufacturers Group, January 20, 2005.

PICMG AMC.2 R1.0 *Ethernet Advanced Mezzanine Card Specification,* PCI Industrial Computer Manufacturers Group, March 1, 2007.

PICMG AMC.3 R1.0 *Advanced Mezzanine Card Specification for Storage,* PCI Industrial Computer Manufacturers Group, August 25, 2005.

IPMI Intelligent Platform Management Interface Specification, v1.5; Revision 1.1, February 20, 2002; Revision 1.1 Markup, June 1, 2004

IPMI Platform Management FRU Information Storage Definition, v1.0, Revision 1.1, September 27, 1999

UL 60950-1 Safety for Information Technology Equipment

CAN/CSA 22.2 #60950-1-03 Safety for Information Technology Equipment, CSA

EN 60950-1:2002 Safety for Information Technology Equipment, CENELEC

IEC 60950-1 Safety for Information Technology Equipment, IEC

SR-3580 Network Equipment–Building Systems (NEBS) Criteria Levels, Issue 2, January 2005, Telcordia

GR-63-CORE NEBS Requirements Physical Protection, Issue 3, March 2006, Telcordia

GR-1089-CORE Electromagnetic Compatibility and Electrical Safety–Generic Criteria for Network Telecommunications Equipment, Issue 4, June 2006, Telcordia

GR-78-CORE Generic Requirements for the Physical Design and Manufacture of Telecommunications Products and Equipment, Issue 1, September 1997, Telcordia

Notational conventions

This manual uses the following conventions:

BoldText A command or keyword.

`MonoText` Screen text and syntax strings.

All numbers are decimal unless otherwise stated.

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Electrostatic discharge

WARNING! This product contains static-sensitive components and should be handled with care. Failure to employ adequate anti-static measures can cause irreparable damage to components.

Electrostatic discharge (ESD) damage can result in partial or complete device failure, performance degradation, or reduced operating life. To avoid ESD damage, the following precautions are strongly recommended.

- Keep each module/PCB in its ESD shielding bag until you are ready to install it.
- Before touching a module, attach an ESD wrist strap to your wrist, and connect its other end to a known ground.
- Handle the module only in an environment in which all work surfaces, floor coverings, and chairs are connected to a known ground.
- Hold modules only by their edges and mounting hardware. Avoid touching PCB components and connector pins.

For further information on ESD, visit www.esda.org.

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PRODUCT DESCRIPTION 1

The ATCA-4300/ATCA-4310 compute processing module (CPM) is a high-performance, single-slot AdvancedTCA carrier-grade compute module based on Intel® architecture. It is designed for high-availability (HA) solutions providing 99.999% up time. This manual provides information about the CPM and serves as a reference for its electrical, mechanical, and environmental aspects.

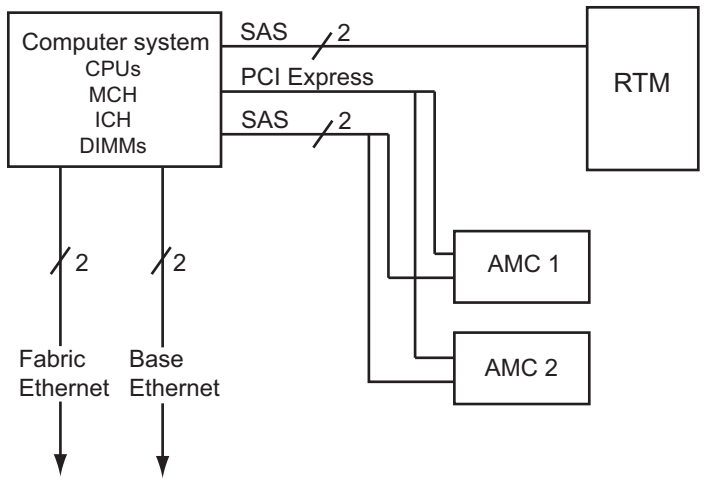
The CPM is an Advanced Mezzanine Card (AMC) carrier module that supports up to two AMCs and incorporates Base Ethernet, Fabric Ethernet, and IPMI interfaces. This hot-swappable module has two dual-core CPUs. The CPM has four DIMM sockets that support up to 16 GB of 400-MHz (PC2-3200) DDR2 SDRAM. The ATCA-4300 supports dual gigabit Ethernet network interfaces and optionally supports dual Fibre Channel star arbitrated loops. The ATCA-4310 supports two 10-Gb network interfaces.

The optional rear transition module (RTM) adds connectivity to the CPM by providing SAS (serial attached SCSI) and serial port connections to the backplane. The RTM is designed to provide cross-cabling to another compute module in the shelf's adjacent slot.

The CPM includes AMC bays to hold optional AMC modules, which can be used for SAS and SATA storage. On the ATCA-4300, the AMC Ethernet ports can connect directly to Fabric channels for multiple-lane Fabric connectivity. On the ATCA-4310, the AMC bay 2 Ethernet ports can connect to the CPUs.

The high-level CPM core components, main peripherals, and data flow are shown in the following figure.

Figure 1. CPM overview



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Product options

Table 1. CPM base order codes and corresponding differences

Model	ATCA-4300			ATCA-4310
Order code	A4300-CPU-SAS-NFE	A4300-CPU-SAS-FE	A4300-CPU-FC-FE	A4310-CPU-SAS-FE
Fabric interface	1-Gb Ethernet	1-Gb Ethernet	1-Gb Ethernet and Fibre Channel	10-Gb Ethernet
Front panel USB ports	2	2	2	1
Front panel Ethernet ports	None	2	2	2
PCI Express storage option	PESO-A (SAS/SATA)	PESO-A (SAS/SATA)	PESO-C (SATA and Fibre Channel)	PESO-A (SAS/SATA)
Additional storage devices and options	Hard disk AMC option	Hard disk AMC option	SATA hard disk AMC option	Redundant on-board flash, secure digital (SD) slot, hard disk AMC option

Because the ATCA-4310 consumes the Fabric interface ports completely with 10-Gb connections to the CPUs, the AMC bay connections are different than for the ATCA-4300. For more information, see *AMC bays* on page 15. The ATCA-4310 also requires a 10-Gb driver, which you should install as instructed in the *ATCA-4300/ATCA-4310 Compute Processing Module Installation Guide*.

An optional rear transition module (RTM) is supported for both the ATCA-4300 and ATCA-4310 with the order code A4300-CPU-RTM. For a detailed description, see *Chapter 5, Rear Transition Module, on page 59*.

Note: The ATCA-4300 CPM without front Ethernet ports (order code A4300-CPU-SAS-NFE) is very similar to the CPM with the ports (A4300-CPU-SAS-FE). The main difference is that the Ethernet connections associated with the missing ports are mapped to another location by the Fabric Crosspoint switch. For details, see *OEM Ethernet Crosspoint switch #1 connectivity record (ATCA-4300 only)* on page 112.

Dual processors

The CPM contains two Intel Dual-Core Xeon LV Sossaman processors; these high-performance CPUs are used for processor-based server systems. Features include:

- 1.66-GHz ULV, 2.0-GHz LV core clock frequency in high-frequency mode (HFM)
- 1.00-GHz core clock frequency in low-frequency mode (LFM)
- 667-MHz Source-Synchronous FSB
- 32-KB on-die L1 instruction and data caches
- 2-MB on-die, ECC-protected L2 cache shared between the two cores
- Thermal monitors, TM1 and TM2
- Digital temperature sensor

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Memory controller hub

The CPM uses the Intel E7520 memory controller hub (MCH) to interface with the memory channels via PCI Express. Features include:

- Two registered DDR2-400 memory channels operating in lock-step or single-channel
- 3.2-GB/s data bandwidth per channel at DDR2-400
- Maximum memory size of 16 GB of x72, ECC, registered DDR2 DIMMs

I/O controller hub

The CPM uses the Intel 6300ESB I/O controller hub to interface with peripheral input/output devices. Features include:

- Two USB 2.0 host controllers, providing two USB 2.0 ports
- LPC bridge
- SMBus 2.0 controller
- Real-time clock (RTC)
- Two 16550-compatible UARTs
- Two serial advanced technology attachment (SATA) ports

Intelligent Platform Management Controller

The CPM uses the Renesas H8S/2166 microcontroller for the Intelligent Platform Management Controller (IPMC). This device manages commands and data throughout the hardware management system. Features include:

- System event log (SEL)
- Remote executable flash and microcontroller software upgrade support
- Electronic keying support for Fabric interface, synchronization clocks, and update channels
- Serial-over-LAN (SOL) support via the Base Ethernet controller
- Local hardware sensors for the CPM and RTM
- Local output actuators
- IPMC, which comprises a microcontroller and an FPGA
- IPMBs
- Nonvolatile RAM
- AMC and RTM control and management

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Ethernet controllers

There are three Ethernet controllers on the CPM. Two provide backplane Ethernet connectivity, and the other provides dual gigabit copper interfaces for front panel connectivity. Features include:

- Dual copper MAC/PHY interfaces supporting 10BASE-T, 100BASE-TX, and 1000BASE-T applications, which are used for the Base interface
- Dual SerDes interfaces supporting 1000BASE-BX (ATCA-4300) or 10GBASE-BX4 (ATCA-4310), which are used for the Fabric interface
- Four-lane (x4) PCI Express interface
- Front-panel Ethernet access

PCI Express storage option (PESO)

The CPM provides a connection to a single PESO daughter card. Two daughter card options are available, and both provide a four-lane (x4) PCI-Express interface. Their individual features include:

PESO-A

- Four-port SAS controller
- SAS/SATA connections to both AMC bays and the RTM

PESO-C (ATCA-4300 only)

- Two-port Fibre Channel controller
- Fibre Channel connections to the Fabric interface
- Routing of two SATA ports from the I/O controller hub to the AMC bays (one port to each bay)

Front-panel interface

The CPM front panel provides AMC bays, port connectors, and LED indicators. Features include:

- Two mid-height AMC bays
- Two USB connectors on the ATCA-4300, one USB connector on the ATCA-4310
- Dual Ethernet ports
- An RJ-45 connector for the RS-232 serial port
- A reset button
- LEDs

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Backplane interfaces

The CPM provides backplane interfaces for Base and Fabric ports, AMC ports, the update channel, synchronization channels, and the IPMB interfaces. Features include:

- Two 10/100/1000 copper ports, Base interface.
- Two 1000BASE-BX ports from the CPUs, Fabric interface (ATCA-4300 only).
- Four 1000BASE-BX ports from the two AMC bays, Fabric interface. Up to two ports are routed from AMC bay 1, and up to four ports from bay 2, for a total of four backplane ports (ATCA-4300 only).
- Two Fibre Channel ports routed to the optional PESO-C, Fabric interface (ATCA-4300 only).
- Two 10GBASE-BX4 ports from the CPUs, Fabric interface (ATCA-4310 only).
- AMC port-12 connection to ports 0 & 1 of the update channel.
- Four sync channel differential clock inputs (CLK1A, CLK1B, CLK2A, CLK2B).
- Two sync channel differential clock outputs (CLK3A, CLK3B).
- Two –48V power rails.
- Two IPMB interfaces.

See *Backplane interfaces* on page 101 for related information.

AMC bays

The CPM uses dual Advanced Mezzanine Card (AMC) bays which accept midsize form-factor modules. One of the functions of an AMC is to provide on-board hard drive storage. Features include:

- Compliance of both bays with AMC.0, AMC.1, AMC.2, and AMC.3 specifications
- Support for dual 1000BASE-BX connections from each bay to the Fabric interface (ATCA-4300 only)
- Bay 2 supports two additional 1000Base-BX connections to the Fabric interface that can be used instead of the bay 1 Fabric interface connections (ATCA-4300 only)
- Bay 2 supports two 1000BASE-BX connections through an Ethernet controller to the CPUs (ATCA-4310 only)
- Four-lane (x4) PCI-Express interface to each bay
- Support for a single midheight double-wide AMC

For more details, see *AMC bays* on page 34.

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Rear transition module (RTM)

The RTM is an optional device that provides additional Zone 3 connectivity to the CPM via the SAS ports. The RTM also contains a serial port (COM2), which is used to provide cross-cabling to other CPMs. Features of the RTM include:

- Four SAS ports
- IPMC I^2C bus
- IPMC hot-swap control signals
- Serial port (3.3V signals)
- Eight high-speed differential ports (ports 17–20 on each AMC bay)

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THEORY OF OPERATION 2

The CPM provides the general-purpose compute and processing capability within an ATCA platform. It includes two processors, each with two processing cores, in a symmetric multiprocessing (SMP) configuration. The CPM is a self-contained compute element and provides its own local memory, storage, and network and I/O connections. The optional RTM provides additional I/O connections to the CPM through the back side of an ATCA shelf.

The CPM is a hot-swappable single-slot node module that integrates into the ATCA platform. The main core of the CPM comprises the dual-processor, dual-core CPUs, and the chipset containing the memory controller hub (MCH) and the I/O controller hub (ICH). The CPUs communicate with other blades in the ATCA system through the Base and Fabric Ethernet interfaces. Peripheral I/O expansion is provided via two AdvancedMC (AMC) mezzanine sites. Communication to AMC sites is provided via PCI Express, SAS/SATA, and Ethernet interfaces. (On the ATCA-4310, Ethernet connectivity is provided to AMC bay 2 only.)

There are four SAS interfaces; two connect to the RTM, and one connects to each of the two AMC sites. For redundancy purposes, it is typical to have the local CPU access both the local storage disk and a remote storage disk on another CPM. To link redundant pairs, one CPM is cabled to another CPM through the RTM and the backside of the shelf. This setup can be used to create a 1+1 RAID array between a pair of CPMs, each with its own AMC storage module. When data is written and stored on the active storage disk, the image is mirrored and written to the standby storage disk as well. In the event one storage disk fails, then the application in its entirety will fail over to the backup storage disk.

Each CPM backplane has two Base Ethernet and two Fabric Ethernet channels. These channels interface with the switch modules in the shelf. Typically the Base Ethernet is used for the management/control plane and the Fabric Ethernet is used for the user/data plane. These channels interface to other elements in the shelf through the Ethernet switches on the switch and control module (SCM).

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Figure 2 shows the management/control and user/data planes.

Figure 2. Management/control and user/data planes

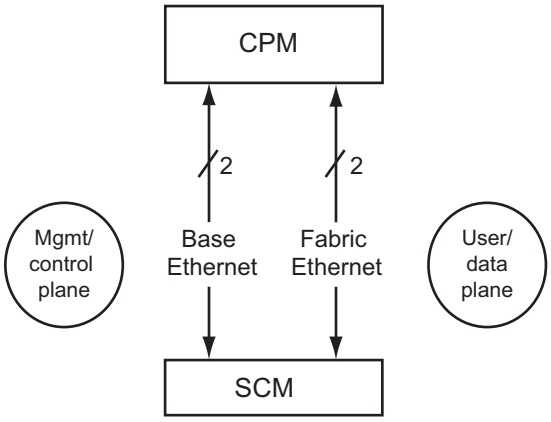
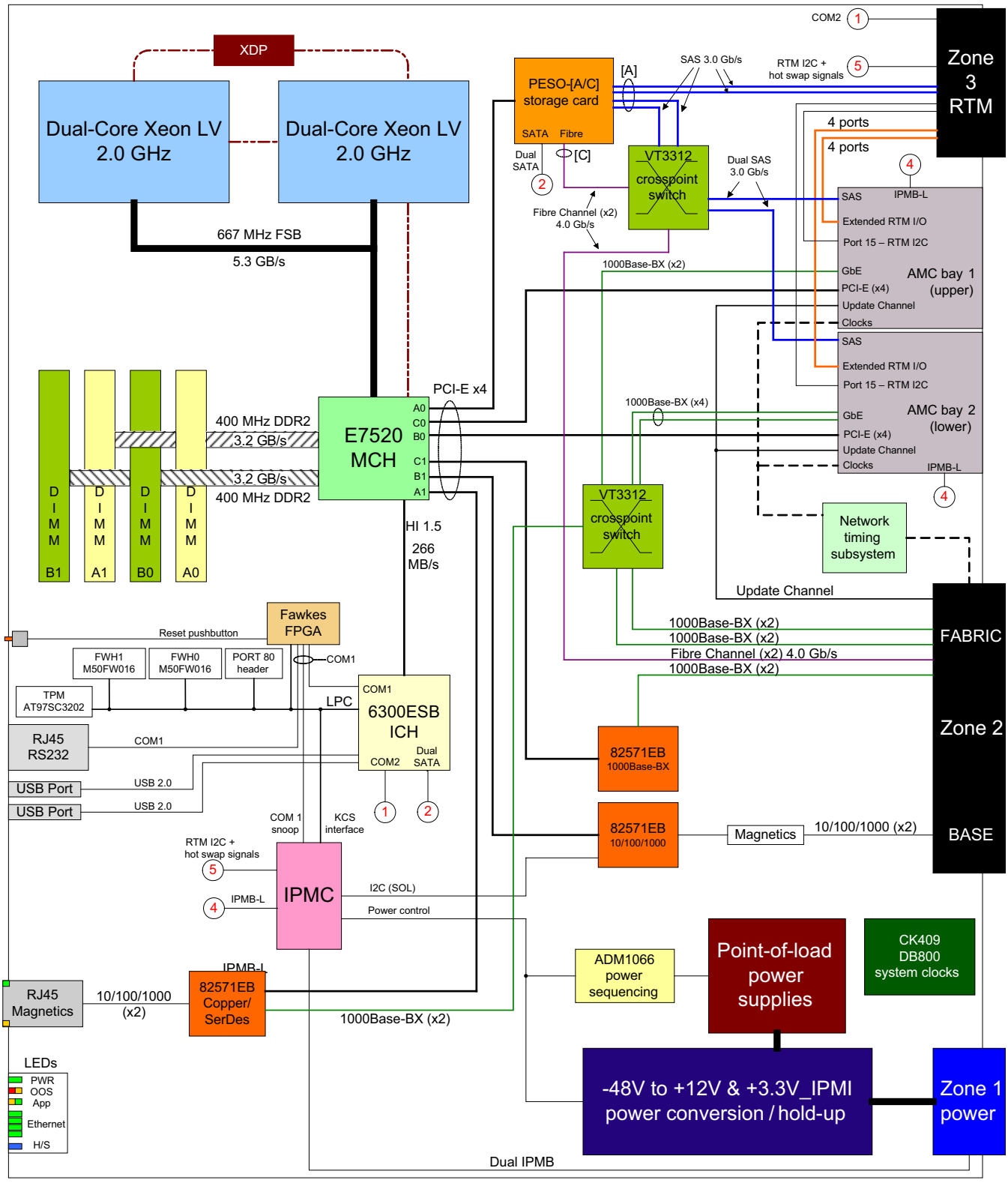


Figure 3 on page 19 shows the ATCA-4300 CPM's block diagram, and Figure 4 on page 20 shows the ATCA-4310 CPM's block diagram.

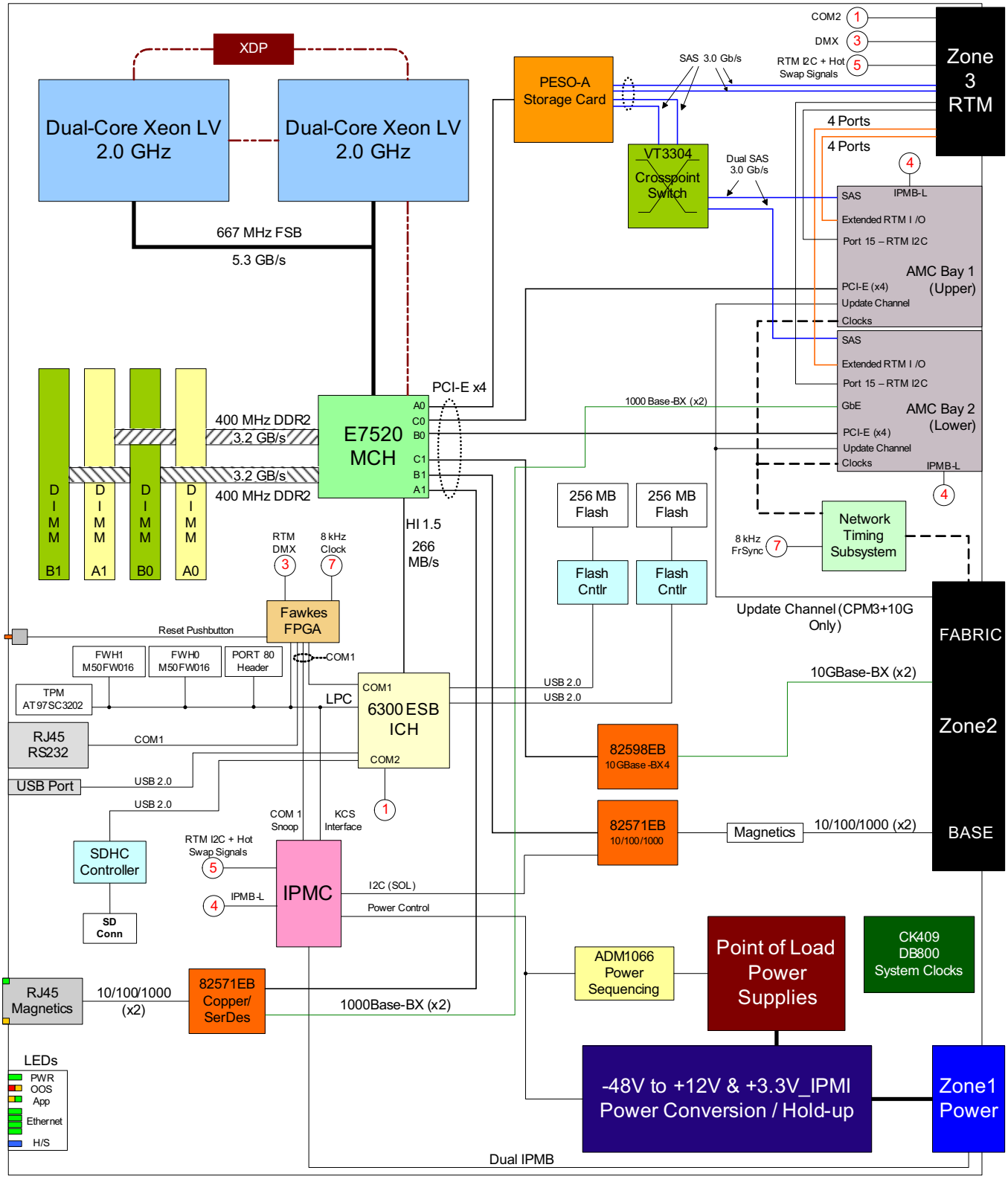
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Figure 3. ATCA-4300 CPM block diagram



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Figure 4. ATCA-4310 CPM block diagram



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COMPONENTS AND SUBSYSTEMS 3

This chapter provides information for the various components and subsystems used on the CPM.

Computer subsystem

The main components on the CPM are the dual processors and the memory controller hub (MCH) subsystem, which contains the MCH and the I/O controller hub (ICH). These three components are comprised in the CPM's central computer system and are detailed in the following sections.

Dual processors

The compute processing module has two CPUs with first-generation, dual-core processors for embedded and communications infrastructure applications. The CPM supports 1.67-GHz and 2.0-GHz 32-bit CPUs.

Each execution core has separate 32-KB L1 instruction and write-back data caches. A 2-MB L2 cache is shared between the execution cores. Data logic speculatively fetches data to the L2 cache before an L1 cache requests it, to reduce bus cycle penalties and increase performance.

The dual-core CPUs support Internet streaming using SIMD (Single Instruction Multiple Data) and are fully compatible with IA32 software. Streaming extensions (SSE2 and SSE3) are also supported. SSE3 instructions enhance the performance of optimized applications like video, image processing, and media compression.

The following table provides the various processors' specifications.

Table 2. Processor specifications

Processor	Frequency mode	Core voltage	Temp max TJ	Thermal design power (TDP)	Theoretical max power
1.67-GHz, Dual-Core Xeon ULV	HFM	1.0–1.2125 V	100° C	15 W	23.04 W
	LFM	0.825–1.1 V	100° C	13.1 W	17.05 W
2.0-GHz Dual-Core Xeon LV	HFM	1.125–1.25 V	100° C	31 W	45 W
	LFM	0.825–1.1 V	100° C	19.4 W	24.2 W

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Memory controller hub subsystem

The memory controller hub (MCH) is the bridge between the CPU bus interface, memory (DRAM) interface, and I/O hub interface on the CPM. Connecting the MCH to an ICH device provides legacy I/O features required by a platform server. In addition, the MCH implements three x8 PCI Express ports, each of which is divided into two separate x4 ports.

The MCH supports a 64-byte cache line size and two processors with a 333-MHz address bus and 667-MHz data bus. The MCH integrates the processor bus termination and is placed at one electrical and physical end of the daisy-chained bus. The MCH supports a 36-bit (64-gigabyte) address space.

The MCH provides an integrated memory controller for direct connection to two channels of registered DDR2-400 memory, single or dual ranked. The MCH supports single-channel operation using either of its memory channels. When both DDR channels are identically populated and operating, they can function in lock-step mode. The MCH uses a system bus and a memory bus for data transport. The MCH interacts with the PCI Express and ICH interfaces; it has the following features.

System bus

- System bus bandwidth of 5.3 GB/s
- 36-bit system bus addressing
- 12-deep in-order queue
- Dynamic bus inversion to improve signal integrity and minimize power consumption
- Parity protection for address response and data signals and address request

Memory bus

- 144-bit wide (lock-stepped, dual 72-bit wide), DDR2-400 memory interface with a total memory bandwidth of 6.4 GB/s
- Supports x72, error correction code (ECC), registered DDR2-400 using 256-megabit, 512-megabit, and 1-gigabit DRAMs
- Full operational support in 72-bit single-channel mode on either channel interface; lockstep support only for dual-channel operation
- Four DDR2 sockets, supporting up to 16 GB of total memory with 4-gigabyte DIMMs using 1-gigabit DRAMs
    - Support for ECC in dual-channel mode
    - Support for S4EC/D4ED x4 Single Device Data Correction (x4 SDDC) ECC in dual-channel mode

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PCI Express

- Support for three x8 port configuration interface, each x8 interface capable of logically dividing into separate x4 interfaces, each with half the bandwidth of an x8 interface
- Automatic wake-up and training of PCI Express ports after reset
- 32-bit CRC on all transaction layers with link-level retry on error
- 16-bit CRC with all link message information
- Hardware detection of hot-plug events supported at the PCI Express link level at ports B0 and C0

Hub interface 1.5

- Interface connection to the ICH

DIMMs

There are four DIMM sockets on the CPM that can hold up to four DDR2-400 registered DIMMs. For dual-channel DIMMs on parallel slots in the two memory channels to operate, they must have identical speed and CL values, sizes, and organization—single-rank or dual-rank. DIMMs within a memory channel can vary in size and organization. If you mix dual- and single-rank DIMMs, be sure to install the dual-rank DIMMS first (that is, in the slots furthest from the MCH).

For a higher performance rate, it is best to run DIMMs in dual-channel mode. Note that DIMMs must be populated as pairs to run in dual-channel mode. When not populated as pairs, the DIMMs run in single-channel mode. The pairs must have identical rank structure and the same capacity, device width (x4 or x8), and technology (such as 256-MB). Mixing of pairs is supported; however, a single x8 device failure is not correctable in SDDC mode.

The MCH supports 4-, 8-, 16-, 32-, and 64-KB page sizes and a burst length of 4, whether in single- or dual-channel mode. In dual-channel mode this results in eight 64-bit cycles (a full 64-byte cache line) from a single read or write. In single-channel mode two read or write cycles are required to access a cache line.

The MCH includes specialized hardware to support failover to a spare DIMM device in the event that an available primary DIMM exceeds a specified threshold of runtime errors. One of the DIMMs installed per channel is not used, but held in reserve. In the event of significant failures in a particular DIMM, it and its corresponding partner on the other channel will, over time, have its data copied to the spare DIMM held in reserve. When all the data has been copied, the reserve DIMM will become active, and the failing DIMM will be ignored. Only one sparing cycle is supported. If this feature is not enabled, then all DIMMs will be visible in normal address space.

Refer to *Installing DIMMs* on page 88 for instructions on inserting memory cards into the DIMM sockets.

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Memory ECC

The MCH only supports DIMMs with ECC. ECC reporting can be set up and controlled through the BIOS setup menus.

Supported DDR2-400 DRAM cards

The CPM includes four 25° 240-pin DDR2 sockets. The angled sockets allow standard height (1.18-inch) registered DIMMs to be installed. The following table lists the possible DIMM-types supported by the CPM.

Table 3. Supported memory cards

Module size	Memory component	Number of components	Component configuration	CAS latency	Module ranks
256 MB	256 Mbit	9	32 Mbit x 8	3	Single Rank
512 MB	256 Mbit	18	32 Mbit x 8	3	Dual Rank
512 MB	256 Mbit	18	64 Mbit x 4	3	Single Rank
512 MB	512 Mbit	9	64 Mbit x 8	3	Single Rank
1 GB	512 Mbit	18	64 Mbit x 8	3	Dual Rank
1 GB	512 Mbit	18	128 Mbit x 4	3	Single Rank
1 GB	1 Gbit	9	128 Mbit x 8	3	Single Rank
2 GB	512 Mbit	36	128 Mbit x 4	3	Dual Rank
2 GB	1 Gbit	18	128 Mbit x 8	3	Dual Rank
2 GB	1 Gbit	18	256 Mbit x 4	3	Single Rank
4 GB	1 Gbit	36	256 Mbit x 4	3	Dual Rank

I/O controller hub

The I/O controller hub (ICH) controls the USB ports, SATA ports, LPC bridge, and firmware hubs. These components are detailed in the next sections.

For information on accessing the storage devices in Linux, see *Access to storage devices from Linux* on page 41.

USB 2.0 ports and devices

The I/O controller hub controls the CPM's USB ports. The ATCA-4300 CPM has two USB connectors on the front panel, and the ATCA-4310 has one. The ATCA-4310 additionally supplies two USB flash devices and a socket for a removable USB secure digital (SD) card. See Figure 5 and Figure 6 on page 25.

The ICH contains an Enhanced Host Controller Interface (EHCI)–compliant host controller, which supports up to four high-speed USB 2.0 specification–compliant root ports. High-speed USB 2.0 allows data transfers up to 480 Mbps using the same pins as the four full-speed and low-speed USB Universal Host Controller Interface (UHCI) ports. The ICH contains port-routing logic that determines whether a USB port is controlled by one of the UHCI controllers or by the EHCI controller.

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Figure 5. ATCA-4300 USB 2.0 ports and devices

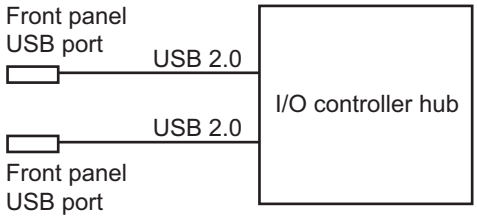
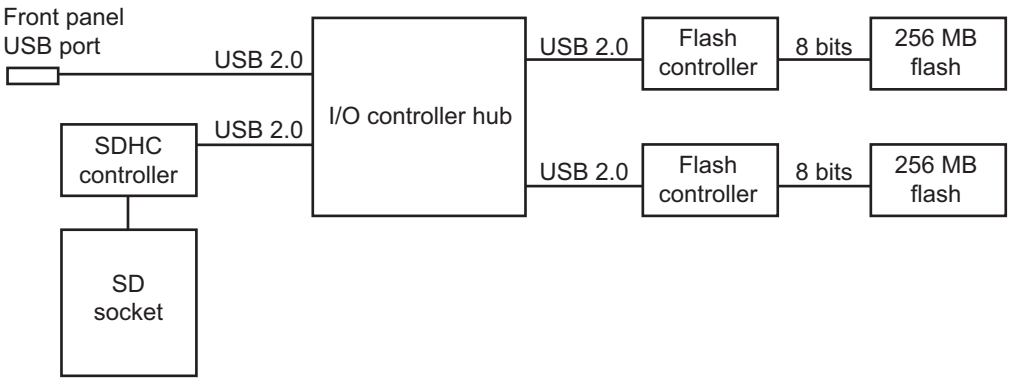


Figure 6. ATCA-4310 USB 2.0 ports and devices



Redundant USB flash devices (ATCA-4310 only)

The ATCA-4310 supplies two 256-MB flash devices for redundant storage. Each flash device is accessed over USB through a dedicated flash controller that provides an 8-bit data bus to the device. The devices are each organized as 256 MB x 8 bits.

Secure digital (SD) card socket (ATCA-4310 only)

The ATCA-4310 supports a removable SD flash memory card. A SDHC (secure digital high capacity, SD 2.0) controller provides access to the SD card socket over USB. SD cards with up to 8 GB of memory have been tested, and the controller is expected to support memory sizes up to the limit supported by the SD form factor.

You cannot insert or remove an SD card when the CPM is installed in a chassis. To identify the SD socket and latch locations, see Figure 17 on page 67. For instructions on inserting an SD card, see *Inserting an SD memory card (ATCA-4310)* on page 91.

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SATA ports

The I/O controller hub supplies two SATA ports that are supported by independent DMA controllers. Each ICH SATA port can transfer data at up to 150 MBps. These SATA ports are routed to the two AMC bays if the PESO-C daughter card is installed (available on the ATCA-4300 only). SATA AMC disks are also supported by the SAS controller if the PESO-A is installed. For more information, see *PCI Express storage option (PESO)* on page 31.

LPC bridge

The processors use the LPC bridge to read and write data to the LPC peripherals. The ICH LPC bridge implements the cycles listed in the following table.

Table 4. Supported LPC cycles

Cycle type	Comment
Memory Read	Single: 1 byte only
Memory Write	Single: 1 byte only
I/O Read	1 byte only; the ICH breaks up 16- and 32-bit CPU cycles into multiple 8-bit transfers
I/O Write	1 byte only; the ICH breaks up 16- and 32-bit CPU cycles into multiple 8-bit transfers
DMA Read	1 or 2 bytes
DMA Write	1 or 2 bytes
Bus Master Read	1,2, or 4 bytes
Bus Master Write	1,2, or 4 bytes

Firmware hubs

The CPM stores system BIOS in the two firmware hubs. The CPM also implements a redundant firmware hub (FWH) scheme, and in the event of a firmware failure the IPMC redirects the signal to access the backup hub. This is possible because firmware hubs are connected to the same interface, and the IPMC controls which hub is selected as primary or secondary using a GPO.

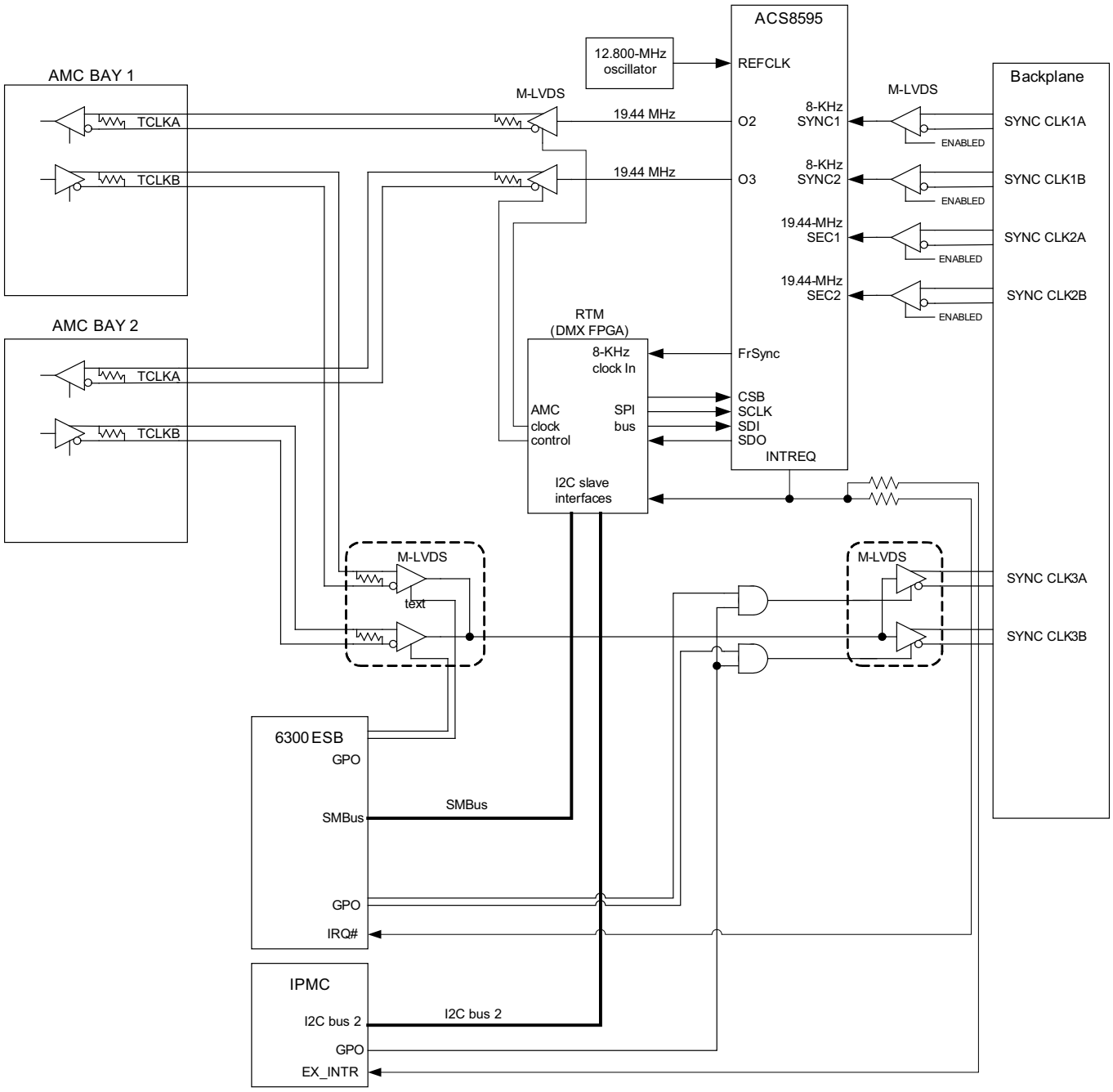
The FWHs can be programmed through software using the 'phlash' utility and a USB floppy disk, after you boot into DOS. A Linux-based 'reflash' utility will also be available for programming the FWHs. See *Upgrading the CPM system BIOS firmware* on page 92.

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Network timing subsystem

The network timing subsystem (NTS) can select reference timing sources from two pairs of synchronization bus inputs and can be configured with priority levels for each input. By monitoring each input, the NTS can automatically switch between valid sources based on those priorities. Figure 7 provides an overview of the operation of NTS.

Figure 7. Synchronization clock diagram



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Backplane CLK1 & CLK2 synchronization clocks

The CPM receives the CLK1A/B and CLK2A/B bused signals. The NTS can be programmed to provide a wide range of output frequencies, including the CLK2 input frequencies, to a clock buffer for each AMC bay. The differential output of each buffer is connected to the CLK1 input on each AMC bay, and a GPO from the custom FPGA controls their output enables. The CLK2A/B signals are connected to SEC inputs, and the CLK1A/B signals are connected to SYNC inputs on the NTS.

Backplane CLK3 synchronization clock

The CLK2 signals from either of the AMC bays can be configured to drive the CLK3A/B synchronization clock bus on the backplane. The multiplexer that selects which AMC bay drives the clock is controlled via GPOs on the ICH. The clock buffers to the synchronization CLK3A/B outputs are enabled or disabled by a GPO on the IPMC and AND'ed with GPOs on the ICH, allowing the IPMC to fully disable the CPM from driving the CLK3 bus. Permission to drive these signals comes from the system manager, through the IPMC, as part of E-Keying.

Trusted platform module

A trusted platform module (TPM) is located on the noncomponent side of the CPM. The TPM sits on the LPC bus and has the ability to assert an interrupt through the ICH interface.

The TPM is a secure key generator and key cache management device, supporting industry-standard cryptographic APIs. The TPM contains sufficient cryptographic functionality to generate, store, and manage cryptographic keys.

Real-time clock

A real-time clock (RTC) is implemented inside the I/O controller hub. This clock keeps track of the time of day and stores system data. When the CPM is powered down, the time and system data are maintained by a capacitor for up to two days.

SMBus controller

The ICH provides a SMBus 2.0–compliant host controller, as well as an SMBus slave interface.

The host controller provides a mechanism for the CPU to initiate communication with SMBus slave peripherals. The ICH is also capable of an operation mode in which it can communicate with I^2C-compatible devices.

The slave interface allows an external master to read from or write to the ICH. Write cycles can be used to cause certain events or pass messages; the read cycles can be used to determine the state of various status bits. The ICH's internal host controller cannot access the internal slave Interface.

The ICH SMBus consists of a transmit data path and host controller. The transmit data path provides the data flow logic needed to implement the seven different SMBus command protocols and is controlled by the host controller. The RTC clocks the ICH SMBus controller logic.

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The host controller's programming model has two segments: a PCI configuration and a system I/O mapping. All static configurations, such as the I/O base address, are configured via the PCI configuration space. Real-time programming of the host interface is done in system I/O space.

UARTs

The ICH has a serial I/O unit (SIU) that contains two compatible UARTs. The SIU communicates with the host CPUs through an LPC interface internally in the ICH. Each UART includes hardware flow control functionality and a programmable baud rate generator supporting data rates from 9600 to 115200 baud.

The CPM uses both UARTS from the ICH. COM1 is routed to a front-panel RJ-45 connector as a console port and is also used to implement the serial-over-LAN (SOL) feature. (See *Serial-over-LAN* on page 50 for more information.) COM2 is routed out to the RTM. The default configuration for both UARTs is 115200 Kbps, 8 bits, no parity, 1 stop bit, and no flow control, which can be changed in the system BIOS setup menus.

Ethernet controllers

Dual gigabit Ethernet controllers

The ATCA-4300 CPM provides six GbE ports and uses three Intel 82571EB dual gigabit Ethernet controllers. The ATCA-4310 CPM provides four GbE ports and uses two dual gigabit Ethernet controllers. Each Ethernet controller is connected to a x4 PCI Express port that provides a peak data bandwidth of 1 Gb/s in each direction. Each Ethernet controller has a private 128-KB EEPROM for storing initialization data and media access control (MAC) addresses. The controller has two fully integrated gigabit Ethernet MAC and PHY (physical layer) ports. These devices use the PCI Express architecture (revision 1.0a).

The Ethernet controller provides a standard Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications. Each port contains a SerDes (serializer-deserializer) interface to support 1000BASE-SX/LX (optical fiber) or 1000BASE-BX for gigabit backplane applications. In addition to managing MAC and PHY Ethernet-layer functions, the controller manages PCI Express packet traffic across its transaction, link, and physical/logical layers.

The on-board system management bus (SMB) ports enable network manageability implementations required by information technology personnel for remote control and alerting via the LAN. With SMB, management packets can be routed to or from the management processor.

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Dual 10-gigabit Ethernet controller (ATCA-4310 only)

The ATCA-4310 CPM additionally provides two 10-GbE ports and uses an Intel 82598EB dual 10-Gb Ethernet controller. The Ethernet controller is connected to a x4 PCI Express port that provides a peak data bandwidth of 2.5 Gb/s in each direction. The Ethernet controller has a private 128-KB EEPROM for storing initialization data and media access control (MAC) addresses. The controller has two fully integrated gigabit Ethernet MAC and XAUI ports. These devices use the PCI Express architecture (revision 1.1).

The Ethernet controller provides a standard SerDes Ethernet interface for 10GBASE-BX4 and 1000BASE-BX applications. In addition to managing MAC and PHY Ethernet-layer functions, the controller manages PCI Express packet traffic across its transaction, link, and physical/logical layers.

Zone 2 Base interface

One dual gigabit Ethernet controller is used to implement the Base interface for the CPM. The controller is configured to use the 10/100/1000 copper ports and is connected to the Base 1 and Base 2 ports.

Zone 2 Fabric interface

On the ATCA-4300, one dual gigabit Ethernet controller is used to connect to Fabric channels 1 and 2 on the Zone 2 connector. The controller is configured to use the 1000BASE-BX SerDes ports.

On the ATCA-4310, the10-gigabit Ethernet controller is used to connect to Fabric channels 1 and 2 on the Zone 2 connector. The controller is configured to use the 10GBASE-BX4 ports.

Front-panel Ethernet

There are two front-panel Ethernet connectors linked to the front Ethernet controller, which supports a dual gigabit copper interface. This connection is the same as the Base Ethernet connections on the backplane and can be used to connect directly to a network.

IPM controller

The IPMC is a general-purpose 32-bit microcontroller with sixteen 16-bit general registers. It can handle a 16-MB linear address space; it also contains 512 KB of embedded flash and 40 KB of RAM.

The IPMC microcontroller provides the only connection for the CPM out to the external ATCA shelf IPMBs. The controller implements six I^2C interfaces and provides for monitoring of the listed inputs and control of the listed outputs.

Several of the digital I/O pins are multiplexed with the other interfaces. Signal sensors are directly connected to the IPMC microcontroller as digital inputs. Output actuators are driven by IPMC microcontroller digital outputs, some of which are provided by the IPMC FPGA.

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PCI Express storage option (PESO)

The CPM supports a daughter card site to provide Fibre Channel or Serial Attached SCSI (SAS) storage.

PESO-A SAS controller

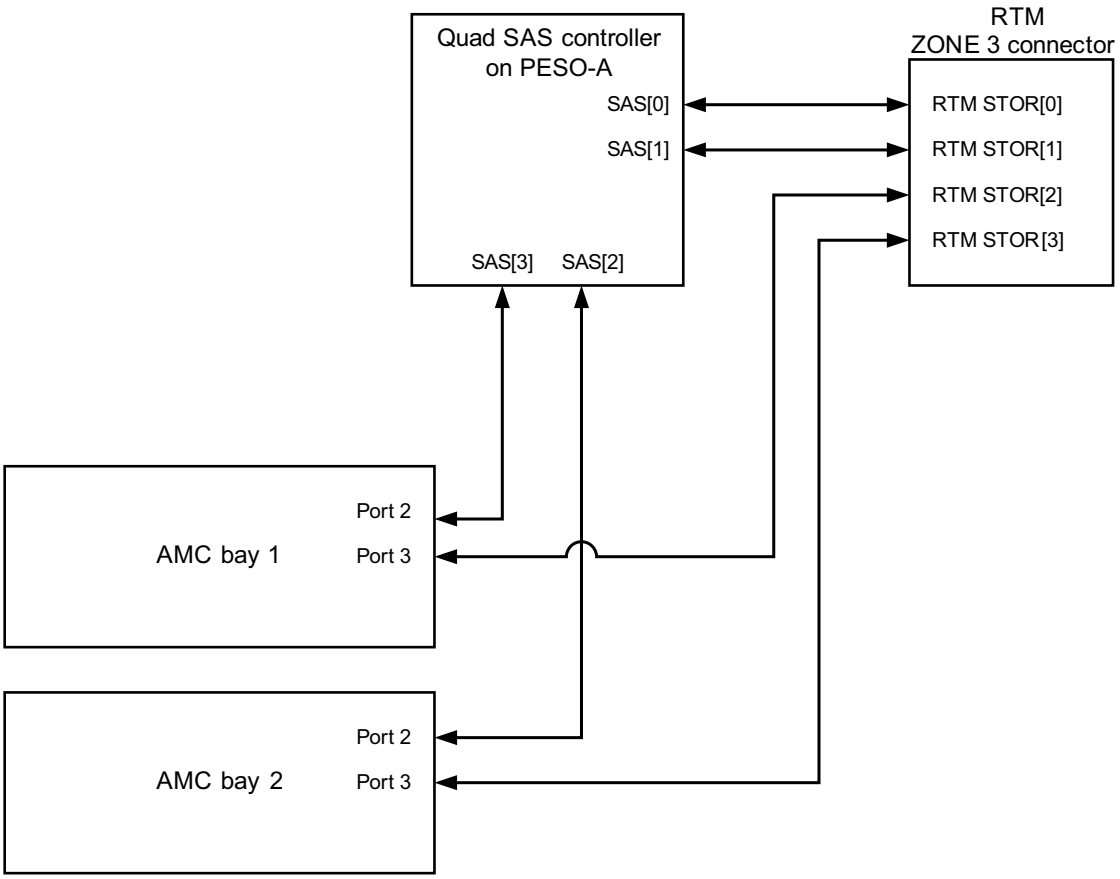
The PESO-A daughter card uses a four-port 3.0-Gbit/s SAS/SATA controller with a x4 PCI Express interface.

The PESO-A SAS controller transceivers perform conversions for SAS and SATA transfers. The transmitter accepts parallel data, changes it to serial data, and transmits it on the differential TX+/TX– signals. The receiver recovers the clock and deserializes the data from the bitstream that it receives on the RX+/RX– signals. Because the transmitter and receiver operate independently, the transceivers can send and receive data simultaneously.

SAS port connectivity with PESO-A

The following diagram shows SAS port connectivity on the CPM.

Figure 8. CPM SAS connectivity



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PESO-C Fibre Channel controller (ATCA-4300 only)

The PESO-C daughter card uses a Fibre Channel (FC) controller with a x4 PCI Express interface. The FC controller supports mass storage and IP protocols on a full-duplex 4-Gbit/s Fibre Channel link and SATA connectivity to the AMC sites. The PESO-C also routes the SATA ports from the I/O controller hub to the AMC bays. For information about the ICH SATA ports, see *SATA ports* on page 26.

Fibre Channel memory

The memory controller provides access to flash ROM and 32-bit synchronous SRAM and NVSRAM. It supports both interleaved and noninterleaved configurations up to a maximum of 16 MB of synchronous SRAM. A general-purpose memory expansion bus supports up to 1 MB of flash ROM.

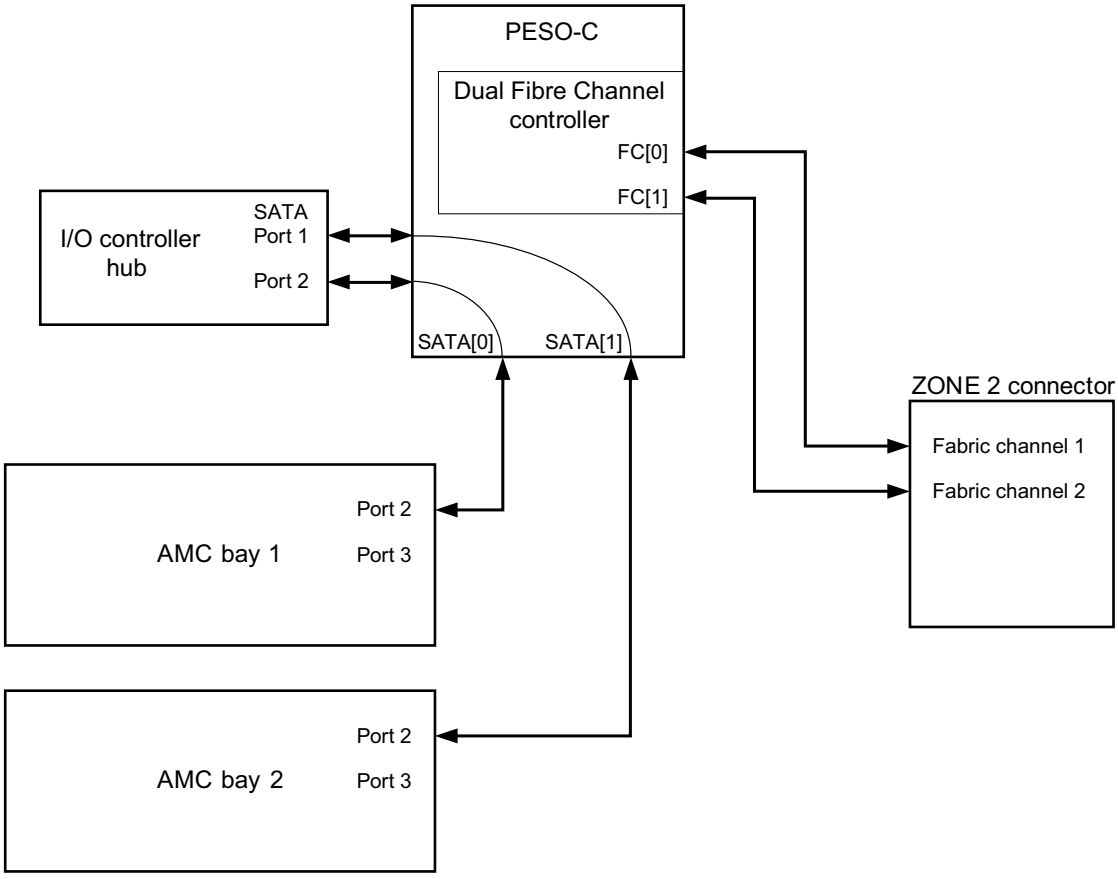
The primary function of SRAM is to store data structures used by the PESO-C controller, manage exchanges, and transmit and receive queues. The flash ROM is used for storing the firmware on the Fibre Channel controller, with1 MB allocated in ROM for firmware storage.

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SATA and Fibre Channel connectivity with PESO-C

The following diagram shows the PESO-C port connectivity on the CPM.

Figure 9. PESO-C Fibre Channel and SATA connectivity



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AMC bays

The CPM supports two Advanced Mezzanine Card (AMC) bays. Each bay is compliant with the AMC.0, AMC.1 (PCI Express), and AMC.3 (storage) PICMG specifications. Each bay on the ATCA-4300 is compliant with AMC.2 (Ethernet), but only bay 2 complies with AMC.2 on the ATCA-4310. Each bay supports midheight modules as defined by the AMC.0 specification.

The physical AMC bay locations on the CPM are B1 and B2. Each bay has basic and extended connector sections.

For the ATCA-4300, the basic section consists of the clocks, dual GbE (SerDes) ports, dual SAS/SATA ports, and a x4 PCI Express port. The extended section includes an update channel port, RTM control, and RTM extended I/O. On bay 2, the extended section also provides two additional GbE ports.

For the ATCA-4310, the basic section consists of the clocks, dual SAS/SATA ports, and a x4 PCI Express port. On bay 2, the basic section also provides two GbE (SerDes) ports. The extended section includes an update channel port, RTM control, and RTM extended I/O.

The CPM's IPMC provides IPM connectivity between the backplane IPMB and the AMC's local IPMB (IPMB-L). Depending on the software involved, the AMC bays may be addressed in any of the following ways:

	Physical bay 1	Physical bay 2
PICMG 3.0 commands	FRU 1	FRU 2
BIOS setup screens	Slot 1	Slot 2
AMC.0 site number	Site 5	Site 6
IPMB-L address	0x7A	0x7C

The Shelf Manager refers to the AMCs as bays 5 and 6, corresponding to the AMC.0 site numbers. Shelf Manager alarms pertaining to AMCs will use these numbers, and the HPI resource IDs will refer to sites 5 and 6. Other shelf managers may refer to the AMCs by their AMC.0 site numbers or FRU numbers.

When adding a AMC PCIe card, the ekey configuration file may require modification (see *Enabling Ethernet Ports using E-Keys* on page 57.)

AMC port mapping on the ATCA-4300 on page 35 and *AMC port mapping on the ATCA-4310* on page 36 provide locations of the AMC connections. Table 7 on page 37 describes AMC port interfaces. See the *Advanced Mezzanine Card Installation Guide* for installation instructions.

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Table 5. AMC port mapping on the ATCA-4300

	Port number	Function	
		AMC bay 1	AMC bay 2
Basic connector	TCLKA	Clocks (AMC.0)	
	TCLKB		
	FCLKA		
	0	GbE (AMC.2)	
	1		
	2	SAS/SATA to CPU (AMC.3)	
	3	SAS/SATA to RTM (AMC.3)	
	4	Type 4 x4 PCI Express (AMC.1)	
	5		
	6		
	7		
Extended connector	8	(no connect)	GbE (AMC.2)
	9		
	10	(no connect)	
	11		
	12	Update channel	
	13	(no connect)	
	14		
	15	Rear Transition Module control	
	16	(no connect)	
	17	Rear Transition Module access (AMC.0)	
	18		
	19		
	20		

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Table 6. AMC port mapping on the ATCA-4310

	Port number	Function	
		AMC bay 1	AMC bay 2
Basic connector	TCLKA	Clocks (AMC.0)	
	TCLKB		
	FCLKA		
	0	(no connect)	GbE (AMC.2)
	1		
	2	SAS/SATA to CPU (AMC.3)	
	3	SAS/SATA to RTM (AMC.3)	
	4	Type 4 x4 PCI Express (AMC.1)	
	5		
	6		
	7		
Extended connector	8	(no connect)	
	9		
	10		
	11		
	12	Update channel	
	13	(no connect)	
	14		
	15	Rear Transition Module control	
	16	(no connect)	
	17	Rear Transition Module access (AMC.0)	
	18		
	19		
	20		

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Table 7. AMC port interfaces

Identity	Function
Synchronization TCLKA	Synchronization TCLKA is driven to the AMC bays by the network timing subsystem on the CPM.
Synchronization TCLKB	The AMC modules drive synchronization TCLKB to the NTS_CLK3 clock selection circuitry on the CPM.
Synchronization FCLKA	Synchronization FCLKA is driven to the AMC bays by the 100-MHz PCI Express clock generator on the CPM.
Common option ports 0 and 1	On the ATCA-4300, ports 0 and 1 of both AMC bays connect to the Crosspoint switch on the CPM to set up Fabric port-1 and port-2 connections. On the ATCA-4310, ports 0 and 1 of AMC bay 2 connect to the CPUs through the Ethernet front panel controller.
Common option ports 2 and 3	Port 2 of the AMC bays connects to two SAS channels on the PESO. Port 3 of the AMC bay connects to the Zone 3 RTM connector. This provides storage interconnection between hard-drive AMC modules, the SAS controller on the PESO-A daughter card, and the RTM.
Fat Pipes ports 4, 5, 6, and 7	Ports 4 through 7 of the AMC bays connect to the MCH PCI Express ports (B0 for bay 1 and C0 for bay 2) on the CPM with a x4 PCI Express link.
Fat Pipes ports 8 and 9	On the ATCA-4300, ports 8 and 9 of AMC bay 2 connect to a Crosspoint switch for two additional 1000BASE-BX Ethernet Fabric port-1 and port-2 connections. On the ATCA-4310, ports 8 and 9 are not used.
Fat Pipes port 12	Port 12 of all AMC bays connects to differential buffers on the CPM that drive the backplane update channel interface. This allows direct interconnection between AMC modules on different CPM carrier blades. AMC bay 1 port 12 is connected to update channel 0; AMC bay 2 port 12 is connected to update channel 1.
Fat Pipes ports 13 and 14	Ports 13 and 14 are not used.
Fat Pipes port 15	Port 15 of the AMC bays connects to the Zone 3 connectors to the RTM. These interconnections provide I^2C interfaces from the AMC module to the RTM for SFP and LED control. The port is routed as a differential pair, allowing for future use as another high-speed channel.
Fat Pipes ports 17, 18, 19, and 20	Ports 17 through 20 of the AMC bays connect through the Zone 3 connector to the RTM. These interconnections provide four high-speed differential SerDes channels between each AMC module and the RTM.

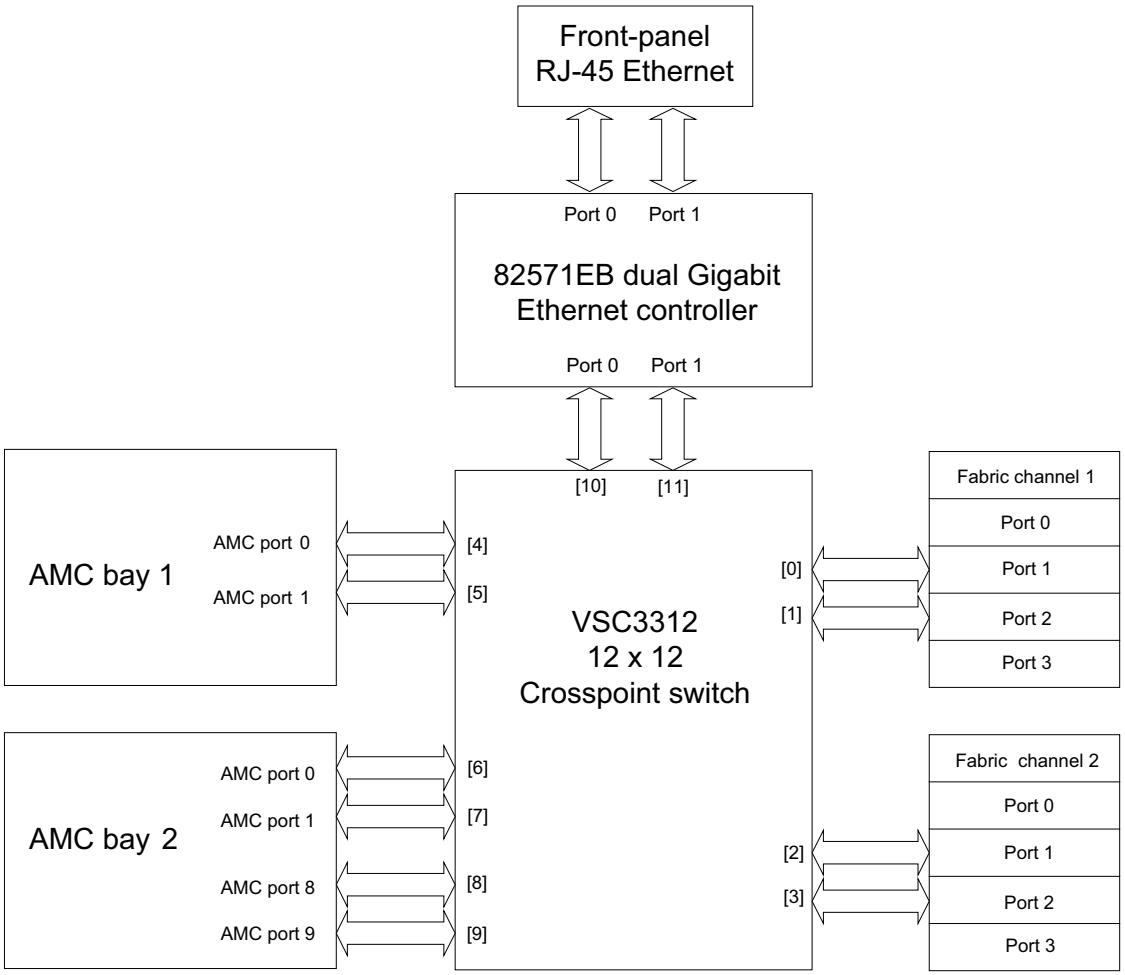
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Fabric Crosspoint switch (ATCA-4300 only)

A Crosspoint switch provides connectivity between the AMC bays, ports 1 and 2 on the Fabric channels, and the front dual Ethernet controller. The switch allows any input port to be connected to any output port. The IPMC programs the port connectivity and enables ports via the I^2C interface on the switch as part of the E-Keying process.

The CPM is preconfigured with the dual gigabit Ethernet controller routed to the front panel. Contact RadiSys for information about obtaining the CPM with the controller routed to the Crosspoint switch instead. The following figure shows both possible configurations.

Figure 10. Fabric Crosspoint switch connectivity



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Configuring Fabric Ethernet connectivity

The Intel® VSC3312 Crosspoint switch provides the ability to configure Ethernet connectivity by mapping Ethernet connections between AMCs, the backplane Fabric interface, and the payload processor. The switch's configuration is stored in the multirecord area of the CPM's FRU information. (See *OEM Ethernet Crosspoint switch #1 connectivity record (ATCA-4300 only)* on page 112.)

This record must be reprogrammed to set up connectivity different from the default. For example, you can use the RadiSys *hpiapp* sample application provided with the SCM to reprogram the multirecord area using the IDR commands. See the *Promentum Shelf Management Software Reference* for information on *hpiapp*.

Serial-port multiplexer

The COM1 serial port from the ICH is routed through the custom FPGA. The RS-232 transceiver provides a digital output that indicates when valid signal levels are present at the front-panel port; it is used for cable detection. If a serial cable is detected at the front panel, the serial port signals will connect directly (through level translators) to the RJ-45 serial connector on the front panel. Copies of the outgoing TX traffic and all the control signals from the ICH are routed to the IPMC for snooping. If the cable is not installed, the serial port signals connect directly to the IPMC for serial-over-LAN (SOL) communication. For more information, see *Serial-over-LAN* on page 50.

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System clocks

A clock generator provides host, chipset, and LPC peripheral clocks on the CPM. All of the CPM's system clocks are listed in the table below.

Table 8. System clocks

Clock name	No. of lines	Frequency	Voltage
DDR2 Command Clocks (Differential) DIMMs	8	200 MHz	1.8 V
Host Clocks (Differential) CPU0, CPU1	8	167 MHz	700 mV
SRC Clock (Differential)	2	100 MHz	700 mV
PCI-E (Differential)	14	100 MHz	700 mV
SATA (Differential) I/O Controller Hub (ICH)	2	100 MHz	700 mV
Hub Link Clocks Memory, ICH	2	66 MHz	3.3V
PCI Clocks ICH, FPGA, FWH0, FWH1, TPM, POST Header	6	33 MHz	3.3V
PCI-X Clocks ICH	2	66 MHz	3.3V
USB Clock ICH	1	48 MHz	3.3V

System reset

The CPM supports warm and cold system resets. A payload cold reset causes all circuitry, with the exception of IPMI circuitry, to be reset to a known initial state, clearing all sticky bits and initializing DRAM. A payload warm reset causes the CPUs to be initialized and resets all the PCI Express devices via their respective buses; the MCH and ICH are not reset, and the contents of DRAM are preserved across the payload warm reset.

Payload cold reset

A payload cold reset will reset the system board with the exception of IPMI circuitry. When a payload cold reset occurs, all devices and registers are reset to their default state. The MCH and CPU are also reset to defaults after a payload cold reset. After a payload cold reset, all data in DRAM is invalidated, and memory is then cleared during the system BIOS initialization.

A common cause of a payload cold reset is power failure; other causes include expiration of the watchdog timer interval, invocation of the FRU Control IPMI command with the Cold Reset option, and control by the user's own application software running on the processor.

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Power-on reset (POR)

A power-on reset occurs when any power supply on the CPM falls below its minimum threshold. A power-on reset is similar to a payload cold reset. The POR is active low.

Payload warm reset

A payload warm reset most frequently occurs when a user presses and releases the Reset button on the CPM front panel. A payload warm reset is used to initialize the PCI Express devices, the CPUs, and LPC devices, while maintaining the contents of DRAM. After a reset, the system BIOS checks to determine whether the reset is warm or cold. Either the system BIOS or OS code then sets the value to indicate a payload warm reset when the next payload warm reset occurs. Any memory data above 8 MB will remain intact during a payload warm reset.

The system BIOS keeps a warm reset counter to track the number of consecutive warm resets. On every consecutive warm boot the warm reset counter is decremented. If the warm reset counter goes to zero, the system BIOS asserts a payload cold reset.

Common causes of payload warm reset include activation of the front-panel reset button, invocation of the FRU Control IPMI command with the Warm Rest option, and control by the user's own application software running on the processor.

Access to storage devices from Linux

The CPM storage devices, such as the ATCA-4310 secure digital (SD) devices, may be accessible from Linux as formattable disk drives, depending on your operating system configuration. To make the SD devices accessible, your SCSI driver must have multiple LUN (logical unit number) support, which enables Linux access to the USB multi-card reader.

Device type naming

The Linux device type is determined by the type of physical device and, in some cases, the type of PESO installed. The names in the Linux file system may be */dev/sd<drive><partition>* for SCSI devices or */dev/hd<drive><partition>* for hard disks. USB and SAS devices are considered SCSI devices (*/dev/sd**).

Tip: SATA hard disk AMCs are named differently with PESO-A installed than with PESO-C. With PESO-A, they are considered SCSI devices (*/dev/sd**). With PESO-C, they are considered hard disks (*/dev/hd**). SAS disk drive AMCs are always considered SCSI devices.

See the *hd*(4) or *sd*(4) man pages for more information on device drivers.

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Order of device discovery and naming

The order in which Linux discovers the storage devices is the order that it assigns them alphabetical names, starting with the suffix "a". For example, the first SCSI device discovered is named */dev/sda*, and the second is named */dev/sdb*.

With PESO-A, the device types are generally discovered in this order:

1. SAS
2. SATA
3. USB (including the on-board USB flash devices on the ATCA-4310)

Note: With PESO-C, the order is not as significant, because SAS devices are not supported, and SATA and USB devices are treated as separate device types.

If two hard drive AMCs are installed when the CPM boots up, the AMCs are generally discovered in this order:

1. Bottom bay
2. Top bay

Tip: With PESO-C, the AMC in the bottom bay is always named */dev/hda*, and the top AMC is always named */dev/hdc.*

Identifying the assigned name for a specific device

To identify the drive name for a specific device, use the Linux command:

```
cat /proc/partitions
```

Look in the results for a drive size that closely matches the device.

To identify the SCSI devices by device model, use the command:

```
cat /proc/scsi/scsi
```

The devices are listed in order, starting with */dev/sda*.

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HARDWARE MANAGEMENT 4

The hardware management of the CPM is implemented by an Intelligent Platform Management Controller (IPMC). The functional blocks of the IPMC are as follows:

- Local hardware sensors for the CPM and RTM
- Local output actuator
- IPMC, comprising a microcontroller and an FPGA
- IPMBs
- Nonvolatile RAM
- AMC and RTM control and management

IPMC functionality

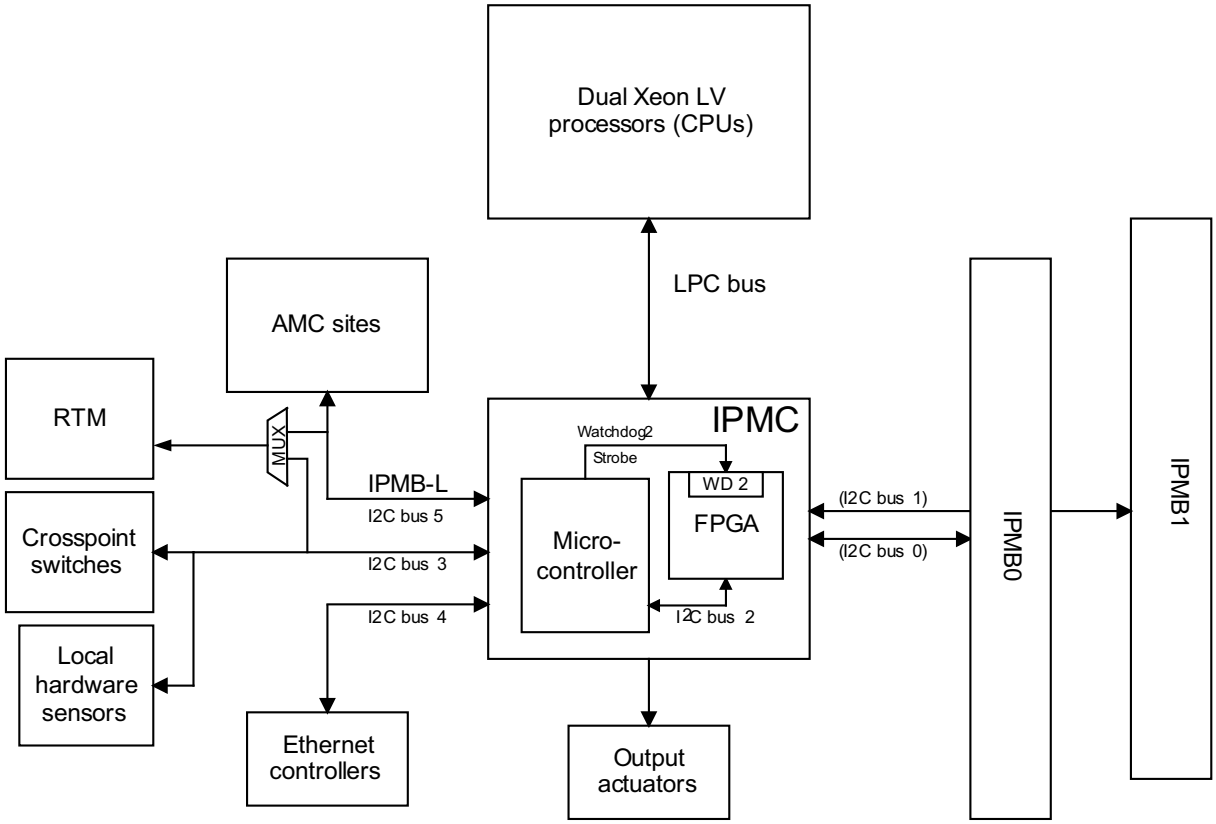
The controller interacts with the CPM's CPUs and the Shelf Manager. The main functions are to monitor temperature, voltage, and other sensors on the CPM. It is also responsible for controlling and monitoring the hot-swap process of the CPM and its AMCs and RTM. The IPMC interacts with the Shelf Manager to implement backplane E-Keying. It also manages onboard E-Keying for its AMCs and the RTM.

Using serial-over-LAN communications, the IPMC provides a remote user with access to the CPU serial console through the Base interface. For more information, see *Serial-over-LAN* on page 50.

The CPM's CPUs interface with the IPMC through a keyboard controller style (KCS) interface, which provides access to Intelligent Platform Management Interface (IPMI) functions. This allows the CPUs to send messages to the CPM's IPMC or to any other management controller in the shelf.

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Figure 11. IPMC block diagram



Payload processor interface

The payload processor interface allows the on-board Intel processor to communicate with the IPMC. The CPM implements this interface as a KCS port, which is similar to how a PC motherboard processor sends commands to a legacy PC-compatible keyboard controller. The IPMC is connected to the payload LPC bus and responds to I/O byte addresses as a KCS interface.

The CPM uses the serial IRQ output of the IPMC to implement the messaging interrupt for the payload. The IPMC uses the serial IRQ output to generate a legacy interrupt IRQ6 to the payload processor. During use of the KCS interface by the payload processor, output buffer full (OBF) conditions generate this interrupt to the payload if the IPMI driver on the payload processor is in interrupt-enabled mode.

The system BIOS- and OS-level code uses this interface to interact directly with the IPMC. With OS packages that support OpenIPMI, the OpenIPMI driver and toolset are available to make it easier to write applications accessible to the IPMC or IPMI subsystem in the shelf. The CPM KCS interface is compatible with OpenIPMI.

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Device ID information

The IPMC contains unique identification information. Use the 'Get Device ID' command to access most of the Device ID information; the remainder of the information is contained in the sensor data records (SDRs) on the IPMC. The information in the table below describes those identifiers.

Table 9. ID Information

Field	Storage location	Value
Device Name	SDR	`ATCA-4300` *or* `ATCA-4310`
Device ID	'Get Device ID' response	0x011
Firmware Version	'Get Device ID' response	*current firmware version in format XX.YY*
IPMI Version	'Get Device ID' response	1.5
IPM Support	'Get Device ID' response	0x02D
Product ID	'Get Device ID' response	0x0B5C for ATCA-4300 or 0x1459 for ATCA-4310
Manufacturing ID	'Get Device ID' response	4337

Sensors

The IPMC sensors monitor voltages, temperatures, control signals, and status events. IPMI events associated with these sensors are generated by the IPMC, based on state changes of the sensors.

The CPM supports a variety of sensors, each with entries in the SDR. The CPM implements a Type 0x12 record for the management controller and Type 0x01 records for the full sensor descriptions. Standard IPMI commands read these sensors from the SDR description.

See *Managed sensors* on page 115 for a list of sensors managed by the CPM.

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Hot swap

Hot swaps of managed FRUs are done in accordance with hot swap requirements defined in the PICMG 3.0 Revision 2.0 *AdvancedTCA Base Specification*. The Shelf Manager controls the hot-swap process, and the IPMC enables and disables payload power to the managed FRUs when instructed by the Shelf Manager. For the CPM, the managed FRUs are the AMCs and the RTM.

AMC hot swap

The IPMC is responsible for enabling power to the AMC bays and determining the functionality through E-Keying. AMC FRU E-Key records are used to indicate the types of connections supported by the installed AMCs. For information on the types of connections supported by the CPM, refer to *AMC bays* on page 34 or *AMC port mapping on the ATCA-4310* on page 36.

AMCs that make use of a PCI Express connection to the CPM are handled in a special way. The memory controller hub (MCH) supports PCI Express hot swap and participates in PCI Express link training. A hot swap is enabled by the system BIOS and IPMC working in conjunction to allow an AMC to be added to or removed from the system without powering down or resetting the CPM.

RTM hot swap

When the RTM is inserted and the RTM latch is closed, a signal to the IPMC enables the I^2C bus to the RTM. The RTM will be enabled when the IPMC detects a supported RTM via the FRU EEPROM. The IPMC will configure the I/O expander on the RTM via the I^2C bus, and then enable the payload to the Zone 3 RTM connector. For hot removal of the RTM, the ejector latch is opened, asserting EJECT to the IPMC. The blue hot-swap LED will begin blinking as soon as the EJECT assertion is seen by the IPMC. When the Shelf Manager is ready, the IPMC will keep the blue hot-swap LED on, indicating that the payload is disabled and that the RTM is ready to be removed.

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IPMI-over-LAN

The IPMC is remotely accessible through the Base Ethernet ports using IPMI-over-LAN. The CPM implements IPMI-over-LAN using RMCP and RMCP+ as described in the IPMI 2.0 specification. IPMI-over-LAN access enables the capability described in *Serial-over-LAN* on page 50.

Configuring IPMI-over-LAN access

You must configure each CPM initially to make IPMI-over-LAN access available. The IPMC saves the configuration changes in non-volatile RAM so they are not lost during reboots, hot swaps, or firmware upgrades.

Before you begin

1. Gather the following resources:
   - A remote computer with network access to the Shelf Manager in the shelf with the CPM.

     Note: The initial steps can be run directly on the CPM's CPU as an alternative.
   - An *ipmitool* utility (available from RadiSys or as open source).
2. Be prepared to fill in values for these variables:

`<ShMgr_IP>`	The IP address of the Shelf Manager.
`<IPMB>`	The IPMB address of the CPM in the shelf.
`<channel>`	The IPMI channel number that represents a CPM Base interface channel. Channel 02 represents the Base interface channel that connects to the hub module in the lower-numbered slot, and channel 03 connects to the hub module in the higher-numbered slot.
`<IP>`	The static IP address to assign to each CPM Base interface channel.
`<protocol>`	The protocol to use (`lan` for RMCP or `lanplus` for RMCP+). The configuration steps need to be done only once and apply to both protocols.

IPMI-over-LAN basic configuration steps

From the Linux prompt:

1. Set the IP address for a Base interface channel:

   `ipmitool -I lan -H <ShMgr_IP> -A none -t <IPMB> lan set <channel> ipaddr <IP>`

   Tip: To run the commands directly on the CPM's CPU, omit the `-I`, `-H`, `-A`, and `-t` options. This would shorten the above command to:

   `ipmitool lan set <channel> ipaddr <IP>`

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2. Repeat step 1 to set the IP address of the other channel.
3. View the current settings for each channel:

   ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **lan print** *<channel>*

4. Verify IPMI-over-LAN access by displaying the system event log (SEL).

   ipmitool -I lanplus -H *<IP>* **-A none -C 0 sel**

   Important: You must do this step from a remote computer to verify IPMI-over-LAN access.

   SEL information should be displayed, which verifies access to IPMI services without relying upon the Shelf Manager. Verifying "lanplus" access also verifies "lan" access.

   If this command does not display SEL information or gives an error, perform the steps in *IPMI-over-LAN additional configuration steps* on page 48.

5. Repeat step 4 to verify access to the IP address of the other channel.

IPMI-over-LAN additional configuration steps

If IPMI-over-LAN does not work after you performed the basic steps:

1. Set the user privileges for both channels:

   ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **user priv 1 4 2**

   ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **user priv 2 4 2**

2. Set the channel and administrator access for a channel:

   ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **raw 06 0x40** *<channel>* **0x42 0x44**

   ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **raw 06 0x40** *<channel>* **0x82 0x84**

   ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **channel getaccess** *<channel>* **01**

   ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **channel setaccess** *<channel>* **01 ipmi=on link=on privilege=4**

3. Repeat step 2 to set access to the other channel.
4. Verify IPMI-over-LAN access by displaying the SEL.

   ipmitool -I lanplus -H *<IP>* **-A none -C 0 sel**

   SEL information should be displayed. If this command does not display SEL information or gives an error, see *IPMI-over-LAN troubleshooting steps* on page 49.

5. Repeat step 4 to verify access to the IP address of the other channel.

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IPMI-over-LAN troubleshooting steps

1. View the current settings for a channel:

   ipmitool -I <*protocol*> **-H** <*ShMgr_IP*> **-A none -t** <*IPMB*> **lan print** <*channel*>

2. Verify that the IP address is correct.
3. Verify that a non-zero MAC address is set.

   A MAC address of 0x00 indicates that the Ethernet controller is not responding to queries. This can occur if the Ethernet controller does not have the correct EEPROM file. Upgrade the Base interface EEPROM image using the image file and instructions from the RadiSys software distribution.

4. Repeat steps 1–3 to check the settings for the other channel.

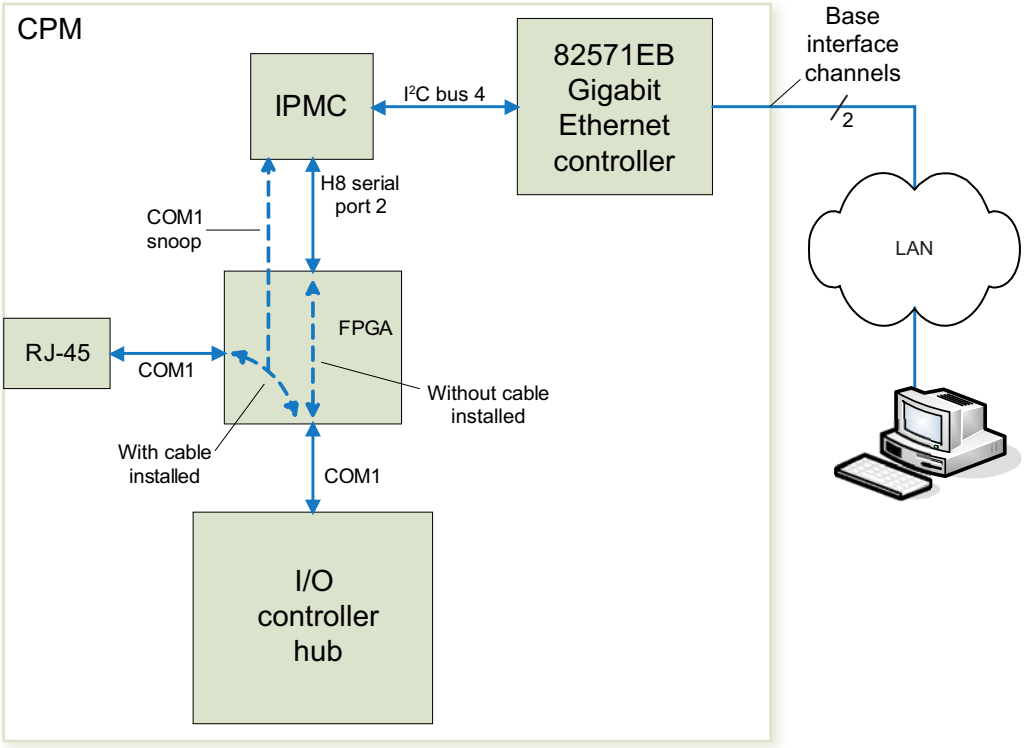
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Serial-over-LAN

Serial-over-LAN (SOL) is the specification of packet formats and protocols for transmitting serial data over a LAN using IPMI-over-LAN packets. SOL operation is conceptually straightforward. A remote management application can establish an IPMI-over-LAN session with the IPMC. After the session is established, the remote console can request that the SOL session be activated.

The remote user has read-only access to the serial console when a cable is plugged into the front panel serial port, and has read/write access otherwise. When a cable is attached, all COM1 signals are connected through voltage-level translators to the RJ-45 serial port connector, and the IPMC snoops the traffic. When the cable is not attached, all the COM signals are routed directly to the IPMC. See Figure 12.

Figure 12. Serial-over-LAN



In SOL mode, any outgoing characters from COM1 from the ICH are assembled into packets by the IPMC and sent to the remote console over one of the Base LAN interfaces. Conversely, in-bound LAN packets carrying characters for the system serial controller have their character data extracted by the IPMC and delivered to the baseboard serial controller. The SOL character data is contained in SOL messages carried in UDP datagrams. The packet format is "IPMI v2.0 RMCP+" with the Payload Type set to "SOL".

The CPM supports one SOL session at a time. The session must be closed before another session, such as through the other Base interface channel, can be opened.

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Establishing a SOL session

Prerequisite: This procedure assumes that the required setup for IPMI-over-LAN has been done once for this CPM. For details, see *Configuring IPMI-over-LAN access* on page 47.

One-time SOL configuration steps

Important: For these one-time steps, you must use the RadiSys-supplied *ipmitool* utility.

To configure retry settings from a remote computer:

1. Configure the retries to keep SOL sessions open for a Base interface IP address:

   ipmitool -I <*protocol*> **-H** <*IP*> **-A none -C 0 sol set retry-interval 0xF0**

   ipmitool -I <*protocol*> **-H** <*IP*> **-A none -C 0 sol set retry-count 7**

   For an explanation of **<*protocol*>** and **<*IP*>**, see *Before you begin* on page 47.

2. Repeat step 1 to configure retries for the other Base interface IP address.
3. View the retry settings for a Base interface IP address:

   ipmitool -I <*protocol*> **-H** <*IP*> **-A none -C 0 sol info**

   The Retry Count should be 7, and the Retry Interval should be 2400 ms.

4. Repeat step 3 to verify access to the IP address of the other Base interface channel.

SOL session open steps

To open a SOL session from a remote computer:

1. Activate the SOL console window:

   ipmitool -I <*protocol*> **-H** <*IP*> **-A none -C 0 sol activate**

   The SOL session is established. If a cable is attached to the CPM front panel serial port, the SOL window is read-only. It is read-write if no cable is attached.

2. Perform an action (such as pressing Enter) from the local serial console if a serial cable is attached, or from the SOL console window if no cable is attached.

   The SOL console window should respond.

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SOL session close step

Note: Only one SOL session can be open at a time to a single CPM.

To terminate a SOL session directly from the active SOL window, enter these characters:

```
~.
```

To terminate a SOL session from another window, enter:

```
ipmitool -I <protocol> -H <IP> -A none -C 0 sol deactivate
```

BIOS access over SOL

A SOL session can be used to remotely enter the BIOS setup screen. Two key considerations when using SOL for this purpose are:

- The BIOS shuts down and brings up the Ethernet interface during reboot which can result in dropped SOL sessions. The recommended SOL session timeout value (**`retry-interval`** and **`retry-count`** in the procedure above) generally allows the session to be re-established without user intervention.
- Linux *init* scripts generally shut down Ethernet interfaces during OS shutdown or reboot. This increases the time that the interface is down beyond the *max session* timeout values that can be set. Removing the links */etc/raid/rc2.d/K*network* and */etc/raid/rc6.d/K*network* prevents the OS from shutting down these interfaces.

Nonvolatile RAM

The CPM hardware supports 32 KB of nonvolatile RAM (NVRAM) divided into partitions as shown in Table 10.

Table 10. CPM nonvolatile RAM mapping

Description	Size	Offset range
IPMC Boot Information (16 bytes)	16 bytes	0x0000–0x0010
FRU Information Area (2 KB)	2032 bytes	0x0010–0x0800
SEL Storage Area (26 KB)	26,624 bytes	0x0800–0x7000
SDR Storage (0.5 KB)	512 bytes	0x7000–0x7200
Reset Recovery Data-Sensors (1.5 KB)	1536 bytes	0x7200–0x7800
Reset Recovery Data-FRUs (2 KB)	2048 bytes	0x7800–0x8000

For details on the contents of the partitions, refer to *FRU Information Areas* on page 111.

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Backplane and AMC interface control (E-Keying)

Electronic Keying (E-Keying) control is used to verify interface compatibility, prevent damage to hardware, and prevent misoperation. The Shelf Manager collects E-Key records that describe the Fabric, Base, update channel, and synchronization clock Interfaces implemented by the shelf and other boards in the system. The PICMG 3.0 Revision 2.0 *AdvancedTCA Base Specification* requires the CPM to support E-Key control by describing its backplane interfaces to the Shelf Manager. For some interfaces, the CPM can respond to Shelf Manager commands by isolating the interfaces from the backplane.

The CPM does not support isolation of the Base Ethernet ports or of some Fabric Ethernet ports; however, CPM ports operate as expected only if the corresponding ports that connect to them through the backplane are enabled. The CPM supplies point-to-point records for all its backplane ports.

For the ATCA-4310 Fabric interface, both 10-Gb Ethernet channels are always enabled. For the ATCA-4300 Fabric interface, the IPMC can enable and disable ports 1–3 of each Fabric channel, but port 0 is always enabled. When the CPM powers up, the IPMC disables Fabric ports 1–3 by reprogramming the Fabric Crosspoint switch (used for Ethernet connections on ports 1 and 2 to the AMCs) or by disabling the high-speed buffers (used for a Fibre Channel connection on port 3 to the PESO card). The IPMC communicates its board point-to-point records to the Shelf Manager and receives permission to enable each Fabric port that is compatible with the corresponding hub module port. The IPMC then compares the point-to-point record of each on-board AMC or PESO card interface with the CPM Fabric port to which it is routed. If the AMC or PESO interface is compatible with the corresponding Fabric port, the IPMC verifies that the Shelf Manager previously granted permission to enable that Fabric port. If so, the IPMC enables the Fabric port.

The update channel connections between the AMC bays and the Zone 2 connector can be disabled by the IPMC, which uses GPIOs to disable the LVDS buffers. The update channel is considered to be a high-speed connection between CPM AMC bays in adjacent slots in the backplane.

The IPMC and CPUs can disable the CLK3 connection between the CPM and the CLK3A and CLK3B buses on the backplane.

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The following tables list the entities that provide E-Key control for each channel and port of the Fabric interface, update channel, and synchronization clocks.

Table 11. ATCA-4300 Fabric interface I/O E-Key descriptions

Fabric channel	Port 0 control	Port 1 control	Port 2 control	Port 3 control	Comments
1	N.A.	IPMC	IPMC	IPMC	Ports 1 and 2 are connected through the Fabric Crosspoint switch to the AMC bays Port 3 (Fibre Channel) is connected through the PESO Crosspoint switch to the PESO daughter card
2	N.A.	IPMC	IPMC	IPMC	

Table 12. ATCA-4310 Fabric interface I/O E-Key descriptions

Fabric channel	Port 0 control	Port 1 control	Port 2 control	Port 3 control	Comments
1	N.A.	N.A.	N.A.	N.A.	Connected through an Ethernet controller to the CPUs
2	N.A.	N.A.	N.A.	N.A.	

Table 13. Update channel and synchronization clock E-Key descriptions

Channel	Controlled by	Comments
Update channel port 0	IPMC	AMC bay 1 port 12 through high-speed buffer
Update channel port 1	IPMC	AMC bay 2 port 12 through high-speed buffer
Synchronization clock 1A	N.A.	8-KHz clock input from backplane
Synchronization clock 1B	N.A.	8-KHz clock input from backplane
Synchronization clock 2A	N.A.	19.44-MHz clock input from backplane
Synchronization clock 2B	N.A.	19.44-MHz clock input from backplane
Synchronization clock 3A	IPMC, CPU	AMC synchronization clock output to backplane IPMC has global control of whether clocks are driven CPM has control of which clock (CLK3A or CLK3B) is driven
Synchronization clock 3B	IPMC, CPU	AMC Synchronization clock output to backplane IPMC has global control of whether clocks are driven CPM has control of which clock (CLK3A or CLK3B) is driven

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As an AMC carrier, the CPM IPMC works with the AMC's module management controller (MMC) to match the ports on the AMC's B+ connector to the corresponding CPM ports. The IPMC or MMC can disable many of the ports that are not compatible. The following tables list the entities that provide E-Key control for each AMC port on the ATCA-4300 and ATCA-4310.

Table 14. ATCA-4300 AMC B+ connector port E-Key descriptions

Channel	Controlled by	Comments
AMC bay 1 port 0	IPMC	Connected to Crosspoint switch
AMC bay 1 port 1	IPMC	Connected to Crosspoint switch
AMC bay 1 port 2	N.A.	Connected to CPUs through SAS/SATA
AMC bay 1 port 3	N.A.	Connected to RTM through SAS/SATA
AMC bay 1 port 4	N.A.	Connected to CPUs through PCI Express to MCH
AMC bay 1 port 5	N.A.	Connected to CPUs through PCI Express to MCH
AMC bay 1 port 6	N.A.	Connected to CPUs through PCI Express to MCH
AMC bay 1 port 7	N.A.	Connected to CPUs through PCI Express to MCH
AMC bay 1 port 12	IPMC	Connected through high-speed buffer to update channel port 0
AMC bay 1 port 15	MMC	Connected to RTM
AMC bay 1 port 17	MMC	Connected to RTM
AMC bay 1 port 18	MMC	Connected to RTM
AMC bay 1 port 19	MMC	Connected to RTM
AMC bay 1 port 20	MMC	Connected to RTM
AMC bay 2 port 0	IPMC	Connected to Crosspoint switch
AMC bay 2 port 1	IPMC	Connected to Crosspoint switch
AMC bay 2 port 2	N.A.	Connected to CPUs through SAS/SATA
AMC bay 2 port 3	N.A.	Connected to RTM through SAS/SATA
AMC bay 2 port 4	N.A.	Connected to CPUs through PCI Express to MCH
AMC bay 2 port 5	N.A.	Connected to CPUs through PCI Express to MCH
AMC bay 2 port 6	N.A.	Connected to CPUs through PCI Express to MCH
AMC bay 2 port 7	N.A.	Connected to CPUs through PCI Express to MCH
AMC bay 2 port 8	IPMC	Connected to Crosspoint switch
AMC bay 2 port 9	IPMC	Connected to Crosspoint switch
AMC bay 2 port 12	IPMC	Connected through high-speed buffer to update channel port 1
AMC bay 2 port 15	MMC	Connected to RTM
AMC bay 2 port 17	MMC	Connected to RTM
AMC bay 2 port 18	MMC	Connected to RTM
AMC bay 2 port 19	MMC	Connected to RTM
AMC bay 2 port 20	MMC	Connected to RTM

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Table 15. ATCA-4310 AMC B+ connector port E-Key descriptions

Channel	Controlled by	Comments
AMC bay 1 port 2	N.A.	Connected to CPUs through SAS/SATA
AMC bay 1 port 3	N.A.	Connected to RTM through SAS/SATA
AMC bay 1 port 4	N.A.	Connected to CPUs through PCI Express to MCH
AMC bay 1 port 5	N.A.	Connected to CPUs through PCI Express to MCH
AMC bay 1 port 6	N.A.	Connected to CPUs through PCI Express to MCH
AMC bay 1 port 7	N.A.	Connected to CPUs through PCI Express to MCH
AMC bay 1 port 12	IPMC	Connected through high-speed buffer to update channel port 0
AMC bay 21 port 15	MMC	Connected to RTM
AMC bay 1 port 17	MMC	Connected to RTM
AMC bay 1 port 18	MMC	Connected to RTM
AMC bay 1 port 19	MMC	Connected to RTM
AMC bay 1 port 20	MMC	Connected to RTM
AMC bay 2 port 0	IPMC	Connected to CPUs through front panel Ethernet controller
AMC bay 2 port 1	IPMC	Connected to CPUs through front panel Ethernet controller
AMC bay 2 port 2	N.A.	Connected to CPUs through SAS/SATA
AMC bay 2 port 3	N.A.	Connected to RTM through SAS/SATA
AMC bay 2 port 4	N.A.	Connected to CPUs through PCI Express to MCH
AMC bay 2 port 5	N.A.	Connected to CPUs through PCI Express to MCH
AMC bay 2 port 6	N.A.	Connected to CPUs through PCI Express to MCH
AMC bay 2 port 7	N.A.	Connected to CPUs through PCI Express to MCH
AMC bay 2 port 12	IPMC	Connected through high-speed buffer to update channel port 1
AMC bay 2 port 15	MMC	Connected to RTM
AMC bay 2 port 17	MMC	Connected to RTM
AMC bay 2 port 18	MMC	Connected to RTM
AMC bay 2 port 19	MMC	Connected to RTM
AMC bay 2 port 20	MMC	Connected to RTM

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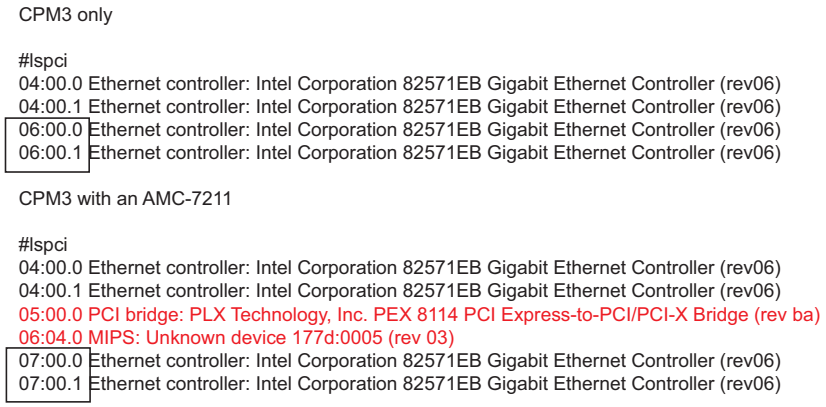
Enabling Ethernet Ports using E-Keys

The PICMG 3.0 Revision 2.0 *AdvancedTCA Base Specification* requires that ports are enabled and disabled when E-key port commands are sent from the Shelf Manager. For Ethernet ports on the CPM, this is supported by the E-key daemon, included in the Linux support package.

When the Shelf Manager enables or disables ports on the CPM, the IPMC sends messages to the OS. The E-key daemon listens for these through the openIPMI interface and enables or disables the appropriate Ethernet ports based on the message. The application behavior is controlled by the */etc/ekeymon.conf* configuration file. This configuration file identifies which PCIbus device and function should be enables or disabled when E-key events are received.

If a PCIe AMC card is installed on the CPM, the values of the Ethernet controller PCIbus numbers may increase depending on the number of buses, if any, required by the AMC. *Figure 13* illustrates an example showing the Fabric Ethernet controller PCIbus numbers changing from 06 to 07 after the AMC is added. The resulting change requires modifying the E-Key daemon configuration file to reflect the new Ethernet controller PCIbus numbers.

Figure 13. Ethernet controller PCIbus number changes



Note: The E-Key daemon is currently only supported under WindRiver PNE-LE-1.4. If using other Linux versions, contact Technical Support.

To modify the *ekeymon.conf* file:

1. Open the *ekeymon.conf* file.
2. Scroll to the *Fabric Ethernet Monitors* section.
3. Replace the existing PCIbus numbers to reflect the new values after the PCIe card addition(s). Replace the ***V*** below with a new number.

```
# Fabric Ethernet Monitors

/usr/sbin/ethchannel $s 0V:00.0 :or:0x10000100:0x10000102
/usr/sbin/ethchannel $s 0V:00.1 :or:0x10000100:0x10000103
```


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4. Restart the E-Key daemon using one of the following methods:

- **`$ /etc/init.d/ekeyd restart`**
- **`$ service ekeyd restart`**

Example

The following example reflects the configuration file change based on *Figure 13*.

CPM3 only

```
# Fabric Ethernet Monitors

/usr/sbin/ethchannel $s 06:00.0 :or:0x10000100:0x10000102
/usr/sbin/ethchannel $s 06:00.1 :or:0x10000100:0x10000103
```

CPM3 after adding the AMC-7211

```
# Fabric Ethernet Monitors

/usr/sbin/ethchannel $s 07:00.0 :or:0x10000100:0x10000102
/usr/sbin/ethchannel $s 07:00.1 :or:0x10000100:0x10000103
```


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REAR TRANSITION MODULE 5

The function of the rear transition module (RTM) is to provide additional connectivity to the CPM. Since the RTM is not a standalone device, it must be connected to the CPM front module through the Zone 3 connector in order to operate.

RTM functionality

The RTM contains connectors for various signals through its front panel and communicates with the main board via the Zone 3 connector. It can be used with the CPM or any other unit in a general purpose slot that supports the CPM-RTM Zone 3 pin map. The SAS lines provide storage linkage between two front CPMs, each of which may contain up to two hard-drive AMCs. These signals are buffered for signal integrity assurance on the RTM by an 8x8 SAS driver with out-of-band signaling. The SAS driver does not require any programming to initialize; buffered SAS signals are initiated upon proper power-up. One side of the RTM consists of SAS differential pairs attached to the front blade by the Zone 3 connector; the other side includes the SAS differential pairs driven between the RTM and a second CPM-RTM combination through the alarm signaling port. Two SAS pairs are connected with an LSI SAS controller on the front module's CPM PESO-A card; the other two directly connect with each occupied AMC slot located on the front module. The SAS channels function only with the PESO-A installed on the CPM.

The serial port (COM2) on the CPM's I/O controller hub is routed to an RJ-45 jack on the RTM to save board space on the front module. The serial port may be used in addition to the serial port located on the main module.

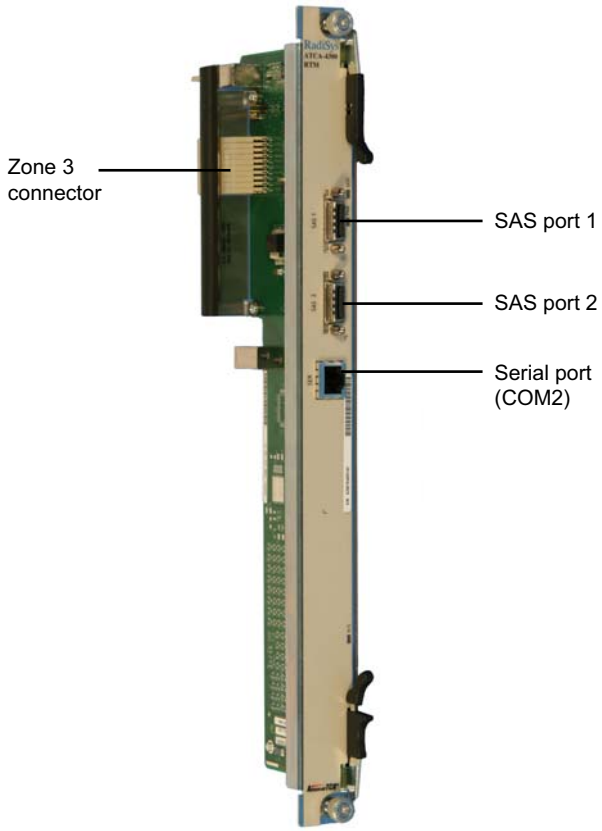
A hot-swap LED on the front panel is directly controlled by the CPM IPMI controller. An I^2C bus connection to the front module allows for IPMI access to FRU information and control of the RTM's LEDs through an I/O expander.

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Interfaces

The RTM is a single-slot unit according to the ATCA specification; it has a sheet metal faceplate that serves as an EMI/RFI barrier. The physical interfaces are identified in the following figure.

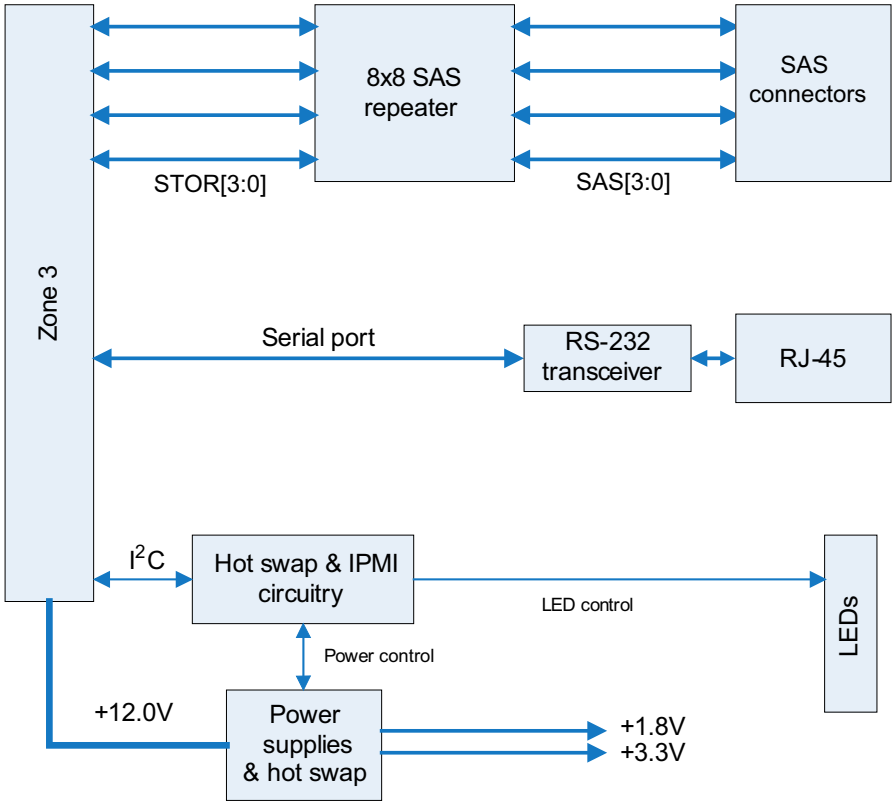
Figure 14. Rear transition module



The RTM serial port signals are sent to an on-board buffer, from which they are then sent to a front-panel connector. For signal integrity, SAS signals are connected to an on-board repeater before they are sent to a front panel connector. The front blade IPMI controller has I^2C access to the CPM's RTM for on-board FRU storage. The block diagram of the RTM module is shown in the following figure.

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Figure 15. RTM block diagram



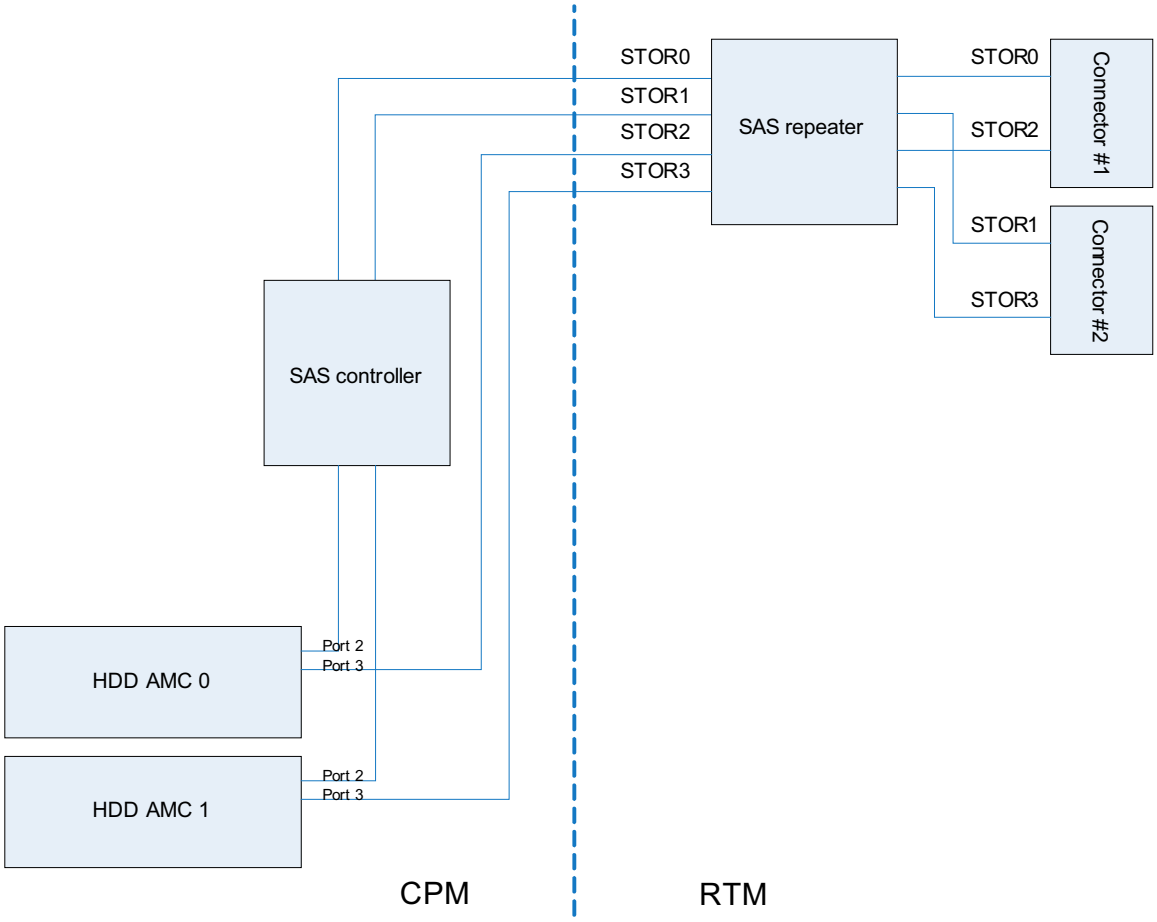
SAS repeater

Four SAS links are connected from the Zone 3 connector to the RTM front panel through an 8x8 repeater. The RTM allows SAS signaling to occur between two RTMs. The repeater guarantees SAS signal integrity over the cable between two CPM RTM modules.

A transmit pair from one RTM is connected to the corresponding and opposite receive pair in the second RTM. This crossing is accomplished in the SAS cabling. One SAS pair from each hard drive AMC is driven to an SAS controller on the CPM; the other pair from each drive connects directly to the SAS repeater. Two additional SAS pairs transmit and receive data to and from the SAS controller.

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Figure 16. SAS interface diagram



The repeater supports automatic out-of-band (OOB) signaling and automatically configures at startup. OOB functionality provides auto-detection of SATA or SAS signals at the input of the device and thereby drives the output pairs to the appropriate voltage level. The SAS links work after both RTM units have been powered up.

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Interface signals

Space has been allocated in the Zone 3 J30 connector for signals passing between the front module and the RTM. This represents a superset of signals that may be used for various combinations of interfaces between the CPM and the RTM. The RTM interface signals are listed in Table 16

Table 16. RTM interface signals

Signal name	Direction	Pins	Description
+12V	Out	6	Power source for RTM circuits, 2-Amp limit
+3.3_IPMI	Out	1	Power source for RTM circuits, 225-mA limit
IPMC_I2C_CLK	In/Out	1	IPMC control bus clock
IPMC_I2C_DAT	In/Out	1	IPMC control bus data
IPMC_INT*	In	1	Optional interrupt driven to IPMC
RTM_PS*	In	1	Indicates RTM is connected
RTM_EJECT*	In	1	Signal is grounded on RTM when ejector handle is closed; pull-up on CPM
RTM_HS_LED	Out	1	Controls RTM blue hot-swap LED
RTM_EN*	Out	1	Enables RTM
INT_0	In	1	Interrupts from RTM (reserved)
INT_1	In	1	
STOR[0:3]_RX±	In/Out	4	Differential pairs used by storage protocol; may be used for SATA or SAS
STOR[0:3]_TX±	In/Out	4	
SP_CTS	In	1	ICH COM2 serial port; TTL-level signals
SP_DSR	In	1	
SP_DTR	Out	1	
SP_RTS	Out	1	
SP_RX*	In	1	
SP_TX*	Out	1	

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SAS connector

Two SAS connectors are provided on the front panel of the RTM to support SAS signaling between RTMs. SAS port 2 is located above SAS port 2.

Table 17. SAS signal connector

Pin	Description		Pin	Description	
	Connector #1	Connector #2		Connector #1	Connector #2
S1	SAS0_RX+	SAS1_RX+	S10	*not connected*	*not connected*
S2	SAS0_RX–	SAS1_RX–	S11	*not connected*	*not connected*
S3	SAS2_RX+	SAS3_RX+	S12	*not connected*	*not connected*
S4	SAS2_RX–	SAS3_RX–	S13	SAS0_TX–	SAS1_TX–
S5	*not connected*	*not connected*	S14	SAS0_TX+	SAS1_TX+
S6	*not connected*	*not connected*	S15	SAS2_TX–	SAS3_TX–
S7	*not connected*	*not connected*	S16	SAS2_TX+	SAS3_TX+
S8	*not connected*	*not connected*	G1–G9	GND	GND
S9	*not connected*	*not connected*			

Serial connector

A standard serial port interface (RS-232) with a RJ-45 connector is provided on the RTM. This port is controlled by the front module.

Table 18. Serial RJ-45 connector

Pin	I/O	Description	Pin	I/O	Description
1	Out	RTS	5	–	GND (cable detect)
2	Out	DTR	6	In	RxD
3	Out	TxD	7	In	DSR
4	–	GND	8	In	CTS

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LEDs

The LED descriptions for the RTM are provided in the table below.

Table 19. LED descriptions

Name	Color	PICMG	Function
PWRGOOD	Green	LED 2	Indicates power supplies within tolerance
OOS	Red or amber	LED 1	Indicates abnormal operation
HOTSWAP	Blue	Hotswap	Indicates safe removal possible

Power-good LED

A green LED is located on the back side of the RTM in the area of the faceplate. It is in the same vertical location as the corresponding LED on the front module.

The power-good LED is driven by the LED2 signal connected through the I/O expander to the I^2C bus. The front CPM module detects power good via the I^2C bus from the PWRGD signals, connected to the I/O expander.

If the LED is green, the RTM power supplies are within tolerance. If the LED is off, the RTM power supplies are either off or out of tolerance.

Out-of-service LED

A red or amber LED—the color is determined by the IPMI software—is located on the back side of the RTM in the area of the faceplate, in the same vertical location as the corresponding LED on the front module.

The out-of-service (OOS) LED is driven by the LED1_A and LED1_B signals connected through the I/O expander to the I^2C bus.

If the LED is red or amber, the RTM is out of service.

Hot-swap LED

A blue hot-swap LED is located on the back side of the RTM in the area of the faceplate, in the same vertical location as the corresponding LED on the front module. Once the LED is solid blue, the module is ready for safe removal.

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Power

The RTM receives a 12V supply from the front blade. The 12V supply is used to generate the rest of the RTM's supplies, including +3.3V and +1.8V. An auxiliary 3.3V supply from the front module is also provided for exclusive use by the hot-swap circuitry.

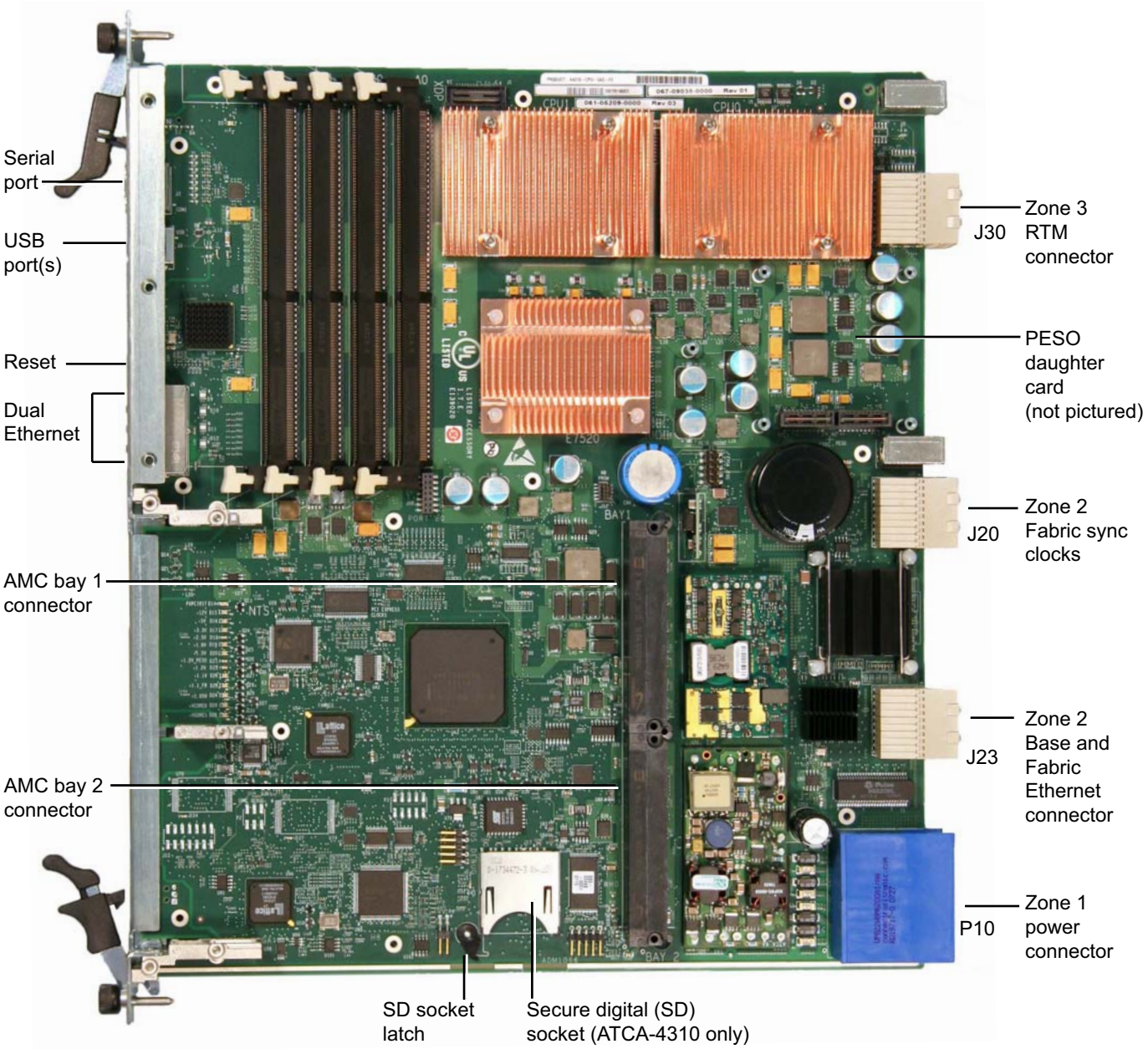
Table 20. Power

Supply	Maximum current / watts	Nominal current / watts
+12V	417 mA / 5.0 W	250 mA / 3. 0W
+3.3V IPMI	225 mA / 0.74 W	50 mA / 0.17 W

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This chapter provides physical interface details for the compute processing module (CPM). The figure below shows physical interface locations on the ATCA-4310 CPM.

Figure 17. ATCA-4310 board layout

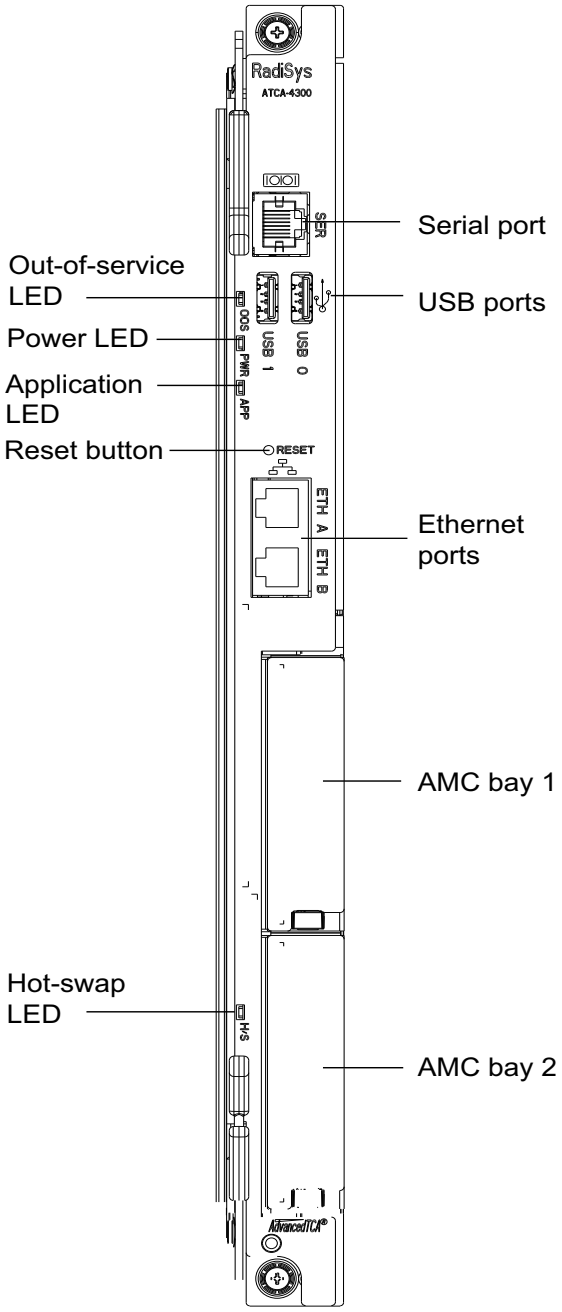


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Front panel interfaces

The CPM's front panel is shown in the following figure.

Figure 18. ATCA-4300 CPM front panel



Note: The ATCA-4310 front panel is similar to Figure 18, but it has only one USB port (the left port).

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Front panel connectors

The tables in this section detail connector pinouts for the front panel interfaces.

Table 21. USB 2.0 connector(s)

Pin	Description	Pin	Description
1	USB1:VCC	7	USB:P0+
2	USB:P1–	8	GND
3	USB:P1+	9	Shield (GND earth)
4	GND	10	Shield (GND earth)
5	USB0:VCC	11	Shield (GND earth)
6	USB:P0–	12	Shield (GND earth)

Table 22. COM1 RJ45 RS232 connector

Pin	Description	Pin	Description
1	RTS	5	GND (cable detect)
2	DTR	6	RxD
3	TxD	7	DSR
4	GND	8	CTS

Table 23. Front panel RJ45 dual gigabit Ethernet connectors

Pin	Description	Pin	Description
1	MDIO[0]+	5	MDIO[2]–
2	MDIO[0]–	6	MDIO[1]–
3	MDIO[1]+	7	MDIO[3]+
4	MDIO[2]+	8	MDIO[3]–

Important: To comply with GR-1089-CORE, if you connect cables to both front panel Ethernet connectors, at least one of the cables must be shielded.

Front panel LEDs

The following LEDs are present on the front panel of the CPM.

Table 24. CPM front panel LEDs

LED	Function	Color	Control
OOS	Out of service (ATCA LED1)	Amber or red	IPMC
Powergood	Power good (ATCA LED2)	Green	IPMC
App	Implementation-specific (ATCA LED3)	Amber	IPMC
Hot Swap	Hot swap (ATCA H/S LED)	Blue	IPMC

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Secure digital socket (ATCA-4310 only)

The SD cards accepted by this socket are described in *Secure digital (SD) card socket (ATCA-4310 only)* on page 25. Instructions for inserting the card are supplied in *Inserting an SD memory card (ATCA-4310)* on page 91.

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The system BIOS is based on Phoenix Technologies® TrustedCore BIOS and is adapted by RadiSys. This BIOS provides multiple-processor support, extensive memory configuration testing, console redirection, PCI Express bus support, and server management.

BIOS setup menus

The system BIOS contains a setup utility for modifying the system configuration. The system configuration information is maintained in the firmware hub and is used by the system BIOS to initialize the hardware.

Access to the setup menus is available for only a short time during the boot process. Pressing **F2** during boot enables access to the setup utility. The **Esc-2** key combination is an alternative that works in some situations when **F2** does not.

The BIOS setup menus include standard Phoenix BIOS menus and additional custom menus from RadiSys. A legend at the bottom of each menu provides information to help the user manipulate the setup options. Table 25 provides a general overview of the BIOS setup menus.

Table 25. BIOS setup menus

Option	Menu	Submenu
Main	Main	None
Advanced	Advanced	▪ Advanced Processor Configuration ▪ ACPI Configuration ▪ Event Log Configuration ▪ Expansion ROM Configuration ▪ PCI Express Configuration ▪ USB Configuration ▪ Advanced Chipset Control
Security	Security	None
Boot	Boot	▪ Boot Settings Configuration ▪ Boot Device Priority ▪ USB Drives (ATCA-4300 only) ▪ SATA Drives (ATCA-4300 only) ▪ SAS/FC Drives (ATCA-4300 only) ▪ Network Drives (ATCA-4300 only)

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Table 25. BIOS setup menus (continued)

Option	Menu	Submenu
System Management	System Management	▪ Remote Access Configuration ▪ Watchdog Timer ▪ System Information ▪ PCI Device Exclusion
Exit	Exit & Save	None

Some configuration settings can result in hardware conflicts. It is the responsibility of the person setting up the configuration to understand their hardware configuration and resource needs to prevent conflicts.

Boot device options

The CPM BIOS allows you to change the boot device priority of the 16 possible boot devices. For the ATCA-4300, you can rearrange the priorities of the groups of devices (USB, SATA, etc.) and then rearrange the individual device priorities within those groups. For the ATCA-4310, you can rearrange the 16 devices in any order in a single list.

Tip: A USB device that is not a CD-ROM or floppy device (FDC) is identified as a USB key or USB hard drive, depending on its size. A device that stores under 2 GB displays as a USB key, and a device that stores 2 GB or above displays as a USB hard drive.

Number and type of boot devices allowed

The ATCA-4300 CPM supports the following numbers of devices in each class:

- Four USB devices—one CD-ROM, one floppy (FDC), one key, and one hard drive
- Four SATA drives, controlled by the 6300ESB
- Four SAS/Fibre Channel hard drives
- Four network devices or Ethernet controllers—Base interface, Fabric interface, etc.

If more than four devices exist in a class, the first four are selected, and the others are ignored.

The ATCA-4310 CPM supports the following numbers of devices in each class:

- Six USB devices—one CD-ROM, one floppy (FDC), three keys (two used by the on-board flash devices), and one hard drive
- Two SATA drives, controlled by the 6300ESB
- Four SAS/Fibre Channel hard drives
- Four network devices or Ethernet controllers—Base interface, Fabric interface, etc.

Some devices must be enabled in the Expansion ROM Configuration submenu (under the Advanced menu) to be valid boot devices. Ethernet option ROMs are treated specially. If the Ethernet BI (Base interface) expansion ROM is enabled, all AMC expansion ROMs are ignored; however, if the Base interface is disabled, the AMC Ethernet expansion ROMs can be used.

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The multiboot BIOS supports a limited number of devices of each bootable type. For example, if the more than four Ethernet devices are enabled (two Fabric Ethernet and an AMC slot with four Ethernet ports), the number of allowable network devices will be exceeded, and some of the enabled devices will be excluded from the boot device list. If too many Ethernet devices are enabled, the enabled devices are included in this order of priority until the device limit is reached:

- Front panel ports (2)
- Base interface
- AMC slot 2 (if the Base interface is disabled)
- AMC slot 1 (if the Base interface is disabled)
- Fabric interface

USB devices are similarly included in the available USB categories in the order in which they are found. Extra devices are excluded from the boot device list.

Linux utility for changing BIOS settings

On the ATCA-4300 only, a Linux utility called *bioscli* enables you to view and change BIOS CMOS settings from the Linux command line. The utility can also create a file containing the CMOS settings, which can be used to distribute the same settings to other CPM modules.

The utility is available on the ATCA-4300 when you install the *bioscli* RPM package, which is in the Promentum software distribution. See the *Software Guide* for information on using the Promentum RPM packages.

To view all of the BIOS CMOS parameters, enter:

```
bioscli-bin -l
```

To change a value, enter:

```
bioscli-bin <parameter>=<value>
```

To redirect the current settings to a file, enter:

```
bioscli-bin -q ALL > <file_name>
```

To apply the settings in a file to another CPM, copy the file to the other CPM. From that CPM, enter:

```
bioscli-bin -f <file_name>
```

For more information, use the **-h** option to obtain help.

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BIOS error and event reporting

The BIOS reports errors and events that occur during the bootup process, during the BIOS power-on self-test (POST) tasks, and while the OS is running. Some of the errors cause the BIOS to stop its attempts to start the OS. The errors and events are identified in *BIOS error and event descriptions* on page 75.

Error reporting can be configured in the BIOS menus. The Advanced > Event Log Configuration submenu lets you enable logging for individual types of errors and select the logging methods. Logging of events is always enabled and is not configurable.

Enabling and disabling errors for logging

The Event Logging option on the Event Log Configuration submenu controls whether any errors are logged with any logging method. If this option is enabled, all individual error types that are enabled are reported to IPMI and the BIOS NVRAM log. If this option is disabled, no errors of any type are reported. Events are always logged regardless of this option setting.

You can enable and disable each type of error individually using the Event Log Configuration submenu. Disabling an error prevents any method of logging for that error type.

BIOS error and event reporting methods

IPMI reporting of errors and events

Events detected by the BIOS are reported using IPMI. IPMI is the only method of reporting that is available for events. In addition, when the Event Logging option is enabled, all error types that are enabled are reported using IPMI.

The BIOS sends IPMI messages through the KCS interface to the IPMC. The IPMC logs them in the CPM's local system event log (SEL) and reports them to the Shelf Manager, which makes the messages available in the global SEL.

You can view the messages in the SEL using the open-source *ipmitool* utility. For example, to view the global SEL from a system that has LAN connectivity to the active Shelf Manager:

```
ipmitool -I lan -H <Shelf_Mgr_IP_addr> -A NONE -t 0x20 sel list
```

Use the `-h` option to obtain help in using the utility. To view the CPM's local SEL, you can substitute the IPMB address of the CPM for the value 0x20 in the command above. See the Promentum *Shelf Management Software Reference* for the IPMB addresses of the slots in each RadiSys shelf.

BIOS NVRAM logging of errors

When the Event Logging option is enabled, all error types that are enabled are reported to the BIOS NVRAM log in addition to IPMI. The BIOS NVRAM log is readable on screen through the BIOS Advanced menu when you select the Event Log Configuration option.

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Non-maskable interrupt (NMI) reporting of errors

In addition to the other error reporting methods, you can enable requests for the chipset to generate non-maskable interrupts to the CPU when errors occur. The NMI Error Reporting option on the Event Log Configuration submenu controls this method. When Event Logging and NMI Error Reporting are enabled, all error types that are enabled generate NMI requests.

BIOS error and event descriptions

Error or event	Description	Type
Memory error	Correctable or uncorrectable ECC DRAM error.	Error–When enabled, reported with IPMI message and to BIOS log. An NMI is optional.
Interface or internal error	System bus, hub interface, PCI Express, or memory buffer error. PCI Express errors use PCI Express advanced error reporting.	
BIOS POST progress	A critical milestone was reached in the BIOS power-on self-test (POST) and boot process. If the BIOS fails to boot, these events indicate where the progress halted. For further details, see *BIOS event and checkpoint codes* on page 76.	Event–Always reported with IPMI message only.
Memory size change	Memory was added or removed since the last boot.	
System misconfiguration	Memory was not installed or incorrect memory installation.	
OS boot failure	Failure to boot from a PXE server or detection of a bad boot sector on the user-specified disk drive. The BIOS did not successfully transition to the OS.	

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BIOS event and checkpoint codes

You can view the SEL contents as described in *IPMI reporting of errors and events* on page 74. Displaying the port 80h codes requires an add-in POST card that attaches to a special connector on the CPM. The POST card shows the two-digit POST code using seven-segment displays.

SEL event codes

The BIOS sends system events, boot events during early POST tasks, and POST error events to the IPMC during BIOS start-up, early POST tasks, and execution. The IPMC logs the events to its local SEL and forwards them to the system SEL.

Table 26. SEL sensor events generated by the BIOS (Sheet 1 of 4)

Sensor type	Sensor type code	Sensor-specific offset	Event description
Processor	07h	00h	IERR
		01h	Thermal trip
		02h	FRB1/BIST failure
		03h	FRB2/hang in POST failure related to a processor failure. The system firmware progress sensor is used for other BIOS hangs.
		04h	FRB3/processor startup/initialization failure (CPU didn't start)
		05h	Configuration error
		06h	SM BIOS uncorrectable CPU-complex error
		07h	Processor presence detected
		08h	Processor disabled
		09h	Terminator presence detected
Memory	0Ch	00h	Correctable ECC / other correctable memory error
		01h	Uncorrectable ECC / other uncorrectable memory error
		02h	Parity
		03h	Memory scrub failed (stuck bit)
		04h	Memory device disabled
		05h	Correctable ECC / other correctable memory error logging limit reached The Event Data 3 field can be used to provide an event extension code, with this definition: 7:0 DIMM/SIMM/RIMM identification, relative to the entity associated with the sensor (if SDR provided for this sensor)
POST memory resize	0Eh	FFh	Memory resize event

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Table 26. SEL sensor events generated by the BIOS (Sheet 2 of 4)

Sensor type	Sensor type code	Sensor-specific offset	Event description
System firmware progress	0Fh	00h	System firmware error (POST error) The Event Data 2 field can be used to provide an event extension code, with this definition: Event Data 2: 00h Unspecified 01h No system memory is physically installed in the system 02h No usable system memory (all installed memory has experienced an unrecoverable failure) 03h Unrecoverable hard-disk/ATAPI/IDE device failure 04h Unrecoverable system-board failure 05h Unrecoverable diskette subsystem failure 06h Unrecoverable hard-disk controller failure 07h Unrecoverable PS/2 or USB keyboard failure 08h Removable boot media not found 09h Unrecoverable video controller failure 0Ah No video device detected 0Bh Firmware (BIOS) ROM corruption detected 0Ch CPU voltage mismatch (processors that share same supply have mismatched voltage requirements) 0Dh CPU speed matching failure 0Eh to FFh reserved
		01h	System firmware hang (shares the Event Data 2 definition with 02h system firmware progress)

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Table 26. SEL sensor events generated by the BIOS (Sheet 3 of 4)

Sensor type	Sensor type code	Sensor-specific offset	Event description
System firmware progress (continued)	0Fh (continued)	02h	System firmware progress The Event Data 2 field can be used to provide an event extension code, with this definition: Event Data 2: 00h Unspecified 01h Memory initialization 02h Hard-disk initialization 03h Secondary processor(s) initialization 04h User authentication 05h User-initiated system setup 06h USB resource configuration 07h PCI resource configuration 08h Option ROM initialization 0Ah Cache initialization 0Bh SM bus initialization 0Ch Keyboard controller initialization 0Dh Embedded controller/management controller initialization 0Eh Docking station attachment 0Fh Enabling docking station 10h Docking station ejection 11h Disabling docking station 12h Calling operating system wake-up vector 13h Starting operating system boot process, e.g., calling Int 19h 14h Baseboard or motherboard initialization 15h reserved 16h Floppy initialization 17h Keyboard test 18h Pointing device test 19h Primary processor initialization 1Ah to FFh reserved

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Table 26. SEL sensor events generated by the BIOS (Sheet 4 of 4)

Sensor type	Sensor type code	Sensor-specific offset	Event description
Event logging disabled	10h	00h	Correctable memory error logging disabled
		01h	Event "Type" logging disabled. Event logging is disabled for the following event/reading type, and the offset has been disabled. Event Data 2: Event/reading type code Event Data 3: [7:6] Reserved, write as 00 binary [5] 1 (binary) - Logging has been disabled for all events of given type [4] 1 (binary) = Assertion event, 0 (binary) = deassertion event [3:0] Event offset
		02h	Log area reset/cleared
		03h	All event logging disabled
Critical interrupt	13h	00h	Front panel NMI/diagnostic interrupt
		01h	Bus timeout
		02h	I/O channel check NMI
		03h	Software NMI
		04h	PCI PERR (PCI parity error, PCI Express advanced error, hub interface error, system bus error, memory buffer error)
		05h	PCI SERR (PCI system error)
		06h	EISA fail safe timeout
		07h	Bus correctable error
		08h	Bus uncorrectable error
		09h	Fatal NMI (port 61h, bit 7)
Boot error	1Eh	00h	No bootable media
		01h	Non-bootable diskette left in drive
		02h	PXE server not found
		03h	Invalid boot sector
		04h	Timeout waiting for user selection of boot source
OEM reserved	C0h-FFh	-	-

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POST codes for the main BIOS

Table 27 describes the POST checkpoint codes that the system BIOS writes to I/O port 80h during BIOS POST to indicate the BIOS progress. The checkpoints are listed in ascending order and are not in order of execution.

Table 27. POST checkpoints for the main BIOS (Sheet 1 of 6)

Checkpoint	POST routine description
02h	Verifies that the CPU is in real mode. If the CPU is in protected mode, (stackless-no memory), turns on A20 and pulses the reset line, forcing a shutdown.
04h	Gets CPU type from CPU registers and other methods. Saves CPU type in NVRAM.
06h	Initializes system hardware. Resets the DMA (stackless) controllers, disables the videos, clears any pending interrupts from the real-time clock.
08h	Initializes chip set registers to the initial POST values.
09h	Sets in-POST flag in CMOS that indicates it is in POST. If this bit is not cleared by postClearBootFlag (AEh), the BIOS on next boot determines that the current configuration caused POST to fail and sets default values for configuration. Clears the CMOS diagnostic byte (register E). Checks the real-time clock and verifies the battery has not lost power. Checksums the CMOS and verifies it has not been corrupted.
0Ah	Initializes CPU registers.
0Bh	Enables CPU cache. Sets bits in CMOS related to cache.
0Ch	Sets the initial POST values of the cache registers if not integrated into the chipset.
0Eh	Sets the initial POST values for registers in the optional integrated I/O chip.
0Fh	Enables the local bus IDE if enabled, then primary or secondary IDE depending on other drives detected.
10h	Initializes power management (optional).
11h	General dispatch for alternate register initialization. Sets initial POST values for other hardware devices defined in the register tables.
13h	Early reset of PCI devices required to disable bus start (optional) master. Assumes the presence of a stack and running from decompressed shadow memory.
14h	Verifies that the keyboard controller is responding. Sends a self-test command to the 8742 and waits for results. Also reads the switch inputs from the 8742 and writes the keyboard controller command byte.
16h	Verifies that the ROM BIOS checksums to zero.
17h	Initializes external cache before auto-sizing memory (stackless, optional).
18h	Initializes all three of the 8254 timers. Sets the clock timer (0) to binary count, mode 3 (square wave mode), and read/write LSB then MSB. Initializes the clock timer to zero. Sets the RAM refresh timer (1) to binary count mode 2 (Rate Generator), and read/write LSB only. Sets the counter to 12H to generate the refresh at the proper rate. Sets sound timer (2) to binary count, mode 3, and read/write LSB, then MSB.

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Table 27. POST checkpoints for the main BIOS (Sheet 2 of 6)

Checkpoint	POST routine description
1Ah	Initializes DMA command register with these settings: ▪ Memory to memory disabled ▪ Channel 0 hold address disabled ▪ Controller enabled ▪ Normal Timing ▪ Fixed priority ▪ Late write selection ▪ DREQ sense active ▪ DACK sense active low Initializes all 8 DMA channels with these settings: ▪ Single mode ▪ Address increment ▪ Auto initialization disabled (channel 4 - Cascade) ▪ Verify transfer
1Ch	Initializes the 8259 interrupt controller with these settings: ▪ ICW4 needed ▪ Cascade ▪ Edge-triggered mode
20h	Verifies that DRAM refresh is operating by polling the refresh bit in PORTB.
22h	Verifies the 8742 keyboard controller is responding. Sends a self-test command to the 8742 and waits for results. Also reads the switch inputs from the 8742 and writes the keyboard controller command byte.
24h	Sets segment-register addressability to 4 GB.
28h	Using the table of configurations supplied by the specific chipset module, tests each DRAM configuration to see if that particular configuration is valid. Then programs the chipset to its auto-sized configuration. Before auto-sizing, disables all caches and all shadow RAM.
29h	Initializes the POST memory manager.
2Ah	Zeroes the first 512K of RAM.
2Ch	Tests 512K base address lines.
2Eh	Tests first 512K of RAM.
2Fh	Initializes external cache before shadowing.
32h	Computes CPU speed.
33h	Initializes the Phoenix dispatch manager.
38h	Shadows the system BIOS.
3Ah	Auto-sizes external cache and program cache size for enabling later in POST.
3Ch	If CMOS is valid, loads chipset registers with values from CMOS, otherwise loads defaults from NV storage to CMOS RAM.
3Dh	Loads alternate registers with CMOS values.
42h	Initializes interrupt vectors 0 through 77h to the BIOS general interrupt handler.

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Table 27. POST checkpoints for the main BIOS (Sheet 3 of 6)

Checkpoint	POST routine description
45h	Initializes all motherboard devices.
46h	Verifies the ROM copyright notice.
48h	Verifies that the equipment specified in the CMOS matches the hardware currently installed. If the monitor type is set to 00, then a video ROM must exist. If the monitor type is 1 or 2, sets the video switch to CGA. If monitor type 3, sets the video switch to mono. Also specifies in the equipment byte that disk drives are installed. Sets appropriate status bits in CMOS or the BDA if configuration errors are found.
49h	Performs these tasks: ▪ Sizes the PCI bus topology and sets bridge bus numbers ▪ Sets the system max bus number ▪ Writes a zero to the command register of every PCI device ▪ Writes a zero to all 6 base registers in every PCI device ▪ Writes a negative one to the status register of every PCI device
4Ah	Initializes all video adapters in system.
4Bh	Initializes QuietBoot if it is installed. Enables both keyboard and timer interrupts (IRQ0 and IRQ1).
4Ch	Shadows video BIOS ROM if all of these conditions are true: ▪ Shadowing is specified by setup ▪ The CMOS is valid ▪ The previous boot was OK
4Eh	Displays copyright notice.
50h	Displays CPU type and speed.
51h	Checksums CMOS and initializes each EISA slot with data from the initialization data block.
52h	Tests for the self-test code if the system is started from a cold start. When powered up, the keyboard performs a self test and sends an AA if successful.
54h	Initializes keystroke clicker if enabled in setup.
58h	Tests for any unexpected, spurious interrupts. Does an STI for unexpected interrupts. Tests the NMI for an unexpected interrupt. Enables the parity checkers and reads from memory, checking for an unexpected interrupt.
59h	Registers POST display services, fonts, and languages with the POST dispatch manager.
5Ah	Displays prompt “Press F2 to enter Setup” if enabled.
5Bh	Disables CPU cache.
5Ch	Tests RAM between 512 K and 640K.
60h	Determines and tests the amount of extended memory available. Determines if memory exists by writing to a few strategic locations to see if the data can be read back. If so, performs an address-line test and a RAM test on the memory. Saves the total extended memory size in the CMOS at CMOS extended.
62h	Performs an address line test on A0 to the amount of memory available. This test is dependent on the processor, since the test varies depending on the width of memory (16 or 32 bits). This test also uses A20 as the skew address to prevent corruption of the system memory.
64h	Jumps to UserPatch1.

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Table 27. POST checkpoints for the main BIOS (Sheet 4 of 6)

Checkpoint	POST routine description
66h	Sets cache registers to their CMOS values if CMOS is valid, unless auto configuration is enabled. If auto-configuration is enabled, loads cache registers from the setup default table.
67h	Early multiprocessor initialization.
68h	Enables external cache and CPU cache if present. Configures non-cacheable regions if necessary.
6Ah	Displays external cache size on the screen if it is non-zero.
6Ch	Displays shadow message.
6Eh	Displays the starting offset of the non-disposable segment of the BIOS.
70h	Checks flags in CMOS and in the BIOS data area for errors detected during POST. Displays error messages on the screen.
72h	Checks status bits to see if configuration problems were detected. If so, displays error messages on the screen.
76h	Checks status bits for keyboard-related failures. Displays error messages on the screen.
7Ch	Initializes the hardware interrupt vectors from 08 to 0F and from 70h to 77H. Also sets the interrupt vectors from 60h to 66H to zero.
7Eh	Performs the coprocessor initialization test. Uses the floating-point instructions to determine if a coprocessor exists instead of the ET bit in CR0.
80h	Disables onboard COM and LPT ports before testing for presence of external I/O devices.
81h	Runs late device initialization routines.
82h	Tests and identifies RS232 ports.
83h	Configures fixed disk Controller.
85h	Displays any ESCD read errors and configures all PnP ISA devices.
86h	Initializes onboard I/O and BDA according to CMOS and presence of external devices.
87h	Initializes motherboard configurable devices.
89h	Enables non-maskable interrupts.
8Ah	Initializes extended BIOS data area and initializes the mouse.
8Bh	Sets up the interrupt vectors and present bit in Equipment byte.
8Ch	Initializes both of the floppy disks and displays an error message if failure was detected. Checks both drives to establish the appropriate diskette types in the BIOS data area.
8Fh	Counts the number of ATA drives in the system and updates the number in the BIOS data area.
90h	Initializes hard-disk controller. If the CMOS RAM is valid and intact and fixed disks are defined, calls the fixed disk initialization routine to initialize the fixed disk system and take over the appropriate interrupt vectors.
91h	Configures the local bus IDE timing register based on the drives attached to it.
92h	Jumps to UserPatch2.
93h	Builds the MPTABLE for multi-processor boards.

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Table 27. POST checkpoints for the main BIOS (Sheet 5 of 6)

Checkpoint	POST routine description
95h	▪ Checks CMOS for CD-ROM drive present ▪ Activates the drive by checking for media present ▪ Checks sector 11h (17) for boot record volume descriptor ▪ Checks the boot catalog for validity ▪ Picks a boot entry ▪ Creates a specification packet
97h	Creates pointer to MP table in Extended BDA.
98h	Searches for option ROMs. Scans the area from C800h to C800h+BCP ROM-Scan-Size (or to E000h by default) on every 2KB boundary, looking for add-on cards that need initialization.
9Ah	Shadows miscellaneous ROMs if all of these conditions are true: ▪ Shadowing is specified by setup ▪ The CMOS is valid ▪ The previous boot was OK
9Ch	Sets up power management. Initiates power-management state machine.
9Dh	Initializes security engine.
9Eh	Enables hardware interrupts.
9Fh	Checks the total number of fast disks (ATA and SCSI) and updates the BIOS data area.
A0h	Verifies that the system clock is interrupting.
A2h	Sets up Numlock indicator. Displays a message if key switch is locked.
A4h	Initializes typematic rate.
A8h	Overwrites the “Press F2 for Setup” prompt with spaces, erasing it from the screen.
AAh	Scans the key buffer to see if the F2 key was struck after keyboard interrupts were enabled. If an F2 keystroke is found, sets a flag.
ACh	Determines whether to enter setup. Goes to setup if F2 was pressed. If errors were found, displays “Press F1 or F2” prompt, and then goes to setup if F2 is pressed or boots if F1 is pressed.
AEh	Clears ConfigFailedBit and InPostBit in CMOS.
B0h	Checks for errors. If errors were found, beeps twice and displays F1 or F2 prompt. If F2 keystroke occurs, goes to setup. If F1 keystroke occurs, boots.
B2h	Changes status bits in CMOS and/or the BIOS data area to indicate that POST is complete.
B5h	Turns off Esc and F2 key checking, fades out screen, and resets video (clears screen, resets cursor, and reloads DAC) if all of these conditions are true: ▪ The VGA adapter is present ▪ The OEM screen is still up
B6h	If password on boot is enabled, makes a call to setup to check password. If the user does not enter a valid password, setup does not return.
B9h	Clears all screen graphics before booting.
BAh	Initializes the DMI header and sub-structures.
BCh	Clears parity-error latch.
BDh	Displays Boot First menu if multiboot is installed.

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Table 27. POST checkpoints for the main BIOS (Sheet 6 of 6)

Checkpoint	POST routine description
BEh	If BCP option is enabled, clears the screen before booting.
BFh	Checks virus and backup reminders. Displays system summary.
C0h	Tries to boot with INT 19.
C1h	Initializes the POST error manager (PEM).
C2h	Writes POST error manager errors.
C3h	Displays POST error manager errors.
C4h	Initializes system error handler.
C9h	Computes extended checksum (optional).
D2h	Unknown interrupt.

Memory initialization POST codes

Table 29 describes the POST checkpoint codes that the system BIOS writes to I/O port 80h during memory initialization POST tasks. The checkpoints are listed in ascending order and are not in order of execution.

Table 28. Memory initialization POST checkpoints

Checkpoint	Description
E1h	No memory devices found error (DIMM slots are not populated)
EFh	Memory population order error (DIMM slots were not populated in the correct order)

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Boot block POST codes

Table 29 describes the POST checkpoint codes that the system BIOS writes to I/O port 80h during early boot block POST tasks. The checkpoints are listed in ascending order and are not in order of execution.

Table 29. Boot block POST checkpoints

Checkpoint	Description
80h	Initializes the chipset
81h	Initializes the bridge
82h	Initializes the CPU
83h	Initializes system timer
84h	Initializes system 1/0
85h	Checks force recovery boot
86h	Checksums BIOS ROM
87h	Goes to main BIOS
88h	Initializes multi processor
89h	Sets huge segment
8Ah	Initializes OEM special code
8Bh	Initializes PIC and DMA
8Ch	Initializes memory type
8Dh	Initializes memory size
8Eh	Shadows boot block
8Fh	Initializes SMM
90h	Performs system memory test
91h	Initializes interrupt vectors
92h	Initializes run time clock
93h	Initializes video
94h	Initializes beeper
95h	Initializes boot
96h	Clears huge segment
97h	Boots to recovery OS
99h	Initializes security (if installed)

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Installing the CPM

For more information on installing or replacing a CPM, please see the *ATCA-4300/ATCA-4310 Compute Processing Module Installation Guide.*

Removing the CPM

Observe appropriate ESD precautions during the following procedure:

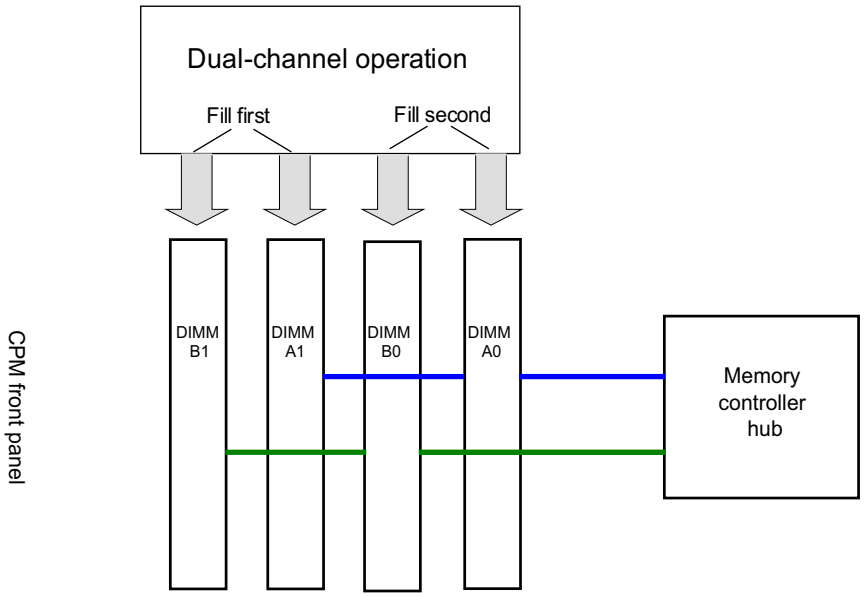
1. Disconnect all cables from the CPM front panel.
2. Loosen the CPM retaining screws at the front of the shelf.
3. Release only one ejector latch—either the right latch or the lower latch—and then stop.
   - If the CPM is oriented vertically, release only the lower ejector latch.
   - If the CPM is oriented horizontally, release only the right ejector latch.
4. The blue hot-swap LED starts flashing. When the hot-swap LED turns solid blue it is safe to remove the CPM.
5. Release the second ejector latch—either the left latch or the upper latch.
6. Simultaneously pull both ejector latches to disengage the module from the backplane.
7. Pull the CPM out of the slot.
8. Place the CPM on a flat, static-free surface.

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Installing DIMMs

There are four DIMM sockets on the CPM. When installing DIMMs, the two sockets closest to the CPM front panel should be loaded with memory first; then the second two DIMM sockets, located closest to the memory controller hub, can be loaded. Refer to Figure 19 for guidance in determining the order of installation and correct DIMM placement.

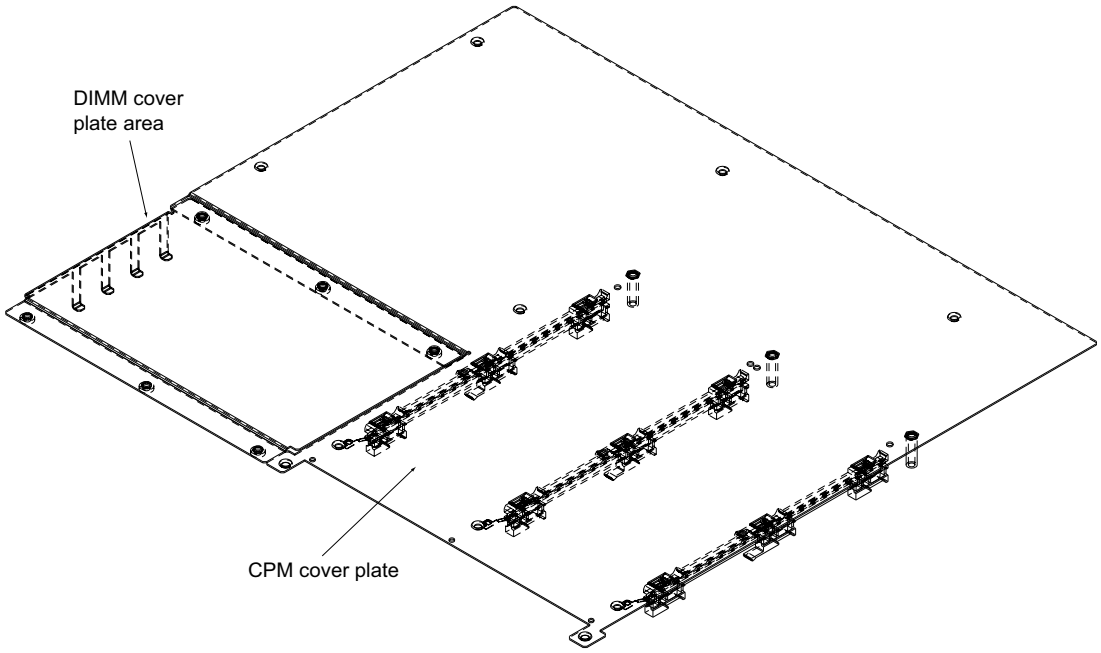
Figure 19. DIMM installation order



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The following instructions assume that the CPM has been removed from the shelf.

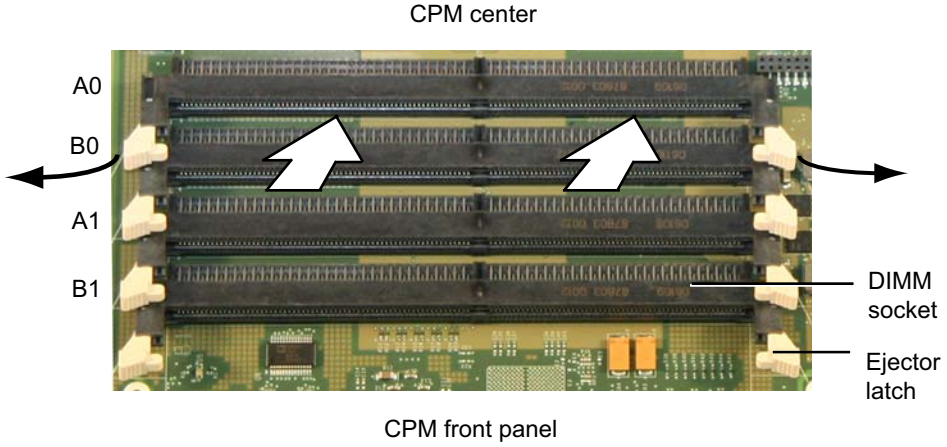
1. Unscrew the small plate covering the DIMMs.



Before inserting DIMMs, check for the correct order of insertion as outlined in Figure 19.

2. Open the DIMM ejector latches by pushing them outward, as indicated by the black arrows in Figure 20.
3. Hold the DIMM memory card by the edges, and push it down firmly into the socket, as indicated by the white arrows in Figure 20. The ejector latches will close, and the DIMM will click into place when it is firmly seated.
4. Insert other DIMMs using the above steps, remembering to fill the corresponding DIMM slot for correct channel operation.

Figure 20. DIMM sockets



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5. Screw the DIMM cover plate back into place.
6. Power up the CPM, and check the BIOS screens to make sure all memory is working.

Removing DIMMs

These instructions assume that the CPM has been removed from the shelf, and the DIMM cover has been removed.

1. Unscrew the small plate covering the DIMM.

   Before removing DIMMs, determine the correct order of removal by examining Figure 19.
2. Open the ejector latches by pushing them outward, as indicated by the black arrows in Figure 20. The DIMM memory card will disengage automatically.
3. Hold the DIMM memory card by the edges and remove it.
4. Remove other DIMMs in the same manner. Be sure to remove the corresponding DIMM for correct channel operation.
   - If you are replacing the DIMM with a new card, follow the steps in the preceding section.
   - If the DIMM socket is to remain empty, close the ejector latches.
5. Screw the DIMM cover plate back into place.
6. Power up the CPM, and check the BIOS screens to make sure all memory is working.

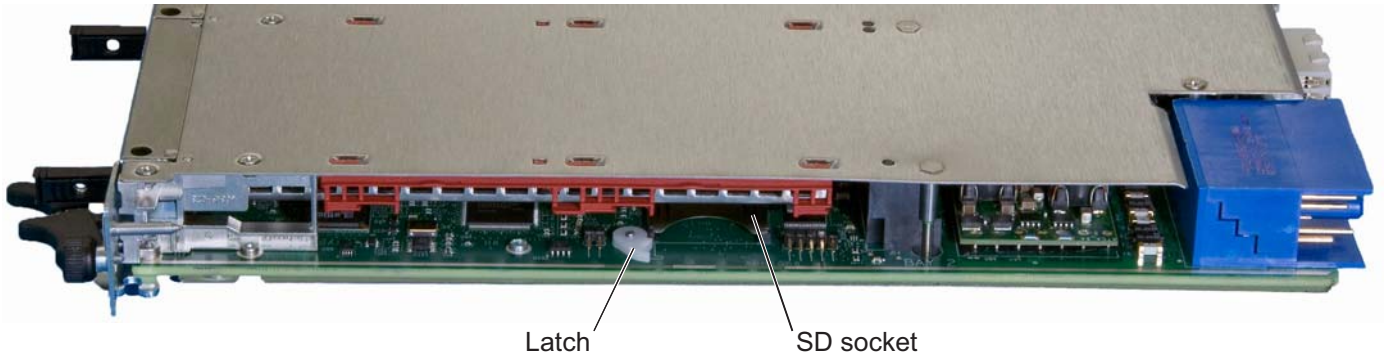
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Inserting an SD memory card (ATCA-4310)

The following instructions assume that the CPM has been removed from the shelf. The instructions require a Phillips screwdriver.

1. Rest the top edge of the CPM on a flat, static-free surface. The CPM is vertical, with the SD socket furthest from the flat surface. See Figure 21.

Figure 21. SD socket and latch locations on the ATCA-4310



2. Insert the SD card into the socket.
3. On the back of the CPM opposite the socket latch, locate the screw that is exposed by a hole in the sheet metal.
4. Close the latch by turning the screw 1/4 turn to the right with a Phillips screwdriver. Figure 22 shows the closed latch.

Figure 22. SD card inserted with the latch closed



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Upgrading the CPM firmware

Table 30 summarizes the CPM's programmable devices and the content that can be upgraded.

Table 30. Programmable devices and upgradeable content

Programmable device	Upgradeable content	Copies to upgrade	Run upgrade commands on
FWHs	BIOS	2	CPM's CPU
	BIOS boot block	2	CPM's CPU
IPMC	IPMI application	2	CPM's CPU or remote CPU
	IPMI boot	1	CPM's CPU or remote CPU
FPGAs	IPMC FPGA	1	CPM's CPU or remote CPU
	FAWKES FPGA	1	CPM's CPU or remote CPU
Ethernet EEPROMs	Base Ethernet EEPROM	1	CPM's CPU
	Fabric Ethernet EEPROM	1	CPM's CPU
	Front panel Ethernet EEPROM	1	CPM's CPU
IPMC EEPROM	FRU records	1	CPM's CPU or remote CPU

All upgrades can be performed from the CPM's local CPU:

- Through a serial console that is directly connected to the CPM or RTM serial port.
- Through a remote serial console as described in *Serial-over-LAN* on page 50.
- By a remote login to the CPM over Ethernet. The session is lost when the CPM reboots. You cannot access the BIOS setup menus or view the bootup messages.

Upgrades of the IPMC, FPGAs, and IPMC EEPROM can alternatively be performed from a remote computer's CPU:

- By specifying the Shelf Manager IP address and the CPM's IPMB address in the upgrade commands.
- By specifying the CPM's Base interface IP address in the upgrade commands. This method is available when access to the IPMC has been configured as described in *IPMI-over-LAN* on page 47.

Instructions for upgrading all of the components are included with the upgrade image, which is available from the RadiSys web site or from RadiSys Technical Support.

Upgrading the CPM system BIOS firmware

For redundancy, the two system BIOS firmware hubs (FWHs) each store a BIOS image. Three methods exist for modifying or restoring the system BIOS stored in the FWHs. The first is a system BIOS upgrade using a Linux 'reflash' utility; use this method if you are able to boot but need to reflash. The second method is transparent: when one BIOS image is corrupted, the other is used automatically. The third method is for crisis recovery; use this method if you are unable to boot, and you have an upgrade image.

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Reflash utility upgrade

Use this option to reflash the FWHs if you are able to boot system BIOS. RadiSys supplies a Linux 'reflash' utility to reprogram FWH flash ROMs on the CPM. The utility allows both FWHs to be reflashed.

It is best to reflash both FWHs as follows: First reflash one FWH. Try to boot the system BIOS from that image. When successful, then reflash the other FWH.

Instructions for use of the 'reflash' utility are included with the upgrade image, which is available from the RadiSys web site or from RadiSys Technical Support.

After reflashing, it is suggested you power down and restart the system to prevent instability.

Crisis recovery

Generally, recovery is automatically initiated upon detection by the boot block of a corrupted system BIOS; however, if you are unable to boot BIOS, you will need to proceed with crisis recovery.

Before starting, you must have a system BIOS upgrade image available on a USB floppy, USB CD-ROM, or USB flash device. Instructions for use of the upgrade image are included with the image download, which is available from the RadiSys web site or from RadiSys Technical support.

Note: A system BIOS recovery requires the boot block code stored in the FWH to be uncorrupted. If corruption of the system BIOS occurs during a system BIOS upgrade or recovery, the boot block detects this on the next boot of the CPM and enters the system BIOS recovery sequence. If the boot blocks of both FWHs are corrupted, the CPM must be returned to RadiSys for repair.

Upgrading the CPM IPMC firmware

The CPM IPMC firmware can be uploaded to the IPMC microcontroller and reprogrammed in-circuit. You can obtain the firmware upgrade image and the *ipmitool* utility from the RadiSys web site or from RadiSys Technical Support. Instructions for their use are included with the downloads.

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Troubleshooting

When you encounter an unexpected situation, in which the CPM does not perform as expected, look for symptoms that might clarify the cause. The following table can aid you in diagnosing and correcting problems.

Table 31. Troubleshooting

Symptom	Probable cause and correction
The login prompt does not appear after BIOS has booted	▪ Is the serial cable plugged into both the module and the system with the serial connection? Check the cabling. ▪ Is the CPM inserted into the correct slot in the shelf? Make sure it is completely inserted into one of the node slots. ▪ Is the application set to the following? 115200 bps, no parity, 8 data bits, I stop bit, with no flow control ▪ Is the power LED lit? Make sure the module is completely inserted, and the hot-swap latch is engaged. ▪ Has the default Linux port speed been changed? Check the */boot/grub/grub.conf* and */etc/inittab files*.
Message: Operating system not found	▪ Is an operating system present on the selected boot media? Make sure the OS is saved to the selected device. ▪ Was the correct device selected in BIOS? Check the BIOS boot menu to ensure the correct device is first in the list. ▪ Is the network boot set up correctly? Verify that an appropriate network link is available between the module and the system.
Sensors generate errors or events	▪ See the troubleshooting recommendations in *Sensor alarms and recommended actions* on page 121.
AMC card not functioning	▪ See the e-key

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Environmental

The CPM is designed to meet the following environmental specifications. The CPM Hardware Verification Plan provides details of the testing environment and procedure.

Table 32. Environmental specifications

Characteristic	State	Value
Temperature (ambient)	Operating	+5° C to +45° C 30° C/hr rate of change
	Short-term operating [1]	–5° C to +55° C 30° C/hr rate of change
	Storage	–40° C to +70° C
Relative humidity	Operating	5% to 85% noncondensing
	Short-term operating [1]	5% to 90% noncondensing at +30× C
	Storage	5% to 90% noncondensing at +40º C
	Short-term storage [1]	5% to 95% noncondensing at +40º C
Altitude	Operating [2]	Up to 1800 meters (5,905 feet), +55×C 1800 meters up to 4000 meters (13,123 feet), derated linearly to +45° C
Shock (drop)	Unpacked Free fall, corners and edges	0 to < 10 kg = 100 mm drop
	Packaged (Unpalletized) Free fall, corners and edges	0 to < 10 kg = 750 mm drop
Vibration	Operating	0.1 g, 5 to 100 Hz and back, 0.1 octave/min sine sweep [2]
	Transportation (packaged)	0.5 g, 5 to 50 Hz and back, 0.1 octave/min sine sweep [2] 3.0 g, 50 to 500 Hz and back, 0.25 octave/min sine sweep [2]
Seismic	Operating	Per Zone 4 test method, GR-63-CORE
1 "Short term" is defined as a maximum of 96 consecutive hours 2 In each direction, for each of three mutually perpendicular axes		

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Safety

The safety specifications are measured with ambient temperature approximately 25° C and relative humidity between 30% and 50%. Testing has been performed in partnership with a nationally recognized testing laboratory (NRTL) accredited to provide the required certifications.

Table 33. Safety

Characteristic	Certification	Standard and test criteria
Product Safety – US	Accessory Listing	UL 60950-1 "Safety for Information Technology Equipment"
Product Safety – Canada	Approval	CSA 22.2 #60950-1 "Safety for Information Technology Equipment"
Product Safety – EU	Conformance with the Low Voltage Directive	EN 60950-1 "Safety for Information Technology Equipment"
Product Safety – Other	CB Report	IEC 60950-1 "Safety for Information Technology Equipment"

Mechanical

Table 34. Mechanical specifications

Characteristic	Value
Overall dimensions	351 mm x 30.48 mm x 305 mm (13.819" x 1.20" x 12.008")
Weight[1]	2.77 kg (6.11 lbs) for the ATCA-4300, 2.81 kg (6.19 lbs) for the ATCA-4310

[1] Weight includes two memory DIMMs and two airflow management filler modules in the AMC bays.

NEBS

The CPM is designed to meet the following Telcordia NEBS standards.

Table 35. Telecommunications Specifications (NEBS)

Standard	Description
GR-63-CORE	NEBS Requirements: Physical Protection
GR-1089-CORE	Electromagnetic Compatibility and Electrical Safety
SR-3580	Network Equipment – Building Systems (NEBS) Criteria Levels Level 3, indoor contaminants levels

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Electromagnetic compatibility (EMC)

The ESD, EMC, and Immunity specifications are measured with ambient temperature between 20° C and 30° C and relative humidity between 30% and 50%.

Table 36. Electromagnetic compatibility (EMC)

Emissions		
Characteristic	**State**	**Standard and criteria**
Radiated emissions	Operating	FCC Part 15, Class B EN 300 386, Non-Telecom Centre
Conducted emissions	Operating	FCC Part 15, Class B EN 300 386, Non-Telecom Centre

Immunity		
Characteristic	**State**	**Standard and criteria**
ESD	Operating	EN 61000-4-2 8KV direct contact, performance criteria A 15KV air discharge, performance criteria A
Radiated	Operating	EN 61000-4-3 10 V/m, 10kHz – 10 GHz, 80% AM Performance Criteria A
Fast transient/burst	Operating	EN 61000-4-4 0.5kV, 5/50 ns, 5kHz repetition frequency Performance criteria B
Surge voltages	Operating	EN 61000-4-5 Data ports: 1kV, 1.2/50 µs or 8/20 µs DC power port: 0.5kV, 1.2/50 µs or 8/20 µs Performance criteria B
Conducted	Operating	EN 61000-4-6 0.01–80 MHz Frequency (MHz) — Min Calibration Current 0.01–0.27 — 89 dBµA (rms) 0.27–0.8 — 77.6 dBµA - 20 $\log_{10}$ f 0.8–30 — 79.5 dBµA 30–80 — TBD Performance criteria A
Magnetic field immunity	Operating	EN 61000-4-8 50 Hz / 1 A/m Performance criteria A

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Mean time between failure (MTBF)

Calculation Type: MTBF/FIT rate

Standard: Telcordia Standard SR-332 Issue 2

Methods: Method I, Case I, Quality Level II

The calculation results were generated using the references and assumptions listed. This specification and its associated calculations supersede all other released mean time between failures (MTBF) and failure in time (FIT) calculations with earlier dates. The reported failure rates do not represent catastrophic failure.

Table 37. Reliability Estimate Data

Failure Rate (FIT) for ATCA-4300	6061 failures in 10^9 hours
Failure Rate (FIT) for ATCA-4310	6944 failures in 10^9 hours
MTBF for ATCA-4300	165,000 hours
MTBF for ATCA-4310	144,000 hours

Environmental assumptions

- Failure rates are based on a 35°C ambient temperature.
- Applied component stress levels are 50% (voltage, current, and/or power).
- Ground, fixed, controlled environment with an environmental adjustment factor equal to 1.0.

General assumptions

- Component failure rates are constant.
- Board-to-system interconnects are included within estimates.
- Non-electrical components (screws, mechanical latches, labels, covers, etc.) are not included in estimates.

General notes

- Method I, Case I = Based on parts count. Equipment failure is estimated by totaling device failures rates and quantities used.
- Quality Level II = Devices purchased to specifications, qualified devices, vendor lot-to-lot controls for AQLs and DPMs.

Where available, direct component supplier predictions or actual FIT rates have been used.

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Pressure drop curves

The P-Q curves below illustrate the pressure drop (P) versus the air flow rate (Q) measured for an ATCA-4310 in a fixed wind-tunnel environment that emulates a slot in an ATCA shelf. Each curve represents a different combination of modules installed in the AMC bays. The modules include:

- An AMC-3202 SAS hard disk drive (HDD) AMC
- An AMC-7211 Quad Gigabit Ethernet AMC
- An airflow management filler module

Figure 23. P-Q curve with two AMC filler modules

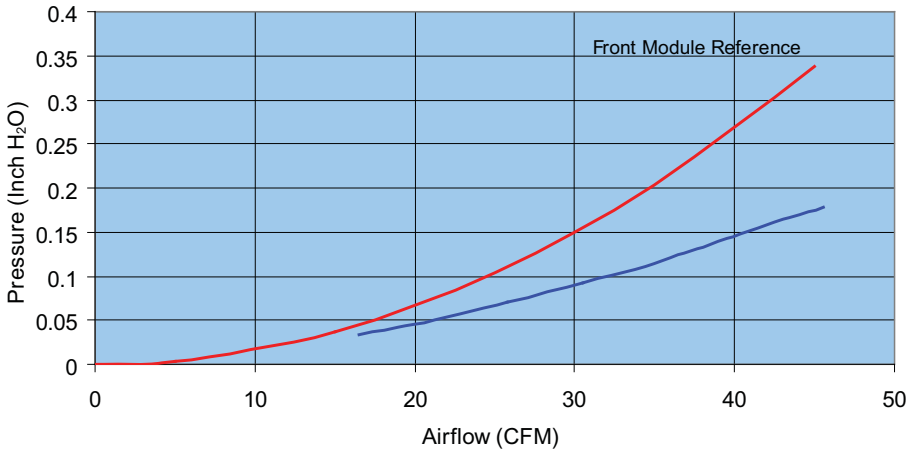
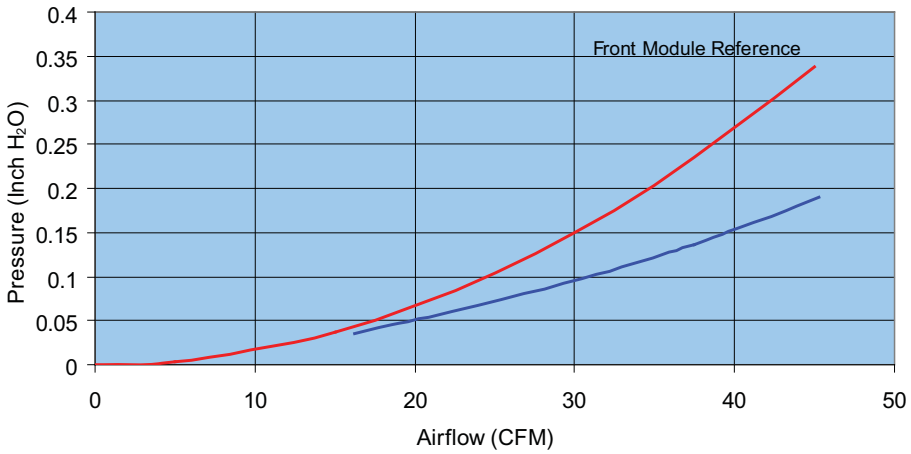
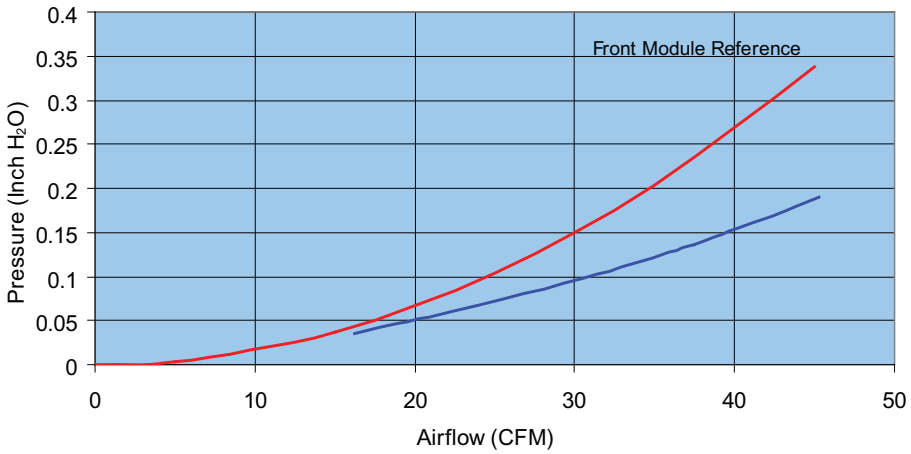


Figure 24. P-Q curve with an AMC-3202 and an AMC filler module



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Figure 25. P-Q curve with an AMC-3202 and an AMC-7211



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Backplane interfaces

This section details the CPM backplane interface connectivity.

Table 38. CPM backplane connectivity summary

Connector	Channel	Port	Board usage	PICMG definition	Comments
P10	48V	A/B	Power	3.0	Dual 48V DC power
	IPMB	A/B	IPMB	3.0	Dual IPMB
J23	Base 1	–	10/100/1000BASE-T port A	3.0	Dual star Base interface
	Base 2	–	10/100/1000BASE-T port B	3.0	
	Fabric 1 (ATCA-4300)	0	1000BASE-BX port A	3.1, option 1, 4, or 5	Dual star Ethernet Fabric interface
		1	AMC bay 1: 1000BASE-BX port 0	3.1, option 2 or 5	Dual star Fabric interface from AMCs
		2	AMC bay 2: 1000BASE-BX port 0	–	
		3	4.25 Gbps Fibre Channel	3.1, option 4 or 5	Dual star Fibre Channel Fabric interface
	Fabric 1 (ATCA-4310)	0	1000BASE-BX port A or 10GBASE-BX4 port A	3.1, option 1 or 9	Dual star 1 Gb or 10Gb Ethernet Fabric interface
		1	10GBASE-BX port A		
		2	10GBASE-BX port A		
		3	10GBASE-BX port A		
	Fabric 2 (ATCA-4300)	0	1000BASE-BX port B	3.1, option 1, 4, or 5	Dual star Ethernet Fabric interface
		1	AMC bay 1: 1000BASE-BX port 1	3.1, option 2 or 5	Dual star Fabric interface from AMC(s)
		2	AMC bay 2: 1000BASE-BX port 1	–	
		3	4.25 Gbps Fibre Channel	3.1, option 4 or 5	Dual star Fibre Channel Fabric interface
	Fabric 1 (ATCA-4310)	0	1000BASE-BX port B or 10GBASE-BX4 port B	3.1, option 1 or 9	Dual star 1 Gb or 10Gb Ethernet Fabric interface
		1	10GBASE-BX port B		
		2	10GBASE-BX port B		
		3	10GBASE-BX port B		

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Table 38. CPM backplane connectivity summary (continued)

Connector	Channel	Port	Board usage	PICMG definition	Comments
J20	Update	0	AMC bay 1	3.0	For AMC APS
		1	AMC bay 2	3.0	For AMC APS
	Clock	1A/1B	Input: 8 KHz	3.0	Multiplexed to AMC bays TCLKA
		2A/2B	Input: 19.44 MHz	3.0	
		3A/3B	Output	3.0	Multiplexed from AMC bays TCLKB

Backplane connector P10 signals

Table 39. Zone 1 contact assignments, P10

Contact	Designation	Description	Mating Sequence
1	Reserved	Reserved	*not applicable*
2	Reserved	Reserved	*not applicable*
3	Reserved	Reserved	*not applicable*
4	Reserved	Reserved	*not applicable*
5	HA0	Hardware Address Bit 0	Third
6	HA1	Hardware Address Bit 1	Third
7	HA2	Hardware Address Bit 2	Third
8	HA3	Hardware Address Bit 3	Third
9	HA4	Hardware Address Bit 4	Third
10	HA5	Hardware Address Bit 5	Third
11	HA6	Hardware Address Bit 6	Third
12	HA7/P	Hardware Address Bit 7 (Odd Parity Bit)	Third
13	SCL_A	IPMB Clock, Port A	Third
14	SDA_A	IPMB Data, Port A	Third
15	SCL_B	IPMB Clock, Port B	Third
16	SDA_B	IPMB Data, Port B	Third
17	MT1_TIP	Metallic Test #1 Tip	Third
18	MT2_TIP	Metallic Test #2 Tip	Third
19	–RING_A	Ringing Generator A Negative Ringing	Third
20	–RING_B	Ringing Generator B Negative Ringing	Third
21	MT1_RING	Metallic Test #1 Ringing	Third
22	MT2_RING	Metallic Test #2 Ringing	Third
23	RRTN_A	Ringing Generator A Return	Third
24	RRTN_B	Ringing Generator B Return	Third
25	SHELF_GND	Shelf Ground	First
26	LOGIC_GND	Logic Ground	First

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Table 39. Zone 1 contact assignments, P10

Contact	Designation	Description	Mating Sequence
27	ENABLE_B	Enable B	Fourth
28	VRTN_A	Voltage Return A	First
29	VRTN_B	Voltage Return B	First
30	EARLY_A	–48 Volt Early A	First
31	EARLY_B	–48 Volt Early B	First
32	ENABLE_A	Enable A	Fourth
33	–48V_A	–48 Volt A	Second
34	–48V_B	–48 Volt B	Third
	Gray indicates unused pins		

Table 40. Power circuit contact definitions

Contact	Designation	Description
33	–48 V_A	–48 Volt input, Feed A, uses ENABLE_A to enable converters
34	–48V_B	–48 Volt input, Feed B, uses ENABLE_B to enable converters
28	VRTN_A	–48 Volt return, Feed A
29	VRTN_B	–48 Volt return, Feed B
30	EARLY_A	–48 Volt input, Feed A precharge
31	EARLY_B	–48 Volt input, Feed B precharge
32	ENABLE_A	Short pin for power sequencing, Feed A, tied to VRTN_A on backplane
27	ENABLE_B	Short pin for power sequencing, Feed B, tied to VRTN_B on backplane
26	LOGIC_GND	Ground reference and return for front blade–to–front blade logic signals
25	SHELF_GND	Connection to shelf ground and safety ground

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Backplane connector J20 signals

Table 41. Backplane connector J20 signals

Row	Interface designation	AB		CD		EF		GH	
1	CLKs	CLK1A+	CLK1A–	CLK1B+	CLK1B–	CLK2A+	CLK2A–	CLK2B+	CLK2B–
2	Update channel and CLKs					CLK3A+	CLK3A–	CLK3B+	CLK3B–
3									
4		Tx0(UP)+	Tx0(UP)–	Rx0(UP)+	Rx0(UP)–	Tx1(UP)+	Tx1(UP)–	Rx1(UP)+	Rx1(UP)–
5	Fabric Channel 15								
6									
7	Fabric Channel 14								
8									
9	Fabric Channel 13								
10									
Note: Each differential pair has an individual L-shaped ground contact (not shown).									
	Gray indicates unused pins								

Backplane connector J23 signals

Table 42. Backplane connector J23 signals

Row	Interface designation	AB		CD		EF		GH	
1	Fabric Channel 2	Tx2[2]+	Tx2[2]–	Rx2[2]+	Rx2[2]–	Tx3[2]+	Tx3[2]–	Rx3[2]+	Rx3[2]–
2		Tx0[2]+	Tx0[2]–	Rx0[2]+	Rx0[2]–	Tx1[2]+	Tx1[2]–	Rx1[2]+	Rx1[2]–
3	Fabric Channel 1	Tx2[1]+	Tx2[1]–	Rx2[1]+	Rx2[1]–	Tx3[1]+	Tx3[1]–	Rx3[1]+	Rx3[1]–
4		Tx0[1]+	Tx0[1]–	Rx0[1]+	Rx0[1]–	Tx1[1]+	Tx1[1]–	Rx1[1]+	Rx1[1]–
5	Base Channel 1	BI_DA1+	BI_DA1–	BI_DB1+	BI_DB1–	BI_DC1+	BI_DC1–	BI_DD1+	BI_DD1–
6	Base Channel 2	BI_DA2+	BI_DA2–	BI_DB2+	BI_DB2–	BI_DC2+	BI_DC2–	BI_DD2+	BI_DD2–
7	Base Channel 3								
8	Base Channel 4								
9	Base Channel 5								
10	Base Channel 6								
Note: Each differential pair has an individual L-shaped ground contact (not shown).									
	Gray indicates unused pins								

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RTM connector J30 signals

Table 43. RTM connector J30 signals

Row	AB		CD		EF		GH	
1	+12V	+12V	+12V	+3.3V_SUS	RTM_EJECT	RTM_PRSNT*	RTM_HS_LED	RTM_EN*
2	+12V	+12V	+12V	IPMC_INT*	IPMC_SCL	IPMC_SDA	BAY4_SCL	BAY4_SDA
3	SP_TX	SP_RX	SP_DTR	SP_RTS	SP_CTS	SP_DSR	BAY3_SCL	BAY3_SDA
4	SOCA	SOCB	INT_0	INT_1	RTML_TX	RTML_RX	RTML_CLK	RSVD
5	BAY3_17_TX+	BAY3_17_TX–	BAY3_17_RX+	BAY3_17_RX–	BAY3_18_TX+	BAY3_18_TX–	BAY3_18_RX+	BAY3_18_RX–
6	BAY3_19_TX+	BAY3_19_TX–	BAY3_19_RX+	BAY3_19_RX–	BAY3_20_TX+	BAY3_20_TX–	BAY3_20_RX+	BAY3_20_RX–
7	BAY4_17_TX+	BAY4_17_TX–	BAY4_17_RX+	BAY4_17_RX–	BAY4_18_TX+	BAY4_18_TX–	BAY4_18_RX+	BAY4_18_RX–
8	BAY4_19_TX+	BAY4_19_TX–	BAY4_19_RX+	BAY4_19_RX–	BAY4_20_TX+	BAY4_20_TX–	BAY4_20_RX+	BAY4_20_RX–
9	STOR0_TX+	STOR0_TX–	STOR0_RX+	STOR0 _RX–	STOR1_TX+	STOR1_TX–	STOR1_RX+	STOR1_RX–
10	STOR2_TX+	STOR2_TX–	STOR2_RX+	STOR2_RX–	STOR3_TX+	STOR3_TX–	STOR3_RX+	STOR3_RX–
Note: Each differential pair has an individual L-shaped ground contact (not listed).								

Internal interfaces

The CPM contains two connectors for inboard AMC modules and four CPU DDR2 memory sockets. The AMC port pinouts for both the AMCs and DDR2 memory sockets are provided in the following sections.

AMC port connections

Table 44 lists the AMC port connections for the ATCA-4300, and Table 45 on page 107 lists them for the ATCA-4310.

Table 44. ATCA-4300 AMC B+ connector pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	44	PCIE_RX0+	87	ETH2_TX– [1]	130	RTM_SDA
2	+12	45	PCIE_RX0–	88	ETH2_TX+ [1]	131	GND
3	PS1*	46	GND	89	GND	132	*N.C.*
4	+3.3_IPMI	47	PCIE_TX0+	90	ETH2_RX– [1]	133	*N.C.*
5	GA0	48	PCIE_TX0–	91	ETH2_RX+ [1]	134	GND
6	RSVD	49	GND	92	GND	135	*N.C.*
7	GND	50	PCIE_RX1+	93	ETH3_TX– [1]	136	*N.C.*
8	RSVD	51	PCIE_RX1–	94	ETH3_TX+ [1]	137	GND
9	+12	52	GND	95	GND	138	*N.C.*
10	GND	53	PCIE_TX1+	96	ETH3_RX– [1]	139	*N.C.*
11	ETH0_RX+	54	PCIE_TX1–	97	ETH3_RX+ [1]	140	GND
12	ETH0_RX–	55	GND	98	GND	141	TX17-

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Table 44. ATCA-4300 AMC B+ connector pinout (continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
13	GND	56	SCL_L	99	*N.C.*	142	TX17+
14	ETH0_TX+	57	+12	100	*N.C.*	143	GND
15	ETH0_TX–	58	GND	101	GND	144	RX17-
16	GND	59	PCIE_RX2+	102	*N.C.*	145	RX17+
17	GA1	60	PCIE_RX2–	103	*N.C.*	146	GND
18	+12	61	GND	104	GND	147	TX18-
19	GND	62	PCIE_TX2+	105	*N.C.*	148	TX18+
20	ETH1_RX+	63	PCIE_TX2–	106	*N.C.*	149	GND
21	ETH1_RX–	64	GND	107	GND	150	RX18-
22	GND	65	PCIE_RX3+	108	*N.C.*	151	RX18+
23	ETH1_TX+	66	PCIE_RX3–	109	*N.C.*	152	GND
24	ETH1_TX–	67	GND	110	GND	153	TX19-
25	GND	68	PCIE_TX3+	111	UC_TX– [2]	154	TX19+
26	GA2	69	PCIE_TX3–	112	UC_TX+ [2]	155	GND
27	+12	70	GND	113	GND	156	RX19-
28	GND	71	SDA_L	114	UC_RX– [2]	157	RX19+
29	SAS0_RX+	72	+12	115	UC_RX+ [2]	158	GND
30	SAS0_RX–	73	GND	116	GND	159	TX20-
31	GND	74	SCLK_IN+	117	*N.C.*	160	TX20+
32	SAS0_TX+	75	SCLK_IN–	118	*N.C.*	161	GND
33	SAS0_TX–	76	GND	119	GND	162	RX20-
34	GND	77	SCLK_OUT+	120	*N.C.*	163	RX20+
35	SAS1_RX+	78	SCLK_OUT–	121	*N.C.*	164	GND
36	SAS1_RX–	79	GND	122	GND	165	*N.C.*
37	GND	80	PCIE_CLK+	123	*N.C.*	166	*N.C.*
38	SAS1_TX+	81	PCIE_CLK–	124	*N.C.*	167	*N.C.*
39	SAS1_TX–	82	GND	125	GND	168	*N.C.*
40	GND	83	PS0*	126	*N.C.*	169	*N.C.*
41	AMC_EN*	84	+12	127	*N.C.*	170	GND
42	+12	85	GND	128	GND		
43	GND	86	GND	129	RTM_SCL		

N.C. = Not connected
1 Available on AMC bay 2 only; other pin assignments apply to both AMC bays
2 AMC_B1 routes to update channel port 0; AMC_B2 routes to update channel port 1

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Table 45. ATCA-4310 AMC B+ connector pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	44	PCIE_RX0+	87	*N.C.*	130	RTM_SDA
2	+12	45	PCIE_RX0–	88	*N.C.*	131	GND
3	PS1*	46	GND	89	GND	132	*N.C.*
4	+3.3_IPMI	47	PCIE_TX0+	90	*N.C.*	133	*N.C.*
5	GA0	48	PCIE_TX0–	91	*N.C.*	134	GND
6	RSVD	49	GND	92	GND	135	*N.C.*
7	GND	50	PCIE_RX1+	93	*N.C.*	136	*N.C.*
8	RSVD	51	PCIE_RX1–	94	*N.C.*	137	GND
9	+12	52	GND	95	GND	138	*N.C.*
10	GND	53	PCIE_TX1+	96	*N.C.*	139	*N.C.*
11	ETH0_RX+[1]	54	PCIE_TX1–	97	*N.C.*	140	GND
12	ETH0_RX–[1]	55	GND	98	GND	141	TX17-
13	GND	56	SCL_L	99	*N.C.*	142	TX17+
14	ETH0_TX+[1]	57	+12	100	*N.C.*	143	GND
15	ETH0_TX–[1]	58	GND	101	GND	144	RX17-
16	GND	59	PCIE_RX2+	102	*N.C.*	145	RX17+
17	GA1	60	PCIE_RX2–	103	*N.C.*	146	GND
18	+12	61	GND	104	GND	147	TX18-
19	GND	62	PCIE_TX2+	105	*N.C.*	148	TX18+
20	ETH1_RX+[1]	63	PCIE_TX2–	106	*N.C.*	149	GND
21	ETH1_RX–[1]	64	GND	107	GND	150	RX18-
22	GND	65	PCIE_RX3+	108	*N.C.*	151	RX18+
23	ETH1_TX+[1]	66	PCIE_RX3–	109	*N.C.*	152	GND
24	ETH1_TX–[1]	67	GND	110	GND	153	TX19-
25	GND	68	PCIE_TX3+	111	UC_TX– [2]	154	TX19+
26	GA2	69	PCIE_TX3–	112	UC_TX+ [2]	155	GND
27	+12	70	GND	113	GND	156	RX19-
28	GND	71	SDA_L	114	UC_RX– [2]	157	RX19+
29	SAS0_RX+	72	+12	115	UC_RX+ [2]	158	GND
30	SAS0_RX–	73	GND	116	GND	159	TX20-
31	GND	74	SCLK_IN+	117	*N.C.*	160	TX20+
32	SAS0_TX+	75	SCLK_IN–	118	*N.C.*	161	GND
33	SAS0_TX–	76	GND	119	GND	162	RX20-
34	GND	77	SCLK_OUT+	120	*N.C.*	163	RX20+
35	SAS1_RX+	78	SCLK_OUT–	121	*N.C.*	164	GND
36	SAS1_RX–	79	GND	122	GND	165	*N.C.*
37	GND	80	PCIE_CLK+	123	*N.C.*	166	*N.C.*
38	SAS1_TX+	81	PCIE_CLK–	124	*N.C.*	167	*N.C.*
39	SAS1_TX–	82	GND	125	GND	168	*N.C.*

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Table 45. ATCA-4310 AMC B+ connector pinout (continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
40	GND	83	PS0*	126	*N.C.*	169	*N.C.*
41	AMC_EN*	84	+12	127	*N.C.*	170	GND
42	+12	85	GND	128	GND		
43	GND	86	GND	129	RTM_SCL		

N.C. = Not connected
1 Available on AMC bay 2 only; other pin assignments apply to both AMC bays
2 AMC_B1 routes to update channel port 0; AMC_B2 routes to update channel port 1

DIMM socket pinouts

The following figure shows the physical location of end and center pins for the DDR2 memory card, and the following table provides the corresponding DIMM socket pinouts.

Figure 26. DDR2 memory card

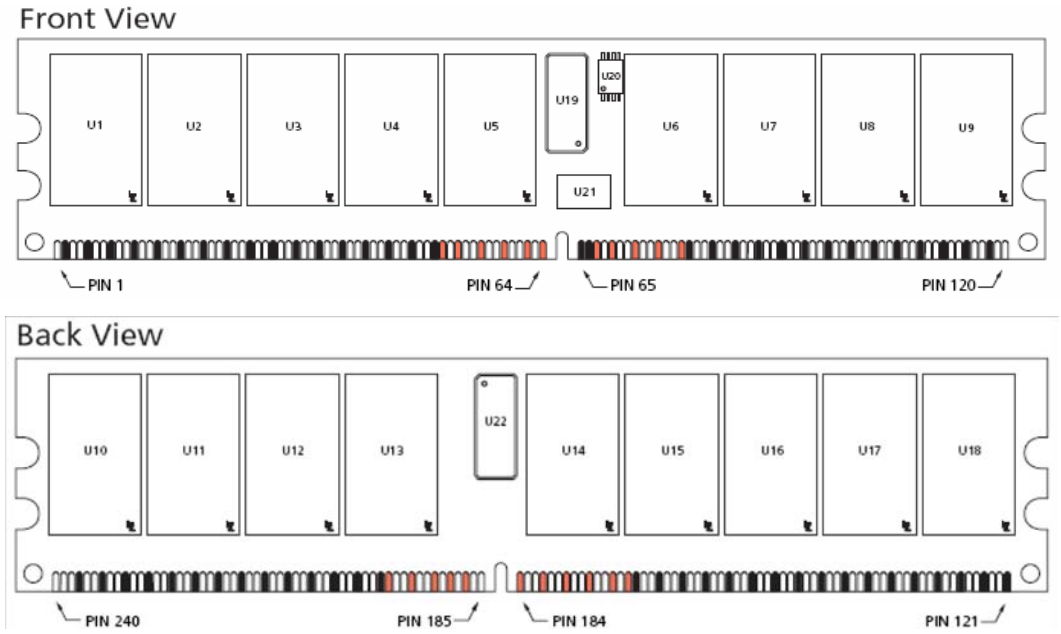


Table 46. DDR2 240-pin DIMM socket

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vref	61	A4	121	V_{SS}	181	V_{DDQ}
2	V_{SS}	62	V_{DDQ}	122	DQ4	182	A3
3	DQ0	63	A2	123	DQ5	183	A1
4	DQ1	64	V_{DD}	124	V_{SS}	184	V_{DD}
5	V_{SS}	65	V_{SS}	125	DQS9	185	CK0
6	DQS0*	66	V_{SS}	126	DQS9*	186	CK0*
7	DQS0	67	V_{DD}	127	V_{SS}	187	V_{DD}

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Table 46. DDR2 240-pin DIMM socket (continued)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
8	V_{SS}	68	NC/PAR_IN	128	DQ6	188	A0
9	DQ2	69	V_{DD}	129	DQ7	189	V_{DD}
10	DQ3	70	A10/AP	130	V_{SS}	190	BA1
11	V_{SS}	71	BA0	131	DQ12	191	V_{DDQ}
12	DQ8	72	V_{DDQ}	132	DQ13	192	RAS*
13	DQ9	73	WE*	133	V_{SS}	193	S0*
14	V_{SS}	74	CAS*	134	DQS10	194	V_{DDQ}
15	DQS1*	75	V_{DDQ}	135	DQS10*	195	ODT0
16	DQS1	76	NC	136	V_{SS}	196	NC/A13
17	V_{SS}	77	NC	137	RSVD	197	V_{DD}
18	RESET*	78	V_{DDQ}	138	RSVD	198	V_{SS}
19	NC	79	V_{SS}	139	V_{SS}	199	DQ36
20	V_{SS}	80	DQ32	140	DQ14	200	DQ37
21	DQ10	81	DQ33	141	DQ15	201	V_{SS}
22	DQ11	82	V_{SS}	142	V_{SS}	202	DQS13
23	V_{SS}	83	DQS4*	143	DQ20	203	DQS13*
24	DQ16	84	DQS4	144	DQ21	204	V_{SS}
25	DQ17	85	V_{SS}	145	V_{SS}	205	DQ38
26	V_{SS}	86	DQ34	146	DQS11	206	DQ39
27	DQS2*	87	DQ35	147	DQS113	207	V_{SS}
28	DQS2	88	V_{SS}	148	V_{SS}	208	DQ44
29	V_{SS}	89	DQ40	149	DQ22	209	DQ45
30	DQ18	90	DQ41	150	DQ23	210	V_{SS}
31	DQ19	91	V_{SS}	151	V_{SS}	211	DQS14
32	V_{SS}	92	DQS5*	152	DQ28	212	DQS14*
33	DQ24	93	DQS5	153	DQ29	213	V_{SS}
34	DQ25	94	V_{SS}	154	V_{SS}	214	DQ46
35	V_{SS}	95	DQ42	155	DQS12	215	DQ47
36	DQS3*	96	DQ43	156	DQS12*	216	V_{SS}
37	DQS3	97	V_{SS}	157	V_{SS}	217	DQ52
38	V_{SS}	98	DQ48	158	DQ30	218	DQ53
39	DQ26	99	DQ49	159	DQ31	219	V_{SS}
40	DQ27	100	V_{SS}	160	V_{SS}	220	RSVD
41	V_{SS}	101	SA2	161	CB4	221	RSVD
42	CB0	102	NC	162	CB5	222	V_{SS}
43	CB1	103	V_{SS}	163	V_{SS}	223	DQS15
44	V_{SS}	104	DQS6*	164	DQS17	224	DQS15*
45	DQS8*	105	DQS6	165	DQS17*	225	V_{SS}
46	DQS8	106	V_{SS}	166	V_{SS}	226	DQ54

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Table 46. DDR2 240-pin DIMM socket (continued)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
47	V_{SS}	107	DQ50	167	CB6	227	DQ55
48	CB2	108	DQ51	168	CB7	228	V_{SS}
49	CB3	109	V_{SS}	169	V_{SS}	229	DQ60
50	V_{SS}	110	DQ56	170	V_{DDQ}	230	DQ61
51	V_{DDQ}	111	DQ57	171	NC	231	V_{SS}
52	CKE0	112	V_{SS}	172	V_{DD}	232	DQS16
53	V_{DD}	113	DQS7*	173	NC	233	DQS16*
54	NC/BA2	114	DQS7	174	NC	234	V_{SS}
55	NC/ERR_OUT	115	V_{SS}	175	V_{DDQ}	235	DQ62
56	V_{DDQ}	116	DQ58	176	A12	236	DQ63
57	A11	117	DQ59	177	A9	237	V_{SS}
58	A7	118	V_{SS}	178	V_{DD}	238	V_{DDSPD}
59	V_{DD}	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

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FRU INFORMATION AREAS C

FRU information is stored in nonvolatile memory and is used by the IPMC to locate and communicate with the available FRUs. The CPM stores its FRU information in compliance with these specifications:

- *IPMI Platform Management FRU Information Storage Definition*, v1.0, Revision 1.1
- PICMG 3.0 Revision 2.0 *AdvancedTCA Base Specification*

You can retrieve all of the FRU information, including backplane E-Keying and on-board E-Keying information, using the *ipmitool* utility. The OEM records are detailed in this manual.

The CPM provides this FRU information:

- Common header
- Internal use area
- Board information area
- Product information area
- Multirecord area
  - Board point-to-point connectivity
  - Carrier information table record
  - Carrier activation and current management record
  - Carrier point-to-point connectivity record
  - AMC Crosspoint switch #1 point-to-point connectivity record (Fabric for ATCA-4300, PESO for ATCA-4310)
  - AMC PESO-A point-to-point connectivity record (ATCA-4300 only)
  - AMC MCH port C0 point-to-point connectivity record (ATCA-4300 only)
  - AMC MCH port B0 point-to-point connectivity record (ATCA-4300 only)
  - AMC MCH point-to-point connectivity record (ATCA-4310 only)
  - Update channel Crosspoint point-to-point connectivity record
  - OEM Ethernet Crosspoint switch #1 record (Fabric, ATCA-4300 only). For details, see *OEM Ethernet Crosspoint switch #1 connectivity record (ATCA-4300 only)* on page 112.

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OEM Ethernet Crosspoint switch #1 connectivity record (ATCA-4300 only)

On the ATCA-4300 only, the Intel® VSC3312 Fabric Crosspoint switch provides the ability to configure Fabric Ethernet connectivity by mapping Ethernet connections between AMCs, the backplane Fabric interfaces, and the payload processor. See *Configuring Fabric Ethernet connectivity* on page 39 for details.

In the Input/Output Mapping field defined in Table 47, set each of the 12 bytes to the number of the port you want it connected to (or to 0xFE to disable the port). By default, CPMs without front panel Ethernet ports have ports 6 and 7 connected to ports 10 and 11, respectively. Note that ports 10 and 11 cannot be connected to each other, and backplane ports cannot be connected to other backplane ports.

The following table shows the default values stored in the Ethernet Crosspoint record. The mapping describes physical ports of the switch in terms of logical ports, as shown in Figure 10 on page 38.

Table 47. OEM Ethernet Crosspoint connectivity record

Field description	Size (bytes)	Default value (hex)		
Record type	1	0xC0		
End of list/version	1	0x02		
Record length	1	*calculated*		
Record checksum	1	*calculated*		
Header checksum	1	*calculated*		
Manufacturer ID	3	0xF1, 0x10, 0x00		
Record ID	1	0x1		
Record format version	1	0x00		
Input/output mapping (for CPMs without front panel Ethernet ports)	12	[0] = 0xFE [1] = 0xFE [2] = 0xFE [3] = 0xFE	[4] = 0xFE [5] = 0xFE [6] = 0x0A [7] = 0x0B	[8] = 0xFE [9] = 0xFE [10] = 0x06 [11] = 0x07
Input/output mapping (for CPMs with front panel Ethernet ports)		[0] = 0x06 [1] = 0x04 [2] = 0x07 [3] = 0x05	[4] = 0x01 [5] = 0x03 [6] = 0x00 [7] = 0x02	[8] = 0xFE [9] = 0xFE [10] = 0xFE [11] = 0xFE
Total	**22**			

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IPMI commands

The IPMI commands in this appendix conform to the *PICMG 3.0 R2.0 Advanced Telecommunications Computing Architecture (ATCA) Specification* and the *IPMI Intelligent Platform Management Interface (IPMI) Specification*; however, these commands have been adapted specifically for use with the RadiSys CPM.

Table 48. Supported IPMI commands (Sheet 1 of 3)

Message commands	NetFn	Command
Get Device ID	App (0x06)	0x01
Cold Reset	App (0x06)	0x02
Warm Reset	App (0x06)	0x03
Get Self Test Results	App (0x06)	0x04
Broadcast "Get Device ID"	App (0x06)	0x01
Reset Watchdog Timer	App (0x06)	0x22
Set Watchdog Timer	App (0x06)	0x24
Get Watchdog Timer	App (0x06)	0x25
Set BMC Global Enables	App (0x06)	0x2E
Get BMC Global Enables	App (0x06)	0x2F
Clear Message Flags	App (0x06)	0x30
Get Message Flags	App (0x06)	0x31
Get Message	App (0x06)	0x33
Send Message	App (0x06)	0x34
Get Channel Authentication Capabilities	App (0x06)	0x38
Get Session Challenge	App (0x06)	0x39
Activate Session	App (0x06)	0x3A
Set Session Privilege Level	App (0x06)	0x3B
Close Session	App (0x06)	0x3C
Get Session Info	App (0x06)	0x3D
Get AuthCode	App (0x06)	0x3F
Set Channel Access	App (0x06)	0x40
Get Channel Access	App (0x06)	0x41
Get Channel Info	App (0x06)	0x42
Set User Access	App (0x06)	0x43
Get User Access	App (0x06)	0x44
Set User Name	App (0x06)	0x45
Get User Name	App (0x06)	0x46

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Table 48. Supported IPMI commands (Sheet 2 of 3) (continued)

Message commands	NetFn	Command
Set User Password	App (0x06)	0x47
Activate Payload	App (0x06)	0x48
Deactivate Payload	App (0x06)	0x49
Get Channel Payload Support	App (0x06)	0x4E
Set Event Receiver	S/E (0x04)	0x00
Get Event Receiver	S/E (0x04)	0x01
Platform Event (a.k.a "Event Message")	S/E (0x04)	0x02
Get Device SDR Info	S/E (0x04)	0x20
Get Device SDR	S/E (0x04)	0x21
Reserve Device SDR Repository	S/E (0x04)	0x22
Set Sensor Hysteresis	S/E (0x04)	0x24
Get Sensor Hysteresis	S/E (0x04)	0x25
Set Sensor Threshold	S/E (0x04)	0x26
Get Sensor Threshold	S/E (0x04)	0x27
Set Sensor Event Enable	S/E (0x04)	0x28
Get Sensor Event Enable	S/E (0x04)	0x29
Get Sensor Reading	S/E (0x04)	0x2D
Get FRU Inventory Area Info	Storage (0x0A)	0x10
Read FRU Data	Storage (0x0A)	0x11
Write FRU Data	Storage (0x0A)	0x12
Get SDR Repository Info	Storage (0x0A)	0x20
Reserve SDR Repository	Storage (0x0A)	0x22
Get SDR	Storage (0x0A)	0x23
Get SEL Info	Storage (0x0A)	0x40
Get SEL Entry	Storage (0x0A)	0x43
Add SEL Entry	Storage (0x0A)	0x44
Partial Add SEL Entry	Storage (0x0A)	0x45
Clear SEL	Storage (0x0A)	0x47
Get SEL Time	Storage (0x0A)	0x48
Set SEL Time	Storage (0x0A)	0x49
Set LAN Configuration Parameters	Transport (0x0C)	0x01
Get LAN Configuration Parameters	Transport (0x0C)	0x02
Get Address Info	PICMG (0x2C)	0x01
Get PICMG Properties	PICMG (0x2C)	0x00
FRU Control	PICMG (0x2C)	0x04
Get FRU LED Properties	PICMG (0x2C)	0x05
Get LED Color Capabilities	PICMG (0x2C)	0x06
Set FRU LED State	PICMG (0x2C)	0x07
Get FRU LED State	PICMG (0x2C)	0x08

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Table 48. Supported IPMI commands (Sheet 3 of 3) (continued)

Message commands	NetFn	Command
Set IPMB State	PICMG (0x2C)	0x09
Set FRU Activation Policy	PICMG (0x2C)	0x0A
Get FRU Activation Policy	PICMG (0x2C)	0x0B
Set FRU Activation	PICMG (0x2C)	0x0C
Get Device Locator Record ID	PICMG (0x2C)	0x0D
Set Port State	PICMG (0x2C)	0x0E
Get Port State	PICMG (0x2C)	0x0F
Compute Power Properties	PICMG (0x2C)	0x10
Set Power Level	PICMG (0x2C)	0x11
Get Power Level	PICMG (0x2C)	0x12
Bused Resource	PICMG (0x2C)	0x17
Set AMC Port State	PICMG (0x2C)	0x19
Get AMC Port State	PICMG (0x2C)	0x1A

Managed sensors

The following table describes the sensors managed by the IPMC.

Table 49. Managed sensors (Sheet 1 of 6)

Number	Name	Type	Reading type	Normal reading	Notes
0	ATCA FRU Hotswap	OEM: PICMG FRU Hot Swap	Sensor-specific	0x00–0x07	Return M0 to M7 ATCA hot-swap states.
1	AMC1 FRU Hotswap	OEM: PICMG FRU Hot Swap	Sensor-specific	0x00–0x07	Return M0 to M7 ATCA hot-swap states for AMC bay 1.
2	AMC2 FRU Hotswap	OEM: PICMG FRU Hot Swap	Sensor-specific	0x00–0x07	Return M0 to M7 ATCA hot-swap states for AMC bay 2.
3	RTM FRU Hotswap	OEM: PICMG FRU Hot Swap	Sensor-specific	0x00–0x07	Return M0 to M7 ATCA hot-swap states for the RTM.

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Table 49. Managed sensors (Sheet 2 of 6) (continued)

Number	Name	Type	Reading type	Normal reading	Notes
4	Version Change	Version Change (IPMI 2.0)	Sensor-specific	0x00–0x07	00h = Hardware change detected with associated entity. Informational. This offset does not imply whether the hardware change was successful or not, only that a change occurred. 01h = Firmware or software change detected with associated entity. Informational. Success or failure not implied. 02h = Hardware incompatibility detected with associated entity. 03h = Firmware or software incompatibility detected with associated entity. 04h = Entity is of an invalid or unsupported hardware version. 05h = Entity contains an invalid or unsupported firmware or software version. 06h = Hardware change detected with associated entity was successful (deassertion event means 'unsuccessful'). 07h = Software or firmware change detected with associated entity was successful (deassertion event means 'unsuccessful')
5–11					Reserved
12	Ejector Open	Slot/ Connector	Digital	1	0: Ejector latch is open 1: Ejector latch is closed
13	RTM PRSNT# or RTM Present	Slot/ Connector	Digital	0 or 1	0: RTM is not present 1: RTM is present
14	AMC1 PS1# or AMC1 Present	Slot/ Connector	Digital	0 or 1	0: AMC1 is not present 1: AMC1 is present
15	AMC2 PS1# or AMC2 Present	Slot/ Connector	Digital	0 or 1	0: AMC 2 is not present 1: AMC 2 is present
16	Board Temp 0	Temp	Threshold	25	This sensor measures temperature in ° C. Hysteresis: ±3 Default thresholds LNR[1] = −10, LC[2] = −5, LNC[3] = 0, UNC[4] = 65, UC[5] = 72, UNR[6] = 80
17	Board Temp 1	Temp	Threshold	25	This sensor measures temperature in ° C. Hysteresis: ±3 Default thresholds LNR = −10, LC = −5, LNC = 0, UNC = 65, UC = 72, UNR = 80
18	CPU 0 Temp	Temp	Threshold	25	This sensor measures temperature in ° C. Hysteresis: ±3 Default thresholds LNR = −10, LC = −5, LNC = 0, UNC = 90, UC = 100, UNR = 115

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Table 49. Managed sensors (Sheet 3 of 6) (continued)

Number	Name	Type	Reading type	Normal reading	Notes					
19	CPU 1 Temp	Temp	Threshold	25	This sensor measures temperature in ° C. Hysteresis: ±3					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					–10	–5	0	90	100	115
20	CPU 0 THERMTRIP	Slot/ Connector	Digital	0 or 1	0			1		
					CPU 0 THERMTRIP not asserted			CPU 0 THERMTRIP asserted		
21	CPU 1 THERMTRIP	Slot/ Connector	Digital	0 or 1	0			1		
					CPU 1 THERMTRIP not asserted			CPU 1 THERMTRIP asserted		
22	Board Temp 2	Temp	Threshold	25	This sensor measures temperature in ° C. Hysteresis: ±3					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					–10	–5	0	65	72	80
23	Board Temp 3	Temp	Threshold	25	This sensor measures temperature in ° C. Hysteresis: ±3					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					–10	–5	0	65	72	80
24	CPU 0 PROCHOT	Temp	Threshold	0	This sensor monitors PROCHOT and, when it is asserted, reports a reading of 90. Hysteresis: ±3					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					–15	–10	–5	65	72	100
25	CPU 1 PROCHOT	Temp	Threshold	0	This sensor monitors PROCHOT and, when it is asserted, reports a reading of 90. Hysteresis: ±3					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					–15	–10	–5	65	72	100
26–63					Reserved					
64	PWRGOOD	Slot/ Connector	Digital	0 or 1	0			1		
					Power is not good			Power is good		
65	VCORE 0	Voltage	Threshold	1.04	This sensor measures voltage in Volts. Hysteresis: ±0.02					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					0.00	0.72	0.76	1.30	1.38	1.43
66	VCORE 1	Voltage	Threshold	1.04	This sensor measures voltage in Volts. Hysteresis: ±0.02					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					0.00	0.72	0.76	1.30	1.38	1.43

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Table 49. Managed sensors (Sheet 4 of 6) (continued)

Number	Name	Type	Reading type	Normal reading	Notes					
67	–48V Absent A	Power Supply	Digital	0	0			1		
					Power Supply A Presence detected			Power Supply A Failure detected		
68	–48V Absent B	Power Supply	Digital	0	0			1		
					Power Supply B Presence detected			Power Supply B Failure detected		
69	+12V	Voltage	Threshold	12.00	This sensor measures voltage in Volts. Hysteresis: ±0.25					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					0.00	10.8	11.4	12.6	13.2	13.8
70	+5V	Voltage	Threshold	5.00	This sensor measures voltage in Volts. Hysteresis: ±0.10					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					0.00	4.5	4.76	5.25	5.5	5.74
71	+3.3V	Voltage	Threshold	3.30	This sensor measures voltage in Volts. Hysteresis: ±0.07					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					0.00	2.96	3.13	3.47	3.64	3.81
72	+2.5V	Voltage	Threshold	2.50	This sensor measures voltage in Volts. Hysteresis: ±0.07					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					0.00	2.31	2.43	2.7	2.82	2.96
73	+1.8V	Voltage	Threshold	1.80	This sensor measures voltage in Volts. Hysteresis: ±0.05					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					0.00	1.61	1.72	1.89	1.98	2.07
74	–48V Fuse Fault	Power Supply	Digital	0	0			1		
					Both A & B fuses OK Presence detected			Either A or B fuse blown Failure detected		
75–103					Reserved					
104	+3.3_IPMI	Voltage	Threshold	3.30	This sensor measures voltage in Volts. Hysteresis: ±0.10					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					0.00	2.98	3.15	3.47	3.64	3.78
105	+1.5V	Voltage	Threshold	1.50	This sensor measures voltage in Volts. Hysteresis: ±0.04					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					0.00	1.35	1.44	1.58	1.65	1.73

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Table 49. Managed sensors (Sheet 5 of 6) (continued)

Number	Name	Type	Reading type	Normal reading	Notes					
106	+1.1V_FRONT	Voltage	Threshold	1.20	This sensor measures voltage in Volts. Hysteresis: ±0.02					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					0.00	0.98	1.05	1.14	1.21	1.26
107	+1.1V	Voltage	Threshold	1.10	This sensor measures voltage in Volts. Hysteresis: ±0.02					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					0.00	0.98	1.05	1.14	1.21	1.26
108	+1.05V	Voltage	Threshold	1.05	This sensor measures voltage in Volts. Hysteresis: ±0.02					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					0.00	0.94	1.0	1.10	1.15	1.21
109	+1.2_PESO	Voltage	Threshold	1.20	This sensor measures voltage in Volts. Hysteresis: ±0.05					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					0.00	1.08	1.14	1.26	1.32	1.38
110	–5V	Voltage	Digital	1	0			1		
					–5V not good			–5V good		
111	+5_STANDBY	Voltage	Threshold	5.00	This sensor measures voltage in Volts. Hysteresis: ±0.10					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					0.00	4.5	4.75	5.23	5.49	5.75
112	System Reset	Slot/ Connector	Digital	0 or 1	0			1		
					Deasserted			Asserted		
113	+1.2V (ATCA-4310 only)	Voltage	Threshold	1.20	This sensor measures voltage to the PESO in Volts					
					Default thresholds					
					LNR	LC	LNC	UNC	UC	UNR
					0.00	1.08	1.14	1.26	1.32	1.38
113 or 114–121					Reserved					
122	CPU Reset	Slot/ Connector	Digital	0 or 1	0			1		
					Deasserted			Asserted		
123–126 or127					Reserved					

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Table 49. Managed sensors (Sheet 6 of 6) (continued)

Number	Name	Type	Reading type	Normal reading	Notes	
127	BMC Watchdog (ATCA-4310 only)	Watchdog 2	Sensor-specific	N/A	Sensor-specific event offset = watchdog action: 0 = Timer expired. Status only (no action, no interrupt). 1 = Payload cold reset. 2 = Payload power down. 3 = Payload power cycle. 4–7 = Reserved. 8 = Pre-timer interrupt.	
128	IPMC Watchdog	Slot/ Connector	Digital	0	0	1
					IPMC not reset	IPMC reset due to watchdog
129	ATCAPhysIpmb	OEM: PICMG IPMB Physical Link	Sensor-specific	0x00–0xFF	Bit [7] = IPMB B Override State Bit [6:4] = IPMB B Local Status Bit [3] = IPMB A Override State Bit [2:0] = IPMB A Local Status	
130	ATCAPhysIpmb -L	OEM: RadiSys Physical IPMB-0	Sensor-specific	0x00–0xFF	Bit [7:4] = Reserved Bit [3] = IPMB-L Override State Bit [2:0] = IPMB-L Local Status	
131–139					Reserved	
140	CPU 0 IERR	Slot/ Connector	Digital	0 or 1	0	1
					CPU 0 IERR not asserted	CPU 0 IERR asserted
141	CPU 1 IERR	Slot/ Connector	Digital	0 or 1	0	1
					CPU 1 IERR not asserted	CPU 1 IERR asserted
142	NMI	Slot/ Connector	Digital	0 or 1	0	1
					Deasserted	Asserted
143–159					Reserved	
160–255					Open for dynamically added sensors from AMCs and the RTM	

1 Lower non-recoverable (LNR) threshold generates a critical alarm on the low side.

2 Lower critical (LC) threshold generates a major alarm on the low side.

3 Lower non-critical (LNC) threshold generates a minor alarm on the low side.

4 Upper non-critical (UNC) threshold generates a minor alarm on the high side.

5 Upper critical (UC) threshold generates a major alarm on the high side.

6 Upper non-recoverable (UNR) threshold generates a critical alarm on the high side.

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Sensor alarm troubleshooting

The following table recommends actions to take when the managed sensors generate alarms.

Table 50. Sensor alarms and recommended actions (Sheet 1 of 11)

Number	Name	Alarm level	Possible errors or faults	Recommendation
0	ATCA FRU Hot Swap	N/A	M7 state	Remove CPM and reinsert to see if problem persists. If problem still persists, then remove CPM and contact customer support.
1	AMC1 FRU Hot Swap	N/A	M7 state	Remove CPM and reinsert to see if problem persists. If problem still persists, then remove CPM and contact customer support.
2	AMC2 FRU Hot Swap	N/A	M7 state	Remove CPM and reinsert to see if problem persists. If problem still persists, then remove CPM and contact customer support.
3	RTM FRU Hot Swap	N/A	M7 state	Remove CPM and reinsert to see if problem persists. If problem still persists, then remove CPM and contact customer support.
4	Version Change	N/A	Sensor puts an event into the SEL when a change as been detected.	No action required; information only.
5-11		N/A		
12	Ejector Open	N/A	None	No action required; information only.
13	RTM PRSNT#	N/A	None	No action required; information only.
14	AMC1 PS1#	N/A	None	No action required; information only.
15	AMC2 PS1#	N/A	None	No action required; information only.
16	Board Temp 0	Minor temperature high	Temperature over 65°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 72°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 80°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under 0°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -5°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -10°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.

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Table 50. Sensor alarms and recommended actions (Sheet 2 of 11) (continued)

Number	Name	Alarm level	Possible errors or faults	Recommendation
17	Board Temp 1	Minor temperature high	Temperature over 65°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 72°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 80°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under 0°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -5°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -10°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
18	CPU 0 Temp	Minor temperature high	Temperature over 90°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 100°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 115°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under 0°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -5°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -10°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.

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Table 50. Sensor alarms and recommended actions (Sheet 3 of 11) (continued)

Number	Name	Alarm level	Possible errors or faults	Recommendation
19	CPU 1 Temp	Minor temperature high	Temperature over 90°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 100°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 115°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under 0°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -5°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -10°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
20	CPU 0 THERMTRIP	N/A	CPM3 over temperature event	Check other CPU Temp sensors. Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
21	CPU 1 THERMTRIP	N/A	CPM3 over temperature event	Check other CPU Temp sensors. Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
22	Board Temp 2	Minor temperature high	Temperature over 65°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 72°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 80°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under 0°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -5°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -10°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.

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Table 50. Sensor alarms and recommended actions (Sheet 4 of 11) (continued)

Number	Name	Alarm level	Possible errors or faults	Recommendation
23	Board Temp 3	Minor temperature high	Temperature over 65°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 72°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 80°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under 0°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -5°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -10°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
24	CPU 0 PROCHOT	Minor temperature high	Temperature over 65°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 72°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 100°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under -5°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -10°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -15°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.

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Table 50. Sensor alarms and recommended actions (Sheet 5 of 11) (continued)

Number	Name	Alarm level	Possible errors or faults	Recommendation
25	CPU 1 PROCHOT	Minor temperature high	Temperature over 65°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 72°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 100°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under -5°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -10°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -15°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
26-63		N/A		
64	PWRGOOD	N/A	Power problem	Monitor to see if the alarm worsens or is persistent for more than 1 day.
65	VCORE 0	Minor voltage high	Voltage over 1.30V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.38V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 1.43V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 0.76V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 0.72V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.

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Table 50. Sensor alarms and recommended actions (Sheet 6 of 11) (continued)

Number	Name	Alarm level	Possible errors or faults	Recommendation
66	VCORE 1	Minor voltage high	Voltage over 1.30V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.38V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 1.43V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 0.76V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 0.72V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
67	-48V Absent A	N/A	Voltage from -48V power source 'A' is not healthy.	Investigate power loss
68	-48V Absent B	N/A	Voltage from -48V power source 'B' is not healthy.	Investigate power loss
69	+12V	Minor voltage high	Voltage over 12.6V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 13.2V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 13.8V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 11.4V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 10.8V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
70	+5V	Minor voltage high	Voltage over 5.25V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 5.5V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 5.74V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 4.76V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 4.5V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.

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Table 50. Sensor alarms and recommended actions (Sheet 7 of 11) (continued)

Number	Name	Alarm level	Possible errors or faults	Recommendation
71	+3.3V	Minor voltage high	Voltage over 3.47V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 3.64V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 3.81V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 3.13V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 2.96V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
72	+2.5V	Minor voltage high	Voltage over 2.7V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 2.82V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 2.96V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 2.43V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 2.31V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
73	+1.8V	Minor voltage high	Voltage over 1.89V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.98V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 2.07V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 1.72V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 1.61V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
74	-48V Fuse Fault	N/A	A -48V fuse is not functioning.	Check the -48V fuses. Contact customer support if a replacement fuse is required.
75-103		N/A		

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Table 50. Sensor alarms and recommended actions (Sheet 8 of 11) (continued)

Number	Name	Alarm level	Possible errors or faults	Recommendation
104	+3.3_IPMI	Minor voltage high	Voltage over 3.47V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 3.64V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 3.78V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 3.15V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 2.98V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
105	+1.5V	Minor voltage high	Voltage over 1.58V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.65V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 1.73V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 1.44V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 1.35V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
106	+1.1V_FRONT	Minor voltage high	Voltage over 1.14V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.21V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 1.26V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 1.05V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 0.98V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.

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Table 50. Sensor alarms and recommended actions (Sheet 9 of 11) (continued)

Number	Name	Alarm level	Possible errors or faults	Recommendation
107	+1.1V	Minor voltage high	Voltage over 1.14V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.21V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 1.26V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 1.05V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 0.98V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
108	+1.05V	Minor voltage high	Voltage over 1.10V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.15V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 1.21V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 1.0V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 0.94V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
109	+1.2_PESO	Minor voltage high	Voltage over 1.26V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.32V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 1.38V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 1.14V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 1.08V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
110	-5V	N/A	-5V problem event	Remove CPM and investigate power rail error.

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Table 50. Sensor alarms and recommended actions (Sheet 10 of 11) (continued)

Number	Name	Alarm level	Possible errors or faults	Recommendation
111	+5_STANDBY	Minor voltage high	Voltage over 5.24V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 5.49V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 5.75V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 4.75V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 4.5V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
112	System Reset	N/A	Payload cold reset from watchdog BIOS/OS event or reboot	Investigate why system reset, look at the events in the SEL, and monitor CPM.
113	+1.2V (ATCA-4310 only)	Minor voltage high	Voltage over 1.26V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.32V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 1.38V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 1.14V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 1.08V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
113 or 114–121		N/A		
122	CPU Reset	N/A	Payload warm reset from command or front panel reset button	Monitor to see if the alarm worsens or is persistent for more than 1 day.
123–126 or 127		N/A		
127	BMC Watchdog (ATCA-4310 only)	N/A	Missing strobe from the application to the BMC watchdog	Verify that the application strobing the watchdog is running. Check communications between the watchdog and IPMC.
128	IPMC Watchdog	N/A	Missing strobe from the IPMC to the IPMC FPGA	Monitor to see if the event occurs again or becomes frequent.
129	ATCAPhys Ipmb	N/A	I2C data or clock lines problem	Investigate bus communication error. Possibly remove CPM and reinsert.
130	ATCAPhys Ipmb-L	N/A	I2C data or clock lines problem	If IPMB-L bus does not recover on its own, hot swap CPM, and/or remove AMCs until problem is resolved.
131–139		N/A		

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Table 50. Sensor alarms and recommended actions (Sheet 11 of 11) (continued)

Number	Name	Alarm level	Possible errors or faults	Recommendation
140	CPU 0 IERR	N/A	IERR CPU error	Investigate error
141	CPU 1 IERR	N/A	IERR CPU error	Investigate error
142	NMI	N/A	NMI generated	Investigate error
143–159		N/A		

[1] Any voltage alarm during CPM bootup keeps the CPM in M3 state. If the CPM has already reached M4 state when the alarm occurs, it remains in M4 state.

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LOW-LEVEL HARDWARE MAP E

This appendix provides details for the CPM input/output, main memory maps, and SMBus maps. Additional information is provided for the PCI bus device map, including interrupt lines for the PCI device peripherals. This appendix provides crucial information for the developer who needs to know memory locations of the peripheral devices and their interrupt routing.

Main memory map

After the boot process has been completed, the physical addresses from the CPU are mapped into memory according to the following table. Regions that are routed to the PCI bus will get routed to the LPC interface if no PCI device claims the transaction.

Additionally, the table provides CPU memory ranges for the ICH to decode. When cycles arrive from the hub interface and are not directed to any of the internal memory targets that decode directly from the memory controller hub interface, they are sent to the PCI. The ICH may then claim the cycle for forwarding to the LPC, or the ICH may be claimed by the internal APIC. If subtractive decode is enabled, the cycle can be forwarded to the LPC bridge.

Table 51. Main memory map

CPU address	Region	Cacheable?
0x00000000–0x0009FFFF	Base 640KB	Yes
0x000A0000–0x000BFFFF	Video memory (if used)	No
0x000C0000-0x000CXXXX	Video BIOS (if used)	Yes
0x000CXXXX–0x000DFFFF	Shadowed Extension BIOS	Yes
0x000E0000-0x000FFFFF	Shadowed System BIOS runtime code	Yes
0x00100000–TOM (top of memory)	DRAM (1MB up to 16GB) Some memory may be remapped to exclude PCI mapped devices	Yes
TOLM–0xDFFFFFFF	PCI (Memory mapped I/O devices)	Yes
0xE0000000–0xEFFFFFFF	PCI Express Enhanced Configuration Aperture	No
0xFEC00000–0xFEC7FFFF	IOAPIC0 IOxAPIC (HI)	No
0xFEC80000–0xFEC80FFF	IOAPIC2 IOxAPIC (PCI Express A)	No
0xFEC81000–0xFEC81FFF	IOAPIC3 IOxAPIC (PCI Express A1)	No
0xFEC82000–0xFEC82FFF	IOAPIC4 IOxAPIC (PCI Express B)	No
0xFEC83000–0xFEC83FFF	IOAPIC5 IOxAPIC (PCI Express B1)	No
0xFEC84000–0xFEC84FFF	IOAPIC6 IOxAPIC (PCI Express C)	No
0xFEC85000–0xFEC85FFF	IOAPIC7 IOxAPIC (PCI Express C1)	No
0xFED40000–0xFED40FFF	Trusted Platform Module	No
0xFEDA0000–0xFEDBFFFF	High SMM memory space	No
0xFEE00000–0xFEEFFFFF	Local APIC Unit	No

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Table 51. Main memory map (continued)

CPU address	Region	Cacheable?
0xFEF00000–0xFFBFFFFF	PCI (memory mapped I/O devices)	No
0xFFC00000–0xFFDFFFFF	FWH 1	No
0xFFE00000–0xFFFFFFFF	FWH 0	No

PCI bus device map

The following table provides device identification for the CPM's peripheral connections.

Table 52. PCI device map

Peripheral	Device ID	Device #	Func #	Bus #	ICH INTR mapping	Enabled?
Memory controller hub (MCH) I/F	0x3590	0	0	0	N.A.	Yes
MCH Error Reporting (Hub I/F)	0x3591	0	1	0	N.A.	Yes
MCH DMA Controller	0x3594	1	0	0	N.A.	Yes
MCH Host-to-PCI Express A0 Bridge	0x3595	2	0	0	N.A.	Yes
MCH Host-to-PCI Express A1 Bridge	0x3596	3	0	0	N.A.	Yes
MCH Host-to-PCI Express B0 Bridge	0x3597	4	0	0	N.A.	Yes
MCH Host-to-PCI Express B1 Bridge	0x3598	5	0	0	N.A.	Yes
MCH Host-to-PCI Express C0 Bridge	0x3599	6	0	0	N.A.	Yes
MCH Host-to-PCI Express C1 Bridge	0x359A	7	0	0	N.A.	Yes
MCH Extended Configuration Registers	0x359B	8	0	0	N.A.	Yes
I/O controller hub (ICH) I/F to PCI Bridge	0x244E	30	0	0	N.A.	Yes
ICH PCI to LPC Bridge	0x25A1	31	0	0	N.A.	Yes
ICH SATA Controller	0x25A3	31	2	0	N.A.	Yes
ICH SMBus Controller	0x25A4	31	3	0	N.A.	Yes
ICH USB UHCI #1	0x25A9	29	0	0	N.A.	Yes
ICH USB UHCI #2	0x25AA	29	1	0	N.A.	No
ICH WDT	0x25AB	29	4	0	N.A.	Yes
ICH IOxAPIC	0x25AC	29	5	0	N.A.	Yes
ICH USB EHCI	0x25AD	29	7	0	N.A.	Yes
I/O controller hub I/F to PCI-X Bridge	0x25AE	28	0	0	N.A.	No

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Interrupts

This section describes I/O controller hub interrupts, system bus interrupts, and PIC-mode interrupt assignment.

I/O controller hub interrupts

The I/O controller hub (ICH) provides the following interrupts: the system timer, RTC, serial ports, and DMA channels. In addition, the interrupt controller can support the PCI-based interrupts by mapping the PCI interrupt onto the compatible ISA interrupt line.

The ICH supports the following interrupt features:

- 8 possible PCI interrupt pins
- PCI 2.2 Message Signaled interrupts
- Two cascaded interrupt controllers with 15 interrupts
- Integrated I/O APIC capability with 24 interrupts
- Serial Interrupt Protocol

System bus interrupts

The CPU processors only support the PIC and Processor System Bus Interrupt Delivery modes. When the CPM boots up in the standard PIC mode, it switches over to Processor System Bus Interrupt Delivery mode. Processing interrupts are handled as a 32-bit memory write cycle to PCI and to the host controller with the CPU “snooping” the cycle to get all the information it needs to process the interrupt. The switch from PIC mode to Processor System Bus Interrupt Delivery mode is performed in the OS.

Front Side Bus interrupts may originate in one of the CPUs as an IPI (interprocessor interrupt), or from a downstream device on either the hub interface or one of the PCI Express ports.

Any device below the HI or a PCI Express port may also issue an interrupt directly with a memory write to the system bus interrupt space (0_FEE0_0000 to 0_FEEF_FFFF). The memory controller hub will forward the write to the system bus as an MSI transaction.

When the CPM is booting and in PIC mode, interrupts from PCI Express devices are passed to the CPU normally. PIC mode does not affect the interrupt delivery from the MCH to the CPUs.

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A list of interrupts for the ICH is provided in the following table.

Table 53. Connection of interrupts

Device	Index	Index within device	Pin	Signal name	Description
6300ESB (APIC 0)		0	–	<Internal>	Cascade from 8259 #1
		2	–	<Internal>	8254 Counter 0, MMT #0
		8	–	<Internal>	RTC, MMT #1
		16	PIRQ[A]*	<Internal>	USB 1.1 UCHI Controller #1
		17	PIRQ[B]*	MESSAGE_INT_BACKUP	Optional messaging interrupt from the IPMC
		18	PIRQ[C]*	Not used	N.A.
		19	PIRQ[D]*	<Internal>	USB 1.1 UCHI Controller #2
		20	PIRQ[E]*	Not used	N.A.
		21	PIRQ[F]*	Not used	N.A.
		22	PIRQ[G]*	NTS_INT*	NTS Interrupt
		23	PIRQ[H]*	<Internal>	USB 2.0 EHCI Controller
6300ESB (APIC 1)		0	PXIRQ0	INT_0	RTM Interrupt
		1	PXIRQ1	INT_1	RTM Interrupt
		2	PXIRQ2	Not used	N.A.
		3	PXIRQ3	Not used	N.A.
		10	WDT	<Internal>	Interrupt from WDT

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Interrupt assignment in PIC mode

This table lists the signals connected to the legacy-compatible Programmable Interrupt Controllers (PIC).

Table 54. IRQ map for PIC

Legacy 8259	Input	Interrupt source	Pin/function
Master	0	Internal	Internal Timer / Counter 0 / MMT #0
	1		
	2	Internal	Slave Controller INTR output
	3	UART0	Internal
	4	UART1	Internal
	5		
	6	IPMC	IPMI messaging interrupt
	7		
Slave	0	Internal Real Time Clock	Internal RTC / MMT #1
	1		
	2		
	3		
	4		
	5	Internal	FERR*
	6	Primary IDE cable	IRQ14 from input signal
	7		

PCI Interrupts can be assigned to any of the empty IRQs. APIC interrupts are configured by the system BIOS.

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I/O map

The hub interface cycles that go to target ranges that are marked as "RESERVED" are not decoded by the ICH; they are passed to the PCI. If a PCI master targets one of the fixed I/O target ranges, it is positively decoded by the ICH in Medium speed. Address ranges that are not marked or specified in the following table are not decoded by the ICH unless assigned to one of the variables ranges.

Table 55. I/O address map

I/O address	Read target	Write target	Functional unit	Location
0x00–0x08	DMA Controller	DMA Controller	DMA	ICH
0x09–0x0E	RSVD	DMA Controller	DMA	ICH
0x0F	DMA Controller	DMA Controller	DMA	ICH
0x10–0x18	DMA Controller	DMA Controller	DMA	ICH
0x19–0x1E	RSVD	DMA Controller	DMA	ICH
0x1F	DMA Controller	DMA Controller	DMA	ICH
0x20–0x21	Interrupt Controller	Interrupt Controller	Interrupt	ICH
0x24–0x25	Interrupt Controller	Interrupt Controller	Interrupt	ICH
0x28–0x29	Interrupt Controller	Interrupt Controller	Interrupt	ICH
0x2C–0x2D	Interrupt Controller	Interrupt Controller	Interrupt	ICH
0x2E–0x2F	LPC SIO	LPC SIO	Forwarded to LPC	
0x30–0x31	Interrupt Controller	Interrupt Controller	Interrupt	ICH
0x34–0x35	Interrupt Controller	Interrupt Controller	Interrupt	ICH
0x38–0x39	Interrupt Controller	Interrupt Controller	Interrupt	ICH
0x3C–0x3D	Interrupt Controller	Interrupt Controller	Interrupt	ICH
0x40–0x42	Timer/Counter	Timer/Counter	PIT (8254)	ICH
0x43	RSVD	Timer/Counter	PIT	ICH
0x4E–0x4F	LPC SIU (UARTs)	LPC SIU (UARTs)	Forwarded to LPC	ICH
0x50–0x52	Timer/Counter	Timer/Counter	PIT	ICH
0x53	RSVD	Timer/Counter	PIT	ICH
0x60	µcontroller/Emulation	µcontroller/Emulation	Forwarded to LPC	
0x61	NMI Controller	NMI Controller	CPU I/F	ICH
0x62	µcontroller/Emulation	µcontroller/Emulation	Forwarded to LPC	
0x63	NMI Controller	NMI Controller	CPU I/F	ICH
0x64	µcontroller/Emulation	µcontroller/Emulation	Forwarded to LPC	
0x65	NMI Controller	NMI Controller	CPU I/F	ICH
0x66	µController/Emulation	µcontroller/Emulation	Forwarded to LPC	
0x67	NMI Controller	NMI Controller	CPU I/F	ICH
0x70	RSVD	NMI and RTC Controller	RTC	ICH
0x71	RTC Controller	RTC Controller	RTC	ICH
0x72	RTC Controller	NMI and RTC Controller	RTC	ICH
0x73	RTC Controller	RTC Controller	RTC	ICH

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Table 55. I/O address map (continued)

I/O address	Read target	Write target	Functional unit	Location
0x74	RTC Controller	NMI and RTC Controller	RTC	ICH
0x75	RTC Controller	RTC Controller	RTC	ICH
0x76	RTC Controller	NMI and RTC Controller	RTC	ICH
0x77	RTC Controller	RTC Controller	RTC	ICH
0x80	LPC or PCI	LPC or PCI	Port 80 Diagnostic	Port 80 Card
0x81–0x83	DMA Controller	DMA Controller	DMA	ICH
0x84–0x86	DMA Controller	DMA Controller and LPC or PCI	DMA	ICH
0x87	DMA Controller	DMA Controller	DMA	ICH
0x88	DMA Controller	DMA Controller and LPC or PCI	DMA	ICH
0x89–0x8B	DMA Controller	DMA Controller	DMA	ICH
0x8C–0x8E	DMA Controller	DMA Controller and LPC or PCI	DMA	ICH
0x08F	DMA Controller	DMA Controller	DMA	ICH
0x90–0x91	DMA Controller	DMA Controller	DMA	ICH
0x92	Reset Generator	Reset Generator	CPU I/F	ICH
0x93–0x9F	DMA Controller	DMA Controller	DMA	ICH
0xA0–0xA1	Interrupt Controller	Interrupt Controller	Interrupt	ICH
0xA4–0xA5	Interrupt Controller	Interrupt Controller	Interrupt	ICH
0xA8–0xA9	Interrupt Controller	Interrupt Controller	Interrupt	ICH
0xAC–0xAD	Interrupt Controller	Interrupt Controller	Interrupt	ICH
0xB0–0xB1	Interrupt Controller	Interrupt Controller	Interrupt	ICH
0xB2–0xB3	Power Management	Power Management	Power Management	ICH
0xB4–0xB5	Interrupt Controller	Interrupt Controller	Interrupt	ICH
0xB8–0xB9	Interrupt Controller	Interrupt Controller	Interrupt	ICH
0xBC–0xBD	Interrupt Controller	Interrupt Controller	Interrupt	ICH
0xC0–0xD1	DMA Controller	DMA Controller	DMA	ICH
0xD2–0xDD	RSVD	DMA Controller	DMA	ICH
0xDE–0xDF	DMA Controller	DMA Controller	DMA	ICH
0xF0	See Note	FERR* / IGNNE* / Interrupt Controller	CPU I/F	ICH
0x170–0x177	IDE Controller	IDE Controller	Forwarded to IDE	ICH
0x1F0–0x1F7	IDE Controller	IDE Controller	Forwarded to IDE	ICH
0x200–0x207	Gameport Low	Gameport Low	Forwarded to LPC	
0x208–0x20F	Gameport High	Gameport High	Forwarded to LPC	
0x376	IDE Controller2	IDE Controller2	Forwarded to IDE	ICH
0x388–0x38B	Ad Lib	Ad Lib	Forwarded to LPC	
0x3F6	IDE Controller2	IDE Controller2	Forwarded to IDE	ICH
0x4D0–0x4D1	Interrupt Controller	Interrupt Controller	Interrupt	ICH
0xCA2–0xCA3	IPMC KCS I/O	IPMC KCS I/O	Forward to LPC	IPMC
0xCF9	Reset Generator	Reset Generator	CPU I/F	ICH

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SMBus map

The following diagram and table provide the SMBus connections and addresses.

Figure 27. SMBus devices

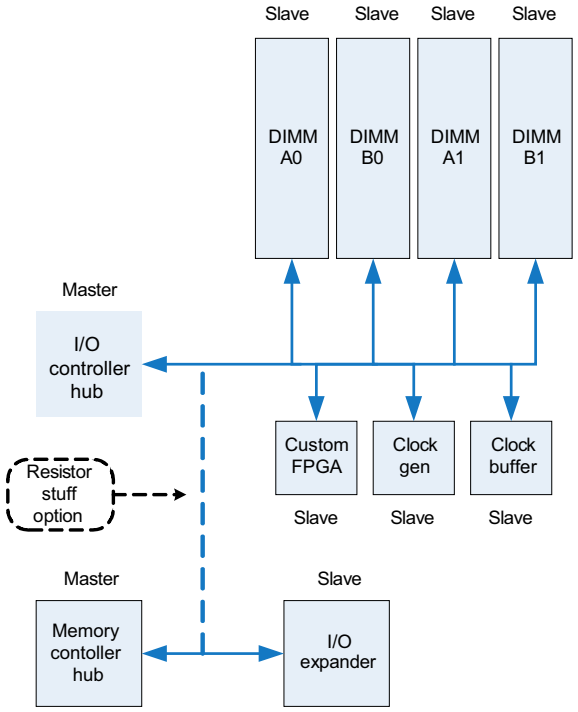


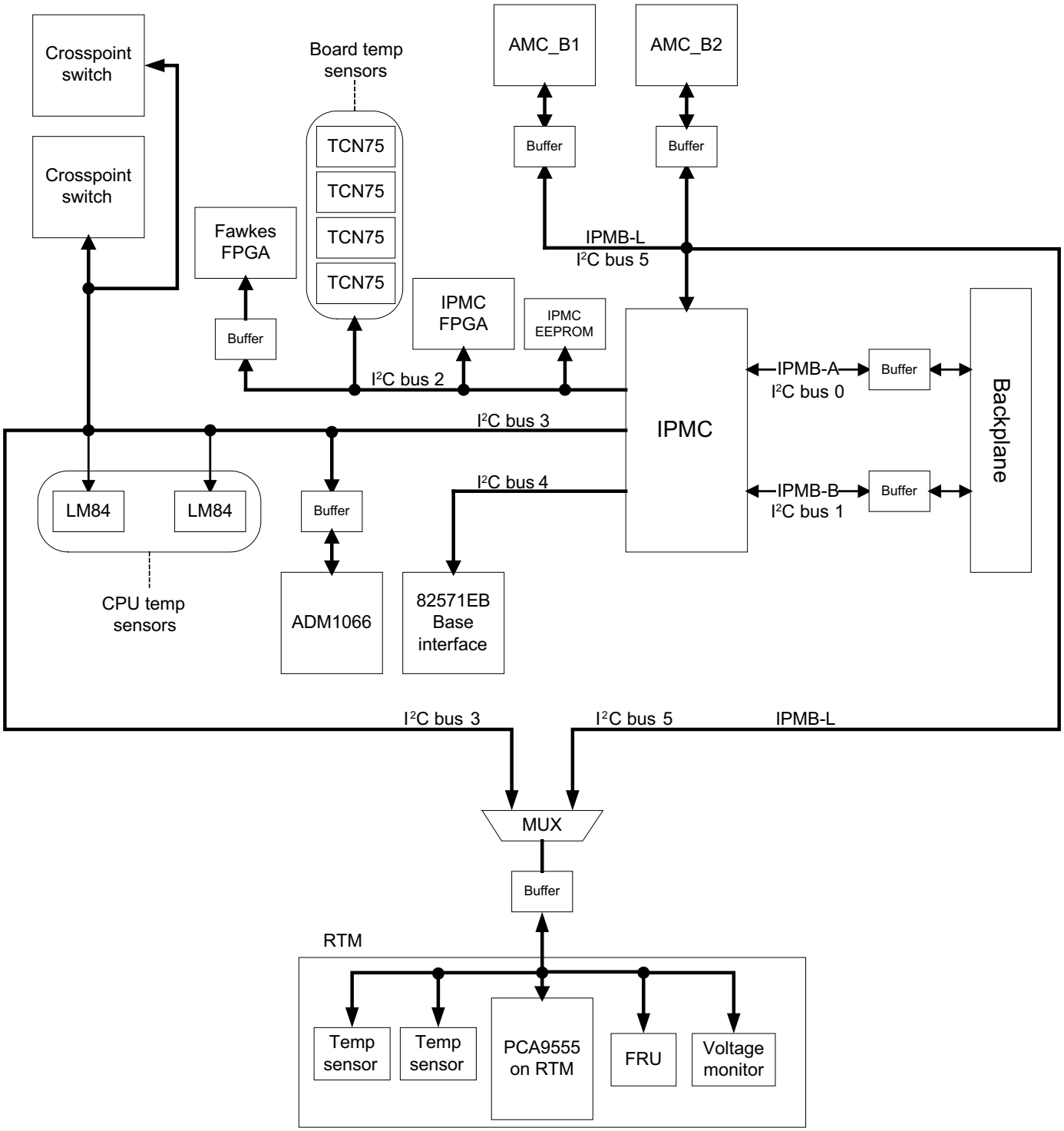
Table 56. SMBus device addresses

Device	Role	Read address	Write address
6300ESB	Master	*not applicable*	*not applicable*
Fawkes	Slave	D1h	D0h
Fawkes NTS registers	Slave	B3h	B2h
DIMM A1	Slave	A5h	*not applicable*
DIMM B1	Slave	A7h	*not applicable*
DIMM A0	Slave	A9h	*not applicable*
DIMM B0	Slave	ABh	*not applicable*
DB800 clock buffer	Slave	DDh	DCh
CK409 clock gen	Slave	D3h	D2h
E7520	Master	*not applicable*	*not applicable*
PSA9555 (MCH SMBus)	Slave	01h	00h

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IPMC I²C map

The following diagram and table provide the IPMC I²C connections and addresses.



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Table 57. I²C device addresses

Device	Master / slave	Bus #	Read address	Write address
IPMC EEPROM	Slave	2	A1h	A0h
IPMC FPGA	Slave	2	C1h	C0h
TCN75 (Temp 0)	Slave	2	9Fh	9Eh
TCN75 (Temp 1)	Slave	2	9Dh	9Ch
TCN75 (Temp 2)	Slave	2	9Bh	9Ah
TCN75 (Temp 3)	Slave	2	99h	98h
Fawkes FPGA	Slave	2	B1h	B0h
Fawkes NTS registers	Slave	2	B3h	B2h
ADM1066	Slave	3	69h	68h
LM84_CPU0	Slave	3	99h	98h
LM84_CPU1	Slave	3	9Dh	9Ch
3312 Crosspoint (AMC)	Slave	3	B1h	B0h
3312 Crosspoint (PESO)	Slave	3	B3h	B2h
3304 Crosspoint (update channel)	Slave	3	1Fh	1Eh
PCA9555 (RTM)	Slave	3	41h	40h
FRU EEPROM (RTM)	Slave	3	AFh	AEh
Voltage monitor (RTM)	Slave	3	45h	44h
Temp sensor (RTM)	Slave	3	9Fh	9Eh
Temp sensor (RTM)	Slave	3	9Bh	9Ah
82571EB (Base) LAN0	Slave	4	21h	20h
82571EB (Base) LAN1	Slave	4	23h	22h
AMC_B1 MMC	Master/Slave	5	GA[2:0] = UGU; IPMB-L Address = 7Ah	
AMC_B2 MMC	Master/Slave	5	GA[2:0] = UUG; IPMB-L Address = 7Ch	

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