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PROMENTUM®

COMPUTE PROCESSING MODULE

REFERENCE

ATCA-4500



RadiSys
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Release	Date	Description
-0000	August 2009	First release.

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About this manual

This manual describes the Promentum® ATCA-4500, a compute processing module (CPM) that is fully compliant with AdvancedTCA® (PICMG 3.0 Advanced Telecommunications Computing Architecture R2.0). The module is designed to be incorporated into high availability (HA) systems, such as the Promentum SYS-6006 and SYS-6010.

Use this manual as a reference for the operation and maintenance of the ATCA-4500 CPM. The material presented here is not introductory; it assumes you are already familiar with the intended use of the ATCA-4500 in your organization's ATCA platform.

For instructions on initial setup of the ATCA-4500, see the *ATCA-4500 Compute Processing Module Installation Guide*.

The simplified name of "CPM" or "module" is used in place of "ATCA-4500 Compute Processing Module" and "ATCA-4500" in this manual.

Notational conventions

This manual uses the following conventions

BoldText	A keyword.
ItalicText	File, function, and utility names.
`MonoText`	Screen text and syntax strings.
`BoldMonoText`	A command to enter.
`ItalicMonoText`	Variable parameters.
Brackets [ ]	Command options.
Curly braces { }	A grouped list of parameters.
Vertical line |	An "OR" in the syntax. Indicates a choice of parameters.

All numbers are decimal unless otherwise stated.

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Electrostatic discharge

WARNING! This product contains static-sensitive components and should be handled with care. Failure to employ adequate anti-static measures can cause irreparable damage to components.

Electrostatic discharge (ESD) damage can result in partial or complete device failure, performance degradation, or reduced operating life. To avoid ESD damage, the following precautions are strongly recommended.

- Keep each module in its ESD shielding bag until you are ready to install it.
- Before touching a module, attach an ESD wrist strap to your wrist and connect its other end to a known ground.
- Handle the module only in an environment that has its working surfaces, floor coverings, and chairs connected to a known ground.
- Hold the module only by its edge and mounting hardware. Avoid touching PCB components and connector pins.

For further information on ESD, visit www.esda.org.

Related manuals

See the following resources for information on the CPM not described in this manual:

- **Installation and initial setup instructions**. The *ATCA-4500 Compute Processing Module Installation Guide* provides the steps for installing the module into a shelf and completing the initial configuration.
- **Software reference information**. The *Software Guide for Management Processors and General Purpose Computing Processors* describes software concepts and serves as a reference for procedural and usage information. When referenced in this manual, the simplified name of *Software Guide* will be used. The *ATCA-4500 CPM BIOS Crisis Recovery Instructions* explain how to recover if the BIOS is corrupted in both of the redundant banks.
- **Command line interface (CLI) reference information**. The *Command Line Interface Reference* describes the master CLI and its command modes, and serves as a reference for command syntax and options. When referenced in this manual, the simplified name of *CLI Reference* will be used.
- **Developer information**. The *RadiSys Developer's Guide* provides background concepts and tasks for assembling flash images and file systems from vendor and RadiSys RPMs, performing post-configuration on the file systems for a particular module, rebuilding RadiSys software, and integrating everything into vendor development environments.
- **Update information**. Firmware and software updates may be available for the CPM components from time to time. For information on updating components on the CPM and other modules, see the *Firmware and Software Update Instructions*.

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Where to get more product information

Visit the RadiSys Web site at www.radisys.com for product information and other resources. Downloads (manuals, release notes, software, etc.) are available at www.radisys.com/downloads.

About related RadiSys products

The CPM is part of the Promentum family of products. For information on the Promentum product family and other RadiSys products, see the RadiSys Web site at www.radisys.com.

Standards information

For information about the PCI Industrial Computer Manufacturers Group (PICMG) and the AdvancedTCA standard, consult the PICMG Web site at this URL:

http://www.picmg.org

For more information about IPMI and the IPMI standards, consult the Intel Web site at this URL:

http://developer.intel.com/design/servers/ipmi

For information about SCSI storage interfaces (i.e., SAS and SATA), consult the Web site of the International Committee for Information Technology Standards (INCITS) at this URL:

http://www.incits.org

Related Documents

CAN/CSA 22.2 #60950-1-03 Safety for Information Technology Equipment, CSA

EN 60950-1:2002 Safety for Information Technology Equipment, CENELEC

GR-1089-CORE Electromagnetic Compatibility and Electrical Safety—Generic Criteria for Network Telecommunications Equipment, Issue 4, June 2006, Telcordia

GR-63-CORE NEBS Requirements Physical Protection, Issue 3, March 2006, Telcordia

GR-78-CORE Generic Requirements for the Physical Design and Manufacture of Telecommunications Products and Equipment, Issue 1, September 1997, Telcordia

IEC 60950-1 Safety for Information Technology Equipment, IEC

Intel® Low Pin Count Interface Specification, Revision 1.1

IPMI Intelligent Platform Management Interface Specification, v1.5; Revision 1.1, February 20, 2002; Revision 1.1 Markup, June 1, 2004

IPMI Platform Management FRU Information Storage Definition, v1.0, Revision 1.1, September 27, 1999

PICMG 3.0 Revision 2.0 AdvancedTCA® Base Specification, ECN-002, PCI Industrial Computer Manufacturers Group, May 19, 2006

PICMG AMC.0 R2.0 Advanced Mezzanine Card Base Specification, PCI Industrial Computer Manufacturers Group, November 15, 2006

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PICMG AMC.1 R1.0 PCI Express and Advanced Switching on AdvancedMC, PCI Industrial Computer Manufacturers Group, January 20, 2005

PICMG AMC.2 R1.0 Ethernet Advanced Mezzanine Card Specification, PCI Industrial Computer Manufacturers Group, March 1, 2007

PICMG AMC.3 R1.0 Advanced Mezzanine Card Specification for Storage, PCI Industrial Computer Manufacturers Group, August 25, 2005

PICMG® 3.1 R1.0 Ethernet/Fibre Channel over PICMG 3.0, PICMG

Serial Attached SCSI-2 (SAS-2) Specification (T10/1760-D Revision 15); ISO/IEC 14776-152:200x, November 19, 2008

SR-3580 Network Equipment–Building Systems (NEBS) Criteria Levels, Issue 2, January 2005, Telcordia

UL 60950-1 Safety for Information Technology Equipment

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PRODUCT OVERVIEW 1

The Promentum ATCA-4500 Compute Processing Module (CPM) is a high-end, general-purpose computing module that provides multi-core processing power and multiple data-storage options within a single slot. The CPM can be used as a stand-alone ATCA computing module, or it can be put to use serving blade-server applications.

The CPM uses an Intel® Xeon® processor with hyper-threading technology and an integrated memory controller, which gives the CPM access to up to 64 GB of memory. The CPM can host a mid-height advanced mezzanine card (AMC), supporting Ethernet, PCI Express, SAS, and SATA connections to the AMC. The CPM can also provide additional I/O connections through an optional rear transition module (RTM) that contains a SAS hard disk drive.

The CPM comes with an extensible firmware interface (EFI) compliant BIOS that includes an EFI shell. The EFI shell allows command and script execution before operating system initialization. The CPM runs a Linux operating system, which is supported by RadiSys Promentum software packages.

The ATCA-4500 CPM is compatible with the PICMG® 3.0 Advanced Telecommunications Computing Architecture (ATCA) specification. The CPM supports dual 1-gigabit Ethernet (GbE) links for the Base interface that are PICMG 3.0 compliant, and dual 10 GbE links for the Fabric interface that are PICMG 3.1 (option 1 or 9) compliant.

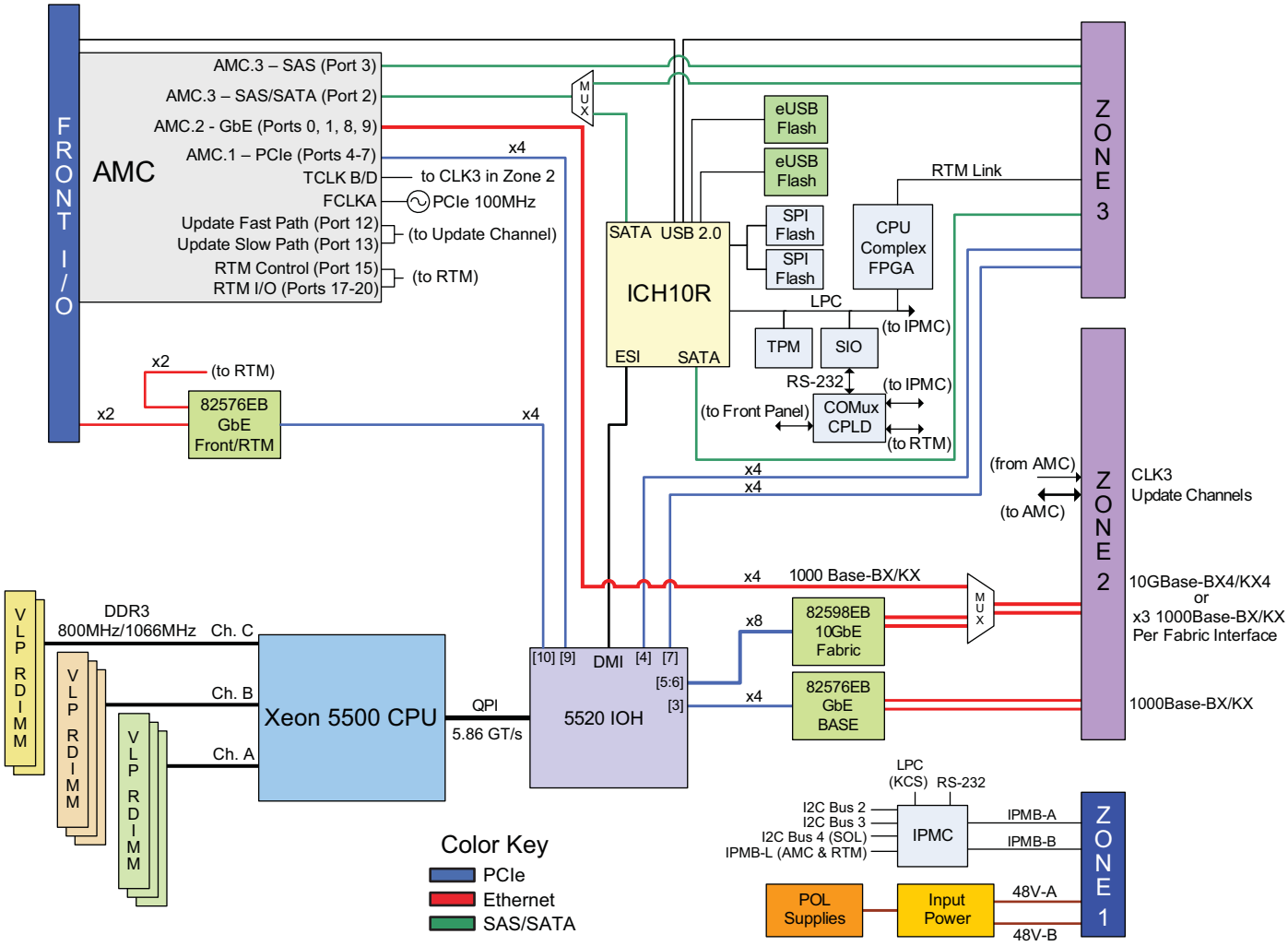
Block diagram

Figure 1 on page 12 illustrates the CPM's major functional blocks. *Chapter 4, Components and Subsystems,* on page 27 contains detailed information about how the CPM functions.

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Figure 1. ATCA-4500 CPM functional blocks

Front I/O
(2) USB 2.0
(1) RS-232 (RJ-45)
(2) 10/100/1000 Ethernet (RJ-45)
Reset Switch
ATCA LEDs



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Quad-core processor with integrated memory controller

For central processing operations, the CPM uses the Intel® Xeon® 5500 series processor and an integrated memory controller. For detailed information about the processor and memory controller, see *Processor and memory controller* on page 27.

Memory and data storage options

The CPM provides 8 VLP DIMM sockets to support ECC memory options ranging from 1 GB to 64 GB. The CPM supports up to 64 GB of DDR3 memory when running at 800MHz, and up to 48 GB at 1066MHz.

Memory storage is also provided through two banks of optional user flash memory (eUSB) that can be configured for up to 16 GB each.

The CPM can be configured with additional storage options. For details, see *Memory and storage devices* on page 29.

I/O capabilities

The CPM uses the Intel 5520 chipset in conjunction with the ICH10R I/O controller hub to interface with peripheral input and output devices.

The CPM front panel provides:

- Two USB 2.0 compliant ports for connecting peripheral devices.
- Two 10/100/1000 copper Ethernet ports for network communications.
- One RS-232 serial port for console operations.

Refer to *Front panel LEDs, buttons, and ports* on page 19 for more information about the front panel, and to *Backplane interfaces* on page 24 for information on the backplane.

The CPM provides backplane interfaces for Base and Fabric ports, AMC ports, synchronization clocks, and the IPMB connections. Features include:

- Two GbE/10 GbE ports for the Fabric interface
- Support for quad GbE connections from the AMC to the Fabric interface. The AMC has two GbE ports for each Fabric interface.

The CPM can be configured with a rear transition module (RTM), an optional device that provides additional Zone 3 connectivity to the CPM via the SAS ports. For information about RTM features, refer to the *ATCA-5400 RTM Reference*.

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Hardware management

The function and operation of the CPM hardware management subsystem is controlled by the Intelligent Platform Management Controller (IPMC). The IPMC manages these functions:

- System event log (SEL)
- Remote executable flash and microcontroller software upgrade support.
- Electronic keying support for Fabric interface, synchronization clocks, and update channels.
- Serial-over-LAN (SOL) support via the Base Ethernet controller or the front/rear Ethernet controller.
- Local hardware sensors for the CPM and RTM.
- Local output actuators
- Renesas H8S/2166 microcontroller and a supporting FPGA. The H8 manages commands and data throughout the hardware management system.
- IPMBs
- Serial EEPROM
- AMC and RTM control and management.

For more information, refer to *Chapter 5, Hardware Management,* on page 43.

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Supported DIMM combinations

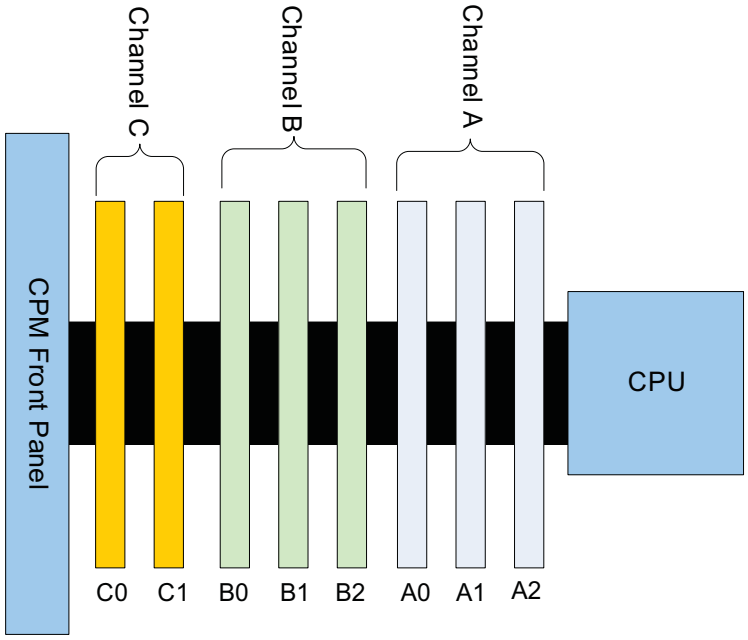
There are eight DIMM sockets (dual inline memory modules) on the CPM for installing VLP DDR3 (double data rate 3) registered ECC DIMMs. As shown in Figure 2, the sockets are grouped into three channels. When installing DIMMs, begin by populating the channels that are farthest from the CPU. Balance the DIMMs across the channels; that is, populate slot 0 for each channel first, followed by slot 1, and then slot 2. The preferred memory configurations are listed in Table 1 on page 16.

The CPU's integrated memory controller supports up to three channels of DDR3 DIMMs, using 64 data bits and 8 ECC bits per channel. Each channel supports up to three DIMMs (single, dual and quad-rank DIMMs) and supports DRAM speeds of 800MHz and 1066MHz with the following limitations:

- Three DIMMs per channel are only supported for single and dual-rank DIMMs running at 800 MHz.
- At 1066 MHz, only two DIMMs per channel are allowed for single and dual-rank.
- For quad-rank, only one DIMM per channel is allowed at any speed.

Note: Optimum memory performance is only achieved when DIMMs of identical rank and size are installed equally in all three channels.

Figure 2. DIMM slots and channels



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Table 1. Preferred memory population options

Number of DIMMs	DIMM Type	Channels Populated
3	Single-rank	C0, B0, A0
3	Dual-rank	C0, B0, A0
6	Single-rank	C0, C1, B0, B1, A0, A1
6	Dual-rank	C0, C1, B0, B1, A0, A1
8	Dual-rank	C0, C1, B0, B1, B2, A0, A1, A2[a]

[a] This configuration yields maximum memory.

Replacing DIMMs

Replacing DIMMs consists of removing the CPM from the shelf, removing the DIMM cover, removing the DIMMs to be replaced, installing the new DIMMs, replacing the DIMM cover, and re-installing the CPM in the shelf. The following sections detail these procedures.

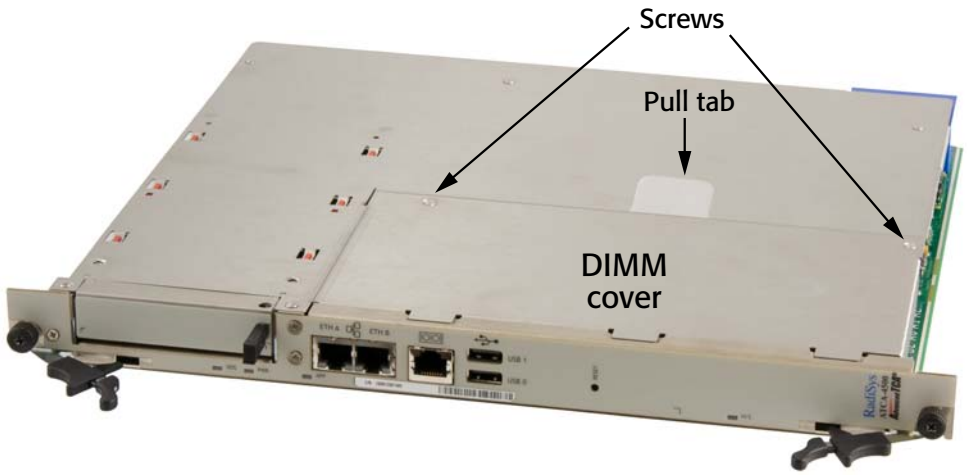
WARNING! Observe appropriate ESD precautions when performing the procedures in this chapter (see *Electrostatic discharge* on page 8).

Removing the DIMM cover

The following instructions assume that the CPM has been removed from the shelf.

1. Place the CPM on a flat, static-free surface.
2. Remove the two screws holding the DIMM cover in place (see Figure 3).
3. Use the "pull tab" to pull (in a horizontal motion) away from the front panel and toward the backplane connectors.
4. Lift off the cover.

Figure 3. DIMM cover



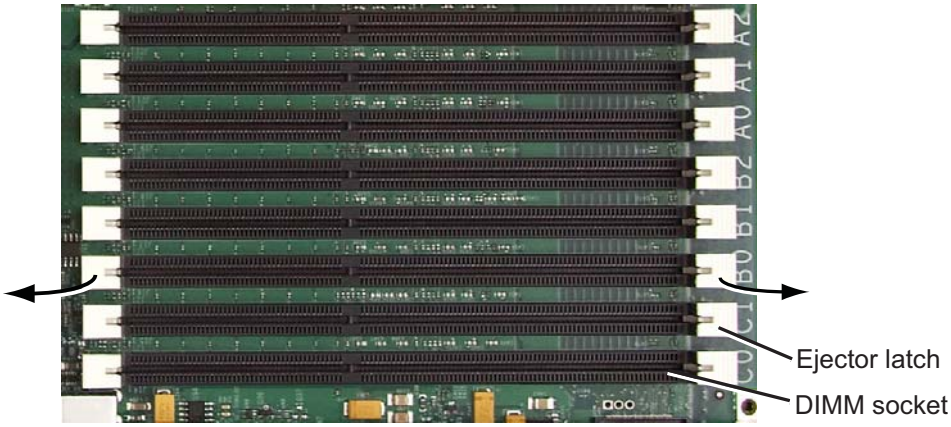
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Removing DIMMs

These instructions assume the CPM has been removed from the shelf and the DIMM cover has been removed.

1. Determine which DIMMs to remove (see previous discussion under *Supported DIMM combinations*).
2. Press outward on the ejector latches to pop out a DIMM, as shown in Figure 4.

Figure 4. DIMM sockets



3. Hold the DIMM by the edges and remove it.
4. Remove the other DIMMs in the same manner. To replace the DIMM with a new card, follow the steps under *Installing DIMMs*.
5. Screw the DIMM cover plate back into place.
6. Power up the CPM and check the BIOS screens to make sure all memory is detected.

Installing DIMMs

These instructions assume that the CPM has been removed from the shelf and the DIMM cover has been removed.

1. Open the DIMM ejector latches by pushing them outward, as shown in Figure 4.
2. The DIMMs are keyed so they can be inserted in only one way. Hold the DIMM by the edges, align the slot (keyway) of the DIMM with the tab molded in the base of the socket, and push the card down firmly into the socket. The ejector latches close and the DIMM clicks into place when it is firmly seated.
3. Insert the other DIMMs in the same manner, remembering to fill the corresponding DIMM slot for correct channel operation.
4. Screw the DIMM cover plate back into place.
5. Power up the CPM and check the BIOS screens to make sure all memory is working.

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Testing installed memory

After the DIMMs are installed, a memory test can be run from the EFI shell by executing the `memtest` command. The test scans all memory regions and reports any errors.

The EFI shell is accessed from the BIOS setup utility by making it the first boot device, or by choosing EFI shell after selecting the *Override boot source for next boot* setting in the Save & Exit menu.

The memory test is started by entering `memtest` without any command arguments. The memory test loops continuously through available memory regions until the ESC key is pressed.

Help is available for `memtest` by entering `memtest /?`.

Note: Disable ECC error correction in the BIOS setup before running the memory test. This ensures maximum test accuracy and prevents the masking of hardware errors. If ECC is enabled, check the system event log for any ECC errors that may occur during the memory test.

The following is an example of `memtest` output:

```
Shell> memtest
LOOP:    Starting pass 1

START:   Testing Memory Region 0x8000 -> 0x5FFFF
PASSED:  0x8000 -> 0x5FFFF Addressing Test (Fast)
PASSED:  0x8000 -> 0x5FFFF Data Test (Patterns)
PASSED:  0x8000 -> 0x5FFFF Addressing Test (Complex)
PASSED:  0x8000 -> 0x5FFFF Data Test (Walking Bits)
END:     Total Error Count (All Tests) = 0.

START:   Testing Memory Region 0x100000 -> 0xFFFFFF
PASSED:  0x100000 -> 0xFFFFFF Addressing Test (Fast)
PASSED:  0x100000 -> 0xFFFFFF Data Test (Patterns)
```

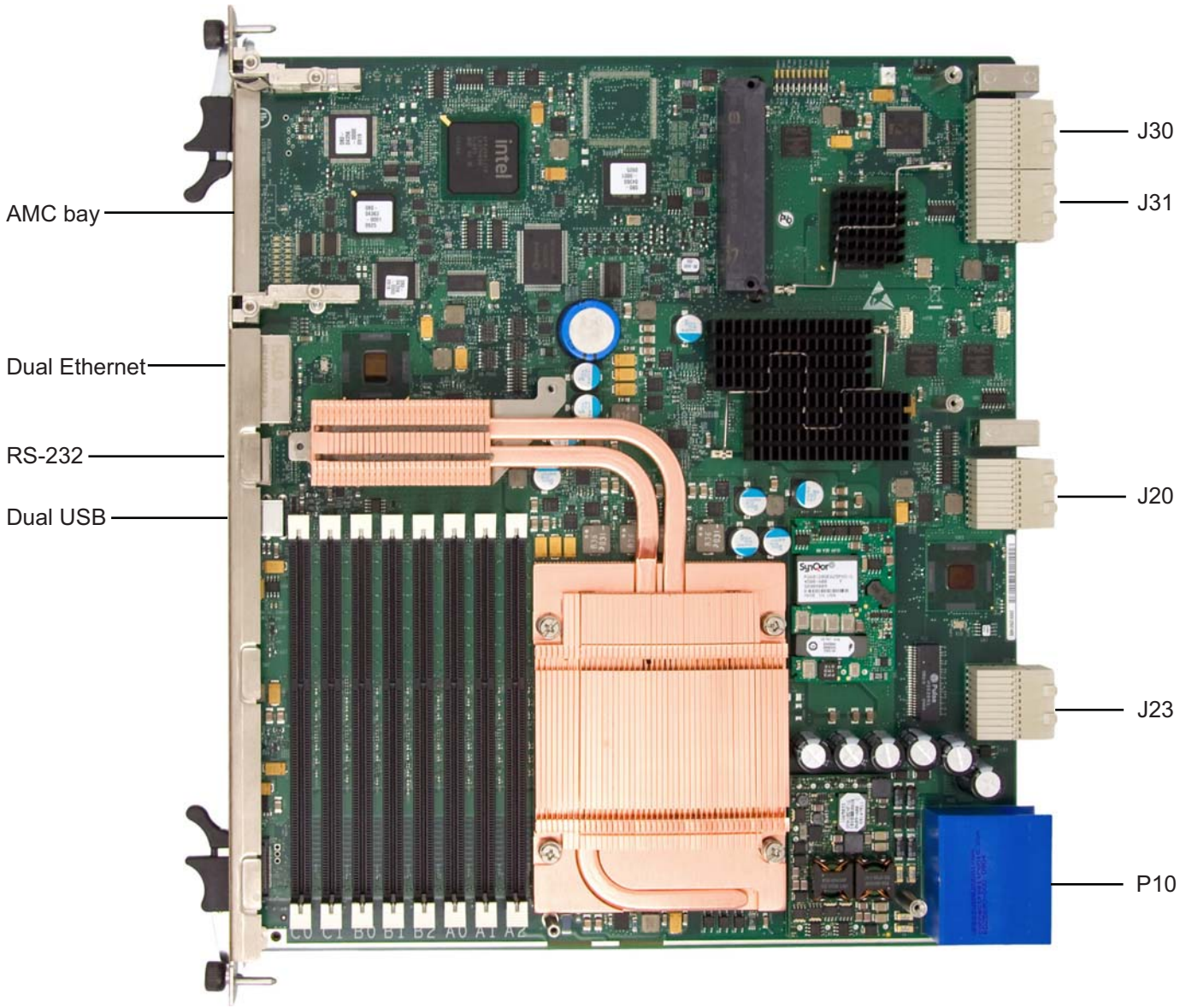
Note: If the system stops responding while `memtest` is executing it may be due to a memory failure that affects the areas of memory used for the executable code running the test.

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This chapter describes the ATCA-4500 CPM external indicators, switches, and ports.

Front panel LEDs, buttons, and ports

Figure 5. ATCA-4500 CPM interfaces



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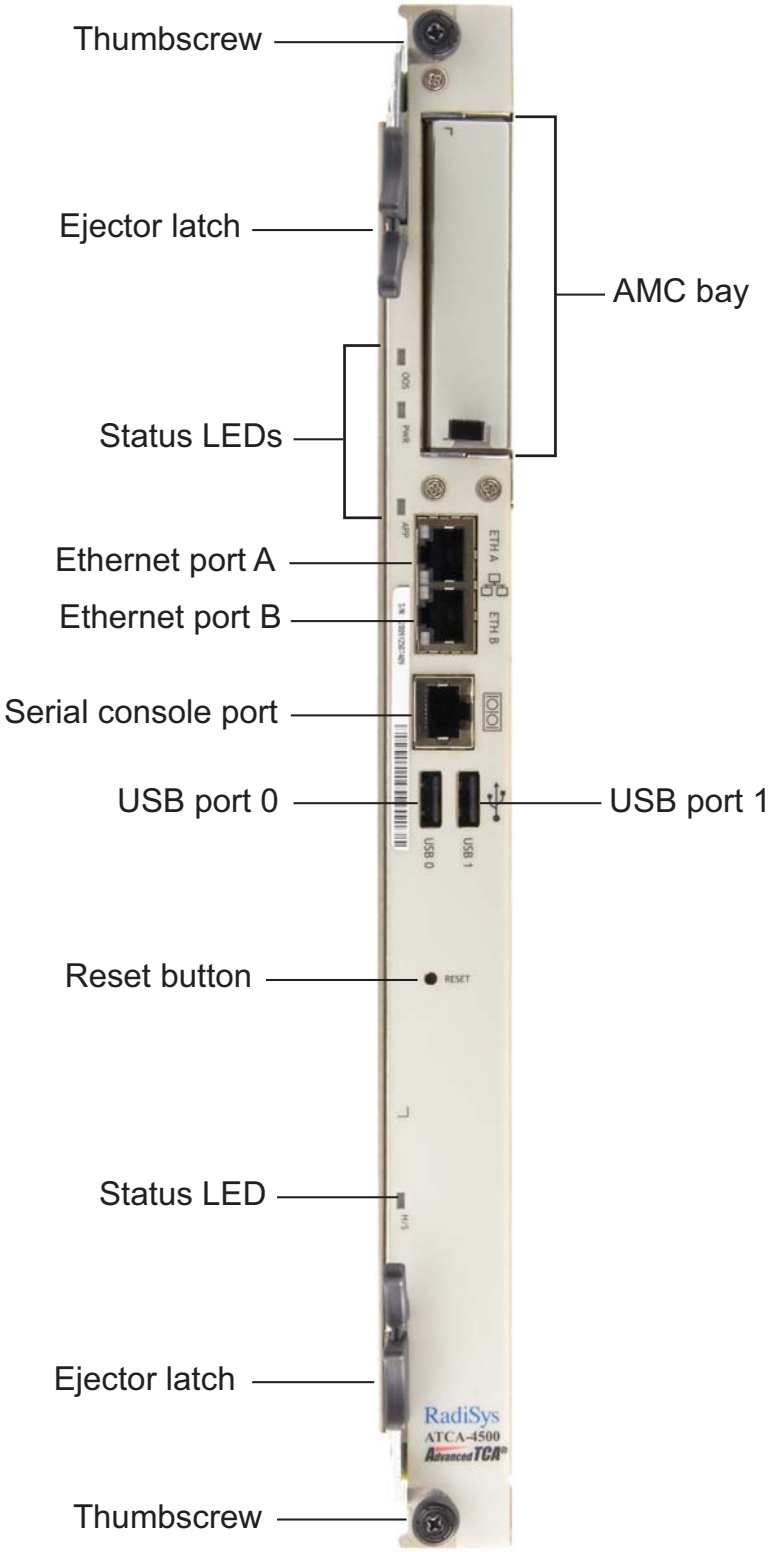
The CPM has a metal front panel that complies with PICMG 3.0 Revision 2.0 and serves as an EMI/RFI barrier. As shown in Figure 6 on page 21, the front panel includes:

- Status LEDs
- One AMC bay
- Dual USB connector
- Dual 1000Base-T Ethernet connector (two RJ-45)
- An RS-232 serial port (RJ-45)
- A recessed reset switch
- Top and bottom ejector handles, with a hot swap switch in the bottom handle
- Top and bottom thumbscrews that secure the CPM to the shelf

Important: RadiSys recommends the use of shielded cables for both serial and Ethernet port connections to minimize the possibility of issues related to external electromagnetic interference (EMI).

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Figure 6. ATCA-4500 CPM front panel features



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Front panel LEDs

Table 2 describes the front panel status and activity LEDs.

Table 2. Front panel LEDs

Label	LED ID	Definition	Color	LED states
OOS	LED 1	Out of service	Amber or red[a] 	Controlled by the IPMC, with application-defined functionality[b]. This LED is off during normal operation. If the LED is red or amber, the CPM is out of service.
PWR	LED 2	Power	Green 	Indicates whether CPM power supplies are within tolerance. The possible states are: ▪ Green: All power supplies initially good, and power has not been removed. ▪ Off: Module not powered on.
APP	LED 3	Application defined	Amber[c] 	Controlled by the IPMC, with application-defined functionality[c].
H/S	H/S	Hot swap status	Blue 	Controlled by the IPMC with these possible states: ▪ Long blink: Activating the module after insertion. ▪ Short blink: Preparing for hot swap. ▪ Solid: Ready for hot swap. ▪ Off: No hot swap activity in progress.

[a] The user application can select the LED color using the Set FRU LED State IPMI command.

[b] The user application can control LED illumination using the Set FRU LED State IPMI command.

[c] The user application can control the LED color and illumination using the Set FRU LED State IPMI command or through the GPIO registers.

The IPMC uses GPIO pins to control the hot swap and power LEDs. The IPMC supplies default states for the LEDs and responds to sensor readings, GPIO inputs, and IPMI commands from other entities to change LED states.

Front panel connectors

USB 2.0 connectors

The USB interface on the front panel is a dual-port stacked connector. Using a standard USB 2.0 cable, these ports connect the CPM to standard USB peripheral devices such as CD-ROM drives.

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Serial RS-232 connector

An external computer can display and interact with the CPM software by connecting an RJ-45 cable to the computer and the front panel RS-232 serial port. The pinout for the RS-232 connector is shown in Table 38 on page 113.

In order to communicate with the CPM, configure the terminal emulator on the external computer to match the default settings for the CPM serial port, as listed below:

- 115200 bps
- no parity
- 8 data bits
- 1 stop bit
- no flow control

For best display results, the terminal should be set to 80 columns by 25 lines.

Dual Ethernet connector

The dual Ethernet connector provides two front panel Ethernet ports that can be used to connect directly to a network. The front panel Ethernet ports are disabled when the RTM is being used for Ethernet communication. For more information, refer to *Configuring the front or rear Ethernet ports* on page 62.

Important: To comply with GR-1089-CORE, if cables are connected to both front panel Ethernet connectors then at least one of the cables must be shielded.

AMC bay

The CPM includes one Advanced Mezzanine Card (AMC) bay to hold an optional AMC module which slides into rails that guide it into the right-angle AMC B+ edge connector. The bay supports mid-sized AMCs, such as a Promentum AMC-3202 HDD AMC. For more information about the AMC bay, see *AMC bay* on page 39 and *AMC connector pinout* on page 119.

Reset button

The front panel includes a reset switch that performs a cold reset of the CPM. A cold reset returns all registers and devices (except the IPMC) to their default state. Note that pressing the reset button does not clear sticky bits in the CPU and I/O Hub registers. Clearing sticky bits requires a powergood reset.

The reset switch is a recessed button; to push it, use a pen, stylus, or other small pointed object.

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Backplane interfaces

Backplane connector J23 is the ATCA data transport connector, which provides Zone 2 connections for two 10/100/1000BASE-T Ethernet Base channels and two 10GBASE-BX4 Ethernet Fabric channels. See *10-gigabit Ethernet Fabric interface* on page 37 for details about all supported Ethernet Fabric channel modes. For more information about the backplane connectors, refer to *Backplane interfaces* on page 114.

Backplane connector J20 provides Zone 2 connections to the synchronization clocks and the AMC update channels. For information about using update channels to connect the AMC bays on two ATCA-4500s, refer to *Update channel connections to the AMC bay* on page 41. For detailed information about the connector itself, refer to *Zone 2 J20 connector pinout* on page 117.

The CPM supports E-Key control by describing its backplane interfaces to the Shelf Manager, as described under *E-Key control of interfaces* on page 51.

The power control interface to the IPMC is through the backplane connector P10, the Zone 1 power distribution connector. Refer to *Zone 1 P10 connector pinout* on page 115 for details.

Alignment keys

The CPM implements the K1 and K2 alignment blocks at the top of Zone 2 and Zone 3, as required by the PICMG 3.0 specification. The Zone 2 alignment block (K1) is assigned a keying value of 11. The Zone 3 alignment block (K2) is assigned a keying value of 55.

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Rear transition module (RTM) interface

The CPM includes the standard Zone 3 backplane interface to provide connectivity to an optional RTM, such as the ATCA-5400. This interface consists of two connectors: J30 for common and maintenance signals, and J31 for SerDes (serialization/deserialization). For details, refer to *Zone 3 J30 connector pinout* and *Zone 3 J31 connector pinout* on page 118.

The electrical connections between the CPM and the associated RTM include:

- Switched +12V power, under the control of the IPMC
- Switched +3.3V IPMC power, under the control of the IPMC
- I2C management bus from the IPMC
- Hot swap control signals
- One JTAG boundary scan interface
- Switchover signals
- RTM link signals
- Serial port
- I2C management bus, connected to I/O Controller Hub SMBus
- Two Serial-Attached-SCSI (SAS) channels
- Two 1-Gb Ethernet interfaces from the CPM front/rear Ethernet controller, supporting SerDes or SGMII
- Two I2C interfaces from the front/rear Ethernet controller for SGMII mode support
- Four 1-Gb interfaces from the AMC bay, supporting SerDes or SGMII
- One I2C port from the AMC bay to provide SFP and LED control functions
- One SATA port from the I/O Controller Hub (ICH10R)
- RTM_RESET# signal used to cold reset ICs on the RTM
- Two x4 PCI Express generation 2 ports from the Intel 5520 I/O Hub (36D)

The RTM Ethernet ports are disabled when the front-panel Ethernet ports are in use. Refer to *Configuring the front or rear Ethernet ports* on page 62 for more information.

A current limit switch controls the amount of current that the RTM can draw. Refer to *Power consumption* on page 78 for more information.

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Other physical interfaces

For information about the DDR3 DIMM interface, refer to *Supported DIMM combinations* on page 15 and to *DDR3 SDRAM* on page 29.

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This chapter discusses the CPM's major components and subsystems.

Processor and memory controller

The CPM supports various versions of the Intel Xeon 5500 series processors. The processor has an integrated memory controller and two point-to-point Quickpath Interconnect (QPI) interfaces for I/O Hub (IOH) and CPU connectivity. The processor cores share an 8MB cache and support SSE2, SSE3 and SSE4 streaming SIMD (Single Instruction, Multiple Data) extensions. The extensions enhance the performance of optimized applications like video, image processing, and media compression.

Note: The CPM does not use the CPU's turbo boost feature.

The CPU includes the Execute Disable Bit, 64-bit technology, Intel SpeedStep®, virtualization technology and simultaneous multi-threading. The processor also features a loop stream detector that greatly increases loop execution speed. Table 3 and Table 4 provide the various processor specifications.

Table 3. CPU power specifications

Processor	Core Frequency	Core voltage	Temp max TJ	Thermal design power (TDP)
L5518 LV 60W	2.13 GHz	0.75 V - 1.35 V	70°C	60 W

Table 4. CPU bus specifications

Processor	Cores	Threads	Core frequency	QPI speed	DDR3 speed	Cache size
L5518 LV 60W	4	8	2.13 GHz	5.86 GT/s	1066 MHz	8 MB

Adaptive thermal monitor for processor protection

The CPU case temperature must remain within the specified operating range in order to maintain reliability over the life of the processor. The CPU includes an adaptive thermal monitor (ATM) to help control the processor temperature. The ATM selects between voltage and frequency control (Intel SpeedStep®) and internal clock modulation to reduce processor power and to activate the thermal control circuitry.

The CPU includes a single digital thermal sensor (DTS) that continuously measures the temperature at each processing core and provides processor die temperature information that represents the worst case temperature for all cores. The DTS data represents the difference between the current die temperature and the temperature at which the ATM activates the thermal control circuitry. The IPMC accesses DTS information through the platform environmental control interface (PECI).

For more information on the temperature sensors, refer to *Managed sensors* on page 87.

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Integrated memory controller

The integrated CPU memory controller supports up to three independent channels of DDR3 DIMMs, using 64 data bits and 8 ECC bits per channel. When running at 800 MHz, the CPM supports up to 64 GB of DDR3 memory. At 1066 MHz, it supports up to 48 GB. Refer to *DDR3 SDRAM* on page 29 for more information about the DIMMs and to *Supported DIMM combinations* on page 15 for more information about CPM DIMM configurations.

Memory modes

The memory controller operates in independent mode. Independent mode allows the memory controller to interleave the memory map across all three channels, resulting in the highest level of performance. In independent mode, DIMMs can be placed in any of the three channels and there are no matching requirements for rank or DIMM speed. A burst-length of 8 is used.

Note:

- Maximum performance is achieved only when the DIMMs are identically populated across the three channels.
- The CPM only supports registered ECC DDR3 DIMMs; it does not support unbuffered DIMMs (with or without ECC).

DRAM temperature control

The CPU can influence the DRAM temperature by reducing the memory channel frequency (throttling). The CPM triggers a frequency decrease by asserting a DDR_THERM# input to the CPU whenever the DIMM temperature gets too high (implemented by wiring together the EVENT# pins from each DIMM).

2x refresh mode

The CPU doubles the refresh rate to the memory channels to better preserve the data when the DRAM is operating at elevated temperatures. The DRAM components have two temperature limits: T32 and T64. T32 is the temperature limit for a 1x refresh rate. T64 is the upper DRAM temperature limit when operating in 2x refresh mode. When T64 is exceeded, an SMI (system manager interrupt) is generated because the DRAM is operating out of specification. For a typical DDR3 DRAM component, T32 is 85°C and T64 is 95°C.

The double refresh rate can be disabled by changing the setting to 1x refresh in the BIOS.

Quick path interconnect

The CPU includes two point-to-point Intel QuickPath interconnect interfaces (QPI) for communication between the CPU and the I/O hub. However, the CPM uses only one QPI interface from the CPU (QPI port 1). The QPI interface is 20 lanes wide under full operation. With its integrated memory controller, the CPU incorporates the QPI caching agents for maintaining cache coherence as well as the home agents for managing access to memory regions. Data of any width is converted to packets and then sent serially over the QPI link (see Table 4).

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Memory and storage devices

The CPM provides the following memory devices:

- Sockets for installing DDR3 DIMMs. See *DDR3 SDRAM* for more information.
- Two 16Mb (redundant) SPI flash memory chips dedicated to BIOS and boot operations (see *Redundant boot flash*).
- Pluggable eUSB modules for user flash memory (see *Redundant user flash*).

These devices provide additional storage options for the CPM:

- a SFF flash drive on the AMC
- a local SFF SAS hard disk drive on the RTM, which includes a storage controller for a hardware-based redundant array of inexpensive hard disk drives (RAID)
- iSCSI storage over both the Base and Fabric interfaces

DDR3 SDRAM

The CPM has 8 VLP DIMM sockets for registered DDR3 SDRAM modules. These DIMM sockets are grouped into three independent channels. Two of the channels (A and B) can hold up to three DIMMs, while the third channel (C) only holds up to two DIMMs:

- Three DIMMs per channel (A and B) is only supported for single- and dual-rank DIMMs running at 800 MHz.
- At 1066 MHz, only two DIMMs per channel are allowed for single and dual-rank.
- For quad-ranked DIMMs, only two DIMMs per channel are allowed at any speed.

See Table 1 on page 16 for a list of preferred memory configurations.

For more information on supported SDRAM configurations, refer to *Supported DIMM combinations* on page 15. For information regarding memory operating modes, refer to the discussion under *Integrated memory controller* on page 28.

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Redundant boot flash

Two 16Mb Serial Peripheral Interface (SPI) flash memory devices are used on the CPM to provide a redundant boot function.

The SPI connection to the redundant boot flash runs around 30MHz and consists of 4-pins: clock, data out, data in, and chip select. The SPI flash operates in descriptor mode, which looks for a descriptor on the SPI flash device.

SPI flash selection

The primary SPI flash is selected when the CPM is powered up. If the CFD watchdog timer expires, the IPMC powers down the CPM, selects the secondary SPI flash, then powers up the CPM. For more information on the CFD watchdog, refer to *Corrupt flash detection watchdog* on page 50.

Tip: The flash device selection for the next boot can be overridden by setting an option on the BIOS boot menu.

SPI flash programming

The SPI flash is programmed by booting into the EFI shell and using an EFI reflash utility and a USB flash disk. Standard Linux and DOS-based reflash utilities can also be used for programming the flash.

Boot block protection

The CPM uses a hardware jumper to control the write-protect signal to the SPI flash in order to protect the boot block. When the jumper is installed, the boot block is write protected. When the jumper is not installed, the boot block is write-enabled. Refer to *Jumper settings* on page 124 for more information.

Redundant user flash

The CPM optionally includes two banks of user flash memory with up to 16 GB storage capacity for each bank. Each redundant flash bank can be used to store an operating system and application image, allowing it to function as a boot device.

Each user flash consists of an embedded universal serial bus (eUSB) flash module. The eUSB flash memory has a small form factor, low power consumption, and fast access time. The I/O controller hub uses standard USB 2.0 connections to communicate with the user flash.

Note: The CPM includes a write-protection jumper for each memory bank. Refer to *Jumper settings* on page 124 for more information.

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Access to storage devices from Linux

The CPM storage devices are accessible from Linux as formattable media, depending on your operating system configuration.

Device type naming

The Linux device type is determined by the physical device type installed. The Linux file system names may be */dev/sd<drive><partition>* for SCSI devices or */dev/hd<drive><partition>* for hard disks. USB and SAS devices are considered SCSI devices (*/dev/sd<drive><partition>*).

Order of device discovery and naming

The order in which Linux discovers the storage devices is the order that it assigns them alphabetical names, starting with the suffix "a". For example, the first SCSI device discovered is named */dev/sda*, and the second is named */dev/sdb*.

Identifying the assigned name for a specific device

To identify the drive name for a specific device, use the Linux command:

```
cat /proc/partitions
```

Look in the results for a drive size that closely matches the device.

To identify the SCSI devices by device model, use the command:

```
cat /proc/scsi/scsi
```

The devices are listed in order, starting with */dev/sda*.

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I/O hub to PCI Express devices

The CPM includes an Intel 5520 chipset I/O hub (IOH) that provides the bridge between the PCI Express (PCIe) devices in the system and the CPU QPI interface.

The IOH provides 36 PCIe ports capable of Gen1 (2.5 GT/s) and Gen2 (5 GT/s) speeds. Table 5 shows the PCI Express port mapping.

Table 5. PCI Express port mapping

Port	Port Width	PCI Express Peripheral	PCIe Type
1	x2	Not used	
2	x2	Not used	
3	x4	Base Ethernet controller	Gen 1
4	x4	RTM 0	Gen 2 capable
5	x8	10 Gigabit Fabric Ethernet controller	Gen 1
6			
7	x4	RTM 1	Gen 1 and Gen 2 capable
8	x4	Not used	Gen 1
9	x4	AMC bay	Gen 2 capable
10	x4	Front/rear Ethernet controller	Gen 1

I/O controller hub (south bridge)

The CPM uses the Intel ICH10R I/O controller hub (ICH) to communicate with peripheral input and output devices. Its features include:

- Up to six SATA ports with data transfer rates up to 3.0 Gbps and an integrated advanced host controller interface (AHCI) controller.
- Two USB host controllers, providing up to twelve USB 2.0 ports
- An LPC bridge
- An SMBus 2.0 controller
- An enhanced DMA controller (two cascaded 8237 DMA controllers)
- An interrupt controller that supports:
  - Up to eight PCI interrupt pins
  - PCI2.3 message Ssgnaled interrupts
  - Two cascaded 82C59 with 15 interrupts
  - An integrated I/O APIC capability with 24 interrupts
  - Processor system bus interrupt delivery
- Real-time clock (RTC) circuitry

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USB controller

The ICH contains four controllers that share the same set of pins: Two universal host controller interface (UHCI) controllers and two enhanced controller host interface (EHCI) controllers. Each pair of controllers provides up to twelve USB 1.1 or USB 2.0 ports. Each EHCI port allows data transfers up to 480 Mb/s and reports over-current status back to the ICH.

The CPM provides the five ports listed in Table 6 when configured for EHCI (USB 2.0):

Table 6. USB 2.0 ports

Port Number	Port Location	Notes
0	Front panel, upper USB port	Refer to *Front panel connectors* on page 22 for additional information.
1	Front panel, lower USB port	
2	No external port connections	USB NAND flash A and B. User flash is discussed under *Redundant user flash*.
3		
4	RTM USB port	Refer to *Rear transition module (RTM) interface* on page 25.

SATA controller

The ICH includes two SATA host controllers that support data transfer rates of up to 3.0 Gbps. Communication over the SATA bus can operate in one of two different modes, depending on operating system requirements:

- In native mode, both controllers are used to implement up to six SATA ports. Ports 0 - 3 are handled by the first controller and ports 4 - 5 are handled by the second controller.
- In legacy mode, only ports 0 - 3 are available from the first controller.

SATA port 1 is connected to the RTM. If an AMC that includes a SATA-compatible hard disk drive is installed, the IPMC configures the SAS/SATA multiplexer to connect SATA port 0 or SAS from the RTM to AMC port 2. This provides both native and legacy support from the first controller. For more information about SAS/SATA switching control, refer to *SAS and SATA* on page 35.

SPI bus

The ICH uses a serial peripheral interface (SPI) bus operating at about 30MHz for communication with the two boot flash devices. This connection is discussed in more detail under *Redundant boot flash*.

LPC bridge

The ICH enables communication between the CPU and low-bandwidth peripherals by providing a low pin count (LPC) bridge connection to the following devices:

- Super I/O (see *Super I/O chip*)
- CPU complex FPGA (see *CPU complex FPGA*)
- IPMC (see *Intelligent Platform Management Controller*)

The LPC bridge implements all of the cycles described in the *Intel Low Pin Count Interface Specification, Revision 1.1*.

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Real-time clock

The ICH includes an integrated real-time clock (RTC) that keeps track of the time of day and stores system data. The RTC circuitry includes 256 bytes of capacitor-backed CMOS RAM. The RTC is derived from a 32.768 KHz crystal with the following specifications:

- Frequency tolerance @ 25°C: ± 20 ppm
- Frequency stability: maximum of -0.04 ppm/(Δ °C)^2
- Aging ΔF/f (first year @ 25 °C): ± 3 ppm
- ± 20 ppm from 0-55 °C and aging 1 ppm/year

When power is removed from the board, the time and system data are maintained by an electrolytic capacitor for up to two hours. When the chassis is turned on, the RTC gets power from the IPMI 3.3 V power supply, which allows the capacitor to begin charging before the CPM payload power is turned on.

SMBus controller and multiplexers

The ICH includes a SMBus 2.0-compliant host controller, which allows the CPU to initiate communication with SMBus slave peripherals and I^{2}C-compatible devices. Two SMBus multiplexers give the IPMC access to the ICH slave registers and to the DIMM temperature sensors. Refer to *I^{2}C and SMBus map* on page 134 for information on the devices connected to the SMBus.

The slave interface allows an external master to read from or write to the ICH. Write cycles can be used to cause certain events or to pass messages. Read cycles can be used to determine the state of various status bits. The ICH's internal host controller cannot access the internal slave Interface.

The ICH SMBus consists of a transmit data path and host controller. The transmit data path provides the data flow logic needed to implement the seven different SMBus command protocols and is controlled by the host controller. The RTC clocks the ICH SMBus controller logic.

The host controller's programming model has two segments: a PCI configuration and a system I/O mapping. All static configurations, such as the I/O base address, are configured via the PCI configuration space. Real-time programming of the host interface is done in system I/O space.

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Super I/O chip

A Winbond W83627 super I/O chip provides dual serial ports and voltage monitors to the CPU. On the CPM, the super I/O is connected to the ICH through the LPC bus and is used primarily for serial connectivity and voltage monitoring.

Both of the CPM COM ports are connected to the COMux CPLD. The serial connection to the front panel (COM 1) supports dual hardware handshaking and implements the following signals: TXD, RXD, DTR, RTS, DSR and CTS. The serial connection to the RTM (COM2) supports TXD and RXD only. Software handshaking is possible.

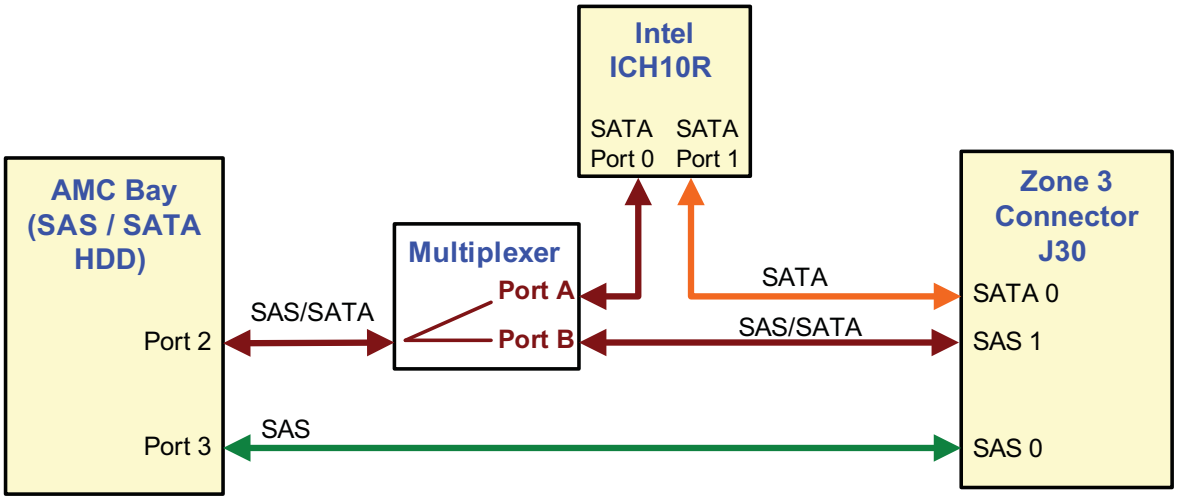
SAS and SATA

The CPM supports either SAS or SATA connections to AMC bay port 2. This provides data storage options if the AMC has a SAS or SATA hard disk drive. The connection to AMC bay port 2 is configured in the BIOS setup menu. The CPM also supports either SAS or SATA connections to the RTM through the Zone 3 interface, providing additional data storage if the RTM has a SAS or SATA hard disk drive.

The CPM supports a SAS connection between AMC bay port 3 and the RTM through the Zone 3 interface, as well as a SATA connection from the ICH10R I/O controller hub to the RTM.

The SAS and SATA connections are diagrammed in Figure 7.

Figure 7. SAS/SATA multiplexer connections



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Ethernet controllers and interfaces

Gigabit Ethernet interfaces

The CPM uses two dual gigabit Ethernet controllers (Intel 82576EB devices) to provide four GbE ports. One controller is used for the two GbE Base interface channels, and the other is used for the front panel and RTM Ethernet ports.

Each controller has two independent network interfaces that support SerDes (serializer-deserializer), SGMII, or MDI (copper) protocols. Each controller is connected to a x4 PCIe port that operates at 2.5 GT/s and is capable of negotiating x2 and x1 link widths.

The Ethernet controllers provide virtualization support including PCI-SIG single-root I/O virtualization, VMDq2 support for up to 8 virtual machines and 16 TX and RX queues. A system management bus (SMBus) interface supports pass-through traffic for Serial-over-LAN from the IPMC.

Each Ethernet controller has a private128-KB SPI EEPROM for storing initialization data and media access control (MAC) addresses. During power up, the initial configuration information for the controllers (including management setup and SMBus addresses) is read from these EEPROMs. Refer to *Overview of firmware updates* on page 70 for information about updating the EEPROM software.

The controllers have two fully integrated gigabit Ethernet MAC and PHY (physical layer) ports. These devices use the PCI Express architecture (revision 1.0a).

Base Interface

The Base controller is configured for MDI (copper), providing 1000Base-T, 100-Base-TX, and 10Base-T support. The Base controller is connected to the BASE 1 and BASE 2 backplane ports, and the controller is connected with a x4 link to PCIe port 3 on the I/O hub. The EEPROM for the Base controller enables pass-through mode via the SMBus, which allows the IPMC to implement serial-over-LAN on either base port.

Front panel and RTM Ethernet interfaces

One of the GbE controllers is used to implement dual Ethernet ports to either the front panel or the RTM rear panel. The MDI (copper) ports are connected to the front panel interface for 1000Base-T, 100-Base-TX and 10Base-T support. The SerDes signals are routed through the Zone 3 connector to two SFP transceivers on the RTM.

Selection of front or rear ports is controlled through a BIOS menu (see *Configuring the front or rear Ethernet ports* on page 62).

The front/rear GbE controller is connected with a x4 link to PCIe port 10 on the I/O hub. The EEPROM for the front /rear controller enables pass-through mode over the SMBus to allow the IPMC to implement serial-over-LAN on either port. Refer to *Serial-over-LAN* on page 57 for more information.

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10-gigabit Ethernet Fabric interface

The CPM uses an Intel 82598EB controller to provide two10-GbE port connections to the Fabric interface channels. The 10-GbE controller is connected to a x8 PCIe port that provides a peak data bandwidth of 2.5 Gbps in each direction (PCIe 1.1 compliant). A private 128-KB EEPROM stores initialization data and MAC addresses.

The 10-GbE controller includes two independent XAUI ports that support the following standard Ethernet interfaces:

- 10GBASE-KX4
- 1000BASE-KX (IEEE 802.3ap)
- 10GBASE-CX4 (IEEE 802.3ak)

Each port also contains a SerDes interface to support 1000BASE-SX/LX (optical fiber) and 1000BASE-BX for gigabit backplane applications. Auto negotiation (as specified by IEEE 802.3ap Clause 73) is also supported.

Fabric interface

The CPM provides multiple connectivity options to Fabric channels 1 and 2. The multiplexer option for Fabric channels 1 and 2 connects either the 10-GbE controller for 10-Gb Fabric connections or the AMC bay to the backplace. The Fabric connections are determined by the interface E-Keying (see *E-Key control of interfaces* on page 51). The default configuration is to route Fabric channels 1 and 2 to the 10-GbE controller as 10GBase-BX4/1000Base-BX (see Figure 8).

Depending on the interface E-Keying, Fabric channel 1 is configured as one of these options:

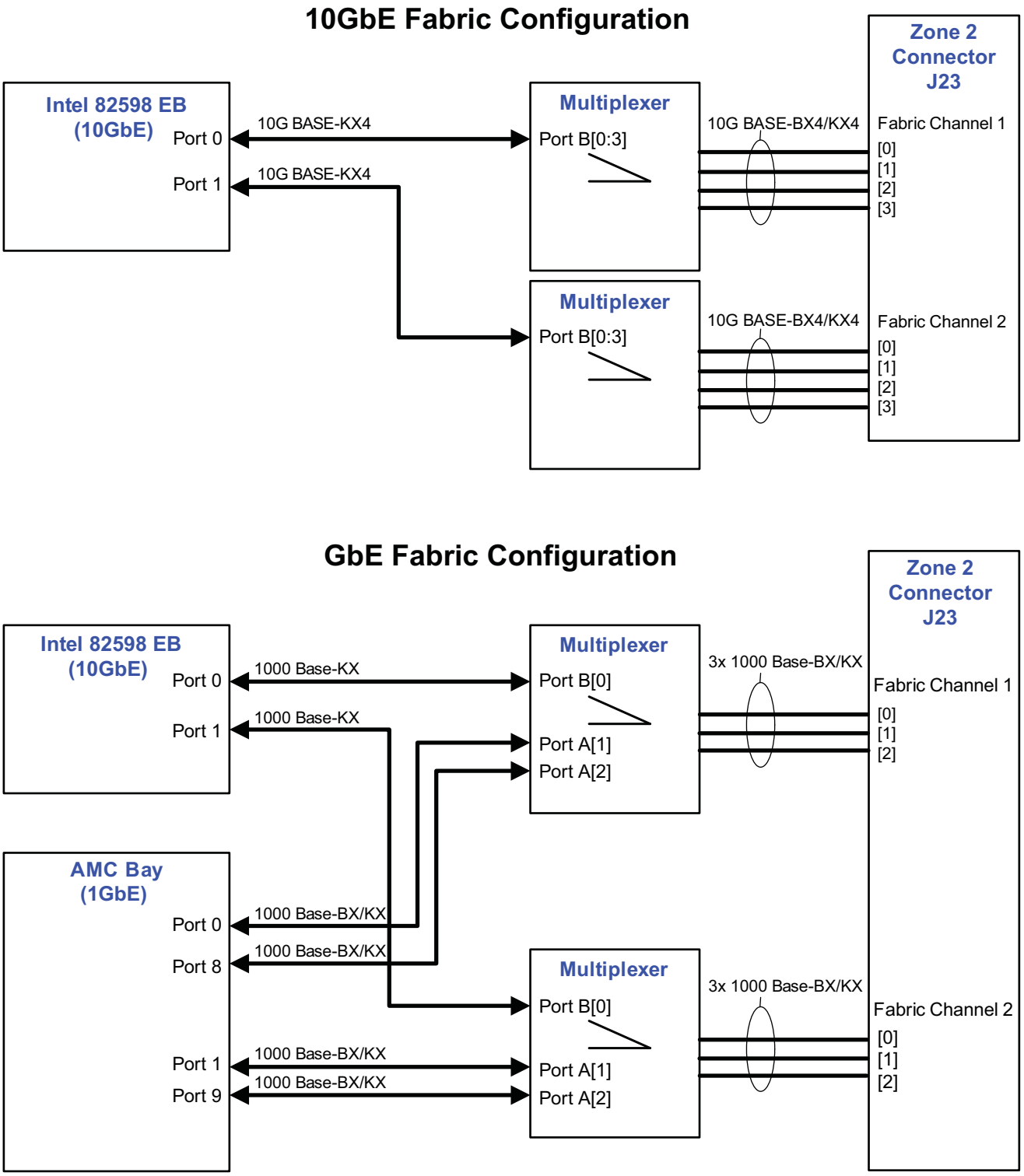
- A 10GBase-BX4 (or KX4) connected to Port 0 of the 10-GbE controller
- Three 1000Base-BX (or KX) links connected to Port 0 of the 10-GbE controller or to AMC Ports 0 and 8.

Similarly, Fabric Channel 2 is configured as one of these options:

- A10GBase-BX4 (or KX4) connected to Port 1 of the 10-GbE controller
- Three 1000Base-BX (or KX) connected to Port 1 of the 10-GbE controller and AMC Ports 1 and 9.

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Figure 8. Ethernet Fabric interface



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AMC bay

The CPM supports one Advanced Mezzanine Card (AMC) bay that is compliant with the AMC.0, AMC.1 (PCI Express), AMC.2 (Ethernet), and AMC.3 (Storage) PICMG specifications. The bay supports mid-size modules and the RadiSys HDD-AMC. The bay can provide up to the AMC.0 maximum of 80W, but the total power consumption allowed is 40W.

The AMC bay has basic and extended connector sections. The basic section consists of the clocks, dual GbE (SerDes) ports, SAS/SATA ports, and a x4 PCI Express port. The extended section includes two additional GbE ports, an update channel port, RTM control, and RTM extended I/O. Table 7 shows the port mapping for the AMC bay, and Table 8 describes AMC port interfaces. Also refer to *AMC connector pinout* in Appendix C for connection details.

Table 7. AMC port mapping

	Port	Function
Basic connector	TCLKA	Telecom Clocks (AMC.0). TCLKA and TCLKC are not supported.
	TCLKB	
	TCLKC	
	TCLKD	
	FCLKA	Fabric Clock (AMC.0/AMC.1)
	0	GbE (AMC.2 Type E2)
	1	
	2	SAS/SATA to RTM/ICH Mux (AMC.3)
	3	SAS to RTM (AMC.3)
	4	Type 4 x4 PCI Express (AMC.1)
	5	
	6	
	7	
Extended connector	8	GbE (AMC.2 Type 2)
	9	
	10	(no connect)
	11	
	12	Fast Path Update Channel
	13	Slow Path Update Channel
	14	(no connect)
	15	Rear Transition Module Control
	16	(TCLKD above)
	17	Rear Transition Module access (AMC.0)
	18	
	19	
	20	

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The CPM's IPMC provides intelligent platform management (IPM) connectivity between the backplane IPMB and the AMC's local IPMB (IPMB-L). Depending on the software involved, the AMC bay may be addressed in any of the following ways:

	AMC bay
PICMG 3.0 commands	FRU 1
BIOS setup screens	Slot 1
AMC.0 site number	Site 5
IPMB-L address	0x7A

The Shelf Manager refers to the AMC as bay 5, corresponding to the AMC.0 site number. Shelf Manager alarms pertaining to the AMC will use this number, and the HPI resource IDs will refer to site 5. Other shelf managers may refer to the AMCs by their AMC.0 site numbers or FRU numbers.

See the *Advanced Mezzanine Card Installation Guide* for installation instructions.

Table 8. AMC port interfaces

Identity	Function
Synchronization TCLKA	Not supported.
Synchronization TCLKB	The AMC can drive synchronization TCLKB to the CLK3 clock selection circuitry on the CPM.
Synchronization TCLKC	Not supported.
Synchronization TCLKD	The AMC can drive synchronization TCLKD to the CLK3 clock selection circuitry on the CPM.
Fabric FCLKA	Fabric FCLKA is driven to the AMC bay by the 100-MHz PCIe clock generator on the CPM.
Common option Fabric ports 0 and 1	Ports 0 and 1 of the AMC bay connect 1000Base-BX Ethernet to the Fabric multiplexer on the CPM.
Common option Fabric ports 2 and 3	Ports 2 connects to the SAS multiplexer. The Port 2 connection switches between SAS channel 0 from the RTM and SATA channel 0 from the ICH. The Port 3 connection passes directly to SAS channel 1 on the RTM. These interconnections are compliant with the PICMG AMC.3 Storage AMC specification.
Fat Pipes Fabric ports 4, 5, 6, and 7	Ports 4 through 7 of the AMC bay connect to IOH PCIe port 9 on CPM with a x4 link. These interconnections are compliant with the PICMG AMC.1 PCI Express AMC specification (Type 4).
Fat Pipes Fabric ports 8 and 9	Ports 8 and 9 of the AMC bay connect 1000Base-BX Ethernet to the Fabric multiplexer on the CPM.
Fat Pipes Fabric ports 10 and 11	Ports 10 and 11 are unused on CPM.
Extended options Fabric port 12	Port 12 of the AMC bay connects to the SAS multiplexer for driving and receiving signals to and from Update Channel 0. This allows direct interconnection between AMC modules on redundant CPM carrier blades. This connection can operate up to 3.2 Gbps. The E-Keying function is provided by the IPMC, which controls the enabling over an I^2C bus.
Extended options Fabric port 13	Port 13 of the AMC bay is dedicated to a non-standard "slow path" update channel. The connection is used for single-ended general-purpose I/O (GPIO) signals. The E-Keying function is provided by the IPMC on the CPM, which controls the enable pins of the buffers using GPOs. The signals on Port 13 are non-LVDS, and therefore must power up disabled until E-keying enables them.
Extended options Fabric port 14	Port 14 is unused on CPM.

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Table 8. AMC port interfaces (Continued)

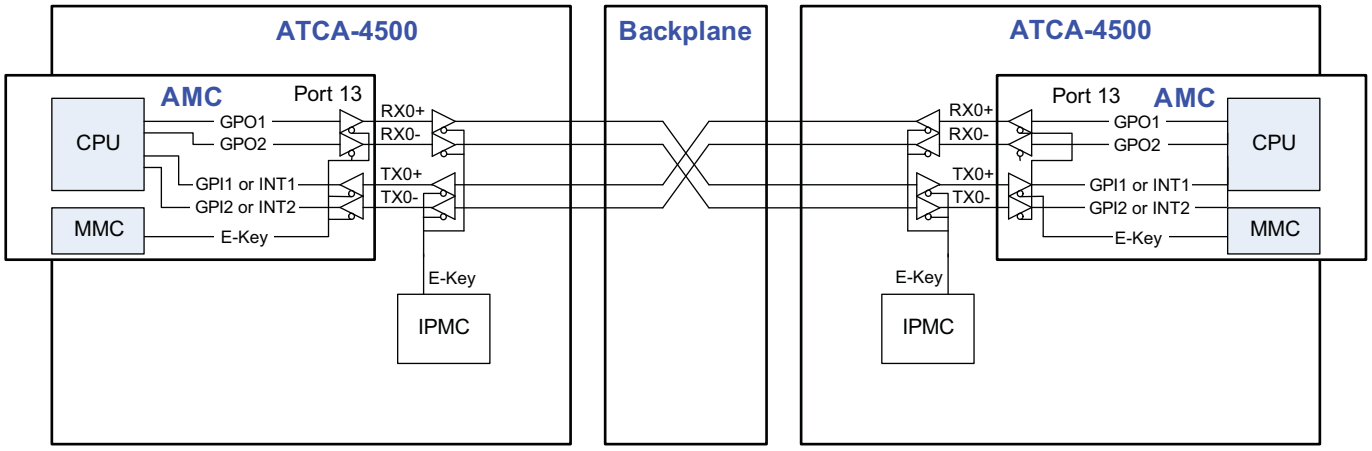
Identity	Function
Extended options Fabric port 15	Port 15 of the AMC bay connects through the Zone 3 J30 connector to the RTM. These interconnections are to provide an I²C bus from the AMC module to the RTM for SFP and LED control. They also provide a serial port for RTM access to the AMC for debug. Per the AMC.0 specification, AMC modules are required to power up with their ports disabled if the signal levels used are non-LVDS. This is the case for the I²C interface and its pull-ups on the AMC module. The RTM must also have an I²C bus isolator. The TTL-level serial port signals on the AMC must also power up disabled. The E-Keying function is provided by software on the CPM's IPMC and the AMC module's MMC (module management controller) working together to determine whether the ports are enabled. No hardware buffer is provided for the port on CPM.
Extended options Fabric ports 17, 18, 19, and 20	Ports 17, 18, 19 and 20 connect through the Zone 3 J31 connector to the RTM. These interconnections are to provide four 1.25 Gbps differential SerDes or SGMII channels between the AMC module and the RTM. Per the AMC.0 specification, AMC modules are required to power up with their ports disabled if the signal levels used are non-LVDS. The E-Keying function is provided by software on the CPM's IPMC and the AMC module's MMC working together to determine whether the ports are enabled. No hardware buffers are provided for the ports on CPM.

Update channel connections to the AMC bay

The update channel on the backplane has both fast (channel 0) and slow (channel 4) connections to the AMC bay. Both update channels are used to connect two ATCA-4500 CPMs (installed in chassis slots linked by the PICMG update channel). Refer to the entries for AMC ports 12 and 13 in Table 8 for a functional description of the update channels.

The slow path update channel (AMC port 13) provides a means to pass relatively slow data between redundant AMC modules on different CPMs, as illustrated in Figure 9.

Figure 9. AMC bay slow path update channel



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The connections to Port 13 of each AMC bay are used for single-ended general-purpose I/O (GPIO) signals. The signals on Port 13 power up disabled on both the AMC and the CPM, and are E-Keyed. The E-Keying function is provided by the IPMC on the CPM and the MMC on the AMC modules. Each controls the enable pins of their respective buffers with GPO pins.

If an AMC module chooses to use Port 13, it must drive GPO outputs on the AMC-side TX+ and TX- pins. The corresponding carrier-side RX+ and RX- signals are applied to the input of the redundant CPM and AMC. The buffers drive the carrier-side TX+ and TX- pins with signals received from the redundant CPM. The AMC module receives these signals on its RX+ and RX- pins, and can either connect them to GPI inputs or interrupt inputs.

Intelligent Platform Management Controller

The Intelligent Platform Management Controller (IPMC) monitors the health of the system and manages the CPM hardware by controlling power to the CPM payload, managing the sensors, using E-Keys to enable ports, performing CPM resets, and executing IPMI commands. The IPMC consists of a microcontroller (a Renesas H8S/2166 device), an IPMC FPGA, and nonvolatile RAM. For more information about the IPMC, refer to *Chapter 5, Hardware Management,* on page 43.

CPU complex FPGA

The CPU complex FPGA provides the legacy southbridge functions required by the CPM board and the functions used by legacy operating systems. CPU complex FPGA features include:

- Watchdog timers (see *IPMC watchdog* on page 49)
- Support for Ethernet controller LEDs on the front panel
- Transfer of RTM status and alarm signals over the RTM-link bus
- Additional glue logic

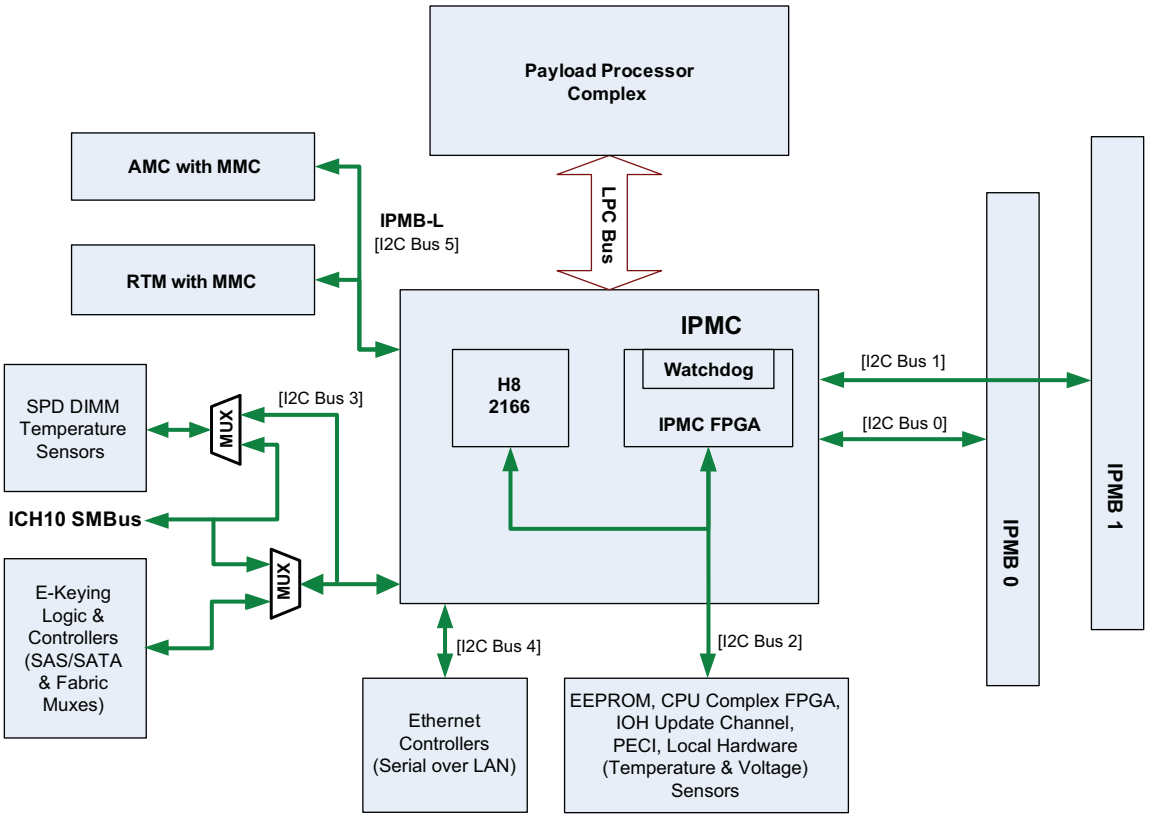
Access to most of the status and control functions are provided by a register file internal to the FPGA. The register file can be accessed by the LPC bus, by the IPMI SMBus, or by the ICH SMBus. Access to the registers is symmetrical; all of the busses have equal access to the internal registers of the FPGA for both reading and writing.

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The hardware management subsystem includes the Intelligent Platform Management Controller (IPMC), the managed sensors, and the communication interfaces to external entities such as the Shelf Manager. The IPMC controls the hardware management subsystem by enabling payload power and ports, detecting component hardware states, initiating resets, and monitoring managed sensors.

The CPM's hardware management system complies with the Intelligent Platform Management Interface (IPMI) 1.5 specification, which defines a set of common interfaces for managing the system and for monitoring system health. The IPMC (which is independent from the CPU) runs the IPMI firmware. This allows administrators to manage a system remotely even in the absence of operating system or system management software. Figure 10 shows the functional blocks making up the hardware management subsystem.

Figure 10. Hardware management subsystem block diagram



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IPMC description

The hardware management system of the CPM is controlled by an IPMC, which comprises a microcontroller, an IPMC FPGA, and EEPROMs for IPMC data storage. The IPMC interacts with the CPM's CPU and the Shelf Manager to:

- monitor temperature, voltage, and other sensors on the CPM
- control and monitor the hot swap process for the CPM, AMC, and RTM
- interact with the Shelf Manager to implement backplane E-Keying
- manage on-board E-Keying for the AMC and the RTM
- provide remote console access to the CPM payload

Using serial-over-LAN communications, the IPMC provides a remote user with access to the CPU serial console through the base interface. For more information, see *Serial-over-LAN* on page 57.

The CPM's CPU communicates with the IPMC through a keyboard controller style (KCS) interface, which provides access to IPMI functions. This allows the CPU to send messages to the CPM's IPMC or to any other management controller in the shelf. For a list of the IPMI commands and details on the sensors used on the CPM, refer to *Appendix B, IPMI commands and Managed Sensors,* on page 81).

IPMC microcontroller

The IPMC's microcontroller is a Renesas H8S/2166 microcontroller. This device is a general-purpose 32-bit microcontroller with sixteen 16-bit general registers. It can handle a 16-MB linear address space; it also contains 512 KB of embedded flash and 40 KB of RAM.

The IPMC microcontroller provides the only connection between the CPM and the external ATCA shelf IPMBs. The microcontroller implements six I²C interfaces. It also supports the following interfaces, monitoring the inputs and controlling the outputs:

- Digital inputs/outputs
- Analog-to-digital inputs
- HW-based I2C interfaces
- Serial interfaces
- LPC interfaces

IPMC FPGA

The IPMC FPGA consists of a Lattice LFXP6CF256I-3 FPGA that is used to provide General Purpose I/O (GPIO) expansion for the IPMC. General purpose outputs (GPOs) from the IPMC FPGA are configured and reserved for power and reset controls on the CPM.

When executing E-Key logic, the IPMC uses the IPMC FPGA to connect I²C bus 3 to the multiplexer (see *E-Key control of interfaces* on page 51).

The FPGA also contains the IPMC's hardware watchdog (see *IPMC watchdog*).

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IPMC SEEPROM

The IPMC provides 32 KB of serial EEPROM non-volatile memory located on an internal I2C connection. The memory is used to store IPMI-specific information and is divided into the partitions listed in Table 9. For details on the contents of the partitions, refer to *Appendix D, FRU Information,* on page 125.

Table 9. SEEPROM mapping

Description	Size (bytes)	Offset range
IPMC Boot Component Information	(0x0010) 16	0x0000 - 0x000F
FRU Information Area	(0x0BF0) 3056	0x0010 - 0x0BFF
Sensor Data Record (SDR)[a]	(0x0800) 2048	0x0C00 - 0x13FF
Sensor Parameters	(0x0800) 2048	0x1400 - 0x1BFF
Reset Data Save Area	(0x3280) 12928	0x1C00 - 0x4E7F
Local SEL Storage Area	(0x2000) 8192	0x4E80 - 0x6E7F
On-board E-Key Area	(0x0880) 2176	0x6E80 - 0x76FF
Clock E-Key Area	(0x0900) 2304	0x7700 - 0x7FFF

[a] The SDR storage area is unused in the CPM.

IPMC system event log

The CPM supports a System Event Log (SEL) for logging its own local events. The SEL space contains 8192 bytes with a 16 byte header, and each full SEL entry consumes 16 bytes of space. The SEL space can store a maximum of 511 entries. If the SEL becomes full, new events are logged by overwriting the oldest entries in the SEL (FIFO implementation). SEL entries are read by issuing the `GET SEL Entry` command. Issuing a `Clear SEL` command clears the SEL.

Events generated by sensors or the BIOS are forwarded to the Shelf Manager for storage in the shelf's SEL.

IPMC interface to the payload processor

The payload processor interface allows the CPU to communicate with the IPMC. The CPM implements this interface as a KCS port, which is similar to how a PC motherboard processor sends commands to a legacy PC-compatible keyboard controller. The IPMC is connected to the payload LPC bus and responds to I/O byte addresses as a KCS interface.

The CPM uses the serial IRQ output of the IPMC to implement the messaging interrupt for the payload. The IPMC uses the serial IRQ output to generate a legacy interrupt IRQ6 to the payload processor. During use of the KCS interface by the payload processor, output buffer full (OBF) conditions generate this interrupt to the payload if the IPMI driver on the payload processor is in interrupt-enabled mode.

The system BIOS and the OS-level code use this interface to interact directly with the IPMC. With OS packages that support OpenIPMI, the OpenIPMI driver and toolset are available to make it easier to write applications accessible to the IPMC or IPMI subsystem in the shelf. The CPM KCS interface is compatible with OpenIPMI.

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Summary of IPMC controls

The IPMC manages resets, power states, and IPMB isolation for the CPM and its AMC and RTM. The output actuators (defined in the PICMG 2.0 specification) are implemented as IPMC GPIO outputs controlled by the IPMI firmware.

Note: Under normal running conditions, the IPMC controls the state of the GPIO outputs. However, the controls can be accessed for debug situations using the Set/Get Control State OEM IPMI commands.

CPM controls

The IPMC manages the CPM controls listed in Table 10.

Table 10. IPMC-managed CPM controls

Control	Function
Payload Cold Reset	Platform Reset: controls Payload Cold Reset (generates SYS_RESET* to the I/O controller hub)
Payload Warm Reset	Warm Reset: controls Payload Warm Reset (generates INIT* to the CPM CPUs)
Payload Power Enable (Main)	CPM Payload Power Enable: controls the board main payload power supplies
IPMB0-A Isolator	Isolates the CPM IPMB0-A from the IPMB (Backplane)
IPMB0-B Isolator	Isolates the CPM IPMB0-B from the IPMB (Backplane)
Boot Flash Select	FLASH_SEL: controls the selection of which SPI flash device (0 or 1) is used for the BIOS during boot-strap
NMI Control	NMI: used to assert NMI to the payload processors.
Payload Interrupt Control	SERIRQ: used to assert the messaging interrupt to the payload processor.
CLK3_ENABLE	CLK3_EN: used to enable the CLK3A and CLK3B output buffers
Graceful Shutdown Interrupt	Asserts or de-asserts the interrupt to the X86 processor complex; indicating a graceful shutdown needs to be started.
Update Channel 4 TX Enable	UPDATE4_TXEN: used to enable or disable the update channel 4 transmission
Update Channel 4 RX Enable	UPDATE4_RXEN: used to enable or disable the update channel 4 reception

AMC controls

The IPMC manages the AMC controls listed in Table 11.

Table 11. IPMC-managed AMC controls

Control	Function
AMC Payload Power Enable (+12V)	AMC Bay Power Enable: controls AMC 12V power
AMC Isolator	AMC IPMB Enable: isolates the AMC module from the CPM IPMB-L (I2C Bus 5)
AMC Payload Reset	AMC Bay MMC Reset (ENABLE*)
AMC_PCIE_PRES	Asserted for AMC with PCI Express capability when the AMC is ready to be activated.
AMC_PCIE_BUTTON	Asserted for AMC with PCI Express capability to notify OS that the PCIe links can now be enabled (for training during activation) or disabled (during deactivation).

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Table 11. IPMC-managed AMC controls

Control	Function
AMC Management Power (+3.3V)	AMC_+3_3 Power Enable: controls AMC 3.3V management power
AMC PCIE CLK Enable	AMC_CLKEN: enables or disables 100Mhz differential clock for PCI Express on AMC bay

RTM controls

The IPMC manages the RTM controls listed in Table 12.

Table 12. IPMC-managed RTM controls

Control	Function
RTM Payload Power Enable (+12V)	RTM_+12 Power Enable: controls RTM 12V power
RTM Isolator	RTM I2C Enable: isolates the RTM module from the CPM I²C Bus 5
RTM Payload Reset	RTM Bay MMC Reset (ENABLE*)
RTM_PCIE_PRES	Asserted for RTM with PCI Express capability when the AMC is ready to be activated.
RTM_PCIE_BUTTON	Asserted for RTM with PCI Express capability to notify OS that the PCI Express links can now be enabled (for training during activation) or disabled (during deactivation).
RTM Management Power (+3.3V)	RTM_+3_3 Power Enable: controls RTM 3.3V management power
RTM PCIE CLK Enable	RTM_CLKEN: enables or disables 100Mhz differential clock for PCI Express on RTM

Overview of sensor management

The IPMC sensors monitor voltages, temperatures, control signals, and status events. IPMI events associated with these sensors are generated by the IPMC, based on state changes of the sensors.

The sensors monitoring the voltages are analog-to-digital inputs to the IPMC microcontroller and an ADM1066 voltage sequencer/monitor, which communicates with the microcontroller over an I²C bus. The sensors monitoring the control signals are digital inputs to the microcontroller and IPMC FPGA. Temperature sensors are used to measure the air temperature at various locations across the CPM. The IPMI firmware in the IPMC monitors all sensors in a continuous polling loop.

Each sensor has entries in the IPMC's sensor data records (SDRs). The CPM implements a type 0x12 record for the management controller and type 0x01 records for the full sensor descriptions. Standard IPMI commands read these sensors from the SDR description. See *Managed sensors* on page 87 for a list of sensors managed by the CPM.

CPM resets

The CPM supports only cold and powergood resets. The RST_SRC inputs of the IPMC are used to monitor the various reset sources on the board. When one of the inputs is asserted, an interrupt is generated.

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Cold reset

A cold reset is a total system board reset (except for the IPMI circuitry). All devices and registers are reset to their default state. After a cold reset, data in DRAM might be invalid due to the CPU memory controller discontinuing refresh cycles. Memory is then cleared during the system BIOS initialization.

Note: A cold reset on the CPM does not clear the sticky bits in the CPU and I/O hub registers. Clearing sticky bits requires a powergood reset. See *Powergood reset* for details.

Common causes of a cold reset include expiration of the watchdog timer interval, invocation of the FRU Control IPMI command with the Cold Reset option, and control by the user's own application software running on the processor. Table 13 lists the sources that can initiate a cold reset and the resultant actions.

Table 13. Cold reset sources

Cold Reset Source	Action
Initial Watchdog timeout	CPU complex FPGA asserts SYS_RESET* (low). See *Initial watchdog*.
Programmable Watchdog timeout	CPU complex FPGA asserts SYS_RESET* (low). See *Programmable watchdog*.
Watchdog 1 timeout	IPMC asserts SYS_RESET* (low). See *OS watchdog*.
"FRU Control (Cold Reset) IPMI command"	IPMC asserts SYS_RESET* (low). See *Supported IPMI commands* on page 81.
IPMC Corrupt Flash Watchdog expires	IPMC asserts SYS_RESET* (low) and drives FLASH_SEL to select the alternate SPI flash. The IPMC then de-asserts SYS_RESET* (high) to allow the CPM to attempt to boot from the alternate flash. See *Corrupt flash detection watchdog*.
CPU XDP emulator reset	CPU XDP port asserts SYS_RESET* (low)
06h written to Reset Control register (CF9h)	ICH asserts PLTRST* (low)
Pushbutton reset is asserted	The CPU complex FPGA asserts SYS_RESET* (low).

Powergood reset

A powergood reset is similar to a cold reset, except that all sticky bits in the CPU and I/O hub registers are also cleared. A powergood reset can be initiated by the BIOS or user application by writing 0Eh to the CF9h reset register on the ICH10R.

Note: A powergood reset should only be used when the sticky bits need to be cleared.

Watchdog timers

The CPM provides five watchdog timers (see Table 14 on page 49) to help prevent the board from entering an unrecoverable state. The CPU complex FPGA, the IPMC, and the IPMC FPGA provide the watchdog timers. Figure 11 on page 49 illustrates when and how the CPM enables, resets, and disables watchdog timers.

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Figure 11. Watchdog timer operation

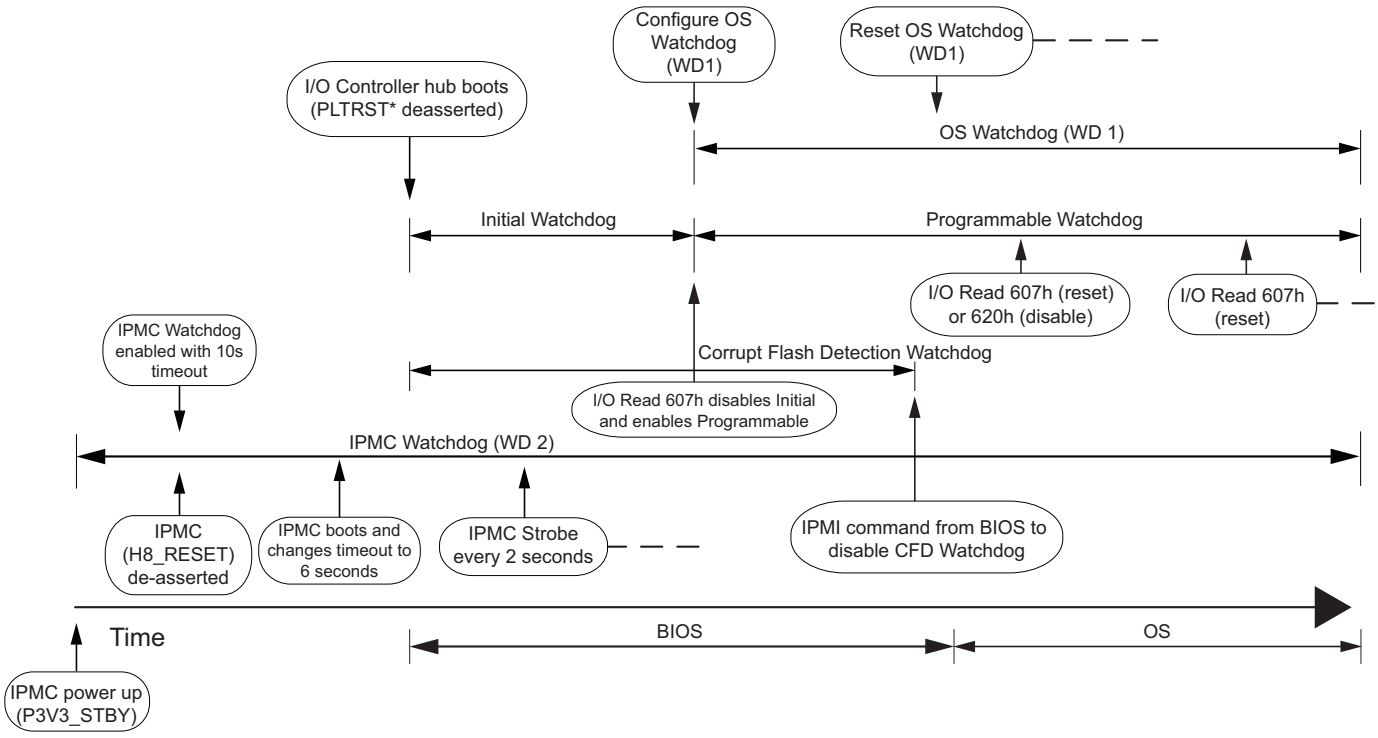


Table 14. Watchdog timer locations and controls

Watchdog	Location	Controlled by	Action
IPMC watchdog (WD 2)	IPMC memory block	IPMC	Resets and isolates the IPMC block
Corrupt Flash Detection (CFD) watchdog	IPMC	CPU	Power cycle, followed by boot from secondary SPI flash device
Initial watchdog	CPU complex FPGA	CPU	Cold reset
Operating system (OS) watchdog (WD 1)	IPMC	CPU	Cold reset
Programmable watchdog	CPU complex FPGA	CPU	Cold reset

IPMC watchdog

The IPMC FPGA includes a hardware watchdog timer, referred to as Watchdog 2. This watchdog prevents IPMC hardware or firmware problems from impacting the ability of other modules installed in the chassis to use the IPMB buses.

The IPMC watchdog is enabled by default and starts running as soon as power is present and the IPMC FPGA has loaded its internal flash image into its internal SRAM. The default timeout on power-up is 10 seconds. After the IPMC boot-loader is finished, the IPMC reprograms the timeout for 6 seconds and will continue to strobe every 2 seconds. If a firmware or hardware problem on the IPMC causes it to stop strobing the watchdog timer in the IPMC FPGA, the IPMC is automatically isolated from the IPMB-A, IPMB-B, and IPMB-L buses so they remain functional for the remaining blades in the chassis and then resets the IPMC.

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Corrupt flash detection watchdog

The Corrupt Flash Detection (CFD) watchdog is a software-based watchdog that allows the CPM to recover when the primary SPI flash is either blank or the boot block is corrupted. The CFD watchdog is implemented in the IPMC and is controlled by the CPU. The system BIOS must send an IPMI command to disable the watchdog within 30 seconds to prevent the timer from expiring.

The CFD watchdog timer is started any time a reset is asserted to the payload processor (payload cold reset, push button reset, or any other reset). Responsibility is then passed to the system BIOS to disable the timer. If the timer is not disabled before it expires, and the previous reset (if one exists) was a cold reset or a power-on reset, then the IPMC firmware disables payload power, selects the secondary SPI flash, then enables payload power to boot from the secondary SPI flash. If the timer is not disabled before it expires, then the IPMC firmware asserts and de-asserts cold reset.

Initial watchdog

The initial watchdog is a hardware-based watchdog timer that protects the CPM from getting stuck before it initializes any of the programmable watchdogs. It is implemented in the CPU complex FPGA and is controlled by the CPU. To prevent the timer from expiring and triggering a cold reset, the system BIOS must disable the initial watchdog and enable the programmable watchdog within 1 second by reading absolute address location 607h.

OS watchdog

The operating system (OS) watchdog, referred to as WD 1, is a programmable watchdog that triggers a cold reset if some fault condition in the system prevents the CPU from writing a service pulse to the timer within the programmed time interval.

The OS watchdog is implemented in the IPMC and can be configured or disabled by standard IPMI v1.5 commands. Its programmable range is from 10 ms to 6,553,600 ms in 100 ms intervals.

Programmable watchdog

The programmable watchdog is implemented by timer 0 in counter 0 (82C54 function) in the CPU complex FPGA. The timer expires and triggers a cold reset if it does not receive a service pulse from the CPU within the programmed time interval. The programmable range is from 819 µs to 53.67 s in 819 µs intervals.

The first I/O read of absolute address 607h enables the programmable watchdog and disables the Initial watchdog. Subsequent reads of this location reset the timer. An I/O read of absolute address 620h disables the watchdog.

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Hot swap of the CPM and managed FRUs

The CPM and its managed FRUs are hot-swap capable and meet the hot-swap requirements defined in the PICMG 3.0 Revision 2.0 *AdvancedTCA Base Specification*. The Shelf Manager controls the hot-swap process, and the IPMC enables and disables payload power to the managed FRUs (the AMC and the RTM) when instructed by the Shelf Manager.

The IPMC is responsible for enabling power to the AMC bay and for determining the functionality through E-Keying. AMC FRU E-Key records indicate the types of connections supported by the installed AMC. For more information, refer to *AMC bay* on page 39.

AMCs that use a PCI Express connection to the CPM are handled in a special way. The I/O controller hub (ICH) supports PCI Express hot-swap and participates in PCI Express link training. A hot swap is enabled by the system BIOS and IPMC working in conjunction to allow an AMC to be added to or removed from the system without powering down or resetting the CPM.

When the RTM is inserted and the RTM latch is closed, a signal to the IPMC enables the I^2C bus to the RTM. The RTM will be enabled when the IPMC detects a supported RTM via the FRU EEPROM. The IPMC will configure the I/O expander on the RTM via the I^2C bus, and then enable the payload to the Zone 3 RTM connector.

E-Key control of interfaces

Electronic Keying (E-Keying) control is used to verify interface compatibility, prevent damage to hardware, and prevent incorrect operation. The Shelf Manager collects E-Key records that describe the Fabric, Base, update channel, and synchronization clock Interfaces implemented by the shelf and other boards in the system. The PICMG 3.0 Revision 2.0 *AdvancedTCA Base Specification* requires the CPM to support E-Key control by describing its backplane interfaces to the Shelf Manager. For some interfaces, the CPM can respond to Shelf Manager commands by isolating the interfaces from the backplane.

The IPMC is used to:

- Disable and enable Ports 0-3 on each Fabric channel.
- Communicate with the memory module controller (MMC) on the AMC to read the FRU data for E-Keying.
- Control the CLK3 connection between the CPM and the CLK3A and CLK3B busses on the backplane.

Update channel 0 is considered the “fast path” update port and connects the AMC bay port 12 to the Zone 2 connector. It is E-Keyed (enabled or disabled) through a set of differential buffers that are controlled by the IPMC. Update channel 4 is considered the “slow path” update port and connects the AMC bay port 13 to the Zone 2 connector. The “slow path” is E-Keyed with single-ended TTL-level buffers. The backplane connects the update channels to an adjacent physical slot and provides operational redundancy across the backplane.

The RTM has two x4 PCI Express ports that require E-keying as part of the hot swap handshaking that must take place between the MMC on the RTM, the IPMC, and the I/O hub. Ports 17-20 on the AMC are directly connected between the AMC bay and the RTM. AMC bay port 15 also routes directly to the RTM for I^2C and RS-232. The E-keying for these ports is controlled by the MMC on the RTM and the AMC.

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Table 15 and Table 16 list I/O channels from the IPMC that provide E-Key control for each channel and port of the Fabric interface, update channel, and synchronization clocks.

Table 15. Fabric interface I/O E-Key descriptions

Fabric channel[a]	Port 0 control	Port 1 control	Port 2 control	Port 3 control	Comments
1	IPMC	IPMC	IPMC	IPMC	Connected through an Ethernet controller to the CPU.
2	IPMC	IPMC	IPMC	IPMC	

[a] Fabric channels 3 through 15 are not used on the CPM.

Table 16. Update channel and synchronization clock E-Key descriptions

Channel	Controlled by	Comments
Update channel 0	IPMC	PMC8380 (shared with SAS multiplexer) between AMC bay port 12 and backplane update channel 0
Update channel 1	IPMC	Not used
Update channel 2		
Update channel 3		
Update channel 4	IPMC	TTL-Level buffers between AMC bay 1 port 13 and update channel 4
Synchronization clock 1A	Always disabled	8-KHz clock input from backplane
Synchronization clock 1B		
Synchronization clock 2A	Always disabled	19.44-MHz clock input from backplane
Synchronization clock 2B		
Synchronization clock 3A	IPMC, CPU	AMC synchronization clock output to backplane. IPMC has global control of whether clocks are driven. CPM has control of which clock (CLK3A or CLK3B or none) is driven.
Synchronization clock 3B	Disabled by default; enabled by E-Key when a supported device function is detected.	

As an AMC carrier, the CPM IPMC works with the AMC's module management controller (MMC) to match the ports on the AMC's connector to the corresponding CPM ports. The IPMC or MMC can disable many of the ports that are not compatible. Table 17 lists the entities that provide E-Key control for each AMC port on the CPM.

Table 17. AMC connector port E-Key descriptions

Channel	Controlled by	Comments
AMC bay TCLKA	CPU	Not supported
AMC bay TCLKB	CPU	Differential buffer driving TCLKB from AMC bay to CPM
AMC bay TCLKC	IPMC, CPU	Not supported
AMC bay TCLKD	IPMC, CPU	Differential buffer driving TCLKD from AMC bay to CPM
AMC bay FCLKA	MMC[a],IPMC	Differential buffer driving FCLKA from CPM to AMC bay

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Table 17. AMC connector port E-Key descriptions

Channel	Controlled by	Comments
AMC bay port 0	MMC, IPMC	1000BASE-BX or -KX to Fabric A port 1
AMC bay port 1	MMC, IPMC	1000BASE-BX or -KX to Fabric B port 1
AMC bay port 2	MMC, IPMC	3.0G SAS/SATA to SAS mux that connects to ICH SATA port 0 or SAS1064E controller on RTM
AMC bay port 3	MMC, IPMC	3.0G SAS to SAS1064E controller on RTM
AMC bay ports 4 - 7	MMC, IPMC, CPU	AMC Bay 1 Ports 4-7 PCI Express connected to IOH Gen 2 PCI Express port 9 (x4)
AMC bay port 8	MMC, IPMC	1000BASE-BX or -KX to Fabric A port 2
AMC bay port 9	MMC, IPMC	1000BASE-BX or -KX to Fabric B port 2
AMC bay port 10	N.A.	unused
AMC bay port 11	N.A.	unused
AMC bay port 12	IPMC	Differential transceiver on CPM between port 12 and update channel 0 (fast path)
AMC bay port 13	IPMC	TTL-level buffers on CPM 1 between port 13 and update channel 4
AMC bay port 14	IPMC, CPU	TCLKD; see above.
AMC bay port 15 I2C	MMC, MMCR[b]	I²C connected to SFP on RTM
AMC bay port 15 serial	MMC, MMCR	Serial connected to RS-232 buffer on RTM
AMC bay port 16	MMC, IPMC	FCLKA; see above.
AMC bay port 17	MMC, MMCR	1000BASE-BX or SGMII connected to SFP on RTM
AMC bay port 18	MMC, MMCR	1000BASE-BX or SGMII connected to SFP on RTM
AMC bay port 19	MMC, MMCR	1000BASE-BX or SGMII connected to SFP on RTM
AMC bay port 20	MMC, MMCR	1000BASE-BX or SGMII connected to SFP on RTM

[a] The enable is driven by the AMC module management controller (MMC).

[b] The enable is driven by the RTM MMC.

Table 18 lists the E-Key controls for additional RTM ports.

Table 18. RTM connector port E-Key descriptions

Port	Controlled by	Comments
RTM PCI Express port 0	IPMC, MMC, CPU	Gen 2 PCI Express port 4 from the I/O hub.
RTM PCI Express port 1	IPMC, MMC, CPU	Gen 2 PCI Express port 7 from the I/ O hub.

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IPMI-over-LAN

A remote management application can establish an IPMI-over-LAN session with the IPMC. The IPMC is remotely accessible through the front serial port (COM1), the rear serial port (COM2), and the Base Ethernet ports. The CPM implements IPMI-over-LAN using RMCP and RMCP+ as described in the IPMI 2.0 specification. The IPMI-over-LAN session can be used to enable the functionality described in *Serial-over-LAN* on page 57.

Configuring IPMI-over-LAN access

The CPM must be initially configured to make IPMI-over-LAN access available. The IPMC saves the configuration changes in non-volatile RAM so they are not lost during reboots, hot-swaps, or firmware upgrades.

Before you begin

1. Gather the following resources:
   - A remote computer with network access to the Shelf Manager in the shelf with the CPM.

     Note: The initial steps can be run directly on the CPM's CPU as an alternative.
   - An *rsys-ipmitool* utility (available from RadiSys).
2. Be prepared to fill in values for these variables:

`<ShMgr_IP>`	The IP address of the Shelf Manager.
`<IPMB>`	The IPMB address of the CPM in the shelf.
`<channel>`	The IPMI channel number representing a CPM Base interface channel or the front/rear Ethernet interface channel. Channel 02 represents the Base interface channel that connects to the hub module in the lower-numbered slot, and channel 03 connects to the hub module in the higher-numbered slot. Channel 08 represents ETHA on the front panel and channel 09 represents ETHB on the front panel if the CPM is configured for Front Ethernet in BIOS setup. If it is configured for Rear Ethernet in the BIOS, Channel 08 is ETHA and Channel 09 is ETHB on the RTM.
`<IP>`	The static IP address to assign to each CPM Base interface channel and the front and rear Ethernet interface channels.
`<protocol>`	The protocol to use (`lan` for RMCP or `lanplus` for RMCP+). The configuration steps are done only once and apply to both protocols.

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IPMI-over-LAN basic configuration steps

From the Linux prompt:

1. Set the IP address for a Base interface channel or the front/rear Ethernet interface channel:

   rsys-ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **lan set** *<channel>* **ipaddr** *<IP>*

   The **-I** option specifies the IPMI interface to use (**lan**), and the **-A** option specifies an authentication type to use during session activation (**none**). The other command options are defined in step 2 on the previous page.

   Tip: To run the commands directly on the CPM's CPU, omit the `-I, -H, -A, and -t` options. This shortens the above command to:

   rsys-ipmitool lan set *<channel>* **ipaddr** *<IP>*

2. Repeat step 1 to set the IP addresses for the other channels.

3. View the current settings for each channel:

   rsys-ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **lan print** *<channel>*

4. Verify IPMI-over-LAN access by displaying the system event log (SEL).

   rsys-ipmitool -I lanplus -H *<IP>* **-A none -C 0 sel**

   Important: Do this step from a remote computer to verify IPMI-over-LAN access.

   SEL information should be displayed, which verifies access to IPMI services without relying upon the Shelf Manager. Verifying "lanplus" access also verifies "lan" access.

   If this command does not display SEL information or gives an error, perform the steps in *IPMI-over-LAN additional configuration steps*.

5. Repeat step 4 to verify access to the IP addresses of the other channels.

IPMI-over-LAN additional configuration steps

If IPMI-over-LAN does not work after performing the basic steps:

1. Set the user privileges for both channels:

   rsys-ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **user priv 1 4 2**

   rsys-ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **user priv 2 4 2**

2. Set the channel and administrator access for a channel:

   rsys-ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **raw 06 0x40** *<channel>* **0x42 0x44**

   rsys-ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **raw 06 0x40** *<channel>* **0x82 0x84**

   rsys-ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **channel getaccess** *<channel>* **01**

   rsys-ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **channel setaccess** *<channel>* **01 ipmi=on link=on privilege=4**

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3. Repeat step 2 to set access to the other channel.
4. Verify IPMI-over-LAN access by displaying the SEL.

   rsys-ipmitool -I lanplus -H *<IP>* **-A none -C 0 sel**

   SEL information should be displayed. If this command does not display SEL information or gives an error, see *IPMI-over-LAN troubleshooting steps*.
5. Repeat step 4 to verify access to the IP address of the other channel.

IPMI-over-LAN troubleshooting steps

1. View the current settings for a channel:

   rsys-ipmitool -I *<protocol>* **-H** *<ShMgr_IP>* **-A none -t** *<IPMB>* **lan print** *<channel>*
2. Verify that the IP address is correct.
3. Verify that a non-zero MAC address is set.

   A MAC address of 00:00:00:00:00:00 indicates the Ethernet controller is not responding to queries. This can occur if the Ethernet controller does not have the correct EEPROM file. Upgrade the Base EEPROM image and the front/rear Ethernet EEPROM image using the image files and instructions from the RadiSys software distribution.
4. Repeat steps 1–3 to check the settings for the other channel.

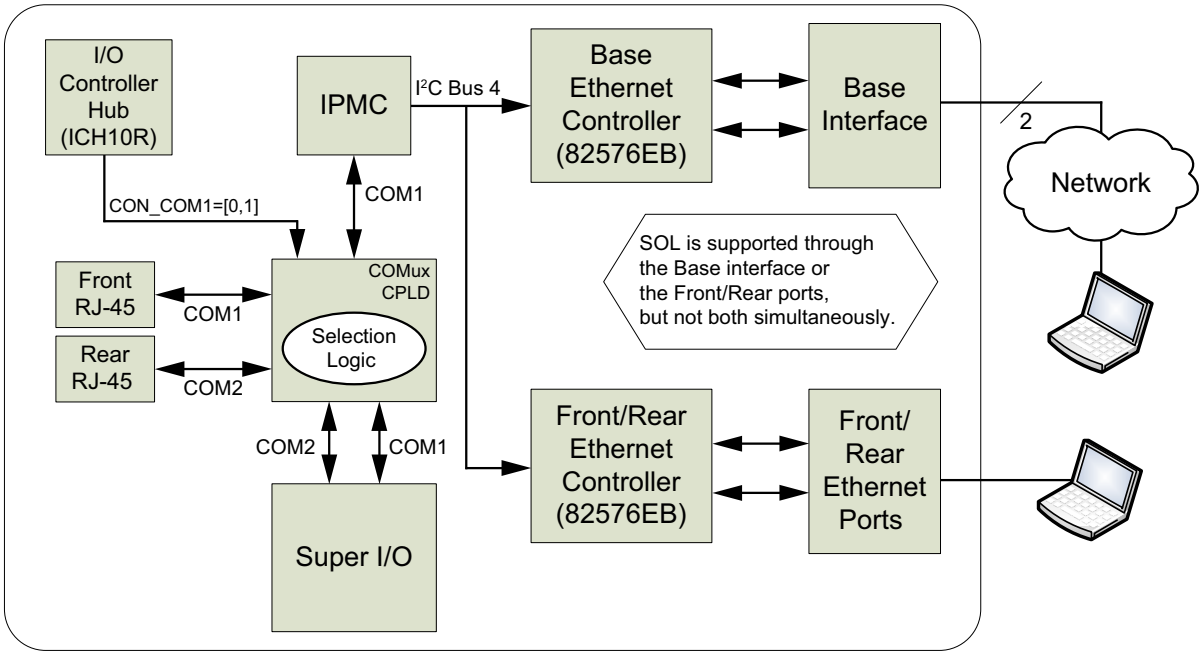
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Serial-over-LAN

Serial-over-LAN (SOL) is the specification of packet formats and protocols for transmitting serial data over a LAN using IPMI-over-LAN packets. SOL operation is conceptually straightforward. A remote management application can establish an IPMI-over-LAN session with the IPMC. Once the session is established, the remote console can request that the SOL session be activated.

The COMux CPLD contains the multiplexer functionality for routing COM port signals. The COM port selection is a combination of the COMux CPLD and BIOS menu selection. There is a BIOS bit that selects the COM snoop and selection priority for COM1 or COM2 (front or rear ports, respectively). Figure 12 shows the overall SOL architecture.

Figure 12. Serial-over-LAN



A SOL session is established on a first-come, first-serve basis through one of the Base Ethernet ports or the front and rear Ethernet ports. If neither the front nor the rear serial port has a cable connected to it, then the system BIOS configuration determines which ports get read and write access. If cables are connected to both the front and rear ports, the BIOS configuration determines which port is granted access. If only one cable is connected, read access is granted to that port. Table 19 summarizes these settings.

Table 19. Truth table for serial port connections

Control inputs			Port connections		
Front cable detect	RTM cable detect	COM1 GPIO	Super I/O COM1 connection	Super I/O COM2 connection	IPMC SOL port connection
0	0	0	IPMC SOL	N/C	COM1
0	0	1	N/C	IPMC SOL	COM2
0	1	x	N/C	Rear SFP	Snoop COM2
1	0	x	Front RJ-45	N/C	Snoop COM1

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Table 19. Truth table for serial port connections (Continued)

Control inputs			Port connections		
1	1	0	Front RJ-45	Rear SFP	Snoop COM1
1	1	1	Front RJ-45	Rear SFP	Snoop COM2

Cable detection is provided by an Intersil ISL4243E RS-232 transceiver. When valid RS-232 signal levels at the front connector are detected, the transceiver asserts the COM1_CBLDET signal (high) to COMux CPLD and the IPMC.

In SOL mode, any outgoing characters from the ICH are assembled into packets by the IPMC and sent to the remote console over one of the Base LAN interfaces. Conversely, inbound LAN packets carrying characters for the system serial controller have their character data extracted by the IPMC and delivered to the baseboard serial controller. The SOL character data is contained in SOL messages carried in UDP datagrams. The packet format is "IPMI v2.0 RMCP+" with the payload type set to "SOL".

Note: The CPM supports one SOL session at a time. The session must be closed before another session can be opened (through the other Base interface channel or the front/rear Ethernet interface channel).

Establishing a SOL session

Prerequisite: This procedure assumes that the required setup for IPMI-over-LAN has been done once for this CPM. For details, see *Configuring IPMI-over-LAN access* on page 54.

One-time SOL configuration steps

Important: For these one-time steps, use the RadiSys-supplied *rsys-ipmitool* utility.

To configure retry settings from a remote computer:

1. Configure the retries to keep SOL sessions open for a Base, front, or rear interface IP address.

   `rsys-ipmitool -I <protocol> -H <IP> -A none -C 0 sol set retry-interval 0xF0`

   `rsys-ipmitool -I <protocol> -H <IP> -A none -C 0 sol set retry-count 7`

   For an explanation of **`<protocol>`** and **`<IP>`**, see *Before you begin* on page 54.

2. Repeat step 1 to configure retries for the other Base interface IP address and the front or rear interface IP address.

3. View the retry settings for a Base, front, or rear interface IP address.

   `rsys-ipmitool -I <protocol> -H <IP> -A none -C 0 sol info`

   The retry count should be 7, and the retry interval should be 2400 ms.

4. Repeat step 3 to verify access to the remaining interface IP addresses.

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SOL session open steps

To open a SOL session from a remote computer:

1. Activate the SOL console window:

   rsys-ipmitool -I *<protocol>* **-H** *<IP>* **-A none -C 0 sol activate**

   The SOL session is established. If a cable is attached to the CPM front panel serial port, the SOL window is read-only. It is read-write if no cable is attached.

2. Perform an action (such as pressing Enter) from the local serial console if a serial cable is attached, or from the SOL console window if no cable is attached.

   The SOL console window should respond.

SOL session close step

Note: Only one SOL session can be open at a time to a single CPM.

To terminate a SOL session directly from the active SOL window, enter these characters:

~.

To terminate a SOL session from another window, enter:

rsys-ipmitool -I *<protocol>* **-H** *<IP>* **-A none -C 0 sol deactivate**

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SYSTEM BIOS 6

The system BIOS is based on AMIBIOS® from American MegaTrends and is adapted by RadiSys. It appears to be a traditional BIOS, but the AMIBIOS firmware is compatible with an extensible firmware interface (EFI) and supplies a compatibility support module. The BIOS offers pre-EFI initialization and a pre-initialization shell, a driver execution environment, and boot services.

BIOS setup menus

The system BIOS contains a setup utility for modifying the system configuration. The system configuration information is maintained in the redundant boot flash devices and is used by the system BIOS to initialize the hardware.

Access to the setup menus is available for only a short time during the boot process. Pressing **F2** during boot enables access to the setup utility. The **Delete** key is an alternative that works in some situations when **F2** does not.

The BIOS setup menus include standard AMIBIOS menus and additional custom menus from RadiSys. A legend on the right side of each menu provides navigation and selection information.

BIOS menu options

Table 20 gives a general overview of the BIOS setup menus.

Table 20. BIOS setup menus and key options

Menu	Key settings and information	
Main	▪ BIOS information ▪ Memory information ▪ Language configuration	▪ Date and time configuration ▪ Access privilege level information
Advanced	▪ PXE boot interface configuration ▪ Front or rear Ethernet port selection ▪ PCI subsystem configuration ▪ Trusted computing configuration ▪ CPU configuration	▪ SATA configuration ▪ USB configuration ▪ Super I/O configuration ▪ Serial port console redirection
Chipset	▪ North bridge configuration	▪ South bridge configuration
IPMI	▪ POST watchdog configuration ▪ OS watchdog configuration	▪ FRU information
Boot	▪ Quiet boot configuration ▪ BIOS setup prompt timeout configuration ▪ Fast boot configuration ▪ Current boot flash device identification ▪ Boot flash device selection	▪ Boot priority configuration for groups of devices ▪ Boot priority configuration within network devices group ▪ Boot priority configuration within hard drive group

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Table 20. BIOS setup menus and key options (Continued)

Menu	Key settings and information	
Security	▪ Administrator password setting	▪ User password setting
Save & Exit	▪ Save or discard changes ▪ Exit BIOS ▪ Reset CPM	▪ Restore factory defaults ▪ Save or restore user defaults ▪ Override boot source for next boot

Some configuration settings can result in hardware conflicts. It is important to understand the hardware configuration and resource needs to prevent conflicts.

BIOS boot specification (BBS) boot devices and priorities

The possible BIOS boot specification (BBS) boot devices are organized into these groups:

- Hard disk devices (SAS, SATA, USB HDD, USB flash depending on format, iSCSI volumes)
- Removable USB media devices (USB floppy drive, USB flash depending on format)
- Removable media devices (CD-ROM, DVD-ROM)
- Network devices (PXE)

Note: EFI boot options, such as the EFI shell and UEFI, are also listed but not grouped.

The groups can be arranged in order of boot priority (Boot Option1, Boot Option2, and so on), and the devices can be arranged in order of boot priority within each group. For details, see Table 20 on page 61 for the group boot priority configuration options in the Boot menu.

The CPM initially attempts to boot from the first priority device in the first priority group. If unsuccessful, it attempts to boot from each device in the first group in priority order before trying the first device in the second group, and so on. Any group or device can be set to a boot priority of disabled to prevent booting from it.

Configuring the front or rear Ethernet ports

The Ethernet ports can be configured to use either the front panel Ethernet ports or the RTM Ethernet ports. A LAN adapter initially sets front or rear Ethernet in the front/rear Ethernet EEPROM, and this becomes the default configuration. The EEPROM configuration can be overridden using this BIOS menu item:

Advanced > Front/Rear Ethernet

Select EEPROM Setting with the same menu item to return to the default configuration.

When the rear ports are selected, either EEPROM Setting, Front/Copper, Rear/SerDes, or Rear/SGMII can be selected. See Table 21 for port configuration details.

Table 21. Ethernet port configurations

Setting	Configuration
EEPROM Setting	Link direction and mode depends on EEPROM configuration
Front/Copper	Link route to front panel, copper mode
Rear/SerDes	Link route to RTM, SerDes mode
Rear/SGMII	Link route to RTM, SGMII mode

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Extensible firmware interface (EFI) shell

The BIOS supports an EFI shell that allows the execution of EFI commands, scripts, or applications before the OS boots.

The EFI shell can be accessed in one of these ways:

- Make the EFI shell the first priority in the BIOS boot priority options. Each subsequent CPM reboot goes to the EFI shell.
- Override the configured boot priorities and immediately boot to the EFI shell using this BIOS menu item:

  Save & Exit > Built-in EFI Shell

Note: A key must be pressed to enter the EFI shell. The shell will terminate after 10 seconds if no key is pressed, then the boot process will proceed.

For more EFI shell information, visit http://www.tianocore.org and review the *EFI Shell User's Guide* and the *Shell Command Reference Manual*. The CPM BIOS includes the set of commands defined in the default build shell.

BIOS error and event reporting

The BIOS sends system events, boot events during early POST tasks, and POST error events to the IPMC during BIOS start-up, early POST tasks, and execution. The IPMC logs the events to its local SEL and forwards them to the system SEL.

Accessing the SEL

Messages in the SEL are viewed using the *rsys-ipmitool* utility. For example, to view the system SEL from a system that has LAN connectivity to the active Shelf Manager:

```
rsys-ipmitool -I lan -H <Shelf_Mgr_IP_addr> -A NONE -t 0x20 sel list
```

Use the `-h` option to obtain help using the utility. To view the CPM's local SEL, substitute the IPMB address of the CPM for the value 0x20 in the command above. See the *Shelf Management Software Reference* for the IPMB addresses of the slots in each RadiSys shelf.

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SEL event codes

Table 22 lists the sensor events generated by the BIOS.

Table 22. SEL sensor events generated by the BIOS (Sheet 1 of 4)

Sensor type	Sensor type code	Sensor-specific offset	Event description
Processor	07h	00h	IERR
		01h	Thermal trip
		02h	FRB1/BIST failure
		03h	FRB2/hang in POST failure related to a processor failure. The system firmware progress sensor is used for other BIOS hangs.
		04h	FRB3/processor startup/initialization failure (CPU didn't start)
		05h	Configuration error
		06h	SM BIOS uncorrectable CPU-complex error
		07h	Processor presence detected
		08h	Processor disabled
		09h	Terminator presence detected
Memory	0Ch	00h	Correctable ECC / other correctable memory error
		01h	Uncorrectable ECC / other uncorrectable memory error
		02h	Parity
		03h	Memory scrub failed (stuck bit)
		04h	Memory device disabled
		05h	Correctable ECC / other correctable memory error logging limit reached The Event Data 3 field can be used to provide an event extension code with this definition: 7:0 DIMM/SIMM/RIMM identification, relative to the entity associated with the sensor (if SDR provided for this sensor)
POST memory resize	0Eh	FFh	Memory resize event

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Table 22. SEL sensor events generated by the BIOS (Sheet 2 of 4)

Sensor type	Sensor type code	Sensor-specific offset	Event description
System firmware progress	0Fh	00h	System firmware error (POST error) The Event Data 2 field can be used to provide an event extension code, with this definition: Event Data 2: 00h Unspecified 01h No system memory is physically installed in the system 02h No usable system memory (all installed memory has experienced an unrecoverable failure) 03h Unrecoverable hard-disk/ATAPI/IDE device failure 04h Unrecoverable system-board failure 05h Unrecoverable diskette subsystem failure 06h Unrecoverable hard-disk controller failure 07h Unrecoverable PS/2 or USB keyboard failure 08h Removable boot media not found 09h Unrecoverable video controller failure 0Ah No video device detected 0Bh Firmware (BIOS) ROM corruption detected 0Ch CPU voltage mismatch (processors that share same supply have mismatched voltage requirements) 0Dh CPU speed matching failure 0Eh to FFh reserved
		01h	System firmware hang (shares the Event Data 2 definition with 02h system firmware progress)

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Table 22. SEL sensor events generated by the BIOS (Sheet 3 of 4)

Sensor type	Sensor type code	Sensor-specific offset	Event description
System firmware progress (continued)	0Fh (continued)	02h	System firmware progress The Event Data 2 field can be used to provide an event extension code, with this definition: Event Data 2: 00h Unspecified 01h Memory initialization 02h Hard-disk initialization 03h Secondary processor(s) initialization 04h User authentication 05h User-initiated system setup 06h USB resource configuration 07h PCI resource configuration 08h Option ROM initialization 09h Video initialization 0Ah Cache initialization 0Bh SM bus initialization 0Ch Keyboard controller initialization 0Dh Embedded controller/management controller initialization 0Eh Docking station attachment 0Fh Enabling docking station 10h Docking station ejection 11h Disabling docking station 12h Calling operating system wake-up vector 13h Starting operating system boot process, e.g., calling Int 19h 14h Baseboard or motherboard initialization 15h reserved 16h Floppy initialization 17h Keyboard test 18h Pointing device test 19h Primary processor initialization

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Table 22. SEL sensor events generated by the BIOS (Sheet 4 of 4)

Sensor type	Sensor type code	Sensor-specific offset	Event description
Event logging disabled	10h	00h	Correctable memory error logging disabled
		01h	Event "Type" logging disabled. Event logging is disabled for the following event/reading type, and the offset has been disabled. Event Data 2: Event/reading type code Event Data 3: [7:6] Reserved, write as 00 binary [5] 1 (binary) - Logging has been disabled for all events of given type [4] 1 (binary) = Assertion event, 0 (binary) = deassertion event [3:0] Event offset
		02h	Log area reset/cleared
		03h	All event logging disabled
Critical interrupt	13h	00h	Front panel NMI/diagnostic interrupt
		01h	Bus timeout
		02h	I/O channel check NMI
		03h	Software NMI
		04h	PCI PERR (PCI parity error, PCI Express advanced error, hub interface error, system bus error, memory buffer error)
		05h	PCI SERR (PCI system error)
		06h	EISA fail safe timeout
		07h	Bus correctable error
		08h	Bus uncorrectable error
		09h	Fatal NMI (port 61h, bit 7)
Boot error	1Eh	00h	No bootable media
		01h	Non-bootable diskette left in drive
		02h	PXE server not found
		03h	Invalid boot sector
		04h	Timeout waiting for user selection of boot source
OEM reserved	C0h-FFh	-	-

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Field replaceable units (FRUs)

The following CPM-related items can be installed or replaced:

- The CPM itself. For installation instructions, see the *ATCA-4500 Compute Processing Module Installation Guide*. For removal instructions, see *Removing and installing the CPM, RTM, or AMC*.
- The DIMMs. For placement information and installation and removal instructions, see *Chapter 2, Installing Memory Modules,* on page 15.
- A compatible AMC. For installation instructions, see the *AMC Installation Guide*.
- A compatible RTM. For installation instructions, see the *ATCA-4500 Compute Processing Module Installation Guide*.

Removing and installing the CPM, RTM, or AMC

The following steps explain the hot-swap procedure for replacing the CPM, RTM, or AMC:

1. Read *Electrostatic discharge* on page 8 and make sure you are adequately grounded before handling any of the modules.
2. Before replacing the CPM, disconnect all cables from the front panel. Before replacing the RTM, disconnect all cables from the rear panel.

   Before swapping the AMC, proceed to step 4.
3. Loosen the two thumbscrews securing the CPM or the RTM.
4. Release the AMC handle or the module ejector latch that contains the hot-swap switch. This will be either the right or the bottom ejector latch, depending on whether the module is oriented vertically or horizontally. *Do not release the other latch at this time.*

   When the handle or ejector latch is opened, a signal is sent to the IPMC which causes the blue hot-swap LED to begin blinking.

   WARNING! Do not remove an AMC, CPM, or RTM before its hot-swap LED turns solid blue. Removing it prematurely can cause unpredictable results in other parts of the system.
5. When it is safe to remove the AMC or module, the hot-swap LED stops blinking and remains on.

   WARNING! Be careful not to touch any heatsinks when removing the AMC, RTM, or CPM because they might be hot to the touch. If possible, wait 3 to 5 minutes after the hot-swap LED turns solid blue to give the air flow in the system time to cool the board.

   To remove an AMC, pull the module handle firmly and slide the module out of the bay.

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To remove the CPM or RTM, release the other ejector latch (the non-hot swap latch), then simultaneously pull both ejector latches to disengage the module from the backplane and remove it from the chassis.

6. Place the AMC, RTM, or CPM on a flat, static-free surface.
7. Install the replacement AMC, RTM, or CPM.

   To install an AMC, insert the AMC into the bay opening, and slide it along the guide rails until it is firmly seated into the CPM's connector. Check to make sure that the EMC gasket is making a tight seal. Press the module handle firmly into the AMC until it stops, which will start the AMC power cycle.

   To install a CPM or RTM, hold the ejector latches in the open position and slide the module all the way into the shelf, making sure it makes a solid connection with the backplane and the EMC gasket forms a tight seal. When the ejector latches reach the latch rail on the shelf, close both ejector latches and tighten the thumbscrews.

   When an AMC, RTM, or CPM is installed in a shelf with power applied, the blue hot swap LED flashes until the module is active, then turns off.

   Important: If the removed CPM will not be replaced with another module, install an airflow management filler designed for the slot to maintain proper cooling and airflow through the shelf for the remaining modules.

   For more information on installing a CPM, see the *ATCA-4500 Compute Processing Module Installation Guide.*
8. Remove the grounding wrist strap when you are done handling the module.

Overview of firmware updates

Table 23 summarizes the CPM's programmable devices and the content that can be upgraded.

Table 23. Programmable devices and upgradeable content

Programmable device	Upgradeable content	Copies to upgrade	Run upgrade commands on
SPI flash	BIOS	2	CPM's CPU
	BIOS boot block	2	CPM's CPU
IPMC	IPMI application	2	CPM's CPU or remote CPU
	IPMI boot	1	CPM's CPU or remote CPU
FPGAs and CPLDs	IPMC FPGA	1	CPM's CPU or remote CPU
	CPU complex FPGA	1	CPM's CPU or remote CPU
	COMux CPLD	1	CPM's CPU or remote CPU
Ethernet EEPROMs	Base Ethernet EEPROM	1	CPM's CPU
	Fabric Ethernet EEPROM	1	CPM's CPU
	Front/rear Ethernet EEPROM	1	CPM's CPU
IPMC EEPROM	FRU records	1	CPM's CPU or remote CPU

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In addition, any upgradeable content for a compatible Promentum RTM may be included in the same firmware bundle and upgraded with the CPM. See the RTM reference manual for a list of its programmable devices.

All upgrades can be performed from the CPM's local CPU:

- Through a serial console that is directly connected to the CPM or RTM serial port.
- Through a remote serial console as described in *Serial-over-LAN* on page 57.
- By a remote login to the CPM over Ethernet. The session is lost when the CPM reboots. The BIOS setup menus cannot be accessed and the bootup messages cannot be viewed.

Upgrades of the IPMC, FPGAs, and IPMC EEPROM can alternatively be performed from a remote computer's CPU:

- By specifying the Shelf Manager IP address and the CPM's IPMB address in the upgrade commands.
- By specifying the CPM's Base interface IP address in the upgrade commands. This method is available when access to the IPMC has been configured as described in *IPMI-over-LAN* on page 54.

Instructions for upgrading all of the components are included with the upgrade image, which is available from the RadiSys Web site or from RadiSys Technical Support.

General troubleshooting tips

When the CPM does not perform as expected, look for symptoms that might clarify the cause. Performing the following actions can help diagnose the problem:

- Check the state of the LEDs on the CPM and other modules in the platform, especially the power and out of service LEDs.
- Check the events logged in the Shelf Manager's system event log (SEL) or the CPM's local SEL. For information on accessing the SEL, see *Accessing the SEL* on page 63.
- Check temperatures on the CPM. If the RadiSys Shelf Manager is used, see the troubleshooting information in the *Shelf Management Software Reference* for details on how to perform these queries.
- Verify the IP address and the subnet mask assignment. See the *Software Guide for Management Processors and General Purpose Computing Processors* for details on verifying these assignments.

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Symptoms and recommended actions

This table lists possible troubleshooting scenarios. Look through the listed symptoms to see if any apply to your situation and follow the recommended actions for the applicable symptoms. When an action reveals the cause of the problem, resolve the problem as indicated.

Table 24. Troubleshooting actions based on symptoms

Symptom	Recommendation

The power LED on the CPM is not lit.	▪ Make sure the CPM is completely inserted and the hot swap latch is engaged.
	▪ Verify that other modules in the shelf are powered. If not, check the power to the shelf.
	▪ Inspect the rear connectors for damage. If they show no sign of damage, try the following:
	  ▪ carefully insert the CPM into a different slot
	  ▪ carefully insert a different CPM in the original slot
	WARNING! Do not force the insertion of the CPM. If insertion is not easy, the pins on the backplane connector may be damaged, which could potentially damage the rear connectors on the CPM.
	▪ Verify the CPM is in the M4 hot swap state (active state). (See the *Shelf Management Software Reference* for more information on hot swap states.)
	▪ Check to see if the software installed on the CPM is communicating with the platform's Shelf Manager or whether the CPM is waiting for an external Shelf Manager to enable it.

The CPM or another module overheats.	▪ Verify that a generic front panel is not installed in the shelf. Instead, empty slots must have air management filler panels designed for the shelf's slots installed to properly maintain airflow and emissions. ▪ Check temperatures at the air intake on the overheating module and at the platform's air exhaust. Use the information to determine whether the overheating may be caused by warm facility air, a module failure, or a failed fan module. If the RadiSys Shelf Manager is used, see the troubleshooting information in the *Shelf Management Software Reference* for details on how to perform these queries. ▪ Try moving the module to a different slot to see if that resolves the overheating. ▪ Verify there is clearance of at least two inches between the side of the shelf and the side of the rack cabinet. ▪ Check the shelf's air filter for obstructions and dirt.
Sensors generate alarms or events	See the troubleshooting recommendations under *Sensor alarm troubleshooting* on page 97.
The CPM does not work correctly.	Check the Shelf Manager's system event log for significant events related to the CPM. In particular, verify that the CPM worked correctly when it was installed, and look for any events since then that would explain the changes. If the log information does not reveal useful events, remove the CPM and install it in a different slot. If possible, install another CPM of the same kind in the original slot to help determine whether the CPM is defective.
The OOS LED blinks when the CPM attempts to power up.	Neither IPMC application image is valid. Upgrade both IPMC application images using the upgrade instructions supplied with the Promentum software distribution.
Intermittently, the CPM experiences random data errors.	Verify that the platform's frame-ground connection is properly connected to a high-quality earth-ground connection. Check for electrical noise at the backplane power connections and at the power entry module power inputs. Consider the possibility of a malfunctioning CPM causing electrical noise on backplane connections.

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Table 24. Troubleshooting actions based on symptoms (Continued)

Symptom	Recommendation
POST failures or other bootup errors appear on the serial console or in the system event log.	For definitions of the error or event codes, see *SEL event codes* on page 64.
The login prompt does not appear after BIOS has booted.	▪ Verify the serial cable is plugged into both the CPM and the system with the serial connection. ▪ Verify the CPM is inserted into one of the shelf's node slots. ▪ Verify the terminal emulation application is set to 115200 bps, no parity, 8 data bits, 1 stop bit, with no flow control. ▪ Verify the default Linux port speed has not been changed in the */boot/grub/grub.conf* or */etc/inittab* file.
Message: Operating system not found.	▪ Make sure an operating system is present on the selected boot media. ▪ Verify the correct device is first in the list in the BIOS boot menu. ▪ Verify that an appropriate network link is available between the CPM and the network boot device.

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Environmental specifications

RadiSys does not provide environmental certification testing because any meaningful emissions agency certification must include the entire system. Thus, the CPM is designed and tested to pass the environmental specifications noted below, but is not certified.

WARNING! This product contains static-sensitive components and should be handled with care. Failure to employ adequate anti-static measures can cause irreparable damage to components.

The operating environment must provide sufficient airflow across the CPM to keep it within its temperature specification.

Table 25. Environmental specifications

Characteristic	State	Value
Temperature (ambient)	Operating	+5° C to +40° C 30° C/hr rate of change
	Short term operating[a]	–5° C to +55° C 30° C/hr rate of change
	Storage	–40° C to +70° C Rate of change: ▪ 23° C to –40° C at 30° C/hr ▪ –40° C to 23° C at 13° C/min ▪ +23° C to +70° C at 30° C/hr ▪ +70° C to +23° C at 10° C/min
Relative humidity	Operating	5% to 85% RH non-condensing
	Short term operating[a]	5% to 90%, RH non-condensing at +30°C but not to exceed 0.024 kg water per kg dry air.
	Storage	5% to 90%, RH non-condensing at +40°C but not to exceed 0.024 kg water per kg dry air.
	Short term storage[a]	5% to 95%, RH non-condensing at +40°C but not to exceed 0.024 kg water per kg dry air.
Altitude	Operating	Up to 1800 meters (5,905 feet), +55°C > 1800 meters up to 4000 meters (13,123 feet), derated linearly 1°C per 305 meters from 1800-4000 meters

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Table 25. Environmental specifications (Continued)

Characteristic	State	Value
Shock (drop)	Unpacked Free fall, corners and edges	0 to < 10 kg = 100 mm drop 10 to < 25 kg = 75 mm drop
	Packaged (Unpalletized) Free fall, corners and edges	0 to < 10 kg = 750 mm drop 10 to < 25 kg = 600 mm drop
	Palletized	300 mm free fall drop
Vibration[b]	Operating	0.1g, 5 to 100 Hz and back, 0.1 octave/min sine sweep[b]
	Transportation (packaged)	0.5g, 5 to 50 Hz and back, 0.1 octave/min sine sweep[b] 3.0g, 50 to 500 Hz and back, 0.25 octave/min sine sweep[b]
Seismic	Operating	Per Zone 4 test method, GR-63-CORE

[a] "Short term" is defined as 96 hours maximum with no more than 15 events or 360 hours within one year.

[b] In each direction, for each of three mutually perpendicular axes.

Safety specifications

The safety specifications are measured under laboratory ambient temperature and humidity (approximately 25° C and humidity between 30% and 50%). Testing was performed in partnership with a Nationally Recognized Testing Laboratory (NRTL) accredited to provide the required certifications.

Table 26. Safety specifications

Characteristic	Certification	Standard and test criteria
Product Safety–US	Accessory Listing	UL 60950-1 "Safety for Information Technology Equipment"
Product Safety–Canada	Approval	CSA 22.2 #60950-1 "Safety for Information Technology Equipment"
Product Safety–EU	Conformance with the Low Voltage Directive	EN 60950-1 "Safety for Information Technology Equipment"
Product Safety–Other	CB Report	IEC 60950-1 "Safety for Information Technology Equipment"

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Mechanical specifications

Table 27. Mechanical dimensions

Characteristic		Value
PCB board	Dimensions	322.25 mm x 280.0 mm +0, –0.3 mm (12.687" x 11.023" +0.0, –0.012")
	Board thickness	2.156 mm ±0.2 mm (0.0849" ± 0.008")
CPM with covers	Thickness	30.48 mm (1.5")
	Weight	6.6 lbs (3 kg)

Electromagnetic compatibility (EMC)

The ESD, EMC, and Immunity specifications are measured with ambient temperature between 20° C and 30° C and relative humidity between 30% and 50%.

Table 28. Electromagnetic compatibility (EMC)

	Characteristic	State	Standard and criteria
Emissions	Radiated emissions	Operating	FCC Part 15, Class A requirement for chassis/system level, Class A with 6db margin objective for blade EN 55022: 2006, Class A requirement for chassis/system level, Class A with 6db margin objective for blade
	Conducted emissions	Operating	FCC Part 15, Class A with 6db margin EN 55022: 2006, Class A with 6db margin
Immunity	ESD	Operating	EN 61000-4-2 8 KV direct contact, performance criteria B 15 KV air discharge, performance criteria C
	Radiated	Operating	EN 61000-4-3 10 V/m, 30 MHz–10 GHz, 80% AM Performance criteria A
	Fast transient/burst	Operating	EN 61000-4-4 0.5 kV, 5/50 ns, 5 kHz repetition frequency Performance criteria B
	Surge voltages	Operating	EN 61000-4-5 Data ports: 1 kV, 1.2/50 µs or 8/20 µs DC power port: 0.5 kV, 1.2/50 µs or 8/20 µs Performance criteria B
	Conducted	Operating	EN 61000-4-6 0.15–80 MHz, 3 V, 80% AM Performance criteria A
	Magnetic field immunity	Operating	EN 61000-4-8 50 Hz / 1 A/m Performance criteria A

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Power consumption

Table 29. ATCA-4500 power consumption

Product	Typical power consumption measured at 25° C	Maximum power consumption measured at 55° C
CPM with SAS drive and RTM installed	85 W	163 W
CPM with AMC and RTM installed	116 W	185 W

Table 30. AMC and RTM power limitations

Product	Maximum
AMC	20 W
RTM	25 W

Mean time between failures (MTBF)

- Calculation Type: MTBF/FIT rate
- Standard: Telcordia Standard SR-332 Issue 2
- Methods: Method I, Case III, Quality Level II

The calculation results in Table 31 were generated using the references and assumptions listed. This specification and its associated calculations supersede all other released mean time between failures (MTBF) and failure in time (FIT) calculations with earlier dates. The reported failure rates do not represent catastrophic failure.

Table 31. Reliability estimate data[a]

MTBF	Failure rate (FIT)
149,000 hours	6711 per 10^9 hours

[a] Calculations based on the blade only; does not include DIMMs or AMC.

Environmental assumptions

- Failure rates are based on a 35° C ambient temperature.
- Applied component stress levels are 50% (voltage, current, and/or power).
- Ground, fixed, controlled environment with an environmental adjustment factor equal to 1.0.

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General assumptions

- Component failure rates are constant.
- Board-to-system interconnects are included within estimates.
- Non-electrical components (screws, mechanical latches, labels, covers, etc.) are not included in estimates.

General notes

- Method I, Case I = Based on parts count. Equipment failure is estimated by totaling device failures rates and quantities used.
- Quality Level II = Devices purchased to specifications, qualified devices, vendor lot-to-lot controls for QLs and DPMs.

Where available, direct component supplier predictions or actual FIT rates have been used.

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Supported IPMI commands

Table 32 lists the supported IPMI commands.

Table 32. Supported IPMI commands

Message commands	NetFn	Command
Get Device ID	App (0x06)	0x01
Cold Reset	App (0x06)	0x02
Warm Reset	App (0x06)	0x03
Get Self Test Results	App (0x06)	0x04
Set ACPI Power State	App (0x06)	0x06
Broadcast "Get Device ID"	App (0x06)	0x01
Reset Watchdog Timer	App (0x06)	0x22
Set Watchdog Timer	App (0x06)	0x24
Get Watchdog Timer	App (0x06)	0x25
Set BMC Global Enables	App (0x06)	0x2E
Get BMC Global Enables	App (0x06)	0x2F
Clear Message Flags	App (0x06)	0x30
Get Message Flags	App (0x06)	0x31
Get Message	App (0x06)	0x33
Send Message	App (0x06)	0x34
Get Channel Authentication Capabilities	App (0x06)	0x38
Get Session Challenge	App (0x06)	0x39
Activate Session	App (0x06)	0x3A
Set Session Privilege Level	App (0x06)	0x3B
Close Session	App (0x06)	0x3C
Get Session Info	App (0x06)	0x3D
Get AuthCode	App (0x06)	0x3F
Set Channel Access	App (0x06)	0x40
Get Channel Access	App (0x06)	0x41
Get Channel Info	App (0x06)	0x42
Set User Access	App (0x06)	0x43
Get User Access	App (0x06)	0x44
Set User Name	App (0x06)	0x45
Get User Name	App (0x06)	0x46
Set User Password	App (0x06)	0x47

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Table 32. Supported IPMI commands (continued)

Message commands	NetFn	Command
Activate Payload	App (0x06)	0x48
Deactivate Payload	App (0x06)	0x49
Get Channel Payload Support	App (0x06)	0x4E
Set Event Receiver	S/E (0x04)	0x00
Get Event Receiver	S/E (0x04)	0x01
Platform Event (a.k.a "Event Message")	S/E (0x04)	0x02
Get Device SDR Info	S/E (0x04)	0x20
Get Device SDR	S/E (0x04)	0x21
Reserve Device SDR Repository	S/E (0x04)	0x22
Set Sensor Hysteresis	S/E (0x04)	0x24
Get Sensor Hysteresis	S/E (0x04)	0x25
Set Sensor Threshold	S/E (0x04)	0x26
Get Sensor Threshold	S/E (0x04)	0x27
Set Sensor Event Enable	S/E (0x04)	0x28
Get Sensor Event Enable	S/E (0x04)	0x29
Get Sensor Reading	S/E (0x04)	0x2D
Get FRU Inventory Area Info	Storage (0x0A)	0x10
Read FRU Data	Storage (0x0A)	0x11
Write FRU Data	Storage (0x0A)	0x12
Get SDR Repository Info	Storage (0x0A)	0x20
Reserve SDR Repository	Storage (0x0A)	0x22
Get SDR	Storage (0x0A)	0x23
Get SEL Info	Storage (0x0A)	0x40
Get SEL Entry	Storage (0x0A)	0x43
Add SEL Entry	Storage (0x0A)	0x44
Partial Add SEL Entry	Storage (0x0A)	0x45
Clear SEL	Storage (0x0A)	0x47
Get SEL Time	Storage (0x0A)	0x48
Set SEL Time	Storage (0x0A)	0x49
Set LAN Configuration Parameters	Transport (0x0C)	0x01
Get LAN Configuration Parameters	Transport (0x0C)	0x02
Get Address Info	PICMG (0x2C)	0x01
Get PICMG Properties	PICMG (0x2C)	0x00
FRU Control	PICMG (0x2C)	0x04
Get FRU LED Properties	PICMG (0x2C)	0x05
Get LED Color Capabilities	PICMG (0x2C)	0x06
Set FRU LED State	PICMG (0x2C)	0x07
Get FRU LED State	PICMG (0x2C)	0x08
Set IPMB State	PICMG (0x2C)	0x09

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Table 32. Supported IPMI commands (continued)

Message commands	NetFn	Command
Set FRU Activation Policy	PICMG (0x2C)	0x0A
Get FRU Activation Policy	PICMG (0x2C)	0x0B
Set FRU Activation	PICMG (0x2C)	0x0C
Get Device Locator Record ID	PICMG (0x2C)	0x0D
Set Port State	PICMG (0x2C)	0x0E
Get Port State	PICMG (0x2C)	0x0F
Compute Power Properties	PICMG (0x2C)	0x10
Set Power Level	PICMG (0x2C)	0x11
Get Power Level	PICMG (0x2C)	0x12
Bused Resource	PICMG (0x2C)	0x17
Set AMC Port State	PICMG (0x2C)	0x19
Get AMC Port State	PICMG (0x2C)	0x1A
Set Clock State	PICMG (0x2C)	0x2C
Get Clock State	PICMG (0x2C)	0x2D
Get Target Upgrade Capabilities	PICMG (0x2C)	0x2E
Get Component Properties	PICMG (0x2C)	0x2F
Abort Firmware Upgrade	PICMG (0x2C)	0x30
Initiate Upgrade Action	PICMG (0x2C)	0x31
Upload Firmware Block	PICMG (0x2C)	0x32
Finish Firmware Upload	PICMG (0x2C)	0x33
Get Upgrade Status	PICMG (0x2C)	0x34
Activate Firmware	PICMG (0x2C)	0x35
Query Self Test Results	PICMG (0x2C)	0x36
Query Rollback Status	PICMG (0x2C)	0x37
Initiate Manual Rollback	PICMG (0x2C)	0x38
Restore Factory Defaults[1]	RadiSys OEM (0x30)	0x05
Disable CFD[1]	RadiSys OEM (0x30)	0xE7
Set WDT Reset Type[1]	RadiSys OEM (0x30)	0xA8
Switch Active Boot Flash[1]	RadiSys OEM (0x30)	0xA9
Get Active Boot Flash[1]	RadiSys OEM (0x30)	0xAA
Set Control State (for debug only)[1]	RadiSys OEM (0x30)	0x20
Get Control State (for debug only)[1]	RadiSys OEM (0x30)	0x21

[1] See *OEM command descriptions* on page 84.

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OEM command descriptions

Special commands are available to facilitate CPM-specific functionality. Descriptions of each command and their parameters are listed in this section.

Restore Factory Defaults

Restores the factory default configuration and threshold parameters for onboard sensors. No data byte is required.

Data field	Byte	N/A	N/A
Response field	Byte	1	Completion code

Set Control State (for debug only)

Overrides the current firmware setting of the control pin. Use only for debug situations.

Data field	Byte	1	FRU ID;
	Byte	2	Control number
	Byte	3	Control state: 0x00 = de-assert; 0x01 = assert; 0x02 = pulse de-assert; 0x03 = pulse assert
Response field	Byte	1	Completion code

Get Control State (for debug only)

Returns the current state of a control pin Use only for debug situations.

Data field	Byte	1	FRU ID
	Byte	2	Control number
Response field	Byte	1	Completion code
	Byte	2	Control state: 0x00 = de-assert; 0x01 = assert

Disable CFD

Indicates to the IPMC that the CFD watchdog timer needs to be disabled. No data byte is required.

Data field	Byte	N/A	N/A
Response field	Byte	1	Completion code

Set WDT Reset Type

Allows a BMC watchdog timeout configured for "Hard Reset" to cause a warm reset or a cold reset.

Data field	Byte	1	Reset Type Configuration: 1: Warm Reset; 0: Cold Reset
Response field	Byte	1	Completion code

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Switch Active Boot Flash

Sets the current boot flash and can cause a cold reset to the x86 processor complex portion of the board if the appropriate bits in the command data are set. The command can also set the primary boot flash, which is selected during a power-on reset of the blade.

Data field	Byte	1	Bit 7 = Sets the primary boot flash - 0b (do not set), 1b (Set primary flash to flash selected by bit 0) Bit 6 = Selects whether or not a reset will occur as a result of calling this command - 0b (causes reset), 1b (Does not cause reset) Bits 5:1 = Reserved Bit 0 (boot flash) = 0b (boot flash 0), 1b (boot flash 1)
Response field	Byte	1	Completion code

Get Active Boot Flash

Gets the current boot flash and the primary boot flash from the H8 IPMI firmware.

Note: This command should be used only if the active SPM is in state M7, or if only one SPM is installed. Hardware failure could occur if shared resources are linked across two active SPMs.

Data field	Byte	1	FRU ID
Response field	Byte	1	Completion code
		2	Currently selected boot flash
		3	Primary boot flash

RTM Reset Button

Instructs the H8 IPMI firmware to perform a cold reset.

Data field	Byte	1	Radisys IANA PEN0: F1h
	Byte	2	Radisys IANA PEN1: 10h
	Byte	3	Radisys IANA PEN2: 00h
Response field	Byte	1	Completion code
		2	Radisys IANA PEN0: F1h
		3	Radisys IANA PEN1: 10h
		4	Radisys IANA PEN2: 00h

Set Payload Status

Informs the H8 IPMI firmware about the current payload processor status. The IPMI firmware uses the reported information to initiate its internal processes, which are dependent on resources controllable by the onboard x86 processor complex.

Boot phases 1 and 4 specified in status byte 1 report respectively the commencement and completion of the onboard x86 processor complex boot-up processes. The remaining boot phases may optionally report other milestones in the payload boot-up process.

When boot phase 1 is received, the IPMI firmware initializes all appropriate control signals to yield access of all hardware shared resources to the onboard x86 processor complex. When boot phase 4 is received, the IPMI firmware reconfigures the appropriate control signals to

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regain access of all hardware shared resources and commences the applicable management functions.

Data field	Byte 1	Radisys IANA PEN0: F1h
	Byte 2	Radisys IANA PEN1: 10h
	Byte 3	Radisys IANA PEN2: 00h
	Byte 4	Command Version: hard coded to 0x00
	Byte 5	Status Byte 1 Bits 7:4 = Reserved Bit 3 (Boot Phase 4) = 0b (Not Complete) 1b (Complete) Bit 2 (Boot Phase 3) = 0b (Not Complete) 1b (Complete) Bit 1 (Boot Phase 2) = 0b (Not Complete) 1b (Complete) Bit 0 (Boot Phase 1) = 0b (Not Complete) 1b (Complete)
	Byte 6	Status Byte 2 Bits 7:0 = Reserved
Response field	Byte 1	Completion code
	2	Radisys IANA PEN0: F1h
	3	Radisys IANA PEN1: 10h
	4	Radisys IANA PEN2: 00h

Get Payload Status (debug only)

Returns the H8 IPMI firmware acknowledgement of the payload processor status. The BIOS/OS uses this command to check if the IPMI firmware finished the internal processes for the x86 processor complex boot phase specified in a sent `Set Payload status` command.

The IPMI firmware reports boot phase 1 is complete after it has initialized all appropriate control signals to yield access of all hardware shared resources to the onboard x86 processor complex. It reports boot phase 4 is complete after reconfiguring the appropriate control signals to regain access of all hardware shared resources and commencing the applicable management functions.

Data field	Byte 1	Radisys IANA PEN0: F1h
	Byte 2	Radisys IANA PEN1: 10h
	Byte 3	Radisys IANA PEN2: 00h
	Byte 4	Command Version: hard coded to 0x00
Response field	Byte 1	Completion code
	2	Radisys IANA PEN0: F1h
	3	Radisys IANA PEN1: 10h
	4	Radisys IANA PEN2: 00h
	5	Command Version
	6	Status Byte 1 Bits 7:4 = Reserved Bit 3 (Boot Phase 4) = 0b (Not Complete) 1b (Complete) Bit 2 (Boot Phase 3) = 0b (Not Complete) 1b (Complete) Bit 1 (Boot Phase 2) = 0b (Not Complete) 1b (Complete) Bit 0 (Boot Phase 1) = 0b (Not Complete) 1b (Complete)
	Byte 7	Status Byte 2 Bits 7:0 = Reserved

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Managed sensors

On the CPM, the IPMC sensors monitor voltages, temperatures, control signals, and status events. For functional information, refer to *IPMC description* on page 44. The sensors are described in Table 34.

Types of sensors

The CPM implements the following types of sensors.

- **Discrete** — A discrete sensor can have up to 16 bitmapped states, with one state as true.
- **Digital** — A digital sensor has two possible states, only one of which can be active at any given time. For example, a digital sensor monitoring the power may indicate whether the power is good or not good.
- **OEM** — An OEM sensor has its states defined by the manufacturer. The reading types of these sensors are sometimes defined as "sensor-specific."
- **Threshold** — A threshold sensor has a range of 256 values, which represent measurements on the PPM and its FRUs. Temperature, voltage, current, and fan speed sensors are examples of threshold sensors. Table 33 lists the possible threshold types, which are used in Table 34 on page 88.

Table 33. Threshold types

Threshold type	Description
UNR	Upper non-recoverable thresholds generate a critical alarm on the high side.
UC	Upper critical thresholds generate a major alarm on the high side.
UNC	Upper non-critical thresholds generate a minor alarm on the high side.
LNC	Lower non-critical thresholds generate a minor alarm on the low side.
LC	Lower critical thresholds generate a major alarm on the low side.
LNR	Lower non-recoverable thresholds typically generate a critical alarm on the low side.

Note: If the CPM exceeds one of the UNR thresholds (Table 34 on page 88), the Shelf Manager generates a critical alarm and shuts down the CPM. See the *Software Guide* for details.

List of sensors

Table 34 provides details about the sensors managed by the IPMC. All sensors generate events unless noted otherwise in the footnotes below the table.

Note: The digital and discrete sensor readings reported by the active Shelf Manager may differ from the raw values reported in Table 34.

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Table 34. Managed sensors

No.	Name	Type	Reading type	Normal reading	Alarm level	Notes
0	ATCA FRU Hotswap	ATCA FRU Hotswap	Sensor-specific	0x00–0x07	N/A	Returns the ATCA M0 through M7 hot swap states for the front blade
1	AMC FRU Hotswap	ATCA FRU Hotswap	Sensor-specific	0x00–0x07	N/A	Returns the ATCA M0 through M7 hot swap states for the AMC.
2	RTM FRU Hotswap	ATCA FRU Hotswap	Sensor-specific	0x00–0x07	N/A	Returns the M0 through M7 ATCA hot swap states for the RTM.
3	Version Change	Version Change (IPMI 2.0)	Sensor-specific	0x00–0x07	N/A	Firmware or software change detected with associated entity. Informational. Success or failure not implied. Reading 0x00 indicates no version change; 0x01 through 0x07 indicate version change. Software or firmware change detected with associated entity was successful. (de-assertion event means 'unsuccessful') Event Data 2 (for both event offsets 1h, 2h): 02h management controller firmware revision 05h management controller IPMI version 06h management controller auxiliary firmware ID 07h management controller firmware boot block
4	Ejector Closed	Slot or Connector	Digital	1	N/A	0: Ejector latch is open Fault Status asserted 1: Ejector latch is closed Identify Status asserted
5	RTM Present	Slot or Connector	Digital	0 or 1	N/A	0: RTM is not present 1: RTM is present Asserted at module insertion (M0 - M1)
6	AMC Present	Slot or Connector	Digital	0 or 1	N/A	0: AMC is not present 1: AMC is present
7	SPD DIMM A0 Temp	Temp	Threshold	25	Major, Minor, Critical	This sensor measures temperature in °C. Default thresholds: LNR –10.0, LC –5.0, LNC 0.0, UNC 72.0, UC 80.0, UNR 95.0
8	SPD DIMM A1 Temp	Temp	Threshold	25	Major, Minor, Critical	This sensor measures temperature in °C. Default thresholds: LNR –10.0, LC –5.0, LNC 0.0, UNC 72.0, UC 80.0, UNR 95.0
9	SPD DIMM A2 Temp	Temp	Threshold	25	Major, Minor, Critical	This sensor measures temperature in °C. Default thresholds: LNR –10.0, LC –5.0, LNC 0.0, UNC 72.0, UC 80.0, UNR 95.0

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Table 34. Managed sensors (continued)

No.	Name	Type	Reading type	Normal reading	Alarm level	Notes
10	SPD DIMM B0 Temp	Temp	Threshold	25	Major, Minor, Critical	This sensor measures temperature in °C. Default thresholds LNR: −10.0 | LC: −5.0 | LNC: 0.0 | UNC: 72.0 | UC: 80.0 | UNR: 95.0
11	SPD DIMM B1 Temp	Temp	Threshold	25	Major, Minor, Critical	This sensor measures temperature in °C. Default thresholds LNR: −10.0 | LC: −5.0 | LNC: 0.0 | UNC: 72.0 | UC: 80.0 | UNR: 95.0
12	SPD DIMM B2 Temp	Temp	Threshold	25	Major, Minor, Critical	This sensor measures temperature in °C. Default thresholds LNR: −10.0 | LC: −5.0 | LNC: 0.0 | UNC: 72.0 | UC: 80.0 | UNR: 95.0
13	SPD DIMM C0 Temp	Temp	Threshold	25	Major, Minor, Critical	This sensor measures temperature in °C. Default thresholds LNR: −10.0 | LC: −5.0 | LNC: 0.0 | UNC: 72.0 | UC: 80.0 | UNR: 95.0
14	SPD DIMM C1 Temp	Temp	Threshold	25	Major, Minor, Critical	This sensor measures temperature in °C. Default thresholds LNR: −10.0 | LC: −5.0 | LNC: 0.0 | UNC: 72.0 | UC: 80.0 | UNR: 95.0
15	AMC Inlet Temp	Temp	Threshold	25	Major, Minor, Critical	This sensor measures temperature in °C. ***Note:*** This sensor has events disabled, so no event is generated if a reading crosses a threshold. Default thresholds LNR: −10.4 | LC: −4.8 | LNC: 0.0 | UNC: 64.8 | UC: 72.0 | UNR: 80.0
16	IOH Die Temp	Temp	Threshold	25	Major, Minor, Critical	This sensor measures temperature in unspecified units Default thresholds LNR: N/A | LC: N/A | LNC: N/A | UNC: -20.0 | UC: -13.0 | UNR: -1.0
17	CPU Core DTS (Digital Thermal Sensor)	Temp	Threshold	25	Major, Minor, Critical	This sensor measures temperature in unspecified units. Default thresholds LNR: N/A | LC: N/A | LNC: N/A | UNC: -20.0 | UC: -13.0 | UNR: -1.0
18	CPU ThermTrip[1]	Processor	Digital	0 or 1	N/A	0: CPU ThermTrip not asserted 1: CPU ThermTrip asserted

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Table 34. Managed sensors (continued)

No.	Name	Type	Reading type	Normal reading	Alarm level	Notes
19	CPU ProcHot[1]	Temp	Threshold	0	Major, Minor, Critical	This sensor monitors ProcHot and, when it is asserted, reports a reading of 90.
						Default thresholds
						LNR: −15.0 | LC: −10.0 | LNC: −5.0 | UNC: 65.0 | UC: 72.0 | UNR: 100.0
20	−48V Absent A	Power Supply	Digital	0	N/A	0: Power Supply A Presence detected | 1: Power Supply A Failure detected
21	−48V Absent B	Power Supply	Digital	0	N/A	0: Power Supply B Presence detected | 1: Power Supply B Failure detected
22	−48V Fuse Fault	Power Supply	Digital	0	N/A	0: Both A & B fuses OK Presence detected | 1: Either A or B fuse blown Failure detected
23	System PwrFail[2]	Power Supply	Digital	0 or 1	N/A	0: Power is good | 1: Power fail detected
24	VCORE	Voltage	Threshold	1.04 VID=0.75 ~ 1.35[3]	Major, Minor, Critical	This sensor measures voltage in Volts. Hysteresis: ±0.02
						Default thresholds
						LNR: 0.00[4] | LC: 0.72 | LNC: 0.76 | UNC: 1.31 | UC: 1.38 | UNR: 1.44
25	+12V	Voltage	Threshold	12.00	Major, Minor, Critical	This sensor measures voltage in Volts.
						Default thresholds
						LNR: 0.00 | LC: 10.8 | LNC: 11.4 | UNC: 12.6 | UC: 13.2 | UNR: 13.8
26	+5V	Voltage	Threshold	5.00	Major, Minor, Critical	This sensor measures voltage in Volts. Hysteresis: ±0.10
						Default thresholds
						LNR: 0.00 | LC: 4.5 | LNC: 4.76 | UNC: 5.25 | UC: 5.49 | UNR: 5.75
27	+5V_Standby	Voltage	Threshold	5.00	Major, Minor, Critical	This sensor measures voltage in Volts. Hysteresis: ±0.10
						Default thresholds
						LNR: 0.00 | LC: 4.5 | LNC: 4.75 | UNC: 5.25 | UC: 5.5 | UNR: 5.75
28	+3.3V_IPMI	Voltage	Threshold	3.30	Major, Minor, Critical	This sensor measures voltage in Volts. Hysteresis: ±0.10
						Default thresholds
						LNR: 0.00 | LC: 2.97 | LNC: 3.14 | UNC: 3.47 | UC: 3.63 | UNR: 3.8

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Table 34. Managed sensors (continued)

No.	Name	Type	Reading type	Normal reading	Alarm level	Notes					
29	+3.3V	Voltage	Threshold	3.30	Major, Minor, Critical	This sensor measures voltage in Volts.					
						Default thresholds					
						LNR	LC	LNC	UNC	UC	UNR
						0.00	2.97	3.14	3.47	3.63	3.8
30	+1.8V	Voltage	Threshold	1.80	Major, Minor, Critical	This sensor measures voltage in Volts.					
						Default thresholds					
						LNR	LC	LNC	UNC	UC	UNR
						0.00	1.62	1.71	1.89	1.98	2.07
31	+1.8V_CPU	Voltage	Threshold	1.80	Major, Minor, Critical	This sensor measures voltage in Volts.					
						Default thresholds					
						LNR	LC	LNC	UNC	UC	UNR
						0.00	1.62	1.71	1.89	1.98	2.07
32	+1.8V_BASE	Voltage	Threshold	1.80	Major, Minor, Critical	This sensor measures voltage in Volts.					
						Default thresholds					
						LNR	LC	LNC	UNC	UC	UNR
						0.00	1.62	1.71	1.89	1.98	2.07
33	+1.8V_FRONT	Voltage	Threshold	1.80	Major, Minor, Critical	This sensor measures voltage in Volts.					
						Default thresholds					
						LNR	LC	LNC	UNC	UC	UNR
						0.00	1.62	1.71	1.89	1.98	2.07
34	+1.5V	Voltage	Threshold	1.50	Major, Minor, Critical	This sensor measures voltage in Volts.					
						Default thresholds					
						LNR	LC	LNC	UNC	UC	UNR
						0.00	1.35	1.43	1.58	1.65	1.73
35	+1.5V_DDR3	Voltage	Threshold	1.50	Major, Minor, Critical	This sensor measures voltage in Volts.					
						Default thresholds					
						LNR	LC	LNC	UNC	UC	UNR
						0.00	1.35	1.43	1.58	1.65	1.73
36	+1.2V	Voltage	Threshold	1.20	Major, Minor, Critical	This sensor measures voltage in Volts.					
						Default thresholds					
						LNR	LC	LNC	UNC	UC	UNR
						0.00	1.08	1.14	1.26	1.32	1.38
37	+1.1V	Voltage	Threshold	1.10	Major, Minor, Critical	This sensor measures voltage in Volts.					
						Default thresholds					
						LNR	LC	LNC	UNC	UC	UNR
						0.00	0.99	1.05	1.17	1.23	1.29

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Table 34. Managed sensors (continued)

No.	Name	Type	Reading type	Normal reading	Alarm level	Notes
38	+1.1V_VTT	Voltage	Threshold	VID = 1.025 ~ 1.22	Major, Minor, Critical	This sensor measures voltage in Volts. Default thresholds LNR: 0.00 | LC: 0.90 | LNC: 0.96 | UNC: 1.28 | UC: 1.34 | UNR: 1.37
39	+1.0V_BASE	Voltage	Threshold	1.00	Major, Minor, Critical	This sensor measures voltage in Volts. Default thresholds LNR: 0.00 | LC: 0.90 | LNC: 0.95 | UNC: 1.05 | UC: 1.10 | UNR: 1.15
40	+1.0V_FRONT	Voltage	Threshold	1.00	Major, Minor, Critical	This sensor measures voltage in Volts. Default thresholds LNR: 0.00 | LC: 0.90 | LNC: 0.95 | UNC: 1.05 | UC: 1.10 | UNR: 1.15
41	+0.75V_DDR3	Voltage	Threshold	0.75	Major, Minor, Critical	This sensor measures voltage in Volts. Default thresholds LNR: 0.00 | LC: 0.68 | LNC: 0.73 | UNC: 0.79 | UC: 0.83 | UNR: 0.87
42	OEM Payload Reset	Other sensor (0xD4)	Sensor-specific	0x00-0xFF	N/A	See *OEM Payload Reset sensor* on page 95.
43	OEM Active Boot Flash	Other sensor (0x0B)	Sensor-specific	0 or 1	N/A	See *OEM Active Boot Flash sensor* on page 95.
44	BMC Watchdog	Watchdog 2	Sensor-specific	N/A	N/A	Sensor-specific event offset = watchdog action: 0 = Timer expired. Status only (no action, no interrupt). 1 = Payload cold reset. 2 = Payload power down. 3 = Payload power cycle. 4–7 = Reserved. 8 = Pre-timer interrupt.
45	IPMC Watchdog	OEM (0xED for IPMC FPGA WDT)	Digital	N/A (Does not return analog readings)	N/A	Sensor SDR states that this sensor does not return any analog readings (a Get Sensor Reading command directed at this sensor always returns '0' for a reading). However, an "assert" event is logged to the SEL once the IPMC is reset due to the Watchdog

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Table 34. Managed sensors (continued)

No.	Name	Type	Reading type	Normal reading	Alarm level	Notes	
46	ATCA Physical IPMB	ATCA Physical IPMB-0	Sensor-specific	0x00–0xFF	N/A	Bit [7] = IPMB B Override State Bit [6:4] = IPMB B Local Status Bit [3] = IPMB A Override State Bit [2:0] = IPMB A Local Status	
47	ATCA Physical IPMB-L	ATCA Physical IPMB-0	Sensor-specific	0x00–0xFF	N/A	Bit [7:4] = Reserved Bit [3] = IPMB-L Override State Bit [2:0] = IPMB-L Local Status	
48	NMI	Critical interrupt	Digital	0 or 1	N/A	0	1
						Deasserted	Asserted
49	+12V RTM PwrFail	Voltage	Digital	0 or 1	N/A	1	0
						Deasserted	Asserted
50	+3.3V RTM Fail	Voltage	Digital	0 or 1	N/A	1	0
						Deasserted	Asserted
51	+12V AMC PwrFail	Voltage	Digital	0 or 1	N/A	1	0
						Deasserted	Asserted
52	+3.3V AMC Fail	Voltage	Digital	0 or 1	N/A	1	0
						Deasserted	Asserted
53	IOH ThermTrip[1]	Temp	Digital	0 or 1	N/A	0	1
						IOH ThermTrip not asserted	IOH ThermTrip asserted
54	IOH Therm Alert[1]	Temp	Digital	0 or 1	N/A	0	1
						IOH Therm Alert not asserted	IOH Therm Alert asserted
55	DDR Therm T64[1]	Temp	Digital	0 or 1	N/A	0	1
						Therm T64 not asserted	Therm T64 asserted
56	CPU CAT ERR[1]	Processor	Digital	0 or 1	N/A	0	1
						CPU CAT ERR not asserted	CPU CAT ERR asserted
57	AMC PwrFault	Voltage	Digital	0 or 1	N/A	0	1
						AMC PwrFault not asserted	AMC PwrFault asserted
58	RTM PwrFault	Voltage	Digital	0 or 1	N/A	0	1
						RTM PwrFault not asserted	RTM PwrFault asserted
59	AMC PCIe PwrEn	Voltage	Digital	0 or 1	N/A	0	1
						AMC PCIe PwrEn not asserted	AMC PCIe PwrEn asserted
60	RTM PCIe PwrEn	Voltage	Digital	0 or 1	N/A	0	1
						RTM PCIe PwrEn not asserted	RTM PCIe PwrEn asserted

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Table 34. Managed sensors (continued)

No.	Name	Type	Reading type	Normal reading	Alarm level	Notes	
61	ENET Link 0	Slot or Connector	Digital	0 or 1	N/A	0	1
						E0_LINK_LED* not asserted	E0_LINK_LED* asserted
62	ENET Link 1	Slot or Connector	Digital	0 or 1	N/A	0	1
						E1_LINK_LED* not asserted	E1_LINK_LED* asserted
63	ENET Link 2	Slot or Connector	Digital	0 or 1	N/A	0	1
						E2_LINK_LED* not asserted	E2_LINK_LED* asserted
64	ENET Link 3	Slot or Connector	Digital	0 or 1	N/A	0	1
						E3_LINK_LED* not asserted	E3_LINK_LED* asserted
65	ENET Link 4	Slot or Connector	Digital	0 or 1	N/A	0	1
						E4_LINK_LED* not asserted	E4_LINK_LED* asserted
66	ENET Link 5	Slot or Connector	Digital	0 or 1	N/A	0	1
						E5_LINK_LED* not asserted	E5_LINK_LED* asserted
67–254	Open for dynamically added sensors from an AMC and RTM For details on the range of available sensors, see the product documentation for the applicable AMC or RTM.						

1 These sensors are Active Low inputs. The IPMC sees a 0 when these hardware signals are asserted and a 1 when not asserted.

2 System Power Good is the ORing function of all local voltage sources derived from the -48V power supply.

3 VID: Voltage Identifier, the processor communicated with the voltage regulator module (VRM) at start-up via the VID bits to specify the level of required voltage supply.

4 The LNR threshold is not used on the CPM and is set at 0.00 to indicate this state cannot occur. The ADM1066 hardware voltage monitor shuts down the board if any supply voltages drop near or below the LR trip point value.

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OEM sensor details

This section provides details about the OEM managed sensors listed in Table 34 on page 88.

OEM Payload Reset sensor

The OEM Payload Reset sensor (managed sensor 42) indicates the cause of payload resets that occur during standard CPM operation. Each time a payload reset occurs, an event containing the cause of the reset is generated by the CPM.

The logic for the reset sensor is located on the IPMC FPGA, where all reset sources are physically routed. The IPMC FPGA monitors each reset source and toggles an interrupt connected to the IPMC whenever a payload reset is detected. The IPMC learns the reason for the reset by reading a status register on the FPGA. In the event that multiple resets are generated at the same time (the front panel push button is pressed at the same time a FRU control cold reset is issued), the IPMC prioritizes the reset sources for the sake of listing event data. This prioritization is not related in any way to the hardware functionality. The format of the event data generated from the reset sensor is described in Table 35.

Table 35. OEM Payload Reset sensor event data format

Event Data	Data Field
1	[7:6] - 10b = OEM code in byte 2 [5:4] - 10b = OEM code in byte 3 [3:0] - 0000b = No reset has occurred 0001b = Reset occurred
2	The highest priority reset source
3	The second highest priority reset source. If only one reset occurs, this value is set to 0x00.

OEM Active Boot Flash sensor

The OEM Active Boot Flash sensor (managed sensor 43) indicates when the boot flash select signal changes state and why the signal has changed state. The OEM Active Boot Flash sensor reading indicates which bank the IPMC has currently selected. The format of the event data generated from the OEM Active Boot Flash sensor is described in Table 36.

Table 36. OEM Active Boot Flash sensor event data format

Event Data	Data Field
1	[7:6] - 00b = Unspecified in byte 2 [5:4] - 10b = OEM code in byte 3 [3:0] - 00h = Flash bank 0 has been selected 01h = Flash bank 1 has been selected
2	Not used. Set to 00h.
3	The cause of reset. [7:0]: 00h = CFD Timer was initialized 01h = CFD Timeout has occurred 02h = Flash bank switch was externally initiated 03h = No change

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Temperature sensor details

This section describes temperature sensors which require initial configuration support or a handshake mechanism with the X86 processor complex. It also explains the presentations for sensors with reported readings different from other traditional temperature sensors.

SPD DIMM DDR3 temperature sensors

When memory modules containing serial EEPROMs are detected with the thermal sensors and Serial Present Detect (SPD) circuit, the CPM monitors up to eight SPD DIMM DDR3 sensors and reports the sensor measurements in degrees centigrade.

The CPM uses the SMBUS_FREE* signal to arbitrate the memory access with the X86 processor complex through a multiplexer on I^2C bus 3. The IPMC controls the select input to the MUX, but it qualifies its control with a handshake signal from an ICH10R GPIO. When the CPM initially powers up, the I^2C bus 3 DIMM multiplexer is configured to allow the X86 processor complex to have access to the DIMMs. After all SPDs are read, the X86 processor complex asserts SMBUS_FREE* (GPIO) to indicate it is finished. The IPMC selects I^2C bus 3 to access the DIMMs about every 250 ms as part of the round robin sensor scan.

The CPM has individual access to each of these temperature sensors via a series of I^2C addresses ranged between 0x30 and 0x3F for SPD slots A0, A1, A2, B0, B1, B2, and C0, C1.

CPU Core DTS temperature sensor

The CPM acquires the CPU core DTS (digital temperature sensor) reading from the PECI bus using a PECI-to-I^2C translator available at address 0x54 on I^2C bus 2. The PECI reading indicates how far the current CPU temperature is from the internal thermal control circuit activation point where the PROCHOT event is issued.

The CPM presents the CPU core DTS temperature sensor readings as negative units in the range of [0, -128] below the internal thermal throttle temperature.

IOH DIE temperature sensor

The Intel 5520 IOH provides an on-die temperature measurement which can be accessed via the on-die Thermal Sensor Fan-Speed Control Register (IOH TSFSC). This field contains the difference between the die temperature and the maximum permissible die temperature. The register has a resolution of 0.5° C. Hence, a value in the range of 0 to 127 refers to a temperature difference of 0 to 63.5° C lower than the maximum permissible die temperature. A value in the range of 128 to 255 refers to a temperature difference of 64 to 0.5° C above the maximum permissible die temperature. For difference exceeding these limits, the register values are clamped at 63.5° C for the lower range and 64° C for the upper range.

When the CPM first powers up, the X86 processor complex configures and enables the IOH on-die temperature sensor operations. The CPM acquires IOH on-die temperature via address 0xE0 on I^2C bus 2 and present the readings in the range as negative units in the range of [0, -64] below the internal maximum permissible temperature.

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Sensor alarm troubleshooting

Table 37 recommends actions to take when the sensors generate alarms or events.

Table 37. Sensor alarms and recommended actions (Sheet 1 of 15)

Number	Name	Alarm level	Possible errors or faults	Recommendation
0	ATCA FRU Hot Swap	N/A	M7 state	Remove CPM and reinsert to see if problem persists. If problem still persists, then remove CPM and contact customer support.
1	AMC FRU Hot Swap	N/A	M7 state	Remove CPM and reinsert to see if problem persists. If problem still persists, then remove CPM and contact customer support.
2	RTM FRU Hot Swap	N/A	M7 state	Remove CPM and reinsert to see if problem persists. If problem still persists, then remove CPM and contact customer support.
3	Version Change	N/A	Sensor puts an event into the SEL when a change as been detected.	No action required; information only.
4	Ejector Closed	N/A	None	No action required; information only.
5	RTM Present	N/A	None	No action required; information only.
6	AMC Present	N/A	None	No action required; information only.
7	SPD DIMM A0 Temp	Minor temperature high	Temperature over 72°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 80°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 95°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under 0°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -5°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -10°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.

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Table 37. Sensor alarms and recommended actions (Sheet 2 of 15)

Number	Name	Alarm level	Possible errors or faults	Recommendation
8	SPD DIMM A1 Temp	Minor temperature high	Temperature over 72°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 80°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 95°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under 0°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -5°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -10°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
9	SPD DIMM A2 Temp	Minor temperature high	Temperature over 72°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 80°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 95°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under 0°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -5°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -10°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.

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Table 37. Sensor alarms and recommended actions (Sheet 3 of 15)

Number	Name	Alarm level	Possible errors or faults	Recommendation
10	SPD DIMM B0 Temp	Minor temperature high	Temperature over 72°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 80°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 95°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under 0°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -5°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -10°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
11	SPD DIMM B1 Temp	Minor temperature high	Temperature over 72°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 80°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 95°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under 0°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -5°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -10°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.

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Table 37. Sensor alarms and recommended actions (Sheet 4 of 15)

Number	Name	Alarm level	Possible errors or faults	Recommendation
12	SPD DIMM B2 Temp	Minor temperature high	Temperature over 72°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 80°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 95°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under 0°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -5°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -10°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
13	SPD DIMM C0 Temp	Minor temperature high	Temperature over 72°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 80°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 95°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under 0°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -5°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -10°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.

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Table 37. Sensor alarms and recommended actions (Sheet 5 of 15)

Number	Name	Alarm level	Possible errors or faults	Recommendation
14	SPD DIMM C1 Temp	Minor temperature high	Temperature over 72°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 80°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 95°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under 0°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -5°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -10°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
15	AMC Inlet Temp	Minor temperature high	Temperature over 64.8°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 72°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 80°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under 0°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -4.8°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -10.4°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.

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Table 37. Sensor alarms and recommended actions (Sheet 6 of 15)

Number	Name	Alarm level	Possible errors or faults	Recommendation
16	IOH Die Temp	Minor temperature high	Temperature over -20 threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over -13 threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over -1 threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	N/A	N/A
		Major temperature low	N/A	N/A
		Critical temperature low	N/A	N/A
17	CPU Core DTS	Minor temperature high	Temperature over -20 threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over -13 threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over -1 threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	N/A	N/A
		Major temperature low	N/A	N/A
		Critical temperature low	N/A	N/A
18	CPU ThermTrip	N/A	CPM over temperature event	Check other CPU Temp sensors. Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.

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Table 37. Sensor alarms and recommended actions (Sheet 7 of 15)

Number	Name	Alarm level	Possible errors or faults	Recommendation
19	CPU ProcHot	Minor temperature high	Temperature over 65°C threshold.	Monitor to see if the alarm worsens.
		Major temperature high	Temperature over 72°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature high	Temperature over 100°C threshold. Most Shelf Managers shut down the CPM.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Minor temperature low	Temperature under -5°C threshold.	Monitor to see if the alarm worsens.
		Major temperature low	Temperature under -10°C threshold.	Monitor to see if the alarm worsens or is persistent for more than 1 hour. If persistent, remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
		Critical temperature low	Temperature under -15°C threshold.	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
20	-48V Absent A	N/A	Voltage from -48V power source 'A' is not healthy.	Investigate power loss
21	-48V Absent B	N/A	Voltage from -48V power source 'B' is not healthy.	Investigate power loss
22	-48V Fuse Fault	N/A	A -48V fuse is not functioning.	Check the -48V fuses. Contact customer support if a replacement fuse is required.
23	System PwrFail	N/A	Power problem	Monitor to see if the event is repeated. Investigate power loss.
24	VCORE	Minor voltage high	Voltage over 1.31V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.38V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 1.44V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 0.76V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 0.72V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.

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Table 37. Sensor alarms and recommended actions (Sheet 8 of 15)

Number	Name	Alarm level	Possible errors or faults	Recommendation
25	+12V	Minor voltage high	Voltage over 12.6V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 13.2V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 13.8V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 11.4V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 10.8V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
26	+5V	Minor voltage high	Voltage over 5.25V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 5.49V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 5.75V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 4.76V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 4.5V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
27	+5V_Standby	Minor voltage high	Voltage over 5.25V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 5.5V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 5.75V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 4.75V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 4.5V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.

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Table 37. Sensor alarms and recommended actions (Sheet 9 of 15)

Number	Name	Alarm level	Possible errors or faults	Recommendation
28	+3.3V IPMI	Minor voltage high	Voltage over 3.47V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 3.63V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 3.8V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 3.14V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 2.97V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
29	+3.3V	Minor voltage high	Voltage over 3.47V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 3.63V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 3.8V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 3.14V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 2.97V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
30	+1.8V	Minor voltage high	Voltage over 1.89V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.98V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 2.07V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 1.71V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 1.62V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.

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Table 37. Sensor alarms and recommended actions (Sheet 10 of 15)

Number	Name	Alarm level	Possible errors or faults	Recommendation
31	+1.8V_CPU	Minor voltage high	Voltage over 1.89V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.98V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 2.07V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 1.71V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 1.62V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
32	+1.8V_BASE	Minor voltage high	Voltage over 1.89V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.98V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 2.07V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 1.71V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 1.62V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
33	+1.8V_FRONT	Minor voltage high	Voltage over 1.89V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.98V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 2.07V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 1.71V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 1.62V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.

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Table 37. Sensor alarms and recommended actions (Sheet 11 of 15)

Number	Name	Alarm level	Possible errors or faults	Recommendation
34	+1.5V	Minor voltage high	Voltage over 1.58V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.65V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 1.73V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 1.43V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 1.35V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
35	+1.5V_DDR3	Minor voltage high	Voltage over 1.58V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.65V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 1.73V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 1.43V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 1.35V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
36	+1.2V	Minor voltage high	Voltage over 1.26V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.32V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 1.38V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 1.14V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 1.08V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.

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Table 37. Sensor alarms and recommended actions (Sheet 12 of 15)

Number	Name	Alarm level	Possible errors or faults	Recommendation
37	+1.1V	Minor voltage high	Voltage over 1.17V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.23V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 1.29V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 1.05V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 0.99V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
38	+1.1V_VTT	Minor voltage high	Voltage over 1.28V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.34V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 1.37V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 0.96V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 0.90V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
39	+1.0V_BASE	Minor voltage high	Voltage over 1.05V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.10V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 1.15V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 0.95V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 0.90V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.

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Table 37. Sensor alarms and recommended actions (Sheet 13 of 15)

Number	Name	Alarm level	Possible errors or faults	Recommendation
40	+1.0V_FRONT	Minor voltage high	Voltage over 1.05V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 1.10V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 1.15V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 0.95V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 0.90V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
41	0.75V_DDR3	Minor voltage high	Voltage over 0.79V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage high	Voltage over 0.83V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage high	Voltage over 0.87V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
		Minor voltage low	Voltage under 0.73V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm worsens.
		Major voltage low	Voltage under 0.68V threshold; CPM will not go into M4 state.[1]	Monitor to see if the alarm is persistent. If persistent, remove CPM and contact customer support.
		Critical voltage low	Voltage at 0V threshold; CPM will not go into M4 state.[1]	Remove CPM and contact customer support.
42	OEM Payload Reset	N/A	Payload cold reset from watchdog BIOS/OS event or reboot	Investigate why system reset, look at the events in the SEL, and monitor CPM.
43	OEM Active Boot Flash	Event only	CFD watchdog timed out, secondary flash bank was set to active.	Investigate watchdog timeout.
			Flash bank was set externally.	Customer-specific.
44	BMC Watchdog	Event only	Status only	No action required; information only.
			Payload cold reset	Investigate watchdog timeout. Check communications between the watchdog and IPMC.
			Payload power down	
			Payload power cycle	
			Pre-timeout interrupt	
45	IPMC Watchdog	N/A	Missing strobe from the IPMC to the IPMC FPGA.	Monitor to see if the event occurs again or becomes frequent.

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Table 37. Sensor alarms and recommended actions (Sheet 14 of 15)

Number	Name	Alarm level	Possible errors or faults	Recommendation
46	ATCA Physical IPMB	N/A	I²C data or clock lines problem	Investigate bus communication error. Possibly remove CPM and reinsert.
47	ATCA Physical IPMB-L	N/A	I²C data or clock lines problem	If IPMB-L bus does not recover on its own, hot swap CPM, and/or remove AMC until problem is resolved.
48	NMI	N/A	NMI generated	Investigate error.
49	+12V RTM PwrFail	N/A	Power problem	Monitor to see if the alarm worsens or is persistent for more than 1 day. If persistent, remove CPM and contact customer support.
50	+3.3V RTM Fail	N/A	Power problem	Monitor to see if the alarm worsens or is persistent for more than 1 day. If persistent, remove CPM and contact customer support.
51	+12V AMC PwrFail	N/A	Power problem	Monitor to see if the alarm worsens or is persistent for more than 1 day. If persistent, remove CPM and contact customer support.
52	+3.3V AMC Fail	N/A	Power problem	Monitor to see if the alarm worsens or is persistent for more than 1 day. If persistent, remove CPM and contact customer support.
53	IOH ThermTrip	N/A	IOH over temperature event	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
54	IOH Therm Alert	N/A	IOH over temperature event	Remove and/or hot swap CPM. If problem persists, remove CPM and contact customer support.
55	DDR Therm T64	N/A	Potential thermal problem	The board automatically shuts down when any of the temperature sensors trip the UNR setting on the up side.
56	CPU CAT ERR	N/A	CPU catastrophic failure	Remove the CPM and contact customer support.
57	AMC PwrFault	N/A	Power problem	Remove the CPM and contact customer support.
58	RTM PwrFault	N/A	Power problem	Check the power supply. The problem could be a hardware issue.
59	AMC PCIe PwrEn	N/A	AMC PCI Express device improperly enabled or disabled during hot swap	Check if the AMC is a PCI Express device. Also check if the device is supported by the CPM via E-Key.
60	RTM PCIe PwrEn	N/A	RTM PCI Express device improperly enabled or disabled during hot swap	Check if the RTM is a PCI Express device. Also check if the device is supported by the CPM via E-Key.
61	ENET Link 0	N/A	Ethernet link sensor does not report the link status	Check the network configuration, the type of cable, and the connector.
62	ENET Link 1	N/A	Ethernet link sensor does not report the link status	Check the network configuration, the type of cable, and the connector.
63	ENET Link 2	N/A	Ethernet link sensor does not report the link status	Check the network configuration, the type of cable, and the connector.

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Table 37. Sensor alarms and recommended actions (Sheet 15 of 15)

Number	Name	Alarm level	Possible errors or faults	Recommendation
64	ENET Link 3	N/A	Ethernet link sensor does not report the link status	Check the network configuration, the type of cable, and the connector.
65	ENET Link 4	N/A	Ethernet link sensor does not report the link status	Check the network configuration, the type of cable, and the connector.
66	ENET Link 5	N/A	Ethernet link sensor does not report the link status	Check the network configuration, the type of cable, and the connector.
67–254		N/A		

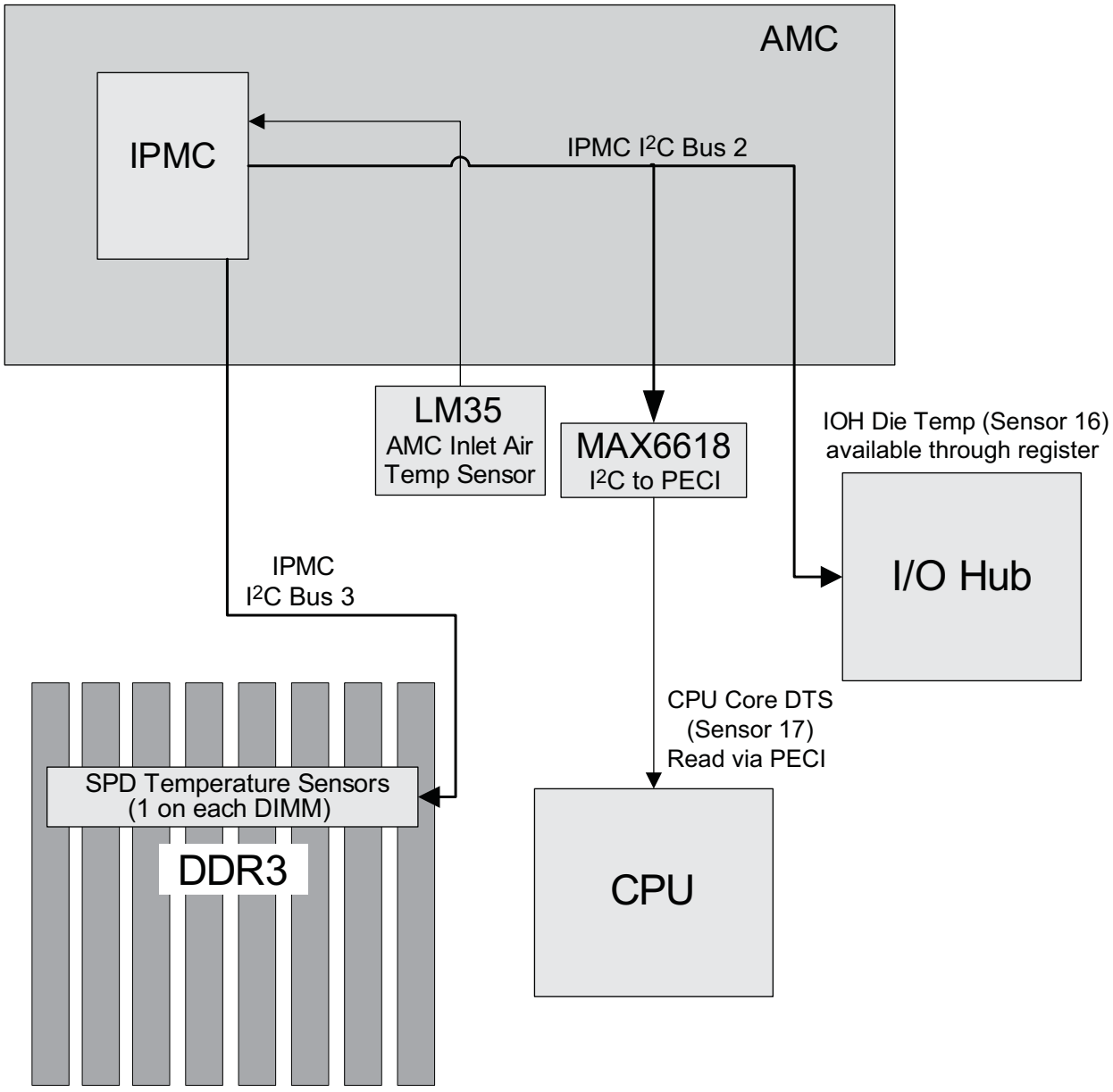
[1] Any voltage alarm during CPM bootup keeps the CPM in M3 state. If the CPM has already reached M4 state when the alarm occurs, it remains in M4 state.

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Temperature sensor locations

As shown in Figure 13, the CPM uses I²C busses 2 and 3 to access internal temperature information for the DIMMs, CPU cores, and the I/O hub.

Figure 13. Temperature sensor locations



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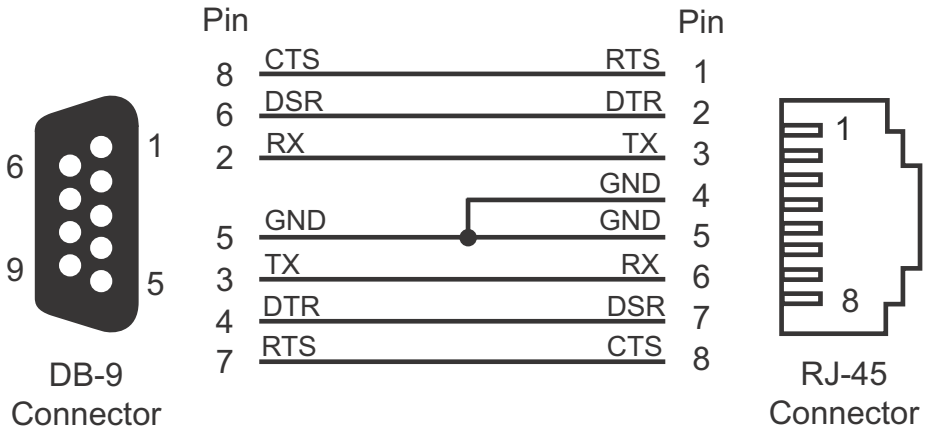
Front panel interfaces

The front USB and Ethernet interfaces are standard and not detailed here. The console serial port pins are described in Table 38 and illustrated in Figure 14.

Table 38. RS-232 serial port connector

Description	RJ-45 Pin	DB-9 Pin	Function
RTS	1	8	CTS ⇔ RTS
DTR	2	6	DSR ⇔ DTR
TXD	3	2	RX ⇔ TX
GND	4	5	ground
GND (Cable Detect)	5	5	ground
RXD	6	3	TX ⇔ RX
DSR	7	4	DTR ⇔ DSR
CTS	8	7	RTS ⇔ CTS

Figure 14. DB-9 to RJ-45 translation



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Backplane interfaces

Backplane connectivity summary

This section describes the backplane interface connectivity.

Table 39. Backplane connectivity summary

Connector	Channel	Port	Board usage	PICMG definition	Comments
P10	48V	A/B	Power	3.0	Dual 48V DC power
	IPMB	A/B	IPMB	3.0	Dual IPMB
J23	Base 1	–	10/100/1000Base-T Port A	3.0	Dual star Base interface
	Base 2	–	10/100/1000Base-T Port B	3.0	
	Fabric 1	0	10G BASE-BX4/KX4 Port A lane 0 or 1000BASE-BX/KX Port A	3.1 Option 1 or 9	Dual star Ethernet Fabric interface
		1	10G BASE-BX4/KX4 Port A lane 1 or 1000BASE-BX/KX AMC Port 0	3.1 Option 2 or 9	
		2	10G BASE-BX4/KX4 Port A lane 2 or 1000BASE-BX/KX AMC Port 8	3.1 Option 9 or Undefined Option	
		3	10G BASE-BX4/KX4 Port A lane 3	3.1 Option 9 or unused	
	Fabric 2	0	10G BASE-BX4/KX4 Port B lane 0 or 1000BASE-BX/KX Port B	3.1 Option 9, Option 1 or Option 2	Dual star Ethernet Fabric interface
		1	10G BASE-BX4/KX4 Port B lane 1 or 1000BASE-BX/KX AMC Port 1	3.1 Option 9 or Option 2	
		2	10G BASE-BX4/KX4 Port B lane 2 or 1000BASE-BX/KX AMC Port 9	3.1 Option 9 or Undefined Option	
		3	10G BASE-BX4/KX4 Port B lane 3	3.1 Option 9 or unused	
J20	Update	0	AMC Site “Fastpath” update channel port 12	3.0	For AMC APS
	Update	4	AMC Site “Slowpath”	3.0	For AMC APS
	Clock	1A/1B	Input: 8 kHz	3.0	Multiplexed to AMC bay TCLKA, TCLKC
		2A/2B	Input: 19.44 MHz	3.0	
		3A/3B	Output	3.0	Multiplexed from AMC bay TCLKB, TCLKD

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Zone 1 P10 connector pinout

Table 40. Zone 1 contact assignments, P10

Contact	Designation	Description	Mating sequence
1	Reserved	Reserved	*not applicable*
2	Reserved	Reserved	*not applicable*
3	Reserved	Reserved	*not applicable*
4	Reserved	Reserved	*not applicable*
5	HA0	Hardware Address Bit 0	Third
6	HA1	Hardware Address Bit 1	Third
7	HA2	Hardware Address Bit 2	Third
8	HA3	Hardware Address Bit 3	Third
9	HA4	Hardware Address Bit 4	Third
10	HA5	Hardware Address Bit 5	Third
11	HA6	Hardware Address Bit 6	Third
12	HA7/P	Hardware Address Bit 7 (Odd Parity Bit)	Third
13	SCL_A	IPMB Clock, Port A	Third
14	SDA_A	IPMB Data, Port A	Third
15	SCL_B	IPMB Clock, Port B	Third
16	SDA_B	IPMB Data, Port B	Third
17			
18			
19			
20			
21			
22			
23			
24			
25	SHELF_GND	Shelf Ground Connection to Shelf Ground and safety ground	First
26	LOGIC_GND	Logic Ground Ground reference and return for front blade-to-front blade logic signals	First
27	ENABLE_B	Enable B Short pin for power sequencing, Feed B, tied to VRTN_B on Backplane	Fourth
28	VRTN_A	Voltage Return A –48 Volt return, Feed A	First
29	VRTN_B	Voltage Return B –48 Volt return, Feed B	First

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Table 40. Zone 1 contact assignments, P10 (Continued)

Contact	Designation	Description	Mating sequence
30	EARLY_A	–48 Volt Early A –48 Volt input, Feed A precharge	First
31	EARLY_B	–48 Volt Early B –48 Volt input, Feed B precharge	First
32	ENABLE_A	Enable A Short pin for power sequencing, Feed A, tied to VRTN_A on Backplane	Fourth
33	–48V_A	–48 Volt A –48 Volt input, Feed A, uses ENABLE_A to enable converters	Second
34	–48V_B	–48 Volt B –48 Volt input, Feed B, uses ENABLE_B to enable converters	Third
	Gray indicates unused pins		

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Zone 2 J20 connector pinout

Table 41. Backplane connector J20 signals

Row	Interface designation	AB		CD		EF		GH	
1	Clks	CLK1A+	CLK1A–	CLK1B+	CLK1B–	CLK2A+	CLK2A–	CLK2B+	CLK2B–
2	Update Channel and Clks	Tx4(UP)+	Tx4(UP)–	Rx4(UP)+	Rx4(UP)–	CLK3A+	CLK3A–	CLK3B+	CLK3B–
3									
4		Tx0(UP)+	Tx0(UP)–	Rx0(UP)+	Rx0(UP)–				
5	Fabric Channel 15								
6									
7	Fabric Channel 14								
8									
9	Fabric Channel 13								
10									
Note: Each differential pair has an individual L-shaped ground contact (not shown).									
	Gray indicates unused pins								

Zone 2 J23 connector pinout

Table 42. Backplane connector J23 signals

Row	Interface designation	AB		CD		EF		GH	
1	Fabric Channel 2	Tx2[2]+	Tx2[2]–	Rx2[2]+	Rx2[2]–	Tx3[2]+	Tx3[2]–	Rx3[2]+	Rx3[2]–
2		Tx0[2]+	Tx0[2]–	Rx0[2]+	Rx0[2]–	Tx1[2]+	Tx1[2]–	Rx1[2]+	Rx1[2]–
3	Fabric Channel 1	Tx2[1]+	Tx2[1]–	Rx2[1]+	Rx2[1]–	Tx3[1]+	Tx3[1]–	Rx3[1]+	Rx3[1]–
4		Tx0[1]+	Tx0[1]–	Rx0[1]+	Rx0[1]–	Tx1[1]+	Tx1[1]–	Rx1[1]+	Rx1[1]–
5	Base Channel 1	BI_DA1+	BI_DA1–	BI_DB1+	BI_DB1–	BI_DC1+	BI_DC1–	BI_DD1+	BI_DD1–
6	Base Channel 2	BI_DA2+	BI_DA2–	BI_DB2+	BI_DB2–	BI_DC2+	BI_DC2–	BI_DD2+	BI_DD2–
7	Base Channel 3								
8	Base Channel 4								
9	Base Channel 5								
10	Base Channel 6								
Note: Each differential pair has an individual L-shaped ground contact (not shown).									
	Gray indicates unused pins								

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RTM interface pinout

Zone 3 J30 connector pinout

Table 43. RTM connector J30 signals

Row	AB		CD		EF		GH	
1	+12V_RTM	+12V_RTM	+12V_RTM	+3.3V_IPMC	RES_STATE	RTM_PRSNT*	RTM_HS_LED	RTM_EN*
2	+12V_RTM	+12V_RTM	+12V_RTM	IPMC_INT*	IPMC_I2C_CLK	IPMC_I2C_DAT	USB_D+	USB_D–
3	SERIAL_0_TX	SERIAL_0_RX	JTAG_TDI	JTAG_TDO	JTAG_TMS	JTAG_TCK	JTAG_TRST*	
4	SOCA	SOCB	INT_0	INT_1	RTML_TX	RTML_RX	RTML_CLK	RTM_RESET
5	SERIAL_1_TX	SERIAL_1_RX						
6							CPU0_SCL (SMB_SCL)	CPU0_SDA (SMB_SDA)
7								
8								
9	SAS0_TX+	SAS0_TX–	SAS0_RX+	SAS0_RX–	SAS1_TX+	SAS1_TX–	SAS1_RX+	SAS1_RX–
10	GE1_TX+	GE1_TX–	GE1_RX+	GE1_RX–	GE0_TX+	GE0_TX–	GE0_RX+	GE0_RX–
Note: Each differential pair has an individual L-shaped ground contact (not listed).								
	Gray indicates unused pins							

Zone 3 J31 connector pinout

Table 44. RTM connector J31 signals

Row	AB		CD		EF		GH	
1	AMC_17_TX+	AMC_17_TX–	AMC_17_RX+	AMC_17_RX–	AMC_18_TX+	AMC_18_TX–	AMC_18_RX+	AMC_18_RX–
2	AMC_19_TX+	AMC_19_TX–	AMC_19_RX+	AMC_19_RX–	AMC_20_TX+	AMC_20_TX–	AMC_20_RX+	AMC_20_RX–
3								
4								
5	PCIE1_RX2+	PCIE1_RX2–	PCIE1_TX2+	PCIE1_TX2–	PCIE1_RX3+	PCIE1_RX3–	PCIE1_TX3+	PCIE1_TX3–
6	PCIE1_RX0+	PCIE1_RX0–	PCIE1_TX0+	PCIE1_TX0–	PCIE1_RX1+	PCIE1_RX1–	PCIE1_TX1+	PCIE1_TX1–
7			PCI1_REFCLK+	PCI1_REFCLK–			PCI0_REFCLK+	PCI0_REFCLK–
8	PCIE0_RX2+	PCIE0_RX2–	PCIE0_TX2+	PCIE0_TX2–	PCIE0_RX3+	PCIE0_RX3–	PCIE0_TX3+	PCIE0_TX3–
9	AMC1_I2C_SCL	AMC1_I2C_SDA	SFP1_I2C_SCL	SFP1_I2C_SDA	SFP0_I2C_SCL	SFP0_I2C_SDA		
10	PCIE0_RX0+	PCIE0_RX0–	PCIE0_TX0+	PCIE0_TX0–	PCIE0_RX1+	PCIE0_RX1–	PCIE0_TX1+	PCIE0_TX1–
Note: Each differential pair has an individual L-shaped ground contact (not listed).								
	Gray indicates unused pins							

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AMC connector pinout

Table 45. AMC connector pinout

Pin	AMC pin name	Source	Description
1	GND		Logic Ground
2	MB_PWR	Carrier	Payload Power
3	MB_PS1#	AMC	Presence Sense 1
4	MB_MP	Carrier	Management Power
5	MB_GA0	Carrier	Geographical Address 0
6	MB_RSRVD6		Reserved
7	GND		Logic Ground
8	MB_RSRVD8		
9	MB_PWR	Carrier	Payload Power
10	GND		Logic Ground
11	MB_RX0+	AMC	GE RX from AMC to CPM Fabric Mux
12	MB_RX0–	AMC	GE RX from AMC to CPM Fabric Mux
13	GND		Logic Ground
14	MB_TX0+	Carrier	GE TX to AMC from CPM Fabric Mux
15	MB_TX0–	Carrier	GE TX to AMC from CPM Fabric Mux
16	GND		Logic Ground
17	MB_GA1	Carrier	Geographical Address 1
18	MB_PWR		Payload Power
19	GND		Logic Ground
20	MB_RX1+	AMC	GE RX from AMC to CPM Fabric Mux
21	MB_RX1–	AMC	GE RX from AMC to CPM Fabric Mux
22	GND		Logic Ground
23	MB_TX1+	Carrier	GE TX to AMC from CPM Fabric Mux
24	MB_TX1–	Carrier	GE TX to AMC from CPM Fabric Mux
25	GND		Logic Ground
26	MB_GA2	Carrier	Geographical Address 2
27	MB_PWR		Payload Power
28	GND		Logic Ground
29	MB_RX2+	AMC	SAS/SATA RX from AMC to SAS Mux
30	MB_RX2–	AMC	SAS/SATA RX from AMC to SAS Mux
31	GND		Logic Ground
32	MB_TX2+	Carrier	SAS/SATA RX to AMC from SAS Mux
33	MB_TX2–	Carrier	SAS/SATA RX to AMC from SAS Mux
34	GND		Logic Ground
35	MB_RX3+	AMC	SAS RX from AMC to the RTM (through the mux)
36	MB_RX3–	AMC	SAS RX from AMC to the RTM (through the mux)
37	GND		Logic Ground

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Table 45. AMC connector pinout (Continued)

Pin	AMC pin name	Source	Description
38	MB_TX3+	Carrier	SAS RX to AMC from the RTM (through the mux)
39	MB_TX3–	Carrier	SAS RX to AMC from the RTM (through the mux)
40	GND		Logic Ground
41	MB_ENABLE#	Carrier	AMC Enable
42	MB_PWR		Payload Power
43	GND		Logic Ground
44	MB_RX4+	AMC	PCIe from AMC RX to IOH Port 9 Lane 0
45	MB_RX4–	AMC	PCIe from AMC RX to IOH Port 9 Lane 0
46	GND		Logic Ground
47	MB_TX4+	Carrier	PCIe to AMC TX from IOH Port 9 Lane 0
48	MB_TX4–	Carrier	PCIe to AMC TX from IOH Port 9 Lane 0
49	GND		Logic Ground
50	MB_RX5+	AMC	PCIe from AMC RX to IOH Port 9 Lane 1
51	MB_RX5–	AMC	PCIe from AMC RX to IOH Port 9 Lane 1
52	GND		Logic Ground
53	MB_TX5+	Carrier	PCIe to AMC TX from IOH Port 9 Lane 1
54	MB_TX5–	Carrier	PCIe to AMC TX from IOH Port 9 Lane 1
55	GND		Logic Ground
56	MB_SCL_L	Carrier IPMC	IPMB-L Clock
57	MB_PWR	Carrier	Payload Power
58	GND		Logic Ground
59	MB_RX5+	AMC	PCIe from AMC RX to IOH Port 9 Lane 2
60	MB_RX5–	AMC	PCIe from AMC RX to IOH Port 9 Lane 2
61	GND		Logic Ground
62	MB_TX5+	Carrier	PCIe to AMC TX from IOH Port 9 Lane 2
63	MB_TX5–	Carrier	PCIe to AMC TX from IOH Port 9 Lane 2
64	GND		Logic Ground
65	MB_RX5+	AMC	PCIe from AMC RX to IOH Port 9 Lane 3
66	MB_RX5–	AMC	PCIe from AMC RX to IOH Port 9 Lane 3
67	GND		Logic Ground
68	MB_TX5+	Carrier	PCIe to AMC TX from IOH Port 9 Lane 3
69	MB_TX5–	Carrier	PCIe to AMC TX from IOH Port 9 Lane 3
70	GND		Logic Ground
71	MB_SDA_L	Carrier IPMC	IPMB-L Data
72	MB_PWR	Carrier	Payload Power
73	GND		Logic Ground
74	MB_TCLKA+	Carrier	Not supported
75	MB_TCLKA–	Carrier	Not supported

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Table 45. AMC connector pinout (Continued)

Pin	AMC pin name	Source	Description
76	GND		Logic Ground
77	MB_TCLKB+	AMC	Telecom Clock B+ Clock from AMC selectable to backplane SYNC_CLK3
78	MB_TCLKB–	AMC	Telecom Clock B– Clock from AMC selectable to backplane SYNC_CLK3
79	GND		Logic Ground
80	MB_FCLKA+	Carrier	Fabric Clock A+ 100 MHz clock from PCI Express clock generator
81	MB_FCLKA–	Carrier	Fabric Clock A– 100 MHz clock from PCI Express clock generator
82	GND		Logic Ground
83	MB_PS0#	Carrier	Presence Sense 0
84	MB_PWR	Carrier	Payload Power
85	GND		Logic Ground
86	GND		Logic Ground
87	MB_TX8–	Carrier	GE TX to AMC from CPM Fabric Mux
88	MB_TX8+	Carrier	GE TX to AMC from CPM Fabric Mux
89	GND		Logic Ground
90	MB_RX8–	AMC	GE RX from AMC to CPM Fabric Mux
91	MB_RX8+	AMC	GE RX from AMC to CPM Fabric Mux
92	GND		Logic Ground
93	MB_TX9–	Carrier	GE TX to AMC from CPM Fabric Mux
94	MB_TX9+	Carrier	GE TX to AMC from CPM Fabric Mux
95	GND		Logic Ground
96	MB_RX9–	AMC	GE RX from AMC to CPM Fabric Mux
97	MB_RX9+	AMC	GE RX from AMC to CPM Fabric Mux
98	GND		Logic Ground
99	MB_TX10–	Carrier	Not Used
100	MB_TX10+	Carrier	Not Used
101	GND		Logic Ground
102	MB_RX10–	AMC	Not Used
103	MB_RX10+	AMC	Not Used
104	GND		Logic Ground
105	MB_TX11–	Carrier	Not Used
106	MB_TX11+	Carrier	Not Used
107	GND		Logic Ground
108	MB_RX11–	AMC	Not Used
109	MB_RX11+	AMC	Not Used
110	GND		Logic Ground

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Table 45. AMC connector pinout (Continued)

Pin	AMC pin name	Source	Description
111	MB_TX12–	Carrier	Update channel TX to AMC from Fast Path Buffer
112	MB_TX12+	Carrier	Update channel TX to AMC from Fast Path Buffer
113	GND		Logic Ground
114	MB_RX12–	AMC	Update channel RX from AMC to Fast Path Buffer
115	MB_RX12+	AMC	Update channel RX from AMC to Fast Path Buffer
116	GND		Logic Ground
117	MB_TX13–	Carrier	Update channel TX to AMC from Slow Path Buffer
118	MB_TX13+	Carrier	Update channel TX to AMC from Slow Path Buffer
119	GND		Logic Ground
120	MB_RX13–	AMC	Update channel RX from AMC to Slow Path Buffer
121	MB_RX13+	AMC	Update channel RX from AMC to Slow Path Buffer
122	GND		Logic Ground
123	MB_TX14–	Carrier	Not Used
124	MB_TX14+	Carrier	Not Used
125	GND		Logic Ground
126	MB_RX14–	AMC	Not Used
127	MB_RX14+	AMC	Not Used
128	GND		Logic Ground
129	MB_TX15–	AMC	I²C clock from AMC through CPM to RTM used for SFP and LED control
130	MB_TX15+	AMC Carrier	I²C data from AMC through CM7 to RTM used for SFP and LED control
131	GND		Logic Ground
132	MB_RX15–	RTM	Serial port RX from RTM through CPM to AMC used for AMC debug
133	MB_RX15+	AMC	Serial port TX from AMC through CPM to RTM used for AMC debug
134	GND		Logic Ground
135	MB_TCLKC–	Carrier	Not supported
136	MB_TCLKC+	Carrier	Not supported
137	GND		Logic Ground
138	MB_TCLKD–	AMC	Telecom Clock D–
139	MB_TCLKD+	AMC	Telecom Clock D+
140	GND		Logic Ground
141	MB_TX17–	Carrier	SERDES TX from RTM through CPM to AMC
142	MB_TX17+	Carrier	SERDES TX from RTM through CPM to AMC
143	GND		Logic Ground
144	MB_RX17–	AMC	SERDES RX from AMC through CPM to RTM
145	MB_RX17+	AMC	SERDES RX from AMC through CPM to RTM

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Table 45. AMC connector pinout (Continued)

Pin	AMC pin name	Source	Description
146	GND		Logic Ground
147	MB_TX18–	Carrier	SERDES TX from RTM through CPM to AMC
148	MB_TX18+	Carrier	SERDES TX from RTM through CPM to AMC
149	GND		Logic Ground
150	MB_RX18–	AMC	SERDES RX from AMC through CPM to RTM
151	MB_RX18+	AMC	SERDES RX from AMC through CPM to RTM
152	GND		Logic Ground
153	MB_TX19–	Carrier	SERDES TX from RTM through CPM to AMC
154	MB_TX19+	Carrier	SERDES TX from RTM through CPM to AMC
155	GND		Logic Ground
156	MB_RX19–	AMC	SERDES RX from AMC through CPM to RTM
157	MB_RX19+	AMC	SERDES RX from AMC through CPM to RTM
158	GND		Logic Ground
159	MB_TX20–	Carrier	SERDES TX from RTM through CPM to AMC
160	MB_TX20+	Carrier	SERDES TX from RTM through CPM to AMC
161	GND		Logic Ground
162	MB_RX20–	AMC	SERDES RX from AMC through CPM to RTM
163	MB_RX20+	AMC	SERDES RX from AMC through CPM to RTM
164	GND		Logic Ground
165	MB_TCK	Carrier	JTAG Test Clock from CPM to AMC
166	MB_TMS	Carrier	JTAG Test Mode Select from CPM to AMC
167	MB_TRST#	Carrier	JTAG Test Reset from CPM to AMC
168	MB_TDO	AMC	JTAG Test Data Out from AMC to CPM
169	MB_TDI	Carrier	JTAG Test Data In from CPM to AMC
170	GND		Logic Ground
LEGEND			
	Logic Ground		
	+12V Payload Power		
	+3.3V Management Power		
	Fabric Interface Differential Signals		
	Synchronization Clocks		

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Jumper settings

Figure 15 shows the physical location of the strapping header, and Table 46 describes the effect of jumpering each pair of pins.

Figure 15. Strapping header

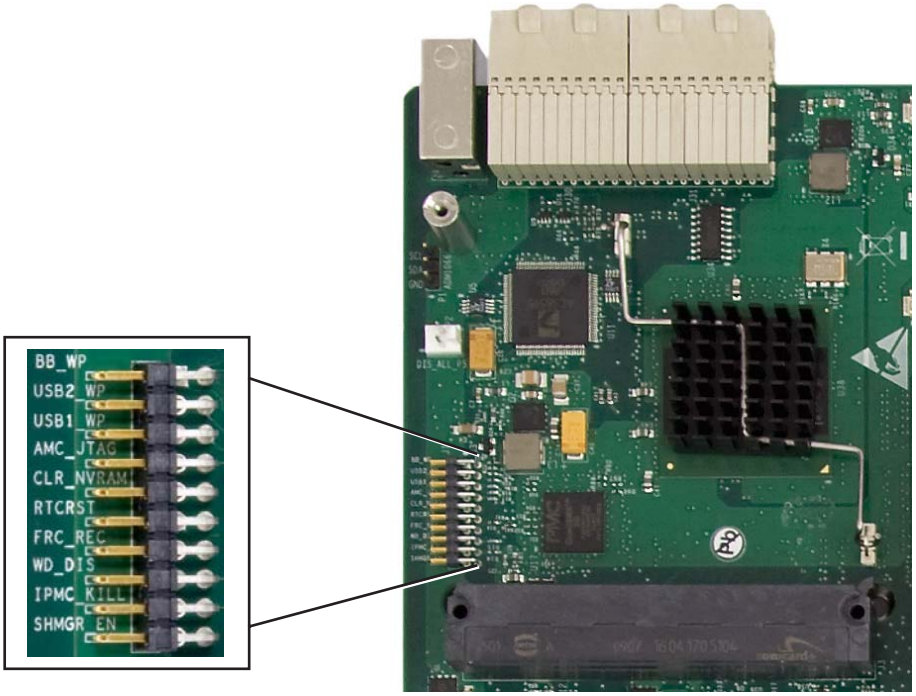


Table 46. Jumpering pin pairs

Pin pair	Effect
1 and 2	Write protect the BIOS boot block
3 and 4	Write protect eUSB module 2
5 and 6	Write protect eUSB module 1
7 and 8	Include the AMC in the JTAG chain
9 and 10	Clear CMOS asserted
11 and 12	RTCRST asserted
13 and 14	Force BIOS recovery mode (debug only)
15 and 16	Disable all watchdogs (debug only)
17 and 18	IPMC kill enable (debug only)
19 and 20	Shelf Manager enable (reserved for future use)

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FRU INFORMATION D

FRU information is stored in non-volatile memory and is used by the IPMC to locate and communicate with the available FRUs. The CPM stores its FRU information in compliance with these specifications:

- *IPMI Platform Management FRU Information Storage Definition*, v1.0, Revision 1.1
- PICMG 3.0 Revision 2.0 *AdvancedTCA Base Specification*

The *rsys-ipmitool* utility can retrieve all FRU information, including backplane E-Keying and on-board E-Keying information.

FRU information areas used

The CPM provides this FRU information:

- Common header
- Internal use area
- Board information area
- Product information area
- Multirecord area

Multirecord area records used

- Carrier information record
- Carrier activation and current management record
- LED description record
- Board point-to-point connectivity record
- Carrier point-to-point connectivity record
- PMC8380 SAS (MUX Device#1) point-to-point connectivity record
- PMC8380 Fabric-A (MUX Device#2) point-to-point connectivity record
- PMC8380 Fabric-B (MUX Device#3) point-to-point connectivity record
- TTL Buffer (Update Channel 4) point-to-point connectivity record
- OPLIN point-to-point connectivity record
- Carrier clock point-to-point connectivity record
- DB800 PCIe clock buffer configuration record
- Sync Clock3 A/B clock configuration record
- ACS8595 clock configuration record

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CPM and FRU device IDs

The CPM IPMC contains unique identification information. Table 47 and Table 48 describe those identifiers.

Table 47. CPM ID information

Field	Value
Device Name	ATCA-4500
Device ID	011h (ATCA CPU module)
Firmware Version	<Current Firmware Version in format XX.YY>
IPMI Version	1.5
IPM Support	02Dh
Product ID[a]	03873
Manufacturing ID	4337

[a] From the 061-XXXXX-0000 number for the CPM PC board with components fully populated.

Table 48. CPM FRU ID

Module	FRU ID
CPM main board	0
AMC bay 1	1
RTM	2

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LOW-LEVEL HARDWARE MAP E

This appendix provides details for the CPM input and output, main memory maps, and SMBus maps. Additional information is provided for the PCI bus device map, including interrupt lines for the PCI device peripherals. This appendix provides crucial information for the developer who needs to know memory locations of the peripheral devices and their interrupt routing.

PCI bus device map

Table 49 provides device identification for the CPM's peripheral connections. Many of the devices available in the various chipset components are not used. They are shown here, but the devices do not show up in a PCI scan when they are disabled by the system BIOS.

Table 49. PCI device map

Peripheral	Device ID	Device #	Function #	Bus #	INTR mapping	Enabled?
Intel 5520 I/O Hub						
ESI (Dev 0 in ESI mode)	3406h	0	0	0	**N.A.**	Yes
PCI-Express Root Port 0 (Dev #0 in PCIe Mode)	3420h or 3421h	0	0	0	**N.A.**	Yes
PCI-Express Root Port 1	3408h	1	0	0	**N.A.**	No
PCI-Express Root Port 2	3409h	2	0	0	**N.A.**	No
PCI-Express Root Port 3	340Ah	3	0	0	**N.A.**	Yes
PCI-Express Root Port 4	340Bh	4	0	0	**N.A.**	Yes
PCI-Express Root Port 5	340Ch	5	0	0	**N.A.**	Yes
PCI-Express Root Port 6	340Dh	6	0	0	**N.A.**	Yes
PCI-Express Root Port 7	340Eh	7	0	0	**N.A.**	Yes
PCI-Express Root Port 8	340Fh	8	0	0	**N.A.**	No
PCI-Express Root Port 9	3410h	9	0	0	**N.A.**	Yes
PCI-Express Root Port 10	3411h	10	0	0	**N.A.**	Yes
Intel QPI Port 0	3425h	16	0	0	**N.A.**	No
Intel QPI Port 0	3426h	16	1	0	**N.A.**	No
Intel QPI Port 1	3427h	17	0	0	**N.A.**	Yes
Intel QPI Port 1	3428h	17	1	0	**N.A.**	Yes
IOxAPIC	342Dh	19	0	0	**N.A.**	Yes
Core	342Eh	20	0	0	**N.A.**	Yes
Core	3422h	20	1	0	**N.A.**	Yes
Core	3423h	20	2	0	**N.A.**	Yes
Core	3438h	20	3	0	**N.A.**	Yes

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Table 49. PCI device map (Continued)

Peripheral	Device ID	Device #	Function #	Bus #	INTR mapping	Enabled?
ICH10R I/O Controller Hub						
SATA	3A55h	22	0	0	N.A.	Yes
VECI	3A51h	23	0	0	N.A.	
LAN	3A7Ch	25	0	0	N.A.	No
USB UHCI #4	3A67h	26	0	0	N.A.	
USB UHCI #5	3A68h	26	1	0	N.A.	
USB UHCI #6	3A69h	26	2	0	N.A.	
USB EHCI #2	3A6Ch	26	7	0	N.A.	
Intel High Definition Audio	3A6Eh	27	0	0	N.A.	No
PCI Express Port 1	3A70h	28	0	0	N.A.	No
PCI Express Port 2	3A72h	28	1	0	N.A.	No
PCI Express Port 3	3A74h	28	2	0	N.A.	No
PCI Express Port 4	3A76h	28	3	0	N.A.	No
PCI Express Port 5	3A78h	28	4	0	N.A.	No
PCI Express Port 6	3A7Ah	28	5	0	N.A.	No
USB UHCI #1	3A64h	29	0	0	N.A.	
USB UHCI #2	3A65h	29	1	0	N.A.	
USB UHCI #3	3A66h	29	2	0	N.A.	
USB UHCI #6	3A69h	29	3	0	N.A.	
USB EHCI #1	3A6Ah	29	7	0	N.A.	
DMT to PCI Bridge	244Eh	30	0	0	N.A.	Yes
LPC-Corp ENG. Samples	3A10h	31	0	0	N.A.	Yes
LPC-ICH10DO	3A14h	31	0	0	N.A.	Yes
LPC-ICH10D	3A1Ah	31	0	0	N.A.	Yes
SATA-Non-AHCI and Non-RAID Mode (Ports 0, 1, 2, 3)	3A00h	31	2	0	N.A.	Yes
SATA-AHCI Mode (Ports 0-5)	3A02h	31	2	0	N.A.	Yes
SATA-RAID 0/1/5/10 Mode for Corp ENG. Samples	3A04h	31	2	0	N.A.	Yes
SATA-RAID 0/1/5/10 Mode	3A05h	31	2	0	N.A.	Yes
SMBus	3A60h	31	3	0	N.A.	Yes
SATA	3A06h	31	5	0	N.A.	Yes
Thermal	3A62h	31	6	0	N.A.	
Intel Xeon L5518 CPU						
QPI Architecture Generic Non-core Registers	2C40h	0	0		N.A.	
QPI Architecture System Address Decoder	2C01h	0	1		N.A.	
QPI Link 0	2C10h	2	0		N.A.	

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Table 49. PCI device map (Continued)

Peripheral	Device ID	Device #	Function #	Bus #	INTR mapping	Enabled?
QPI Physical 0	2C11h	2	1		N.A.	
QPI Link 1	2C14h	2	4		N.A.	
QPI Physical 1	2C15h	2	5		N.A.	
Intel Xeon L5518 CPU Integrated Memory Controller						
Registers	2C18h	3	0		N.A.	
Target Address Decoder	2C19h	3	1		N.A.	
RAS Registers	2C1Ah	3	2		N.A.	
Test Registers	2C1Ch	3	4		N.A.	
Channel 0 Control	2C20h	4	0		N.A.	
Channel 0 Address	2C21h	4	1		N.A.	
Channel 0 Rank	2C22h	4	2		N.A.	
Channel 0 Thermal Control	2C23h	4	3		N.A.	
Channel 1 Control	2C28h	5	0		N.A.	
Channel 1 Address	2C29h	5	1		N.A.	
Channel 1 Rank	2C2Ah	5	2		N.A.	
Channel 1 Thermal Control	2C2Bh	5	3		N.A.	
Channel 2 Control	2C30h	6	0		N.A.	
Channel 2 Address	2C31h	6	1		N.A.	
Channel 2 Rank	2C32h	6	2		N.A.	
Channel 2 Thermal Control	2C33h	6	3		N.A.	
82576EB (Base Controller)					N.A.	
RTM Device[a]					N.A.	
82598EB					N.A.	
AMC Device[b]					N.A.	
82576EB (Front Controller)					N.A.	

[a] Dependent on the RTM that is used

[b] Dependent on the AMC that is used

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Interrupts

This section describes I/O controller hub interrupts, APIC interrupt mapping, and PIC interrupt mapping.

I/O controller hub interrupts

The I/O controller hub (ICH10R) has two built-in interrupt controllers: the 8259 Programmable Interrupt Controller (PIC) and the Advanced Programmable Interrupt Controller (APIC). The ICH accepts interrupts from the following sources:

- PIRQ[D:A]#–PCI interrupt requests
- PIRQ[H:E]#–PCI interrupt requests
- System Control Interrupt (SCI)
- Internal High Precision Event Timer (HPET)
- Serial IRQ (SERIRQ#)

The PIC implements two 8259s that provide ISA-compatible interrupts for system timer, serial/parallel ports, keyboard controller, mouse, floppy disk, and DMA channels. In addition, the 8259 can support PCI interrupts if they are mapped onto the compatible ISA interrupt lines.

The APIC provides 24 interrupts and handles interrupt requests through memory accesses on the CPU data path. Interrupt priorities can be reassigned based on the end application.

APIC interrupt mapping

Table 50 lists the APIC interrupt mapping for the CPM.

Table 50. APIC interrupt mapping

ICH APIC IRQ#	Source	Interrupt	ICH input	Shared?
IRQ0	Cascade from 8259 #1	N/A	Internal	
IRQ1	USB keyboard controller	INT9	Internal	No
IRQ2	8254 counter 0, HPET #0	N/A	Internal	
IRQ3 (data frame 4)	Super I/O	COM2	SERIRQ	No
IRQ4 (data frame 5)	Super I/O	COM1	SERIRQ	No
IRQ5 (data frame 6)	RTM (future RTM)	RTM_INT0	SERIRQ (from CPU complex FPGA)	No
IRQ6 (data frame 7)	IPMC	Message Interrupt	SERIRQ	No
IRQ7 (data frame 8)	RTM (future RTM)	RTM_INT1	SERIRQ (from CPU complex FPGA)	No
IRQ8	RTC, HPET #1	N/A	Internal	
IRQ9				

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Table 50. APIC interrupt mapping (Continued)

ICH APIC IRQ#	Source	Interrupt	ICH input	Shared?
IRQ10 (data frame 11)	TPM	SERIRQ	SERIRQ	No (BIOS or SW must program)
IRQ11	HPET #2	N/A	Internal	No[a]
IRQ12	HPET #3	N/A	Internal	No[a]
IRQ13				
IRQ14	SATA PRIMARY (legacy mode)	N/A	Internal	No
IRQ15				
IRQ16	CPU complex FPGA	SOC_INT_N	PIRQA#	No
IRQ17	PCI9030	INTA#	PIRQB#	No
IRQ18	CPU complex FPGA	CS_INT_N	PIRQC#	No
IRQ19	CPU complex FPGA	N/A	PIRQD#	No
IRQ20	CPU complex FPGA	COUNT_INT_N	PIRQE#	No
IRQ21	CPU complex FPGA	CLOCK_INT_N	PIRQF#	No
IRQ22	IPMC	Optional payload interrupt	PIRQG#	No
IRQ23	CPU complex FPGA	FPGA_INT_N	PIRQH#	No
N/A (data frame 3)	IPMC	SMI	SERIRQ	No

[a] If used for HPET, no interrupt sharing is allowed.

PIC interrupt mapping

Table 51 lists the signals connected to the 8259-compatible programmable interrupt controller.

Table 51. PIC interrupt mapping

8259 input	Interrupt signal name	Ball	Function	Shared?
PIRQA*	FPGA_INT0_N	J5	Spare interrupt from CPU complex FPGA	No
PIRQB*	Unused	E1		No
PIRQC*	FPGA_INT1_N	F1	Spare interrupt from CPU complex FPGA	No
PIRQD*	FPGA_INT2_N	A3	Spare interrupt from CPU complex FPGA	No
PIRQE*	FPGA_INT3	K6	Spare interrupt from CPU complex FPGA	No
PIRQF*	FPGA_INT4	L7	Spare interrupt from CPU complex FPGA	No
PIRQG*	IPMC_INTR_N	F2	Spare interrupt from IPMC	No
PIRQH*	FPGA_INT_N	G2	Spare interrupt from CPU complex FPGA	No

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I/O map

The hub interface cycles that go to target ranges that are marked as "RESERVED" are not decoded by the ICH; they are passed to the PCI. If a PCI master targets one of the fixed I/O target ranges, it is positively decoded by the ICH in Medium speed. Address ranges that are not marked or specified in Table 52 are not decoded by the ICH unless assigned to one of the variables ranges.

Table 52. ICH10R I/O address map

I/O address	Read target	Write target	Functional unit	Location
00h–08h	DMA Controller	DMA Controller	DMA	ICH10R
09h–0Eh	RESERVED	DMA Controller	DMA	ICH10R
0Fh	DMA Controller	DMA Controller	DMA	ICH10R
10h–18h	DMA Controller	DMA Controller	DMA	ICH10R
19h–1Eh	RESERVED	DMA Controller	DMA	ICH10R
1Fh	DMA Controller	DMA Controller	DMA	ICH10R
20h–21h	Interrupt Controller	Interrupt Controller	Interrupt	ICH10R
24h–25h	Interrupt Controller	Interrupt Controller	Interrupt	ICH10R
28h–29h	Interrupt Controller	Interrupt Controller	Interrupt	ICH10R
2Ch–2Dh	Interrupt Controller	Interrupt Controller	Interrupt	ICH10R
2Eh–2Fh	LPC SIO	LPC SIO	Forwarded to LPC	ICH10R
30h–31h	Interrupt Controller	Interrupt Controller	Interrupt	ICH10R
34h–35h	Interrupt Controller	Interrupt Controller	Interrupt	ICH10R
38h–39h	Interrupt Controller	Interrupt Controller	Interrupt	ICH10R
3Ch–3Dh	Interrupt Controller	Interrupt Controller	Interrupt	ICH10R
40h–42h	Timer/Counter	Timer/Counter	PIT (8254)	ICH10R
43h	RESERVED	Timer/Counter	PIT	ICH10R
4Eh–4Fh	LPC-SIO	LPC SIO	Forwarded to LPC	ICH10R
50h-52h	Timer/Counter	Timer/Counter	PIT	ICH10R
53h	RESERVED	Timer/Counter	PIT	ICH10R
60h	Microcontroller	Microcontroller	Forwarded to LPC	ICH10R
61h	NMI Controller	NMI Controller	Processor I/F	ICH10R
62h	Microcontroller	Microcontroller	Forwarded to LPC	ICH10R
64h	Microcontroller	Microcontroller	Forwarded to LPC	ICH10R
66h	Microcontroller	Microcontroller	Forwarded to LPC	ICH10R
70h	RESERVED	NMI and RTC Controller	RTC	ICH10R
71h	RTC Controller	RTC Controller	RTC	ICH10R
72h	RTC Controller	NMI and RTC Controller	RTC	ICH10R
73h	RTC Controller	RTC Controller	RTC	ICH10R
74h	RTC Controller	NMI and RTC Controller	RTC	ICH10R
75h	RTC Controller	RTC Controller	RTC	ICH10R
76h	RTC Controller	NMI and RTC Controller	RTC	ICH10R

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Table 52. ICH10R I/O address map (Continued)

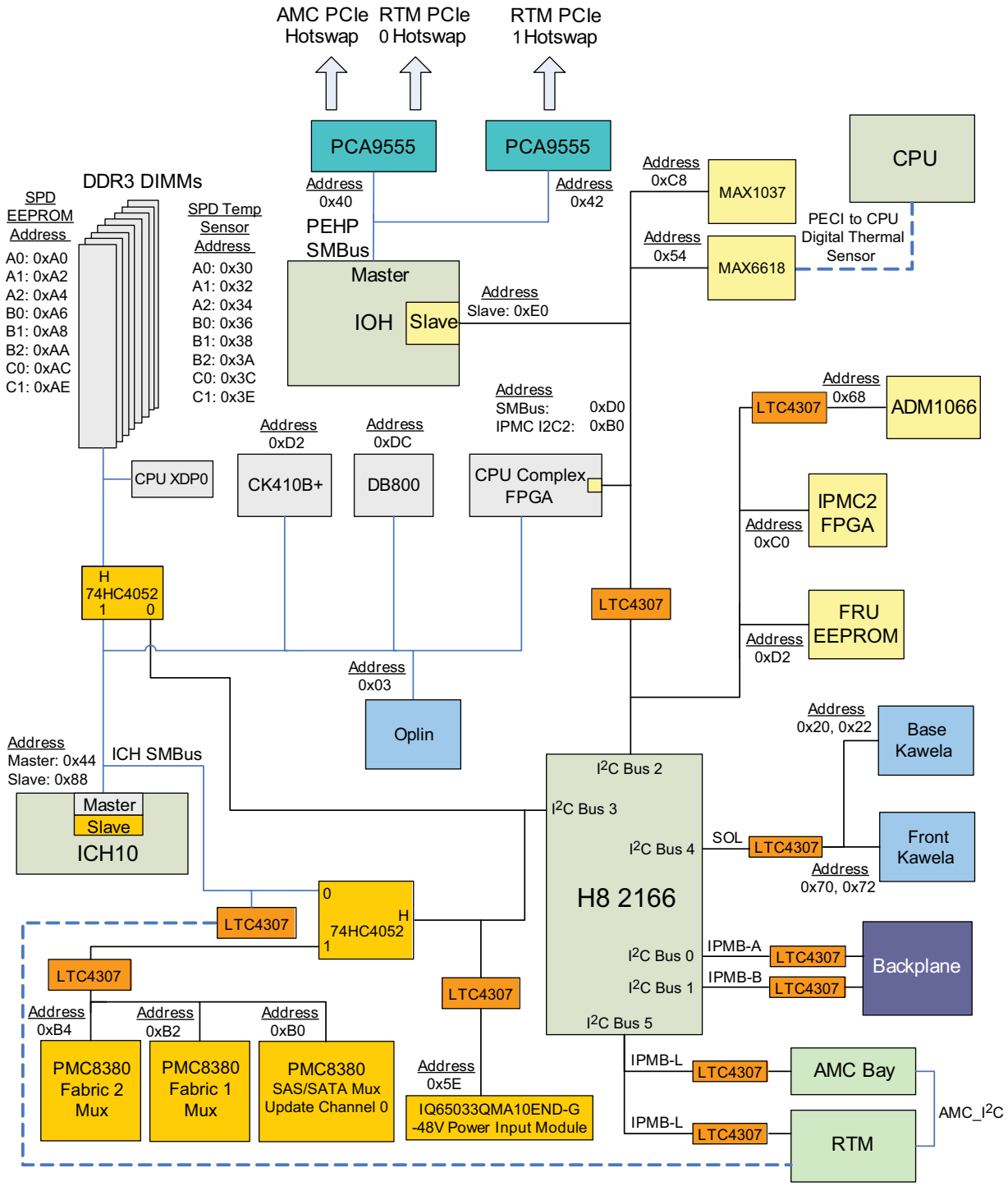
I/O address	Read target	Write target	Functional unit	Location
77h	RTC Controller	RTC Controller	RTC	ICH10R
80h	DMA Controller, or LPC, or PCI	DMA Controller, or LPC, or PCI	DMA	ICH10R
81h–83h	DMA Controller	DMA Controller	DMA	ICH10R
84h–86h	DMA Controller	DMA Controller, or LPC, or PCI	DMA	ICH10R
87h	DMA Controller	DMA Controller	DMA	ICH10R
88h	DMA Controller	DMA Controller, or LPC, or PCI	DMA	ICH10R
89h–8Bh	DMA Controller	DMA Controller	DMA	ICH10R
8Ch–8Eh	DMA Controller	DMA Controller, or LPC, or PCI	DMA	ICH10R
08Fh	DMA Controller	DMA Controller	DMA	ICH10R
90h–91h	DMA Controller	DMA Controller	DMA	ICH10R
92h	Reset Generator	Reset Generator	Processor I/F	ICH10R
93h-9Fh	DMA Controller	DMA Controller	DMA	ICH10R
A0h–A1h	Interrupt Controller	Interrupt Controller	Interrupt	ICH10R
A4h–A5h	Interrupt Controller	Interrupt Controller	Interrupt	ICH10R
A8h–A9h	Interrupt Controller	Interrupt Controller	Interrupt	ICH10R
ACh–ADh	Interrupt Controller	Interrupt Controller	Interrupt	ICH10R
B0h–B1h	Interrupt Controller	Interrupt Controller	Interrupt	ICH10R
B2h–B3h	Power Management	Power Management	Power Management	ICH10R
B4h–B5h	Interrupt Controller	Interrupt Controller	Interrupt	ICH10R
B8h–B9h	Interrupt Controller	Interrupt Controller	Interrupt	ICH10R
BCh–BDh	Interrupt Controller	Interrupt Controller	Interrupt	ICH10R
C0h–D1h	DMA Controller	DMA Controller	DMA	ICH10R
D2h–DDh	RESERVED	DMA Controller	DMA	ICH10R
DEh–DFh	DMA Controller	DMA Controller	DMA	ICH10R
F0h	PCI and Master Abort	FERR#/IGNNE#/Interrupt Controller	Processor I/F	ICH10R
170h–177h	SAS Controller or PCI	SAS Controller or PCI	Forwarded to SATA	ICH10R
1F0h–1F7h	SAS Controller or PCI	SAS Controller or PCI	Forwarded to SATA	ICH10R
376h	SAS Controller or PCI	SAS Controller or PCI	Forwarded to SATA	ICH10R
3F6h	SAS Controller or PCI	SAS Controller or PCI	Forwarded to SATA	ICH10R
4D0h–4D1h	Interrupt Controller	Interrupt Controller	interrupt	ICH10R
CF9h	Reset Generator	Reset Generator	Processor I/F	ICH10R

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I²C and SMBus map

Figure 16 illustrates the SMBus connections and addresses, which are listed in Table 53 on page 135.

Figure 16. I²C and SMBus devices



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Table 53. I²C and SMBus device addresses

Device	Master / slave	Bus #	Read address	Write address
IPMC EEPROM	Slave	2	A1h	A0h
IPMC FPGA	Slave	2	C1h	C0h
CPU Complex FPGA	Slave	2	B1h	B0h
MAX1037 ADC	Slave	2	C9h	C8h
MAX6618 PECI-to-I2C	Slave	2	55h	54h
Tylersburg IOH	Slave	2	E1h	E0h
ADM1066	Slave	2	69h	68h
PMC8380 Fabric 1	Slave	3	B3h	B2h
PMC8380 Fabric 2	Slave	3	B5h	B6h
PMC8380 SAS	Slave	3	B1h	B0h
48V Power Input Module	Slave	3	5Fh	5Eh
ICH10R	Slave	3	89h	88h
DIMM A0 Temp Sensor	Slave	3	31h	30h
DIMM A1 Temp Sensor	Slave	3	33h	32h
DIMM A2 Temp Sensor	Slave	3	35h	34h
DIMM B0 Temp Sensor	Slave	3	37h	36h
DIMM B1 Temp Sensor	Slave	3	39h	38h
DIMM B2 Temp Sensor	Slave	3	3Bh	3Ah
DIMM C0 Temp Sensor	Slave	3	3Dh	3Ch
DIMM C1 Temp Sensor	Slave	3	3Fh	3Eh
82576EB (Base) LAN0	Slave	4	21h	20h
82576EB (Base) LAN1	Slave	4	23h	22h
82576EB (Front) LAN0	Slave	4	71h	70h
82576EB (Front) LAN1	Slave	4	73h	72h
AMC MMC	Master/Slave	5	GA[2:0] = UGU; IPMB-L Address = 7Ah[a]	
RTM MMC	Master/Slave	5	GA[2:0] = GPU; IPMB-L Address = 90h[b]	
CK410B+	Slave	SMBus	D3h	D2h
DB800	Slave	SMBus	DDh	DCh
CPU Complex FPGA	Slave	SMBus	D1h	D0h
82598EB (Oplin)	Slave	SMBus	03h	02h
DIMM A0 SPD	Slave	SMBus	A1h	A0h
DIMM A1 SPD	Slave	SMBus	A3h	A2h
DIMM A2 SPD	Slave	SMBus	A5h	A4h
DIMM B0 SPD	Slave	SMBus	A7h	A6h
DIMM B1 SPD	Slave	SMBus	A9h	A8h
DIMM B2 SPD	Slave	SMBus	ABh	AAh
DIMM C0 SPD	Slave	SMBus	ADh	ACh

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Table 53. I²C and SMBus device addresses (Continued)

Device	Master / slave	Bus #	Read address	Write address
DIMM C1 SPD	Slave	SMBus	AFh	AEh
PCA9555 (AMC PCIe and RTM PCIe0)	Slave	IOH SMBus	41h	40h
PCA9555 (RTM PCIe1)	Slave	IOH SMBus	43h	42h

[a] The three geographical pins GA[2:0] are used to assign to IPMB-L address of the AMC. G=Logic Ground, U=Unconnected, P=Pulled up to P3V3 Management Power.

[b] The IPMB-L address of the RTM is assigned in the firmware.

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