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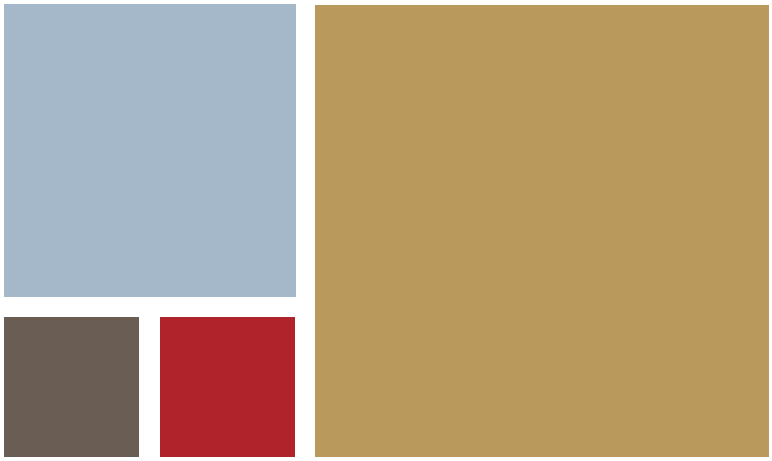
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PROMENTUM™

ATCA-4200
Compute Processing Module

Hardware Reference



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Preface

This manual describes the Promentum ATCA-4200 Compute Processing Module (CPM).

This manual assists engineers or technicians who perform any of these functions related to the ATCA-4200 module:

- Installs the blade—for development or configuration.
- Installs application-specific software on the blade.
- Configures the blade for use in a particular application.
- Designs or develops application-specific software for use on the blade.

This manual assumes you know how to connect and disconnect standard types of cables. If you configure, modify, or install software on the blade, this guide assumes you know how to use and configure operating systems and networks.

About This Manual

Notational Conventions

This manual uses the following conventions:

BoldText	A command or keyword.
`MonoText`	Screen text and syntax strings.
`ItalicText`	Variable parameters.

All numbers are decimal unless otherwise stated.

Notes	Indicates important information about the product.
WARNING	Indicates potentially hazardous situations which, if not avoided, may result in minor or moderate injury, or damage to data or hardware.

Electrostatic Discharge

WARNING
This product contains static-sensitive components and should be handled with care. Failure to employ adequate anti-static measures can cause irreparable damage to components.

Electrostatic discharge (ESD) damage can result in partial or complete device failure, performance degradation, or reduced operating life. To avoid ESD damage, the following precautions are strongly recommended.

- Keep each module/PCB in its ESD shielding bag until you are ready to install it.
- Before touching a module, attach an ESD wrist strap to your wrist and connect its other end to a known ground.
- Handle the module only in an area that has its working surfaces, floor coverings, and chairs connected to a known ground.
- Hold modules only by their edges and mounting hardware. Avoid touching PCB components and connector pins.

For further information on ESD, visit www.esda.org.

Where To Get More Information

You can find out more about the ATCA-4200 module from these sources:

- **World Wide Web**: RadiSys maintains an active Web site at www.radisys.com. The site contains current information about the company and locations of sales offices, new and existing products, contacts for sales, service, software updates, manuals, and technical support information.
- **RadiSys sales representative:** If you purchased your product from RadiSys, contact your sales representative via email or phone.
- **Other**: If you purchased your RadiSys product from a third-party vendor, you can contact that vendor for service and support.

Related Information

RadiSys Promentum™ SYS-6000 Platform Manuals

Title	Description
SYS-6000 Reference Manual, ATCA Blade Server Platform	Describes the SYS-6000 Platform and assists an engineer or technician who performs the following actions related to the platform: • Hardware installation • Software installation • System configuration • System maintenance • Application software development related to the platform.
SYS-6000 Installation Guide	Explains how to install the Promentum™ SYS-6000 Platform.
ATCA Module Installation Guide	Explains how to install ATCA modules, such as the ATCA-2100 (Switch and Control Module) and ATCA-3000 (Fibre Channel Disk Storage Module.
ATCA-1000 Reference Manual, Universal PMC Processing Module	Documents the ATCA-1000 (Universal PMC Processing Module), an optional expansion module that accommodates up to four PMCs (PCI Mezzanine Cards).
ATCA-2100 Reference Manual, Switch and Control Module	Documents the ATCA-2100s (Switch and Control Modules) that contain processors and base-interface and fabric-interface switches.
ATCA-3000 Reference Manual, Fibre Channel Disk Storage Module	Documents the ATCA-3000 (Fibre Channel Disk Storage Module), an optional module that contains high-capacity disk storage devices.
ATCA-4000 Reference Manual, Intel® Architecture Compute Processing Module	Documents the ATCA-4000 (Compute Processing Module), an optional module that contains dual high-speed CPUs.
ATCA-6000 Reference Manual, 12U 14-Slot ATCA Shelf	Documents the ATCA-6000 shelf, backplane, SDP (Shelf Display Panel), PEMs (Power Entry Modules), AMMs (Air Mover Modules), ATCA-5000 (Shelf Peripherals Module), and related hardware that provide the platform's foundation.
ATCA-7010 Hardware Reference Manual, Packet Processing Module	Documents the ATCA-7010 (10 GBPS Packet Processing Module), an optional module that extends the capability of the Promentum family to applications requiring high bandwidth line cards.
ATCA-7010 Software Reference Manual, Packet Processing Module	Documents the software for the ATCA-7010, a module that enables wire speed packet-processing capability in networks.
ATCA-7010 Installation Guide, Packet Processing Module	Documents both hardware and software installation and setup for the ATCA-7010 module.

Title	Description
SYS-6000 Platform Software Reference Manual, Ethernet Software	Documents the base-interface management CLI that enables you to configure and manage the Ethernet base interface.
SYS-6000 Platform Software Reference Manual, Fibre Channel Software	Documents the Fibre Channel management CLI that enables you to configure and manage the Fibre Channel fabric interface.
SYS-6000 Platform Software Reference Manual, Shelf Manager Software	Documents the Shelf Manager API that enables your application software to interact with shelf-management software.
Release Notes	Lists features and issues not included in other documentation.
Regulatory Compliance	Lists how the SYS-6000 Promentum Platform complies with regulatory requirements.

Reference Documents

The following documents should be available when using this specification. Documents that are not available on web sites may be obtained from your IBL (Intel Business Link) account, or contact your Intel Field Sales Engineer (FSE) or Field Application Engineer (FAE).

- AdvancedTCA Specification (http://www.advancedtca.org)
- PICMG Advanced Mezzanine Card AMC.0 Specification D0.97, September, 2004 (http://www.picmg.org)
- Renesas H8S/2168 Group Product Specification (http://www.renesas.com/fmwk.jsp?cnt=h8s2168_root.jsp&fp=/products/mpumcu/h8s_family/h8s2100_series/h8s2168_group/)
- Zarlink* ZL30410 Multi-service Line Card PLL Product Information (http://products.zarlink.com/product_profiles/ZL30410.htm)

The following Intel Corporation documents may be required for more detailed information:

- Intel® 6300ESB I/O Controller Hub Datasheet (http://www.intel.com/design/chipsets/embedded/docs/6300esb.htm)
- Intel® 6700PXH 64-bit PCI Hub Datasheet (http://www.intel.com/design/chipsets/embedded/docs/e7520.htm)
- Intel® 82546GB Gigabit Ethernet Controller Datasheet (http://www.intel.com/design/network/products/lan/controllers/82546gb.htm)
- Intel® 82551ER Fast Ethernet PCI Controller Datasheet (http://www.intel.com/design/network/datashts/82551ER_ds.htm)
- Intel® E7520 Chipset Datasheet: Intel E7520 Memory Controller Hub (MCH) (http://www.intel.com/design/chipsets/embedded/docs/e7520.htm)
- Intel® Boot Agent. (http://www.intel.com/support/network/adapter/pro100/bootagent/manual.htm)

- Intel NetStructure® MPCHC0001 14U Shelf Technical Product Specification (http://www.intel.com/design/network/products/cbp/atca/MPCHC0001.htm)
- Intel NetStructure® MPCMM0001 Chassis Management Module Hardware Technical Product Specification (http://www.intel.com/design/network/products/cbp/atca/mpcmm0001.htm)
- Intel NetStructure® MPCMM0001 Chassis Management Module Software Technical Product Specification (http://www.intel.com/design/network/products/cbp/atca/mpcmm0001.htm)
- Intel's AdvancedTCA product line (http://developer.intel.com/technology/atca/)
- Intelligent Platform Management Interface v1.5 Specification (http://developer.intel.com/design/servers/ipmi/spec.htm)
- Intelligent Platform Management Interface Implementer's Guide (http://developer.intel.com/design/servers/ipmi/spec.htm)
- ITP700 Debug Port Design Guide (http://www.intel.com/design/xeon/documentation.htm)
- Low Pin Count (LPC) Interface Specification (http://www.intel.com/design/chipsets/industry/lpc.htm)
- Low Voltage Intel® Xeon™ Processor Datasheet (http://www.intel.com/design/xeon/documentation.htm)
- Low Voltage Intel® Xeon™ Processor Product Page (http://www.intel.com/products/server/processors/server/xeon/index.htm?iid=ipp_srvr_proc+xeon512kb&)

1 Introduction

Document Organization

This document provides technical specifications related to the ATCA-4200 Computer Processing Module (CPM). The ATCA-4200 design follows the standards of the Advanced Telecommunications Computing Architecture (AdvancedTCA*). This document is intended for support during system product development and while sustaining a product. It specifies the architecture, design requirements, external requirements, board functionality, and design limitations of the ATCA-4200 module.

The following summarizes the focus of each section in this document.

Chapter 1, "Introduction" gives an overview of the information contained in the ATCA-4200 Technical Product Specification as well as a glossary of acronyms and important terms.

Chapter 2, "Feature Overview" introduces key features of the ATCA-4200.

Chapter 3, "Operating the Unit" provides specifics for configuring the ATCA-4200, including BIOS configuration and jumper settings.

Chapter 4, "Connectors and LEDs" includes an illustration of LEDs, connector locations, connector descriptions, and pinout tables.

Chapter 5, "Hardware Management Overview" provides a high-level overview of the IPMI implementation based on the PICMG* 3.0 and IPMI 2.0 specifications.

Chapter 6, "Specifications" contains the mechanical, environmental, and reliability specifications for the ATCA-4200.

Chapter 8, "BIOS Features" provides an introduction to the Intel/AMI BIOS and the System Management BIOS stored in flash memory on the ATCA-4200 module.

Chapter 9, "BIOS Setup" describes the interactive menu system of the BIOS Setup program, which allows users to configure the BIOS for a given system.

Chapter 10, "BIOS Errors and Checkpoints" lists BIOS error messages, Port 80h POST codes, and bus initialization checkpoints and provides a brief description of each.

Reference Documents on page 8 lists other documents that are relevant to this TPS.

Appendix A, "List of Supported Commands (IPMI v1.5 and PICMG 3.0)" lists all the supported IMPI commands.

Glossary

For ease of use, numeric entries are listed first with alpha entries following. Acronyms and terms are then entered in their respective place.

ACPI	Advanced Configuration and Power Interface.
AdvancedTCA	Advanced Telecommunications Computing Architecture
BIOS	Basic Input/Output Subsystem. ROM code that initializes the computer and performs some basic functions.
Blade	An assembled PCB card that plugs into a chassis.
DIMM	Dual Inline Memory Module. Small card with memory on it used for ATCA-4200.
DMI	Desktop Management Interface
ECC	Error Correcting Code
EEPROM	Electrically Erasable Programmable Read-Only Memory
Fabric Board	A board capable of moving packet data between Node Boards via the ports of the backplane. This is sometimes referred to as a switch.
Fabric Slot	A slot supporting a link port connection to/from each Node Slot and/or out of the chassis.
FPGA	Field Programmable Gate Array
FRB	Fault Resilient Booting.
FWH	Firmware Hub
GPIO	General Purpose I/O
Hyper-Threading Technology† (HT Technology)	Allows a single (or dual) physical processor, to appear as two (or quad) logical processors to an HT Technology-aware operating system.
I^2C*	Inter-IC (Integrated Circuit). 2-wire interface commonly used to carry management data.
IBA	Intel® Boot Agent. The Intel Boot Agent is a software product that allows your networked client computer to boot using a program code image supplied by a remote server.
ICH	I/O Controller Hub
IDE	Integrated Device Electronics. Common, low-cost disk interface.
IPMB	Intelligent Platform Management Bus. Physical 2-wire medium to carry IPMI.
IPMC	Intelligent Platform Management Controller. ASIC in baseboard responsible for low-level system management.
IPMI	Intelligent Platform Management Interface. Programming model for system management.

KCS	Keyboard Controller Style interface.
LPC Bus	Los Pin Count Bus. Legacy I/O bus that replaces ISA and X-bus. See the Low Pin Count (LPC) Interface Specification.
MCH	Memory Controller Hub
MTBF	Mean Time Between Failures. A reliability measure based on the probability of failure.
NEBS	National Equipment Building Standards. Telco standards for equipment emissions, thermal, shock, contaminants, and fire suppression requirements.
NMI	Non-Maskable Interrupt. Low-level PC interrupt.
Node Board	A board capable of providing and/or receiving packet data to/from a Fabric Board via the ports of the networks. The term is used interchangeably with ATCA-4200 module.
ATCA-4200	Single Board Computer module with Dual Intel® Xeon® M 2.8 GHz processor
Node Slot	A slot supporting port connections to/from Fabric Slot(s). A Node slot is intended to accept a Node Board
Physical Port	A port that physically exists. It is supported by one of many physical (PHY) type components.
PMC	PCI Mezzanine Card. IEEE1386 standard for embedded PCI cards. They mount parallel to the ATCA-4200.
POST	Power On Self Test
ROM	Read-Only Memory.
RTM	Rear Transition Module.
SBC	Single Board Computer. This term is used interchangeably with Node Board.
SEL	System Event Log. Action logged by management controller.
SFP	Small Form Factor Pluggable receptacle for the front panel Fibre Channel* interfaces.
SMBus	System Management Bus. Similar to I^2C.
SMI	System Management Interrupt. Low-level PC interrupt which can be initiated by chipset or management controller. Used to service IPMC or handle things like memory errors.
SMS, SMSC	Standard Microsystems Corporation*
SoL	Serial Over LAN
USB	Universal Serial Bus. General-purpose peripheral interconnect, operating at 1–12 Mbps. The newer Hi-Speed USB operates at up to 480 Mbps.

2 Feature Overview

Application

The AdvancedTCA* standards define open architecture modular computing components for a carrier-grade communications network infrastructure. The goals of these standards are to enable blade-based modular platforms to be:

- Cost effective
- High-density
- Highly available
- High Performance
- Scalable

These modular platform systems use a fabric I/O network for connecting multiple, independent processor boards, I/O nodes (e.g., line cards), and I/O devices (e.g., storage subsystem).

The ATCA-4200 module is designed according to the AdvancedTCA Design Guide for High Availability, Switched Network Computing.

Functional Description

This section defines the architecture of the ATCA-4200 through descriptions of its functional blocks. Figure 1 shows the functional blocks of the ATCA-4200. The ATCA-4200 is a hot-swappable module with backplane connections to Gigabit Ethernet (GbE) ports on the base and fabric interface. Implementation is based on option 2 of the PICMG 3.1 Specification.

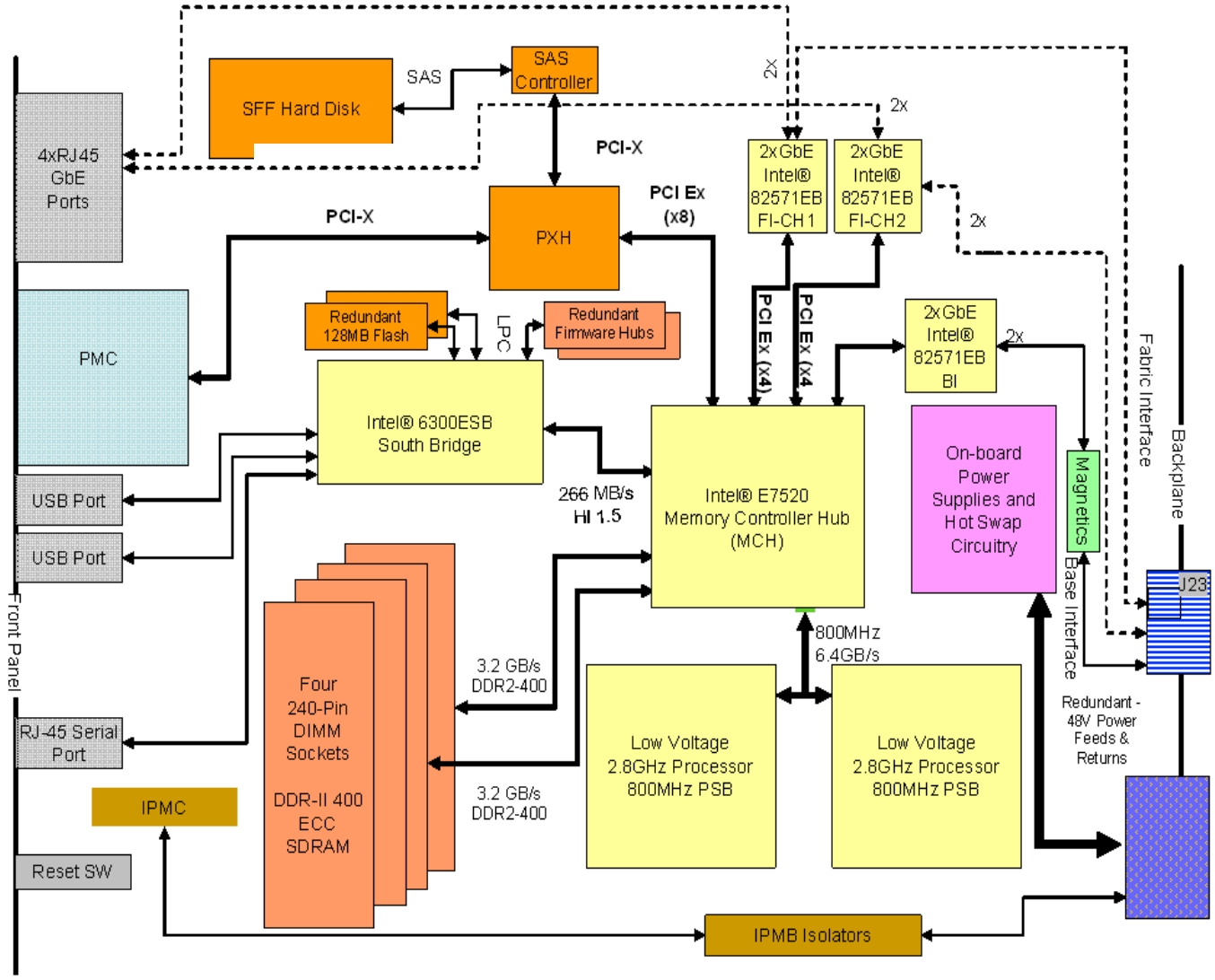
For storage, the ATCA-4200 module itself also supports Serial Attached SCSI (SAS) small form factor (SFF) hard disk and redundant (two) IDE (ATA) flash disks of 128 MBytes each for user applications.

The ATCA-4200 incorporates an Intelligent Platform Management Controller (IPMC) that monitors critical functions of the board, responds to commands from the shelf manager, and reports events.

Power is supplied to the ATCA-4200 through two redundant -48 V power feed connections. Power for on-board hardware management circuitry is provided through a standby converter on the power management circuitry. This converter, along with all the other converters on the power mezzanine, is fed by the diode OR'd -48 V redundant feeds from the backplane.

The ATCA-4200 provides for the addition of one PMC device and also offers two USB ports and one serial console interface on the front panel.

Figure 1. ATCA-4200 CPM Block Diagram



64-Bit Low Voltage Intel® Xeon™ Processor, 2.8GHz with 1 MB L2 Cache and an 800 MHz System Bus (U20,U37)

The ATCA-4200 supports dual 64-bit low voltage Intel® Xeon™ processors at 2.8GHz with 1 MB of L2 Cache and an 800 MHz System Bus. This processor is designed for high-performance. Based on the Intel® NetBurst™ microarchitecture and Hyper-Threading Technology, it is binary-compatible with previous Intel® Architecture (IA-32) processors.

Low voltage Xeon processors require their package case temperatures to be operated below the absolute maximum specification. If the chassis ambient temperature exceeds a level where the processor thermal cooling subsystem can no longer maintain the specified case temperature, the processors automatically enter a mode called Thermal Monitor to reduce their case temperatures. Thermal Monitor controls the processor temperature by modulating the internal processor core clocks and reducing internal power dissipation. This mode does not require any interaction by the operating system or application. Once the case temperatures have reached a safe operating level, the processor returns to its non-modulated operating frequency.

See the 64-Bit Low Voltage Intel Xeon Processor datasheet, referenced in *Reference Documents* on page 8, for further details.

Chipset

The ATCA-4200 uses a chipset with the following major components:

- Intel® E7520 Memory Controller Hub (MCH)
- Intel® 6300ESB I/O Controller Hub (ICH)
- Intel®6700PXH 64-bit PCH Hub (PXH)

A brief overview of each of these components is provided here and detailed information can be found in each device's documentation.

E7520 MCH (U28)

The architecture of the Intel® E7520 Memory Controller Hub (MCH) provides the performance and feature set required for performance servers, with configuration options that facilitate optimization of the platform for workloads characteristic of communication, presentation, storage, performance computation, or database applications. To accomplish this, the MCH has numerous Reliability, Availability, Serviceability, Usability and Manageability (RASUM) features on multiple interfaces.

The front side bus supports a base system bus frequency of 200 MHz. The address and request interface is double-pumped to 400 MHz and the 64-bit data interface (+ parity) is quad-pumped to 800 MHz. This setup provides a matched system bus address and data bandwidths of 6.4 GB/s. The MCH provides an integrated memory controller for direct connection to registered DDR2-400 memory.

The MCH is compatible with the PCI Express* Interface Specification, Rev 1.0a. The MCH provides three configurable x8 PCI Express interfaces, each with a maximum

theoretical bandwidth of 2 GBytes in each direction. The MCH supports PCI Express Hot Swap. The MCH is a root class component, as defined in the *PCI Express Interface Specification, Rev1.0a*.

The MCH interfaces with the Intel® 6300ESB I/O Controller Hub (ICH) through a dedicated Hub Interface 1.5 link that supports a peak bandwidth of 266 MByte/s by using an x4 base clock of 66 MHz with parity protection.

Table 1 shows the PCI Express port mapping:

Table 1. PCI Express Port Mapping

Port	Function
A0	Connects to base interface gigabit Ethernet controller, 82571 (U34)
A1	Not used
B0	Connects to fabric interface gigabit Ethernet controller, 82571 (U68, Channel 1, Ports 0 & 1)
B1	Connects to fabric interface gigabit Ethernet controller, 82571 ((U69, Channel 2, Ports 0 & 1))
C0/C1	Connects to 6700PXH PCI hub (U18) for PCI-X

6300ESB I/O Controller Hub (U40)

The 6300ESB ICH provides legacy function support similar to that of previous ICH-family devices, but with extensions in Serial-ATA technology and 64-bit/66 MHz PCI-X support. The 6300ESB ICH also includes integrated USB 2.0 and USB 1.0 support, an LPC interface, a system management interface, a power management interface, integrated IOxAPIC and 8259 interrupt controllers, and an integrated DMA controller.

6700PXH 64-Bit PXH Hub (U18)

The 6700PXH 64-bit PXH hub provides the connection between a PCI Express interface and two independent PCI bus interfaces that are configurable for standard PCI 2.3 protocol, as well as the enhanced high-frequency PCI-X 1.0b protocol. The PXH provides configurable support for 32- or 64-bit PCI devices.

An SAS controller and one PMC card (64-bit/100 MHz) are connected to the PXH to maximize data throughput.

Table 2. PXH Interfaces

PXH Device	Interface
LSI SAS Controller	PCI-X A LSI SAS Controller (U6), bus running 64-bit, 133 MHz, PCI-X mode
PMC Interface	PCI-X B interface to PMC carrier (64-bit, 100 MHz)

Memory (U5,U12,U15,U17)

The memory subsystem is designed to support Double Data Rate2 (DDR2) Synchronous Dynamic Random Access Memory (SDRAM) using the E7520 MCH. The MCH provides two independent DDR channels, which support DDR2-400 DIMMs. The peak bandwidth of each DDR2 branch channel is 3.2 GByte/s (8 Bytes x 400 MT/s) with DDR2-400. The two DDR2 channels from the MCH operate in lock step, making the effective overall peak bandwidth of the DDR2 memory subsystem 6.4 GByte/s for DDR2-400. Four 25-degree, 240-pin DIMMs support memory configuration up to 16 GB of PC2-3200 registered DDR2-400 SDRAM.

Note
DIMM modules must be no taller than 1.125 inches, accounting for the angle of the DIMMs and clearence to the cover and other components on the ATCA-4200, to comply with AdvancedTCA specifications.

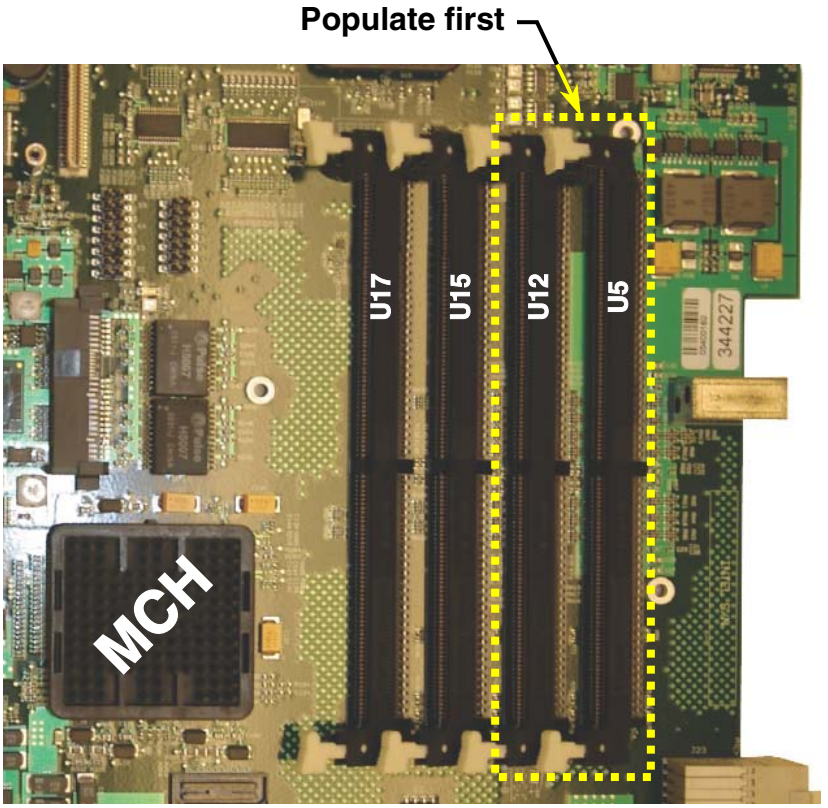
Memory Ordering Rule for the MCH

Table 3. Supported Memory Configuration

Total Memory	U5	U12	U15	U17
2 GBytes	1 GByte DIMM	1 GByte DIMM		
4 GBytes	1 GByte DIMM	1 GByte DIMM	1 GByte DIMM	1 GByte DIMM
4 GBytes	2 GByte DIMM	2 GByte DIMM		
8 GBytes	2 GByte DIMM	2 GByte DIMM	2 GByte DIMM	2 GByte DIMM
8 GBytes	4 GByte DIMM	4 GByte DIMM		
16 GBytes	4 GByte DIMM	4 GByte DIMM	4 GByte DIMM	4 GByte DIMM

The ATCA-4200 components can address up to 16 GB of memory. The board provides an integrated memory controller for direct connection to two channels of registered memory utilizing DDRII-400 memory modules. The board has four DIMM sockets and can physically hold up to four sticks of memory modules. The ATCA-4200 supports single-channel operation using either of its memory channels. When both DDR channels are populated and operating, they function in lock-step mode. The DIMM modules must be populated as pairs (identical modules) to run in dual-channel mode. When not populated as pairs (identical modules), the MCH only runs in single-channel mode. The ATCA-4200 can support up to four DIMM modules of 1 GB, 2 GB, or 4 GB registered DDR-2 DRAM with ECC modules. The recommended order for installing the memory modules is starting from the DIMM socket at U5 first, then followed by U12, U15, and U17 as the last socket. (See Figure 2 for these locations.)

Figure 2. Memory Ordering



I/O Interface

Real-Time Clock

The ATCA-4200 real-time clock is integrated into the ICH. It is derived from a 32.768 KHz crystal with the following specifications:

- Frequency tolerance @ 25° C: ± 20 ppm
- Frequency stability: maximum of -0.04 ppm/$(\Delta^{\circ}C)^2$
- Aging $\Delta F/f$ (first year @ 25° C): ± 3 ppm
- ± 20 ppm from 0-55° C and aging 1 ppm/year

The real-time clock is powered by a 0.47 F SuperCap* capacitor when main power is not applied to the board. This capacitor powers the real-time clock for a minimum of 10 hours while external power is removed from the ATCA-4200.

Timers

The 6300ESB ICH provides three timers. The three timers are implemented as a single counter, with each timer having its own comparator and value register. Each timer's counter increases monotonically. Each individual timer can generate an interrupt when the value in its value register matches the value in the main counter. Some of the timers may be enabled to generate a periodic interrupt.

The registers associated with these timers are mapped to a memory space (much like the I/O APIC). However, the implementation is not as a standard PCI function. The BIOS reports the location of the register space to the operating system. The hardware may support an assignable decode space, but the BIOS sets this space prior to handing it over to the OS. The OS is not expected to move the location of these timers once it is set by the BIOS.

One timer block is implemented in the 6300ESB ICH. The timer block has one counter and three timers (comparators). Various capability registers indicate the number of timers and the capabilities of each.

Timer Accuracy

The timers are accurate over any 1 ms period to within 0.005% of the time specified in the timer resolution fields. Within any 100 ms period, the timer will report a time that is up to two ticks too early or too late. Each tick is less than or equal to 100 ns, so this range represents an error of less than 0.2%. The timer is monotonic. It will not return the same value on two consecutive reads (unless the counter has rolled over and reached the same value). The main counter is clocked by the 14.31818 MHz clock, synchronized into the 66.666 MHz domain. This results in a non-uniform duty cycle on the synchronized clock, but the average period is correct. The main counter is as accurate as the 14.3818 MHz clock.

Gigabit Ethernet (U34 for Base Interface, U76 and U77 for Fabric Interface)

The ATCA-4200 implements six Gigabit Ethernet (GbE) interfaces from three separate GbE controllers (82571EBs). Two of these interfaces are routed to the base interface, and the other four are routed to the fabric interface on the backplane to support the PICMG* 3.0 and 3.1 option 2 specifications.

Users have the option of routing the fabric interface GbE ports by pairs to RJ-45 on the front panel by using a BIOS setting.

USB 2.0

The ATCA-4200 has two horizontal USB connectors that support USB 2.0 and 1.1.

USB supports Plug and Play* and Hot Swapping operations (OS level) that allow USB devices to be automatically attached, configured, and detached without rebooting.

Serial Ports

The ATCA-4200 supports one serial port and is software compatible with NS16C550. Serial port 1 is routed to the front panel RJ-45 connector for normal operation.

PMC Connector

The ATCA-4200 supports one 64-bit, 100MHz PMC slot connected to the Intel® 6700PXH bridge.

The PMC slot has an opening in the front panel of the ATCA-4200 that exposes the I/O connectors of the add-in PMC card. PMC cards can only be added to or removed from this slot when the board is outside the system chassis.

See Table 10 through Table 12 in Chapter 4, "Connectors and LEDs" for pin definitions.

The PCI bus specification provides the means for backward compatibility with slower PMC cards (32-bit or 33 MHz) through the use of the M66EN pin. A PMC card that does not support 66 MHz operation should have the M66EN pin set to Ground when it is installed to inform the ATCA-4200 hardware to provide a 33 MHz clock to this interface. Support for 32-bit only PMC cards is accomplished through the use of the REQ64#/ACK64# PCI bus protocol.

The PMC slot provided by the ATCA-4200 connects the PCI VI/O voltage pins to +3.3 V. This requires use of PMC plug-in cards that support +3.3 V I/O signal levels. Only PMC plug-in cards designated “+3.3 V only” or “universal” voltage I/O are supported. The PMC plug-in location provides a key pin to prevent insertion of cards that do not meet this requirement. Note that +5 V power is still supplied to the PMC pins designated for +5 V connections.

Firmware Hubs (U24, U23)

The ATCA-4200 supports two 8-Mbit (1 MByte) BIOS flash ROMs:

- Primary BIOS flash ROM (FWH0)
- Recovery BIOS flash ROM (FWH1)

The flash is allocated for storing the BIOS binary code.

The ATCA-4200 boots from the primary flash ROM under normal circumstances. During the boot process, if the BIOS (or IPMC) determines that the content of the primary flash ROM is corrupted, an IPMI command is available to change the flash device select logic to use the recovery flash ROM.

Flash ROM BIOS updates can be performed by an end user or a network administrator over the LAN. The system should complete booting with Linux* and logging on as root user. The system should have a local copy of the flash program and the BIOS data files or have the capability to copy the flash program and BIOS data files onto a local drive over the network. The flash program has a command line interface to specify the path and the file name of the BIOS data files. After completing the BIOS ROM update, the user should shutdown and reset the system for the new BIOS ROM to take effect.

See *BIOS Configuration* on page 27, for more information about updating the BIOS.

Firmware Hub 0 (Main BIOS) (U24)

The BIOS executes code off of the flash ROM and performs a checksum validation of its operational code. This checksum occurs in the boot block of the BIOS. The BIOS image is also stored in FWH0. When the user performs a BIOS update, the BIOS image is stored in FWH0 only. FWH0 will also store the factory default CMOS settings and user-configured CMOS settings.

Firmware Hub 1 (Backup/Recovery BIOS) (U23)

FWH1 stores the recovery BIOS. In the event of checksum failure on the main BIOS operational code, the BIOS will request the IPMC to switch firmware hubs, so that the board is able to boot from FWH1 for recovery.

Flash ROM Backup Mechanism

The on-board Intelligent Platform Management Controller (IPMC) manages which of the two BIOS flash ROMs is used during the boot process. The IPMC monitors the boot progress and can change the flash ROM selection and reset the processor.

The default state of this control configures the primary Firmware Hub (FWH) ROM device ID to be the boot device; the secondary FWH is assigned the next ID. The secondary FWH responds to the address range just below the primary FWH ROM in high memory.

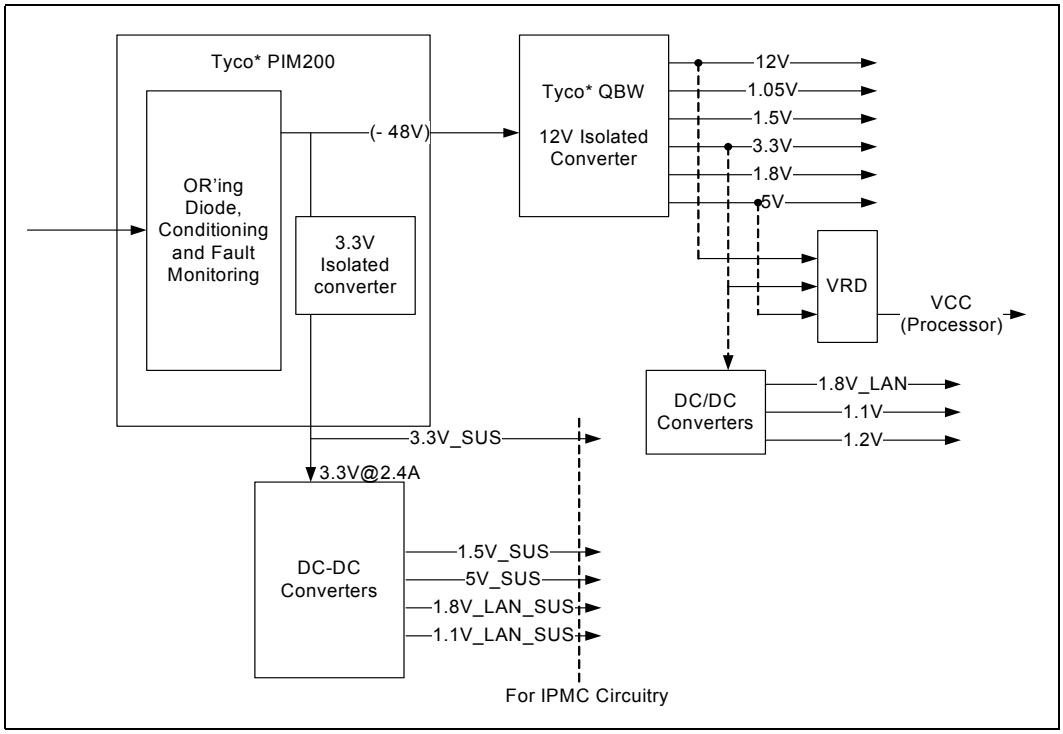
The IPMC sets the ID for both FWH devices. Boot accesses are directed to the FWH with ID = 0000; unconnected ID pins are pulled low by the FWH device. In this way the IPMC may select which flash ROM is used for the boot process.

On-board Power Supplies

The main power supply rails on the ATCA-4200 are powered from dual-redundant -48 V power supply inputs from the backplane power connector (P10). There are also dual redundant, limited current, make-last-break-first (MLBF) power connections.

Figure 3 shows the high-level power distribution on the CPM.

Figure 3. Power Conversion



As required by the PICMG 3.0 Specification, the ATCA-4200 provides fuses on each of the-48 V power feeds and on the RTN connections as well. The fuses on the return feeds are critical to prevent overcurrent situations if an ORing diode in the return path fails and there is a voltage potential difference between the A and B return paths.

A Power Input Module (Tyco* PIM200) is used to interface directly to the chassis power feeds.

The main features of the PIM are listed below:

- Provide 200 W of isolated -12 VDC.
- Inrush current limiting (per the PICMG 3.0 specification).
- Isolated Management Power Output, 8 W of 3.3 VDC for IPMC circuitry.
- ORing function for Feed A and B and their returns.
- EMI filtering for conducted emissions.
- 72 VDC charging current for external holdup storage capacitors to meet the holdup requirement in the PICMG 3.0 specifications.
- Feed A and B loss alarms.

3.3 V Isolated Converter

A 3.3 V sustaining voltage is provided by the Tyco PIM module. This voltage is used to generate the other required sustaining voltages. They are 1.5/5 V for the ICH and 1.8 V/1.1 V for the base interface GbE controller. The sustaining voltages are always enabled.

When the board is in M1 state, no more than 10 W is drawn from the -48 V input (as specified in PICMG 3.0). All other outputs are enabled under IPMC control.

Current values here indicate the maximum that can be delivered by design and do not reflect the current actually provided on the ATCA-4200.

12 V Isolated Converter

The Tyco QBW power brick performs the -48 V to 12 V isolation conversion. It is an industry standard quarter brick that is capable of delivering up to 18 A of output current with high efficiency.

Processor Voltage Regulator Down (VRD)

The Voltage Regulator Down (VRD) provides core power to the processor. The input to the VRD is connected to the 5 V, 3.3 V, and 12 V power rails.

The VRD controller is designed to support the processor core voltages selected by the voltage identification (VID) pins on the processor. `The voltage regulator module is designed to support up to 27 A.

IPMC Standby Power

The IPMC circuitry is powered by the sustaining voltages (5V_SUS, 3.3V_SUS, 1.5V_SUS), and is operational before the rest of the components power up.

Intelligent Platform Management Controller (U79)

For its IPMC, the ATCA-4200 uses an Intel-designed baseboard management controller device manufactured by Philips Semiconductor* for Intel. Please refer to Chapter 5 “Hardware Management Overview” for more detail on the IPMC operation.

Application Flash Disks

The board is equipped with dual 128-MB IDE (ATA) flash disks. User can utilize these dual flash disks to store recovery OS, application, diagnostics software, and network configuration files.

Serial Attached SCSI Controller (UJ7)

The ATCA-4200 includes a four-port Serial Attached SCSI (SAS) controller. The controller is connected to the PCI-X bus of the PXH6700. All ports have a serial point-to-point interface using a differential transmit/receive pair. The device has a flash device to store the firmware of the controller itself. The first port (Port 0) is connected to the on-board SAS carrier port, the other three ports are not connected.

Compliance

The ATCA-4200 product conforms to the following specifications:

- PICMG 3.0 R1.0 and ECN001 (AdvancedTCA Core Specification)
- PICMG 3.1 R1.0 (Ethernet/Fibre Channel over AdvancedTCA)
- PMC - IEEE 1386.1
- IPMI 1.5 (Intelligent Platform Management Interface)

3 Operating the Unit

BIOS Configuration

In most cases, the BIOS defaults will provide the correct configuration for using the board. See Chapter 9, "BIOS Setup", for a complete list of BIOS options if you need to modify to the default BIOS options.

Remote Access Configuration

Console redirection to the serial port is enabled by default. This setting redirects the text output of the BIOS and operating system to the RJ-45 serial port on the ATCA-4200 faceplate. The default settings are 115200, N, 8, 1 with no flow control. Use these terminal emulator settings to access the console data.

Boot Devices

The BIOS Setup program includes a choice of available boot devices, with each boot device having options for removable media (USB CD-ROM, USB flash disk, etc.), SAS hard drive, on-board IDE flash disks, or PXE boot through any of the six GbE adapters.

In every POST, the BIOS detects all available boot devices and displays them on the boot order screen, with the exception of the Intel® Boot Agent (IBA), which displays even if the LAN cable is disconnected.

The default settings are:

- 1st boot device: USB removable media (only if a USB device is present)
- 2nd boot device: Primary Master - 128 MByte ATA flash disk
- 3rd boot device: Secondary Master - 128 MByte ATA flash disk
- 4th boot device: SAS drives

Booting from an SAS Hard Disk

By default, the SAS hard disk is the fourth boot device under the Hard Disk Drives boot priority list (if a USB device is present). The BIOS will attempt to boot any OS image from the hard disk.

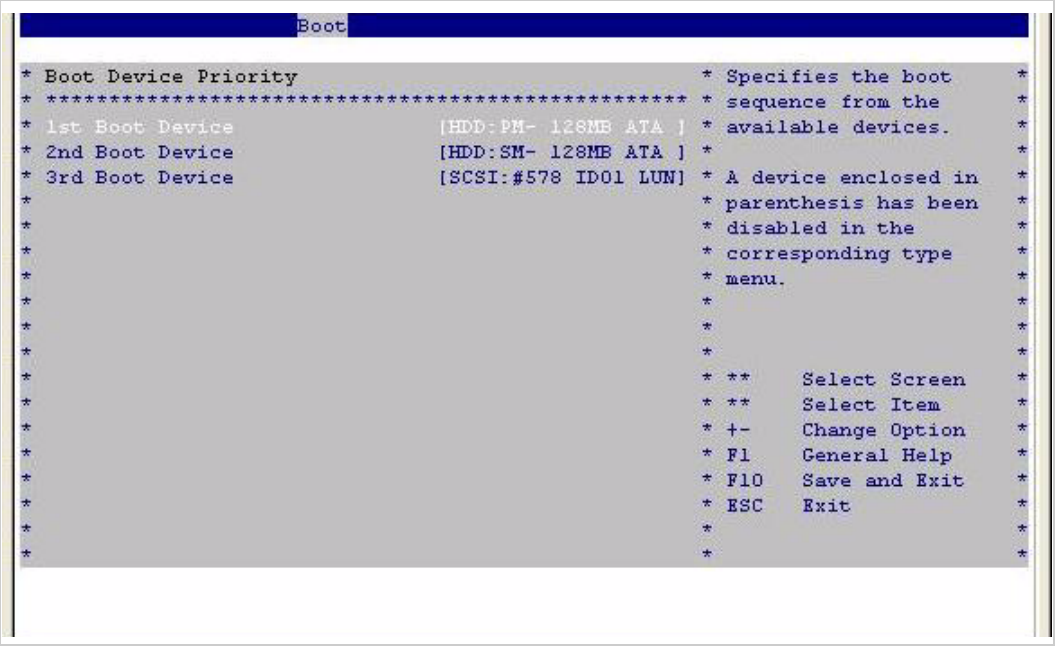
Booting from a 128 MByte ATA Flash Disk (On-board)

By default, the flash disks (Flash 0 and Flash 1) are the second and third boot device respectively in the Hard Disk Drives boot priority list.

To configure a 128-MByte ATA flash disk as the first boot device, follow this procedure:

1. Press "DEL" or "F4" (remote console) during system boot to enter the BIOS Setup utility.
2. In the Setup utility, select "BOOT" from the menu bar.
3. Go to the "Hard Disk Drives" list and click "Enter".
4. To enable the board to boot from Flash 0, go to the first drive, click "Enter", and scroll down to "HDD: PM - 128 MB ATA Flash Disk". Click "Enter". (See Figure 4.)

Figure 4. Booting from PATA Flash ROM



Booting from USB Removable Media

If a USB flash disk or USB floppy drive is connected to the board during boot up, the BIOS detects the disk and it appears as the first boot device on the BIOS Setup menu.

If the disk is non-bootable, the BIOS attempts to boot from the next boot device as configured in the Boot Device Priority list.

Booting from a LAN (PXE Boot)

Any of the six on-board Gigabit Ethernet LAN connectors on the base and fabric interfaces can be used for the remote boot process. You will need to set up a PXE boot server that stores the Linux image. (Details on how to set up a PXE boot server are beyond the scope of this document.) Remember to configure your boot device priority in the BIOS Setup utility to specify the GbE LAN adapter(s) as the top priority.

Software Updates

This section describes how to update the System BIOS and IPMC firmware on the ATCA-4200 module.

BIOS Image Updates

Periodically, new BIOS images will be released to add features or fix issues. These updates and utilities will be provided in a package on the support web site. The package will include the utilities and images, along with the latest installation instructions and release notes.

The BIOS may be updated using any of three methods, as described in the following sections:

- DOS*
- Linux (Interactive)
- Linux (Quiet Mode).

Note
See the Release Notes and instructions provided with the BIOS release for the latest information.

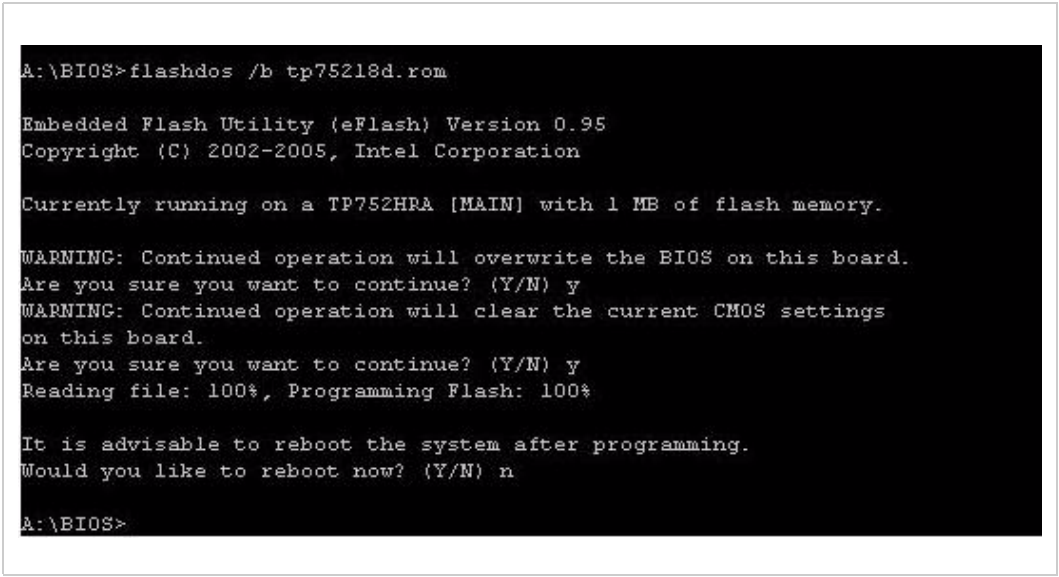
Updating the BIOS under DOS

Below is a step-by-step procedure to update the BIOS under MS-DOS*.

1. Copy the flash utility (Flashdos.exe) and the TPxxxxxx.rom file to an DOS-bootable floppy disk or USB flash drive.
2. Boot the board from a USB floppy disk/USB flash drive (connected to a USB port) to a DOS prompt.
3. Issue the command "flashdos /b TPxxxxxx.ROM".
4. Enter "Y" to overwrite the BIOS on the board.
5. Enter "Y" to clear the current CMOS settings on the board.
6. Enter "Y" to reboot the system after the BIOS has been upgraded successfully.

Figure 5 shows an example of the screen display for steps 3 through 6.

Figure 5. Updating the BIOS under MS-DOS



Updating the BIOS under Linux (Interactive mode)

This method requires user intervention. Below is a step-by-step procedure to update the BIOS under MontaVista* Linux.

1. Copy the flash utility (flashlnx) and the TPxxxxxx.rom file to the ATCA-4200 (via FTP/etc.)
2. Issue the command "./flashlnx -b TPxxxxxx.ROM".
3. Enter "Y" to overwrite the BIOS on the board.
4. Enter "Y" to clear the current CMOS settings on the board.
5. Enter "Y" to reboot the system after the BIOS has been updated successfully.

Updating BIOS under Linux (Quiet Mode)

The BIOS update utility supports quiet mode, where messages are not sent to the screen. This mode can be used for automatic (programmatic) invocations of the update utility.

To update the BIOS automatically without user intervention or responses to prompts, execute the following command: "./flashlnx -q -b TPxxxxxx.ROM".

Synchronizing BIOS Image and Settings from FWH0 (Main) to FWH1 (Backup)

Prior to upgrading the main BIOS (FWH0), you can create a mirror image to copy all the operational codes and CMOS settings to the redundant BIOS flash bank. This approach is suggested to ensure that you preserve a copy of the old BIOS image prior to updating the main BIOS.

The syntax "./flashlnx –m" or "flashdos -m" can be used to initiate this transfer. Refer the suggested method below in Table 4.

Table 4. Suggested Method of BIOS Image Synchronization Prior to BIOS Upgrade

BIOS Image	Command	Behavior
FWH0 FWH1		- This is the original FWH image before an upgrade. - FWH0 has a newer image than FWH1.
FWH0 FWH1	./flashlnx –m	User can initiate this during OS runtime prior to a BIOS upgrade. When command is executed, the FWH0 image (BIOS codes + CMOS settings) is synchronized to FWH1. No reboot is needed for this operation.
FWH0 FWH1	./flashlnx –b Pxx-xxxx	When this command is initiated, the FWH0 image will be updated to the latest version. The latest version of the BIOS will take effect after the user initiates a reset. If a checksum error is detected on FWH0 after a reboot, it will automatically switch to FWH1 and regain normal operation.

Legend

P0(x)	Current BIOS image before initiating an update.
P0(x-1)	Older BIOS image.
P0(x+1)	New BIOS image.

X = BIOS version.

IPMC Firmware Updates

IPMC firmware updates are covered in Chapter 5, "Hardware Management Overview". Each release of firmware also has complete installation instructions and Release Notes with the latest update information for that particular release.

Accessories

The ATCA-4200 allows for the use of onboard third-party hard disk drives and PMC devices. To mount these devices properly, use the accessory kit that is included with the board package.

The following items come in the accessory kit. (See Figure 6.)

- One bag
- For the hard disk drive:
  - Four M3 screws, 4 mm long, panhead
  - Four M3 screws, 4 mm long, countersunk
  - Two HDD mounting brackets
- For the PMC
  - Four M2.5 screws, 6 mm long, panhead
  - Two M2.5 standoffs, 6 mm long, male/female

Figure 6. Accessory Kit Contents



Onboard Hard Disk Drive Installation (Optional)

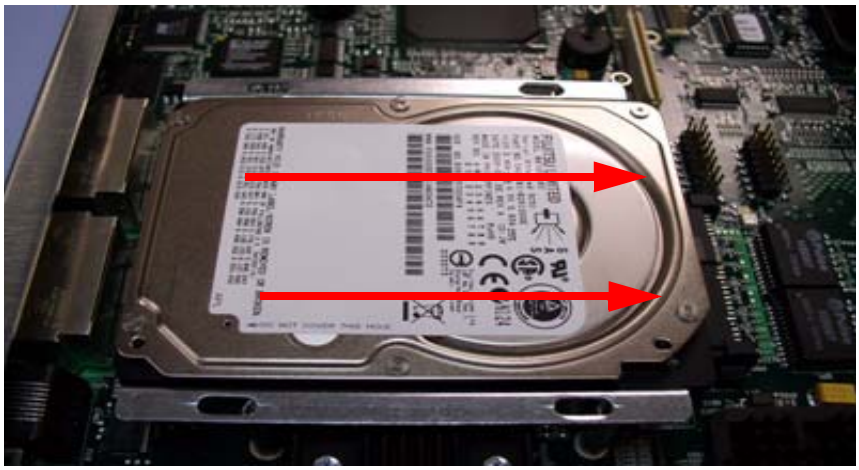
1. Check that the following accessories are available:
   - Four M3 screws, 4 mm long, panhead
   - Four M3 screws, 4 mm long, countersunk
   - Two HDD mounting brackets
   - SAS hard drive(s) (not shipped with the baseboard)
2. Attach the hard drive to the mounting cage with the 4 mm screws and tighten to 5 - 7 in-lbs. (Do not torque this over the limit above).

Figure 7. Attaching a Hard Drive to the HDD Mounting Cage



3. Place the mounting cage on top of the board. Align the hard drive connector with the on-board connector and slide the mounting cage from right to left to secure the connection.

Figure 8. Attaching a Hard Drive to the On-board Connector

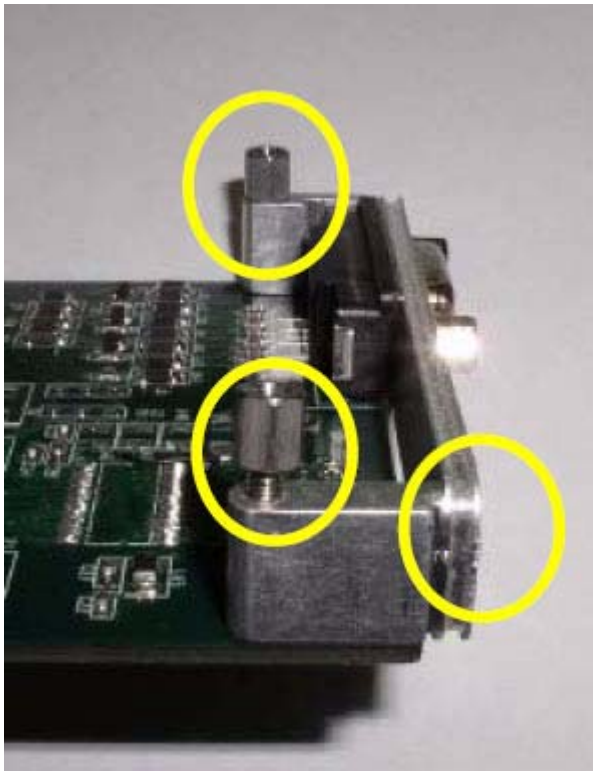


4. Align the screw holes on the mounting cage with the screw holes on the baseboard. Insert the 6 mm screws and tighten to 6 in-lbs.

PMC Installation (Optional)

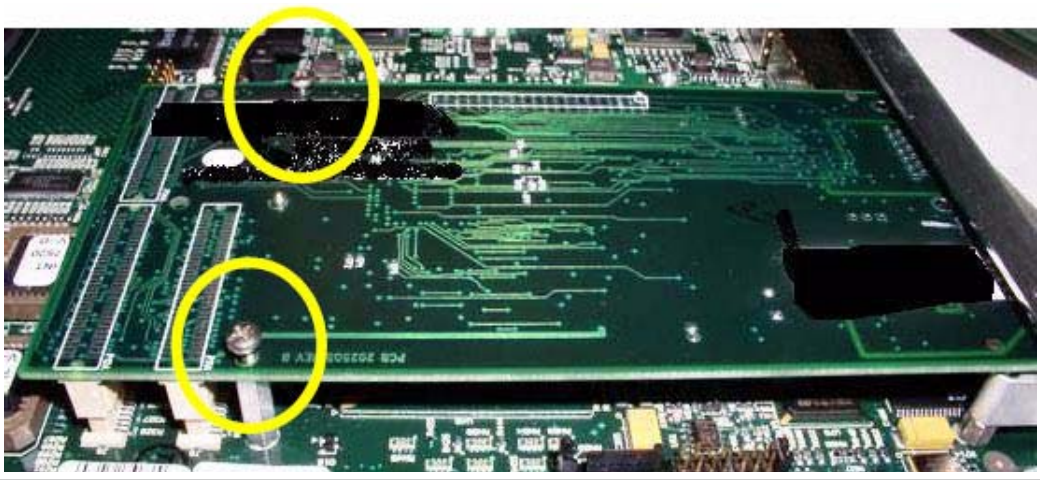
1. Check that the following accessories are available:
   - Four M2.5 screws, 6 mm long, panhead
   - Two M2.5 standoffs, 6 mm long, male/female
2. Attach the M2.5 standoffs to the PMC as shown in Figure 9 and tighten to 3 -5 in-lbs.

Figure 9. Attaching the PMC Standoffs



3. Insert the PMC on the ATCA-4200 board using two of the PMC M2.5 screws in the rear mounting posts as shown in Figure 10 and tighten to 3 - 5 in-lbs.

Figure 10. Mounting the PMC on the ATCA-4200 Board Using the Rear Mounting Posts



4. Turn the ATCA-4200 board over, insert the two remaining M2.5 mounting screws into the locations near the faceplate as shown in Figure 11, and tighten to 3 - 5 in-lbs.

Figure 11. Attaching the PMC with the Mounting Screws Near the ATCA-4200 Faceplate.



Digital Ground to Chassis Ground Connectivity

Location MH1 allows for the use of a metal standoff and metal screw to connect the bracket and digital GND. The default configuration is the population of a metal standoff with a plastic screw (Digital Ground isolated from Chassis Ground). A metal screw comes in the kit along with the board, leaving the end user the choice of whether of not to isolate.

Note
Digital ground is also called logic ground. Chassis ground is also known as shelf ground.

Figure 12. Digital Ground to Chassis Ground



4 Connectors and LEDs

Connectors along the rear edge of AdvancedTCA* server blades are divided into three distinct zones, as described in Section 2.3 of the PICMG 3.0 Specification:

- Zone 1 for system management and power distribution.
- Zone 2 for data fabric.
- Zone 3 for the rear transition module (RTM). RTMs are not used on ATCA-4200.

As shown in Figure 13, the ATCA-4200 module includes several connectors for interfaces with application-specific devices. Some of the connectors are available at the front panel as shown in Figure 14. The following sections contain pinouts and detailed descriptions for each connector.

Figure 13. Backplane and On-Board Connector/DIP Switch Locations

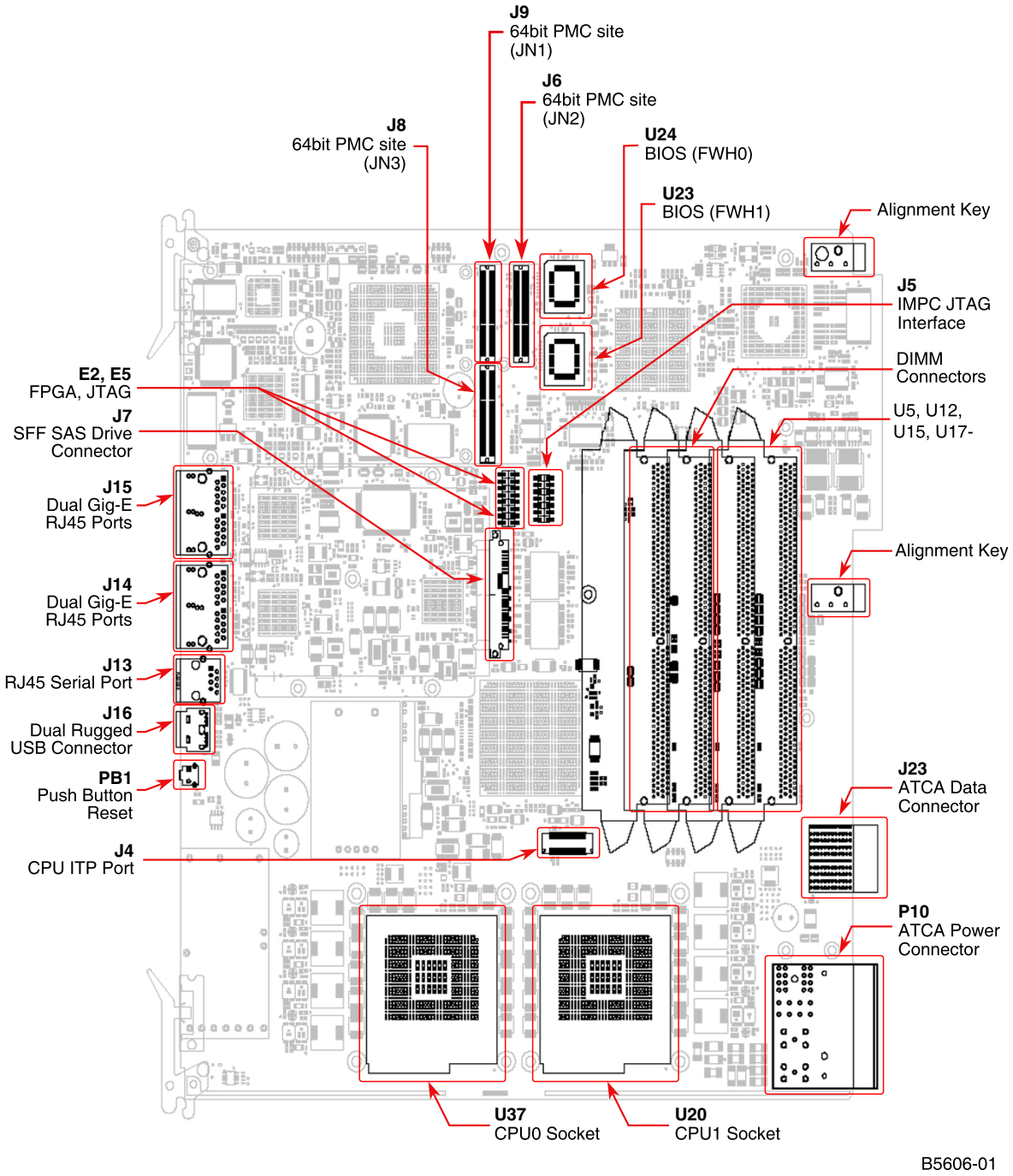


Table 5. Backplane and On-Board Connector Assignments

Connector	Description
P10	AdvancedTCA power and IPMB
J23	AdvancedTCA data transport for Base and Fabric interfaces (Zone 2)
J5	System Management Controller JTAG Connector
J4	CPU JTAG Connector
J9/J6/J8	PMC 1 connectors (JN1/JN2/JN3)
J7	Serial attached SCSI (SAS) hard disk connectors
J14/J15	Dual Port RJ45 Ethernet Connectors
J13	RJ45 Serial Port
J16	Dual Port USB Connector
MH1	Bracket GND to Digital GND Connectivity

Figure 14. Front Panel

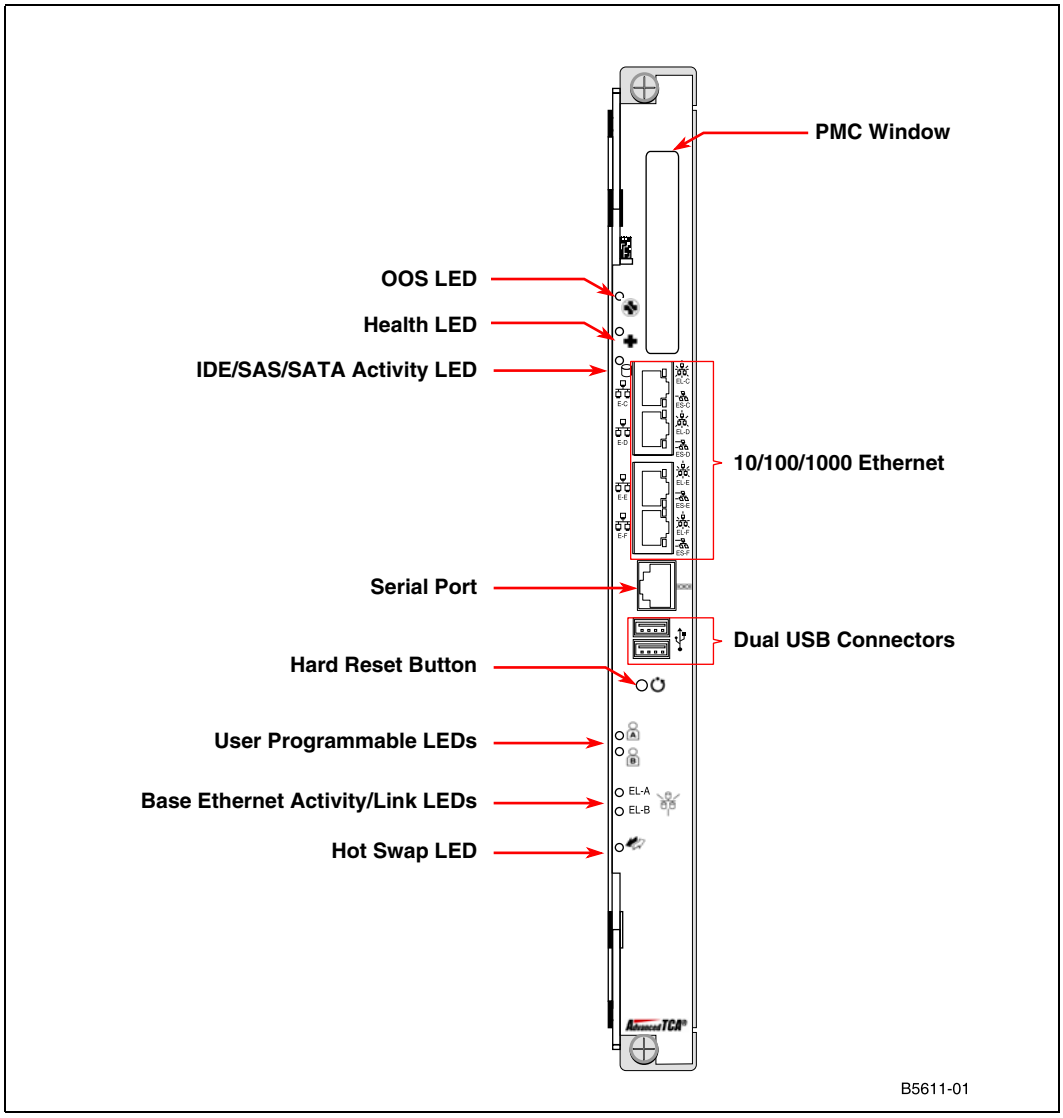


Table 6. Front Panel Connector Assignments

Connector	Description
J3	USB connector
J4	Serial Port connector
J8	RJ-45 10/100Mbps Ethernet connector

Backplane Connectors

Power Distribution Connector (P10)

The Zone 1 connector, P10, is a 34-pin Positronic* header that provides the following signals:

- Two -48 VDC power feeds (four signals each; eight signals total).
- Two IPMB ports (two signals each, four signals total).
- Geographic address (eight signals).
- Two ground pins.
- 12 unpopulated pins.

Figure 15 below shows the P10 connector. The pin assignments are given in Table 7.

Figure 15. Power Distribution Connector (Zone 1) P10

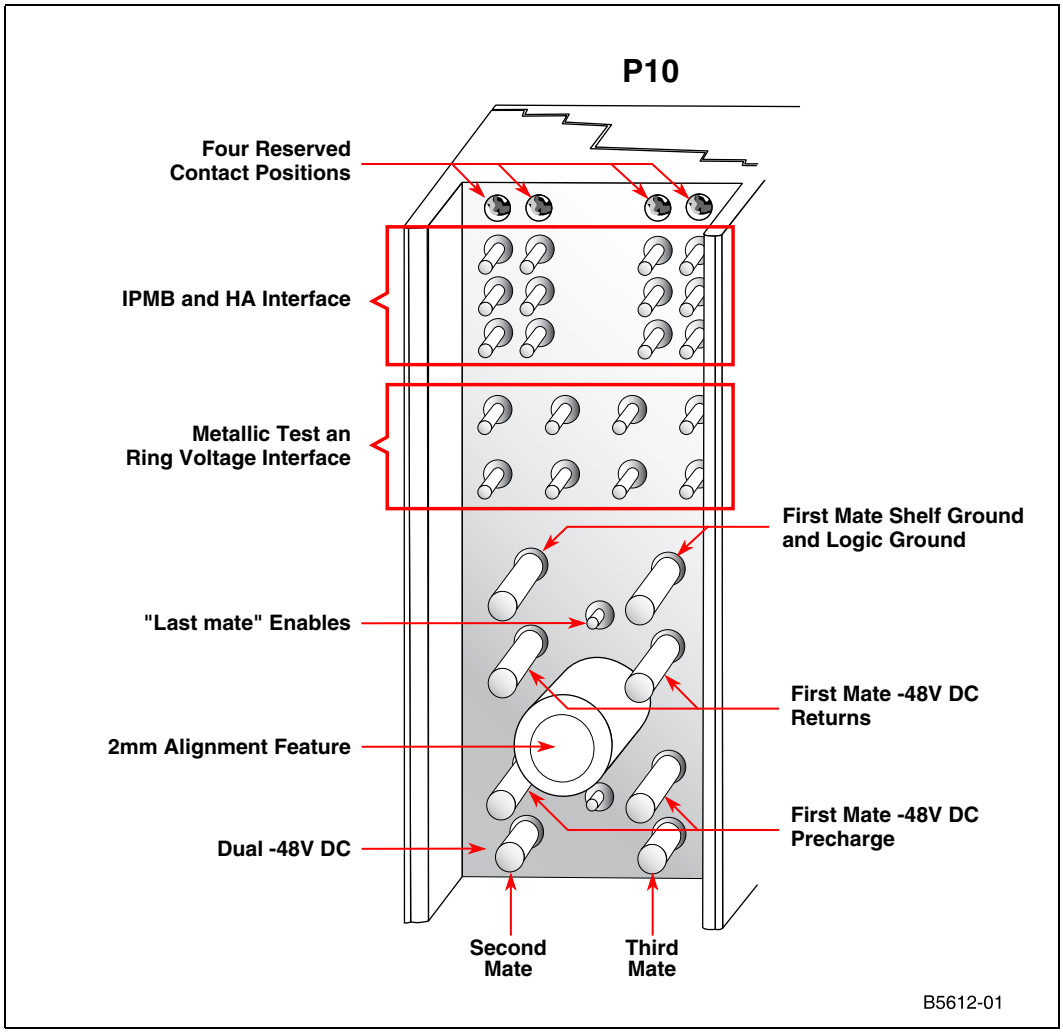


Table 7. Power Distribution Connector (Zone 1) P10 Pin Assignments

Pin	Signal	Description
1	NC	No Connection
2	NC	No Connection
3	NC	No Connection
4	NC	No Connection
5	GA0	Geographic Addr Bit 0
6	GA1	Geographic Addr Bit 1
7	GA2	Geographic Addr Bit 2
8	GA3	Geographic Addr Bit 3
9	GA4	Geographic Addr Bit 4
10	GA5	Geographic Addr Bit 5
11	GA6	Geographic Addr Bit 6
12	GA7/P	Geographic Addr Bit 7 (Odd Parity)
13	IPMB_CLK_A	IPMB Bus A Clock
14	IPMB_DAT_A	IPMB Bus A Data
15	IPMB_CLK_B	IPMB Bus B Clock
16	IPMB_DAT_B	IPMB Bus B Data
17	Unused	No Connection
18	Unused	No Connection
19	Unused	No Connection
20	Unused	No Connection
21	Unused	No Connection
22	Unused	No Connection
23	Unused	No Connection
24	Unused	No Connection
25	EMI_GND	EMI Chassis Ground
26	LOGIC_GND	Gnd Ref for Card Logic
27	ENABLE_B	Enb DC-DC conv, B Feed
28	VRTN_A	-48 V Return, Feed A
29	VRTN_B	-48 V Return, Feed B
30	Unused	No Connection
31	Unused	No Connection
32	ENABLE_A	Enb DC-DC conv, A Feed
33	-48V_A	-48 V Input, Feed A
34	-48V_B	-48 V Input, Feed B

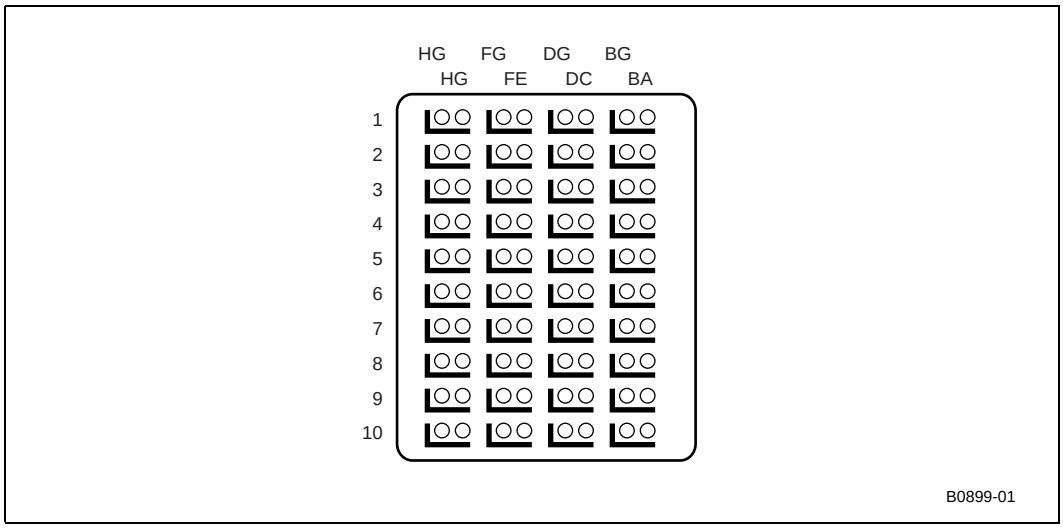
AdvancedTCA* Data Transport Connector (J23)

Zone 2 consists of one 120-pin HM-Zd connector, labeled J23, with 40 differential pairs. This data transport connector provides the following signals:

- Two 10/100/1000BASE-T Ethernet base channels (4 differential signal pairs each, 16 signals total).
- Four 1000BASE-BX Ethernet fabric channels (4 differential signal pairs each, 16 signals total).

Figure 16 shows a face view of the connector.

Figure 16. Data Transport Connector (Zone 2) J23



The BG, DG, FG, and HG (G for Ground) columns contain the ground shields for the four columns of differential pairs. They have been omitted from the pinout tables for simplification. All pins in the BG, DG, FG, and HG columns are connected to Logic Ground.

.

Table 8. AdvancedTCA Data Transport Connector (Zone 2) J23 Pin Assignments

Pin	A	B	C	D	E	F	G	H
1	No Connect	No Connect	Terminated	Terminated	No Connect	No Connect	Terminated	Terminated
2	F[2]Tx0+	F[2]Tx0-	F[2]Rx0+	F[2]Rx0-	F[2]Tx1+	F[2]Tx1-	F[2]Rx1+	F[2]Rx1-
3	No Connect	No Connect	Terminated	Terminated	No Connect	No Connect	Terminated	Terminated
4	F[1]Tx0+	F[1]Tx0-	F[1]Rx0+	F[1]Rx0-	F[1]Tx1+	F[1]Tx1-	F[1]Rx1+	F[1]Rx1-
5	BI_DA1+ (Tx1+)	BI_DA1- (Tx1-)	BI_DB1+ (Rx1+)	BI_DB1- (Rx1+)	BI_DC1+	BI_DC1-	BI_DD1+	BI_DD1-
6	BI_DA2 + (Tx2+)	BI_DA2- (Tx2-)	BI_DB1+ (Rx2+)	BI_DB1- (Rx2-)	BI_DC2+	BI_DC2-	BI_DD2+	BI_DD2-
7	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
8	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
9	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
10	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect

Fabric interface (Gigabit Ethernet) ports

Note

All "Terminated" pins are grounded on the baseboard as defined in the PICMG 3.1, Release 1.0 specification.

The following naming convention describes the signals on this connector. Signal direction is defined from the perspective of the ATCA-4200 module.

For the base interface, the bi-directional 10/100/1000BASE-T data signals have the following conventions:

- BI_Dr[c]p

  r = differential pair (A, B, C, or D)

  c = channel (1, 2)

  p = polarity (+, -)

For the Fabric Interface, the 1000BASE-BX data signals have the following conventions:

- F[c]dnp

  c = channel (1, 2)

  d = direction (Tx = Transmit, Rx = Receive)

  n = port number (0, 1)

  p = polarity (+, -)

A port is two differential pairs; one Tx and one Rx.

Alignment Blocks

The ATCA-4200 module implements the K1 and K2 alignment blocks at the top of Zone 2 and Zone 3, as required in Section 2.4.4 of the PICMG 3.0 Specification. The Zone 2 alignment block (K1) is assigned a keying value of 11 and uses Tyco* 1-1469373-1 (or equivalent). The Zone 3 alignment block (K2) has a solid face and is used to ensure that RTMs with protruding connectors are not plugged into the ATCA-4200 or vice versa.The component used for this is either a Tyco 1469374 or a Tyco 1469275-2 (or equivalent).

Jumpers

The ATCA-4200 module contains several banks of jumpers used to configure certain options not configurable through the BIOS Setup utility. These jumpers are used for diagnostic purposes. Users should take precautions when changing these jumpers.

Figure 17. Jumper Locations

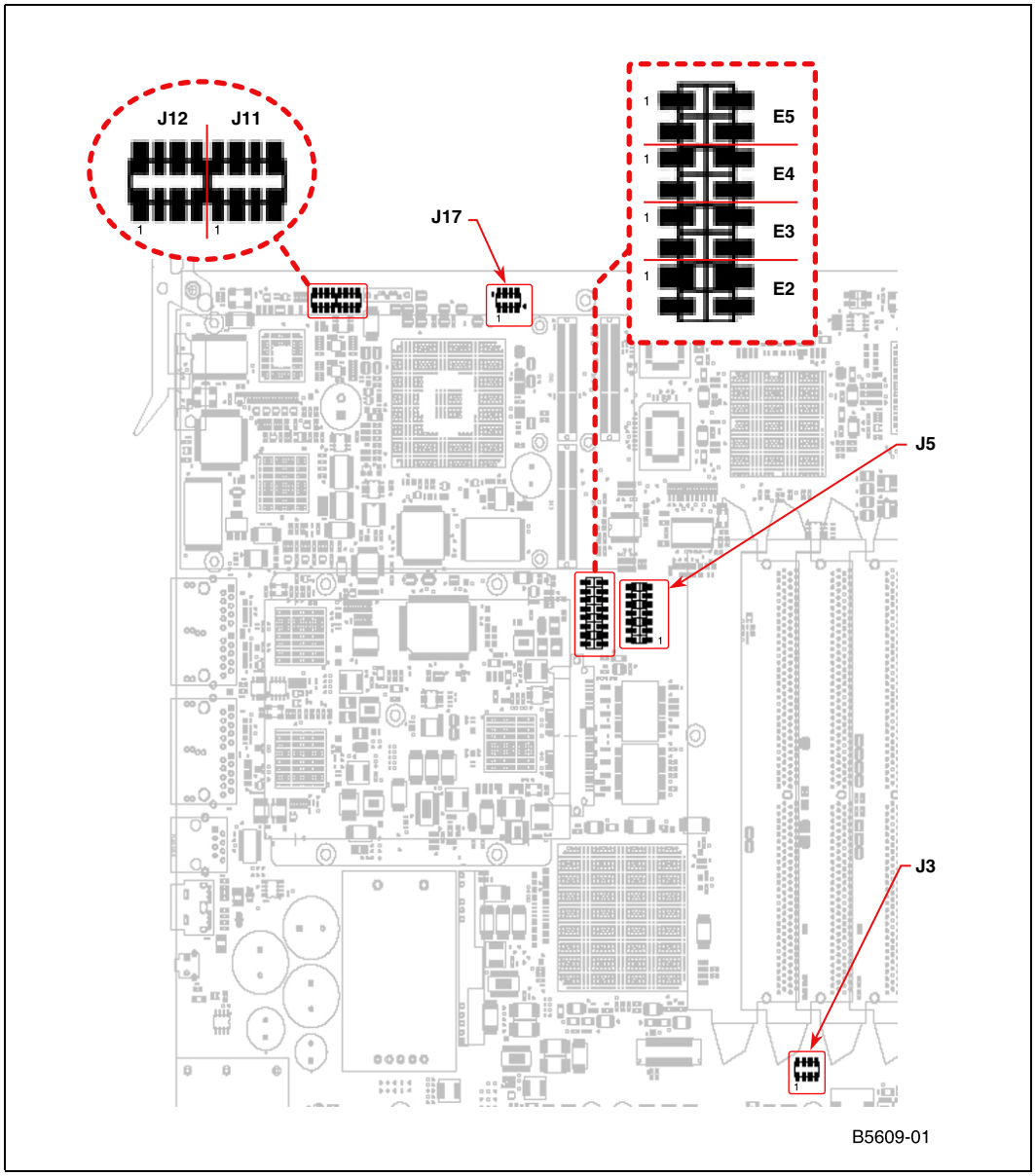


Table 9. Jumper Descriptions

Jumper	Name	Pin	Pin	Signal	Comments
J3	CPU 0 IPT TDO	1	2	CPU 1IPT TDO	Shunt 1-2 and 3-4 to include both CPU's in the ITP chain
	CPU 0 ITP TDO	3	4	CPU 1 ITP TDO	Shunt 1-3 for only CPU 0 in IPT chain
	NC	5	6	NC	
	NC	7	8	NC	

Table 9. Jumper Descriptions (Continued)

Jumper	Name	Pin	Pin	Signal	Comments
J5	NC	1	2	GND	IPMC TAP Port Header
	SMC_TRST#	3	4	GND	
	SMC_TDI	5	6	GND	
	SMC_TMS	7	8	GND	
	SMC_TCK	9	10	GND	
	SMC_TDO	11	12	SMC_DBG_RST #	
	NC	13	14	GND	
J11		1	2		Shunt 1-2 to reset RTC well in 6300ESB
		3	4		Shunt 3-4 for MFG test Mode
		5	6		Shunt 5-6 to clear CMOS password
		7	8		Shunt 7-8 to clear CMOS
J12		1	2		N/A
		3	4		N/A
		5	6		N/A
		7	8		N/A
J17		1	2		Shunt 1-2 to force power on without Shelf Manager interaction
		3	4		Shunt 3-4 to bypass e-keying
		5	6		Shunt 5-6 to program FPGA via JTAG cable
		7	8		N/A
E1	SAS UART RX	1	2	VCC3	E1 is for SAS controller serial debug connection
	SAS UART TX	3	4	GND	
E2	WDT_OFF#	1	2	FPGA_TCK	E2 for FPGA programming
	GND	3	4	FPGA_TDO	Also, shunt 1-3 to force Watchdog off
E3		1	2		Shunt 1-2 to force IPMC into Flash Update mode
		3	4		Shunt 3-4 to write protect IPMC Flash
E4		1	2		Shunt 1-2 to write protect primary ATA flash drive
		3	4		Shunt 3-4 to write protect secondary ATA flash drive

Table 9. Jumper Descriptions (Continued)

Jumper	Name	Pin	Pin	Signal	Comments
E5		1	2	FPGA_TDI	E5 is for FPGA programming
		3	4	FPGA_TMS	

On-Board Connectors

PMC 1 Connectors (Jn 6/8/9)

PMC 1 is connected to the PXH via a 64 bit/66 MHz PCI-X link on Jn1/Jn2/Jn3. Pin assignments are shown in Table 10 through Table 12.

Table 10. PMC 1 Connectors– Jn6 (64 bit PCI)

Pin	Signal	Pin	Signal
1	PMC_TCK_64_66	2	NC
3	GND	4	INTA#
5	INTB#	6	INTC#
7	NC	8	VCC
9	INTD#	10	NC
11	GND	12	VCC3
13	PCLKPMC	14	GND
15	GND	16	GNT#
17	REQ#	18	VCC
19	VCC3 (VIO)	20	AD[31]
21	AD[28]	22	AD[27]
23	AD[25]	24	GND
25	GND	26	C/BE[3]#
27	AD[22]	28	AD[21]
29	AD[19]	30	VCC
31	VCC3 (V I/O)	32	AD[17]
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	VCC
39	PCIX_CAP	40	LOCK#
41	SDONE#	42	SB0#
43	PAR	44	GND
45	VCC (V I/O)	46	AD[15]
47	AD[12]	48	AD[11]
49	AD[09]	50	VCC
51	GND	52	C/BE[0]#
53	AD[06]	54	AD[05]
55	AD[04]	56	GND
57	VCC3 (V I/O)	58	AD[03]

Table 10. PMC 1 Connectors– Jn6 (64 bit PCI) (Continued)

Pin	Signal	Pin	Signal
59	AD[02]	60	AD[01]
61	AD[00]	62	VCC
63	GND	64	REQ64#

Table 11. PMC 1 Connectors– Jn8 (64 Bit)

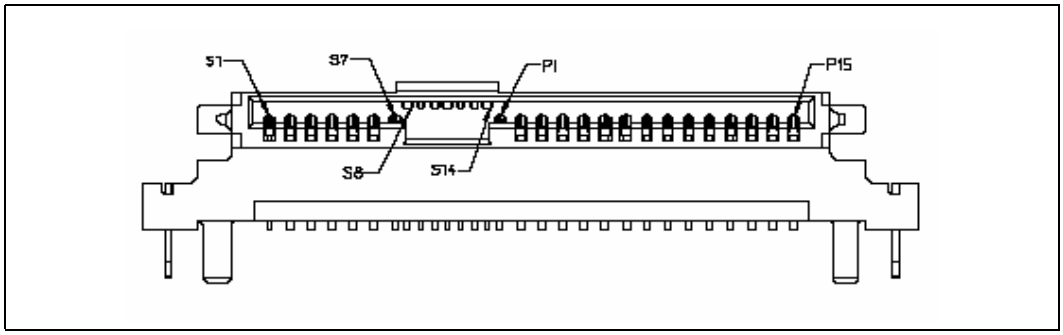
Pin	Signal	Pin	Signal
1	+12V	2	NC
3	TMS	4	NC
5	TDI	6	GND
7	GND	8	NC
9	NC	10	NC
11	BUSMODE2#	12	VCC3
13	RST#	14	BUSMODE3#
15	VCC3	16	BUSMODE4#
17	PME#	18	GND
19	AD[30]	20	AD[29]
21	GND	22	AD[26]
23	AD[24]	24	VCC3
25	IDSEL	26	AD[23]
27	VCC3	28	AD[20]
29	AD[18]	30	GND
31	AD[16]	32	C/BE[2]#
33	GND	34	NC
35	TRDY#	36	VCC3
37	GND	38	STOP#
39	PERR#	40	GND
41	VCC3	42	SERR#
43	C/BE[1]#	44	GND
45	AD[14]	46	AD[13]
47	M66EN	48	AD[10]
49	AD[08]	50	VCC3
51	AD[07]	52	NC
53	VCC3	54	NC
55	NC	56	GND
57	NC	58	NC
59	GND	60	NC
61	ACK64#	62	VCC3
63	GND	64	NC
57	NC	58	NC
59	GND	60	NC
61	ACK64#	62	VCC3
63	GND	64	NC

Table 12. PMC 1 Connectors– Jn9 (64 bit PCI)

Pin	Signal	Pin	Signal
1	NC	2	GND
3	GND	4	C/BE[7]#
5	C/BE[6]#	6	C/BE[5]#
7	C/BE[4]#	8	GND
9	VCC3 (VIO)	10	PAR64
11	AD[63]	12	AD[62]
13	AD[61]	14	GND
15	GND	16	AD[60]
17	AD[59]	18	AD[58]
19	AD[57]	20	GND
21	VCC3 (VI0)	22	AD[56]
23	AD[55]	24	AD[54]
25	AD[53]	26	GND
27	GND	28	AD[52]
29	AD[51]	30	AD[50]
31	AD[49]	32	GND
33	GND	34	AD[48]
35	AD[47]	36	AD[46]
37	AD[45]	38	GND
39	VCC3 (VIO)	40	AD[44]
41	AD[43]	42	AD[42]
43	AD[41]	44	GND
45	GND	46	AD[40]
47	AD[39]	48	AD[38]
49	AD[37]	50	GND
51	GND	52	AD[36]
53	AD[35]	54	AD[34]
55	AD[33]	56	GND
57	VCC3 (VIO)	58	AD[32]
59	NC	60	NC
61	NC	62	GND
63	GND	64	NC

Serial Attached SCSI (SAS*) Connector (J7)

Figure 18. SAS Connector



Extended ITP700 Debug Port Connector (J4)

An Extended ITP700 port connection is included to facilitate debug and BIOS/software development efforts. This JTAG connection to the processors utilizes voltage-signaling levels that are specific to the Intel® Xeon® processor family. These levels must not be exceeded or processor damage may occur.

Note
These connectors are not intended for use by customers.

Front Panel Connectors

USB Connector (J3)

The ATCA-4200 module has a dual-port USB connector that supports 2.0 and 1.1 USB. USB connector J3 is accessed at the front panel. Figure 19 shows the USB connector position on the board.

Figure 19. USB Connector (J3)

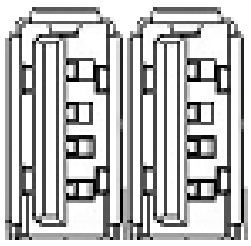


Table 13. USB Connector (J3) Pin Assignments

Pin	Signal
1	+5 V
2	-DATA
3	+DATA
4	GND

Serial Port Connector (J4)

A single serial port interface using an RJ-45 style shielded connector is provided on the front edge of the card. See Figure 20 for its position on the board. The default connector is an 8-pin RJ-45.

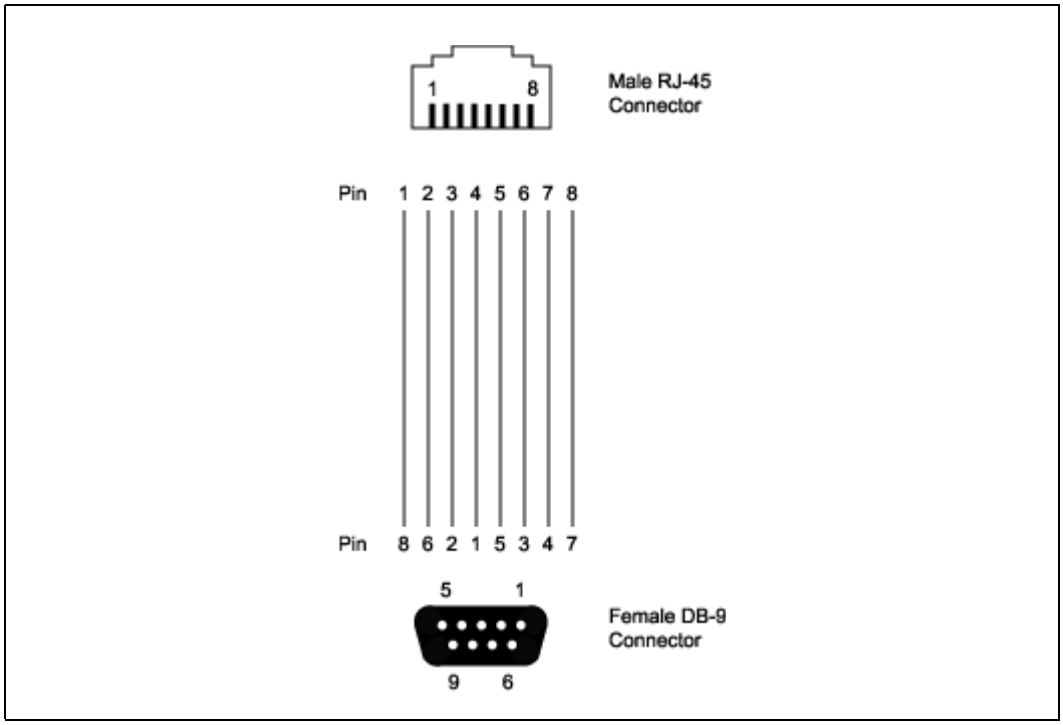
Figure 20. Serial Port Connector (J4)



Table 14. Serial Port Connector (J4) Pin Assignments

Pin	Signal
1	RTS#
2	DTR#
3	TXD#
4	GND#
5	GND#
6	RXD#
7	DSR#
8	CTS#

Figure 21. DB-9 to RJ-45 Pin Translation



Ethernet Front Panel Connectors(J14,J15)

Four gigabit Ethernet port interfaces that use two dual RJ-45 style shielded connectors are provided on the front edge of the board.

Figure 22. Front Panel Ethernet Connectors

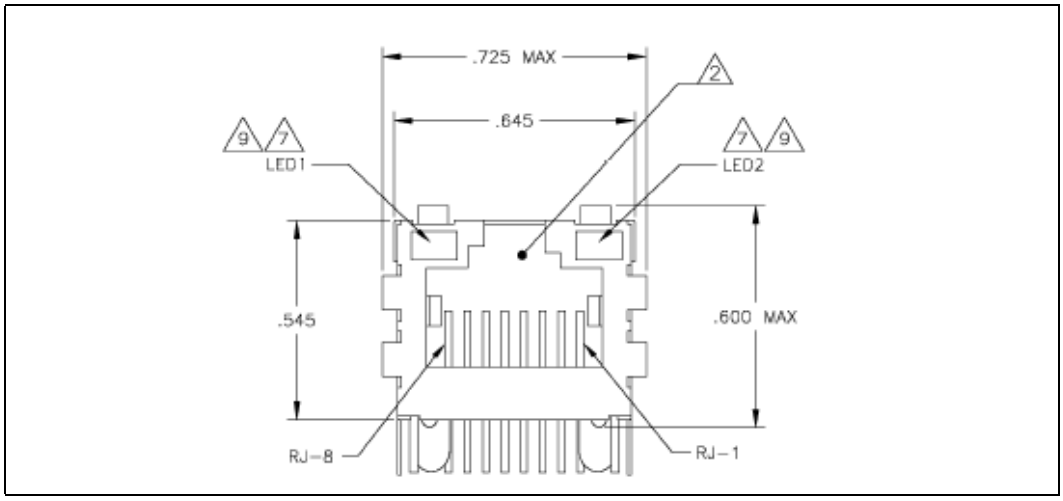


Table 15. Front Panel Dual GbE RJ-45 Connectors (J14, J15) Pin Assignments

Pin	Signal Name	Signal Name
1	BI_DA+	BI_DA+
2	BI_DA-	BI_DA-
3	BI_DB+	BI_DB+
4	BI_DB-	BI_DB-
5	BI_DC+	BI_DC+
6	BI_DC-	BI_DC-
7	BI_DD+	BI_DD+
8	BI_DD-	BI_DD-

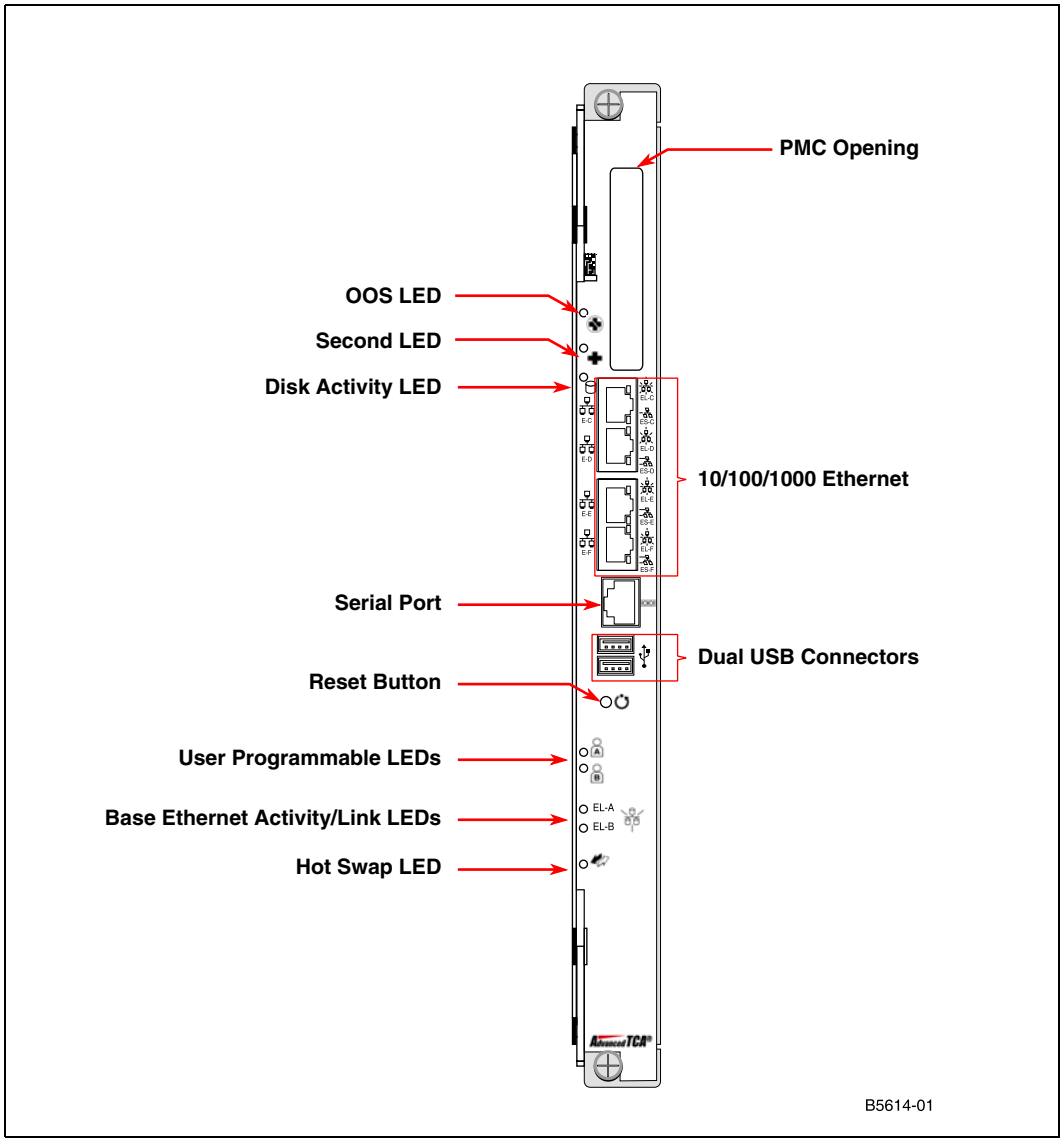
Table 16. Front Panel Ethernet Port LED States

LED	Status	Description
Top Green LED	Off	No Link
	Blinking	Transmission Activity
	Solid On	Link established, but no activity
Lower Amber/Green LED	Off	10 Mbps Connection
	Green	100 Mbps Connection
	Amber	1000 Mbps Connection

Front Panel LEDs

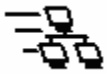
The ATCA-4200 module provides several LEDs to indicate status. The LEDs can be driven to display red, green, or amber.

Figure 23. Front Panel LEDs



When these LEDs are lit, they indicate the status defined in the Table 17.

Table 17. Front Panel LED Descriptions

LED	Function
Hot Swap 	Function: Hot Swap as defined in AdvancedTCA* 3.0 Specification It is also possible to override the default behavior of the LED using AdvancedTCA FRU LED Control commands. Possible States: OFF / BLUE / SHORT BLINK / LONG BLINK
Out of Service 	Function: Out of Service (AdvancedTCA LED 1). RED: The board is out of service. OFF: The board is running. It is possible to override the default IPMC behavior of the LED using AdvancedTCA FRU LED Control commands. Possible States: OFF / RED / AMBER
Health 	Function: Health (AdvancedTCA LED 2). The ATCA-4200 health is be based on an aggregation of IPMI sensors, like board temperature and voltage. GREEN: The ATCA-4200 is healthy. RED: The ATCA-4200 is not healthy. It is possible to override the default IPMC behavior of the LED using AdvancedTCA FRU LED Control commands. Possible States: OFF / GREEN / RED / AMBER
Base/Fabric GbE Link 	Function: Gigabit Ethernet base/fabric interface link and activity OFF: No link GREEN: link GREEN-BLINK: link and activity
Base/Fabric GbE Speed 	Function: Gigabit Ethernet base/fabric interface speed OFF: 10 Mb/s GREEN: 100 Mb/s AMBER: 1000 Mb/s

Reset Button

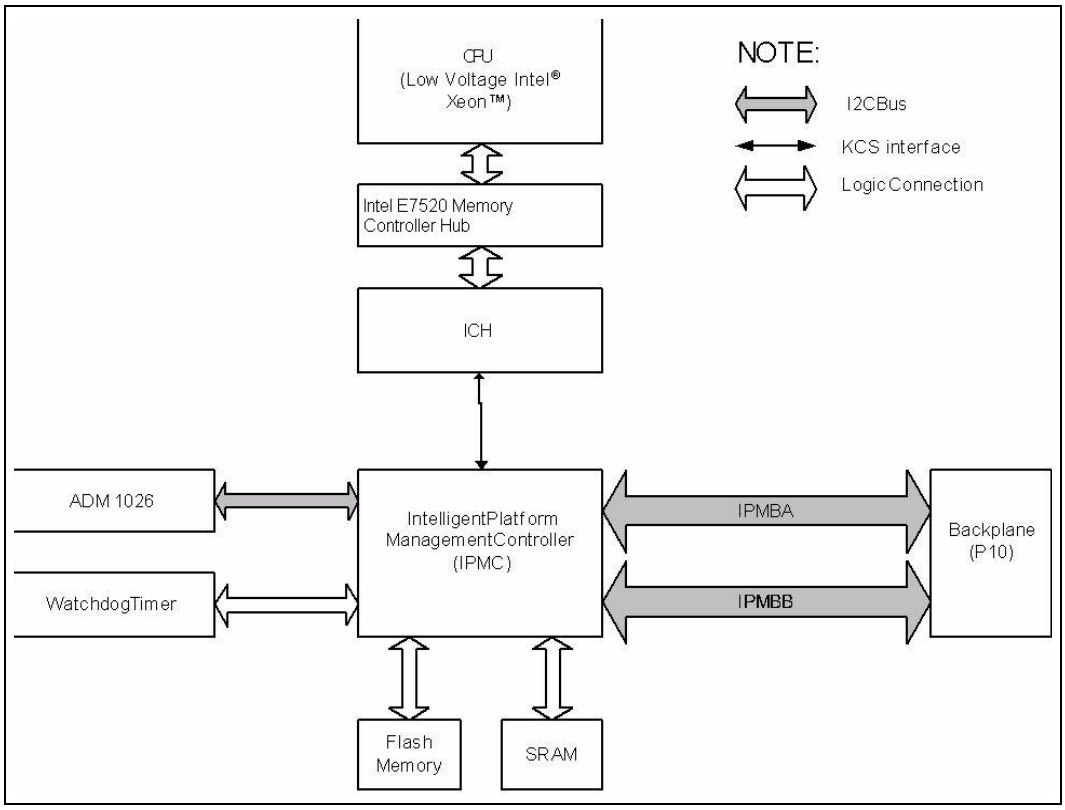
The reset button is located in a small recessed hole below the USB ports. The reset button is used as an input to the IPMC to request a cold reset. There are IPMI commands to reset the board and change power states through the software. The reset button is a last resort since you must be physically present at the chassis to reset the board. The reset button is located on the front panel, as shown in Figure 14.

5 Hardware Management Overview

The Intelligent Platform Management Controller (IPMC) is an Intel-designed baseboard management controller device manufactured by Philips Semiconductor* for Intel.

The high-level architecture of the baseboard management for ATCA-4200 is represented in Figure 24.

Figure 24. Hardware Management Block Diagram



The main processors communicate with the IPMC using the Keyboard Controller Style (KCS) interface. Two KCS interfaces are available for the BIOS to communicate to the IPMC. The BIOS uses the SMS interface for normal communication and the SMM interface when executing code under systems management mode (SMM). The base address of the LPC interface for SMS is 0xCA2 and 0xCA4 for SMM operation. Besides that, the BIOS is able to communicate with the IPMC for POST error logging purposes, fault resilient purposes, and critical interrupts using the KCS interface.

The memory subsystem of the IPMC consists of flash memory to hold the IPMC operation code, firmware update code, system event log (SEL), and a sensor data record (SDR) repository. RAM is used for data and occasionally as a storage area for code when flash programming is under execution. The field replacement unit (FRU)

inventory information is stored in the nonvolatile memory on an ADM1026*, manufactured by Analog Devices*. The flash memory can store up to 64 KBytes of SEL events and SDR information, while the ADM1026 can store up to 512 bytes of FRU information. Having the SEL and logging functions managed by the IPMC helps ensure that 'post-mortem' logging information is available even if the system processor becomes disabled.

The IPMC provides six I^2C bus connections. Two are used as the redundant IPMB bus connections to the backplane while another one is used for communication with the ADM1026. The remaining buses are unused. If an IPMB bus fault or IPMC failure occurs, IPMB isolators are used to switch and isolate the backplane/system IPMB bus from the faulted ATCA-4200 board. Where possible, the IPMC activates the redundant IPMB bus to re-establish system management communication to report the fault.

The onboard DC voltages are monitored by the ADM1026 device. The IPMC queries the ADM1026 over a local system management I^2C bus. The ADM1026 includes voltage threshold settings that can be configured to generate an interrupt to the IPMC if any of the thresholds are exceeded.

To increase the reliability of the ATCA-4200, a watchdog timer is implemented that strobes an external watchdog timer at two-second intervals to ensure continuity of operation of the board's management subsystem. If the IPMC ceases to strobe the watchdog timer, the watchdog timer isolates the IPMC from the IPMBs and resets the IPMC. The watchdog timer expires after six seconds if strobes are not generated, and it resets the IPMC. Detailed information on the watchdog timer configuration can be queried using standard IPMI v1.5 watchdog timer commands. The watchdog timer does not reset the payload power.

Sensor Data Record (SDR)

Sensor Data Records contain information about the type and number of sensors in the baseboard, sensor threshold support, event generation capabilities, and the types of sensor readings handled by system management firmware.

The ATCA-4200 management controller is set up as a satellite management controller (SMC). It supports sensor devices whose population is static by nature. SDRs can be queried using Device SDR commands to the firmware. Refer to Appendix A, "List of Supported Commands (IPMI v1.5 and PICMG 3.0)" for the list of supported IPMI commands for SDRs. Hardware sensors that have been implemented are listed below.

Table 18. Hardware Sensors

Sensor Number	Sensor Type	Voltage/Signals Monitored	Monitored via	Scanning Enabled under Power State	Health LED (Green to Red)
03h	Watchdog Timer	IPMC Watchdog Timer timeout	IPMC	Power On/Off	No change
06h	System Firmware Progress		IPMC	Power On	No change
07h	CPU Critical Interrupt	PCI SERR	BIOS	Power On	PCI SERR signal asserted
		PCI PERR	BIOS	Power On	PCI PERR signal asserted
08h	Memory Error	ECC Multiple Bit error	BIOS	Power On	Multiple Bit Error or Uncorrectable ECC occurred
		ECC Single Bit error	BIOS	Power On	No change
01h	Power Unit	Payload Power	IPMC	Power On	Soft power control failure (Offset Bit 05h asserted
10h	Voltage	3.3 VSB	ADM 1026	Power On/Off	Exceeds critical threshold
11h		+5 VSB	ADM 1026	Power On/Off	Exceeds critical threshold
13h		V BAT	ADM 1026	Power On/Off	Exceeds critical threshold
14h		+1.2 V	ADM 1026	Power On	Exceeds critical threshold
15h		VTT DDR (+1.25 V)	ADM 1026	Power On	Exceeds critical threshold
16h		+1.8 V	ADM 1026	Power On	Exceeds critical threshold
17h		+2.5 V	ADM 1026	Power On	Exceeds critical threshold
18h		+3.3 V	ADM 1026	Power On	Exceeds critical threshold
19h		+5 V	ADM 1026	Power On	Exceeds critical threshold

Table 18. Hardware Sensors (Continued)

Sensor Number	Sensor Type	Voltage/Signals Monitored	Monitored via	Scanning Enabled under Power State	Health LED (Green to Red)
1A	Voltage	+12V	ADM 1026	Power On	Exceeds critical threshold
1B		CPU 0 Voltage	ADM 1026	Power On	Exceeds critical threshold
1C		CPU 1Voltage	ADM 1026	Power On	Exceeds critical threshold
1D		+1.5V	ADM 1026	Power On	Exceeds critical threshold
1F	?	-48V Feed Alarm	?	?	?b
30h	Temperature	Board Temperature	ADM 1026	Power On/Off	Exceeds critical threshold
37h		CPU 0 Temperature	ADM 1026	Power On	Exceeds critical threshold
38h		CPU 1 Temperature	ADM 1026	Power On	Exceeds critical threshold
50h	Processor	CPU 0 Presence	ADM 1026	Power On/Off	IERR signal asserted???
50h		CPU 0 IERR	IPMC	Power On	No change
50h		CPU 0 Thermtrip	IPMC	Power On	ThermTrip signal asserted
50h		CPU 0 Non-Presence	ADM 1026	Power On/Off	CPU 0 is detected as missing
51h		CPU 1 Presence	ADM 1026	Power On/Off	IERR signal asserted
51h		CPU 1 IERR	IPMC	Power On	No change
51h		CPU 1 Thermtrip	IPMC	Power On	ThermTrip signal asserted
54h	Boot Error	BIOS Main Flash	IPMC	Power On	No change
55h		BIOS FRED Flash	IPMC	Power On	No change

Table 18. Hardware Sensors (Continued)

Sensor Number	Sensor Type	Voltage/Signals Monitored	Monitored via	Scanning Enabled under Power State	Health LED (Green to Red)
56h	Temperature	CPU 0 ProcHot[1]	IPMC	Power On	ProcHot signal asserted
57h		CPU1 ProcHot[1]	IPMC	Power On	ProcHot signal asserted
5D		Drive Temp	ADM 1026	Power On/Off	Exceeds critical threshold
5E		DRAM Temp	ADM 1026	Power On/Off	Exceeds critical threshold
5F		Inlet Temp	ADM 1026	Power On/Off	Exceeds critical threshold
82h	ACPI State	ACPI State	IPMC	Power On/Off	No change
83h	System Event	System Event	IPMC	Power On	No change
85		SMI Timeout	IPMC	Power ON	SMI Line Asserted
8Ah	FRU Hot Swap	FRU State	IPMC	Power On/Off	No change
8Bh	IPMB Link Sensor	Operational state of IPMB-0	Logical	Power On/Off	No change

Note: The PROCHOT signal is a discrete signal but it is treated as a threshold sensor so that it can have a Sensor Type of Temperature. IPMI does not have a discrete sensor type for temperatures. The advantage of the PROCHOT sensor acting as a temperature sensor is that the CMM can recognize events from this sensor as temperature events and adjust fan speed accordingly.

System Event Log (SEL)

The SEL is the collection of events that are generated by the IPMC. Event logs are stored in non-volatile memory, and are forwarded to the shelf manager. The SEL resides on the board and allows better tracking of error conditions on the baseboard when it is moved from chassis to chassis. Having the SEL and logging functions managed by the IPMC helps ensure that post-mortem logging information is available should a failure occur that disables the systems processor(s). In the ATCA-4200, flash memory for IPMI firmware can store up to 3276 SEL entries. Management software running on the host processor is responsible for ensuring that SEL storage has sufficient space for SEL logging. Events are normally forwarded to shelf manager and logged to SEL on the board. If SEL storage on the board is full, new events are forwarded to the Shelf Manager but are not logged in to SEL on the board.

A set of IPMI commands (see Table 75) allows the SEL to be read and cleared and allows events to be added to the SEL. The IPMI commands used for adding events to the SEL are *Platform Event Message, Add SEL entry,* and *Partial Add Entry.* Table 19 lists supported SEL events. Event messages can be sent to the IPMC through the IPMB so satellite controllers can detect events and log them into the SEL.

Table 19. SEL Events Supported by the ATCA-4200

Sensor Type	Sensor Type Code	Sensor-Specific Offset (Event Data 1, Bit 0-3)	Event	Remarks
Reserved	00h	-	Reserved	-
Temperatu re	01h	-	Temperature	Threshold exceeded for upper critical, upper non-critical, lower critical and lower non-critical thresholds. Refer to <Link>Table 20, "Sensor Thresholds for IPMC Firmware 1.x." on page 67 for sensor thresholds data.
Voltage	02h	-	Voltage	Voltage exceeded upper critical, upper non-critical, lower critical and lower non-critical thresholds. Refer to <Link>Table 18 for sensor thresholds data.
Processor	07h	00h	IERR	Processor IERR has occurred.
		01h	Thermal Trip	Processor thermal trip has occurred.
		04h	FRB3/Processor Startup/Initialization Failure (CPU did not start)	An FRB3 Timer (30 seconds) was implemented to detect the failure of the CPUs from booting. Event data 3 = Last Post 80 code byte
		05h	Configuration Error	CPU 0 and CPU 1 are not present.
		07h	Processor Presence Detected[1]	
		09h	Terminator Presence Detected[1]	
Power Supply	08h	01h	DC-DC Input lost	Monitors -48 volt feed to on-board DC-DC convertor

Note:

These sensor offsets do not generate events, but they are valid offsets when reading the sensor values.

Table 19. SEL Events Supported by the ATCA-4200 (Continued)

Sensor Type	Sensor Type Code	Sensor-Specific Offset (Event Data 1, Bit 0-3)	Event	Remarks
Power Unit	09h	00h	Power Off/Power On	Normal power off indication. Offset 0 is just a status indicating that the payload power is off. It does not generate an event when it is set. (For internal use).
		05h	Soft Power Control Failure (unit did not respond to request to turn on)	The Power Unit sensor is used to detect when the Payload power does not come up when the board is told to power on. When the board enters M4 state, the IPMC asserts a Power Enable line to cause the Payload to power up. The IPMC then waits for another line that indicates that the power has come up successfully. If that line does not assert within 2 seconds, then offset 05h is asserted on the Power Unit sensor, which generates an event to notify the Shelf Manager of the failure.
Memory	0Ch	00h	Correctable ECC	Event data 3 = DIMM pair number 00 refers to J8/J9 01 refers to J10/J11
		01h	Uncorrectable ECC	Event data 3 = DIMM pair number 00 refers to J8/J9 01 refers to J10/J11

Note:

These sensor offsets do not generate events, but they are valid offsets when reading the sensor values.

Table 19. SEL Events Supported by the ATCA-4200 (Continued)

Sensor Type	Sensor Type Code	Sensor-Specific Offset (Event Data 1, Bit 0-3)	Event	Remarks
System Firmware Progress 0Fh 00h			BIOS checksum error	Event data 2 = 99h Event data 3 = 99h
			Timer Count Read/Write error	Event data 2 = FEh Event data 3 = 00h
			CMOS Battery error	Event data 2 = FEh Event data 3 = 01h
			CMOS Diagnosis status error	Event data 2 = FEh Event data 3 = 02h
			CMOS Checksum error	Event data 2 = FEh Event data 3 = 03h
			CMOS Memory Size error	Event data 2 = FEh Event data 3 = 04h
			RAM Read/Write test error	Event data 2 = FEh Event data 3 = 05h
			CMOS Date/Time error	Event data 2 = FEh Event data 3 = 06h
			Clear CMOS jumper	Event data 2 = FEh Event data 3 = 07h
			Clear Password Jumper	Event data 2 = FEh Event data 3 = 08h
			Manufacturing Jumper	Event data 2 = FEh Event data 3 = 09h
			Configuration error on DIMM pair 0 (J8 & J9)	Event data 2 = FEh Event data 3 = 10h
			Configuration error on DIMM pair 1(J10/J11)	Event data 2 = FEh Event data 3 = 11h
			No system memory is physically installed or fails to access any DIMM's SPD data	Event data 2 = FEh Event data 3 = 12h
			BMC in update error	Event data 2 = FEh Event data 3 = 0Ah
			BMC Response Fail error	Event data 2 = FEh Event data 3 = 0Bh Note: This event is generated by the BIOS, but since the BMC cannot respond, No IPMC event, and no SEL event will be generated.

Note:

These sensor offsets do not generate events, but they are valid offsets when reading the sensor values.

Table 19. SEL Events Supported by the ATCA-4200 (Continued)

Sensor Type	Sensor Type Code	Sensor-Specific Offset (Event Data 1, Bit 0-3)	Event	Remarks
System Firmware Progress			Event Log Full error	Event data 2 = FEh Event data 3 = 0Ch Note: Event will only be generated one time until the SEL is cleared.
Event Logging Disabled	10h	00h	Correctable Memory Error Logging Disabled	Error Logging will be disabled after 10 events within one hour.
Critical Interrupt	13h	04h	PCI PERR	Event data 2 = Bus No. Event data 3: Byte [7:3] = Device No Byte [2:0] = Func. No
		05h	PCI SERR	Event data 2 = Bus No. Event data 3: Byte [7:3] = Device No Byte [2:0] = Func. No
		07h	PCI Non-Fatal error	Event data 2 = Bus No. Event data 3: Byte [7:3] = Device No Byte [2:0] = Func. No
System ACPI Power state	22h	00h	S0/G0[1]	Board is running
		06h	S4/S5[1]	Soft-off
		0Bh	Legacy ON state[1]	Indicate ON for board that doesn't support ACPI
		0Ch	Legacy OFF state[1]	Legacy soft-off
Watchdog	23h	00h	Timer expired, status only	
		01h	Hard Reset	POST/Boot monitor timed out
		02h	Power Down	OS WDT shutdown after the monitor timeout
		03h	Power Cycle	OS WDT reset after the monitor timeout
		08h	Timer Interrupt	Event data 2: Byte [7:4] = Interrupt Type 0h = none 2h = NMI

Note:

These sensor offsets do not generate events, but they are valid offsets when reading the sensor values.

Table 19. SEL Events Supported by the ATCA-4200 (Continued)

Sensor Type	Sensor Type Code	Sensor-Specific Offset (Event Data 1, Bit 0-3)	Event	Remarks
Boot Error	1Eh	03h	Invalid Boot Sector	Event will be logged if there's an invalid boot sector detected by the BIOS.
SMI Timeout	E0h	00h	State De-Asserted[1]	This is the normal situation when a board is able to power up.
		01h	State Asserted	The SMI line has been constantly asserted for 10 seconds which indicates a severe hardware failure around the CPU.
FRU Hot Swap	F0h	00h	M0 – FRU not installed	Refer to PICMG 3.0 Specifications (Table 3-14)
		01h	M1 – FRU inactive	
		02h	M2 – FRU activation request	
		03h	M3 - FRU activation in progress	
		04h	M4 - FRU active	
		05h	M5 - FRU deactivation request	
		06h	M6 - FRU deactivation in progress	
		07h	M7 - Communication lost	
IPMB Link Sensor	F1h	00h	IPMB A & B disabled	Refer to PICMG 3.0 Specifications (Table 3-46)
		01h	IPBM A enabled IPMB B disabled	
		02h	IPMB A disabled IPMB B disabled	
		03h	IPMB A & B enabled	

Note:

These sensor offsets do not generate events, but they are valid offsets when reading the sensor values.

Temperature and Voltage Sensors

Temperature and voltage readings are monitored by the ADM1026. They are critical sensors that ensure the ATCA-4200 is operating at its predefined threshold limits. The sensors are categorized as follows:

- Lower Non-Critical
- Lower Critical
- Upper Non-Critical
- Upper Critical

If the lower critical or upper critical threshold is exceeded, it raises a major alarm. If the lower non-critical or upper non-critical threshold is exceeded, it raises a minor alarm.

Only critical thresholds which are exceeded turn the Health LED solid red. However, for any events above, IPMC forwards the events to the shelf manager to log it into shelf manager's SEL.

Table 20. Sensor Thresholds for IPMC Firmware 1.x.

Sensor Name	Description	Sensor Number	Normal Value	Thresholds				
				Lower Critical	Lower Noncritical	Upper Noncritical	Upper Critical	Upper Non-recoverable
+3.3VSB	+3.3VSB	10h	3.30	3.13	-	-	3.46	-
+5VSB	+5VSB	11h	5.00	4.09	-	-	5.24	-
VBAT	VBAT	13h	3.55	1.99	2.79	-	-	-
+1.2V	+1.2V	14h	1.20	1.14	-	-	1.25	-
VTT DDR	DDR Voltage	15h	1.79	1.71	-	-	1.87	-
+1.8V	+1.8V	16h	1.79	1.71	-	-	1.88	-
+2.5V	+2.5V	17h	2.49	2.29	2.35	2.63	2.69	-
+3.3V	+3.3V	18h	3.30	3.13	-	-	3.46	-
+5V	+5V	19h	4.99	4.73	-	-	5.23	-
+12V	+12V	1Ah	12.10	7.56	11.28	12.85	15.06	-
CPU 0 Voltage	CPU 0 Voltage	1Bh	1.17	0.99	-	-	1.23	-
CPU 1Voltage	CPU 1 Voltage	1Ch	1.17	0.99	-	-	1.23	-
+1.5V	+1.5V	1Dh	1.50	1.43	-	-	1.57	-
Baseboard Temp	Baseboard Temp	30h	30	-5	5	60	70	80
CPU 0 Temp	CPU 0 Temp	37h	45	5	10	75	85	127
CPU 0 Temp	CPU 0 Temp	38h	45	5	10	75	85	127

Table 20. Sensor Thresholds for IPMC Firmware 1.x. (Continued)

Sensor Name	Description	Sensor Number	Normal Value	Thresholds				
				Lower Critical	Lower Noncritical	Upper Noncritical	Upper Critical	Upper Non-recoverable
Drive Temp	Drive Temp	5Dh	35	-5	5	45	50	-
DRAM Temp	DRAM Temp	5Eh	35	-5	5	65	75	85
Inlet Temp	Inlet Temp	5Fh	30	-5	5	60	70	80

Note: Values in parentheses are deassertion values.

Processor Events

The processor asserts IERR as the result of an internal error. A thermal trip error indicates the processor junction temperature has reached a level where permanent silicon damage may occur. Upon THERMTRIP assertion, the IPMC powers down the board.

The CPU0 and CPU1 PROCHOT signals are monitored by the IPMC directly. Assertion of the signal indicates that the CPU is becoming overheated. Assertion of this signal can be used to tell the shelf manager to increase the fan speed to cool the CPU. When the CPU cools off, the signal is de-asserted. See the *CPU Specifications* to determine the temperature at which this signal is asserted and de-asserted.

DIMM Memory Events

The MCH (E7520) instructs the ICH to report memory parity errors on SMI#. The SMI handler extracts the error information (address) from the DRAM error registers in the MCH and logs it into the SEL. The KCS interface performs error reporting to IPMC. The BIOS sends a platform event message with the appropriate data to the IPMC, which logs the event to the SEL and forwards the event to the shelf manager. Correctable memory errors generate an SMI and are logged into the SEL. Normally, a board with non-correctable errors is likely to hang as the multi-bit error may cause the CPU to execute corrupted instructions. If the CPU executes corrupted instructions before executing the code to log the event, then this event will not be logged in the SEL.

System Firmware Progress (POST Error)

The BIOS is able to log both POST and critical events to the IPMC error log.

System ACPI Power State

The ATCA-4200 supports ACPI functionality with support for the sleep states S0, S4 & S5. On assertion of SLP_S5 and SLP_S3 GPIOs, IPMC sends out a hot-swap event message to the shelf manager requesting deactivation. On successful reception of a deactivation message from the shelf manager, the FRU enters M1 power state and remains in this state.

Under conditions where an ACPI-enabled operating system is in S4/S5 sleep state, the chipset can de-assert SLP_S5 and SLP_S3 GPIOs requiring the IPMC to attempt AdvancedTCA power state transition to the M4 state (through M2, M3).

The ACPI capabilities of an operating system are communicated by the BIOS to the IPMC at initialization. An OEM-style IPMI command is sent by the BIOS for this purpose. This command (*SetACPIConfig*; *NetFn: 30h, command: 83h*) is sent by the BIOS every time an operating system is initialized. The IPMC firmware defaults to no ACPI until this command is received with proper data in the request to indicate the OS is either ACPI-enabled or disabled. This command is only executable over the SMS channel.

IPMB Link Sensor

The ATCA-4200 provides two IPMB links to increase communication reliability to the shelf manager and other IPM devices on the IPMB bus. These IPMB links work together for increased throughput where both busses are actively used for communication at any point. A request might be received over IPMB Bus A, and the response is sent over IPMB Bus B. Any requests that time out are retried on the redundant IPMB bus. In the event of any link state changes, the events are written to the ATCA-4200 SEL. The IPMC monitors the bus for any link failure and isolates itself from the bus if it detects that it is causing errors on the bus. Events are sent to signify the failure of a bus or, conversely, the recovery of a bus.

FRU Hot Swap

The hot-swap event message conveys the current state of the FRU, the previous state, and the cause of the state change as determined by the IPMC. Refer to the *PICMG 3.0 Specifications* for further details on the hot-swap state.

Port 80h POST Codes

Table 21. CPU Failure Behavior

CPU Failure Detection	CPU Identification		Behavior		
Operational Phase	CPU0	CPU1	Board Power Status	CMM SEL Event	Health LED
POST	Normal	Normal	Bootable	No	Green
	Fail	Normal	Stop Booting	Yes	Red
	Normal	Fail	Stop Booting	Yes	Red
	Fail	Fail	Stop Booting	Yes	Red
Runtime	Normal	Normal	Keep Working	No	Green
	Fail	Normal	Halt	Yes	Red
	Normal	Fail	Halt	Yes	Red
	Fail	Fail	Halt	Yes	Red

When there is an FRB3 failure, the event message sent from the CPU Status sensor with sensor type code 07 provides the last Port 80 code byte written by the BIOS. This information is contained in Data Byte 3 of the event message.

Example:

To decode Port 80 data from the SEL event when a board is booted without memory, use the following method.

SEL EVENT - ID:0DD8(Tue Jan 25 18:45:20 2005) Gen:8E Type:07 No:50 Dir:6F D1:64 D2:6F D3:E1

The values shown in bold above convey the following information:

- The sensor type is 07. This refers to the processor.
- Event data 1, bit 0-3 is 4. This refers to an FRB3/processor startup or initialization failure (the CPU did not start).
- Event data 3 is E1. This refers to the last Port 80h POST codes before the board hangs.

Refer to the tables in *Port 80h POST Codes* on page 70, for descriptions of the Port 80h POST codes.

Note

At any time when a board hangs, you can also use an OEM IPMI command to query the Port 80 POST codes. For the command syntax, refer to *Get Port80 Data* on page 77.

Field Replaceable Unit (FRU) Information

The FRU Information feature provides inventory data about the boards where the FRU Information Device is located. The part number or version number can be read through software.

FRU information includes data describing the ATCA-4200 board according to the PICMG 3.0 Specification requirements. Additional multi-records are added for the BIOS to write CPU information, BIOS version number, and PMC information to FRU data correctly. This information is retrieved by the shelf manager (ShMC)for reporting board-specific information through an out-of-band mechanism.

Table 22 provides definitions for the mult-irecord implemented by the firmware as part of FRU data.

Table 22. Multi-Record FRU Data (BIOS Information)

Variable	Size (byte)	Data	Type	Description
Manufacturer ID (Intel IANA number)	3	0x000157 (LSB first, MSB next)	Binary	
Record Version	1	0x02	Binary	
Type/Length	1	1	Binary	See Table 2-7
No. of CPUs	1	0x01 or 0x02	Binary	
Type/Length	1	2	Binary	See Table 2-7
RAM Info	2	0xYYYY (in units of 1MB)	Binary	YYYY*1MB = RAM Size
Type/Length	1	0x06	Binary	See Table 2-7
No. of PMCs	1	1	Binary	
PMC 1 Info	5	PMC_Data	Binary	See Table 2-6
Type/Length	1	0x02	Binary	See Table 2-7
IPMC FW Boot Version Major (VV)	1	0xVV	Binary	Populated by BIOS
IPMC FW Boot Version Minor (vv)	1	0xvv	Binary	Populated by BIOS
Type/Length	1	0x03	Binary	See Table 2-7
IPMC FW Version Major (VV)	1	0xVV	Binary	Populated by BIOS
IPMC FW Version Minor vv)	1	0xvv	Binary	Populated by BIOS
IPMC FW Version Build (bb)	1	0xbb	Binary	Populated by BIOS
Type/Length	1	0xC8	ASCII	See Table 2-7
FPGA Version	8	8 char ascii string	Binary	Populated by BIOS
Type/Length	1	1	Binary	See Table 2-7

Table 22. Multi-Record FRU Data (BIOS Information) (Continued)

Variable	Size (byte)	Data	Type	Description
Board Version	1	Fab revision bits [3:0] Fab version bits [6:4] Bit 7 is fixed at 0 to indicate ATCA-4200 Board	Binary	
Type/Length	1	1	Binary	See Table 2-7
Selected FWH	1	0x00 or 0x01	Binary	Populated by BIOS
Type/Length	1	0xFF	Binary	See Table 2-7
BIOS Version FW0	63	63 char ascii string	ASC-II	Populated by BIOS
Type/Length	1	0xFF	Binary	See Table 2-7
BIOS Version FW1	63	63 char ascii string	ASC-II	Populated by BIOS
End of fields	1	0xC1	Binary	

E-Keying

E-Keying is included in the PICMG 3.0 Specification to prevent board damage, prevent misoperation, and verify fabric compatibility. The FRU data contains the board point-to-point connectivity record as described in Section 3.7.2.3 of the *PICMG 3.0 Specification*.

On the ATCA-4200 the user can select in the BIOS whether each pair of fabric Ethernet is directed to the front panel RJ-45 connectors (copper-based) or the backplane (SERDES interface). By default the BIOS sets the ports to the front panel.

If the fabric Ethernet channels are set to "Fabric" in the BIOS, when the board enters M3 power state, the shelf manager reads in the board point-to-point connectivity record from the FRU and determines whether the board can enable the fabric Ethernet channel ports to the back plane. Set/Get Port State IPMI commands defined by the *PICMG 3.0 Specification* are used for either granting or rejecting the E-keys.

If the fabric Ethernet channel selection is to the front, the firmware maintains the ports to the front panel regardless of whether the shelf manager grants or rejects E-keys for the board.

Table 23, describes the:

- Connections to the base and fabric interfaces on the ATCA-4200 board for E-keying purposes.
- Link descriptor list for the two gigabit Ethernet channels connected to the base interface and the two fiber channels on the fabric interface.

Table 23. Link Descriptors for E-Keying

#	Ethernet Link Descriptor	Link Grouping ID	Link Type Extension	Link Type	Link Designator			Link Desc Value
					Port 0 - 3 Flags	Interface	Channel	
		[31:24]	[23:20]	[19:12]	[11:8]	[7:6]	[5:0]	
1	Base Eth Port 1	00000000	0000	00000001	0001	00	000001	0x00001101
2	Base Eth Port 2	00000000	0000	00000001	0001	00	000010	0x00001102
3	Fabric Eth 1	00000000	0000	00000010	0001	01	000001	0x00002141
4	Fabric Eth 1 & 2	00000000	0000	00000010	0011	01	000001	0x00002341
5	Fabric Eth 3	00000000	0000	00000010	0001	01	000010	0x00002142
6	Fabric Eth 3 & 4	00000000	0000	00000010	0011	01	000010	0x00002342

IPMC Firmware Code

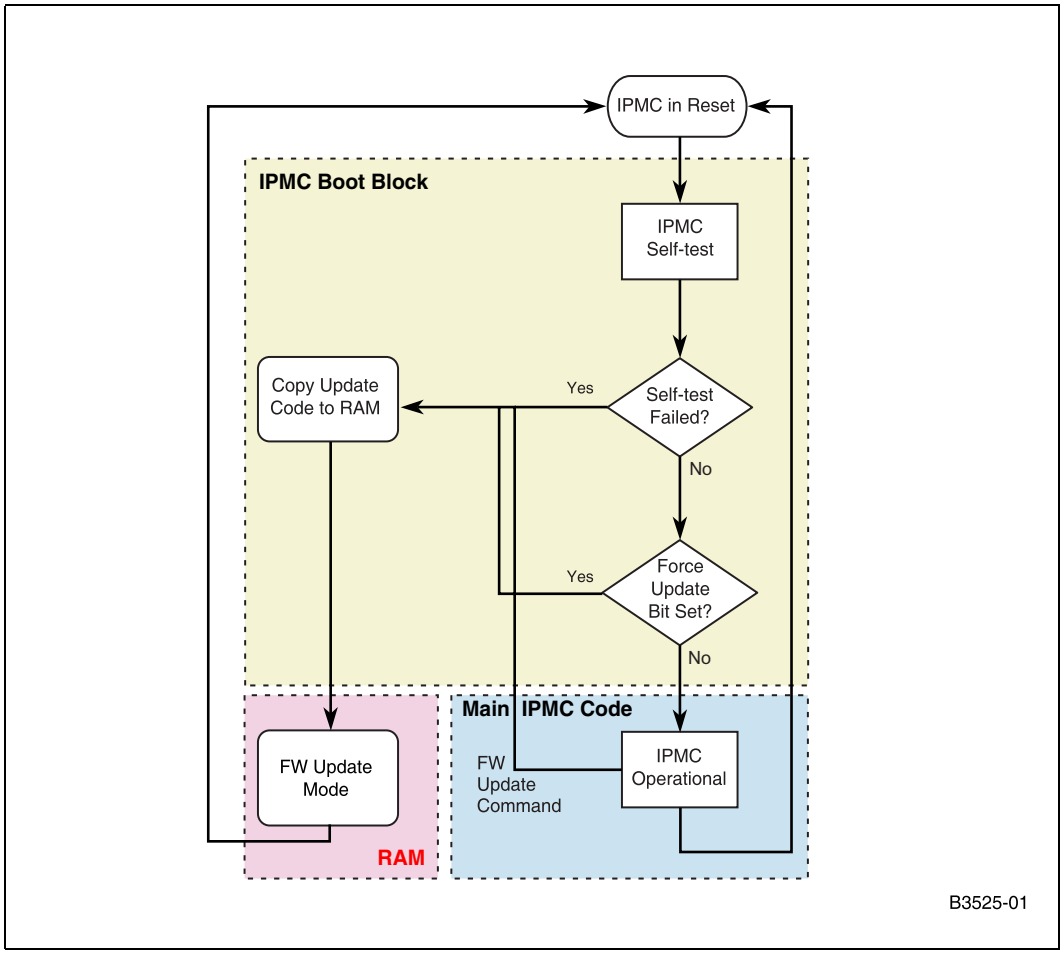
IPMC firmware code is organized into boot code and operational code, both of which are stored in a flash module. Upon an IPMC reset, the IPMC executes the boot code and performs the following:

1. Self test to verify the status of its hardware and memory.
2. Sets up the internal real-time operating system (RTOS).
3. Performs a checksum of the operational code.

Upon successful verification of the operational code checksum, the firmware jumps to the operational code.

When the firmware is commanded to enter firmware (FW) update mode, the operational code uses a special branch, Software Interrupt, to jump to the FW update code in the boot block. Once in FW update mode, the update code is copied into RAM, and then the firmware jumps to the code in RAM to execute. The FW update code cannot execute out of flash while the flash is being updated.

Figure 25. IPMC Firmware Code Process



IPMC Firmware Upgrade Procedure

ATCA-4200 firmware is upgraded using either of two methods, the KCS interface or the IPMB (RMCP) interface.There are one DOS and two Linux versions (32-bit and 64-bit) of the firmware update utility. See the release package of the applicable firmware for details, installation instructions, and release notes.

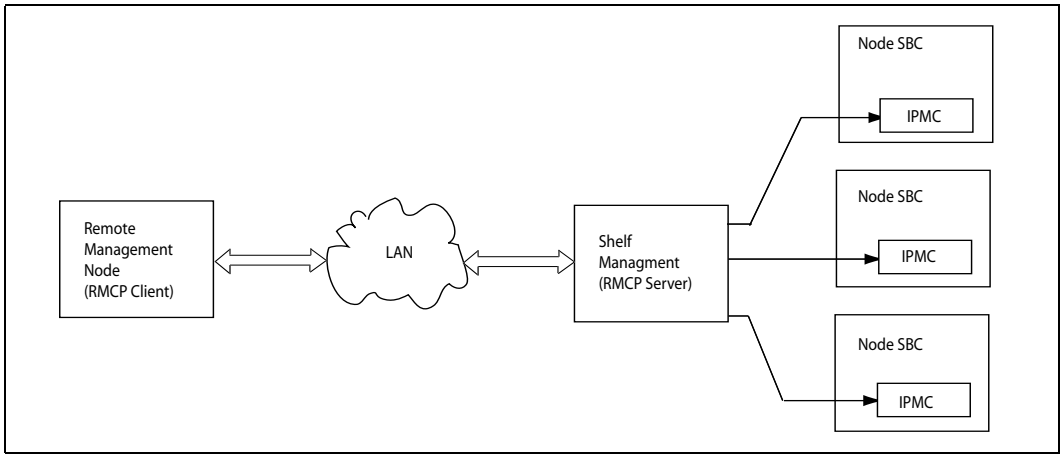
IPMC Firmware Upgrade Using KCS Interface

The KCS interface is the communication mechanism between the host processor on the ATCA-4200 and the IPMC controller. A firmware update utility is available. The utility takes a hex file to be updated as input from the command line. It can also verify that updates are completed successfully by reading back data written to the flash memory. Typically, the utility takes around two minutes to complete the update over the KCS interface. After the firmware update is completed, the controller goes through a reset and boots up with the new firmware. The host processor is not reset when going through a firmware update, so the operating system and applications running on the host processor are not interrupted.

Refer to the latest IPMC firmware release notes for the upgrade procedure. The upgrade procedure, utility, and upgraded firmware are part of the IPMC firmware release package, which can be downloaded from the Intel web site at http://www.intel.com/design/network/products/cbp/atca/index.htm.

IPMC Firmware Upgrade Using the IPMB Interface (RMCP)

Figure 26. Upgrade through the Remote Management Node



IPMI Specification v1.5 defines the Remote Management Control Protocol (RMCP). Version 1.5 adds features for layering commands through virtual networks like Ethernet.

The IPMC firmware that needs to be upgraded is loaded to client utility software on the RMCP client. The RMCP client uses the RMCP protocol carrying embedded IPMI messages to send to the RMCP server running in the CMM. The RMCP server decodes the RMCP package and forwards the IPMI messages to the ATCA-4200.

Updating ATCA-4200 Firmware

Refer to the latest *IPMC firmware release notes* for the upgrade procedure. The upgrade procedure, utility and upgraded firmware are part of the IPMC firmware release package, which can be downloaded from the Intel web site at http://www.intel.com/design/network/products/cbp/atca/index.htm.

OEM IPMI Commands

This section documents the OEM-style IPMI commands implemented and supported on the ATCA-4200.

Reset BIOS Flash Type

This command resets the processor and changes the BIOS bank select signal so that CPU boots off a redundant BIOS bank.

Table 24. Reset BIOS Flash Type

	7	6	5	4	3	2	1	0
NetFn/LUN	NetFn = 3Ah (OEM Request)						RsLUN	
Command	Cmd = 01h							
Byte 1	BIOS checksum success/failure indication 00h – Checksum success 01h – Checksum failure							
Byte 1	Completion code							

Set Control State

This command sets the state of a control pin and overrides the control pin's auto state. Refer to Table 28 for control number information.

Table 25. Set Control State

	7	6	5	4	3	2	1	0
NetFn/LUN	NetFn = 3Eh (OEM Request)						RsLUN	
Command	Cmd = 20h							
Byte 1	Control number							
Byte 2	Control state, 0 = Deassert, 1 = Assert, 3 = Reserved, FF = Don't change settings							
Byte 1	Completion code							

Get Control State

This command sets the state of a control pin. This command overrides the AUTO-state of the control pin. Refer to Table 28 for control number information.

Table 26. Get Control State

	7	6	5	4	3	2	1	0
NetFn/LUN	NetFn = 3Eh (OEM Request)						RsLUN	
Command	Cmd = 21h							
Byte 1	Control number							
Byte 1	Completion code							
Byte 2	Control state, 0 = Deassert, 1 = Assert, 3 = Reserved, FF = Don't change settings							

Get Port80 Data

This command returns the last byte value written by the BIOS to Port 80 since the last System Reset. If no data has been written to the port since System Reset, the Completion Code returned is CBh.

Table 27. Get Port80 Data

	7	6	5	4	3	2	1	0
NetFn/LUN	NetFn = 30h (OEM Request)						RsLUN	
Command	Cmd = 2Dh							
Byte 1	– (BLANK)							
Byte 1	Completion code							
Byte 2	Last Port 80 code value (in HEX)							

Controls Identifier Table

Table 28 lists the control identifiers that can be used with Set/Get Control State IPMI commands to query or set information on certain controls in the firmware.

Table 28. Controls Identifier Table

Control Description	Control Number
FWH Hub (for BIOS bank information) 0	1
FWH 0 Write Protect	4
FWH 0 Top Block Lock	6

Hot-Swap Process

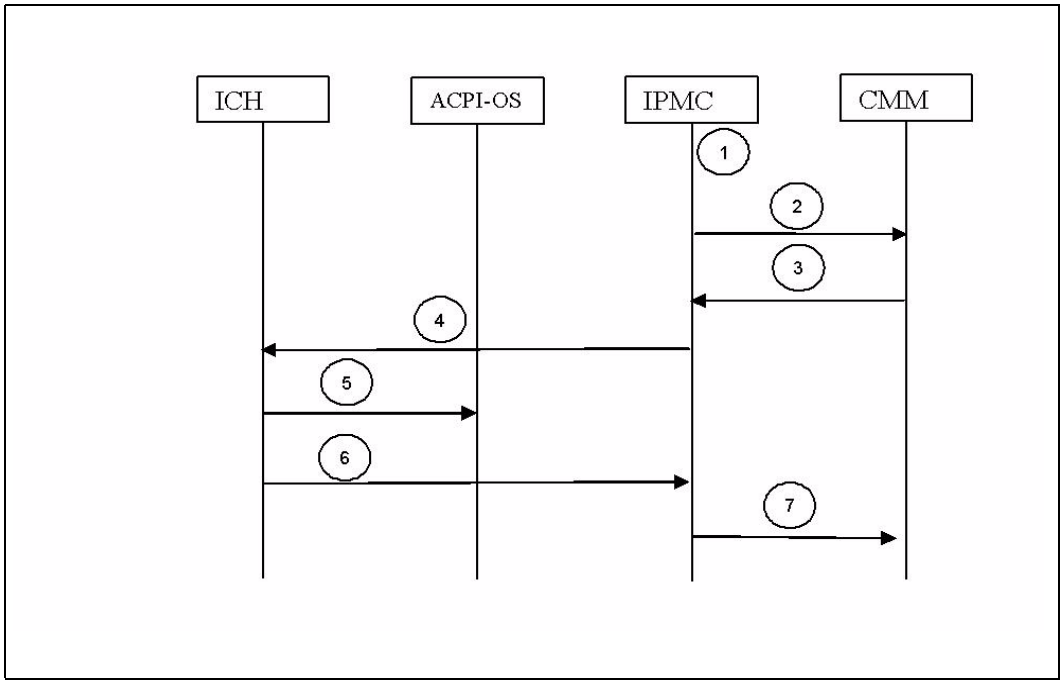
The ATCA-4200 can be hot-swapped in and out of a chassis. The onboard IPMC manages the ATCA-4200 power-up and power-down transitions. The following steps, along with Figure 27, illustrate this process.

1. Ejector latch is opened. HOT_SWAP_PB# assertion. IPMC firmware detects the assertion of this signal.
2. IPMC sends a "Deactivation Request" message to the CMM. M state moves from M4 to M5.
3. The board moves from M5 to M6 if the CMM grants the request.
4. The IPMC ACPI timer (3 minutes) starts if an ACPI-enabled OS is loaded. Otherwise, it goes to Step 7 below. The IPMC asserts a 20 ms pulse on SMC_PWRBTN#.
5. The Power Button Status register (PWRBTN_STS) is set. It then asserts SCI/SMI# to the OS. If the OS is ACPI-enabled, the SCI interrupt handler on the OS is called. The interrupt handler clears the PWRBTN_STS bits. The OS begins a graceful shutdown.

6. The Chipset detects "LOW" on the PWRBTN# and asserts SLP_S3# and SLP_S5# to IPMC. Upon detection of SLP_S5# and SLP_S3#, the board transitions to Step 7. If the chipset does not assert the signals, the board transitions to Step 7 upon the ACPI timer expiration.
7. The firmware deasserts payload power and sets the IPMI locked bit before it transitions from M6 to M1 state.

Note
If the upper-level software moves the IPMC to M6, the same procedure is followed, starting at Step 4.

Figure 27. Hot-Swap Process



Hot-Swap LED (DS10)

The ATCA-4200 supports one blue Hot Swap LED, mounted on the front panel. See Table 23 for its location. This LED indicates when it is safe to remove the ATCA-4200 from the chassis. The on-board IPMC drives this LED to indicate the hot-swap state. Refer to Table 29.

When the lower ejector handle is disengaged from the faceplate, the hot swap switch embedded in the PCB will assert a "HOT_SWAP_PB#" signal to the IPMC, and the IPMC will move from the M4 state to the M5 state. At the M5 state, the IPMC will ask the CMM (or Shelf Manager) for permission to move to the M6 state. The Hot Swap LED will indicate this state by blinking on for about 100 milliseconds, followed by 900 milliseconds in the off state. This will occur as long as the ATCA-4200 remains in the M5 state. Once permission is received from the CMM or higher-level software, the ATCA-4200 will move to the M6 state.

The CMM or higher level software can reject the request to move to the M6 state. If this occurs, the Hot Swap LED returns to a solid off condition, indicating that the ATCA-4200 has returned to M4 state.

If the ATCA-4200 reaches the M6 state, either through an extraction request through the lower ejector handle or a direct command from higher-level software, and an ACPI-enabled OS is loaded on the ATCA-4200, the IPMC communicates to the OS that the module must discontinue operation in preparation for removal. The Hot Swap LED continues to flash during this preparation time, just like it does at the M5 state. When main board power is successfully removed from the ATCA-4200, the Hot Swap LED remains lit, indicating it is safe to remove the ATCA-4200 from the chassis.

WARNING
Removing the ATCA-4200 prematurely can lead to device corruption or failure.

Table 29. Hot-Swap LED (DS11)

LED Status	Meaning
Off	Normal status
Blinking Blue	Preparing for removal/insertion: Long blink indicates activation is in progress, short blink when deactivation is in progress.
Solid Blue	Ready for hot swap

Ejector Mechanism

In addition to captive retaining screws, the ATCA-4200 has two ejector mechanisms to provide a positive cam action; This ensures the blade is properly seated. The bottom ejector handle also has a switch that is connected to the IPMC to determine if the board has been properly inserted.

Error Reporting

The MCH handles error reporting from the memory subsystem. Errors consist of correctable and uncorrectable bit errors. The ECC algorithms used are capable of correcting any number of bit errors contained within a 4-bit nibble. In addition, any number of bit errors contained within two 4-bit nibbles is detected. The MCH communicates these errors to the ICH via special cycles over the hub link interface. These special cycles indicate to the ICH that an MCH-detected error has occurred. The MCH special cycle communicates the type of event that should be generated by the ICH when an error is detected. Selection for the generation of an SERR, SMI, or SCI event is provided. Status for these reported errors is then found in the MCH DRAM_FERR (first error) and DRAM_NERR (next error) status registers. Refer to the MCH data sheet for more information (see *Reference Documents* on page 8).

Correctable memory errors generate an SMI and are logged by IPMI as SEL. Non-correctable errors first generate an SMI (which generates a SEL) and then an NMI.

Each P64H2 device reports the PCI errors that occur on the buses to which it is attached. These consist of the PCI error assertions of the PERR# or SERR# signals. The errors are reported by sending the DO_SERR special cycle to the MCH on the hub interface. The MCH forwards the error to the ICH, which generates the appropriate error condition to the processor(s) such as NMI, SMI, or SCI.

PCI address parity errors are considered catastrophic and may abort further data transfers by the P64H2 if that is the programmed response. Parity/ECC is checked on both the hub interface and PCI bus transactions. PCI data parity errors are considered less severe and allow transactions to continue. Data parity errors cause the "Detected Parity Error" status to be logged and, if enabled, the DO_SERR special cycle is transmitted. In a transaction where a data error occurs, the data being forwarded to the next bus is "poisoned" to ensure the error follows the data to its destination. Poisoned data has bad parity or multi-bit ECC errors introduced before being forwarded to the next bus.

PCI assertions of the SERR# signal also result in the DO_SERR special cycle being generated on the hub interface when enabled. Other potential causes for a DO_SERR special cycle include:

- Parity errors on the target bus during a write.
- A master timeout on a delayed transaction.
- The occurrence of a PCI master abort cycle.

Refer to the *P64H2 Data Sheet*, section 4.9, for more information on error handling. For details on obtaining this document, see *Reference Documents* on page 8

The ICH device has the ability to report PCI and hub link errors directly to the processors. When a PERR# or SERR# occurs on the ICH local PCI bus, the ICH can be programmed to generate NMI or SMI. The ICH also fields messages from the MCH and its attached hub devices to indicate errors to the processors on their behalf. The messages may request SMI#, SCI, NMI, or SERR3 to be asserted. Software must check the MCH and attached hub devices to determine the exact cause of the error. Refer to the *ICH Data Sheet* for more information on error handling and generation. For details on obtaining this document, see *Reference Documents* on page 8

ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with theATCA-4200 requires an operating system that provides ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration) and APM support (normally contained in the BIOS).
- Power management control of individual devices, add-in boards (some PMC cards may require an ACPI-aware driver), and hard-disk drives.
- A soft-off feature that enables the operating system to power off the computer.
- Support for an IPMC firmware command switch.

System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 30 lists the power states and the associated system power targets supported by the ATCA-4200. See the *ACPI Specification* for a complete description of the various system and power states.

Table 30. Power States and Targeted System Power

Global States	Sleeping States	Processor States	Device States
G0 – working state	S0 – working	C0 – working	D0 – working state.
G1 – sleeping state	S4 – Suspend to disk. Context saved to disk.	No power	D3 – no power except for wake up logic.
G2/S5	S5 – Soft off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake up logic.
G3 – mechanical off AC power is disconnected from the computer.	No power to the system.	No power	D3 – no power for wake up logic, except when provided by battery or external source.

The watchdog timer on the IPMC can be configured and used through standard IPMI v1.5 watchdog timer commands. Refer to *WDT #1* on page 85 for detailed information.

Reset Types

Reset Logic

The following topics describe the two types of reset requests and the boot relationships between them. The two types of reset requests available on the ATCA-4200 are:

- Hard reset request (always results in a cold boot)
- Soft reset request (can result in either a warm or cold boot)

A hard reset request occurs whenever the processor Reset line is asserted and then de-asserted. A soft reset occurs whenever an assertion occurs on the processor Init line. Whenever a soft reset request occurs, the BIOS checks two memory locations to determine whether to initiate a warm boot while leaving main memory intact or a cold boot that clears memory.

Whenever the BIOS detects that the reset is either a hard reset or a cold boot, it specifically clears the memory location 40h:72h so it does not contain a 1234h. Under warm boot conditions, this memory location contains a 1234h (the developer's application writes this value in this location [using /dev/mem] when it is started). If a hard reset occurs (as defined in the hard reset topic below), it is certain that the 40h:72h location contains a non-1234h value.

Hard Reset Request

A Hard Reset, or CPU Reset, is defined as the assertion of the processor reset signal (see Table 31). This initializes the processor state and registers, disables internal caches, and causes the processor to unconditionally begin execution from the reset vector. A hard reset is initiated by the following events:

1. A power up of the ATCA-4200. The SMC enables the onboard power supplies.
2. The SMC negates the PWROK signal (see Note below).
3. A "reset" command from the Port CF9h I/O register (refer to the "Intel® 6300ESB I/O Controller Hub Datasheet" for information about this register).
4. Watchdog timer (WDT #1) expires and is configured to initiate a hard reset. See *Watchdog Timers (WDTs)* on page 85 for more information.
5. Watchdog timer (WDT #3) expires after failure to perform the first instruction fetch.
6. A command (cmmset -l bladex -d powerstate -v reset) is issued from MPCMM0001.

Note
The IPMC can negate the dedicated signal PWROK to initiate a processor reset. PWROK indicates whether power is OK. If the IPMC deasserts PWROK, the hardware asserts the processor reset lines.

Soft Reset Request

The assertion of the processor's INIT signal causes a soft reset or "CPU INIT" (see Table 31). The ICH is normally responsible for driving the IINIT signal. A CPU INIT event causes the processor(s) to fetch the reset vector at the next instruction boundary. The majority of the processor and all of the cache states are unaffected by an INIT event.

After the INIT event, hardware may be reset (or not reset) under BIOS control. PCI buses are reset using their respective bridge control registers. This signal is then level translated to the processor compatible signal level. INIT may be caused by the following events:

1. The reset button is pressed (see Note below). See for its location.
2. A processor shutdown special cycle occurred.
3. An INIT command from Port 92h I/O register. (Refer to the *Intel® 6300ESB I/O Controller Hub Datasheet* for information about this register.)
4. An INIT command from Port CF9h I/O register.
5. A keyboard reset command (RCIN# signal asserted).

6. The IPMC may also directly assert the INIT signal; WDT #1 expires and is configured for a soft reset.
7. Processor BIST is enabled and a hard reset is initiated from the Port CF9h register. This asserts the INIT signal but is not classified as a soft reset since CPU reset is also asserted.
8. OS reboot commands (eg: "shutdown -r now" or "reboot" in Linux).
9. A processor INIT may also be initiated through an APIC "init" message. This message may target a specific processor or all processors. This "init" is an internally generated event (No INIT signal is asserted) so the IPMC is unable to detect this occurrence.

Note
The reset button (RESET_PB#) is an input to the IPMC. There are also IPMI commands to reset the board and change power states through the software. However, the reset button is a last resort because the user must manually reset the board at the chassis.

After a Soft Reset/CPU Init, the BIOS code executes and determines if the reset is a warm boot or a cold boot. A warm boot restarts the system and keeps memory above the 8 MByte boundary intact. During a warm boot the MCH is not reset, allowing DRAM refresh to continue during and over the soft reset event. A cold boot sets the state of all peripherals to the same state they would be in if a hard reset were triggered.

Table 31. Reset Request

Reset Request	Signal Activated	Type
Hard	Reset	Full reboot
Soft	Init	Partial reboot

Warm Boot

A warm boot occurs when the processor is booting after a soft reset request. To qualify as a warm boot, the reset counter located at 40h:D0h must be non-zero (by default, the reset counter and reset flag are initialized to 10 and 1234h by BIOS after a cold boot.) Execution starts at the reset vector. The BIOS initializes and configures all devices except for memory. Memory contents remain intact except for the first 8 MBytes. The BIOS uses the first 8 MBytes during POST, but does not modify the reset flag or the reset counter. MCH is not reset, allowing DRAM refresh to continue during the warm boot.

Note
On every warm boot, the BIOS automatically decrements the reset counter by one. When the reset counter reaches zero and the soft reset is initiated, a cold boot occurs instead of warm boot.

Cold Boot

Any soft reset that does not meet the configuration described in *Warm Boot* on page 83, "Warm Boot" is classified as a cold boot. Execution starts at the reset vector, and BIOS initializes and configures all devices, including memory subsystem, as if a hard reset had occurred. See Table 32.

During a cold boot the BIOS initializes the warm reset counter to 0x0A and clears the reset flag to 1234h. Software can then read the reset flag to determine the type of reset.

Table 32. Reset Actions

Reset Actions	System Function	Memory Status
Warm boot	Partial restart	Preserves memory above 8MB boundary
Cold boot	Full restart	Functionally equivalent to a hard reset.

Power Good

When the ATCA-4200 is inserted into the chassis, the hardware management circuitry is "hot plugged." The hardware management voltage is immediately applied, and the on-board IPMC is reset. After the hardware management reset, the operation of the IPMC and full power-up of the ATCA-4200 are under firmware control.

When a command to power on the module is issued, the IPMC asserts the "power enable" signal to the FPGA. The FPGA sequences up the DC-DC converter and its VRM contoller. Full power-up of the ATCA-4200 is sequenced by hardware to ensure device-specific power requirements are followed. Sequencing of specific voltages is required to ensure that devices using multiple voltages are not damaged or stressed.

As the many voltages power up, each regulator produces a "power good" signal. All of these power good signals are logically OR'd (with the exception of the VRM power good) to produce the PWROK signal input to the ICH. When this signal is active, it indicates all on-board power is good.

Next, the VRM power good is gated with the PWROK signal in the ICH to produce the processor's power good signal input.

As soon as the ICH device is powered, its PCI reset output is asserted. This reset output remains asserted until all power good signals are present (indicated by the PWROK signal), the processor VRM power good signal is asserted, and device voltage/clock stabilization times have been satisfied.

Device resets are then released, and processor BIOS execution and boot begins. The PCI reset output of the ICH is the source of all other power-up reset signals.

The IPMC is also capable of initiating this power-up or global reset by negating the PWROK signal. Additionally, devices on specific PCI buses may be independently reset by software through their associated bridge devices.

When commanded to do so, the IPMC releases device and processor resets and processor BIOS execution and boot begins.

Watchdog Timers (WDTs)

There are three watchdog timers (WDTs) on the ATCA-4200.

WDT #1

The first WDT (WDT #1) is a hardware timer in the IPMC. WDT #1 is IPMI compliant; its interaction with the host processor BIOS or system software is accomplished through IPMI commands over the Keyboard Controller Style (KCS) interface to the IPMC. The host processor uses the Set Watchdog Timer message to configure WDT #1, then the Reset Watchdog Timer message to strobe the timer.

WDT #1 can be set to any value between 100 ms and 6,553,600 ms in 100 ms intervals. Another configuration parameter is an indicator of which software is controlling WDT #1. This has five state settings:

1. BIOS FRB2: Used during fault-resilient booting to detect issues in the BIOS.
2. BIOS/POST: Used while the BIOS is running through its POST operations.
3. OS Load: Set by the BIOS just before an OS load, then reset by the OS (the OS must be enabled to do so) when it finishes booting.
4. SMS/OS: Used by the system management software or the OS.
5. OEM: Used by any OEM software.

WDT #1 can also be configured to take various actions before timing out (for example, SMI, NMI, nothing) or after timing out (for example, hard reset, power down, or power cycle). In addition, an event can be logged into the SEL whenever the watchdog timer expires. If WDT #1 expires, the IPMC is not reset. For more details on the watchdog timer commands and settings, see the IPMI Specification version 1.5.

On power up, the initial state is that the IPMI WDT #1 is not running. Normally some code (BIOS or OS level) must send the Reset Watchdog Timer command to start the timer running. The same code sends a Set Watchdog Timer command first to set up the timer to a known state (see the IPMI Specification for more details).

When WDT #1 times out, it logs an event into the SEL, provided that the "Don't Log" flag is false (see the IPMI 1.5 Specification for details). The SEL event also describes the timeout action taken.

If WDT #1 times out and causes a hard reset, the timer state is equivalent to the power-up state (that is, not running; either BIOS or the OS must configure and start it). If the host processor is reset (soft or hard) independent of WDT #1, the firmware disables the watchdog timer.

One of the actions BIOS takes very early in its code is to start the WDT #1 to monitor its boot progress. When it finishes POST, the BIOS turns off WDT #1 during the OS load period.

WDT #1 parameters are altered according to BIOS control parameters, and WDT #1 is not running when the OS first (re)starts. The BIOS sets WDT #1 to a length of time longer than the expected POST time; therefore, BIOS does not actively strobe WDT #1.

The flag that determines if a WDT #1 reset must be hard or soft remains over any type of reset, since it is held in the microcontroller.

WDT #2

WDT #2 (implemented in a PLD) must be strobed by the IPMC firmware. If WDT #2 expires, it isolates the ATCA-4200 from the backplane IPMB buses and resets the IPMC. There is no method for the processor to be explicitly notified that the IPMC is reset. Once the IPMC has reset, the main processors can resume communication with the IPMC. The watchdog timer is set to trigger after 96 seconds, and the IPMC strobes it once a second.

WDT #2 is always running; that is, the counter is always counting. However, a PLD component controls the IPMC reset and IPMB isolation associated with WDT #2 expiration, ignoring any WDT event until the IPMC strobes/enables the LTC4300 IPMB interfaces.

WDT #3

WDT #3 is contained within the ICH device. This watchdog timer monitors the processor's first attempt to fetch an instruction after a power up or hard reset. If the processor has not fetched its first instruction within the timeout period, the ICH resets the processors. Since the processor has not begun any execution, the ICH uses a hard reset.

LED Status

Health LED

The ATCA-4200 supports one bicolor health LED to indicate the ATCA-4200's health status, i.e., whether a fault or error condition has been detected on the ATCA-4200. This LED is mounted on the front faceplate and driven by the onboard IPMC. The health LED will only be driven to an error condition (red) if there is a critical or non-recoverable (major or critical in AdvancedTCA parlance) condition active on the ATCA-4200. Alarms could include exceeding sensor thresholds for temperature and on-board logic voltages. The health LED remains red until the sensors return to a normal operating value. Hard-drive failures, boot failures, etc. are not considered critical/major IPMI states, so the IPMC does not explicitly set the health LED in these cases.

Note
The LED's error state color defaults to red, but the color can be overridden using PICMG 3.0-defined commands.

Table 33. Health LED

LED Status (right)	Meaning
Solid Green	Healthy
Solid Amber/Red	Fault or error condition

The default color and override capabilities of the LED follow the LED management requirements defined in Section 3.2.5 of the PICMG 3.0 Specification.

OOS (Out Of Service) LED

The ATCA-4200 supports one bicolor "OOS" LED, mounted on the front faceplate. The LED can be driven to display a red or amber color. When this LED is lit, it indicates that the board is not in service. Its back-end (payload) power could be OFF or ON. Often the OOS state is entered when a critical fault occurs on the board. In this state, the back-end (payload) power is turned OFF. A board could be in this state when its back-end power is OFF but healthy, or when a board is fully powered but not yet deployed, or during the reset process.

Note
Do not extract a board unless the Hot Swap LED is lit.

Table 34. OOS LED (DS9)

LED Status (left)	Meaning
Off	In service
Solid Amber/Red	Fault or error condition

The default color and override capabilities of the LED follow the LED management requirements defined in Section 3.2.5 of the PICMG 3.0 Specification.

Hot-Swap LED

See *Hot-Swap Process* on page 77.

IDE Drive Activity LED

Table 35. IDE Drive Activity LED

LED Status	Meaning
Off	Normal/No disk access
Green (Blinking)	Disk access (read/write activity)

User-Programmable LEDs

The ATCA-4200 provides two bicolor LEDs for user-programmable functions. The LEDs can be driven to display a red, green or amber color. When these LEDs are lit, they indicate a status of a user-defined function.

Table 36. User-Programmable LEDs

LED Status (left)	LED Status (right)	Meaning
Off	Off	No Status
Red	Red/Green	Active Status of user defined function

The user-programmable LEDs are connected to the GPIO pins on the ICH device as follows:

Table 37. GPIO Pin Connections

LED	Pin
User_Prog_LED1_Red#	GPIO21
User_Prog_LED1_GRN#	GPIO20
User_Prog_LED2_Red#	GPIO28
User_Prog_LED2_GRN#	GPIO23

By programming the ICH GPIO registers as outputs, then selecting the appropriate state (low for illumination, high for off), the user enables the LEDs as required. Refer to the *ICH datasheet* section in *Reference Documents* on page 8 for specific GPIO 20, 21, 23, 28 register information.

Network Link/Speed LEDs

The front panel of the ATCA-4200 provides two LEDs for each Ethernet connection indicating the speed and link activity for that network connection:

Table 38. Network Link LEDs

For Channel A : L2 / For Channel B : L6	
Link LED Status	Meaning
Off	No link
Solid Green	Link established
Blinking Green	Link with activity

Note: Refer to Figure 23 for LED (L2 and L6) placement on the Front Panel.

Table 39. Network Speed LEDs (Sheet 1 of 2)

For Ethernet controller Channel A : L3 & L4		
Speed LED Status		Meaning
L3	L4	
Solid Yellow	Off	1 Gbps connection
Off	Solid Green	100 Mbps connection

Table 39. Network Speed LEDs (Sheet 2 of 2)

For Ethernet controller Channel A : L3 & L4		
Off	Off	10 Mbps connection
For Ethernet controller Channel B : L7 & L8		
Speed LED Status		**Meaning**
L7	**L8**	
Solid Yellow	Off	1 Gbps connection
Off	Solid Green	100 Mbps connection
Off	Off	10 Mbps connection

Note: Refer to Figure 22 and Figure 23 for LED (L3, L4, L7 and L8) placement on the Front Panel.

Ethernet Controller Port State LEDs

The front panel of the ATCA-4200 provides a bicolor LED for each Ethernet channel that can light to indicate the Ethernet port state. These LEDs can display a red, green or amber color. The function of the port state LEDs is user definable. The Ethernet Controller SDP[6:7] GPIO bits for each channel are the outputs that control the LEDs. SDP[6] is connected to the Green LED, and SPD[7] is connected to the Red LED.

Refer to the documentation for the Intel® 82546 Dual Gigabit Ethernet Controller for information on how to drive these LED signals. Note that existing network drivers may drive these GPIO pins.

Table 40. Ethernet Controller Port State LED

LED Status (L1 and L5)	Meaning
Off	No Status
Red/Green/Amber	Active status of user-defined function

Note: Refer to Figure 22 and Figure 23 for LED (L1 and L5) placement on the Front Panel.

FRU Payload Control

The ATCA-4200 implements the "FRU Control" command as specified in the PICMG 3.0 Specification. Through this command, the payload can be reset, rebooted, or have its diagnostics initiated.

The FRU payload can be controlled by a command line via the Intel NetStructure® MPCMM0001 Chassis Management Module (CMM). The following CMM commands are supported by the ATCA-4200.

Table 41. CMM Commands for FRU Control Options

FRU Control Options	MPCMM0001 equivalent command
Cold Reset	cmmset –l bladex –d frucontrol –v 0
Warm Reset	cmmset –l bladex –d frucontrol –v 1
Graceful Reboot	cmmset –l bladex –d frucontrol –v 2
Diagnostic Interrupt	cmmset –l bladex –d frucontrol –v 3

Note

The user may issue an RMCP command to control the FRU payload as well. Refer to Table 76 for the associated IPMI command information.

Cold Reset

When this command is initiated, the board will perform a hard reset as described in *Hard Reset Request* on page 82.

Warm Reset

When this command is initiated, the board will perform a soft reset as described in *Soft Reset Request* on page 82.

6 Specifications

This section defines the ATCA-4200 operating and storage environments. It also documents the procedures used to determine the reliability of the ATCA-4200.

Mechanical Specifications

Board Outline

The ATCA-4200 form factor is mechanically compliant with the PICMG 3.0 Specification of 322.25 mm x 280.00 mm (12.69" x 11.16"). The board pitch is 6HP, and the PCB thickness is 2.36 mm (±0.14 mm).

Figure 28 shows the locations of major components on the ATCA-4200. board. Table 42 lists the components shown in the illustration.

Figure 28. Component Layout

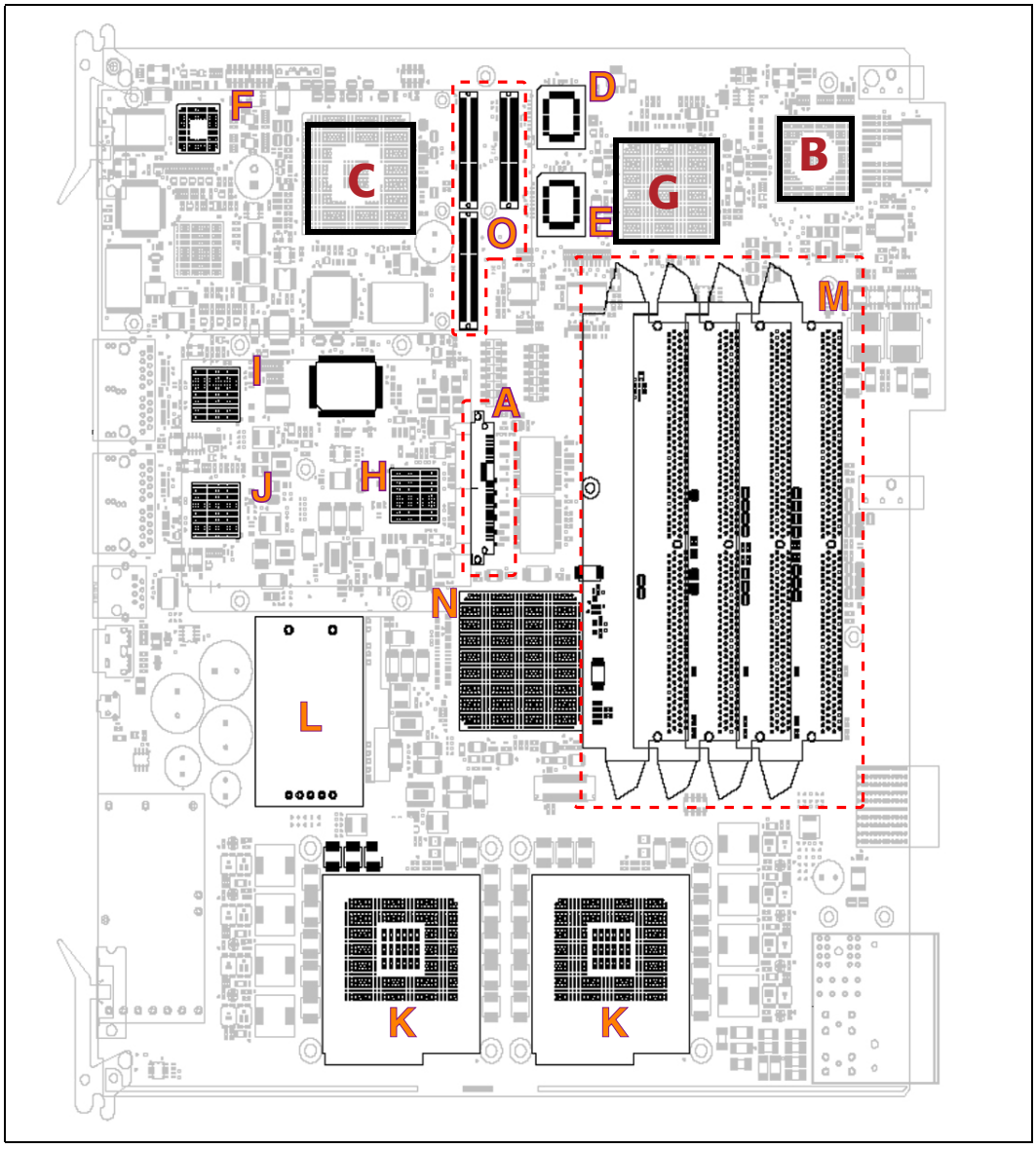


Table 42. Board Components

	Component/Function
A	SAS Hard Disk Connector
B	LSI* 1064 SAS Controller
C	Intel® E6300 ESB
D	FWH0 (Main BIOS)
E	FWH1 (Backup BIOS)
F	Sahalee Microcontroller (IPMC)
G	Intel® 6700PXH

Table 42. Board Components (Continued)

	Component/Function
H	Intel® 82571EB Gigabit Ethernet Controller (Base Interface)
I	Intel® 82571EB Gigabit Ethernet Controller (Fabric Interface)
J	Intel® 82571EB Gigabit Ethernet Controller (Fabric Interface)
K	Intel® Xeon2.8GHz LV Processors with 1MB L2 Cache
L	Tyco* PIM200F Power Module
M	DDR2 Memory Bank
N	Intel ® E7520 Memory Controller Hub (MCH)
O	Connectors for PMC1

Backing Plate and Primary Side Top Cover

The ATCA-4200 has a rugged metal backing plate that forms a single-piece faceplate. This backing plate is made of zinc plated, commercial quality, cold rolled steel. The backing plate and integral faceplate are nominally 1.2mm thick. The top cover is made of zinc plated commercial quality cold rolled steel and is nominally 1.2mm thick.

Two optional holes are provided in the bottom of the backing plate near the faceplate for the PMC location. These holes can be used to secure the PMC in addition to the rear standard mounting positions, using standoffs in the accessory kit.

CAUTION
Removing the backing plate can damage the components on the board and may void the warranty. No user-serviceable parts are available under the PCB. Do not remove the faceplate or backing plate.

Environmental Specifications

The ATCA-4200 meets the board-level specifications as specified in the *Intel Environmental Standards Handbook – Telco Specification* Document No. A78805-01. The test methodology is a combination of Intel and NEBS test requirements with the intent that the product will pass pure system-level NEBS testing. Intel will not be completing NEBS testing on the ATCA-4200. The following table summarizes environmental limits, both operating and nonoperating.

Table 43. Environmental Specifications

Parameter	Conditions	Detailed Specification
Temperature (Ambient)	Operating	0 to 55°C
	Storage	-40 to 70° C
Airflow	Operating	30 cubic feet per minute (CFM) minimum
Humidity	Operating	15%-90% (non-condensing) at 55° C
	Storage	5%-95% (non-condensing) at 40° C
Altitude	Operating	4,000 m (13,123 ft.) Note: may require additional cooling above 1800 m (5,905 ft.)
	Storage	15,000 m (49,212 ft.)
Unpackaged Vibration	Operating	Sine sweep: • 5 to 100 Hz: 1G @ 0.25 Octave/minute • 100 to 500 Hz: 1G @ 1 Octave/minute Random profile: • 5 Hz @ 0.01 g2 /Hz to 20 Hz @ 0.02 g2 /Hz (slope up) • 20 Hz to 500 Hz @ 0.02 g2 /Hz (flat) • 3.13 g RMS, 10 minutes per axis for all three axes
	Storage	5 to 50 Hz: 0.5G @ 0.1 Octave/minute 50 to 500 Hz: 3G @ 0.25 Octave/minute.
Shock	Operating	30G/11 ms half sine
	Storage	50G, 170 inches/second trapezoidal

Reliability Specifications

Mean Time Between Failure (MTBF) Specifications

Calculation Type: MTBF/FIT Rate

Standard: Telcordia* Standard SR-332 Issue 1

Methods: Method I, Case I, Quality Level II

The calculation results were generated using the references and assumptions listed. This report and its associated calculations supersede all other released mean time between failures (MTBF) and Failure in Time (FIT) calculations with earlier report dates. The reported failure rates do not represent catastrophic failure. Catastrophic failure rates will vary based on application environment and features critical to the intended function.

Table 44. Reliability Estimate Data

Failure Rate (FIT)	9616 failures in 10^9 hours
MTBF	103,986 hours

Note: The MTBF data is calculated without the hard disk and memory DIMMs installed.

Environmental Assumptions

- Failure rates are based on a 40°C ambient temperature.
- Applied component stress levels are 50% (voltage, current, and/or power).
- Ground, fixed, controlled environment with an environmental adjustment factor equal to 1.0.

General Assumptions

- Component failure rates are constant.
- Board-to-system interconnects are included within estimates.
- Non-electrical components (screws, mechanical latches, labels, covers, etc.) are not included in estimates.
- The printed circuit board is considered to have a 0 FIT rate.

General Notes

- Method I, Case I = Based on parts count. Equipment failure is estimated by totaling device failures rates and quantities used.
- Quality Level II = Devices purchased to specifications, qualified devices, vendor lot-to-lot controls for AQLs and DPMs.

Where available, direct component supplier predictions or actual FIT rates have been used.

The ATCA-4200 MTBF does not include addition of the PMCs. Please contact the PMC manufacturer for specific component and relevant operational MTBF information.

Power Consumption

The power consumed by the ATCA-4200 is dependent on the configuration. Below are typical consumption values.

Table 45. Power Requirements

Operating Modes	Voltage
Normal	-43 VDC to -72 VDC
Degraded	-38 VDC to < -43 VDC
Non-Operating	0 VDC to < -38 VDC, -72 VDC to -75 VDC

Note: These voltages assume a 1 V round trip drop on power signals between shelf power input terminals and board/module slots.

Note
IPMC will be powered with input voltage as low as -36 V to -38 V.

Table 46. Total Measured Power

Memory	Power
16 GByte (Four 4 Gbyte DIMMs)	Typical power = 173W Max power = 198W
8 GByte (Four 2 Gbyte DIMMs)	Typical power = 165W Max power = 190W

Board Layer Specifications

- Material: TG180 FR4
- Layers: 14
- Copper:
  - Outer layers 1 and 14 are 0.5 oz. copper + plating.
  - Internal Plane Layers 2, 5, 6, 9, 10, and 13 are 1.0 oz. copper.
  - Internal Signal Layers 3, 4, 7, 8, 11 and 12 are 0.5 oz. copper.

Cooling Requirements

The ATCA-4200 should be installed vertically in a chassis, with bottom-to-top airflow. Airflow is expected to be distributed across the bottom edge of the installed ATCA-4200 blade and to maintain at least 390 lfm average airflow.

- Most components on the ATCA-4200 blade are specified to operate with a localized ambient temperature up to 70° C and do not require heat sinks.
- The ATCA-4200 blade uses Intel-designed custom heat sinks. Below are the components on the board that have heat sinks installed.
  - Processors
  - Memory Controller Hub (Intel® E7520 Memory Controller Hub (MCH) Chipset)
  - PCI Bridge (Intel® 6700PXH 64-bit PCI Hub)
- The rate of airflow specified here is critical to ensuring that the blade operates as designed.

Dimensions and Weight

Mechanical dimensions are shown in the "PCB Dimensions" illustration and are outlined below.

- PCB Dimensions: 283.54mm x 322.5mm x 2.4mm (11.16" x 12.69" x 0.094")
- Board Dimensions: 8U (14 inches) x 6HP (one slot)
- Weight: 8.81lbs w/ dual processors, heat sink, 8GB memory (4 x 2GB), and 1 SAS Hard Drive

Figure 29. PCB Dimensions

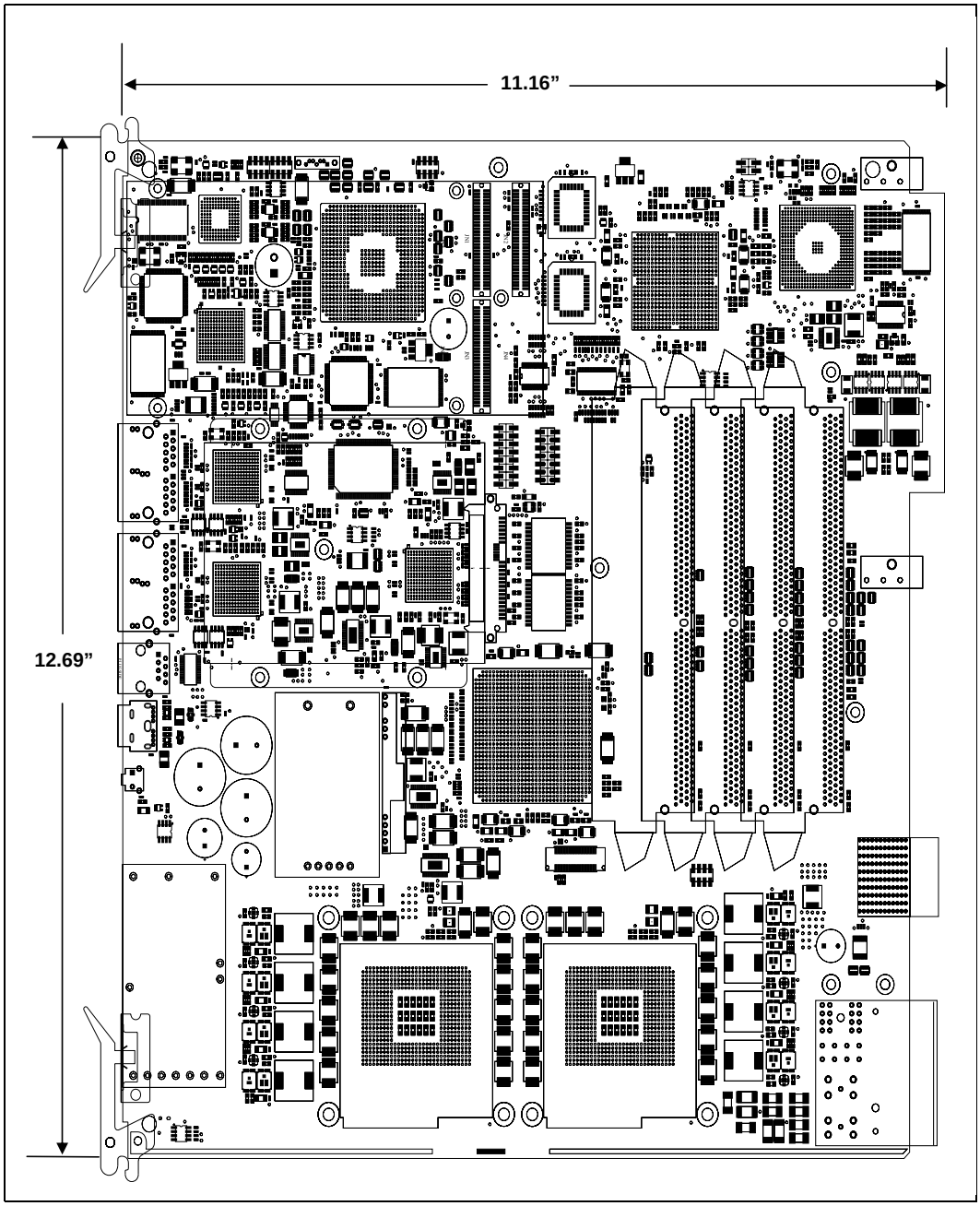


Table 47 shows the serviceable screws and the torque setting for each.

Table 47. User-Serviceable Screws and Torque Settings

Location	Torque (in in-lbs)
Top cover to chassis screws	5 -- 7 in-lbs
Hard driver bracket to hard drive screws	5 -- 7 in-lbs
PMC screws	3 -- 5 in-lbs

7 Maintenance

Supervision

The table below lists the main components that perform hardware monitoring of voltages and timers.

Table 48. Hardware Monitoring Components

Component	Function	Monitors
Intelligent Platform Management Controller	WDT #1	Commands from the BIOS. If the timer expires (times out), causes a hard reset, power down, or power cycle and IPMI event.
LM93	Voltage/Temperature	Monitor on-board voltages/temperature, processor thermal diodes, CPU "PROCHOT", and Processor VID.
Intelligent Platform Management Controller	WDT #2	Strobed by IPMC firmware. If it expires, it isolates the ATCA-4200 from the backplane IPMB buses, and resets the IPMC. Also performs fail safe field upgrade of the IPMC.

Diagnostics

In-Target Probe (ITP)

The ITP connector allows connection of a tool to help you observe and control the step-by-step execution of your program in order to debug the hardware and software. Debugging includes finding a hardware or software error and identifying the location and cause of the error so it can be corrected.

RadiSys continually looks for ways to maximize the development and delivery of mission-critical tools to our internal validation teams and strategic OEM customers. As a result, RadiSys has put together a third-party vendor program team. This team works with third-party vendors to develop and deliver specific tools formerly supplied by RadiSys to internal and external customers.

RadiSys recommends visiting any of the web sites below, and selecting a vendor of your choice to provide in-circuit emulation hardware and software.

- American Arium* currently develops in-circuit emulation and run control tools for Intel processors for use by Intel BIOS and driver teams, RadiSys manufacturing, and OEM customers.

  www.arium.com/

- Agilent Technologies* currently develops logic analyzer and probing tools for Intel processors for use by RadiSys validation teams (chip, system, platform) and OEM customers.

  www.agilent.com

- Tektronix* currently develops logic analyzer and probing tools for Intel processors for use by RadiSys validation teams (chip, system, platform) and OEM customers.

  www.tek.com/Measurement/logic_analyzers/index.html

8 BIOS Features

Introduction

The ATCA-4200 uses an Intel/AMI* BIOS, which is stored in flash memory and can be updated remotely or locally. In addition to the BIOS and BIOS Setup program, the flash memory contains POST and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code.

BIOS Flash Memory Organization

ATCA-4200 contains two Firmware Hub (FWH) devices (see Figure 1). The first device is the primary FWH, which holds the BIOS code that executes during POST. The second is the backup FWH, which recovers the system when the primary FWH is corrupted. The N82802AC FWH includes an 8 Mbit (1024 KByte) symmetrical flash memory device. Internally, the device is grouped into sixteen 64-KByte blocks that are individually erasable, lockable, and unlockable.

Complementary Metal-Oxide Semiconductor (CMOS)

CMOS RAM is a nonvolatile storage that stores data needed by the BIOS. The data consists of certain on-board configurable settings, including time and date. CMOS resides in the Intel® 6300ESB ICH and is powered by the Supercap* capacitor when the blade is powered off. The settings in the BIOS Setup menu are stored in the CMOS RAM and are often called CMOS settings.

Redundant BIOS Functionality

The ATCA-4200 hardware has two flash banks where redundant BIOS copies are stored. BIOS bank selection logic is connected to the IPMC and the IPMC firmware allows selection of the BIOS bank.

By default, firmware selects BIOS bank 0. The BIOS executes code off this flash and performs a checksum validation of its operational code. This checksum occurs in the boot block of the BIOS. If the boot block detects a checksum failure in the remainder of the BIOS, it notifies the IPMC of the failure. In case of failure, the IPMC firmware:

1. Asserts the RESET pin on the processor.
2. Switches the flash bank.
3. Deasserts the RESET pin on the processor, allowing the BIOS to execute off the second flash bank.

Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup utility and install an operating system that supports USB. Legacy USB support is enabled by default.

Note
Legacy USB support is for keyboards, mice, and hubs only. Other USB devices are not supported in legacy mode except bootable devices like CD-ROM drives and floppy disk drives.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS, allowing you to use a USB keyboard.
4. POST completes.
5. The operating system loads. USB keyboards and mice are recognized and may be used to configure the operating system. Keyboards and mice are not recognized during this period if legacy USB support was set to "Disabled" in the BIOS Setup program.
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system. Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that legacy USB support in the BIOS Setup program is set to "Enabled" and follow the operating system's installation instructions.

Language Support

English is the only supported language.

Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from the backup BIOS. Recovery mode is active when BIOS checksum fails and notifies the IPMC to failover to the backup BIOS.

Fast Booting Systems

Quick Boot

Use of the following BIOS Setup program settings reduces the POST execution time.

In the Boot Menu:

- Disable Option - ROM(s) if customer configuration does not use IBA(PXE) boot.
- Enable Quick Boot bypasses memory count and the search for a removable drive.

Note
Quick Boot is enabled by default. The boot time may be so fast that some hard drives might be not be initialized at all. If this occurs, it is possible to introduce a programmable delay ranging from 0 to 35 seconds using the BIOS Setup program, IDE Configuration Submenu, Advanced Menu, IDE Detect Time Out feature.

BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup utility and booting the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup utility. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup utility. This is the user mode.
- If only the supervisor password is set, pressing the “Enter” key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. User access to Setup corresponds to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt is displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 49 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 49. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Password to Enter Setup	Password During Boot
None	Any user can change all options	Any user can change all options	None	None
Supervisor and User	Can change all options	Based on user access level: No Access, View Only, Limited, Full Access	Supervisor or user	If password check option is set to "Setup", no password required. Otherwise requires either supervisor or user password.
Supervisor Only	Can change all options	Based on user access level: No Access, View Only, Limited, Full Access.	Supervisor (for supervisor mode) or enter only (for user mode)	If password check option is set to "Setup",no password required. Otherwise requires either supervisor password or enter only.
User Only	Can't get into supervisor mode until user password is cleared.	Can change all options	User	If password check option is set to "Setup", no password required. Otherwise requires user password.

Remote Access Configuration

Remote access using serial console redirection lets users monitor the ATCA-4200 boot process and run the ATCA-4200 BIOS Setup from a remote serial terminal. Connection is made directly through a serial port.

The console redirection feature is useful in cases where it is necessary to communicate with a processor board in an embedded application without video support.

Note
The default settings used for console redirection to the serial port are 115200, n, 8, 1, and no flow control.

Table 50 shows the escape code sequences that may be useful for things like BIOS Setup if function keys cannot be directly sent from a terminal application:

Table 50. Function Key Escape Code Equivalents

Key	Escape Sequence	Note
F1	ESC OP	
F2	ESC OQ	
F3	ESC OR	To select boot device
F4	ESC OS	To enter BIOS Setup
F5	ESC OT	
F6	ESC OU	
F7	ESC OV	
F8	ESC OW	
F9	ESC OX	
F10	ESC OY	To save and exit Setup
F11	ESC OZ	
F12	ESC OI	PXE boot

9 BIOS Setup

Introduction

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the Delete key from a keyboard or the (F4) key on the serial console after the Power-On Self-Test (POST) begins and before the operating system boot begins. Table 51 lists the BIOS Setup program menu items.

Table 51. BIOS Setup Program Menu Bar

Main	Advanced	Boot	Security	Exit
Provides System Overview, FPGA Version, Time/Date	Configures advanced chipset features	Selects boot options	Sets passwords and security features	Saves or discards changes to Setup program options

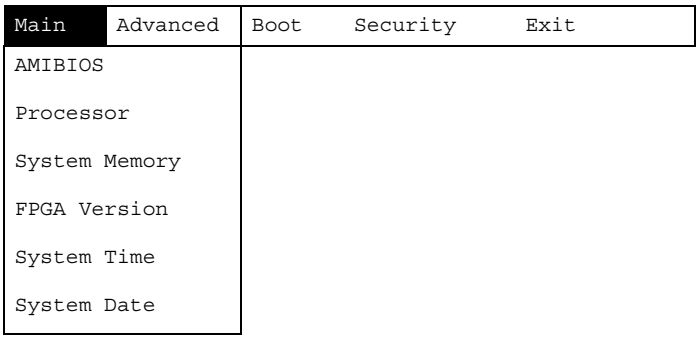
Table 52 lists the function keys available for menu screens.

Table 52. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (moves the cursor left or right).
<↑> or <↓>	Selects an item (moves the cursor up or down).
<Tab>	Selects a field (not implemented).
<Enter>	Executes command or selects the submenu.
<F9>	Loads the default configuration values for the current menu.
<F10>	Saves the current values and exits the BIOS Setup program.
<Esc>	Exits the menu.

Main Menu

To access this menu, select Main on the menu bar at the top of the screen.

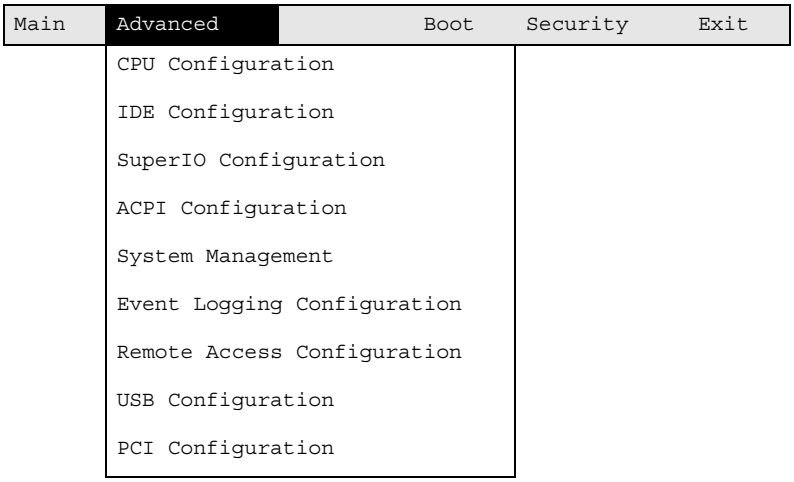


Advanced Menu

Table 53. Main Menu Options

Feature	Options	Description
AMIBIOS	AMIBIOS version Build date ID	Displays the BIOS ID.
Processor	Type Speed Count	Reports processor type, speed, and CPUID.
System Memory	Size	Displays system memory size.
FPGA	Version	Displays the version of the FPGA
System Time	Hour/Minute/Second	Specifies the current time.
System Date	Day of week Month/day/year	Specifies the current date.

To access this menu, select Advanced on the menu bar at the top of the screen.



Under the Advanced menu, the following warning message appears:

"WARNING: Setting the wrong values in the sections that follow may cause system to malfunction."

This is a warning message to users to not modify the settings unless they are familiar with the items. To restore factory defaults, select Exit, then Load Optimal Defaults.

Table 54 describes the Advanced menu, which sets advanced chipset features.

Table 54. Advanced Menu Options

Feature	Options	Description
CPU Configuration	Select to display submenu	Display CPU details, Enable/Disable Intel® Hyper-Threading™ Mode.
IDE Configuration	Select to display submenu	IDE Configuration for dual onboard Flash Disks
SuperIO Configuration	Select to display submenu	Configure SuperIO Chipset Smc27x
ACPI Configuration	Select to display submenu	Enable/disable ACPI support for OS and configure ACPI settings.
System Management	Select to display submenu	View FRU (Board and Product), BMC Device and FW Information
Event Logging Configuration	Select to display submenu	Mark, clear, or view event log. Configure error logging supported by BIOS.
Remote Access Configuration	Select to display submenu	Configure Remote Access
USB Configuration	Select to display submenu	Configure the USB Support
PCI Configuration	Select to display submenu	Section for Advanced PCI Configuration

CPU Configuration Submenu

To access this submenu, select Advanced on the menu bar, then CPU Configuration.

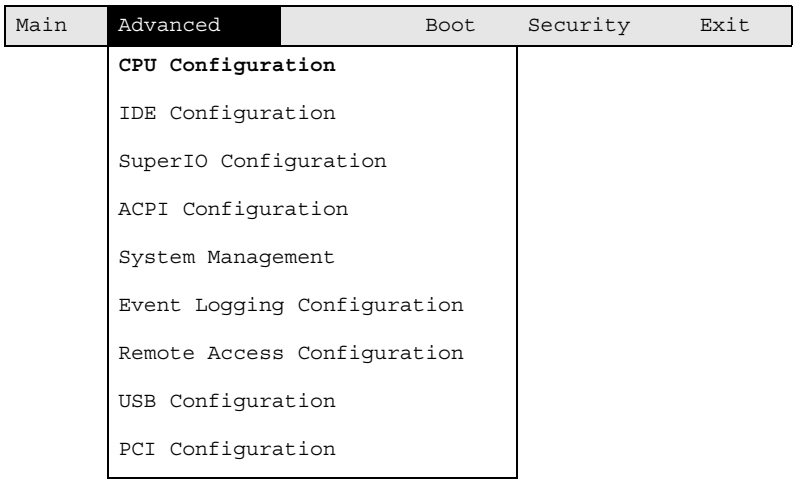


Table 55. CPU Configuration Submenu Options

Feature	Options	Description
Manufacturer		Display CPU manufacturer.
Brand String		Display CPU brand string.
Frequency		Display CPU frequency.
FSB Speed		Display front side bus speed.
Cache L1		Display L1 cache size.
Cache L2		Display L2 cache size.
Intel® Hyper-Threading™ Function	Disabled Enabled	Enable/Disable Hyper-Threading Functionality.

Note: Bold text indicates default setting.

IDE Configuration Submenu

To access this submenu, select Advanced on the menu bar, then IDE Configuration.

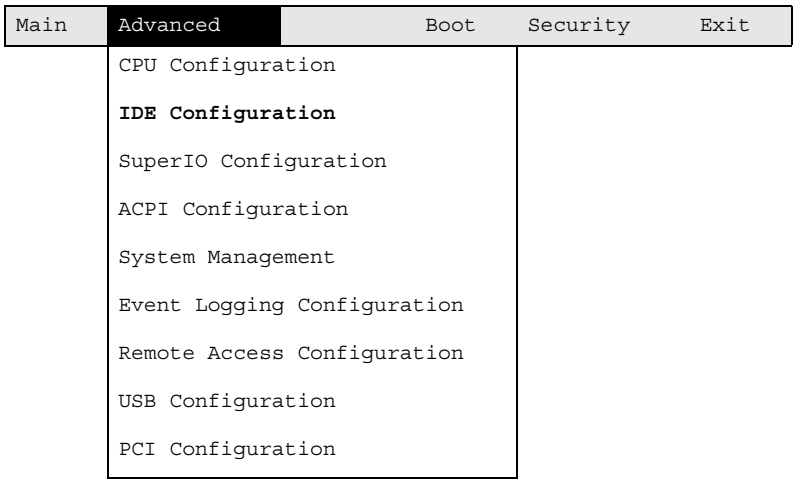


Table 56. IDE Configuration Submenu Options

Feature	Options	Description
IDE Configuration	Enabled Disabled	Enable or Disable the Onboard PCI IDE conroller.
Hard Disk Write Protect	Enabled Disabled	Disable/Enable device write protection. This will be effective only if device is accessed through BIOS.
IDE Detect Time Out	0 5 10 15 20 25 30 35	Select the time out value for detecting ATA/ATAPI device(s).
ATA(PI) 80Pin Cable Detection	Host & Device Host Device	Select the mechanism for detecting 80Pin ATA(PI) Cable.

Note: Bold text indicates default setting.

Primary/Secondary IDE Master Submenu

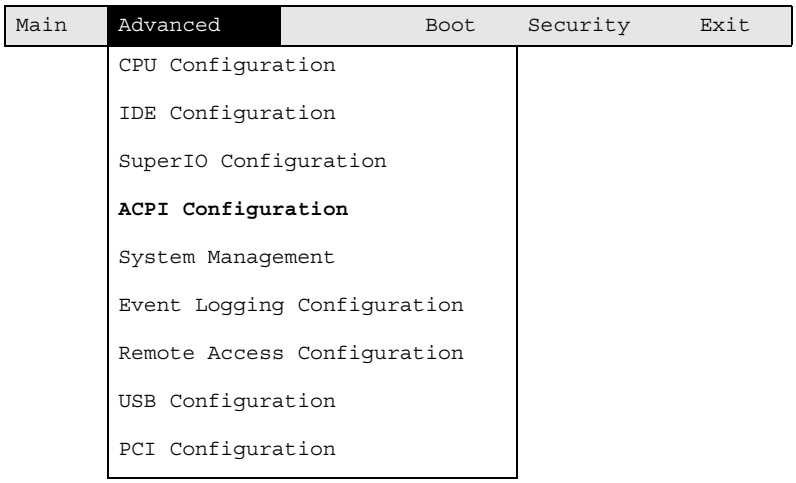
Table 57. Primary/Secondary IDE Master Submenu Options

Feature	Options	Description
Device		Display IDE device.
Vendor		Display IDE vendor name.
Size		Display IDE device size.
LBA Mode		Display IDE LBA Mode status.
Block Mode		Display IDE Block Mode status.
PIO Mode		Display PIO Mode status.
Async DMA		Display Async DMA status.
Ultra DMA		Display Ultra DMA-5 status.
S.M.A.R.T		Display S.M.A.R.T status.
Type	Not installed Auto CDROM ARMD	Select the type of IDE device connected.
LBA/Large Mode	Disabled Auto	Disable: Disable LBA ModeAuto: Enable the LBA Mode if the device supports it and the devices is not already formatted with LBA Mode disable.
Block (Multi-Sector Transfer)	Disabled Auto	Disable: The data transfer from and to the device occurs one sector at a time. Auto: The data transfer from and to the device occurs multiple sectors at a time if the device supports it.
PIO Mode	Auto 0/1/2/3/4	Select PIO Mode.
DMA Mode	Auto SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2	Select DMA Mode. Auto: Auto detected. SWDMAn: SingleWordDMAn. MWDMAn: MultiWordDMAn.
S.M.A.R.T	Auto Disabled Enabled	Enable/disable S.M.A.R.T. Auto: Enable S.M.A.R.T if the device supports it.
32 Data Transfer	Disabled Enabled	Enable/disable 32-bit data transfer.

Note: Bold text indicates default setting.

ACPI Configuration Submenu

To access this submenu, select Advanced on the menu bar, then ACPI Configuration.



There are two ACPI configuration submenus: the Advanced ACPI Configuration submenu and the Chipset ACPI Configuration submenu.

Table 58. Chipset ACPI Configuration Submenu Options

Feature	Options	Description
APIC ACPI SCI IRQ	Disabled Enabled	Enable/disable APIC ACPI SCI IRQ.

Note: Bold text indicates default setting.

Table 59. Advanced ACPI Configuration Submenu Options

Feature	Options	Description
ACPI Version Features	ACPI v1.0 ACPI v2.0 ACPI v3.0	Enable RSDP pointers to 64-bit Fixed System Description Tables.
ACPI APIC support	Disabled Enabled	Include ACPI APIC table pointer to RSDT pointer list.
AMI OEMB Table	Disabled Enabled	Include OEMB table pointer to R(x)SDT pointer lists.
Headless Mode	Disabled Enabled	Enable/disable Headless Operation mode through ACPI.

Note: Bold text indicates default setting.

System Management Submenu

To access this submenu, select Advanced on the menu bar, then System Management.

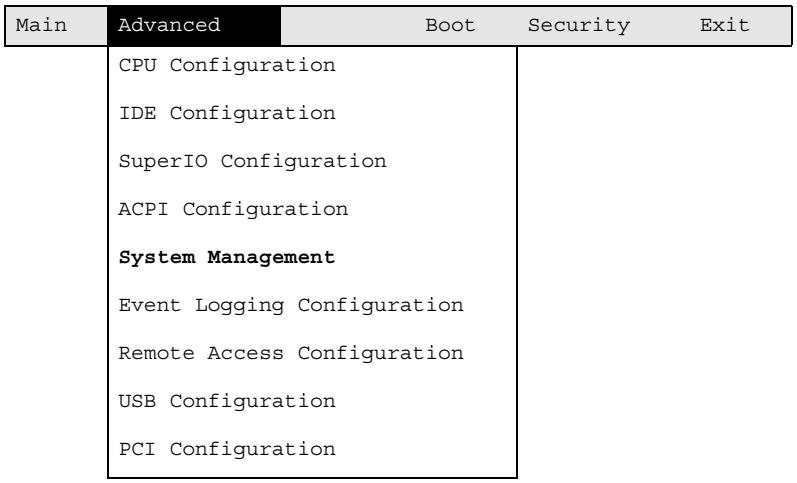


Table 60. System Management Configuration Submenu Options

Feature	Options	Description
FRU Board Information Area		Display FRU board information.
Board Product Name		
Board Serial Number		
Board Part Number		
FRU Product Information Area		Display FRU product information.
Product Name		
Product Part/Model		
Product Version Number		
Product Serial Number		
BMC Device and Firmware Information		Display BMC device and firmware information.
BMC Device ID		
BMC Firmware Revision		
BMC Revision		
SDR Revision		

Note: Bold text indicates default setting.

PCI Configuration Submenu

To access this submenu, select Advanced on the menu bar, then PCI Configuration.

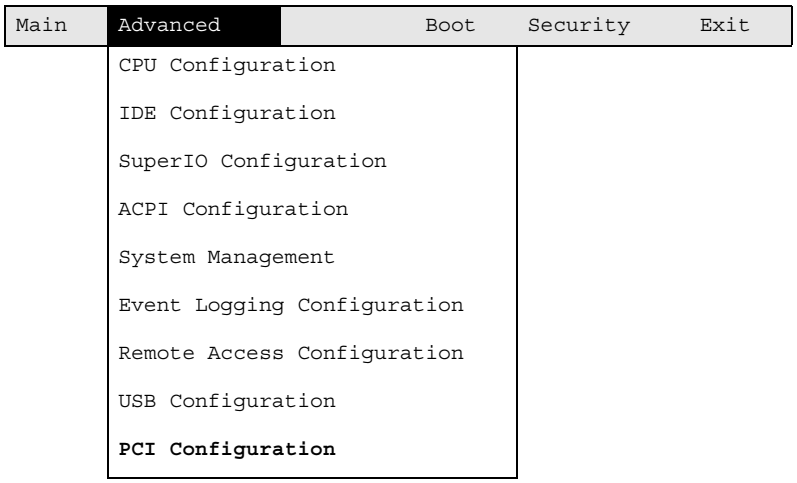


Table 61. On-Board PCI Device Settings

Feature	Options	Description
On-board SAS Controller	Disabled Enabled	Enable/disable Onboard SAS Controller
Base Gigabit LAN 1 PXE ROM	Disabled Enabled	Enable/Disable Base Gigabit LAN Option ROM.
Base Gigabit LAN 2PXE ROM	Disabled Enabled	Enable/Disable Base Gigabit LAN Option ROM.
Fabric Gigabit Controller 1	Front Fabric	Route the Gigabit Controller Ports to the Front LAN Ports or to the Fabric Interface.
Fabric Gigabit LAN 1PXE ROM	Disabled Enabled	Enable/Disable the Fabric Gigabit LAN Option ROM.
Fabric Gigabit LAN 2PXE ROM	Disabled Enabled	Enable/Disable Fabric Gigabit LAN Option ROM.
Fabric Gigabit Controller 2	Front Fabric	Route the Gigabit Controller Ports to the Front LAN Ports or to the Fabric Interface.
Fabric Gigabit LAN 1PXE ROM	Disabled Enabled	Enable/Disable the Fabric Gigabit LAN Option ROM.
Fabric Gigabit LAN 2PXE ROM	Disabled Enabled	Enable/Disable Fabric Gigabit LAN Option ROM.

Note: Bold text indicates default setting.

Event Logging Configuration Submenu

To access this submenu, select Advanced on the menu bar, then Event Logging Configuration.

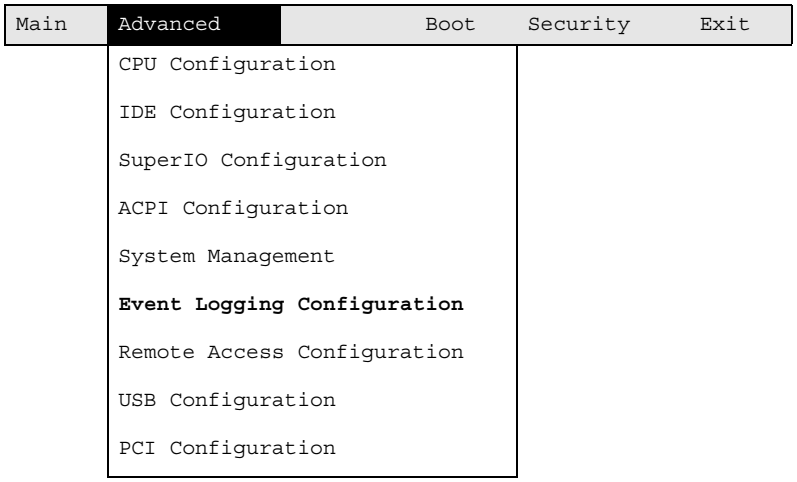


Table 62. SMI Event Logging details Submenu Options

Feature	Options	Description
Event Logging	Disabled Enabled	ENABLE: Enable Error Event handler and allow logging of event errors to SEL. DISABLE: Disable Error Event handler and no event logging to SEL.
ECC Memory Event Logging	Disabled Enabled	Select Enable to allow logging of ECC Memory SBE & MBE error to SEL
Non-Fatal Event Logging	Disabled Enabled	Select Enable to allow logging of SEL non-Fatal error events
Assert NMI on Fatal Error	Disabled Enabled	Select Enabled to allow assertion of NMI on fatal error events
Clear SEL Event Log		Discards all events in the SEL Event Log.

Note: Bold text indicates default setting.

Remote Access Configuration Submenu

To access this submenu, select Advanced on the menu bar, then Remote Access Configuration.

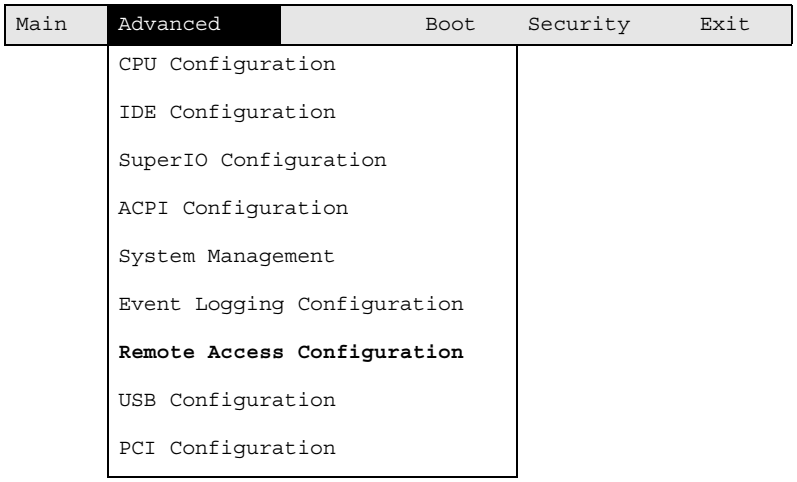


Table 63. Remote Access Configuration Submenu Options

Feature	Options	Description
Remote Access	Disabled Enabled	Select remote access type.
Serial Port Number	COM1	Serial port for console redirection. Make sure the selected port is enabled.
Base Address, IRQ	3F8h, 4	
Serial Port Mode	115200 8, n,1 57600 8, n,1 38400 8, n,1 19200 8, n,1 9600 8, n, 1	Select Serial port settings.
Flow Control	None Hardware Software	Select flow control for console redirection.
Redirection After BIOS POST	Disabled Boot Loader Always	Disable: Turns off the redirection after POST Boot Loader: Redirection is active during POST and during Boot Loader. Always: Redirection is always active (Some OSs may not work if set to Always)

Table 63. Remote Access Configuration Submenu Options (Continued)

Feature	Options	Description
Terminal Type	ANSI VT 100 VT-UTF8	Select the target terminal type.
VT-UTF8 Combo Key Support	Disabled Enabled	Enable VT-UTF8 Combination Key support for ANSI/VT100 terminals.
Sredir Memory Display Delay	No Delay Delay 1 sec Delay 2 sec Delay4 sec	Give the delay in seconds to display memory information.
Terminal Size	80 x 24 80 x 25	Select Terminal Size type.

Note: Bold text indicates default setting.

USB Configuration Submenu

To access this submenu, select Advanced on the menu bar, then USB Configuration.

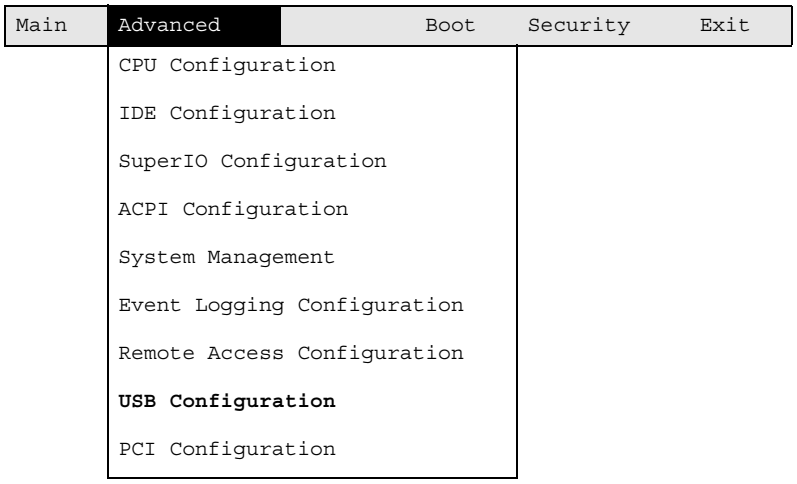


Table 64. USB Configuration Submenu Options

Feature	Options	Description
Legacy USB Support	Disabled Enabled Auto	Enable support for legacy USB. AUTO option disables legacy support if no USB devices are connected.
USB Keyboard Legacy Support	Disabled Enabled	Enables legacy support for USB keyboard
USB Mouse Legacy Support	Disabled Enabled	Enables legacy support for USB mouse
USB Storage Device Support	Disabled Enabled	Enables support for USB mass storage devices.
USB 2.0 Controller Mode	Full Speed HiSpeed	Configures the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps).
USB Beep Message	Disabled Enabled	Enables the beep during USB device enumeration
USB Mass Storage Reset Delay	10 Sec 20 Sec 30 Sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command.
BIOS EHCI Hand Off	Disabled Enabled	This is a workaround for OSs without EHCI hand-off support. The EHCI ownership change should claim by EHCI driver.
USB Mass Storage Device		Configure USB mass storage device (menu will appear if USB flash disk is connected).

Note: Bold text indicates default setting.

The USB Mass Storage Device Configuration option has the following sub-options:

Table 65. USB Mass Storage Device Configuration Sub-Options

Feature	Options	Description
Device #x		Device name will be detected by BIOS and will appear in the menu list.
Device #x : < Disk Name > Emulation Type	Auto Floppy Forced HDD Hard Disk CDROM	If AUTO, USB devices less than 530 MBytes will be emulated as floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).

Note: Bold text indicates default setting.

Boot Menu

To access this menu, select Boot from the menu bar at the top of the screen.

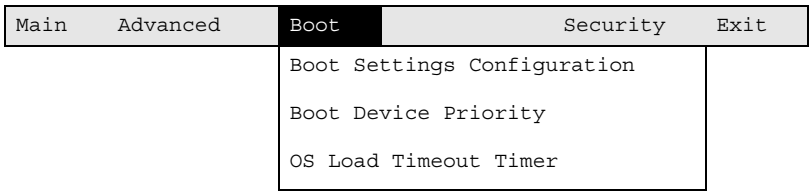


Table 66. Boot Menu Options

Feature	Options	Description
Boot Settings Configuration	Select to display submenu	Set boot options during system boot.
Boot Device Priority	Select to display submenu	Specify the boot device priority sequence.
OS Load Timeout Timer	Select to display submenu	Control time limit of OS loading.

Boot Settings Configuration Submenu

To access this submenu, select Boot on the menu bar, then Boot Settings Configuration.

Table 67. Boot Settings Configuration Submenu Options

Feature	Options	Description
Quick Boot	Disabled Enabled	Allows BIOS to skip certain tests while booting. This will decrease the time needed to boot the system.
Quiet Boot	Disabled Enabled	Disabled: Display normal POST messages. Enabled: Displays OEM logo instead of POST messages.
AddOn ROM Display Mode	Force BIOS Keep Current	Set display mode for Option ROM.
Bootup Num-Lock	Off On	Select Power-on state for Numlock.
PS/2 Mouse Support	Disabled Enabled Auto	Select support for PS/2 mouse.
Wait For 'F1' If Error	Disabled Enabled	Wait for F1 key to be pressed if error occurs.
Hit 'DEL' Message Display	Disabled Enabled	Display "Press DEL to run Setup" in POST.
Soft Reset	Disabled Enabled	Enable or Disable Soft Reset feature.
Spread Spectrum	On Off	Enables or Disables spread spectrum mode for the system clock generator. Enabling this reduces EMI emmissions.
DRAM Fast Refresh	Enabled Disabled	Enables or Disables fast refresh mode on DRAM. Enabling fast refresh mode doubles the refresh rate (Normal rate is 7.8µs, Double rate is 3.9µs).
Interrupt 19 Capture	Disabled Enabled	Enabled : Allows option ROMs to trap interrupt 19.

Note: Bold text indicates default setting.

Boot Device Priority Sub-Menu

To access this sub-menu, select Boot on the menu bar, then Boot Device Priority

Table 68. Boot Device Priority Submenu Options

Feature	Options	Description
1st Boot Device	USB: USB Disk † HDD: PM- 128 MB ATA Flash Disk HDD: SM- 128 MB ATA Flash Disk SCSI: #xxx IDxx IBA GE Slot 0300 IBA GE Slot 0301 IBA GE Slot 0200 IBA GE Slot 0201	Set the first boot device.
2nd Boot Device	HDD: PM- 128MB ATA Flash Disk HDD: SM- 128MB ATA Flash Disk SCSI: #xxx IDxx IBA GE Slot 0300 IBA GE Slot 0301 IBA GE Slot 0200 IBA GE Slot 0201 USB: USB Disk †	Set the second boot device.
3rd Boot Device	HDD: PM- 128MB ATA Flash Disk HDD: SM- 128MB ATA Flash Disk SCSI: #xxx IDxx IBA GE Slot 0300 IBA GE Slot 0301 IBA GE Slot 0200 IBA GE Slot 0201 USB: USB Disk †	Set the third boot device. Default is SAS Hard Drives.

Note:

†: A device only shows as an option if it is installed and detected by the BIOS during boot.

Bold text indicates default setting.

Table 68. Boot Device Priority Submenu Options (Continued)

Feature	Options	Description
4th Boot Device	HDD: PM- 128MB ATA Flash Disk HDD: SM- 128MB ATA Flash Disk SCSI: #xxx IDxx IBA GE Slot 0300 IBA GE Slot 0301 IBA GE Slot 0200 IBA GE Slot 0201 USB: USB Disk †	Set the forth boot device. Default is IBA Slot 0300. (second Ethernet port of base Gigabit Ethernet).
5th Boot Device	HDD: PM- 128MB ATA Flash Disk HDD: SM- 128MB ATA Flash Disk SCSI: #xxx IDxx IBA GE Slot 0300 IBA GE Slot 0301 IBA GE Slot 0200 IBA GE Slot 0201 USB: USB Disk †	Set the sixth boot device. Default is IBA Slot 0301. (second Ethernet port of base Gigabit Ethernet).

Note:

†: A device only shows as an option if it is installed and detected by the BIOS during boot.

Bold text indicates default setting.

Table 68. Boot Device Priority Submenu Options (Continued)

Feature	Options	Description
6th Boot Device	HDD: PM- 128MB ATA Flash Disk HDD: SM- 128MB ATA Flash Disk SCSI: #xxx IDxx IBA GE Slot 0300 IBA GE Slot 0301 IBA GE Slot 0200 IBA GE Slot 0201 USB: USB Disk †	Set the seventh boot device. Default is IBA slot 0200. (First Ethernet port of fabric Gigabit Ethernet).
7th Boot Device	HDD: PM- 128MB ATA Flash Disk HDD: SM- 128MB ATA Flash Disk SCSI: #xxx IDxx IBA GE Slot 0300 IBA GE Slot 0301 IBA GE Slot 0200 IBA GE Slot 0201 USB: USB Disk †	Set the seventh boot device. Default is IBA slot 0200. (First Ethernet port of fabric Gigabit Ethernet).
7th Boot Device	HDD: PM- 128MB ATA Flash Disk HDD: SM- 128MB ATA Flash Disk SCSI: #xxx IDxx IBA GE Slot 0300 IBA GE Slot 0301 IBA GE Slot 0200 IBA GE Slot 0201 USB: USB Disk †	This option will only appear if USB DISK is connected.

Note:

†: A device only shows as an option if it is installed and detected by the BIOS during boot.

Bold text indicates default setting.

OS Load Timeout Timer

To access this submenu, select Boot on the menu bar, then OS Load Timeout Timer.

Table 69. OS Load Timeout Timer Submenu Options

Feature	Options	Description
OS Load Timeout	Disabled 60sec 120 sec 150 sec 240 sec 480 sec 600 sec	Select the timeout value for OS load timer.
OS Load Action	Stay On Reset Power Off Power Cycle	Controls the action upon timeout. Stay On: No action. Reset - Hard reset. Power Off: Shutdown the system. Power Cycle - Soft reset.
Progressive Boot	Disabled Enabled	When this item is enabled and the watchdog timeout is reached before the OS boots, on the next boot, the current boot device will be skipped and the next boot device in the list will attempt to boot.

Note: Bold text indicates default setting.

Security Menu

To access this menu, select Security from the menu bar at the top of the screen.

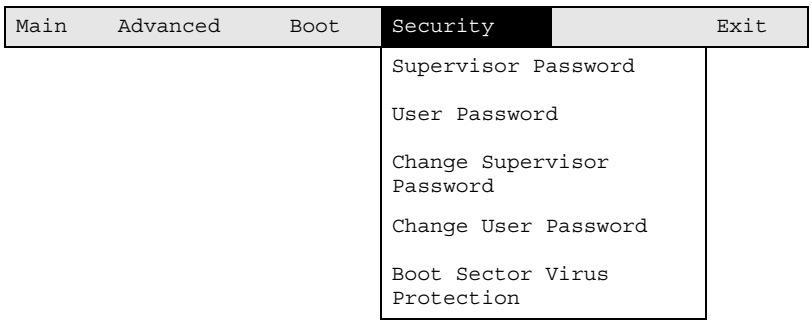


Table 70. Security Menu Options

Feature	Options	Description
Supervisor Password		Display the Supervisor Password status. Installed/not Installed.
User Password		Display the Supervisor Password status. Installed/not Installed.
Change Supervisor Password		Set the supervisor password.
Change User Password		Set the user password.
Boot Sector Virus Protection	Disabled Enabled	Disable/enable boot sector virus protection.

Note: Bold text indicates default setting.

Exit Menu

To access this menu, select Exit from the menu bar at the top of the screen.

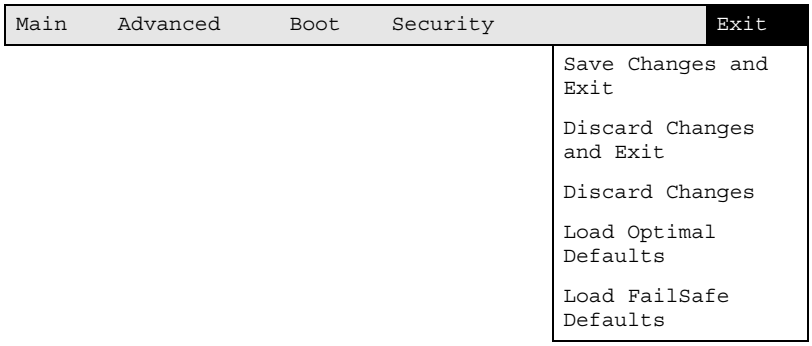


Table 71. Exit Menu Options

Feature	Options	Description
Save Changes and Exit		Exit system Setup after saving changes. Use this to save your configured settings to the CMOS and flash. Similar to pressing F10.
Discard Changes and Exit		Exit system Setup without saving changes. Similar to pressing ESC.
Discard Changes		Discard changes without exiting. Similar to pressing F7.
Load Optimal Defaults		Load optimal default values.Similar to pressing F9
Load FailSafe Defaults		Load failsafe default values. Similar to pressing F8.

10 BIOS Errors and Checkpoints

Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires an add-in card, often called a POST card (PCI, not ISA). The POST card decodes the port and displays the contents on a medium such as a seven-segment display.

Table 72, Table 73, and Table 74 describe the POST codes generated by the BIOS. They define the uncompressed INIT code checkpoints, the boot block recovery code checkpoints, and the runtime code uncompressed in F000 shadow RAM.

Note
Some codes are repeated in the tables because they apply to more than one operation.

Table 72. Boot Block Initialization Code Checkpoints

Checkpoint	Description
Before D0	If boot block debugger is enabled, CPU cache-as-RAM functionality is enabled at this point. Stack will be enabled from this point.
D0	Early Boot Strap Processor (BSP) initialization like microcode update, frequency, and other CPU critical initialization. Early chipset initialization is done.
D1	Early super I/O initialization is done including RTC and keyboard controller. Serial port is enabled at this point if needed for debugging. NMI is disabled. Performs keyboard controller BAT test. Saves power-on CPUID value in scratch CMOS. Goes to flat mode with 4 GByte limit and GA20 enabled.
D2	Verifies the boot block checksum. System will hang here if checksum is bad.
D3	Disables CACHE before memory detection. Executes full memory sizing module. If memory sizing module not executed, start memory refresh and do memory sizing in boot block code. Does additional chipset initialization. Re-enables CACHE. Verify that flat mode is enabled.
D4	Tests base 512 KBytes memory. Adjusts policies and cache first 8 MBytes. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM. Copies compressed boot block code to memory in right segments. Copies BIOS from ROM to RAM for faster access. Performs main BIOS checksum and updates recovery status accordingly.

Table 72. Boot Block Initialization Code Checkpoints (Continued)

Checkpoint	Description
D6	Both key sequence and OEM specific method are checked to determine if BIOS recovery is forced. If BIOS recovery is necessary, control flows to checkpoint E0.
D7	Restores CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determines whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Stores the uncompressed pointer for future use in PMM. Copies main BIOS into memory. Leaves all RAM below 1 MByte read-write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See Table 73 below for more information.
DC	System wakes from ACPI S3 state.
E1-E8 EC-EE	OEM memory detection/configuration error. This range is reserved for chipset vendors and system manufacturers. The error associated with this value may be different from one platform to the next.

Table 73. POST Code Checkpoints

Checkpoint	Description
03	Disables NMI, parity, video for EGA, and DMA controllers. Initializes BIOS, POST, runtime data area. Also initializes BIOS modules on POST entry and GPNV area. Initializes CMOS as mentioned in the kernel variable “wCMOSFlags”.
04	Checks CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verifies CMOS checksum manually by reading storage area. If the CMOS checksum is bad, updates CMOS with power-on default values and clear passwords. Initializes status register A. Initializes data variables that are based on CMOS Setup questions. Initializes both the 8259 compatible PICs in the system.
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Does R/W test to CH-2 count reg. Initialize CH-0 as system timer. Installs the POSTINT1Ch handler. Enables IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to “POSTINT1ChHandlerBlock”.
07	Fixes CPU POST interface calling pointer.
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start – Disable Cache – Init Local APIC.
C1	Sets up bootstrap processor information.
C2	Sets up bootstrap processor for POST.
C5	Enumerates and set up application predecessors.
C6	Re-enables cache for bootstrap processor.

Table 73. POST Code Checkpoints (Continued)

Checkpoint	Description
C7	Early CPU Init Exit.
0A	Initializes the 8042-compatible keyboard controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of keyboard in KBC port.
0E	Tests and initializes different input devices. Also, update the kernel variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and silent logo modules.
13	Early POST initialization of chipset registers.
20	Relocates system management interrupt vector for all CPUs in the system.
24	Uncompress and initialize any platform-specific BIOS modules. GPNV is initialized at this checkpoint.
2A	Initializes different devices through DIM. See Table 74, "DIM Code Checkpoints" on page 130 for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocates memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Sets the window for displaying text information.
37	Displays sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information. USB controllers are initialized at this point.
39	Initializes DMAC-1 and DMAC-2.
3A	Initializes RTC date/time.
3B	Tests for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid-POST initialization of chipset registers.
40	Detects different devices (e.g., parallel ports, serial ports, and coprocessor in CPU) successfully installed in the system and updates the BDA, EBDA, etc.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory. Programs the memory hole or any kind of implementation that needs an adjustment in system RAM size.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initializes Int-13 and prepares for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7C	Generates and writes contents of ESCD in NVRam.

Table 73. POST Code Checkpoints (Continued)

Checkpoint	Description
84	Logs errors encountered during POST.
85	Displays errors to the user and gets the user response to error.
87	Executes BIOS Setup if needed / requested. Checks boot password if installed.
8C	Late POST initialization of chipset registers.
8D	Builds ACPI tables (if ACPI is supported).
8E	Programs the peripheral parameters. Enable/Disable NMI as selected.
90	Initializes of system management interrupt by invoking all handlers. NOTE: This checkpoint comes immediately after checkpoint 20h.
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fills the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initializes runtime language module. Displays boot option popup menu.
A7	Displays the system configuration screen if enabled. Initializes the CPU's before boot, which includes the programming of the MTRRs.
A9	Waits for user input at config display if needed.
AA	Uninstalls POST INT1Ch vector and INT09h vector.
AB	Prepares BBS for Int 19 boot. Init MP tables.
AC	End of POST initialization of chipset registers. De-initializes the ADM module.
B1	Saves system context for ACPI. Prepares CPU for OS boot including final MTRR values.
00	Passes control to OS loader (typically INT19h).

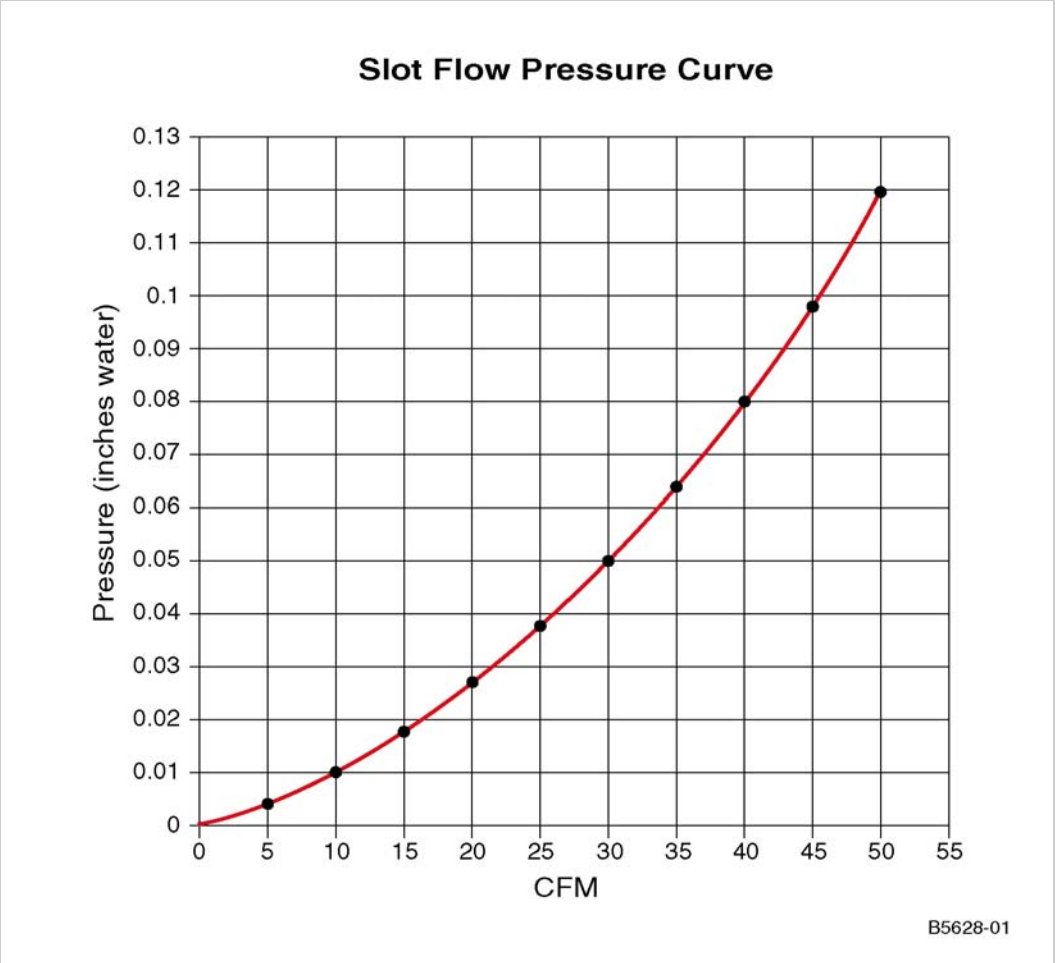
Table 74. DIM Code Checkpoints

Checkpoint	Description
2A	Initializes different buses and performs the following functions: • Function 0: Reset, Detect, and Disable - Disables all device nodes, PCI devices, and PnP ISA cards. Assigns PCI bus numbers. • Function 1: Static Device Initialization - Initializes all static devices that include manual configured on-board peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Reserves static resources. • Function 2: Boot Output Device Initialization - Searches for and initializes any PnP, PCI, or AGP video devices.
38	Initializes different buses and performs the following functions: • Function 3: Boot Input Device Initialization - Searches for and configures PCI input devices and detects if system has standard keyboard controller. • Function 4: IPL Device Initialization - Searches for and configures all PnP and PCI boot devices. • Function 5: General Device Initialization - Configures all on-board peripherals that are set to automatic configuration and configures all remaining PnP and PCI devices.

11 Thermals

The pressure drop curves versus the flow rate in Figure 30 represents flow impedance of the slot This information is provided in accordance with Section 5 of the PICMG 3.0 Specification. It will aid the system integrator in using the ATCA-4200 in various AdvancedTCA shelves.

Figure 30. Power vs. Flow Rate



A List of Supported Commands (IPMI v1.5 and PICMG 3.0)

Table 75. IPMI 1.5 Supported Commands

IPM Device Global Commands			
Command	**NetFn***	**CMD**	**IPMI 1.5 Spec Func**
Get Device ID	App	01h	17.1
Cold Reset	App	02h	17.2
Get Self Test Results	App	04h	17.4
Broadcast "Get Device ID"	App	?	17.9
BMC Watchdog Timer Commands			
Command	**NetFn***	**CMD**	**IPMI 1.5 Spec Func**
Reset Watchdog Timer	App	22h	21.5
Set Watchdog Timer	App	24h	21.6
Get Watchdog Timer	App	25h	21.7
BMC Device and Messaging Commands			
Command	**NetFn***	**CMD**	**IPMI 1.5 Spec Func**
Set IPMC Global Enables	App	2Eh	18.1
Get IPMC Global Enables	App	2Fh	18.2
Clear Message Flags	App	30h	18.3
Get Message Flags	App	31h	18.4
Get Message Flags	App	33h	18.6
Send Message	App	34h	18.7
Read Event Message Buffer	App	35h	18.8
Master Write-Read	App	52h	18.10
Set Channel Access	App	40h	18.20
Get Channel Access	App	41h	18.21
Get Channel Info	App	42h	18.22
Chassis Device Commands			
Command	**NetFn***	**CMD**	**IPMI 1.5 Spec Func**
Get Chassis Capabilities	Chassis	00h	22.1
Chassis Identity	Chassis	04h	22.5
Get POH Counter	Chassis	0Fh	22.12

Table 75. IPMI 1.5 Supported Commands (Continued)

Event Commands			
Command	**NetFn***	**CMD**	**IPMI 1.5 Spec Func**
Set Event Receiver	S/E	00h	23.1
Get Event Receiver	S/E	01h	23.2
Platform Event (Event Message)	S/E	02h	23.3
PEF and Alerting Commands			
Command	**NetFn***	**CMD**	**IPMI 1.5 Spec Func**
Get PEF Capabilities	S/E	10h	24.1
Arm PEF Postpone Timer	S/E	11h	24.2
Set PEF Configuration Parameters	S/E	12h	24.3
Get PEF Configuration Parameters	S/E	13h	24.4
Set Last Processed Event ID	S/E	14h	24.5
Get Last Processed Event ID	S/E	15h	24.6
Alert Immediate	S/E	16h	24.7
PET Acknowledge	S/E	17h	24.8
Sensor Device Commands			
Command	**NetFn***	**CMD**	**IPMI 1.5 Spec Func**
Get Device SDR Info	S/E	20h	29.2
Get Device SDR	S/E	21h	29.3
Reserve Device SDR Repository	S/E	22h	29.4
Set Sensor Hysteresis	S/E	24h	29.6
Get Sensor Hysteresis	S/E	25h	29.7
Set Sensor Threshold	S/E	26h	29.8
Get Sensor Threshold	S/E	27h	29.9
Set Sensor Event Enable	S/E	28h	29.10
Get Sensor Event Enable	S/E	29h	29.11
Re-arm Sensor Events	S/E	2Ah	29.12
Get Sensor Event Status	S/E	2Bh	29.13
Get Sensor Reading	S/E	2Dh	29.14
FRU Device Commands			
Command	**NetFn***	**CMD**	**IPMI 1.5 Spec Func**
Get FRU Inventory Area Info	Storage	10h	28.1
Read FRU Data	Storage	11h	28.2
Write FRU Data	Storage	12h	28.3

Table 75. IPMI 1.5 Supported Commands (Continued)

SDR Device Commands			
Command	**NetFn***	**CMD**	**IPMI 1.5 Spec Func**
Run Initialization Agent	Storage	2Ch	27.21
SEL Device Commands			
Command	**NetFn***	**CMD**	**IPMI 1.5 Spec Func**
Get SEL Info	Storage	40h	25.2
Get SEL Allocation Info	Storage	41h	25.3
Reserve SEL	Storage	42h	25.4
Get SEL Entry	Storage	43h	25.5
Add SEL Entry	Storage	44h	25.6
Partial Add SEL Entry	Storage	45h	25.7
Delete SEL Entry	Storage	46h	25.8
Clear SEL	Storage	47h	25.9
Get SEL Time	Storage	48h	25.10
Set SEL Time	Storage	49h	25.11
Note: *Refer to IPMI 1.5 Specifications for a detailed explanation on NetFn.			

Table 76. PICMG 3.0 IPMI Supported Commands

Command	Net Function	Command	Interface
Get PICMG Properties	2Ch	00h	SMS/SMM/IPMB
Get Address Info	2Ch	01h	SMS/SMM/IPMB
FRU Control	2Ch	04h	SMS/SMM/IPMB
Get FRU LED Properties	2Ch	05h	SMS/SMM/IPMB
Get LED Color Properties	2Ch	06h	SMS/SMM/IPMB
Set FRU LED State	2Ch	07h	SMS/SMM/IPMB
Get FRU LED State	2Ch	08h	SMS/SMM/IPMB
Set IPMB State	2Ch	09h	SMS/SMM/IPMB
Set FRU Activation Policy	2Ch	0Ah	IPMB
Get FRU Activation Policy	2Ch	0Bh	SMS/SMM/IPMB
Set FRU Activation	2Ch	0Ch	SMS/SMM/IPMB
Get Device Locator Record ID	2Ch	0Dh	SMS/SMM/IPMB
Set Port State	2Ch	0Eh	IPMB
Get Port State	2Ch	0Fh	SMS/SMM/IPMB
Compute Power Properties	2Ch	10h	SMS/SMM/IPMB

Table 76. PICMG 3.0 IPMI Supported Commands (Continued)

Command	Net Function	Command	Interface
Set Power Level	2Ch	11h	IPMB
Get Power Level	2Ch	12h	SMS/SMM/IPMB
Note: If a command is received over an invalid interface, a completion code of insufficient privilege level (D4h) is returned.			

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