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ENP-3511 Hardware Reference

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Before you begin

This guide introduces the RadiSys ENP-3511, a board that contains the Intel† IXP1200 network processor (IXP1200), a high-speed packet-processing chip. The ENP-3511, a 6U single-slot 64-bit CompactPCI† board, is ideal for TDM-to-packet or packet-to-packet applications.

This book is for hardware and software designers, programmers, engineers, and those with a knowledge of electronics and/or programming who need to understand the operation of the ENP-3511.

About this guide

Contents

Chapter/appendix		Description
1	Overview	Introduces the ENP-3511, briefly describes its features, and lists specifications.
2	Configuration and installation	Explains how to install the ENP-3511 in a CompactPCI mainframe and how to install driver software.
3	Theory of operation	Describes how ENP-3511 components provide a CompactPCI bus compatible embedded computer with standard PC peripherals plus PCI and ISA interfaces.
4	ENP-3511 RTM	Describes how to install, configure, and use the ENP-3511 RTM (RTM).
A	TDM2IX	Details the TDM2IX operation and registers.
B	CPLD	Details the CPLD registers.
C	Connectors, jumpers, and resistors	Details the location, function, and pin-outs of the ENP-3511's connectors, configuration jumpers, and LEDs.
D	PMC modules	Describes how to install an optional PMC module.
E	Flash memory addresses	Lists the ENP-3511 flash chip's major sections.

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Notational conventions

This manual uses the following conventions:

- `Screen text and syntax strings appear in this font.`
- All numbers are decimal unless otherwise stated.
- Bit 0 is the low-order bit. If a bit is set to 1, the associated description is true unless otherwise stated.


Notes indicate important information about the product.


Tips indicate alternate techniques or procedures that you can use to save time or better understand the product.


The globe indicates a World Wide Web address.


The book indicates a book or file.


ESD cautions indicate situations that *may* cause damage to hardware via electro-static discharge (ESD).


Cautions indicate potentially hazardous situations which, if not avoided, may result in minor or moderate injury, or damage to data or hardware. It may also alert you about unsafe practices.


Warnings indicate potentially hazardous situations which, if not avoided, can result in death or serious injury.


Danger indicates imminently hazardous situations which, if not avoided, will result in death or serious injury.

Where to get more information

About the ENP-3511

You can find out more about ENP-3511 from these sources:

- **Readme file:** Lists features and issues that arose too late to include in other documentation.
- **World Wide Web:** RadiSys maintains an active site on the World Wide Web. The site contains current information about the company and locations of sales offices, new and existing products, contacts for sales, service, and technical support information. You can also send e-mail to RadiSys using the web site.

  
  When sending e-mail for technical support, please include information about both the hardware and software, plus a detailed description of the problem, including how to reproduce it.

  
  To access the RadiSys web site, enter this URL in your web browser:
  `http://www.radisys.com`

  Requests for sales, service, and technical support information receive prompt response.

- **Other:** If you purchased your RadiSys product from a third-party vendor, you can contact that vendor for service and support.

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About related RadiSys products

ENP software development kit (SDK)

The ENP SDK provides programming and runtime libraries for the Intel† Internet Exchange Architecture (IXA) SDK that adds software functionality specific to RadiSys platforms. You use the ENP-3511 to quickly develop optimized applications for the Intel IXP1200 network processor†.

For more information about the ENP SDK, see the *ENP SDK Programmer's Reference*.

Other

ENP-3511 components

For additional information about some ENP-3511 components, see the following documents located on the Intel IXA (Internet Exchange Architecture) SDK CD-ROM:

- *IXF1002 Dual-Port Ethernet Controller Data Sheet*
- *IXP1200 Network Processor Data Sheet*
- *IXP1200 Hardware Reference Manual*



The following web site provides additional information about the board's main components:

http://developer.intel.com

PICMG

For information about PICMG and the CompactPCI standard, consult the PICMG website at this URL:



http://www.picmg.org

PCI architecture

PCI System Architecture, Fourth Edition, published by Addison-Wesley and authored by Mindshare, Inc.

PCI specifications, available at the PCI SIG web site:



www.pcisig.com

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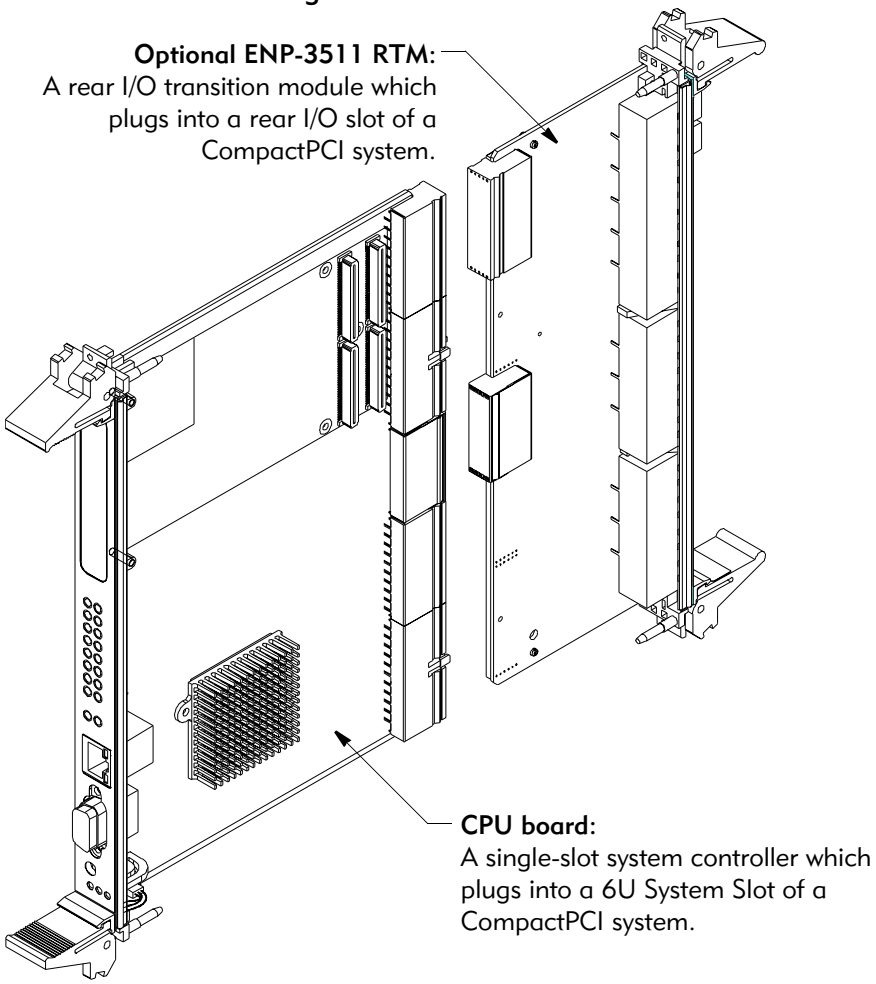
1 Overview

The ENP-3511, a 6U single-slot 64 bit CompactPCI board, is ideal for TDM-to-packet or packet-to-packet applications. It employs an IXP1200 network processor and incorporates an H.110 time-slot interchange chip, a TDM-to-IX bus conversion FPGA or ASIC, and eight 10/100 Ethernet ports on the IX bus to perform this function.

The IXP1200 connects to the backplane PCI bus through a non-transparent bridge. Additionally, the ENP-3511 provides industry-standard PMC connectors for PCI expansion, on-board RS-232, two PCI Ethernet ports, and IPMI. It is compliant with the PICMG 2.1 Hot Swap and PICMG 2.5 CT Hot Swap specifications. The ENP-3511 receives power through the J1, J2, and J4 CompactPCI connectors.

The ENP-3511 includes these subsystems:

Figure 1-1. The ENP-3511



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The ENP-3511 can be ordered in these configurations:

Configuration	Description
ENP-3511-C	Includes the TDM2IX ASIC. Select this option when the contents of your TDM2IX are stable. The PQFP device on this board uses reference designator "U11" and is labelled "RadiSys TDM2IX".
ENP-3511-F	Includes the TDM2IX FPGA. Select this option when you need to repeatedly change the contents of the TDM2IX. Because the BGA device on this board has a footprint slightly smaller than the ASIC contained on the ENP-3511-C, the ASIC pads are visible outside the FPGA.
ENP-3511-F-256	Includes the same features as the ENP-3511-F. Has 256M SDRAM instead of the 128M SDRAM featured in the ENP-3511-F.

The ENP-3511 requires a backplane that supports the *CompactPCI Specification Revision 2.1*.

You can also add a third-party PMC card to the ENP-3511. For information about installing a PMC, see *Appendix C, Connectors, jumpers, and resistors*.



You can add only one PMC to your ENP-3511 system. If your system includes one of the PMCs above, you cannot add another.

Features

The ENP-3511 includes:

Chipset

- IXP1200 (C-step) processor running at 200MHz.
- Lucent T-8105 H.110 time-slot interchange chip (512 simplex channels).
- 512 simplex timeslot TDM-to-IX bus conversion FPGA (only for the ENP-3511-F).
- One IXP 1200 network processor memory subsystem which includes:
  - 8 Mbytes Flash.
  - 8 Mbytes SSRAM.
  - 128 or 256 Mbytes SDRAM.
- Intel 21555 non-transparent PCI bridge chip.
- IPMI-dedicated processor.

I/O

- One RS-232 serial port from the IXP1200 on the faceplate.
- Eight 10/100 Ethernet ports routed to J3, and accessed via the RTM.
  - One Intel IXF440 octal Ethernet MAC.

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  - Two Intel LXT9763 Hex PHYs.
- Two 10/100 Ethernet ports via the Intel 82559ER PCI MAC/PHY routed to J3—available on the RTM; one channel also routed to an RJ45 connector on the faceplate.

Connectors

- One four-connector PMC site with:
  - Two PCI connectors.
  - Two connectors with proprietary pin-out to support interfaces such as POS or ATM PMC cards.
- One RJ-45 connector (on the faceplate).
- CompactPCI connectors:

Connector	Description
J1 and J2	64 bit CompactPCI
J3 and J5	RTM Ethernet and E1/T1 signals, as well as dual backplane Ethernet.
J4	H.110 TDM voice data

- One RS-232 DB-9 serial connector (on the faceplate).
- Connector for POST seven-segment display card.
- Connector for programming the IPMI controller.

Front panel

- PMC faceplate.
- Recessed reset switch.
- Standard ejectors, with hot swap switch in lower ejector.
- LEDs:

LED(s)	Label	Description
Red	Fail	Indicates major failure.
Green	In Service	Indicates the board is provisioned and running.
Blue	Hot Swap	Indicates hot-swap status; board can be removed from chassis.
Green 10-plex	Link	Indicates link status of RTM Ethernet ports (one LED on faceplate RJ-45).
Yellow 10-plex	Activity	Indicates activity of RTM Ethernet ports (one LED on faceplate RJ-45).

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CompactPCI bus

The CompactPCI bus is accessed from the ENP-3511's PCI bus via an Intel 21555 PCI-to-PCI bridge. This bridge connects the onboard PCI bus (bus 0) with the CompactPCI bus, which may have as many as seven additional CompactPCI devices connected to it.

Specifications

Table 1-1. ENP-3511 environmental specifications

Characteristic	State	Value
Mechanical		
Dimensions		160.0 mm x 233.35 mm
Board thickness		1.6 mm
Height	Heat sink and CPU	15.00 mm
	Hard disk drive/ bracket assembly	14.77 mm
Environmental		
Temperature (ambient)[1]	Operating	0°C to +55° with 200LFM airflow. Operation above 30°C reduces the maximum operational relative humidity.
	Storage	–40°C to +70°C, 5° per minute maximum excursion gradient.
Relative humidity	Operating	5% to 85% relative humidity non-condensing at 30°C, linearly decreasing to 5% to 15.5% RH non-condensing at 55°C.
	Storage	15% to 95% relative humidity non-condensing at 40°C.
Shock	Operating	5g, 11 ms duration, half-sine shock pulse.
	Storage	5g, 11ms duration, half-sine shock pulse.
Vibration	Operating	$0.04g^2$/Hz from 5 to 1000 Hz random, 10 min. per sweep cycle
	Storage	$0.06g^2$/Hz from 5 to 1000 Hz random, 10 min. per sweep cycle
EMC		
Immunity (ESD)[2]	Operating	Designed and tested to pass (not certified): • All performance criteria from IEC 1000-4-2/EN61000-4-2:1995 • 4KV direct contact, performance criteria B • 6KV direct contact, performance criteria C • 4KV air discharge, performance criteria B • 8KV air discharge, performance criteria C

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Table 1-1. ENP-3511 environmental specifications

Characteristic	State	Value
Immunity		Designed to pass (not certified):
Fast transient/ burst[2]	Operating	Performance criteria B from IEC 1000-4-4/EN61000-4-4:1995.
Surge voltages[2]	Operating	Performance criteria B from IEC 1000-4-5/EN61000-4-5:1995.
Conducted[2]	Operating	Performance criteria B from IEC 1000-4-6/EN61000-4-6:1995.
Radiated emissions (EMC)[2]	Operating	Designed and tested to pass (not certified) CISPR 22: 1998, Class B.
Radiated immunity[2] 3V/m test level	Operating	Designed and tested to pass (not certified) CISPR 24: 1998.
Safety		
Product safety		Designed to meet the requirements of EN60950/UL60950.

[1] At point of entry of forced air derated 2°C per 1000 ft (300 m) over 6600 ft (2000m) with sufficient airflow to keep within the temperature specification.

[2] These tests are system level tests. Conformation to these specifications is affected by the ability of the rest of the system to conform. Since the board is part of a larger system, it is designed and agency tested—but not agency certified—to these specifications.

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2 Configuration and installation

This chapter explains how to install the ENP-3511 in a CompactPCI chassis.

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Avoid causing ESD (electrostatic discharge) damage:

- Keep the card in its anti-static bag until you are ready to install.
- Install the card (as described later in this chapter) only in a static-free environment:
  - Wear an antistatic wrist strap attached to a known ground such as an antistatic lab mat.
  - Remove the card from its antistatic bag only in a static-free environment.
  - Avoid touching printed circuits, connector pins, and components. Where possible, hold the card only by its edges or mounting hardware.
  - Make the least possible movement with your body to minimize electrostatic charges created by contact with clothing fibers, carpet, and furniture.
  - Keep one hand on the computer chassis, if possible, as you insert or remove a card.
  - Avoid placing the card on the chassis cover or on a metal table. The cover and metal table increase the risk of damage because they provide an electrical path from your body through the card.

The ENP-3511, like most other electronic devices, is susceptible to ESD damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

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Before you begin

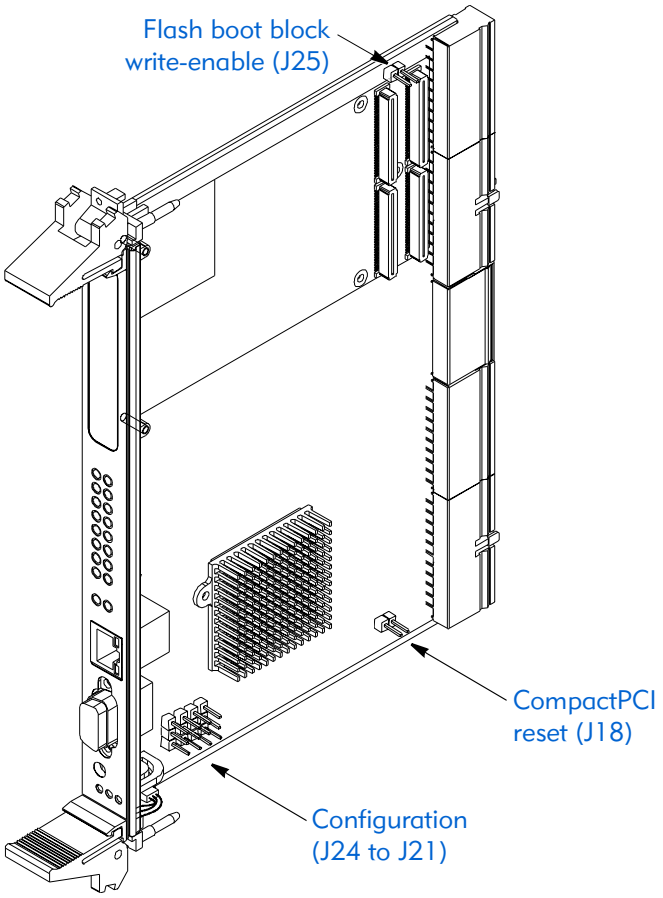
The ENP-3511 requires the following:

- Adequate ventilation.
- A PC that runs Windows NT 4.0, Service Pack 6.
- Software:
  - Internet Exchange Architecture (IXA) Software Developers Kit, version 1.3 (1.3.141) or 2.0 (2.0.83) for the Windows NT workstation, and the version 1.3A patch for the Windows NT workstation This is an integrated development VxWorks environment for developing and delivering code targeted for microengines.
  - Tornado 2.0, available from Wind River Systems, Inc., for StrongARM† development.
  - ENP SDK 2.0. The ENP SDK supports VXworks version 5.4.

The ENP-3511 supports VxWorks BSP version 1.2, revision 2.

Setting jumpers and headers

Figure 2-1. ENP-3511 CPU board: jumper locations

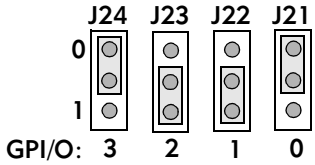


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Configuration (J24 to J21)

A bank of 1x3-pin jumpers (J24 through J21) that you use to configure the board. This figure shows the default settings:

Figure 2-2. Configuration jumper default settings

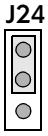


You use software to establish your own purpose for all configuration jumper settings except J24, the Flash operation mode jumper.

Flash operation mode (J24)

A 1x3-pin jumper that you use to specify the Flash operation mode:

Figure 2-3. Flash operation mode jumper settings



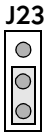
Default position
32-bit mode (two Flash chips)



Leave this jumper in the default position. Other positions cause the boot to fail.

Hardware (J23)

Figure 2-4. Hardware jumper settings



Default position

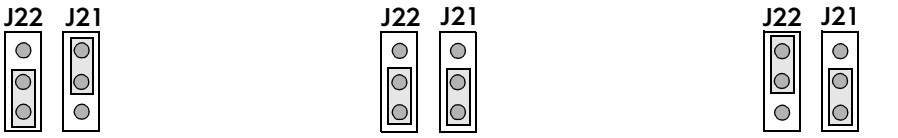


Leave this jumper in the default position. Other positions cause the MAC address load to fail.

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Boot (J21 and J22)

Figure 2-5. Flash operation mode jumper settings



Executes VxWorks.

Executes the System Monitor

Executes the Boot Manager.

For more information about setting boot options, see *Changing boot options* on page 12.

CompactPCI reset (J18)

A 1x2-pin jumper (J18) that you use to enable board reset.

Figure 2-6. CompactPCI reset jumper settings



No pins: Disables backplane CompactPCI reset

Pins 1 and 2: Enables backplane CompactPCI reset

Function	Pins	Description
Enabled	1 and 2	(Default) Causes the board to reset during the next backplane CompactPCI reset.
Disabled	None	Ignores backplane CompactPCI reset.

Flash boot block write-enable (J25)

A 1x2-pin jumper (J25) that you use to re-program the Flash chip boot block.

Flash jumper settings are typically used during manufacturing for re-programming the BIOS in the Flash Boot Device (FBD), and are included here only for reference.

Figure 2-7. Flash write protect jumper settings



No pins: Disables writes to Flash boot block

Pins 1 and 2: Enables writes to Flash boot block

Function	Pins	Description
Disabled	None	(Default) Does not allow writes to the Flash boot block.
Enabled	1 and 2	Enables re-programming of the Flash boot block. The Boot Block is typically *never* re-programmed, even when main and parameter blocks are re-programmed. However, the capability to program the Boot Block facilitates quick changes during manufacturing.

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Inserting the ENP-3511

You install the ENP-3511 CPU board on the CompactPCI bus backplane.



When handling or inserting the ENP-3511, avoid touching the circuit board and connector pins, and ensure that the environment is static-free.

1. Ensure that all options are installed on the ENP-3511 as described in *Maintaining and upgrading the ENP-3511* later in this chapter.
2. Ensure that the ejector handles are in the normal (eject) position. (Push the top handle up and the bottom handle down so that the handles are now tilted.)
3. Slide the ENP-3511 into the slot, pushing it in until the extractor handles rest on the latch rail extrusion of the CompactPCI chassis. The board's connector should be partially mated to the backplane.

   If you are inserting a Hot Swap board and the chassis has a controller, push the ENP-3511 in, and wait until the blue Hot Swap LED light turns on.
4. Move the extractor handles on the front panel to the closed position by pressing the extractor handles inwards towards the center of the front panel until the ENP-3511 is fully seated in the chassis and the extractor handles lock into place.

   If you are inserting a Hot Swap board and the chassis has a controller:

   A. The blue Hot Swap LED turns off.

   B. The ENP-3511 runs the POST, then the red Fault LED turns off.
5. Tighten the retaining screws in the top and bottom of the front panel to ensure proper connector mating and prevent the module from loosening due to vibration.
6. Connect peripherals to the ENP-3511. Peripherals typically include a serial terminal or Ethernet cable. For information about connector pinouts, see *Appendix B, CPLD* and *Appendix C, Connectors, jumpers, and resistors*.

⚠ CAUTION



Observe the following while the system is powered up:

- Do not plug cables or connectors into the front panel connectors. Because electronics equipment generally cannot withstand fluctuations in power, damage can arise from plugging in a device or board while power is on.
- Do not plug in a serial or parallel device, keyboard, transceiver, monitor or other component. This applies to equipment at either end of an interface cable.

7. Complete remaining steps as required. Typical remaining steps include:
   - Driver software installation.
   - Application software installation.

Your system may be preconfigured by your supplier or you may need to perform these tasks yourself.

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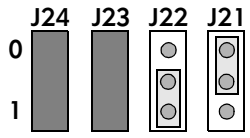
Changing boot options

You can specify which application executes at boot—VxWorks, Boot Manager, or System Monitor—using any of the methods described below. For more information about these applications, see the *ENP SDK Programmer's Reference*.

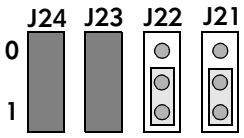
Changing jumper settings

The ENP-3511 provides Configuration jumper settings that you use to configure the board. These jumper positions, which you can change at any time, determine which application executes at boot:

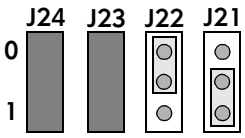
VxWorks module:



System Monitor:



Boot Manager:



Using the Boot Manager

The ENP Software Development Kit (SDK) includes the Boot Manager. From this application you can execute other available boot options.

To select a boot option:

1. Set your COM port to:

Baud rate:	38400
Parity:	N (no parity)
Data bits:	8
Stop bits:	1
Flow control:	N (no flow control)

2. Set the ENP-3511 jumpers for Boot Manager.
3. Power on the ENP-3511. The Boot Manager starts and displays this on the serial port:

   ```
   Press space bar to stop auto-boot...
   10
   ```

4. Press the space bar before the numerical value reaches zero. The Boot Manager prompt displays:

   ```
   [BootMgr]:
   ```

5. (Optional) Enter this command to list available OSs:

   ```
   p
   ```

6. Enter this command:

   ```
   b [n]
   ```

   where *n* is the number of the OS you want to boot when the countdown reaches 0 (zero). You can enter only listed OS numbers.

   The Boot Manager provides more operating system choices than those shown in the jumper settings.

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For detailed information about the Boot Manager and its commands, see the Boot Manager chapter in the *ENP SDK Programmer's Reference guide*.

Post-installation troubleshooting

You can use the diagnostics and System Monitor that come with the ENP Software Development Kit to diagnose and correct hardware problems in the ENP-3511. For a description of these diagnostic tools, see the *ENP SDK Programmer's Guide*.

In addition, the next table lists symptoms and possible solutions to some hardware problems that might occur after you install the ENP-3511.

Symptom	Possible solutions
The ENP-3511 user-controlled LEDs do not turn on at all or are very dim.	Ensure that the power supply can provide the rated power required for the ENP-3511. If the problem still persists, discontinue using the ENP-3511
The ENP-3511 user-controlled LEDs turn on (solid) but do not change.	Re-seat the memory module. If the problem still persists, the flash may be corrupt.
The PC does not recognize a PCI card in the ENP-3511 slot.	Ensure that the ENP-3511 board, memory, and cable are properly installed. Ensure that the ENP-3511 is functioning by: • Watching the user-controlled LEDs for changes. • Using the debug port to watch for serial output. If the PC still does not recognize the ENP-3511, use the diagnostics provided with Windows NT 4.0.
The PC does see a PCI card in the ENP-3511 slot, but does not recognize it as an ENP-3511.	Ensure that the workbench was successfully installed on the host PC.
Any system controller in the same backplane as the ENP-3511 fails to boot.	This is the expected behavior when applying a system-wide reset to all boards in the backplane, and the ENP-3511 boots to either the Boot Manager or FUTIL option. To continue booting, select diagnostics or VxWorks from the Boot Manager. When the operating system configures PCI devices along the backplane, the 21555 'locks' and does not allow backplane configuration to continue until it is configured locally by the IXP1200. Configuration does not occur in the Boot Manager. Instead, it occurs later in all boot menu options except FUTIL.
Your PC does not receive data.	Ensure that the network cables are properly installed.
The ENP-3511 board overheats.	Install a booster fan.

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Maintaining and upgrading the ENP-3511

Occasionally you will want to perform maintenance or upgrades (such as adding options) on the ENP-3511. When this occurs, you must extract the board from the CompactPCI chassis, repair or install the desired option, then re-install the board in the CompactPCI chassis.

If your ENP-3511 includes an option, you may need to disassemble the boards before upgrades or maintenance, then re-assemble the boards before re-inserting the ENP-3511 into the CompactPCI chassis. The following sections describe how.

Removing the ENP-3511

To remove the ENP-3511 from the CompactPCI chassis:

1. Release the extractors using one of these methods:
   A. Press the latch part of the extractors inward until the extractor handle swings out and pivots freely.
   B. If you are removing a Hot Swap board and the chassis has a controller:
      i. Move the lower extractor handle to the eject position.
      ii. If a controller is present, wait for the blue Hot Swap LED to light. When lit, this LED indicates that you can safely remove the board.
      iii. Move the upper extractor handle to the eject position.
2. Pull outward on the extractor handles until the ENP-3511 disengages from the rear connector.
3. If your ENP-3511 includes an option, disassemble the board as described in *Dis-assembling the ENP-3511*.
4. Slide the ENP-3511 out of the CompactPCI chassis and place it in the anti-static bag that it came in.

Dis-assembling the ENP-3511

To separate an option board from the main board:

1. Remove the ENP-3511 in the CompactPCI chassis as described in *Removing the ENP-3511*.
2. Remove PMC modules, including the ARTIC 4-port T1/E1/J1 Line PMC, as described in *Disconnecting the PMC module* in *Appendix D, PMC modules*.

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Re-assembling the ENP-3511

After performing maintenance operations such as upgrading memory, you must re-connect the main board and option boards, and then re-install the ENP-3511 into the CompactPCI chassis.

To re-assemble the ENP-3511:

1. Install PMC modules as described in *Installing a PMC module on the main board* in *Appendix D, PMC modules*.
2. Replace the ENP-3511 in the CompactPCI chassis as described in *Inserting the ENP-3511*.

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3 Theory of operation

The ENP-3511 is a 6U single-slot 64 bit CompactPCI board that performs TDM-to-packet switching. You can expand the ENP-3511 functionality by adding these option boards that connect through the IX Bus/Slow SSRAM or the PMC connectors:



You can use a maximum of one PMC and one RTM at a time.

- **ENP-3511 RTM**: A single slot rear I/O module that provides the ENP-3511 with rear panel access to four T1 or E1 ports, two PCI 10/100 BASE-TX Ethernet ports, and eight IX 10/100 Ethernet ports. For more information, see *Chapter 4, ENP-3511 RTM*.
- **PMC**: The ENP-3511 can also accept most 32-bit PMC modules that are mechanically compliant to the PMC standard

When reading this file online, you can immediately view information about any ENP-3511 topic by placing the mouse cursor over the topic name and clicking:

For information about...	Go to this page...
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PCI interfaces	21
Ethernet interfaces	24
LEDs and other displays	29
Clock sources and distribution	30
Power conditioning, monitoring, consumption, and reset generation	32
External interfaces	33

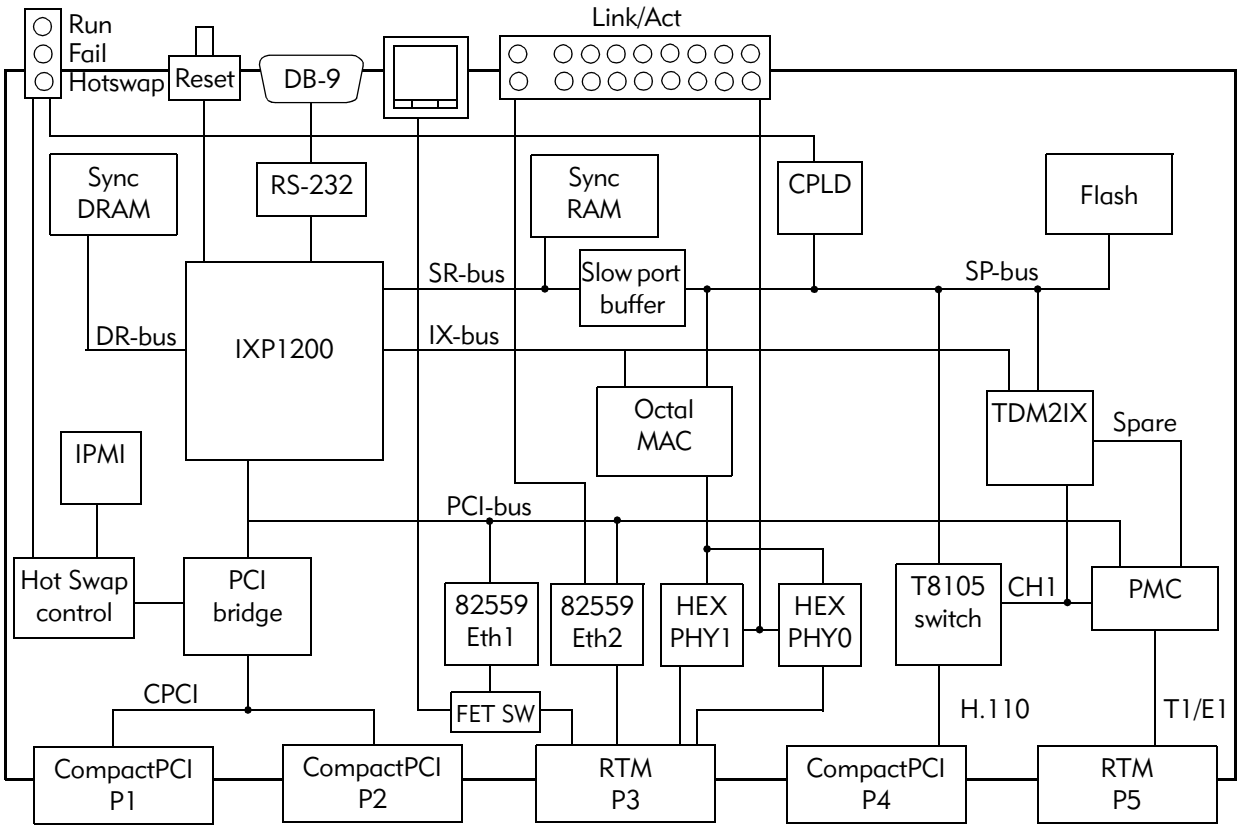
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Organization

Block diagram

The next figure shows the division and interconnection of ENP-3511 functions. The following sections provide detailed descriptions of these items.

Figure 3-1. ENP-3511: block diagram



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Software interface

Slow port memory map

The Slow port is mapped to the range between 0x38400000 to 0x385FFFFF, as shown in the next table. Blank or unlisted fields indicate unused memory locations/ranges while device selects are based only on A13–A18.



For detailed information about CPLD registers, see *Appendix B, CPLD*.

Base address	Read	Write	Base address
0x3840 0000	IXF440 MAC0	IXF440 MAC0	0x3840 0000
0x3840 1000	IXF440 MAC1	IXF440 MAC1	0x3840 1000
0x3840 2000	IXF440 MAC2	IXF440 MAC2	0x3840 2000
0x3840 3000	IXF440 MAC3	IXF440 MAC3	0x3840 3000
0x3840 4000	IXF440 MAC4	IXF440 MAC4	0x3840 4000
0x3840 5000	IXF440 MAC5	IXF440 MAC5	0x3840 5000
0x3840 6000	IXF440 MAC6	IXF440 MAC6	0x3840 6000
0x3840 7000	IXF440 MAC7	IXF440 MAC7	0x3840 7000
0x3840 8000	TDM2IX CR	TDM2IX CR	0x3840 8000
0x3840 8004	TDM2IX SR	TDM2IX SR	0x3840 8004
0x3840 8008	TDM2IX WMRST	TDM2IX WMRST	0x3840 8008
0x3840 800C	TDM2IX IBYTE	TDM2IX IBYTE	0x3840 800C
0x3840 8010	TDM2IX RLEN	TDM2IX RLEN	0x3840 8010
0x3840 8014	TDM2IX TLEN	TDM2IX TLEN	0x3840 8014
0x3840 8018	TDM2IX TEST-XRSYNC (FPGA only)	TDM2IX TEST-XRSYNC (FPGA only)	0x3840 8018
0x3840 801C	TDM2IX TEST-ZOOM (FPGA only)	TDM2IX TEST-ZOOM (FPGA only)	0x3840 801C
0x3840 8020	TDM2IX RXCNT		0x3840 8020
0x3840 8024	TDM2IX TXCNT		0x3840 8024
0x3840 8028	TDM2IX LDOENL or LDOEN	TDM2IX LDOENL or LDOEN	0x3840 8028
0x3840 802C	TDM2IX LDOENU (FPGA only)	TDM2IX LDOENU (FPGA only)	0x3840 802C
0x3840 8030	TDM2IX HWYSEL (FPGA only)	TDM2IX HWYSEL (FPGA only)	0x3840 8030
0x3840 8040	TDM2IX DIO-ENL	TDM2IX DIO-ENL	0x3840 8040
0x3840 8044	TDM2IX DIO-OL	TDM2IX DIO-OL	0x3840 8044
0x3840 8048	TDM2IX DIO-IL		0x3840 8048
0x3840 804C	TDM2IX DIO-ENU	TDM2IX DIO-ENU	0x3840 804C
0x3840 8050	TDM2IX DIO-OH	TDM2IX DIO-OH	0x3840 8050
0x3840 8054	TDM2IX DIO-IH		0x3840 8054
0x3841 0000			0x3841 0000
⋮			⋮
0x3843 FFFF			0x3843 FFFF

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Base address	Read	Write	Base address
0x3844 0000	T8105 MCR	T8105 MCR	0x3844 0000
0x3844 0004	T8105 LAR	T8105 LAR	0x3844 0004
0x3844 0008	T8105 AMR	T8105 AMR	0x3844 0008
0x3844 000C	T8105 IDR	T8105 IDR	0x3844 000C
0x3844 8000	IPMI controller data register	IPMI controller data register	0x3844 8000
0x3844 8004	IPMI controller status register	IPMI controller control register	0x3844 8004
0x3845 0000 ⋮ 0x3845 7FFC	PMC site	PMC site	0x3845 0000 ⋮ 0x3845 7FFC
0x3845 8000			0x3845 8000
0x3849 8000			0x3849 8000
0x3850 0000			0x3850 0000
0x3850 8000		POST HEX display	0x3850 8000
0x3851 0000			0x3851 0000
0x3851 8000	Status LED control register	Status LED control register	0x3851 8000

Hardware components

CPLD

The CPLD is an Altera 7128 or similar in-system re-programmable logic device, which provides the following functions:

- ID/revision level.
- Ethernet MAC chip enable during Slow SRAM bus accesses.
- IX Ready bus latch.
- Parallel FPGA programming interface to allow the host processor to load the FPGA (not yet implemented).
- Chip select, read and write strobes for the IPMI controller keyboard style interface.
- Read and write strobes for the T8105 TSI.
- Link auto-detect circuitry for PCI Ethernet multiplexer.
- Watchdog timer enable.
- RTM signal input/output.
- Interrupt control/mask.

IXP1200

The ENP-3511 uses an Intel IXP1200 processor running at 200 MHz.

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Memory configuration

Flash

The ENP-3511 uses two Intel 28F320C3B or similar flash devices. That is, 32Mbit (2Mbit x 16) bottom boot flash. The boot sector has eight 8 KB memory blocks, and the rest of the memory space has sixty-three 64 KB memory blocks. Both flash parts share the same address and control lines, but one uses data bits D(15:0) and the other uses data bits D(31:16) from the IXP processor's Slow SSRAM bus. Depending on the Flash operation mode (J24) jumper setting, you can:

- **Use both flash devices as boot devices** by driving GPIO3 low during reset (32-bit boot) (J24 in Position 0).
- **Use only the device using D(15:0) as a boot device** by driving GPIO3 high during reset (J24 in Position 1).



The ENP SDK does not support 16-bit boot mode.

SDRAM

The ENP-3511 has 128 Mbytes of 7.5ns (PC133) or faster SDRAM.

SSRAM options

The ENP-3511 has 8 Mbytes of pipelined, two-cycle-deselect, synchronous, 7.5ns SSRAM.

PCI interfaces

The ENP-3511 two PCI buses, linked through a PCI bridge, the Intel 21555.

The primary side is between the 21555 and the CompactPCI connectors. This 64-bit bus runs at the backplane clock speed.

The secondary side uses a +3.3V, 32-bit bus and connects to the IXP1200, the PMC connectors, and the two 82559 PCI Ethernet MAC/PHY chips. The secondary side runs at 33 MHz and is +5V tolerant.

The next table describes the on-board device PCI configuration space locations. The IDSEL pin on each device connects to the listed secondary PCI address pin. To select the configuration registers of a given device, a PCI Configuration Space access must be made using the device's corresponding IDSEL address bit set.

Table 3-1. Secondary PCI bus device configuration

Peripheral	IDSEL	Interrupt	Secondary PCI arbitration ~REQ/~GNT pair
IXP1200	AD11	A	0
21555	AD12	A	–
PMC mezzanine connectors	AD23	A	1
82559 MAC 1	AD17	A	2
82559 MAC 2	AD18	A	3

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21555 non-transparent PCI-PCI bridge

The 21555 performs PCI bridging functions for embedded and intelligent I/O applications. The 21555, a non-transparent PCI-to-PCI bridge, acts as a gateway to an intelligent subsystem. The 21555 functions as a bridge between two PCI processor domains, the host and the local domain.

The 21555 features includes:

- Support for independent primary and secondary PCI clocks.
- Independent primary and secondary address spaces.
- Address translation between the primary (host) and secondary (local) PCI buses (domains).

The 21555 creates a configuration barrier between the two PCI domains. You cannot use standard hierarchical PCI configuration methods using Type 1 configuration transactions to access the configuration space of devices on the opposite side of the 21555. The 21555 uses a Type 0 configuration header, which presents the entire subsystem as a single peripheral device to the CompactPCI controller. Thus, from the CompactPCI side, the board looks like a single PCI device configured by the IXP1200 StrongARM.

The 21555 forwards transactions between the primary and secondary PCI buses like a transparent PCI-to-PCI bridge. In contrast to a transparent PCI-to-PCI bridge, however, the 21555 can translate the address of a forwarded transaction from a system address to a local address, or vice versa. This mechanism allows the 21555 to hide subsystem resources from the host processor and to resolve resource conflicts that may exist between the host and local subsystems.

The 21555 configuration space is divided into primary and secondary interface configuration registers, plus device-specific configuration registers. Both the primary and secondary interface configuration headers contain the 64-byte Type 0 configuration header corresponding to that interface.

Both the primary and secondary interfaces support access to the 21555 configuration registers. The 21555 can pre-load some configuration parameters from the serial ROM attached to the 21555. This enables vendor-specific configuration parameters to load into the 21555 configuration registers, replacing default values specified by Intel. These vendor-specific parameters load before configuration of the 21555 by the local and/or host processors. You can preload address mapping requirements, Class Code, Subsystem ID, Subsystem Vendor ID, and others. During preload, all accesses to 21555 configuration registers receive a target retry.

Secondary PCI bus arbiter and central functions (Local Bus 0)

The 21555, the secondary PCI bus arbiter and central resource, implements an internal secondary PCI bus arbiter that supports nine secondary bus masters, plus the 21555. As the central resource, the 21555 drives the secondary bus AD, C/~BE, and PAR during reset.

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21555 serial pre-load

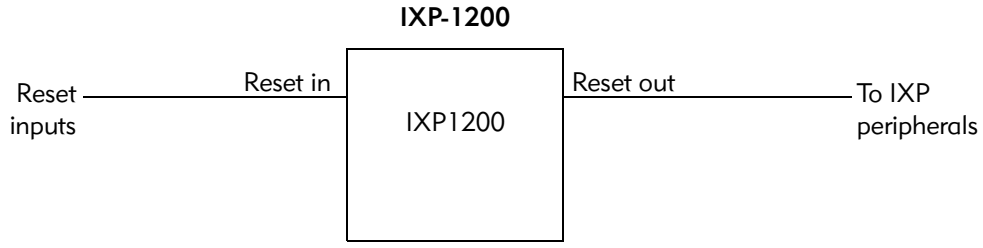
A pre-load from a serial PROM performs the 21555's initial configuration. By default, all windows are closed. The serial preload sets the Primary Class Code and Subvendor ID as follows:

```
Class Code (Both primary and secondary side)
80, Other Bridge Type
06, Bridge Device
Subvendor ID
1331 = RadiSys
Subsystem ID
0022 = ENP3510
```

On-board local reset

The IXP-1200 includes both reset in and reset out signals:

Figure 3-2. IXP-1200 reset signals



The ENP-3511's reset out signal resets these IXP1200 peripherals:

- CPLD registers.
- Octal Ethernet MAC/PHYs.
- T8105 TDM switch.
- TDM2IX.

When any of these conditions occur, the IXP1200 asserts the reset signal:

- The on-board +3.3V supply drops below approximately +2.9V (200ms).
- The on-board +5.0V supply drops below approximately +4.7V (200ms).
- The reset button (located on the faceplate) is pressed.
- The +3.3V supply rises above +2.9V at power up (200ms).
- After a watchdog strobe, approximately 1.6 seconds (1.0 sec min) pass with no further watchdog strobes. Note: the watchdog must be enabled.
- The IPMI circuit forces a reset.
- CompactPCI reset, if jumper J18 is installed.

  If the ENP-3511 is installed in a CompactPCI backplane, and you want the ENP-3511 to ignore the backplane CompactPCI reset, J18 can be removed. Do this only if the backplane PCI bus is not used. The jumper must be installed if

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the ENP-3511 is used with the backplane PCI bus. By default, the jumper is installed.

After the IXP1200 asserts (sets low) the reset out signal asserts, your software must de-assert, or turn off, the reset signal.

Standalone operation

The ENP-3511 works with or without a system CPU in the CompactPCI system slot.

Coming out of reset, the ENP-3511 looks for a CompactPCI clock. If detected, the ENP-3511 uses the clock. If not, the 21555 uses a locally generated clock. Once the 21555 switches to the local clock source, the CompactPCI clock cannot be changed without resetting the board. You can reset the board by pressing the reset button on the front panel, initiating a backplane reset, or recycling power.

Do not disable the secondary clock out via the Chip Control register in the 21555 PCI Configuration space.

The ENP-3511uses secondary clock out from the 21555. An external strapping option enables this clock output at power-up.

PMC expansion slot

The ENP-3511 includes one PMC expansion slot with interfaces through the 10 mm high PMC connectors to the PMC.

The board includes these PMC connectors:

- **Jn1 and Jn2**: Connects to the local PCI bus.
- **Jn3 and Jn4**: Provides an interface to specific telecom PMC boards, including the ARTIC multi-port digital network PMCs.

For a summary of signals on PMC connectors Jn3 and Jn4, see *PMC connectors* on page 79.

Ethernet interfaces

IXF440/LXT9763 (IX bus)

An Intel IXF440 (octal port Ethernet controller) and two LXT9763s (hex port PHY) provide support for eight 10BASE-T or 100BASE-TX connections. Each LXT9763 uses only the first four (0–3) of its six ports, with the remaining ports (4–5) terminated. All eight signal pairs route to the ENP-3511 RTM through J3. LED signals for the eight channels route through J3 as well as to the front panel indicators. Each port has these LEDs:

- **Yellow (1)**: Indicates activity.
- **Green (1)**: Indicates link status.

Unused LED pins (eight) from PHY ports are pulled up to +3.3V.

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82559ER (PCI bus)

Two Intel 82559ER Fast Ethernet controllers (µBGA packaging), which incorporate internal MAC (media access controller) and PHY interfaces, provide support for 10BASE-T or 100BASE-TX connections. They have a standard PCI 2.1 compliant configuration space, allowing system identification and configuration.

The 82559s PHY enables a direct connection to the network media, using a 25 MHz clock to derive its internal transmit digital clocks. In 100BASE-TX mode, the analog subsection of the PHY:

- Converts analog data received from the RD pair to a digital 100 Mbps stream, recovering both clock and data.
- Converts a digital 125 Mbps stream into the proper format and drives it through the TD pair into the physical medium.

The 82559s provide link and activity LED indicators that can sink 10mA. The 82559 signal pairs route to J3 through isolation transformers. Depending on the backplane configuration, they can connect to backplane hubs, or go through the backplane to the ENP-3511 RTM. The RTM has resistor options to disconnect the on-board RJ-45 connectors if the backplane has Ethernet hubs.

The first 82559 also connects through an analog MUX to the faceplate RJ-45 labelled “CTRL 0”. The ENP-3511 can auto-detect which port plugged in first and then “lock” to that port. For more information, see the descriptions for bits 4 and 5 (MAN and FRNT) in *Status Control register (38518000, read/write)* on page 70.



For CTRL 0 (the first 82559):

- Detection may take as long as ten seconds.
- Once a connection is locked, you must unplug the cable from the port before detection resumes.

LED status indicators visible on the ENP-3511’s faceplate also route out to the ENP-3511 RTM. The activity and link LEDs are yellow and green, respectively.

The 82559 uses a NM93C46 serial EEPROM to store configuration information.

The ENP3510 design allows either an 82559 or an 82559ER Ethernet controller. Wake-on-LAN is not supported.

T8105 timeslot interchange chip

The T8105 is an H.110 compliant Timeslot Interchange (TSI) chip that can switch 512 timeslots between the local TDM bus (CHI Bus) and the H.110 backplane TDM bus. You can configure the T8105 for a variety of modes with different backplane control, such as H.110 master or slave, or both modes with fall-back clocking options. Additionally, it can be programmed to use different clock sources as master clock, or as fallback clock. The ENP-3511 provides a 16.384MHz clock source for the T8105 chip, which serve as the master clock for the whole system, the master clock for local clocking operations, or simply the fallback clock if a change occurs in the master/slave orientation.

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The T8105 also provides a number of user-configurable outputs that can drive framing signals or clocks of varying frequencies. Of these, the ENP-3511 uses the L_SC0–3 signals to define local clocks to the TDM2IX and the PMC sites, and uses the FGA0/FGB0 signals as frame synchronization signals to the TDM2IX and PMC sites.

The microprocessor interface is a standard Intel interface via the Slow Port, with chip, read, and write selects, plus two address bits, and an 8-bit data bus. To address the T8105, you select one of four registers, which in turn provide access to a large number of registers within the part.

For details on device configuration, see the Lucent T8105 datasheet. For information about how this part fits into the system, see Figure 3-1 on page 18.

H.110 TDM bus

The T8105 provides a fully compliant H.110 interface that can switch up to 512 timeslots between the local CHI bus and the H.110 bus. This interface can serve as H.110 bus master or H.110 slave, with fallback clocking options. There are 32 bi-directional pins available for accessing the H-bus. The direction of the pins is selected by the timeslot assignments. You select pin data rates in accordance with the H.110 specifications. Unassigned time slots on the H.110 bus tri-state.

For details on programming this interface, see the T8105 datasheet.

Local TDM (CHI) bus

In addition to the H.110 bus, the T8105 can connect to any of thirty-two local highway (CHI) connections (sixteen inputs and sixteen outputs). Each set of sixteen local highways is partitioned into these groups:

- **Group A**: Highways 0–7.
- **Group B**: Highways 8–11.
- **Group C**: Highways 12–15.

You can configure each group to run at a different frequency (2.048MHz, 4.096MHz, or 8.192MHz), with Group A the slowest.

Example: Group A can run at 2.048MHz while Group B runs at 8.192MHz. Note, however, that the maximum number of local connections cannot exceed 1024, so with 256 full-duplex H.110 connections, there remains 512 local-to-local connections possible. One possible arrangement is to connect group A (only using highways 0–3) to the PMC site running at 2.048MHz, and connect Group B (highways 8–9) to the TDM2IX, running at 8.192MHz. This provides the potential for 128 local connections on Group A, and 256 local connections on Group B. The total local-to-local connections could not exceed 256 simplex local-to-local connections. The maximum number of local-to-H.110/H.110-to-local connections, however, is limited to 512 simplex.

Local bus clock alignment is similar to the H.110 bus clock alignment shown above, where C16 is like the 16MHz clock provided to the TDM2IX, CT_C8 is like the 8MHz clock provided to the TDM2IX, and SCLK is like the 2MHz clock provided to the PMC site.

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The TDM2IX is a programmable logic device that performs the TDM-to-IX Bus interface and provides the following features:

- Transfers:

Board	Up to...	Simplex	Full-duplex
ENP-3511-C	2048 each direction	4096	2048[1]
ENP-3511-F	256 each direction	512	256[1]

[1] These timeslots can come from highways 0–1 or highways 8–9, selectable via the Control register.

- Fine-line 672-pin BGA package.
- Operates at IX bus speeds up to 66MHz.
- Loopback mode for testing and validation.
- Programmable open-drain interrupt pin (CINT0).

In the receive direction, the TDM2IX stores TDM data provided by the timeslot interchange chip (which interfaces to the CompactPCI H.l10 bus). The TDM2IX stores one millisecond of TDM data for each timeslot, then signals the IXP1200 for data transfer. The IXP1200 then moves the eight frames worth of data for each timeslot in bursts of eight quad-words (each quad-word represents the data for eight frames of a single timeslot) to IXP1200 memory. This transfer must occur within one frame (125µs).

In the transmit direction, the TDM2IX performs the above process in reverse, signaling the IXP1200 to transfer eight frames of data for each timeslot when the buffers are empty, and then shifting this data out to the TDM bus during the ensuing eight frames. As above, this IX bus transfer must occur within 125µs of the "ready" signal.

ASIC

The TDM2IX ASIC is a lower-cost, higher performance replacement for the TDM2IX FPGA. It is in a 240-pin PQFP package, co-located with the TDM2IX FPGA footprint. For more information including register details, see the TDM2IX specification.

FPGA

Connector J15 offers a JTAG interface connector to the TDM2IX for programming the serial EEPROM devices used during power-on configuration. The JTAG interface is vendor-specific and requires the Altera "Bit-Blaster" or "Byte-Blaster" interface.



You can program the TDM2IX via serial PROMs.

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IPMI baseboard management controller (BMC)

General

The ENP-3511 implements an IPMI Baseboard Management Controller (BMC) in compliance with the PICMG 2.9 R1.0 CompactPCI System Management Specification. This IPMI BMC provides the ability to monitor, query, and log system management events on the ENP-3511 and in the CompactPCI system. This provides the ability to detect failing hardware, log the sequence of events leading to a failure, and remotely manage and reset the system.

The ENP-3511 BMC interfaces to the slow SSRAM bus of the IXP1200.

H8 microcontroller

The ENP-3511 implements the IPMI BMC using a Hitachi H8 microcontroller. The H8 includes on-chip ROM and RAM, a keyboard-controller-like interface, an I^2C controller, an 8-channel A/D, a UART, and multiple digital I/O pins. It is configured to run at 16.0 Mhz.

Sensors and actuators

The ENP-3511 connects the following sensors (inputs) and actuators (outputs) to the BMC. Note that the H8 firmware may not implement control or response from all these devices:

Input sensors	Output actuators
• Ambient temperature. • Power supplies: +12V, +5V, +3.3V, +1.8V (TDM2IX power), VIO, VCORE. • Board reset. • Hot Swap signals: ejector switch, ~HS_FAULT, ~HS_PWRGOOD.	• Thermal fault. • Board reset. • Interrupt CPU. • Ejector switch.

Non-volatile storage

The ENP-3511 includes a NM25C160 serial PROM connected to the H8 controller. This device provides 2KB of non-volatile storage for FRU inventory information (such as serial numbers) as well as system event logging (SEL).

Distributed Hot Swap

Distributed Hot Swap is a method proposed to PICMG for implementing high-availability hot swap in a CompactPCI system without having active management on the CompactPCI backplane. High-availability hot swap logically “swaps” out a failed board and remotely or automatically “swaps” in a new board. To so this, the swapped-out board must be powered down and physically removed from the bus, and then the new board powered up. Distributed Hot Swap puts the control for this swapping in the IPMI controller.

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This board implements Distributed Hot Swap with a combination of the IPMI BMC and the LT1643L Hot Swap Power Controller. The BMC watches the backplane ~BD_SEL and ~PCI_RST, signals ~PWR_FAULT and PWR_GOOD from the LT1643L's ~POWERGOOD, ~ENUM and LED signals from the 21555 bridge and the status of the ejector switch. The BMC then drives PWR_EN to turn on the board's back-end power, the LED and the ~HEALTHY signal to the CompactPCI backplane.

This implementation of DHS does not use a separate Initialization Complete input. Rather, the Init_Done bit in the PM Status Register and the ~HEALTHY signals are derived from the ENUM signal. When ENUM asserts, then Init_Done and ~HEALTHY latch asserted until the next reset.

This implementation of DHS does not directly monitor the early voltages prior to turning on back-end power. It does monitor that the medium-length pins are engaged, however, by monitoring the ~BD_SEL pin (a short-length ground pin). This allows the BMC to dedicate its resources to watching on-board resources rather than verifying that the backplane power is good.

LEDs and other displays

Failure (red) and In Service (green) LEDs

The red and green LEDs are controlled through IPMI. IPMI determines the conditions for lighting each; writes to this register turn LEDs on or off. The LEDs indicate board operational status:

- **Red LED:** Lights when any port connection fails.
- **Green LED:** Lights when the board functions normally.

Software can use various flashing patterns to provide a variety of status messages. Although you can create any status message you desire, CompactPCI standards indicate the LEDs are typically used as shown in the next table.

Green (in-service) LED	Red (failure) LED
Indicates *all* these conditions:	Indicates *at least one* of these conditions:
• Board is out of reset. • POST has run and passed. • All components checked out and operational. • Board is provisioned.	• Board is in reset. • POST has run and not passed. • software load failed. • T8105 is slave and has lost its reference clock.

Hot Swap Status (blue) LED

The blue LED, located on the front of the board, lights when you can safely remove the ENP-3511 from the backplane. This LED indicates that system software is ready for orderly extraction of the board. Upon insertion, the hardware automatically lights the LED until the hardware connection process completes. The LED then remains off until used by software to indicate that extraction is once again permitted.

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Ethernet LEDs

These are described in *Appendix C, Connectors, jumpers, and resistors*.

Hot Swap

You can insert and remove the ENP-3511 from a "live" backplane. A Linear Technology 1643L Hot Swap power controller provides controlled powering up and down of the ENP-3511. With its internal FETs for ±12V and external FET gate control for +5V, the power controller ramps power up and down for the board upon insertion or extraction. It also provides microsecond-rate response to over-current conditions that may exist on any of these voltages.

The board properly operates with voltages that comply with the tolerances in the *PICMG 2.1 Hot Swap Revision 2.0* specification. The input voltages pass through hot swap controller circuitry, reducing the amplitude of these signals slightly, depending on how much current is drawn. The +5V passes through a single-sense resistor and three FETs in parallel. The sense resistor is 5 milli-Ohms, while the worst case R_{DSON} of the three FETs in parallel is 2.7 milli-Ohms.

A local switching power supply generates +3.3V from +5V, instead of using the +3.3V available on the CompactPCI backplane.

The Intel 21555 PCI-PCI bridge supplies the CompactPCI interface on the CPU board. The CompactPCI Hot Swap specification defines these levels of compatibility for compliant PCI devices:

- Hot Swap capable
- Hot Swap friendly
- Hot Swap ready

This CPU board meets the requirements for Hot Swap friendly. The 21555 bridge implements a Hot Swap Control/Status register in Primary PCI configuration space. The register is accessed using the Extended Capabilities Pointer (ECP) mechanism in PCI configuration space.

The Hot-Swap specification requires backplane signals pre-charge to an intermediate voltage prior to connection with backplane busses. This is accomplished by generating an on-board mid-level voltage (VBIAS) which is connected through resistors to the pins. This pre-charge system is applied to the CompactPCI and H.110 backplane busses.

Clock sources and distribution

SDRAM

The SDRAM bus uses a zero-delay clock buffer to provide individual clocks to each chip. The IXP1200 generates a clock with an output one half the IXP1200's core frequency. For the 200MHz core speed, this yields a 100MHz SDRAM clock. Of the six buffer outputs, the first four route to individual SDRAM chips. The buffer skews the SDRAM clocks relative to the IXP1200 clock signal to achieve better overall margins on the setup and hold times for reads and writes.

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Ethernet

A 25MHz 50ppm oscillator drives a clock buffer that provides clocks to the two 82559's MAC/PHY chips and the two LXT9763 hex-PHY chips.

Synchronous SSRAM

The synchronous SSRAM bus uses a zero delay clock buffer to provide clocks to each memory chip. This clock, generated by the IXP1200, provides an output one half the IXP1200's core frequency. For the 200MHz core speed, this yields a 100MHz SSRAM clock. Each of the four buffer outputs route to an SSRAM chip. The zero delay buffer may be set to skew the SSRAM clocks relative to the IXP1200 clock signal to achieve better overall margins on the setup and hold times for reads and writes.

IX bus

The IX bus uses a clock buffer from a 66.0 MHz oscillator. The four outputs from the buffer route to the IXP1200, the PLD, the TDM2IX, and the IXF440.

Local PCI bus

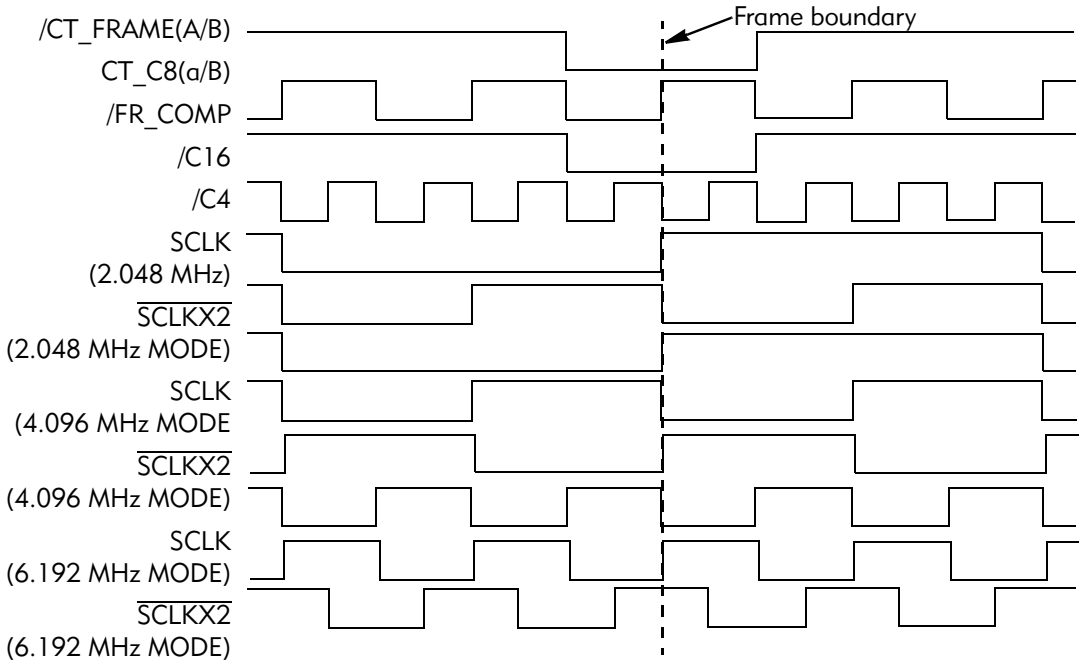
The ENP-3511 uses a 33MHz PCI clock derived from a local oscillator and clock buffer. The clock buffer outputs connect to the IXP1200, the two 82559s, the secondary side of the 21555, and the PMC expansion connector. If a CompactPCI clock is not present, a local clock drives the 21555's primary PCI clock input.

H.110 and Local TDM bus clocking

The following diagram, taken from the Lucent T8105 datasheet, shows H.110 Bus timing and clock alignment:

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Figure 3-3. H.110 bus clock alignment



Local bus clock alignment is similar to H.110 bus clock alignment shown above, where C16 is like the 16MHz clock provided to the TDM2IX, CT_C8 is like the 8MHz clock provided to the TDM2IX, and SCLK is like the 2MHz clock provided to the PMC site.

Power conditioning, monitoring, consumption, and reset generation

Sources and distribution

The board receives power from J1 and J2 CompactPCI interface connectors through the hot swap circuitry for all +5V devices. +3.3V is generated from +5V using a switching power supply. The ±12V from J1 and J2 on the CompactPCI connector route to the PMC connectors, the hot swap controller, and the IPMI circuit for monitoring. Two linear regulators generate the +2.0V and +1.8V needed by the IXP1200 and the TDM2IX respectively from the +3.3V supply.

Power consumption

Total power (worst case), is 33.5 Watts. This estimate does not account for power used by any board attached through the PMC connectors. Attached boards draw power through the ENP-3511 board and increase the power used.

Table 3-2. Power requirements

Power	Maximum current
+5V	250mA
+3.3V	9.8A

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Reset

A reset controller monitors the +3.3V and +5.0V supplies. This monitor provides reset line control, switch debounce, and a minimum reset pulse width. Detection of the input power, +5V and +3.3V, being below +4.5V or +3.0V respectively (10% tolerance) resets of the IXP1200 for at least 200 ms. Additionally, a push-button on the front panel provides a manual reset of the processor. The reset into the IXP1200 propagates to the RESET_OUT pin, which resets the rest of the system. The system can also be reset by the IPMI controller, the watchdog timer, or by a CompactPCI reset from the backplane. You can disable the latter by removing jumper J18.

External interfaces

The ENP-3511 has external interfaces available from the front panel, the CompactPCI standard connectors J1 through J5, and on-board interfaces.

Front panel external interfaces include:

- Red (failure), green (in service), and blue (Hot Swap) LEDs.
- Nine sets of green and yellow LED pairs indicating link and activity for the ENP-3511 RTM's Ethernet ports.
- Reset switch.
- COM, RS-232 DSUB-9 DTE-configured male connector.
- Ethernet RJ-45 connector with 2 LEDs (link and activity).
- Standard-style ejector with hot swap micro switch.

On-board interfaces include PMC connectors for:

- TDM.
- Slow SSRAM bus.
- 32-bit PCI.

Connectors include:

- Programming JTAG ports for PLD.
- Programming JTAG ports for TDM2IX (ENP-3511-F only).
- Programming header for the H8 IPMI controller.
- Socket for plug-in "POST" display card.



These ports are present only for debugging and manufacturing tests.

CompactPCI interfaces include:

- **J1 and J2**: 64-bit Compact PCI interface; +3.3V, +5V, and ±12V power.
- **J4**: H.110 interface.
- **J3**: RTM interface for Ethernet signaling pairs, LED control.

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- J5: RTM interface for T1/E1 signals from PMC and signals from the TDM2IX and IPMI.

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4 ENP-3511 RTM

This chapter describes the ENP-3511 RTM, a 6U single slot rear I/O module that provides the ENP-3511 with rear panel access to four T1 or E1 ports, two PCI 10/100 BASE-TX Ethernet ports, and eight IX 10/100 Ethernet ports.

The RTM interfaces to the ENP-3511 through its J3 and J5 CompactPCI connectors. One EEPROM stores RTM ID and version, accessible from the ENP-3511's Jn3 PMC connector. The card measures 233x80mm.

This chapter includes the topics listed in the table below. When reading this file online, you can immediately view information about any topic by placing the mouse cursor over a topic and clicking:

For information about...	Go to this page...
Features	35
Installation and configuration	36
Theory of operation	38
Connectors	43

Features

The ENP-3511 RTM includes:

- Four independent T1 or E1 ports.
- RJ-45 connections for T1 or 120 Ohm E1.
- Two status LEDs on the RJ-45 of each T1/E1 port. Access is via two I^2C expanders.
- Protection circuitry on each T1/E1 port in compliance with:
  - FCC Part 68—T1 electromagnetic compatibility.
  - UL 1459 and 1950.
- Two independent PCI based 10/100BASE-T Ethernet ports.
- RJ-45 connections for each Ethernet port with two LEDs to indicate line status and activity.
- Eight IX-based 10/100BASE-T Ethernet ports.
- RJ-45 connections with magnetics for each Ethernet port and two LEDs to indicate line status and activity.
- One EEPROM for RTM ID and version accessible from the PMC.
- CompactPCI rear I/O module form factor.

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Installation and configuration

This section explains how to install the ENP-3511 RTM in a PCI chassis.

For information about...	Go to this page...
Inserting the RTM	36
Removing the RTM	37



Avoid causing ESD (electrostatic discharge) damage:

- Keep the card in its anti-static bag until you are ready to install.
- Install the card (as described later in this chapter) only in a static-free environment:
  - Wear an antistatic wrist strap attached to a known ground such as an antistatic lab mat.
  - Remove the card from its antistatic bag only in a static-free environment.
  - Avoid touching printed circuits, connector pins, and components. Where possible, hold the card only by its edges or mounting hardware.
  - Make the least possible movement with your body to minimize electrostatic charges created by contact with clothing fibers, carpet, and furniture.
  - Keep one hand on the computer chassis, if possible, as you insert or remove a card.
  - Avoid placing the card on the chassis cover or on a metal table. The cover and metal table increase the risk of damage because they provide an electrical path from your body through the card.
- During external cable installation, ensure that the cables are not active. This card is not designed for hot insertion of any interface.
- Always turn the computer off before removing a card from the chassis.

The ENP-3511 RTM, like most other electronic devices, is susceptible to ESD damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

Inserting the RTM

To insert the ENP-3511 RTM on the PCI bus backplane.

1. Ensure that power to your CompactPCI system is off, or that the CPU card is removed from the front of the chassis.
2. Ensure that the ejector handles are in the normal (non-eject) position. (Push the top handle down and the bottom handle up so that the handles are not tilted.)
3. Slide the RTM into the slot. Use firm pressure on the handles to mate the module with the connectors.
4. Tighten the retaining screws in the top and bottom of the front panel to ensure proper connector mating and prevent the module from loosening due to vibration.

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5. Connect peripherals to the RTM, if needed. Peripherals typically include a keyboard, but also perhaps a mouse, modem, printer, and so on. For information about connector pinouts, see *Connectors* on page 43.

⚠ CAUTION



Observe the following while the system is powered:

- Do not plug cables or connectors into the front panel connectors. Because electronics equipment generally cannot withstand fluctuations in power, damage can arise from plugging in a device or board while power is on.
- Do not plug in a serial or parallel device, keyboard, transceiver, monitor or other component. This applies to equipment at either end of an interface cable.

6. Complete remaining steps as required. Typical remaining steps include:
   - Driver software installation.
   - Application software installation.

   Your system may be preconfigured by your supplier or you may be required to perform these tasks yourself.

Removing the RTM

Occasionally you may need to remove the RTM to perform maintenance tasks.

To remove the RTM from the CompactPCI chassis:

1. Ensure that power to your CompactPCI system is off, or that the CPU card is removed from the front of the chassis.

   When handling or inserting the ENP-3511, avoid touching the circuit board and connector pins, and ensure that the environment is static-free.

2. Press the latch part of the extractors inward until the extractor handle swings out and pivots freely.
3. Pull outward on the extractor handles until the RTM disengages from the rear connector.
4. Slide the RTM out of the CompactPCI chassis.

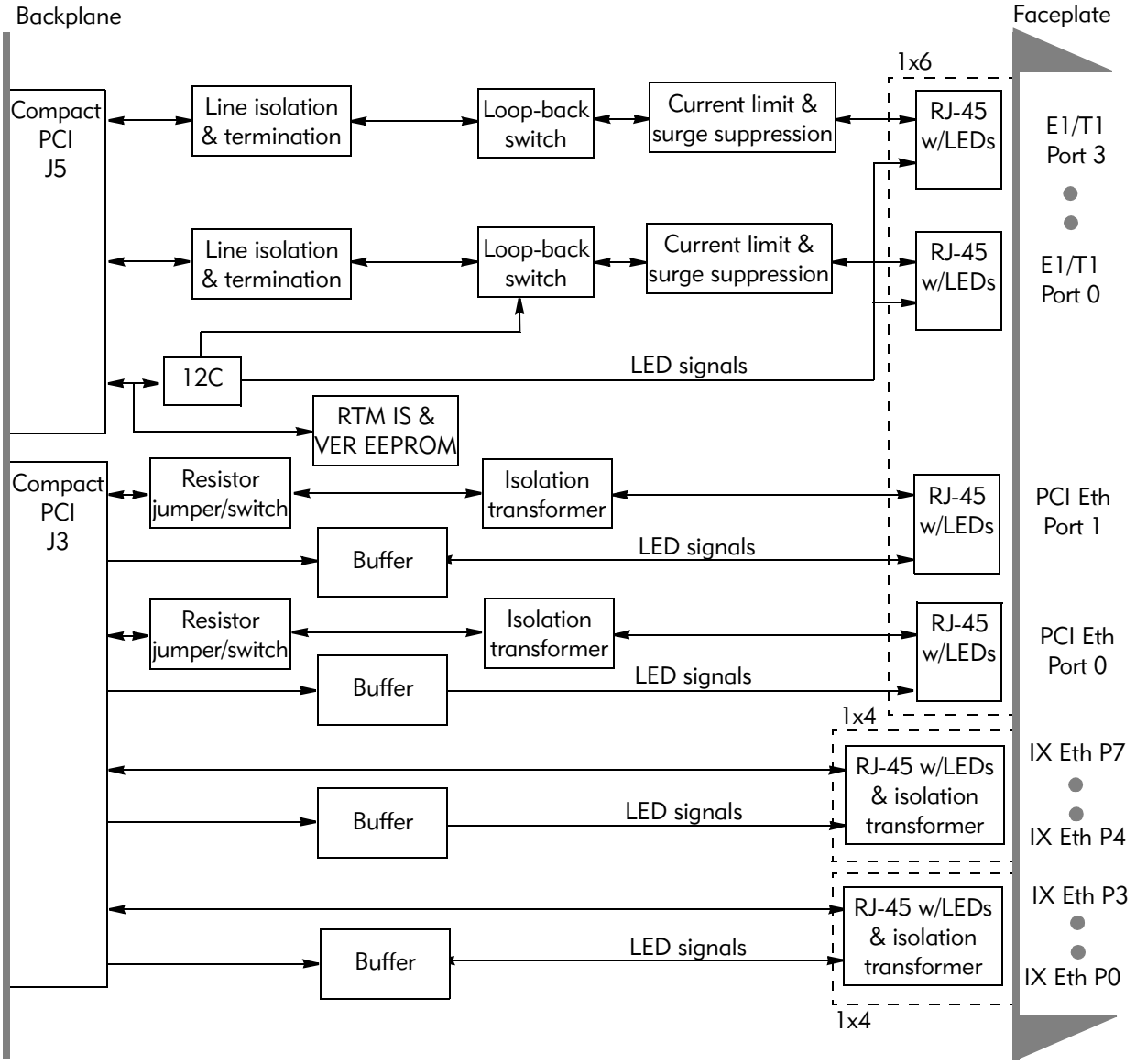
When finished with the tasks at hand, follow the instructions in *Inserting the RTM* on page 36 to re-install the RTM.

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Theory of operation

Block diagram

Figure 4-1. ENP-3511 RTM: block diagram



T1/E1 interface

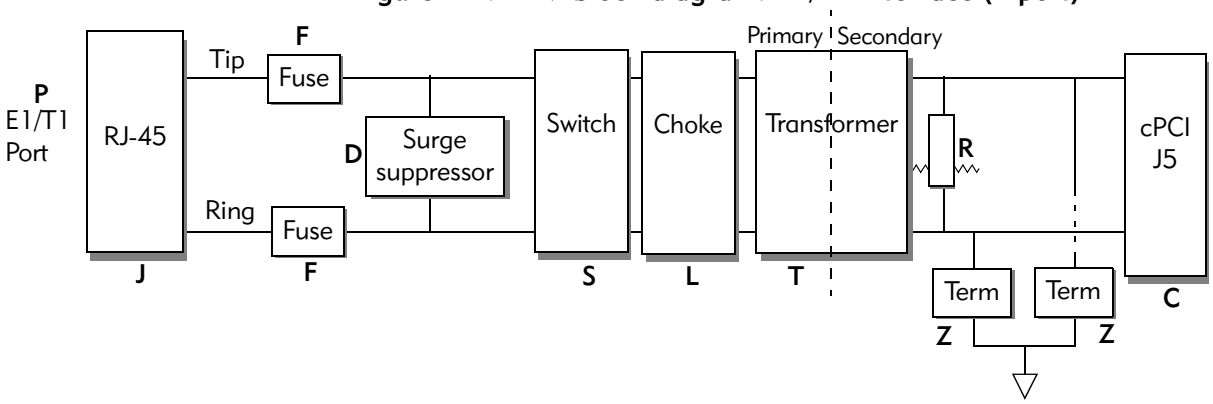
The RTM contains four E1 or T1 line interfaces. These interfaces provide protection, isolation, termination and wrap between signals on the E1 or T1 lines and the FALC device(s) on the T1/E1/J1 PMC.

Each interface has the form shown in the next figure, which applies to both transmit and receive paths with differences described in the text. The following paragraphs describe each of the interface's functional blocks. Unless otherwise specified, the

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description applies to all four interfaces with the RTM configured for either T1 or E1 operation.

Figure 4-2. RTM block diagram: T1/E1 interface (1 port)



Reading figure Figure 4-2 from left to right:

- **An E1 or T1 port** (**P**) interfaces to the card via an RJ-45/RJ-48 (100 Ohms T1 and 120 Ohms E1) connector (J). The four T1/E1 interfaces share a 6-port RJ-45 connector with the two PCI Ethernet interfaces.
- **Two 1.25A fuses** (**F**) limit current under test conditions such as those found in UL1950.
- **The surge suppressor** (**D**) suppresses over-voltage during tests, which simulates T1 to AC power line crosses, and the "metallic" mode lightning surge immunity tests. This device clamps over-voltage to less than 36V and is not required for E1 installations, which do not allow for "direct" connection to outside lines.
- **Solid state relays** (**S**) work as isolation switches and as a loop-back for T1 or E1 port. In normal operation, Tip and Ring signals go through these switches; in loop-back mode, these switches isolate the choke from the RJ-45 connector, and let transmit Tip and Ring signals connect to receive TIP and RING signals. After power-up, all of these switches, isolation and loop-back, are in an open state and will be set open or closed by the I^2C controller on the option card for proper operation. If the PMC option card does not have an I^2C controller, an I^2C Bypass jumper is used to close the isolation switches.
- **Common mode choke** (**L**) **and transformer** (**T**) provides filtering and 3000Vrms of primary to secondary side isolation, respectively. These devices provide isolation during simulated lighting surges such as those found in T1 testing for FCC Part 68 and UL1950.
- **Line termination resistors** (**R**) **and current limiting Zener diodes** (**Z**) in the circuit on the transformer's secondary side on the receive path protect the device from the +36V let through by the surge suppressor.
- **ENP-3511 CompactPCI J5 connector** (**C**) connect the signals to the PMC's FALC.

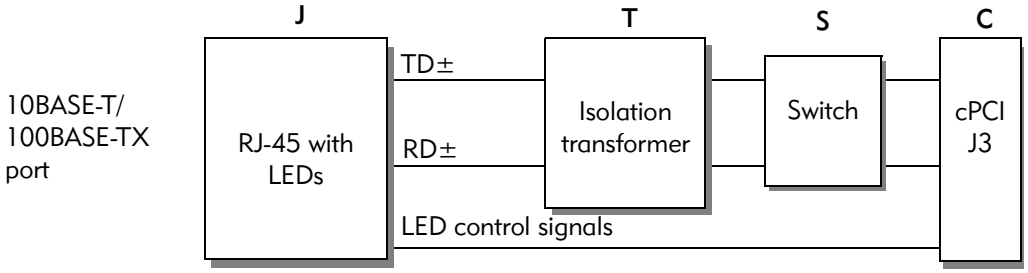
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PCI Ethernet interface

The Ethernet line interface for both 10BASE-T and 100BASE-TX operation match. These interfaces provide isolation and termination between signals on the Ethernet ports and the Intel 82559 MAC/PHY devices on the ENP-3511.

Each interface has the form shown below. The figure applies to both transmit and receive paths, with differences described in the text. The following paragraphs describe each of the interface's functional blocks.

Figure 4-3. RTM block diagram: PCI Ethernet interface (1 port)



Reading figure Figure 4-3 from left to right:

- **RJ-45 connector (J) with LEDs** connects the card and a 10/100BASE-TX port. The two PCI Ethernet interfaces share a 6-port RJ-45 connector with the four T1/E1 interfaces as stated above.

  Transmit and receive signals route as a 100 Ohm differential.

- **Isolation transformers** (**T**) route signal pairs to J3 for transfer to the ENP-3511.
- **Switch SW1** (**S**) routes signal pairs to J3 for transfer to the ENP-3511. The switches, normally closed, can be opened to isolate the RJ-45s from the ENP-3511 if the backplane provides the hub function.
- **CompactPCI J3's** (C) connector pinout minimizes the impedance mismatch seen at the connector pair.

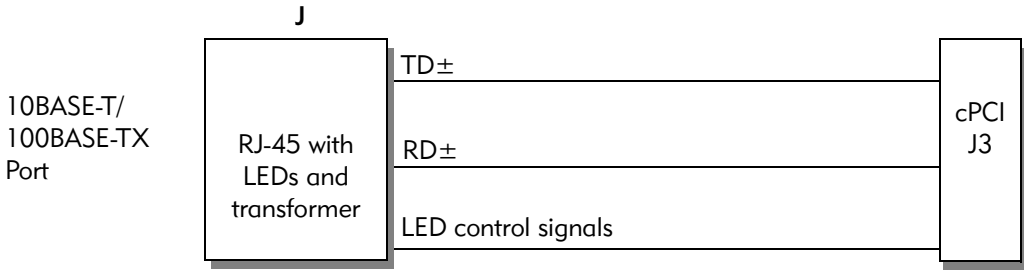
IX Ethernet interface

The Ethernet line interface is the same for both 10BASE-T and 100BASE-TX operation. These interfaces provide isolation and termination between signals on the Ethernet ports and the Intel IXF440 Octal MAC and two LXT9763 Hex PHY devices on the ENP-3511.

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Each interface has the form shown below. The figure applies to both transmit and receive paths, with differences described in the text. The following paragraphs describe each of the interface's functional blocks.

Figure 4-4. RTM block diagram: IX Ethernet interface (1 port)



Reading figure Figure 4-4 from left to right:

- **RJ-45 connector with LEDs (J)** connect the card and a 10/100BASE-TX port with magnetics and LEDs. Eight Ethernet ports are available in this configuration, all on two 4-port RJ-45 connectors.

  Transmit and receive signals route as a 100 Ohm differential.

- **Switch SW1 (R)** routes signal pairs to J3 for transfer to the ENP-3511. The switches, normally closed, can be opened to isolate the RJ-45s from the ENP-3511 if the backplane provides the hub function.

- **CompactPCI J3's (C)** connector pinout minimizes the impedance mismatch seen at the connector pair.

Hot Swap

The RTM derives power only from the front card, as required by the CompactPCI Hot Swap and Computer Telephony specifications. The card itself is not hot swappable, and must be installed when its companion front card is removed or power is off.

RTM ID and revision

The RTM ID and revision are stored at byte 0 of the EEPROM which can be read from the PMC option card. The four upper bits indicate RTM ID and the four lower bits indicate RTM revision.

Table 4-1. ENP-3511 RTM ID values

RTM ID	Bits 7–4
Reserved	0000
ENP-3511 RTM[1]/ RTM	0001
Unused	0010
Unused	0011
Remora RTM	0100
Unused	0101

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Table 4-1. ENP-3511 RTM ID values

RTM ID	Bits 7–4
...	...
Unused	1110
No RTM	1111

[1] To ensure T1/E1 functionality, the ENP-3511 RTM appears as an RTM to the ARTIC multi-port digital network PMCs.

T1/E1 status LEDs

Each T1/E1 port has two status LEDs: green and yellow. The definition/function of those LEDs is application independent.

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Connectors

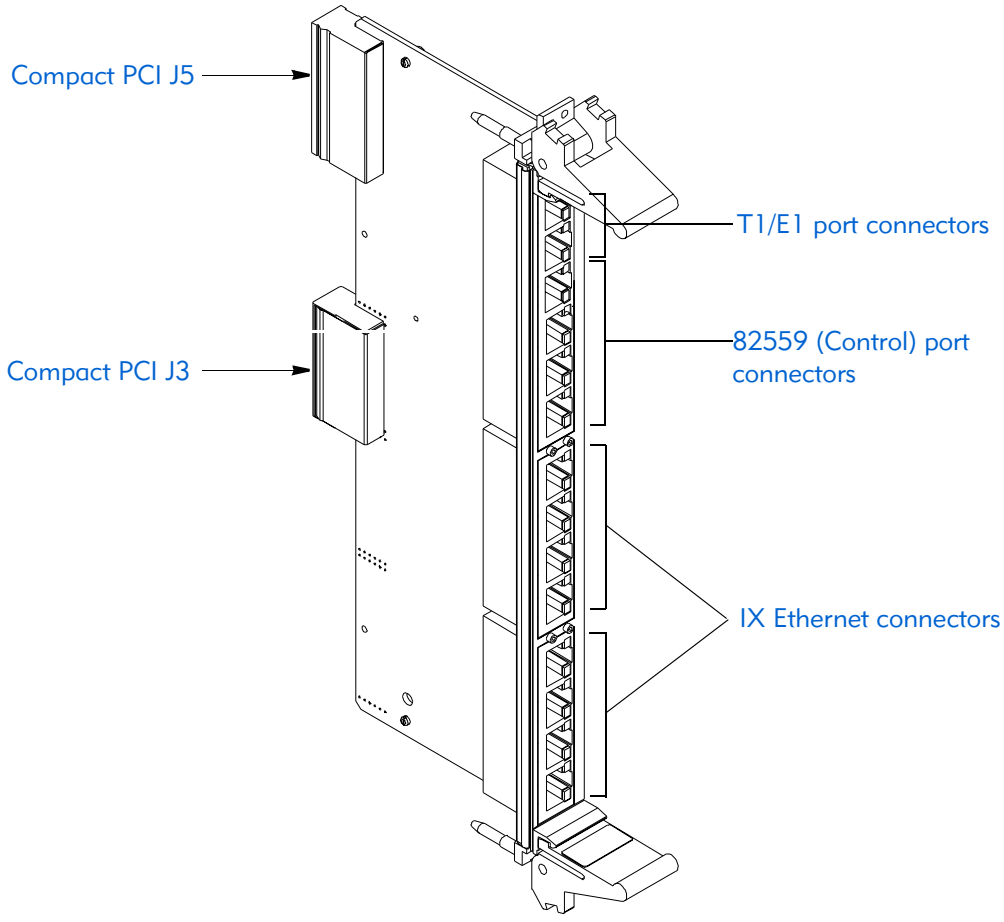
This section details the connectors used by the ENP-3511 RTM and gives the signal pinout of each connector.

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Connector locations

The next figure shows the locations of connectors on the ENP-3511 RTM:

Figure 4-5. ENP-3511 RTM: connectors



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CompactPCI connectors (J3 and J5)

The RTM uses two CompactPCI connectors, J3 and J5.

Compact PCI J5

The J5 connector carries the T1/E1 transmit and receive Tip and Ring pairs, power/ground feedthrough, and I^2C signals for T1/E1 and Ethernet EEPROMs. The connector is pinned out in accordance with the PICMG 2.5 R1.0 for four-wire TNV1-SELV qualified signals.

Table 4-2. Compact PCI J5 connector

Pin	A	B	C	D	E	F
22	TX1_T	No connect	No connect	No connect	No connect	GND
21	TX1_R	No connect	No connect	No connect	No connect	GND
20	RX1_T	No connect	No connect	No connect	No connect	GND
19	RX1_R	No connect	No connect	No connect	No connect	GND
18	TX2_T	No connect	No connect	No connect	No connect	GND
17	TX2_R	No connect	No connect	No connect	No connect	GND
16	RX2_T	No connect	No connect	No connect	No connect	GND
15	RX2_R	No connect	No connect	No connect	No connect	GND
14	TX3_T	No connect	No connect	No connect	No connect	GND
13	TX3_R	No connect	No connect	No connect	No connect	GND
12	RX3_T	No connect	No connect	No connect	No connect	GND
11	RX3_R	No connect	No connect	No connect	No connect	GND
10	TX4_T	No connect	No connect	No connect	No connect	GND
9	TX4_R	No connect	No connect	No connect	No connect	GND
8	RX4_T	No connect	No connect	No connect	No connect	GND
7	RX4_R	No connect	No connect	No connect	No connect	GND
6	No connect	No connect	No connect	No connect	No connect	GND
5	No connect	No connect	No connect	No connect	No connect	GND
4	12C:SCL	12:C:SDA	GND_FT	GND_FT	GND_FT	GND
3	CPLD:RTM2	CPLD:RTM3	CAP:RTM0	CAP:RTM1	No connect	GND
2	CPLD:RTM0	CPLD:RTM1	No connect	No connect	No connect	GND
1	CAP:RTM2	CAP:RTM3	+5V+FT	+12V_FT	–12V_FT	GND

Table 4-3. J5 signal descriptions

Signal	Description
TX*n*_T / TX*n*_R	Transmit TIP and RING pair for T1/E1 port *n* to front card.
RX*n*_T / RX*n*_R	Receive TIP and RING pair for T1/E1 port *n* to front card.
I2C:SCL/I2C:SDA	I2C Bus for T1/E1 port 1–4 status LEDs and RTM ID/Revision from PMC.
CPLD:RTM*n*	CPLD GPIO.
CAP:RTM*n*	TDM2IX GPIO.

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Table 4-3. J5 signal descriptions

Signal	Description
+5V_FT	+5V feedthrough from front card.
+12V_FT	+12V feedthrough from front card. Not used in this implementation.
–12V_FT	–12V feedthrough from front card. Not used in this implementation.
GND_FT	Logic ground feedthrough from front card.
No connect	Not used in this implementation.

Compact PCI J3

The CompactPCI J3 connector carries the Ethernet transmit and receive pairs and status LEDs.

Table 4-4. Compact PCI J3 connector

Pin	A	B	C	D	E	F
19	GND	GND	GND	GND	GND	GND
18	ENET1:TD+	ENET1:TD–	GND	No connect	No connect	GND
17	ENET1:RD+	ENET1:RD–	GND	No connect	No connect	GND
16	ENET2:TD+	ENET2:TD–	GND	No connect	No connect	GND
15	ENET2:RD+	ENET2:RD–	GND	No connect	No connect	GND
14	GND	GND	GND	+3.3V	+3.3V	GND
13	ENET1:~ACT	ENED1:~LINK	GND	ENET2:~ACT	ENET2:~LINK	GND
12	PHY:TDR7+	PHY:TDR7–	GND	PHY:TDR6+	PHY:TDR6–	GND
11	PHY:RFR7+	PHY:RFR7–	GND	PHYRFR6+	PHY:RFR6–	GND
10	PHY:~LED7_1	PHY:~LED7_2	GND	PHY:~LED6_1	PHY:~LED6_2	GND
9	PHY:TDR5+	PHY:TDR5–	GND	PHY:TDR4+	PHY:TDR4–	GND
8	PHY:RFR5+	PHY:RFR5–	GND	PHY:RFR4+	PHY:RFR4–	GND
7	PHY:LED5_1	PHY:~LED5_2	GND	PHY:~LED4_1	PHY:~LED4_2	GND
6	PHY:TDR3+	PHY:TDR3–	GND	PHY:TDR2+	PHY:TDR2–	GND
5	PHY:RFR3+	PHY:RFR3–	GND	PHY:RFR2+	PHY:RFR2–	GND
4	PHY:~LED3_1	PHY:~LED3_2	GND	PHY:~LED2_1	PHY:LED2_2	GND
3	PHY:TDR1+	PHY:TDR1–	GND	PHY:TDR0+	PHY:TDR0–	GND
2	PHY:RFR1+	PHY:RFR1–	GND	PHY:RFR0+	PHY:RFR0–	GND
1	PHY:~LED1_1	PHY:~LED1_2	GND	PHY:LED0_1	PHY:~LED0_2	GND

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Table 4-5. J3 signal descriptions

Signal	Description
ENET*n*:TD+/-	PCI Ethernet transmit pair for port *n*.
ENET*n*:RD+/-	PCI Ethernet receive pair for port *n*.
ENET*n*:~ACT	PCI Ethernet activity LED signal for port *n*.
ENET*n*:~LINK	PCI Ethernet link LED signal for port *n*.
PHY:TDR*n*+/-	IX Ethernet transmit pair for port *n*.
PHY:RFR*n*+/-	IX Ethernet receive pair for port *n*.
PHY:~LED*n*_1	IX Ethernet configured LED #1 signal for port *n* (activity).
PHY:~LED*n*_2	IX Ethernet configured LED #2 signal for port *n* (link).
No connect	Not used in this implementation.
+3.3V	+3.3V feedthrough from front card.
GND	Logic ground.

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Ethernet and T1/E1 connectors

The front panel of RTM contains the following Ethernet connectors:

- Six-port RJ-45 connector:
  - T1/E1 port connectors
  - 82559 (Control) port connectors
- IX Ethernet connectors

Six-port RJ-45 connector

The 6-port connector includes a green and yellow LED per port and comes in these configurations:

- **T1 (100 Ohm) or E1 (120 Ohm):** 4 RJ-45 connectors (ports C, D, E, F).
- **PCI Ethernet:** Two (100 Ohm) RJ-45 connectors (ports A, B).

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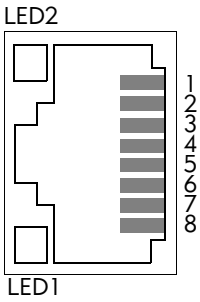


Table 4-6. IX Ethernet connectors

T1/E1 RJ-45 (Ports 0, 1, 2, 3)		Ethernet RJ-45 (Ports 0, 1)	
Pin	**Signal**	**Pin**	**Signal**
1	RxRing	1	Transmit+
2	RxTip	2	Transmit–
3	Unused	3	Receive+
4	TxRing	4	Center tap transmit
5	TxTip	5	Center tap transmit
6	Unused	6	Receive–
7	Frame GND	7	Center tap receive
8	Frame GND	8	Center tap receive

Note: For safety reason, pins 7 and 8 of T1/E1 RJ-45 connectors must be connected to external ground.

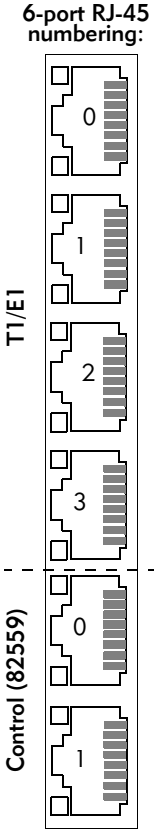


Table 4-7. T1/E1 port connectors

Color	T1/E1 port	LED
Yellow	3	User configurable
Green	3	User configurable
Yellow	2	User configurable
Green	2	User configurable
Yellow	1	User configurable
Green	1	User configurable
Yellow	0	User configurable
Green	0	User configurable

Table 4-8. 82559 (Control) port connectors

Color	82559 port	LED
Yellow	1	Activity
Green	1	Link
Yellow	0	Activity
Green	0	Link

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IX Ethernet connectors

The RTM contains two 4-port RJ-45 connectors with magnetics and a Green and Yellow LED per port.The RTM contains eight (100 Ohm) IX Ethernet connectors.

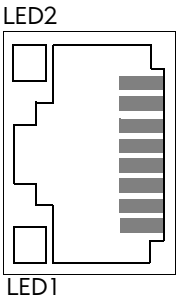


Table 4-9. Octal RJ-45 pin-out

Pin	Signal	Pin	Signal
1	Receive+	5	Center tap transmit
2	Receive–	6	Transmit–
3	Transmit+	7	Center tap receive
4	Center tap transmit	8	Center tap receive

4-port RJ-45 numbering:

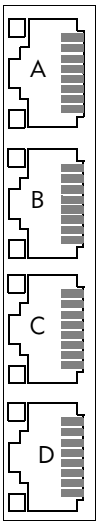


Table 4-10. First 4-port RJ-45 with LEDs

Pin		Color	Port	IXF port	PHY	LED CFG pin
A10	Left	Yellow	1	0	0	Activity
A12	Right	Green	1	0	0	Link
B10	Left	Yellow	2	1	1	Activity
B12	Right	Green	2	1	1	Link
C10	Left	Yellow	3	2	2	Activity
C12	Right	Green	3	2	2	Link
D10	Left	Yellow	4	3	3	Activity
D12	Right	Green	4	3	3	Link

4-port RJ-45 numbering:

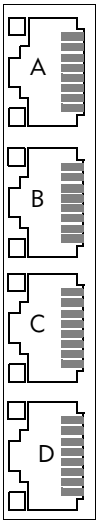


Table 4-11. Second 4-port RJ-45 with LEDs

Pin		Color	Port	IXF port	PHY	LED CFG pin
A10	Left	Yellow	1	4	0	Activity
A12	Right	Green	1	4	0	Link
B10	Left	Yellow	2	5	1	Activity
B12	Right	Green	2	5	1	Link
C10	Left	Yellow	3	6	2	Activity
C12	Right	Green	3	6	2	Link
D10	Left	Yellow	4	7	3	Activity
D12	Right	Green	4	7	3	Link

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Cables

No cables are supplied with this card. The cables for the E1/T1 port connectors—which you supply—must have the shield connected to the shell.

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A TDM2IX

This appendix details the TDM2IX registers.

The TDM2IX is available as either an FPGA or an ASIC. The registers for each are the same except where noted otherwise.

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Write Burst Length register (TLEN)	60
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Zoom Timeslot Select register (ZOOM)	61
Receiver Byte Count register (RXCNT)	61
Transmitter Byte Count register (TXCNT)	62
TDM Stream Output Enable register (LDO_ENL/FPGA; LDO_EN/ASIC)	63
TDM Stream Output Enable register (LDO_ENU)	63
Highway Select (HWYSEL)	64
DIO Output Enable register (DIO_OE)	64
DIO Output Value register (DIO_O)	64
DIO Input Value register (DIO_I)	65

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Accessing the registers

The configuration registers are accessed using asynchronous IXP1200 “slow port” compatible accesses. The next table summarizes the registers.

Note that the offset addresses are not relative to internal IXP addressing, but rather external bus addressing. That is, the IXP1200 generates external addresses for 4-byte wide words (the lower 2-byte address bits are not sourced from the IXP1200); thus all register numbers should be left-shifted by two bits to obtain the internal IXP byte address. For example, the IBYTE register 0x03 corresponds to an IXP1200 byte address of 0xC.

Table A-1. TDM2IX configuration registers and IXP1200 offset addresses

TDM2IX register	IXP1200 offset address	Register name	Access
0x0	0	Control	R/W
0x1	4	Status	R/WC
0x2	8	Warm reset	R/W
0x3	0xC	Idle byte	R/W
0x4	0x10	Read burst length	R/W
0x5	0x14	Write burst length	R/W
0x6	0x18	Transmit-Receive Synchronize Test register[1]	R/W
0x8	0x24	Receiver byte count	R
0x9	0x20	Transmitter byte count	R
0xA	0x28	TDM stream output enable: • For the FPGA: lower (highways 0–7). • For the ASIC: all highways.	R/W
0xB	0x2C	TDM stream output enable upper (highways 8–15)[1]	R/W
0xC	0x30	Highway Select register[1]	R/W
0x10	0x40	DIO[7:0] output enable	R/W
0x11	0x44	DIO[7:0] output value	R/W
0x12	0x48	DIO[7:0] input value	R
0x13	0x4C	DIO[15:8] output enable	R/W
0x14	0x50	DIO[15:8] output value	R/W
0x15	0x54	DIO[15:8] input value	R

[1] Available only in the FPGA.

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Enabling the FPGA

To enable the FPGA to run, perform these steps:

1. Determine the FPGA revision by reading 0x3840800C.
2. Set the transfer length:
   - **If using only one highway**: Write 0x0F to 0x38408010 and 0x38408014, for a total transfer length of 128 timeslots.
   - **If using two highways**: Write 0x1F to 0x38408010 and 0x38408014, for a total transfer length of 256 timeslots.

   If using more highways, write to the appropriate addresses, using the pattern shown in the above examples.
3. Select highways:
   - **To select highways 0–1**: Write 0x00 to 0x38408030.
   - **To select highways 8–9**: Write 0x03 to 0x38408030.
4. Enable the outputs:
   - **For highways 0–7**: Write 0xFF to 0x38408028
   - **For highways 8–15**: Write 0xFF to 0x3840802C (FPGA only; not available in ASIC).
5. Turn on the FPGA by writing 0x0B to 0x38408000.

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Register descriptions

Overview

Table A-2. FPGA register overview

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Offset
CR	0	MD2	MD1	MD0	0	LPBK_SEL	XMT_EN	RCV_EN	0
SR	XMT_UNFL	RCV_OVFL	0	0	UNFL_EN	OVFL_EN	0	0	4
WMRST	AUTO	0	0	0	0	0	0	SRST	8
IBYTE	IBYTE[7]	IBYTE[6]	IBYTE[5]	IBYTE[4]	IBYTE[3]	IBYTE[2]	IBYTE[1]	IBYTE[0]	C
RLEN	0	0	0	RLEN[4]	RLEN[3]	RLEN2]	RLEN[1]	RLEN[0]	10
TLEN	0	0	0	TLEN[4]	TLEN[3]	TLEN[2]	TLEN[1]	TLEN[0]	14
XRSYNC	0	0	0	0	0	XRSYNC[2]	XRSYNC[1]	XRSYNC[0]	18
ZOOM	ZOOM[7]	ZOOM[6]	ZOOM[5]	ZOOM[4]	ZOOM[3]	ZOOM[2]	ZOOM[1]	ZOOM[0]	1C
RXCNT	0	0	0	RXCNT[6]	RXCNT[5]	RXCNT[4]	RXCNT[3]	RXCNT[2]	20
TXCNT	0	0	0	TXCNT[6]	TXCNT[5]	TXCNT[4]	TXCNT[3]	TXCNT[2]	24
LDO_ENL	LDO_EN[7]	LDO_EN[6]	LDO_EN[5]	LDO_EN[4]	LDO_EN[3]	LDO_EN[2]	LDO_EN[1]	LDO_EN[0]	28
LDO_ENU	LDO_EN[7]	LDO_EN[6]	LDO_EN[5]	LDO_EN[4]	LDO_EN[3]	LDO_EN[2]	LDO_EN[1]	LDO_EN[0]	2C
HWYSEL							HW/SEL[1]	HW/SEL[2]	30
DIO_OE	DIO_OE[7]	DIO_OE[6]	DIO_OE[5]	DIO_OE[4]	DIO_OE[3]	DIO_OE[2]	DIO_OE[1]	DIO_OE[0]	40
	DIO_OE[15]	DIO_OE[14]	DIO_OE[13]	DIO_OE[12]	DIO_OE[11]	DIO_OE[10]	DIO_OE[9]	DIO_OE[8]	44
DIO_O	DIO_O[7]	DIO_O[6]	DIO_O[5]	DIO_O[4]	DIO_O[3]	DIO_O[2]	DIO_O[1]	DIO_O[0]	48
	DIO_O[15]	DIO_O[14]	DIO_O[13]	DIO_O[12]	DIO_O[11]	DIO_O[10]	DIO_O[9]	DIO_O[8]	4C
DIO_I	DIO_I[7]	DIO_I[6]	DIO_I[5]	DIO_I[4]	DIO_I[3]	DIO_I[2]	DIO_I[1]	DIO_I[0]	50
	DIO_I[15]	DIO_I[14]	DIO_I[13]	DIO_I[12]	DIO_I[11]	DIO_I[10]	DIO_I[9]	DIO_I[8]	54

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Table A-3. ASIC register overview

Register		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Offset
CR		SB	MD2	MD1	MD0	3/4_TIM	LPBK_SEL	XMT_EN	RCV_EN	0
SR		XMT_UNFL	RCV_OVFL	0	0	UNFL_EN	OVFL_EN	0	0	4
RST		0	0	0	0	0	0	0	SRST	8
IBYTE		IBYTE[7]	IBYTE[6]	IBYTE[5]	IBYTE[4]	IBYTE[3]	IBYTE[2]	IBYTE[1]	IBYTE[0]	C
RLEN		0	RLEN[6]	RLEN[5]	RLEN[4]	RLEN[3]	RLEN2]	RLEN[1]	RLEN[0]	10
TLEN		0	TLEN[6]	TLEN[5]	TLEN[4]	TLEN[3]	TLEN[2]	TLEN[1]	TLEN[0]	14
RXCNT	8 MHz	RFRCNT[2]	RFRCNT[1]	RFRNT[0]	RXCNT[6]	RXCNT[5]	RXCNT[4]	RXCNT[3]	RXCNT[2]	20
	16 MHz	RFRCNT[1]	RFRCNT[0]	RXNT[0]	RXCNT[7]	RXCNT[5]	RXCNT[4]	RXCNT[3]	RXCNT[2]	20
TXCNT	8 MHz	TFRCNT[2]	TFRCNT[1]	TFRCNT[0]	TXCNT[6]	TXCNT[5]	TXCNT[4]	TXCNT[3]	TXCNT[2]	24
	16 MHz	TFRCNT[1]	TFRCNT[0]	TXCNT[7]	TXCNT[6]	TXCNT[5]	TXCNT[4]	TXCNT[3]	TXCNT[2]	
LDO_EN		LDO_EN[7]	LDO_EN[6]	LDO_EN[5]	LDO_EN[4]	LDO_EN[3]	LDO_EN[2]	LDO_EN[1]	LDO_EN[0]	28
DIO_OE		DIO_OE[7]	DIO_OE[6]	DIO_OE[5]	DIO_OE[4]	DIO_OE[3]	DIO_OE[2]	DIO_OE[1]	DIO_OE[0]	40
		DIO_OE[15]	DIO_OE[14]	DIO_OE[13]	DIO_OE[12]	DIO_OE[11]	DIO_OE[10]	DIO_OE[9]	DIO_OE[8]	44
DIO_O		DIO_O[7]	DIO_O[6]	DIO_O[5]	DIO_O[4]	DIO_O[3]	DIO_O[2]	DIO_O[1]	DIO_O[0]	48
		DIO_O[15]	DIO_O[14]	DIO_O[13]	DIO_O[12]	DIO_O[11]	DIO_O[10]	DIO_O[9]	DIO_O[8]	4C
DIO_I		DIO_I[7]	DIO_I[6]	DIO_I[5]	DIO_I[4]	DIO_I[3]	DIO_I[2]	DIO_I[1]	DIO_I[0]	50
		DIO_I[15]	DIO_I[14]	DIO_I[13]	DIO_I[12]	DIO_I[11]	DIO_I[10]	DIO_I[9]	DIO_I[8]	54

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Control register (CR)

The control register. This read/write register has a reset value of 0x00.

FPGA

Offset	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
0	0	MD2	MD1	MD0	0	LPBK_SEL	XMT_EN	RCV_EN

ASIC

Offset	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
0	SB	MD2	MD1	MD0	3/4_TIM	LPBK_SEL	XMT_EN	RCV_EN

SB — You can use one of these values:

- 0 — SOP_TX and EOP_TX should be tied to ground or VDD and all 64 bits of the IX bus both receive and transmit data.
- 1 — Causes the TDM2IX to go into “split” IX bus mode. In this mode the receive data, or TDM2IX input data “driven” by the IXP1200, is obtained from FDATA[63:32] and the transmit data, or data output by the TDM2IX, is driven onto FDATA[31:0]. This mode also enables use of the TDM2IX’s SOP_TX and EOP_TX input pins.

MD2–0 — Defines the TDM-to-IX bus mode of operation used by the TDM2IX as follows:

MD2	MD1	MD0	Function
0	0	0	8-byte packetization—8Mhz TDM streams.
0	0	1	Reserved.
0	1	0	Reserved.
0	1	1	Reserved.
1	x	x	Test modes.
	1	x	When bit 6 and bit 5 are set at the same time, the chip goes into “sync” mode in which the transmit and receive modules are synchronized, based on the contents of the XRSYNC register.[1]

[1] Available only in the FPGA.

3/4_TIM — You can use one of these values:

- 0 — Does not use LCLK2X input and may tie the LCLK2X input high or low to save power. When LCLK2X is clear, input streams are sampled using the rising edge of the LCLK input clock.
- 1 — Samples input streams as follows:

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- **LCLK low**: Samples all TDM input streams on the rising edge of the LCLK2X input clock.
- **LCLK high**: The inputs recirculate the previously sampled data.

LPBK_SEL A control bit.

0	(Default) Turns off the loopback.
1	Forces a TDM loopback mode. In this mode, data output from the TDM2IX loops back to the TDM data inputs. Select this option to test the TDM2IX without valid data from the TDM bus.

XMT_EN An active high signal. You can use one of these values:

0	(Default) The transmit module is inactive and idle byte data (see IBYTE register) is output on all TDM bus timeslots.
1	The transmit module is active.

RCV_EN An active high signal that allows the RCVR_CTL module to run. Valid values include:

0	(Default) The receive module continues to sequence through its RAM address counter, but no operations execute and all status and control signals are disabled.
1	The receive module is active.

Status register (STS)

This status register contains two status bits representing a transmit underflow flag and a receive overflow flag, and two bits which you can use to allow, or mask, interrupts derived for the status bits. This read/write register has a reset value of 0x00.

Offset	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
4	XMT_UNFL	RCV_OVFL	0	0	UNFL_EN	OVFL_EN	0	0

XMT_UNFL

An active high signal that represents a data underflow condition in the IX-to-TDM direction. This flag is set when, at the end of a one-frame buffer period during which the TDM2IX requested a write transfer to fill its buffers, no transfer occurs.

Valid values include:

Value	*Write*	*Read*
0	(Default) The flag remains unchanged.	(Default) No underflow occurred since the flag cleared.
1	Clears the flag.	Underflow occurred since the flag last cleared.

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An underflow often occurs while the host board boots and initializes its software routines.

RCV_OVFL

An active high signal that represents a data overflow condition in the TDM-to-IX direction. This flag is set when, at the end of a two-frame buffer period during which the TDM2IX requested a read transfer, not all the TDM2IX's data unloads from the previous 8-frame period.

Valid values include:

Value	*Write*	*Read*
0	(Default) The flag remains unchanged.	(Default) No overflow occurred since the flag cleared.
1	Clears the flag.	Overflow occurred since the flag last cleared.

UNFL_EN Enables assertion of the CINT_ pin when the XMT_UNFL status bit has a value of '1'.

If this bit and OVFL_EN both have a value of '0', the CINT_ pin is not driven by the TDM2IX and software must "poll" the XMT_UNFL and RCV_OVFL status bits to determine if either condition occurred.

Valid values include:

0 (Default) Disables CINT_assertion.

1 Enables CINT_assertion for the respective condition.

OVFL_EN

Enables assertion of the CINT_ pin when the RCV_OVFL status bit has a value of '1'.

If this bit and UNFL_EN both have a value of '0', the CINT_ pin is not driven by the TDM2IX and software must "poll" the XMT_UNFL and RCV_OVFL status bits to determine if either condition occurred.

Valid values include:

0 (Default) Disables CINT_assertion.

1 Enables CINT_assertion for the respective condition.

Warm Reset register (WMRST/FPGA; RST/ASIC)

Resets the part. This read/write register has a reset value (hardware or AUTO only) of 0x00.

FPGA

Offset	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
8	AUTO	0	0	0	0	0	0	SRST

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FPGA

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8	0	0	0	0	0	0	0	SRST

AUTO Valid values include:

- 0 (Default) No effect.
- 1 Returns the SRST bit to the default state (0x00) after the internal reset sequence completes.

SRST Valid values include:

- 0 (Default) Removes the TDM2IX from the warm reset state.
- 1 Forces a complete reset of the TDM2IX except for the SRST bit itself. After a software-defined delay, clearing the SRST bit to 0 removes the part from reset.

If both the AUTO and SRST bits have a value of '1', the TDM2IX automatically executes a complete reset and then removes itself from the reset state.

Idle Byte register (IBYTE)

Holds the part's revision ID value as the default at power-up.

A read-write register that holds the data pattern output on the local TDM bus timeslots when the XMT_CTL module is not enabled.

Idle byte output is automatically disabled eight frames after the number of write transfer operations matching the value in the TLEN register occurs.

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C	IBYTE[7]	IBYTE[6]	IBYTE[5]	IBYTE[4]	IBYTE[3]	IBYTE[2]	IBYTE[1]	IBYTE[0]

Read Burst Length register (RLEN)

Holds a value that indicates the number of read bursts to execute from TDM2IX memory per 8-frame period. This read/write register has a reset value of 0x00.

Each read burst consists of eight IX Bus reads, each read representing the data from one timeslot over eight frames, so the RLEN register essentially indicates how many sets of eight timeslots to read from the TDM2IX.

FPGA

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10	0	0	0	RLEN[4]	RLEN[3]	RLEN2]	RLEN[1]	RLEN[0]

ASIC

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10	0	RLEN[6]	RLEN[5]	RLEN[4]	RLEN[3]	RLEN2]	RLEN[1]	RLEN[0]

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RLEN[6–0]

The number of eight timeslot sets to read from the TDM2IX.

This is the number of timeslots to read, right-shifted by three places. This value influences when the IX bus receive-ready flag de-asserts, and also influences when the EOP signal is driven for IX bus receive transfers from the TDM2IX.

Valid values fall between:

0x00 (Default) One burst (eight timeslots).

0x1F Where 1F allows 32*8 = 256 (2 highways) transfers.

To force reads from a specific highway, use the pattern shown in this table:

To force reads from...	Use a value lower than...
Highway 0	0x10
Highway 0 and 1	0x20
⋮	⋮

Write Burst Length register (TLEN)

Holds a value that indicates the number of write bursts to execute to TDM2IX memory per eight-frame period. Each transmit burst consists of eight IX Bus writes, each write representing the data from one timeslot over eight frames, so the TLEN register essentially indicates how many sets of eight timeslots to write to the TDM2IX. This read/write register has a reset value of 0x00.

FPGA

Offset	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
14	0	0	0	TLEN[4]	TLEN[3]	TLEN[2]	TLEN[1]	TLEN[0]

ASIC

Offset	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
14	0	TLEN[6]	TLEN[5]	TLEN[4]	TLEN[3]	TLEN[2]	TLEN[1]	TLEN[0]

TLEN[6–0]The number of eight timeslot sets to write to the TDM2IX.

This is the number of timeslots to write, right-shifted by three places. This value influences when the IX bus transmit-ready flag is de-asserted, and also controls how much data must be written during the first transfer before the idle byte data is replaced with actual voice data.

Valid values fall between these:

0x00 (Default) One burst (eight timeslots).

0x1F Where 1F allows 32*8 = 256 (two highways) transfers.

Values lower than 0x10 force all writes to highway 0; values lower than

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0x20 force all writes to highways 0 and 1, and so forth.

Transmit/Receive Sync register (XRSYNC)

Only the FPGA includes this register.

A read-write register which contains an arbitrary 3-bit binary value (0x05 default) used in the XRSYNC mode (CR bits 6 and 5 set) to determine which receive frame (0–7) to synchronize the transmit module to. This read/write register has a reset value of 0x05.

The XRSYNC mode is useful for aligning loopback receive data with transmit data for easy error checking. The default value (0x05) aligns data during internal loopback mode, but this value may require changing for other external loopback scenarios (such as through a TDM switch). The contents of this register have no effect when the XRSYNC mode is not enabled.

Offset	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
18	0	0	0	0	0	XRSYNC[2]	XRSYNC[1]	XRSYNC[0]

Zoom Timeslot Select register (ZOOM)

Only the FPGA includes this register.

Helps provide three test signals to FPGA test output pins. This read/write register has a reset value of 0x00.

This register holds a timeslot value (0–255, with 128 to 255 from local highway 1) which is isolated and “stretched” to fill one complete frame and output. Additionally, based on this timeslot value, a frame clock and a bit-clock are output on test pins.

This feature is very useful for capturing timeslot data from a single timeslot over a number of consecutive frames.

Offset	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
1C	ZOOM[7]	ZOOM[6]	ZOOM[5]	ZOOM[4]	ZOOM[3]	ZOOM[2]	ZOOM[1]	ZOOM[0]

ZOOM[7–0]
To be developed.

Receiver Byte Count register (RXCNT)

Holds the upper five bits of the binary timeslot count value for each TDM stream (one counter is used for all TDM streams since all TDM streams operate from a single FRAME SYNC signal). The resulting register contents count the number of timeslots that passed since the frame boundary. This counter records the number of bytes received on any TDM stream from the TDM bus since the IX bus Receive Ready signal’s flag was sent to the IXP1200.

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When the RCV_EN bit is set in the Control register (CR), this register clears to all 0 at the next frame boundary. Because 128 bytes of buffering per TDM stream is used between IX bus Receive Ready signal set, and when the IXP1200 must remove all data from the TDM2IX RAM, this counter can be used as a gauge for time remaining until overflow occurs. Note that this "guage" has a granularity of four bytes.

For example, a value of 0x04 indicates that 16 bytes of each TDM data stream were loaded since theIX bus Receive Ready signal's flag was received, leaving 109µs (128–16 timeslots).

To avoid reading a "partial update" during a read of this register by the IXP1200, any increments needed are delayed until the register read completes.

The RXCNT portion of this register should normally be the same as the TXCNT portion of the Transmitter Byte Count register (TXCNT) register. This read-only register has a reset value of 0x00.

FPGA

Offset	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
20	0	0	0	RXCNT[4]	RXCNT[3]	RXCNT[2]	RXCNT[1]	RXCNT[0]

ASIC

Offset	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
20	RFRCNT[2]	RFRCNT[1]	RFRCNT[0]	RXCNT[6]	RXCNT[5]	RXCNT[4]	RXCNT[3]	RXCNT[2]
20	RFRCNT[2]	RFRCNT[1]	RXCNT[7]	RXCNT[6]	RXCNT[5]	RXCNT[4]	RXCNT[3]	RXCNT[2]

Transmitter Byte Count register (TXCNT)

Holds the upper five bits of the binary timeslot count value for each TDM stream (one counter is used for all TDM streams since all TDM streams operate from a single FRAME SYNC signal). The resulting register contents count the number of timeslots that have passed since the frame boundary. This counter counts the number of bytes received on any TDM stream from the TDM bus since the IX bus Transmit Ready signal's flag was set to the IXP1200.

When the XMT_EN bit is set in the Control register, this register is cleared to all 0 at the next frame boundary. Since 128 bytes of buffering per TDM stream is used between IX bus Receive Transmit signal's set and when the IXP1200 must write all data from the TDM2IX RAM, this counter can be used as a gauge for time remaining until underflow occurs. Note that this "guage" has a granularity of four bytes.

For example a value of 0x04 indicates 16 bytes of each TDM data stream were loaded since the IX bus Transmit Ready signal's flag was received, leaving 109µs (128–16 timeslots).

To avoid reading a "partial update" during a read of this register by the IXP1200, any increments needed are delayed until the register read completes.

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This register should normally be the same as the Receiver Byte Count register (RXCNT) register. This read-only register has a reset value of 0x00.

FPGA

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
24	0	0	0	TXCNT[4]	TXCNT[3]	TXCNT[2]	TXCNT[1]	TXCNT[0]

ASIC

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20	TXCNT[2]	TXCNT[1]	TXCNT[0]	TXCNT[6]	TXCNT[5]	TXCNT[4]	TXCNT[3]	TXCNT[2]
20	TXCNT[1]	TXCNT[0]	TXCNT[7]	TXCNT[6]	TXCNT[5]	TXCNT[4]	TXCNT[3]	TXCNT[2]

TDM Stream Output Enable register (LDO_ENL/FPGA; LDO_EN/ASIC)

Provides enables for outgoing TDM highways 0 through 7. This read/write register has a reset value of 0x00.

FPGA

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
28	LDO_ENL[7]	LDO_ENL[6]	LDO_ENL[5]	LDO_ENL[4]	LDO_ENL[3]	LDO_ENL[2]	LDO_ENL[1]	LDO_ENL[0]

ASIC

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
28	LDO_EN[7]	LDO_EN[6]	LDO_EN[5]	LDO_EN[4]	LDO_EN[3]	LDO_EN[2]	LDO_EN[1]	LDO_EN[0]

LDO_ENL[7–0] and LDO_EN[7–0]

Valid values include:

0 (Default) Tri-states the specified highway.

1 Enables the specified highway.

TDM Stream Output Enable register (LDO_ENU)



Only the FPGA includes this register.

Provides enables for outgoing TDM highways 8 through 15. This read/write register has a reset value of 0x00.

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2C	LDO_ENU[7]	LDO_ENU[6]	LDO_ENU[5]	LDO_ENU[4]	LDO_ENU[3]	LDO_ENU[2]	LDO_ENU[1]	LDO_ENU[0]

LDO_ENU[7–0]

Valid values include:

0 (Default) Tri-states the specified highway.

1 Enables the specified highway.

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Highway Select (HWYSEL)

Only the FPGA includes this register.

This read/write register has a reset value of 0x00.

Offset	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
2C	LDO_ENU[7]	LDO_ENU[6]	LDO_ENU[5]	LDO_ENU[4]	LDO_ENU[3]	LDO_ENU[2]	LDO_ENU[1]	LDO_ENU[0]

TBD

Valid values for each bit include:

0 (Default) Internal highway connects to corresponding external highway from the set of lower 8.

0 (Default) Internal highway connects to corresponding external highway from the set of upper 8.

DIO Output Enable register (DIO_OE)

Provides enables for all the Digital I/O pins. At power-up (reset), all pins default to inputs. This read/write register has a reset value of 0x00.

Offset	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
40	DIO_OE[7]	DIO_OE[6]	DIO_OE[5]	DIO_OE[4]	DIO_OE[3]	DIO_OE[2]	DIO_OE[1]	DIO_OE[0]
44	DIO_OE[15]	DIO_OE[14]	DIO_OE[13]	DIO_OE[12]	DIO_OE[11]	DIO_OE[10]	DIO_OE[9]	DIO_OE[8]

DIO_OE[7–0] and DIO_OE[15–8]

Valid values include:

0 (Default) Tri-states the corresponding DIO pin, which you can then use as an input.

1 Drives the value stored in the Digital I/O output value register onto the corresponding Digital I/O pin.

DIO Output Value register (DIO_O)

Provides the output values for all the Digital I/O pins.

When enabled by the DIO_EN register as an output, a Digital I/O output drives the value stored in this register (output is non-inverting). This read/write register has a reset value of 0x00.

A read of this register returns the value in this register, not the value of the DIO pin.

Offset	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
48	DIO_O[7]	DIO_O[6]	DIO_O[5]	DIO_O[4]	DIO_O[3]	DIO_O[2]	DIO_O[1]	DIO_O[0]
4C	DIO_O[15]	DIO_O[14]	DIO_O[13]	DIO_O[12]	DIO_O[11]	DIO_O[10]	DIO_O[9]	DIO_O[8]

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DIO_O[7–0] and DIO_O[15–8]
Valid values include:

0 (Default) Drives the corresponding digital I/O pin to a logical 0 (zero).

1 Drives the corresponding digital I/O pin to a logical 1.

DIO Input Value register (DIO_I)

Reports the input status of the Digital I/O pins. All DIO inputs are double-synchronized through FCLK clocked DFFs (FCLK must be "clocking" to read the input levels on the pins).

This read-only register has a reset value of DIO[15:0] input levels.

A write of this register has no effect.

Offset	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
50	DIO_I[7]	DIO_I[6]	DIO_I[5]	DIO_I[4]	DIO_I[3]	DIO_I[2]	DIO_I[1]	DIO_I[0]
54	DIO_I[15]	DIO_I[14]	DIO_I[13]	DIO_I[12]	DIO_I[11]	DIO_I[10]	DIO_I[9]	DIO_I[8]

DIO_I[7–0] and DIO_I[15–8]
Valid values include:

0 (Default) Indicates that the LVTTL I/O pin level is low.

1 Indicates the LVTTL level is high.

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B CPLD

This appendix details the CPLD, which provides watchdog control, FPGA loading control, IPMI support, and ready bus buffering.

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To ensure future compatibility, write 0s to all RSVD (Reseved) bits.

CPLD Code Number (38460000, read only)

The code type programmed into the CPLD. You can use it to determine the product (ENP-3511) and functional configuration for software purposes.

I/O port	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
38460000	CTYP[7]	CTYP[6]	CTYP[5]	CTYP[4]	CTYP[3]	CTYP[2]	CTYP[1]	CTYP[0]

CPLD Revision Number (38468000, read only)

The revision level of code programmed into the CPLD. Related to the revision level of the board assembly, there is no one-to-one correspondence, because some board revisions do not significantly change the board function.

I/O port	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
38468000	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]

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Data Direction register (38470000, read/write)

This byte controls the output drive of the four RTM signals. Setting a bit enables its associated driver, so that the RTM signal is equal to the values written to the Data Value register. Clearing a bit makes the associated RTM pin an input, and the Data Value register bit is ignored. This register is cleared during reset.

I/O port	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
3847000	RSVD	RSVD	RSVD	RSVD	DOE3	DOE2	DOE1	DOE0

Data Value register (38478000, read/write)

Reads the value of the SMI, THRM, and four RTM signals, as well as controls the RTM signals. During a read, all six bits indicate the current level of the on-board signals. A write to this register loads an internal register with the desired four RTM data values. If the associated Data Direction register bit is set, this internal value is driven onto the RTM signal lines. If the Data Direction bit is cleared, the associated signal is an input. Reads from this address always indicate the pin value. This register is cleared during reset.

I/O port	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
3847800	RSVD	RSVD	SMID	THRMD	RTMD3	RTMD2	RTMD1	RTMD0

SMID Current state of the interrupt signal from IPMI processor.

THRMD Current state of thermal alarm signal from IPMI processor.

RTMD*n* Current value of RTM signal.

Interrupt Pending/Clear register (38480000, read/write)

Indicates pending external and internal interrupts to the IXP-1200 StrongARM processor.

An interrupt is pending if the interrupt condition occurs and the corresponding pending bit is not cleared. All pending interrupts with the corresponding interrupt enable bits set are OR'ed to form the CPLD interrupt. The StrongARM also has other interrupt sources which are combined with the CPLD interrupt.

You can use this register to determine the interrupting source for interrupt service routines. More than one bit may be true at any time.

Setting any of these bits during a register write clears the interrupt pending bit. Writing a zero to the register has no effect.

I/O port	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
38478000	RSVD	RSVD	SMII	THRMI	RTMI3	RTMI2	RTMI1	RTMI0

SMII A 1 (one) indicates active transition on interrupt signal from IPMI processor.

THRMI A 1 (one) indicates active transition on thermal alarm signal from IPMI processor.

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RTMI*n* A 1 (one) indicates low-to-high transition on the associated RTM signal.

Interrupt Enable Mask register (38488000, read/write)

Allows independent enabling and disabling of the CPLD interrupts. Setting a mask bit causes an interrupt if the corresponding interrupt pending bit is set. All pending interrupts are OR'ed to form the CPLD interrupt. This register is cleared during reset, interrupts disabled.

I/O port	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
38488000	RSVD	RSVD	SMIM	THRMM	RTMM3	RTMM2	RTMM1	RTMM0

SMIM Interrupt enable bit for IPMI SMI (interrupt) signal.

THRMM Interrupt enable bit for IPMI thermal alarm signal.

SMIM Interrupt enable bit for RTM signal transition.

Watchdog Enable register (38490000, read/write)

Controls the watchdog function.

I/O port	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
3849000	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	WDENA

WDENA Watchdog enable bit.

0 (Default; reset value) Disables watchdog. You can disable the watchdog anytime during the strobe period.

1 Starts the watchdog period. After starting the period, you must strobe the watchdog repeatedly to prevent a reset. If the span between strobes exceeds 1.0 to 1.5 seconds, the watchdog generates a board reset.

FPGA Configuration register (38498000, read/write)

Controls loading of the on-board FPGA. The upper four bits are process status bits from the FPGA. This register is cleared during reset. This register has no effect with ENP-3511-C boards



You must set on-board configuration resistors to give control to the IXP1200 instead of the EPC2 configuration EPROMs.

I/O port	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
3849800	CBSY	CSTAT	CDONE	IDONE	RSVD	RSVD	RSVD	CONF

CBSY: Configuration busy signal from FPGA. This bit is read-only.

0 The FPGA can accept data.

1 The FPGA cannot accept data.

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CSTAT: Configuration status signal from FPGA. This bit is read-only.

- 0 Indicates that the configuration process has not started.
- 1 Indicates that the configuration process started.

CDONE: Configuration done signal from FPGA. This bit is read-only.

- 0 The FPGA has not completed configuration.
- 1 The FPGA has completed configuration.

IDONE: Initialization done signal from FPGA. This bit is read-only.

- 0 The FPGA has not completed initialization.
- 1 The FPGA has completed initialization.

CONF Configuration start control signal to FPGA.

- 0 (Default; reset value) Disables FPGA loading.
- 1 Initializes the FPGA for loading.

Status Control register (38518000, read/write)

Controls the two board status LEDs and the automatic front/rear Ethernet switch.

I/O port	*Bit 7*	*Bit 6*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
38518000	RSVD	RSVD	MAN	FRNT	RSVD	RSVD	RSVD	RSVD

MAN Ethernet switch control. Valid values include:

- 0 (Default) Automatic front/back control of Ethernet 0 port.
- 1 Manual control.

FRNT Front connector use. Valid values include:

- 0 (Default) back (backplane/RTM) Ethernet connection.
- 1 Front connector used.

If the value in MAN is 0 (zero), this bit is ignored.

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C Connectors, jumpers, and resistors

This appendix details the connectors on the ENP-3511 CPU board and gives the signal pinout of each connector.



For more information about connectors on the ENP-3511 RTM, see *Chapter 4, ENP-3511 RTM.*

This product includes the connectors listed in the table below. When reading this file online, you can immediately view information about any connector by placing the mouse cursor over a connector name and clicking.

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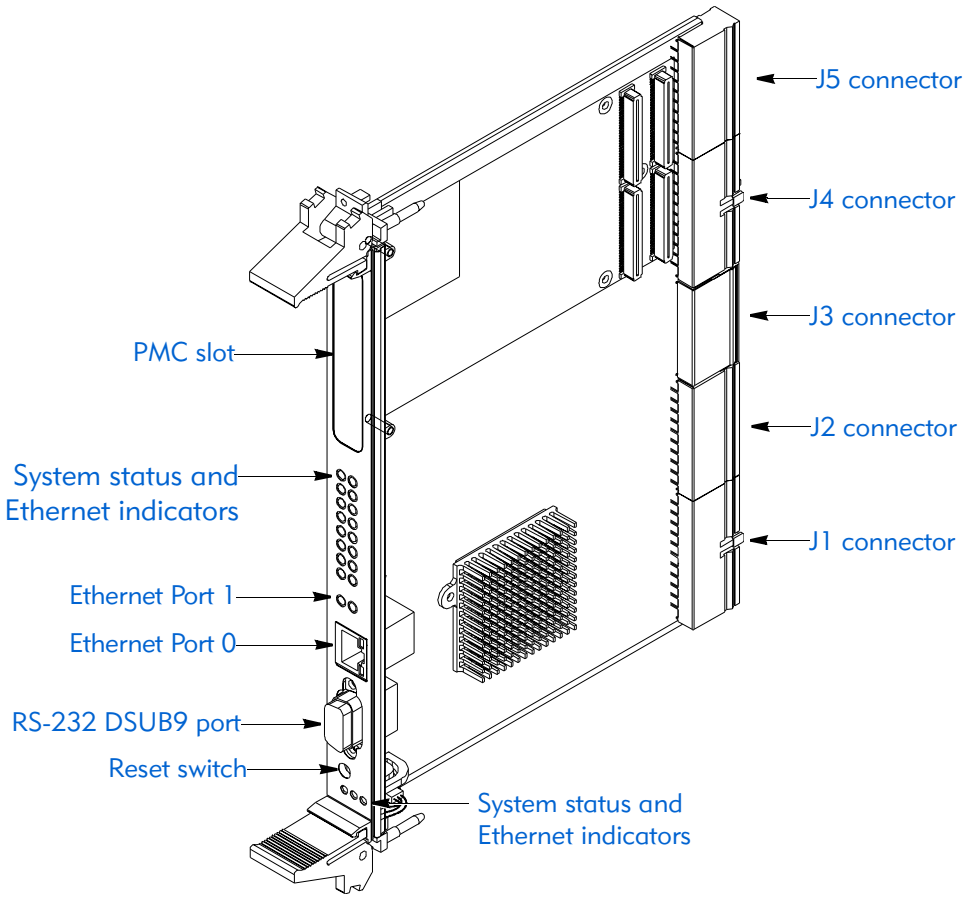
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Connector locations

Figure C-1 shows the locations of the connectors on the ENP-3511's CPU board.

For information about installing peripherals and jumper settings, see *Chapter 2, Configuration and installation*.

Figure C-1. ENP-3511 connector locations



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CompactPCI connectors

All these signals have the standard CompactPCI R2.1 bus definitions. The key is universal for these connectors.

Notes

These footnote descriptions apply to all the CompactPCI tables:

[1] This diagram defines the pin assignments from the front of the system chassis.

[2] The VIO signals are either 5V or 3.3V, depending on the system backplane implementation.

[3] This pin pulled high and not used.

[4] This pin pulled low and not used.

[5] Connector P1 pin D21 (M66EN/GND)is defined as M66EN for 66MHz backplanes.

[6] Connector P1 pin C16 (long, level 3) was originally used for early power to hot swap capable boards for controlling the buffer logic. The PICMG Hot Swap Subcommittee no longer considers this method viable, and other alternatives are under consideration.

[7] This pin not connected.

[8] BRSV signals accommodate PCI reserved signals. Backplanes shall bus these signals even though the PCI specification defines these pins as no connects.

[9] Observation: Some manufacturers of top shields utilize every other ground pin while some use every ground pin. Note: Shield connections mate at approximately the same time as medium length pins.

[10] Connects to Jn3.

[11] Connects to Jn4.

[12] This is a long pin for early power during hot-swap.

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J1 connector

The CompactPCI J1 connector is a female 2mm-pitch 6 column by 25 row right angle Hard Metric (HM) connector with a guide lug in the center.

Table C-1. CompactPCI J1 connector

Pin	A	B	C	D	E	F
25	+5V	~REQ64	~ENUM	+3.3V	+5V	GND
24	AD[1]	+5V	VIO[2]	AD[0]	~ACK64	GND
23	+3.3V	AD[4]	AD[3]	+5V	AD[2]	GND
22	AD[7]	GND	+3.3V	AD[6]	AD[5]	GND
21	+3.3V	AD[9]	AD[8]	M66EN[5]	C/~BE[0]	GND
20	AD[12]	GND	VIO[2]	AD[11]	AD[10]	GND
19	+3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	~SERR	GND	+3.3V	PAR	C/~BE[1]	GND
17	+3.3V	IPMBCLK	IPMBDAT	GND	~PERR	GND
16	~DEVSEL	GND	VIO[2,6]	STOP	~LOCK[3]	GND
15	+3.3V	~FRAME	~IRDY	~BD_SEL	~TRDY	GND
14–12	Key area					
11	AD[18]	AD[17]	AD[16]	GND	C/~BE[2]	GND
10	AD[21]	GND	+3.3V	AD[20]	AD[19]	GND
9	C/~BE[3]	IDSEL	AD[23]	GND	AD[22]	GND
8	AD[26]	GND	VIO[2]	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	~REQ0	GND	+3.3V	CLK	AD[31]	GND
5	BRSV[8]	BRSV[8]	~RST	GND	~GNT0	GND
4	IPMI:SMBP WR	~HEALTHY	VIO[2]	INTP[7]	INTS[7]	GND
3	~INTA	~INTB[7]	~INTC[7]	+5V	~INTD[7]	GND
2	TCK	+5V	TMS	TDO	TDI	GND
1	+5V	–12V	~TRST	+12V	+5V	GND

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J2 connector

The CompactPCI J2 connector is a female 2mm-pitch 6 column by 22 row right angle Hard Metric (HM) connector.

Table C-2. CompactPCI J2 connector

Pin	A	B	C	D	E	F[9]
22	GA4	GA3	GA2	GA1	GA0	GND
21	CLK6[7]	GND[7]	RSV[7]	RSV[7]	RSV[7]	GND
20	CLK5[7]	GND	RSV[7]	GND	RSV[7]	GND
19	GND[7]	GND[7]	RSV[7]	RSV[7]	RSV[7]	GND
18	BRSV[8]	BRSV[8]	BRSV[8]	GND	BRSV[8]	GND
17	BRSV[8]	GND	~PRST	~REQ6[7]	~GNT6[7]	GND
16	BRSV[8]	BRSV[8]	~DEG[7]	GND	BRSV[8]	GND
15	BRSV[8]	GND	~FAL[7]	~REQ5[7]	~GNT5[7]	GND
14	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	AD[38]	GND	VIO[2]	AD[37]	AD[36]	GND
12	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	AD[45]	GND	VIO[2]	AD[44]	AD[43]	GND
10	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	AD[52]	GND	VIO[2]	AD[51]	AD[50]	GND
8	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	AD[59]	GND	VIO[2]	AD[58]	AD[57]	GND
6	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	C/~BE[5]	~64EN	VIO[2]	C/~BE[4]	PAR64	GND
4	VIO[2]	BSRV[8]	C/~BE[7]	GND	C/~BE[6][7]	GND
3	CLK4[7]	GND	~GNT3[7]	~REQ4[7]	~GNT4[7]	GND
2	CLK2[7]	CLK3[7]	~SYSEN[3]	~GNT2[7]	~REQ3[7]	GND
1	CLK1[7]	GND	~REQ1[7]	~GNT1[7]	~REQ2[7]	GND

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J3 connector

The J3 connector is a user-defined connector that routes T1/E1 and Ethernet signal pairs and LED controls to the RTM for specific use with the 8-port Serial 2-port Ethernet RTM.

J3 provides the interface for PCI Ethernet signaling and LED control as well as IX Ethernet signaling and LED control.

The four connections, labeled CAP:RTMn and CPLD:RTMn respectively, are reserved; no functions are programmed into these devices.

Table C-3. CompactPCI J3 connector

Pin	A	B	C	D	E	F
19	GND	GND	GND	GND	GND	GND
18	ENET1:TD+	ENET1:TD–	GND	No connect	No connect	GND
17	ENET1:RD+	ENET1:RD–	GND	No connect	No connect	GND
16	ENET2:TD+	ENET2:TD–	GND	No connect	No connect	GND
15	ENET2:RD+	ENET2:RD–		No connect	No connect	
14	GND	GND	GND	+3.3V	+3.3V	GND
13	ENET1:~ACT	ENET1:~LINK	GND	ENET2:~ACT	ENET2:~LINK	GND
12	PHY:TDR7+	PHY:TDR7–	GND	PHY:TDR6+	PHY:TDR6–	GND
11	PHY:RFR7+	PHY:RFR7–	GND	PHY:RFR6+	PHY:RFR6–	GND
10	PHY:~LED7_1	PHY:~LED7_2	GND	PHY:~LED6_1	PHY:~LED6_2	GND
9	PHY:TDR5+	PHY:TDR5–	GND	PHY:TDR4+	PHY:TDR4–	GND
8	PHY:RFR5+	PHY:RFR5–	GND	PHY:RFR4+	PHY:RFR4–	GND
7	PHY:~LED5_1	PHY:~LED5_2	GND	PHY:~LED4_1	PHY:~LED4_2	GND
6	PHY:TDR3+	PHY:TDR3–	GND	PHY:TDR2+	PHY:TDR2–	GND
5	PHY:RFR3+	PHY:RFR3–	GND	PHY:RFR2+	PHY:RFR2–	GND
4	PHY:~LED3_1	PHY:~LED3_2	GND	PHY:~LED2_1	PHY:~LED2_2	GND
3	PHY:TDR1+	PHY:TDR1–	GND	PHY:TDR0+	PHY:TDR0–	GND
2	PHY:RFR1+	PHY:RFR1–	GND	PHY:RFR0+	PHY:RFR0–	GND
1	PHY:~LED1_1	PHY:~LED1_2	GND	PHY:~LED0_1	PHY:~LED0_2	GND

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J4 connector

J4 provides the connection to the H.110 CT Time Division Multiplexed (TDM) bus, which provides up to 32 highways of 8.192MHz data, for a total of 4096 timeslots, or simplex connections. For detailed information about the H.110 bus, see the ECTF *H.110 Hardware Compatibility Specification: CT Bus, Revision 1.0*.

Table C-4. CompactPCI J4 connector

Pin	A	B	C	D	E	F
25	SGA4	SGA3	SGA2	SGA1	SGA0	No connect
24	GA4	GA3	GA2	GA1	GA0	No connect
23	+12V[7]	~CT_RST	~CT_EN	–12V[7]	CT_MC[3]	No connect
22	RSVD[7]	RSVD[7]	RSVD[7]	RSVD[7]	RSVD[7]	No connect
21	SELVbat[7]	RSVD[7]	RSVD[7]	RSVD[7]	SELVbatRTN[7]	No connect
20	No connect[12]	No connect	No connect	No connect	No connect	No connect
19	No connect	No connect	No connect	No connect	No connect	No connect
18	VRG[7]	No connect	No connect	No connect	VRGRtn[7]	No connect
17	No connect	No connect	No connect	No connect	No connect	No connect
16	No connect	No connect	No connect	No connect	No connect	No connect
15	Vbat[7,12]	No connect	No connect	No connect	VbatRTN[7,12]	No connect
14–12	Key area					
11	CT_D29	CT_D30	CT_D31	V(I/O)	~CT_FRAME_A	GND
10	CT_D27	+3.3V[7]	CT_D28	+5V[7,12]	~CT_FRAME_B	GND
9	CT_D24	CT_D25	CT_D26	GND[12]	~FR_COMP	GND
8	CT_D21	CT_D22	CT_D23	+5V[7]	CT_C8_B	GND
7	CT_D19	+5V[7]	CT_D20	GND[12]	CT_C8_A	GND
6	CT_D16	CT_D17	CT_D18	GND[12]	CT_NETREF_1	GND
5	CT_D13	CT_D14	CT_D15	+3.3V[7,12]	CT_NETREF_2	GND
4	CT_D11	+5V[7]	CT_D12	+3.3V[7,12]	SCLK	GND
3	CT_D8	CT_D9	CT_D10	GND[12]	SCLKX2	GND
2	CT_D4	CT_D5	CT_D6	CT_D7	GND[12]	GND
1	CT_D0	+3.3V[7]	CT_D1	CT_D2	CT_D3	GND

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J5 connector

J5 provides the connection for all T1/E1 pairs and LED control from PMC connector Jn4. J5 also provides connection paths between the RTM and the TDM2IX and the CPLD.

The four connections, labeled CAP:RTMn and CPLD:RTMn respectively, are reserved; no functions are programmed into these devices.

Table C-5. CompactPCI J5 connector

Pin	A	B	C	D	E
22	TX1_T[11]	No connect	No connect	No connect	No connect
21	TX1_R[11]	No connect	No connect	No connect	No connect
20	RX1_T[11]	No connect	No connect	No connect	No connect
19	RX1_R[11]	No connect	No connect	No connect	No connect
18	TX2_T[11]	No connect	No connect	No connect	No connect
17	TX2_R[11]	No connect	No connect	No connect	No connect
16	RX2_T[11]	No connect	No connect	No connect	No connect
15	RX2_R[11]	No connect	No connect	No connect	No connect
14	TX3_T[11]	No connect	No connect	No connect	No connect
13	TX3_R[11]	No connect	No connect	No connect	No connect
12	RX3_T[11]	No connect	No connect	No connect	No connect
11	RX3_R[11]	No connect	No connect	No connect	No connect
10	TX4_T[11]	No connect	No connect	No connect	No connect
9	TX4_R[11]	No connect	No connect	No connect	No connect
8	RX4_T[11]	No connect	No connect	No connect	No connect
7	RX4_R[11]	No connect	No connect	No connect	No connect
6	No connect	No connect	No connect	No connect	No connect
5	No connect	No connect	No connect	No connect	No connect
4	12C:SCL[10]	12C:SDA[10]	GND	GND	GND
3	CPLD:RTM2	CPLD:RTM3	CAP:RTM0	CAP:RTM1	No connect
2	CPLD:RTM0	CPLD:RTM1	TMS:DAT	TMS:DAT	No connect
1	CAP:RTM2	CAP:RTM3	+5V	+12V	No connect

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PMC connectors

Jn1 connector

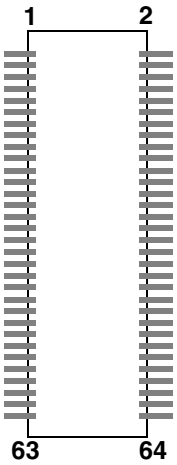


Table C-6. Jn1 pinout (32-bit local PCI)

Pin	Signal	Pin	Signal
1	TCK[1]	2	–12V
3	GND	4	PCI:~IRQA[3]
5	PCI:~IRQB[3]	6	PCI:~IRQC[3]
7	~BUSMODE1[1]	8	VCC
9	PCI:IRQD[3]	10	PCI:Reserved[1]
11	GND	12	PCI:[1]
13	PCI:CLK_PMC	14	GND
15	GND	16	PCI:~GNT1
17	PCI:~REQ1	18	VCC
19	VIO	20	PCI:AD[31]
21	PCI:AD[28]	22	PCI:AD[27]
23	PCI:AD[25]	24	GND
25	GND	26	PCI:C/BE[3]
27	PCI:AD[22]	28	PCI:AD[21]
29	PCI:AD[19]	30	VCC
31	VIO	32	PCI:AD17[]
33	PCI:~FRAME	34	GND
35	GND	36	PCI:~IRDY
37	PCI:~DEVSEL	38	VCC
39	GND	40	PCI:~LOCK[2]
41	PCI:Reserved	42	PCI:Reserved
43	PCI:PAR	44	GND
45	VIO	46	PCI:AD[15]
47	PCI:AD[12]	48	PCI:AD[11]
49	PCI:AD[9]	50	VCC
51	GND	52	PCI:C/BE[0]
53	PCI:AD[6]	54	PCI:AD[5]
55	PCI:AD4[]	56	GND
57	VIO	58	PCI:AD[3]
59	PCI:AD[2]	60	PCI:AD[1]
61	PCI:AD[0]	62	VCC
63	GND	64	REQ64[2]

Notes: VIO = +3.3V

[1] Not connected on main board. Signal name shown is name of connector pin.

[2] Pulled up, but not driven.

[3] Connected to resistor strap on main board for interrupt selection.

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Jn2 connector

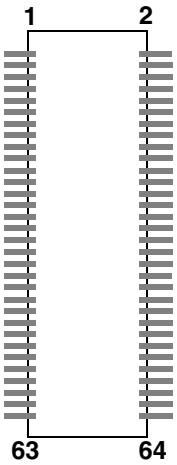


Table C-7. Jn2 pinout (32-bit local PCI)

Pin	Signal	Pin	Signal
1	+12V	2	~TRST[1]
3	TMS[1]	4	TDO[1]
5	TDI[1]	6	GND
7	GND	8	PCI:Reserved[1]
9	PCI:Reserved[1]	10	PCI:Reserved[1]
11	~BUSMODE2HI[2]	12	+3.3V
13	PCI:~RST	14	~BUSMODE3LO[2]
15	+3.3V	16	~BUSMODE4LO[2]
17	PCI:Reserved[1]	18	GND
19	PCI:AD[30]	20	PCI:AD[29]
21	GND	22	PCI:AD[26]
23	PCI:AD[24]	24	+3.3V
25	PCI:IDSEL[3]	26	PCI:AD[23]
27	+3.3V	28	PCI:AD[20]
29	PCI:AD[18]	30	GND
31	PCI:AD[16]	32	PCI:C/BE[2]
33	GND	34	PMC:Reserved[1]
35	PCI:~TRDY	36	+3.3V
37	GND	38	PCI:~STOP
39	PCI:~PERR	40	GND
41	+3.3V	42	PCI:~SERR
43	PCI:C/BE[1]	44	GND
45	PCI:AD[14]	46	PCI:AD[13]
47	GND	48	PCI:AD[10]
49	PCI:AD[8]	50	+3.3V
51	PCI:AD[7]	52	PCI:Reserved[1]
53	+3.3V	54	PCI:Reserved[1]
55	PMC:Reserved[1]	56	GND
57	PMC:Reserved[1]	58	PMC:Reserved[1]
59	GND	60	PMC:Reserved[1]
61	PCI:~ACK64[4]	62	+3.3V
63	GND	64	PMC:Reserved[1]

[1] Not connected on main board. Signal name shown is name of connector pin.

[2] Value of ~BUSMODE(4:2) is LLH, set with pull-ups and pull-downs.

[3] Connected on main board to PCI:AD[17]

[4] Pulled up, but not driven.

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Jn3 connector

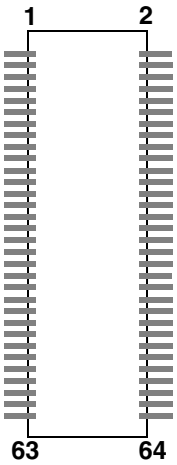


Table C-8. Jn3 pinout (telecom/I/O)

Pin	Signal	Pin	Signal
1	CT:LDO[0]	2	JN3_MUX[9][1]
3	IX:~PMCCS	4	CT:LDI[0]
5	CT:LDO[1]	6	CT:LDI[1]
7	CT:LDO[2]	8	JN3_MUX[0][1]
9	CT:LDO[3]	10	CT:LDI[2]
11	GND	12	CT:LDI[3]
13	CT:LDO[4]	14	GND
15	GND	16	CT:LDI[4]
17	CT:LDO[5]	18	JN3_MUX[1][1]
19	IX:~SRBUFSLRD	20	CT:LDI[5]
21	CT:LDO[6]	22	CT:LDI[6]
23	CT:LDO[7]	24	GND
25	GND	26	CT:LDI[7]
27	IX:SRBUFSLWR	28	JN3_MUX[2][1]
29	LREF[0]	30	JN3_MUX[3][1]
31	UT:RXERR[2]	32	JN3_MUX[4][1]
33	TCLKOUT	34	GND
35	12C_SCL	36	12C_SDA
37	LREF[1]	38	JN3_MUX[5][1]
39	GND	40	JN3_MUX[6][1]
41	UT:RXPRTY[2]	42	JN3_MUX[7][1]
43	LREF[2]	44	GND
45	UT:RXSOF[2]	46	JN3_MUX[8][1]
47	UT:RXEOF[2]	48	H_LSC3
49	LREF[3]	50	UT:TXERR[2]
51	GND	52	CT:FGA0
53	UT:~RXENB[2]	54	UT:TXPRTY[2]
55	GND	56	GND
57	UT:TXCLK[2]	58	TDMCLK2PMC
59	GND	60	UT:TXSOF[2]
61	UT:RXCLK[2]	62	UT:TXEOF[2]
63	GND	64	UT:~TXENB[2]

[1] Resistor strap settings on the PBA determine the pin functionality.

[2] Signals with the UT: prefix are only for RadiSys development use.

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Table C-9. PMC connector Jn3 signal summary

Signal name	Description
LDO[0-7]	Output data from the T8105 chip on the ENP-3511. Can be set by to 2.048, 4.096, or 8.192MHz rate via T8105 configuration registers.
LDI[0-7]	Input data to the T8105 chip on the ENP-3511. Can be set by to 2.048, 4.096, or 8.192MHz rate via T8105 configuration registers.
LREF[0-3]	These signals are connected to L_REF[0–3] on the T8105 on the ENP-3511. They are alternative master clock inputs for the T8105 on the ENP-3511. These signals are connected to the T1/E1 span derived clock signals on the PMC, allowing the ENP-3511's T8105 to derive its master clock from any of the four T1/E1 spans. This is not recommended unless the ENP3510 is H.110 bus master. See T8105 data sheet for details on L_REF stand-alone reference signal usage.
TCLKOUT	*Not connected* on the ARTIC 4-port T1/E1/J1 Line PMC. This signal is connected to the TCLKOUT pin of the T8105 on the ENP-3511.
I2C_SCL	I^2C interface clock that provides T1/E1 LED signaling to the RTM.
I2C_SDA	I^2C interface data that provides T1/E1 LED signaling to the RTM.
H_LSC3	*Not connected* on the ARTIC 4-port T1/E1/J1 Line PMC. Connects to L_SC3 pin on T8105 chip on the ENP-3511. This pin is user configurable and can be programmed through the T8105 configuration registers.
FGA0	Connects to FGA0 pin on T8105 chip on the ENP-3511. This pin provides a frame sync to the PMC and is configurable through the T8105 configuration registers.
TDMCLK2PMC	Connects to L_SC2 pin on T8105 chip on the ENP-3511. This pin provides a clock signal to the PMC and is configurable through the T8105 configuration registers. For the ARTIC 4-port T1/E1/J1 Line PMC, this should be set for 2.048MHz.

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Jn4 connector

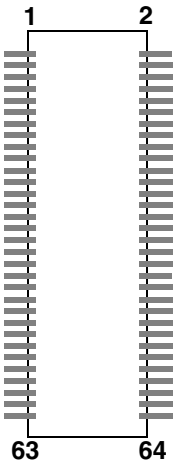


Table C-10. Jn4 pinout (telecom I/O)

Pin	Signal	Pin	Signal
1	No connect	2	TX3_T
3	TX1_T	4	TX3_R
5	TX1_R	6	GND
7	GND	8	RX3_T
9	RX1_T	10	RX3_R
11	RX1_R	12	IX:SRBUFD[0]
13	TX2_T	14	TX4_T
15	IX:SRBUFD[1]	16	TX4_R
17	TX2_T	18	GND
19	TX2_R	20	RX4_T
21	GND	22	RX4_R
23	RX2_R	24	IX:SRBUFD[2]
25	IX:SRBUFD[3]	26	IX:SRBUFD[4]
27	IX:SRBUFD[5]	28	IX:SRBUFD[6]
29	IX:SRBUFD[7]	30	GND
31	UT:RXFA	32	UT:TXFA[1]
33	GND	34	UT:TXPFA[1]
35	UT:RXPFA[1]	36	UT:TXSFA[1]
37	UT:RXVAL[1]	38	UT:TXADR[0][1]
39	UT:RXADR[0][1]	40	UT:TXADR[1][1]
41	UT:RXADR[1][1]	42	No connect
43	UT:RXADR[2][1]	44	GND
45	UT:RXDAT[0][1]	46	UT:TXADR[2][1]
47	GND	48	UT:TXDAT[0][1]
49	UT:RXDAT[1][1]	50	UT:TXDAT[1][1]
51	UT:RXDAT[2][1]	52	UT:TXDAT[2][1]
53	UT:RXDAT[3][1]	54	UT:TXDAT[3][1]
55	UT:RXDAT[4][1]	56	GND
57	UT:RXDAT[5][1]	58	UT:TXDAT[4][1]
59	GND	60	UT:TXDAT[5][1]
61	UT:RXDAT[6][1]	62	UT:TXDAT[6][1]
63	UT:RXDAT[7][1]	64	UT:TXDAT[7][1]

[1] Signals with the UT: prefix are only for RadiSys development use.

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Ethernet

Port 0

This RJ-45 connector, located on the front panel, provides support for one 10/100BASE-T Ethernet channel.

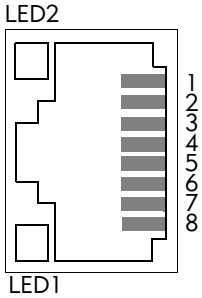


Table C-11. Ethernet RJ-45 (Port 0) pinout

Pin	Signal	Pin	Signal
1	Transmit+	5	Center tap transmit
2	Transmit–	6	Receive–
3	Receive+	7	Center tap receive
4	Center tap transmit	8	Center tap receive

Table C-12. RJ-45 (Port 0) LEDs

LED	Color	Signal
1	Yellow	Activity
2	Green	Link

The Ethernet 10/100 ports support cables with lengths up to 100 m with CAT 5 rated wiring and RJ-45 connectors. The ENP-3511 does not include such cables.

Port 1

Table C-13. RJ-45 (Port 1) LEDs

Color	LED
Yellow	Activity
Green	Link

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Flash

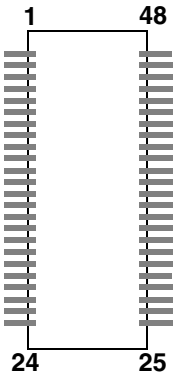


Table C-14. Flash pinout

Pin	Signal	Pin	Signal
1	SR_BUF_A15	48	SR_BUF_A16
2	SR_BUF_A14	47	+3.3V
3	SR_BUF_A13	46	GND
4	SR_BUF_A12	45	SR_BUF_D15 (D31)
5	SR_BUF_A11	44	SR_BUF_D7 (D23)
6	SR_BUF_A10	43	SR_BUF_D14 (D20)
7	SR_BUF_A9	42	SR_BUF_D6 (D22)
8	SR_BUF_A8	41	SR_BUF_D13 (D29)
9	Not connected	40	SR_BUF_D5 (D21)
10	LATA20	39	SR_BUF_D12 (D28)
11	~SRSLWR	38	SR_BUF_D4 (D20)
12	RESET_OUT	37	+3.3V
13	+3.3V	36	SR_BUF_D11 (D27)
14	~WP	35	SR_BUF_D3 (D19)
15	LATA19	34	SR_BUF_D10 (D26)
16	SR_BUF_A18	33	SR_BUF_D2 (D18)
17	SR_BUF_A17	32	SR_BUF_D9 (D25)
18	SR_BUF_A7	31	SR_BUF_D1 (D17)
19	SR_BUF_A6	30	SR_BUF_D8 (D24)
20	SR_BUF_A5	29	SR_BUF_D0 (D16)
21	SR_BUF_A4	28	~SRSLRD
22	SR_BUF_A3	27	GND
23	SR_BUF_A2	26	~SR_BUF_C E0
24	SR_BUF_A1	25	SR_BUF_A0

Address lines in parentheses are connections for the second flash part.

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RS-232 DSUB9 port (COM 1)

The RS-232 serial port, located on the front panel, is a male, 9-pin, DSUB connector.

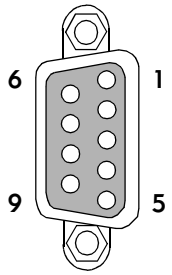


Table C-15. DB-9 pin-out

Pin	Signal	Pin	Signal
1	Not connected	6	Not connected
2	Receive data	7	Not connected
3	Transmit data	8	Not connected
4	DTR (always asserted)	9	Not connected
5	Signal ground		

The serial port uses a standard RS-232 cable. The ENP-3511 does not include this cable.

Headers

Altera CPLD JTAG port (J8)

This is a standard JTAG port for programming Altera CPLD devices using an Altera ByteBlasterMV device.

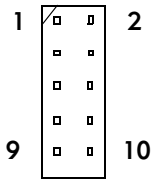


Table C-16. Altera CPLD JTAG port (J8)

Pin	Signal	Pin	Signal
1	TCK	2	GND
3	TDO	4	+3.3V
5	TMS	6	No connect
7	No connect	8	No connect
9	TDI	10	GND

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POST card header (J13)

This header, avialable on the PBA, generates POST signals.

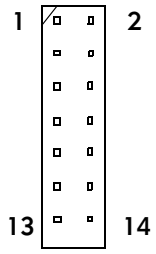


Table C-17. Altera CPLD JTAG port (J13)

Pin	Signal	Pin	Signal
1	VCC	2	IX:SRBUFD[0]
3	IX:SRBUFD[1]	4	IX:SRBUFD[2]
5	IX:SRBUFD[3]	6	IX:SRBUFD[4]
7	IX:SRBUFD[5]	8	IX:SRBUFD[6]
9	IX:SRBUFD[7]	10	POST:~PWRGD
11	POST:~CS	12	POST:~IOW
13	GND	14	GND

Programming headers

FPGA EEPROM programming header (J15)

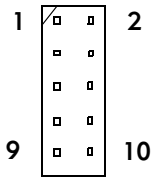


Table C-18. FPGA EEPROM programming header (J15)

Pin	Signal	Pin	Signal
1	TCK	2	GND
3	TDO	4	+3.3V
5	TMS	6	No connect
7	No connect	8	No connect
9	TDI	10	GND

IPMI programming header (J9)

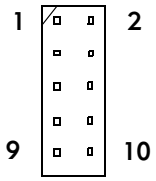


Table C-19. IPMI programming header (J9)

Pin	Signal	Pin	Signal
1	+5V_ALRM	2	~XIOW/H8DO
3	H8_MUX_EN	4	PGM_H8
5	RST_H8	6	No connect
7	GND	8	~ALRMCS2/H9DI
9	No connect	10	No connect

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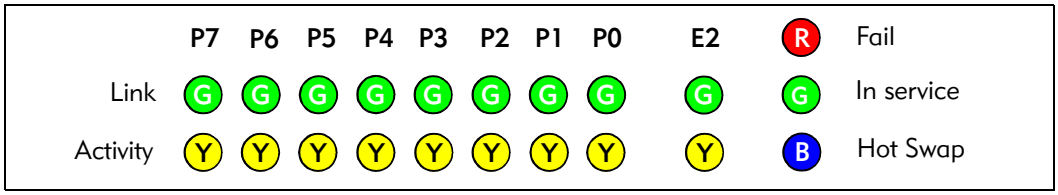
Front panel

System status and Ethernet indicators

The front panel of the ENP-3511 houses an array of lights that indicate system status, and Ethernet connections and activity. P7 through P0, shown in the next figure, are the Link and Activity indicators for the eight ports coming from the IXF440. E2 indicates the Link and Activity of the second 82559 Ethernet port.

The Link and Activity from the first 82559 Ethernet port is indicated in the PCI Ethernet RJ45 on the front panel. Fail, In Service, and Hot Swap lights indicate system status.

Figure C-2. Front panel indicator lights



Reset switch

The reset is a momentary push-button recessed switch. It is available on the front panel to manually force reset.

Cable compatibility

The serial port functions with a standard RS-232 cable. The Ethernet 10/100 ports support cables with lengths up to 100m with CAT 5 rated wiring and RJ-45 connectors.

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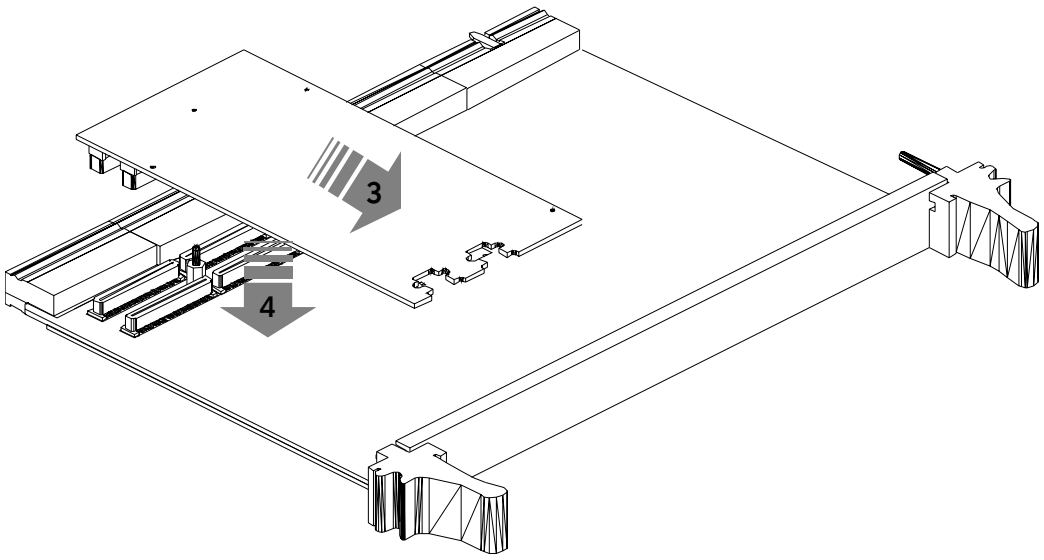
D PMC modules

The ENP-3511 can accept most 32-bit PMC modules that are mechanically compliant to the PMC standard.

Installing a PMC module on the main board

You can install a PMC module on the ENP-3511 as shown below.

Figure D-1. Installing a PMC module



To install a PMC module:

Avoid causing ESD damage:

- Remove PMCs from their antistatic bags only in a static-free environment.
- Perform the installation process (described later in this chapter) only in a static-free environment.
- During external cable installation, ensure that the cables are not active. PMCs are not designed for hot insertion of any interface.

PMCs, like most other electronic devices, are susceptible to electrostatic discharge (ESD) damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

1. Remove the ENP-3511 from the CompactPCI chassis as described in *Removing the ENP-3511* on page 14.

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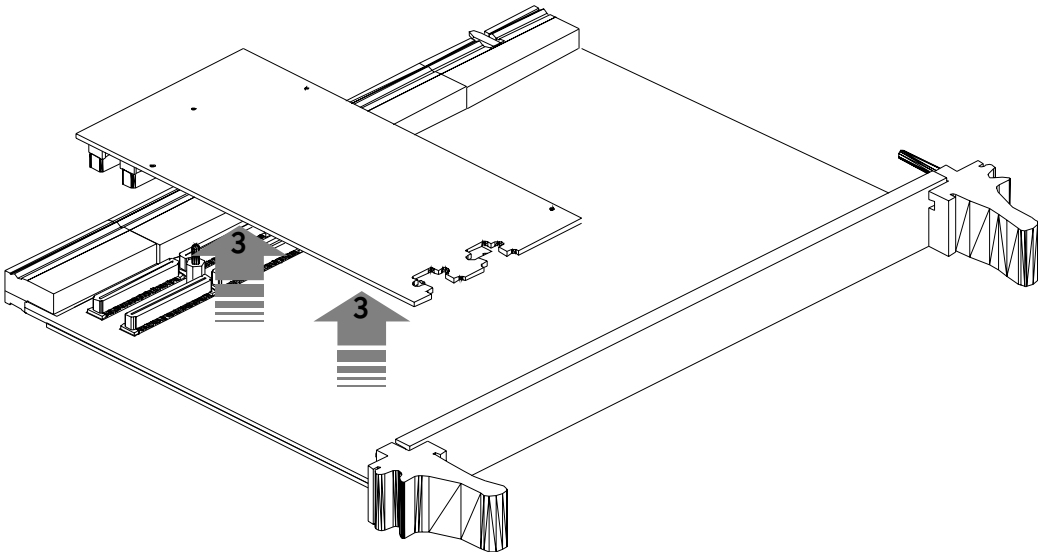
2. Remove and save the blank face plate from the PMC slot in the ENP-3511 face plate.
3. Position the PMC bezel through the PMC slot on the front panel.
4. Push the rear connectors into the main board.
5. Insert and tighten the screws on the back of the main board.
6. Replace the ENP-3511 in the CompactPCI chassis as described in *Inserting the ENP-3511* on page 11.

Disconnecting the PMC module

If your ENP-3511 includes an optional PMC module, you must disassemble the board before performing maintenance or upgrades on the ENP-3511.

To separate the PMC module and the main board:

Figure D-2. Separating a PMC module from the main board



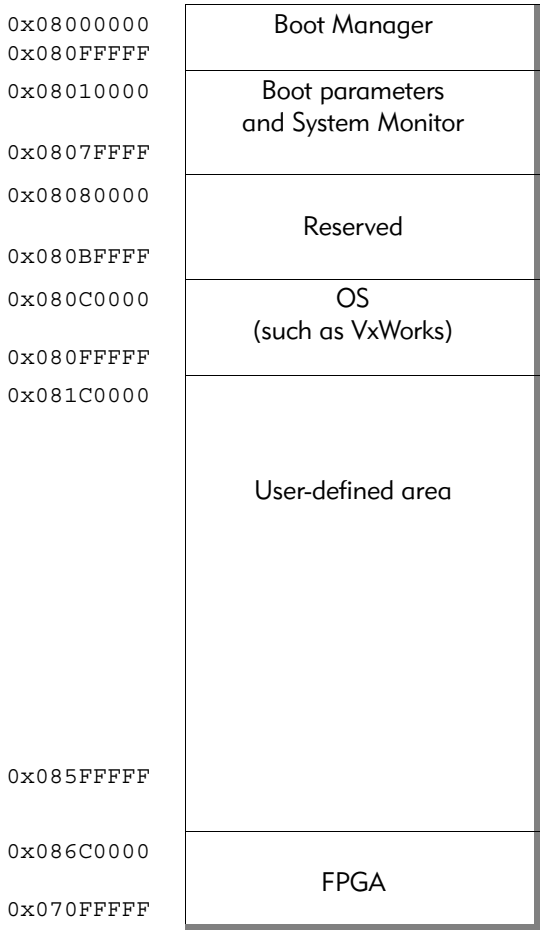
1. Remove the ENP-3511 from the CompactPCI chassis as described in *Removing the ENP-3511* on page 14.
2. Remove screws on the back of the main board.
3. Pull the boards apart while keeping them parallel. Continue applying force until the connectors completely disengage.

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E Flash memory addresses

The ENP-3511 flash chip contains these major sections:

Figure E-1. Flash chip configuration



For information about re-programming the flash chip's contents, see *Appendix C: Re-programming the Flash chip* in the *ENP Programmer's Guide*.

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Glossary

Access time — A factor in measurement of a memory storage device's operating speed. It is the amount of time required to perform a read operation. More specifically, it is the period of time between which the memory receives a read command signal and the time when the requested data becomes available to the system data bus.

Address — A number that identifies the location of a word in memory. Each word in a memory storage device or system has a unique address. Addresses are always specified as a binary number, although octal, hexadecimal, and decimal numbers are often used for convenience.

APM 1.1 — (Advanced Power Management) A software interface specification that allows operating system device drivers to control the power management functionality of a PC.

ANSI — (American National Standards Institute) An organization dedicated to advancement of national standards related to product manufacturing.

ATA — (AT Bus Attachment) An interface definition for PC peripherals. See *IDE*.

Autotype — A convenient method of IDE device detection whereby the system BIOS queries the IDE device to obtain operational parameters. If the device supports autotype, this information is passed to the BIOS where it is used to automatically configure the drive controller.

BDA — (BIOS Data Area) BIOS Data Area. A 256 byte block of DRAM starting at address 400H that contains data initialized and used by the System BIOS detailing the system configuration and errors encountered during POST.

BGA — Ball Grid Array.

Bit — A binary digit.

Boot — The process of starting a computer and loading the operating system from a powered down state (cold boot) or after a computer reset (warm boot). Before the operating system loads, the computer performs a general hardware initialization and resets internal registers.

Boot block — A write-protected 16KB section of the flash boot device located at physical address FFFFC000h to FFFFFFFFh which contains code to perform rudimentary hardware intitialization at system power up. The boot block also contains code to recover the BIOS via floppy disk.

Boot device — The storage device from which the computer boots the operating system.

Boot sequence — The order in which a computer searches external storage devices for an operating system to boot. The boot device must be the first in the boot sequence.

Byte — A group of 8 bits.

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CPU	(Central Processing Unit) A semiconductor device which performs the processing of data in a computer. The CPU, also referred to as the microprocessor, consists of an arithmetic/logic unit to perform the data processing, and a control unit which provides timing and control signals necessary to execute instructions in a program.
Chipset	One or more integrated circuits that, along with a CPU, memory, and other peripherals, implements an IBM PC-AT compatible computer. The chipset typically implements a DRAM controller, bus, interface logic, and PC peripheral devices.
CAS	(Column Address Strobe) An input signal from the DRAM controller to an internal DRAM latch register specifying the column at which to read or write data. The DRAM requires a column address and a row address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of column addresses and row addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required.
COM port	A bi-directional serial communication port which implements the RS-232 specification.
CMOS	(Complimentary Metal Oxide Semiconductor) A fast, low power semiconductor RAM used to store system configuration data.
Conventional memory	The first 640 KB of a computer's total memory capacity. If a computer has no extended memory, conventional memory equals the total memory capacity. In typical computer systems, conventional memory can contain BIOS data, the operating system, applications, application data, and terminate and stay resident (TSR) programs. Also called system memory.
CSR	(CMOS Save and Restore) A System BIOS feature that allows the user to backup the contents of CMOS RAM (contained within the real time clock) to the BIOS Flash device to be restored later if necessary (such as when the real time clock battery dies).
CHS	(Cylinders/Heads/Sectors) A specification of disk drive operating parameters consisting of the number of disk cylinders, disk drive read/write heads, and disk sectors.
Default	The state of all user-changeable hardware and software settings as they are originally configured before any changes are made.
DOS	(Disk Operating System) One or more programs which allow a computer to use a disk drive as an external storage device. These programs manage storage and retrieval of data to and from the disk and interpret commands from the computer operator.
Driver	A software component of the operating system which directs the computer interface with a hardware device. The software interface to the driver is standardized such that application software calling the driver requires no specific operational information about the hardware device.
DIP	(Dual In-Line Package) A semiconductor package configuration consisting of a rectangular plastic case with two rows of pins, one row on each lengthwise side.
DRAM	(Dynamic Random Access Memory) A semiconductor RAM memory device that does not permanently store data, even with power applied, unless the data are periodically rewritten into memory during a refresh operation. See *SDRAM*.

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EEPROM	(Electrically Erasable Programmable ROM) Specifically, those EPROMs which may be erased electrically as compared to other erasing methods.
Error checking and correction	A feature of the T2 chipset that enables it to detect single or multi-bit errors in DRAM reads and correct single bit errors. This feature requires that all banks of DRAM use x36 (parity) SO DIMMs.
ECP	(Extended Capabilities Port) An enhancement of the standard PC parallel port that allows high speed bi-directional data transfers and other features.
EDO	(Extended Data Out) A type of DRAM that allows higher memory system performance since the data pins are still driven when CAS# is de-asserted. This allows the next DRAM address to be presented to the device sooner than with Fast Page Mode DRAM.
Extended memory	The RAM address space, in a computer so equipped, above the 1 MB level.
ESCD	(Extended System Configuration Data) A block of nonvolatile memory that stores information on the devices found and configured by the Plug and Play BIOS.
External device	A peripheral or other device connected to the computer from an external location via an interface cable.
FPM	(Fast Page Mode) A “standard” type of DRAM that is lower performance than EDO.
Fixed disk	A hard disk drive or other data storage device having no removable storage medium. Fixed disk storage devices use inflexible disk media and are sealed to prevent data loss due to media surface contamination. Fixed disks generally provide the most storage space for a given cost when compared to semiconductor, tape, and other popular mass storage technologies.
FPGA	(Field Programmable Gate Array) A large, general-purpose logic device that is programmed at power-up to perform specific logic functions.
FBD	(Flash Boot Device) A flash memory device containing the computer’s BIOS. In the NY1210, a 1 MByte Intel 28F800B5 semiconductor flash memory containing the system and video BIOS images, the BIOS initializing code and the recovery code which allows self hosted reflashing.
Flash memory	A fast EEPROM semiconductor memory typically used to store firmware such as the computer flash image. Flash memory also finds general application where a semiconductor non-volatile storage device is required.
Flash recovery	A process whereby an existing, corrupt flash image in the flash boot device is overwritten with a new image. Also referred to as a flash recovery.
Flash update	A process whereby an existing, uncorrupted flash image in the flash boot device is overwritten with a new image. Also referred to as a flash update.
Force update	See *FPGA*.
GB or GByte	(Gigabyte) Approximately one billion (US) or one thousand million (Great Britain) bytes. 2^30 = 1,073,741,824 bytes exactly.

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Hang	A condition where the system microprocessor suspends processing operations due to an anomaly in the data or an illegal instruction.
Header	A mechanical pin and sleeve style connector on a circuit board. The header may exist in either a male or female configuration. For example, a male header has a number and pattern of pins which corresponds to the number and pattern of sleeves on a female header plug.
h	(Hexadecimal) A base-16 numbering system using numeric symbols 0 through 9 plus alpha characters A, B, C, D, E, and F as the 16 digit symbols. Digits A through F are equivalent to the decimal values 10 through 15.
Host bus	The address/data bus that connects the CPU and the chipset.
ISA	(Industry Standard Architecture) A popular microcomputer expansion bus architecture standard. The ISA standard originated with the IBM PC when the system bus was expanded to accept peripheral cards.
I/O	(Input/Output) The communication interface between system components and between the system and connected peripherals.
IDE	(Integrated Drive Electronics) A hard disk drive/controller interface standard. IDE drives contain the controller circuitry at the drive itself, as compared to the location of this circuitry on the computer motherboard in non-IDE systems. IDE drives typically connect to the system bus with a simple adapter card containing a minimum of on-board logic.
IRDA or IrDA	(Infra-red Data Association) A specification for high-speed data communication using infrared drivers and receivers for short-range wireless data transmission.
INT	(Interrupt Request) A software-generated interrupt request.
IRQ	(Interrupt Request) In ISAbus systems, a microprocessor input from the control bus used by I/O devices to interrupt execution of the current program and cause the microprocessor to jump to a special program called the interrupt service routine. The microprocessor executes this special program, which normally involves servicing the interrupting device. When the interrupt service routine is completed, the microprocessor resumes execution of the program it was working on before the interruption occurred.
ISR	(Interrupt Service Routine) A program executed by the microprocessor upon receipt of an interrupt request from an I/O device and containing instructions for servicing of the device.
Jumper	A set of male connector pins on a circuit board over which can be placed coupling devices to electrically connect pairs of the pins. By electrically connecting different pins, a circuit board can be configured to function in predictable ways to suit different applications.
KB or KByte	(Kilobyte) Approximately one thousand bytes. 2^{10} = 1024 bytes exactly.
Logical address	The memory-mapped location of a segment after application of the address offset to the physical address.
LBA	(Logical Block Addressing) A method the system BIOS uses to reference hard disk data as logical blocks, with each block having a specific location on the disk. LBA

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	differs from the CHS reference method in that the BIOS requires no information relating to disk cylinders, heads, or sectors. LBA can be used only on hard disk drives designed to support it.
MB or MByte	(Megabyte) Approximately one million bytes. 2^20 = 1,048,576 bytes exactly.
Memory	A designated system area to which data can be stored and from which data can be retrieved. A typical computer system has more than one memory area. See *Conventional memory* and *Extended memory*.
Memory shadowing	Copying information from an extension ROM into DRAM and accessing it in this alternate memory location.
Offset	The difference in location of memory-mapped data between the physical address and the logical address.
Operating system	See *DOS*.
PMC	(PCI Mezzanine Card) A new standard form factor for PCI add-in modules. PMCs mate with their respective connectors on the motherboard and are secured with screws.
PCI	(Peripheral Connect Interface) A popular microcomputer bus architecture standard.
Peripheral device	An external device connected to the system for the purpose of transferring data into or out of the system.
PC/AT	(Personal Computer/Advanced Technology) A popular computer design first introduced by IBM in the early 1980s.
PS/2	(Personal System 2) Computers designed with IBM's proprietary bus architecture known as Micro Channel.
PLL	(Phase-Locked Loop) A semiconductor device which functions as an electronic feedback control system to maintain a closely regulated output frequency from an unregulated input frequency. The typical PLL consists of an internal phase comparator or detector, a low pass filter, and a voltage controlled oscillator which function together to capture and lock onto an input frequency. When locked onto the input frequency, the PLL can maintain a stable, regulated output frequency (within bounds) despite frequency variance at the input.
Physical address	The address or location in memory where data is stored before it is moved as memory remapping occurs. The physical address is that which appears on the computer's address bus when the CPU requests data from a memory address. When remapping occurs, the data can be moved to a different memory location or logical address.
Pinout	A diagram or table describing the location and function of pins on an electrical connector.
PQFP	(Plastic Quad Flat Pack) A popular package design for integrated circuits of high complexity.
POST	(Power On Self Test) A diagnostic routine which a computer runs at power up. Along with other testing functions, this comprehensive test initializes the system chipset and

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hardware, resets registers and flags, performs ROM checksums, and checks disk drive devices and the keyboard interface.

Program A set of instructions a computer follows to perform specific functions relative to user need or system requirements. In a broad sense, a program is also referred to as a software application, which can actually contain many related, individual programs.

PAL (Programmable Array Logic) A semiconductor programmable ROM which accepts customized logic gate programming to produce a desired sum-of-products output function.

RAM (Random Access Memory) Memory in which the actual physical location of a memory word has no effect on how long it takes to read from or write to that location. In other words, the access time is the same for any address in memory. Most semiconductor memories are RAM.

RAS (Row Address Strobe) An input signal to an internal DRAM latch register specifying the row at which to read or write data. The DRAM requires a row address and a column address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of row addresses and column addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required.

Real mode The operational mode of Intelx86 CPUs that uses a segmented, offset memory addressing method. These CPUs can address 1 MB of memory using real mode.

Real mode address A memory address composed of two 16-bit values: a segment address and an offset quantity. A real mode address is constructed by shifting a segment address 4 bits to the left and then adding the offset value. A real mode address is a physical address.

when the computer is powered down.

Reflashing The process of replacing a BIOS image, in binary format, in the flash boot device.

Register An area typically inside the microprocessor where data, addresses, instruction codes, and information on the status on various microprocessor operations are stored. Different types of registers store different types of information.

Reset A signal delivered to the microprocessor by the control bus, which causes a halt to internal processing and resets most CPU registers to 0. The CPU then jumps to a starting address vector to begin the boot process.

RFA (Resident Flash Array) The RFA represents flash memory that is resident on the hardware platform that is utilized for OS or application purposes.

ROM (Read Only Memory) A broad class of semiconductor memories designed for applications where the ratio of read operations to write operations is very high. Technically, a ROM can be written to (programmed) only once, and this operation is normally performed at the factory. Thereafter, information can be read from the memory indefinitely.

RS-232 A popular asynchronous bi-directional serial communication protocol. Among other things, the RS-232 standard defines the interface cabling and electrical characteristics, and the pin arrangement for cable connectors.

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RTC	(Real Time Clock) Peripheral circuitry on a computer motherboard which provides a nonvolatile time-of-day clock, an alarm, calendar, programmable interrupt, square wave generator, and a small amount of SSRAM. In the NY1210, the RTC operates independently of the system PLL which generates the internal system clocks. The RTC is typically receives power from a small battery to retain the current time of day.
RTM	Rear Transition Module.
SDRAM	(Synchronous Dynamic Random Access Memory) A memory device that does not permanently store data, even with the power applied, unless the data are periodically rewritten into memory during a refresh operation. SDRAM's memory access cycles are synchronized with the CPU clock to eliminate wait time associated with memory fetches between RAM and the CPU. See *DRAM*.
Segment	A section or portion of addressable memory serving to hold code, data, stack, or other information allowing more efficient memory usage in a computer system. A segment is the portion of a real mode address which specifies the fixed base address to which the offset is applied.
Serial port	A physical connection with a computer for the purpose of serial data exchange with a peripheral device. The port requires an I/O address, a dedicated IRQ line, and a name to identify the physical connection and establish serial communication between the computer and a connected hardware device. A serial port is often referred to as a COM port.
Shadow memory	RAM in the address range 0xC000h through 0xFFFFFh used for shadowing. Shadowing is the process of copying BIOS extensions from ROM into DRAM for the purpose of faster CPU access to the extensions when the system requires frequent BIOS calls. Typically, system and video BIOS extensions are shadowed in DRAM to increase system performance.
SIMM	(Single In-Line Memory Module) A small, rectangular circuit board on which is mounted semiconductor memory ICs.
SODIMM	(Small Outline Dual Inline Memory Module) A new form factor for memory modules that is smaller and denser than SIMMs.
Standoff	A mechanical device, typically constructed of an electrically non-conductive material, used to fasten a circuit board to the bottom, top, or side of a protective enclosure.
SRAM	(Static Random Access Memory) A semiconductor RAM device that permanently stores data as long as power is applied, without the need for periodically rewriting the data into memory.
SSRAM	(Synchronous Burst SRAM) A semiconductor RAM device that permanently stores data as long as power is applied, without the need for periodically rewriting the data into memory. SDRAM's memory access cycles are synchronized with the CPU clock to eliminate wait time associated with memory writes between RAM and the CPU. See *SRAM*.
Symmetrically addressable SIMM	A SIMM, the memory content of which is configured as two independent banks. Each 16-bit wide bank contains an equal number of rows and columns and is independently addressable by the CPU via twin row address strobe registers in the DRAM controller.

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SYSCLK (ISAbus System Clock) The ~8.33MHz clock signal present on the ISAbus to which all bus transactions are synchronized.

System memory See *Conventional memory*.

TB or TByte (Terabyte) Approximately one thousand billion (US) or one billion (Great Britain) bytes. 2^40 = 1,099,511,627,776 bytes exactly.

USB (Universal Serial Bus) A new serial data bus that is intended to eliminate the need for separate serial, parallel, mouse, keyboard, joystick, etc. ports on a PC-compatible. These ports can be conceivably replaced by a few, daisy-chained USB ports, all with identical connectors but capable of much higher throughput, upwards of 12Mbs.

UED (User Editable Drive) A feature of the NY1210's Phoenix NuBIOS. When a "User" type hard disk drive setting shows in the IDE Adapter Sub-Menu the BIOS queries the hard disk drive for the purpose of retrieving disk geometry. If the hard disk drive is capable of providing this information, the BIOS uses it to automatically set up the drive for use with the system.

VESA (Video Electronics Standards Association) A group of hardware and software vendors that define specifications for hardware and software interfaces for a variety of devices.

VGA (Video Graphics Adapter) A popular PC graphics controller and display adapter standard developed by IBM. The standard specifies, among other things, the resolution capabilities of the display device. Display devices meeting the VGA standard must be capable of displaying a minimum resolution of 640 horizontal pixels by 480 vertical pixels with at least 16 screen colors.

Wait state A period of one or more microprocessor clock pulses during which the CPU suspends processing while waiting for data to be transferred to or from the system data or address buses.

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