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RadiSys

EPC® -3311 Hardware Reference

www.radisys.com

007-01289-0005 • November 2003

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Safety

To avoid the risk of fire or electric shock, carefully follow the instructions provided in this manual.

Important

Always use caution when handling or operating the equipment. Only qualified and trained electronics service personnel should access the equipment. Use extreme caution when installing or removing components. For additional information, please contact RadiSys Technical Support at 866–385–6167 Monday through Friday between 6:00 a.m. and 5:00 p.m., PST, continental USA.

Wichtig

Arbeiten am System bzw. Betrieb des Systems, sollten immer mit der nötigen Vorsicht vorgenommen werden. Nur qualifiziertes und ausgebildetes Fachpersonal sollte am Inneren des Gerätes arbeiten. Beim Installieren und Entfernen von Komponenten ist besondere Vorsicht geboten.

Für weitere Informationen wenden Sie sich bitte an den Technical Support von RadiSys:

- **USA**: 866–385–6167 Montags bis Freitags von 0600 Uhr bis 1700 Uhr, Pacific USA.
- **International**: +31–36–5365595 Montags bis Freitags von 0830 Uhr bis 1700 Uhr. (CET GMT +1.00)

Changes or modifications not expressly approved by RadiSys Corporation could void the product warranty and the user's authority to operate the equipment.

Notice

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential environment.

This equipment generates, uses, and can emit radio frequency energy and, if not installed and used in accordance with this instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient the receiving antenna
- Relocate this equipment in relation to the receiver
- Place the AC power connection for this equipment on another circuit

Any change or modification not expressly approved by the manufacturer is prohibited and could void the user's authority to operate the equipment.

Shielded interface cables, if any, must be used in order to comply with the emission limits. Use of non-shielded cables may result in interference to TV and radio reception. The following booklet prepared by the FCC may be helpful.

"How to Identify and Resolve Radio-TV Interference Problems"

This booklet is available from the U.S. Government Printing Office, Washington, D.C. 20402, Stock No. 004-000-003454.

This product also meets requirements for compliance with EN55022 and EN55024, Class B ITE.

November2003
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Before you begin

This guide describes the EPC®-3311, a high performance single-slot CompactPCI† board that operates as either a host or task processor. It is fully compliant with PICMG† 2.16 for use with packet-switched backplanes and the dual Gigabit Ethernet channels offer maximum bandwidth to the backplane.

This book is for hardware and software designers, programmers, engineers, and those with a knowledge of electronics and/or programming who need to understand the operation of the EPC-3311.

About this guide

Contents

Chapter/appendix		Description
1	Introduction	Introduces the EPC-3311 and briefly describes its features and functions.
2	Installation and operation	Explains how to install the EPC-3311 in a CompactPCI mainframe.
3	BIOS configuration	Explains how to configure the BIOS using the built-in BIOS setup menus.
5	Theory of operation	Describes how EPC-3311 components provide a CompactPCI bus compatible embedded computer with standard PC peripherals plus PCI and ISA interfaces.
6	RTMs	Describes how to install, configure, and use the Rear Transition Module (RTM).
7	Hardware management	Provides hardware management information.
A	Chipset and I/O map	Maps the addresses used for I/O and by the chipset registers.
B	Interrupts	Shows the EPC-3311's interrupt assignments.
C	Flash memory addresses	Lists the EPC-3311 flash chip's major sections.
D	Connectors	Details the location, function, and pin-outs of the EPC-3311's connectors and LEDs.
E	Messages	Explains common error messages and start-up codes.
F	PMC modules	Describes how to install an optional PMC module.
G	CompactFlash cards	Describes how to install, configure, and use the optional CompactFlash card.

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Chapter/appendix		Description
H	FPGA features register set	Maps the address space used by the FPGA registers.
I	Re-programming the flash chip	Explains how to update or recover your system BIOS by re-programming all or part of the EPC-3311's flash chip

Notational conventions

This manual uses the following conventions:

- `Screen text and syntax strings appear in this font.`
- All numbers are decimal unless otherwise stated.
- Bit 0 is the low-order bit. If a bit is set to 1, the associated description is true unless otherwise stated.


Notes indicate important information about the product.


Tips indicate alternate techniques or procedures that you can use to save time or better understand the product.


The globe indicates a World Wide Web address.


The book indicates a book or file.


ESD cautions indicate situations that *may* cause damage to hardware via electro-static discharge (ESD).


Cautions indicate potentially hazardous situations which, if not avoided, *may* result in minor or moderate injury, or damage to data or hardware. It may also alert you about unsafe practices.


Warnings indicate potentially hazardous situations which, if not avoided, *can* result in death or serious injury.


Danger indicates imminently hazardous situations which, if not avoided, *will* result in death or serious injury.

Where to get more information

About the EPC-3311

You can find out more about EPC-3311 from these sources:

- **World Wide Web:** RadiSys maintains an active site on the World Wide Web. The site contains current information about the company and locations of sales offices, new and existing products, contacts for sales, service, and technical support information. You can also send e-mail to RadiSys using the web site.


When sending e-mail for technical support, please include information about both the hardware and software, plus a detailed description of the problem, including how to reproduce it.


To access the RadiSys web site, enter this URL in your web browser:
`http://www.radisys.com`

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Requests for sales, service, and technical support information receive prompt response.

- **Other**: If you purchased your RadiSys product from a third-party vendor, you can contact that vendor for service and support.

About related RadiSys products

82600 High Performance System Controller

A member of the RadiSys family of long-life embedded PC compatible core logic. the 82600 is a highly integrated single chip implementation of all requirements of a high performance Compact PCI Central Resource and Peripheral Bridge including the North Bridge, South Bridge, PCI to PCI Bridge, and a selected set of Super I/O functions targeted at embedded, PC-compatible systems. It supports Intel Celeron†, Pentium II, and Pentium III processors with 66MHz, 100MHz and 133MHz system bus frequencies.

CP50 chassis

A 9-U tall rack-mountable CompactPCI chassis that incorporates packet-switching technology, the CP50 is NEBS-compliant and provides a highly available, fault-tolerant platform through redundancy, system management reporting, and effective thermal design.

The chassis is an industry-standard, 19" wide housing that accomodates the system modules and provides power and communications busing for these components via a 21-slot wide backplane.

MM50 IDE Media Module

The MM50 IDE Media Module is a 4HP module used in CompactPCI systems which incorporates these features:

- Support for these IDE device types:
  - Notebook-style 2.5" IDE hard drives.
  - Notebook-style ATAPI CD-RW or ATAPI CD-RW/DVD.
- Support for these options:
  - MM50-01: Two 2.5" IDE drives (on a single bus).
  - MM50-02: One 2.5" IDE drive and one CD-RW or CD-RW/DVD drive (on a single bus).
- System Management support, using a microcontroller.
- A companion RTM which supports a dual-IDE MM50.
- Support for dual IPMBs (Intelligent Platform Management Buses).

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ESM/EFM-31xx blades

Single-slot CompactPCI PICMG 2.16 compliant Layer 2 and Layer 3 switches that feature 24 Fast Ethernet link ports, 4Gb up-links, and integrated platform management.

Other

PICMG

CompactPCI specification, PICMG. For information about PICMG and the CompactPCI standard, consult the PICMG website at this URL:



http://www.picmg.org

PCI architecture

PCI System Architecture, Fourth Edition, published by Addison-Wesley and authored by Mindshare, Inc.

PCI specifications, available at the PCI SIG web site:



www.pcisig.com

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1 Introduction

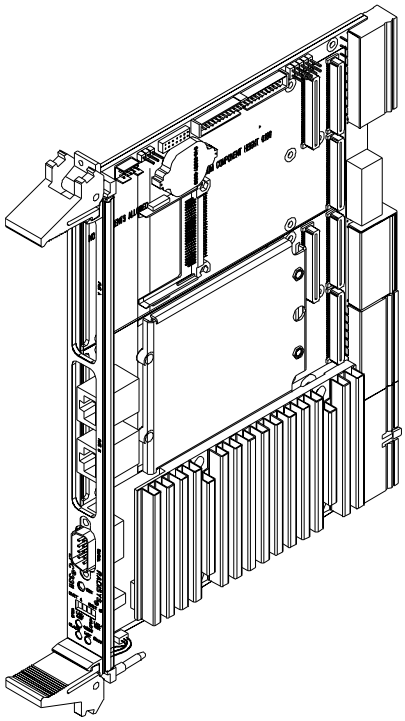
The EPC-3311 is a high performance, single slot CompactPCI board that operates as either a host or task processor. It is fully compliant with PICMG 2.16 for use with packet-switched backplanes and the dual Gigabit Ethernet channels offer maximum bandwidth to the backplane. The EPC-3311 uses the RadiSys 82600 chipset and a Mobile Intel† Pentium†III Processor-M. It also provides two PMC sites, allowing the use of a variety of PMC modules such as SCSI, LAN or WAN adapters. The EPC-3311 can operate in these environments:

- PICMG 2.16-compliant node slot.
- PICMG 2.0-compliant PCI system slot.
- PICMG 2.0-compliant PCI peripheral slot.

The EPC-3311 includes these subsystems:

- **CPU board**: A single-slot system controller which plugs into a 6U System Slot of a CompactPCI system.
- **Optional rear transition module**: A rear I/O transition module which plugs into a rear I/O slot of a CompactPCI system. The EPC-3311 can operate with either the RTML or the RTM216.

Figure 1-1. The EPC-3311



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The EPC-3311 requires a backplane that supports the *CompactPCI Specification Revision 2.1*.

The EPC-3311 can be ordered in these configurations:

Configuration	Description
EPC-3311-512	Includes 512 MB memory.
EPC-3311-1G	Includes 1 GB memory.
EPC-3311-RTM216	An RTM that works with the EPC-3311 in a 2.16-compliant system. This RTM has an additional optional PIM in place of the Ethernet connectors.
EPC-3311-RTML	An RTM that works with the EPC-3311 in a legacy (non-2.16) chassis. This RTM expands EPC-3311 connectivity and functionality for use as part of a CompactPCI computer system.
EPC-3311-HDD[1]	An onboard 2.5" IDE hard disk drive which occupies the space for the PMC "A" site.

[1] If you install this option, you can install only one PMC. Also, if you plan to install a CompactFlash, you must do so *before* installing the drive as the drive is mounted over the CompactFlash connector.

You can also add to the EPC-3311:

- One or two PMCs (either RadiSys or third-party). For information about installing a PMC, see *Appendix F, PMC modules*.
- A CompactFlash device. For information about CompactFlash cards, see *Appendix G, CompactFlash cards*.

  You cannot install a Processor PMC (such as the EPC-6315) the PMC A/B site when a CompactFlash is installed.

- IDE devices. The EPC-3311 supports a maximum of two IDE devices connected to the processor board or the RTM. For information about the IDE connectors, see *Appendix D, Connectors* and *Chapter 6, RTMs*.

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Features

- Mobile Intel Pentium III Processor-M (Tualatin):
  - 1200 MHz.
  - Micro FC-BGA (Flip Chip Ball Grid Array) package.
- A front side bus frequency of 133 MHz.
- A RadiSys 82600 High Integration Dual PCI System Controller, which includes:
  - Host bridge.
  - One Ultra DMA/33 EIDE channel.
  - One USB channel (with appropriate OS drivers).
  - One RS-232 serial (COM1) port (300 to 115,200 baud).
  - Hardware watchdog timer, two-stage configurable.
  - RTC (Real-Time Clock).
- A CR2032 Lithium (Li/MnO2) coin battery that powers the RTC to retain date, time, and CMOS parameters.
- A discrete memory module in capacities of 512 MB or 1 GB.
- An Intel Strataflash† BIOS/Flash ROM device of 4 MB.
- EPC-3311 CompactPCI bus configuration:
  - When installed in a system slot, the EPC-3311 functions as a system controller.
  - When installed in a peripheral slot, the EPC-3311 functions as a peripheral processor.
- Two Intel 82544EI 10/100/1000BASE-T Ethernet controllers incorporating internal MAC and PHY interface support for 10BASE-T, 100BASE-TX, or 1000BASE-T connectivity.
- Two 32-bit PCI +5V I/O compatible PMC sites.
  - These sites support Jn1 and Jn2, for local PCI signal and power.
  - Jn4 signals route out the CompactPCI J3/J5 connectors.
- IPMI hardware management controller, implementing dual IPMB. The controller uses an I^2C-style system management bus.
- Disk drives:
  - Optional bootable CF (CompactFlash†) via industry standard CF Type I socket.
  - Optional factory-installed onboard IDE hard disk drive.
  - IDE bus available for other IDE devices through an RTM connector.



You can use either the on-board or the RTM IDE bus; you cannot use both at the same time.

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- Front panel:
  - LEDs, including Hot Swap, user-status, blade, and Ethernet link/speed.
  - Reset button.
  - Injector/ejector levers (with a hot swap micro switch).

External interfaces

The EPC-3311 has external interfaces available from the front panel, the CompactPCI standard connectors J1-J5, and onboard interfaces. The RTM offers more connectors for the functions on the main board.

The front panel external indicators and interfaces are:

- Hot Swap micro switch contained within board ejector
- CompactPCI Blue Hot Swap LED
- Red/Green User LED for software status (IPMI-controlled)
- Red/Green Blade Status LED (IPMI-controlled)
- Ethernet Link/Activity (Speed) LEDs
- Reset switch
- COM 1 serial port on DE9 connector
- The CompactPCI backplane connections are:
  - J1/J2, 32-bit CompactPCI interface, +3.3V, +5V, and ±12V power
  - Ethernet 1 & 2, PMC J24 rear I/O signals, and Fused +3.3V and +5V to RTM
  - EIDE, keyboard, mouse, Serial port, USB, PMC J14 rear I/O signals

Onboard interfaces include:

- Two PMC sites (Jn1, Jn2, Jn4 connectors)
- Manufacturing test header
- IPMI HMC 10-pin programming header
- Processor ITP (installed only on prototypes)
- Battery holder (for a 20mm, 3V Lithium coin cell)
- Type I CompactFlash socket
- IDE 44-pin connector to support an onboard IDE drive

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Specifications

System specifications

Table 1-1. System specifications

Characteristic	Value
CPU	Mobile Intel Pentium III Processor-M with a 133 MHz front side bus. • 1200 MHz. • Micro FC–BGA package.
Chipset	RadiSys 82600 chipset (North bridge and P2P bridge).
Cache	512 KB Level 2 write-back cache operating at full clock speed.
Memory	• 512MB or 1GB. • ECC. • Single-bit error correction, double-bit detection (ECC mode only).
Addressing	Real and protected mode supported. • **Real address mode**: 20-bit • **Protected address mode**: 32-bit on PCI local bus
Data path	32-bit onboard processor bus at 133 MHz.
Flash memory	4 Mb (4096 KB x 8).
Clock/calendar	• Embedded Real-Time Clock. • Accurate to ±12 minutes/year, at 25°C. • Includes 256 bytes of CMOS SRAM in two 128 byte banks.
Power requirements with 512 MB SDRAM	***Input power*** ***30 W maximum*** +3.3V 3 A maximum/2.5 A typical +5V 3.5 A maximum/2.0 A typical +12V 0.1 A –12V 0.1 A **Note**: These values represent all components fully populated.
Battery	CR2032 Lithium (Li/MnO_2).

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Environmental

The EPC-3311 meets the following environmental specifications with no hard disk drive installed:

- The EPC-3311 is for use only with compatible UL Listed computers that have installation instructions detailing user installation of card cage accessories.
- The operating environment must provide sufficient airflow (300 LFM) across the board to keep it within its temperature specification. Failure to provide sufficient airflow may result in board failure.

Table 1-2. Environmental specifications

Parameter	Conditions	Detailed specification
Temperature (ambient)[1]	Operating	+5°C to 55°C (41°F to 131°F) derated 2°C per 1000 feet (300 m) over 6600ft (2000m) with 300 LFM airflow.
	Storage	–20°C to +60°C (–4°F to +140°F).
Relative humidity	Operating	20% to 80% non-condensing; 10% per hour maximum excursion gradient.
	Storage	5% to 85% non-condensing; 10% per hour maximum excursion gradient.
Vibration[2]	Operating	0.005G²/Hz from 5 to1000 Hz random, 10 min per sweep cycle.
	Storage	0.02G²/Hz from 5 to1000 Hz random, 10 min per sweep cycle.
Shock[2] (un-packaged)	Operating	5G, 11ms duration, half-sine shock pulse.
	Storage	15G, 11ms duration, half-sine shock pulse.
Altitude	Operating	0 to 15,000ft. (4,500 m).
	Storage	0 to 40,000 ft. (12,000 m).

[1] Ambient temperature is measured at the leading edge of the EPC-3311 heatsink with a 1200 MHz processor installed and all components fully populated. RadiSys validates the operating specifications of its products by testing with the "hottest" available hardware and software configuration to maximize the power supply draw and generate a worst-case scenario. Despite these efforts, the specifications outlined above are only benchmarks and should be regarded as such.

[2] Measured only under ambient temperature of 20°C to 30°C and ambient humidity of 30% to 60%.

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Additional specifications

Table 1-3. Additional EPC-3311 specifications

Characteristic	Value	
Mechanical[1]	EPC-3311	Standard 6U form factor; 100 mm x 160 mm x 20.32 mm.
	EPC-3311-RTM216	100 mm x 80 mm x 20.32 mm.
	EPC-3311-RTML	100 mm x 80 mm x 20.32 mm.
Heat sink	Provides sufficient cooling for the processor and other components as required when used in an environment providing 300 LFM airflow at a maximum ambient temperature of 55 °C.[2]	

[1] The EPC-3311's mechanical outline complies with IEEE 1101.1, 1101.11, and P1101.11 mechanical requirements.

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2 Installation and operation

Before using the EPC-3311, you need to determine how you want to install the board, install peripherals, and set switches and jumpers. This chapter explains how. To install or configure options for the EPC-3311, see the appropriate appendix:

- **CompactFlash card:** see *Appendix G, CompactFlash cards*.
- **PMC module:** see *Appendix F, PMC modules*.
- **RTM:** see *Chapter 6, RTMs*.



Other setup is done by configuring BIOS options as described in *Chapter 3, BIOS configuration*.

When reading this file online, you can immediately view information about any topic by placing the mouse cursor over a topic name and clicking

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Avoid causing ESD (electrostatic discharge) damage:

- Keep the card in its anti-static bag until you are ready to install.
- Install the card (as described later in this chapter) only in a static-free environment:
  - Wear an antistatic wrist strap attached to a known ground such as an antistatic lab mat.

    Um unbeabsichtigte Schäden durch elektrostatische Entladung vorzubeugen, sollte bei Arbeiten am System immer ein Erdungsarmband getragen oder andere elektrostatische Entladungs-Vorsichtsmaßnahmen verwendet werden.
  - Remove the card from its antistatic bag only in a static-free environment.
  - Avoid touching printed circuits, connector pins, and components. Where possible, hold the card only by its edges or mounting hardware.
  - Make the least possible movement with your body to minimize electrostatic charges created by contact with clothing fibers, carpet, and furniture.
  - Keep one hand on the computer chassis, if possible, as you insert or remove a card.
  - Avoid placing the card on the chassis cover or on a metal table. The cover and metal table increase the risk of damage because they provide an electrical path from your body through the card.

The EPC-3311, like most other electronic devices, is susceptible to ESD damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

Before you begin

The EPC-3311 requires the following:

- Adequate ventilation. Ensure that the platform complies with the environmental requirements listed in *Specifications* on page 5.
- A chassis such as the RadiSys CP50. For information about the CP50, see *CP50 chassis* on page v.

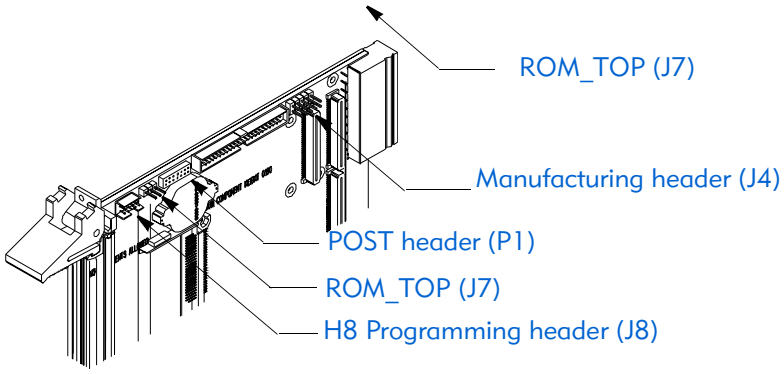


To install the EPC-3311 onto a passive backplane not manufactured by RadiSys, consult the instructions provided by the backplane manufacturer.

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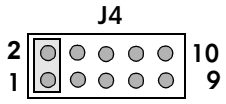
Setting jumpers and headers

Figure 2-1. EPC-3311: jumper locations



Manufacturing header (J4)

Figure 2-2. Manufacturing header settings



Enables writes to the ROM's *lower* 512KB in the top 1MB.

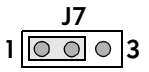
Function	Pins	Description
Write to the ROM's *lower* 512KB in the top 1MB.	1, 2	To write to the *lower* 512KB of the ROM, connect pin 1 to pin 2. **Note**: You must also connect pins 2 and 3 of J7 and write a '1' to bit 5 of register 0x0A. For information about J7, see *ROM_TOP (J7)* on page 12. For information about registers, see *Appendix H, FPGA features register set*.

All other settings are reserved for manufacturer use.

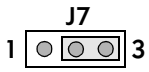
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ROM_TOP (J7)

Figure 2-3. ROM_TOP jumper settings



Moves the System BIOS to the flash chip's *upper* 512KB of the top 1MB.



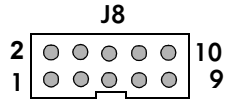
Moves the System BIOS to the flash chip's *lower* 512KB of the top 1MB.

For more information about the ROM, see *Appendix I, Re-programming the flash chip*.

Function	Pins	Description
Moves the ROM's *upper* 512KB in the top 1MB to the top of system memory.	1, 2	To access the *upper* 512KB of the ROM, connect pin 1 to pin 2. When the board resets, the program stored in the *upper* 512KB block runs. You will typically set the jumper in this position.
Moves the ROM's *lower* 512KB in the top 1MB to the top of system memory.	2, 3	To access the *lower* 512KB of the ROM, connect pin 2 to pin 3. When the board resets, the program stored in the *lower* 512KB block runs. **Note**: You must also connect pins 1 and 2 of J4 and write a '1' to bit 5 of register 0x0A. For information about J4, see *Manufacturing header (J4)* on page 11. For information about registers, see *Appendix H, FPGA features register set*.

H8 Programming header (J8)

Figure 2-4. H8 Programming header settings



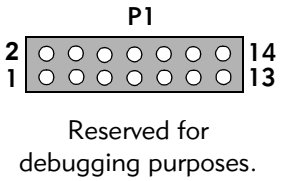
Reserved for manufacturing use.

This header is reserved for manufacturing use; no setup is required.

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POST header (P1)

Figure 2-5. P1 POST header settings



This header is reserved for debugging purposes; no setup is required.

Inserting the EPC-3311

You install the EPC-3311 on the backplane. Before installation, ensure that all options are installed on the EPC-3311 as described in *Maintaining and upgrading the EPC-3311* later in this chapter.

1. Ensure that the ejector handles are in the normal (non-eject) position. (Push the top handle down and the bottom handle up so that the handles are not tilted.)
2. Insert the EPC-3311 into the chassis subrack with the card edges in the card guide rails and carefully push the EPC-3311 into the chassis subrack until the CompactPCI connectors engage the connector body at the backplane.

   You insert the alignment pins on the board's I/O panel into the alignment holes in the card guide rails.

3. Simultaneously lock both injector/ejector levers on the board's I/O panel. Inspect the board's faceplate to ensure it is fully seated.
4. Tighten the retaining screws in the top and bottom of the front panel to ensure proper connector mating and to prevent the module from loosening due to vibration.
5. Install an optional RTM, if desired, as described in *Appendix E, Rear Transition I/O Modules*.
6. Connect peripherals to the EPC-3311. Periperals typically include a video display and keyboard, but also perhaps a mouse, modem, printer, and so on.

   Always power-off the system and disconnect all power cords from their source before connecting or disconnecting cables for peripheral devices.

   For information about specific peripherals and setup considerations, see *Peripheral devices* on page 18.

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For information about front-panel connector pinouts, see *Appendix C, Connectors*.



Observe the following while the system is powered up:

- Do not plug cables or connectors into the front panel connectors. Because electronics equipment generally cannot withstand fluctuations in power, damage can arise from plugging in a device or board while power is on.
- Do not plug in a serial or parallel device, keyboard, transceiver, monitor or other component. This applies to equipment at either end of an interface cable.

7. Complete remaining steps as required. Typical remaining steps include:
   - BIOS configuration (For information about setting up the BIOS configuration, see *Chapter 3, BIOS configuration*.).
   - Driver software installation.
   - Application software installation.

   Your system may be preconfigured by your supplier or you may be required to perform these tasks yourself.

Operation

Powering on the system

1. Connect all power cords.
2. Turn the power to your system on.

   If there is no power, Check all power connections and the power source.



System management can direct the EPC-3311 to remain unpowered. Ensure that any system management applications are properly configured to allow the board to power up.

The system can be powered and active, However, if a fault is detected, backend power is prevented.

The system executes the POST to ensure that the hardware is functional and properly configured, then starts the operating system. During the POST, you can use the BIOS configuration (see *BIOS configuration* on page 19 to configure the system.



Before using the processor board for the first time, verify the system settings in the BIOS Setup program. For details, see *Chapter 3, BIOS configuration*.

When System BIOS standard POST error codes occur, messages may display. For details, see *Appendix E, Messages*.

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Hot insertion/Hot swapping

Hot insertion and hot swapping behavior differs, depending upon the slot the board is in:

- **System slot:** The board resets and re-initializes the PCI bus to which it connects.
- **Peripheral slot:** The board initializes only itself. This does not affect the PCI bus.

Post-installation troubleshooting

The next table lists symptoms and possible solutions to some hardware problems that might occur after you install the EPC-3311.

Symptom	Possible solutions
The EPC-3311 Sys LEDs do not turn on at all or are very dim.	Ensure that the power supply can provide the rated power required for the EPC-3311. If the problem still persists, discontinue using the EPC-3311
The platform does not recognize an ESM-3100 in the EPC-3311 slot.	This is normal operation as the ESM-3100 does not connect to the PCI bus.
The Ethernet LEDs do not light.	The EPC-3311 is not receiving data. Ensure that the network cables are properly installed.
The EPC-3311 board overheats.	Ensure that the platform complies with the environmental requirements listed in *Specifications* on page 5. Install a booster fan.

Maintaining and upgrading the EPC-3311

Occasionally you will want to perform maintenance (such as replacing the battery) or upgrades (such as adding options) on the EPC-3311. When this occurs, you must extract the board from the chassis, repair or install the desired option, then re-install the board in the chassis.

If your EPC-3311 includes an option, you may need to disassemble the boards before upgrades or maintenance, then re-assemble the boards before re-inserting the EPC-3311 into the chassis. The following sections describe how.

Extracting the EPC-3311

Before performing certain maintenance operations such as replacing the battery or upgrading memory, you must remove the EPC-3311 from the chassis:

1. Loosen the retaining screws in the top and bottom of the front panel to prepare for connector release.
2. Move the ejector handles to the eject position: push the top handle up and the bottom handle down so that the handles appear tilted.
3. Slide the EPC-3311 module out of its slot. Pull firmly on the handles to release the module from the connectors.

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4. If your EPC-3311 includes an option, disassemble the board as described in *Dis-assembling the EPC-3311*.

Dis-assembling the EPC-3311

To separate an option board from the main board:

1. Remove the EPC-3311 in the chassis as described in *Extracting the EPC-3311*.
2. Remove the option as described below:
   - **CompactFlash card:** see *Appendix G, CompactFlash cards*.
   - **PMC module:** see *Appendix F, PMC modules*.
   - **RTM:** see *Chapter 6, RTMs*.

Replacing the battery



For more information about the battery, see *System battery* on page 56.

⚠ WARNING

- Due to risk of fire or explosion, do not attempt to recharge, force open, or heat the battery. There is danger of explosion if the battery is incorrectly installed. Replace the battery only with the same or equivalent type. Reference the battery manufacturer's packaging or labeling for further cautions and warnings.

  Wegen Feuer- oder Explosionsgefahr, versuchen Sie nicht die Batterie wieder aufzuladen, sie zu öffnen oder zu erhitzen. Bei falscher Installierung besteht eine Explosionsgefahr. Ersetzen Sie die Batterie nur mit einem Gleichen oder gleichwertigen Typ. Weitere Informationen und Warnungen entnehmen Sie bitte der Verpackung bzw. dem Aufdruck des Herstellers.
- The battery must be used or stored within the temperature specifications outlined on page 56.
- Bezüglich Betrieb und Lagerung der Batterie beachten Sie bitte die Temperaturspezifikationen auf Seite 56.

To replace the battery:

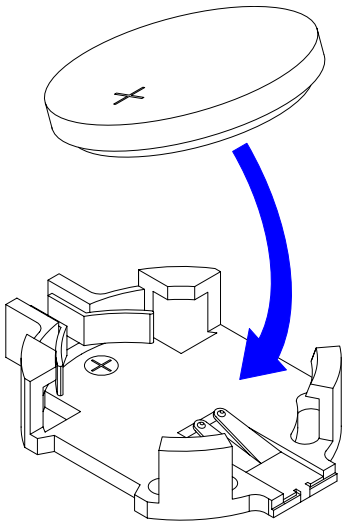
1. Before you begin, write down the CMOS setup parameters.
2. Turn off the power and disconnect all power cords.

   If you leave the power on when removing the battery, setup values are retained.
3. Remove the EPC-3311 from the chassis as described in *Extracting the EPC-3311*.
4. If your EPC-3311 includes an option, disassemble the board as described in *Dis-assembling the EPC-3311*.
5. Locate the battery on the main board (see Figure C-1), then lift the battery out, pushing the battery toward the positive end before lifting it out. The battery is located under the 2.5" HDD (when installed).

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6. Press the new battery into place, positive (+) side up.
   Note: The battery will not discharge voltage if installed backwards.



7. If your EPC-3311 includes an option, re-assemble the board as described in *Re-assembling the EPC-3311*.
8. Replace the EPC-3311 in the chassis as described in *Inserting the EPC-3311*.

After replacing the battery, system settings revert to manufacturer defaults. To restore your settings, run the BIOS program and enter the values you recorded in step 1 of this procedure. For more information about the BIOS program, see *Chapter 3, BIOS configuration*.

Installing other options

For information about installing other EPC-3311 options, see the appropriate appendix:

- **CompactFlash card:** see *Appendix G, CompactFlash cards*.
- **PMC module:** see *Appendix F, PMC modules*.

Re-assembling the EPC-3311

After performing maintenance operations such as replacing the battery or upgrading memory, you must reconnect the main board and option boards, and then re-install the EPC-3311 into the chassis.

To re-assemble the EPC-3311:

1. Install the option as described below:
   - **CompactFlash card:** see *Appendix G, CompactFlash cards*.
   - **PMC module:** see *Appendix F, PMC modules*.
   - **RTM:** see Appendix E, Rear Transition I/O Modules.
2. Replace the EPC-3311 in the chassis as described in *Inserting the EPC-3311*.

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Peripheral devices

This table lists and provides installation information regarding peripheral devices you might choose to connect to the EPC-3311.

Table 2-1. Attaching peripheral devices

Device(s)	Consideration
Serial	• These ports are 9-pin male D-Sub connectors on the I/O panels. • Only one serial device can be attached. • These ports provide a single RS-232 interface. • A serial device can be attached to *only* the processor board *or* the RTM.
USB	• The USB bus supports up to 127 USB devices, which can be attached in a daisy-chain configuration. • The EPC-3311 supports one USB controller on the RTM panel. • A single USB cable cannot exceed 5 meters (16.4 feet) in length. • Software drivers appropriate to the OS will be needed to operate USB devices. RadiSys does *not* supply such drivers. • The BIOS cannot boot from USB devices.
EIDE or IDE	• Up to two EIDE or IDE devices can be attached to the EIDE header on either the RTM or processor board. • The BIOS supports up to two EIDE or IDE devices. For more information on IDE operations, see *page 22*. • RTMs and on-board devices cannot be simultaneously accessed. There is a BIOS setup switch. **Note**: When using a flat cable to attach a device, the colored trace for pin 1 on the cable must align with pin 1 on the header/connector.
Floppy	The EPC-3311 does not support the legacy PC-style floppy drive. However, an ATAPI removable-media-style floppy drive may be connected to the RTM's IDE header.
PS/2 Devices	• A PS/2 mouse and keyboard can both be attached to the 6-pin female mini-DIN connector on the rear I/O panel bracket using a dual PS/2 adapter. **Note**: This connector can support only a PS/2 keyboard without an adapter. • These devices can *only* be attached to the RTM.
Ethernet	The Ethernet connectors on the optional EPC3311-RTM216 are 8-pin RJ-45 connectors.

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3 BIOS configuration

The EPC-3311 uses Phoenix NuBIOS to configure and select various system options. This chapter details the various menus and sub-menus used to configure the system. This chapter is written as though you are setting up each field in sequence and for the first time. Your system may be correctly pre-configured and require very little setup.

When you turn on the power (as described in *Powering on the system* on page 14), the BIOS initializes the hardware, then starts the operating system.

Messages may display during the BIOS initialization sequence. If initialization errors occur, the BIOS may display a message on the appropriate line of the screen and, depending on how your system is configured, either pause or try to continue. For details about these messages, see *Appendix E, Messages*.

During initialization, you can:

- Press the space bar to abbreviate the BIOS extended memory test.
- Press the Escape key to display the Boot-First pop-up menu after initialization completes. You can use this menu to override, for only this boot, the boot options. This menu includes the same options as the Boot menu. For information about the options, see *Boot menu* on page 39.

BIOS setup screens

The EPC-3311's BIOS includes a setup program that displays and modifies the system configuration. The EPC-3311's nonvolatile CMOS RAM stores configuration information, and the BIOS uses it to initialize the EPC-3311 hardware.

You can enter the BIOS Setup only during the system reset process, following a power-up, front panel reset, or equivalent. To enter Setup, press the F2 key when prompted.



To revert to the original BIOS settings, enter the BIOS Setup program, then do one of these:

- Press the F9 key.
- Select Load Setup Defaults from the *Exit menu* on page 41.

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Select from the menus shown in the next table to set up the BIOS.

Menu	Sub-menu
Main Setup menu	IDE Configuration sub-menu Primary Master/Slave sub-menus Console Redirection sub-menu Boot Options sub-menu Keyboard Features sub-menu
Advanced menu	Advanced Chipset Control sub-menu PCI Configuration sub-menu PCI/PNP ISA IRQ Resource Exclusion sub-menu
Boot menu	None
Exit menu	None

Navigation

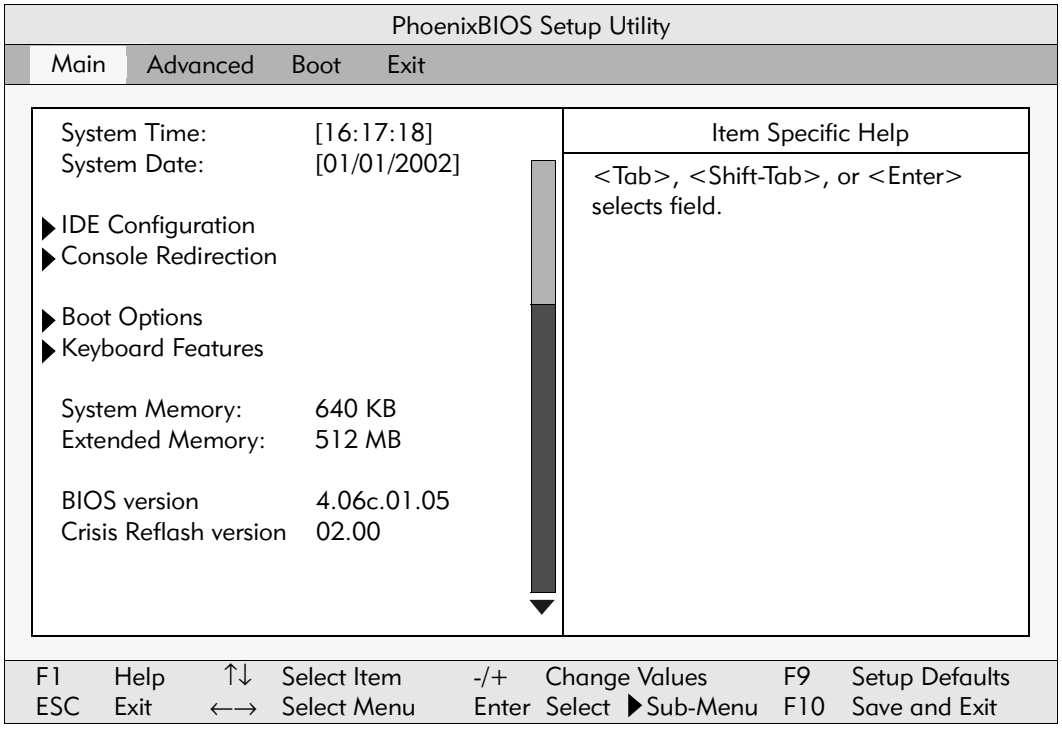
To...	Do...
Display a menu	Press the left or right cursor (arrow) keys and press the Enter key. If you use the arrow keys to leave a menu and then return, your active field is always at the beginning of the menu.
Display a submenu (fields with a triangle at left)	Move the cursor to a field with a triangle and press the Enter key. If you select a sub-menu and then return to the main menu, the active field is that sub-menu heading.
Select a field	Press the up or down cursor (arrow) keys
Select an option	Do one of these: • Press the + and – keys to rotate through available options. • In certain numeric fields, simply enter the desired number.
Select the Exit menu	Press the ESC key. Use the options in this menu to save your changes, reload default BIOS settings, and so on.
Find information about fields in a menu	In addition to the information in this chapter, read the information in the help area on the right side of each screen.

The remainder of this chapter describes the fields in each menu and sub-menu. Additional help information is available in the help area on the Setup screen.

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Main Setup menu

Figure 3-1. BIOS Main Setup menu



The fields in each menu and sub-menu are explained in the next table. You can get additional help in the help area on the right side of each screen.

Field	Description
System Time/System Date	Sets the system time and date. To change these values, go to each field and enter the desired value. Press the tab key to move from hour to minute to second, or from month to day to year. The year field is four digits; there is no default.
IDE Configuration sub-menu	Displays a menu that you use to configure IDE devices. For more information, see *IDE Configuration sub-menu* on page 22.
Console Redirection sub-menu	Displays a menu that you use to redirect console output. For more information, see *Console Redirection sub-menu* on page 28.
Boot Options sub-menu	Displays a menu that you use to specify system behavior during the boot process. For more information, see *Boot Options sub-menu* on page 29.
Keyboard Features sub-menu	Displays a menu that you use to set and change the keyboard settings. For more information, see *Keyboard Features sub-menu* on page 31.
System memory	Displays the amount of conventional memory (below1 MB). This field is not editable; no user interaction is required.
Extended memory	Displays the amount of extended memory (above 1MB). This field is not editable; no user interaction is required.

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Field	Description
BIOS version	Displays the EPC-3311 System BIOS version. This field is not editable; no user interaction is required.
Crisis Reflash version	Displays the EPC-3311 Crisis Reflash program version. If the program is not installed, this field displays "none". This field is not editable; no user interaction is required.

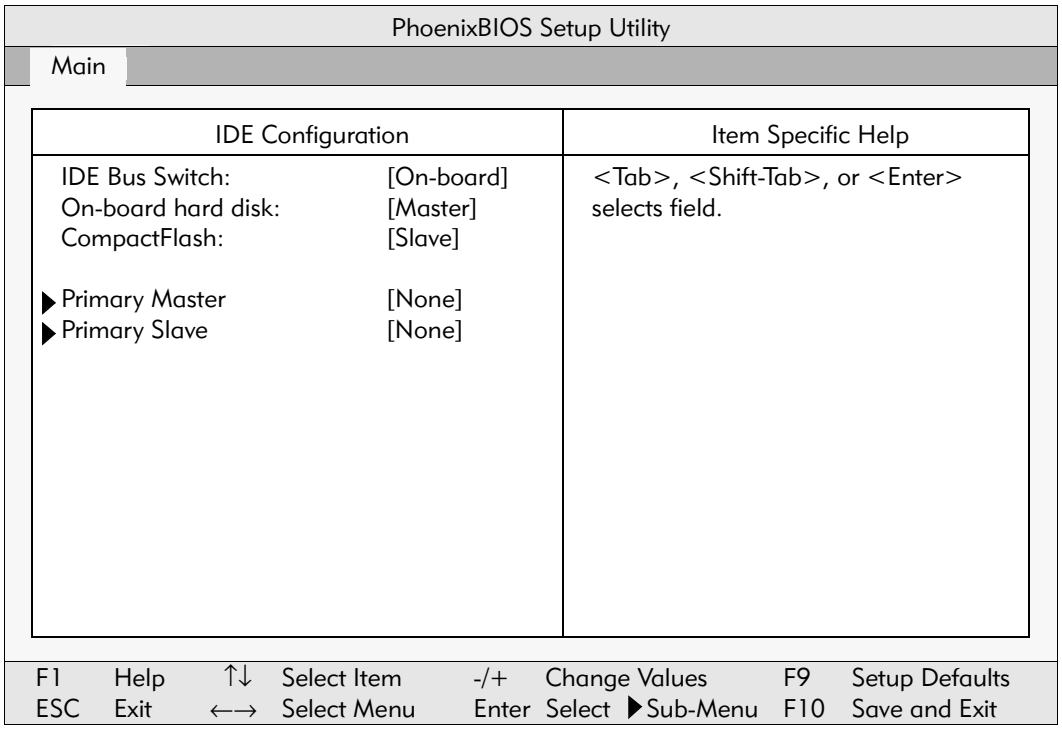
IDE Configuration sub-menu

Options on this menu configure IDE devices.



If you make changes in this menu, do not make changes in the Boot menu. Instead, save your changes and exit the setup program, then boot. If your system doesn't boot from the appropriate drive, then go back to the Setup program and edit only the Boot menu.

Figure 3-2. IDE Configuration sub-menu



Field	Description
IDE Bus Switch	Switches the IDE bus between the on-board IDE header and the RTM IDE header.
IDE Bus Switch (cont'd)	You can select one of these: • **On-board (default)**: Accesses on-board devices. If you select this option, you cannot access an RTM device. • **RTM**: Accesses RTM devices. If you select this option, you cannot access an on-board device.

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On-board hard disk	Determines whether the onboard HDD or 2.5" or 2.5" HDD drive is a Master or Slave device. This option toggles the IDE CSEL (cable select) signal to only the on-board devices. A CompactFlash device always relies on the state of CSEL to tell whether it is a Master or Slave. A 2.5" hard disk must be jumpered for CSEL so that it responds to this option. You can select one of these: • **Master (default)**: Designates the selected drive as ATA device 0. Selecting this value automatically sets the CompactFlash field's value to [Slave]. • **Slave**: Designates the selected drive as ATA device 1. Selecting this value automatically sets the CompactFlash field's value to [Master]. • **Not Installed**: No hard disk exists on the board. With this value, the field is not editable.
CompactFlash	Indicates whether the onboard CompactFlash drive is configured to be the Master or Slave device. This option toggles the IDE CSEL signal to only the on-board devices. A CompactFlash device always relies on the state of CSEL to tell whether it is a Master or Slave. A 2.5" hard disk must be jumpered for CSEL so that it responds to this option. You can select one of these: • **Slave (default)**: Designates the selected drive as ATA device 1. Selecting this value automatically sets the On-board hard disk field's value to [Master]. • **Master**: Designates the selected drive as ATA device 0. Selecting this value automatically sets the On-board hard disk field's value to [Slave].
Primary Master sub-menu	Displays a menu that you use to enter information for the master IDE drive connected to the primary IDE controller. For more information, see *Primary Master/Slave sub-menus* on page 24.
Primary Slave sub-menu	Displays a menu that you use to enter information for the slave IDE drive connected to the primary IDE controller.For more information, see *Primary Master/Slave sub-menus* on page 24.

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Primary Master/Slave sub-menus

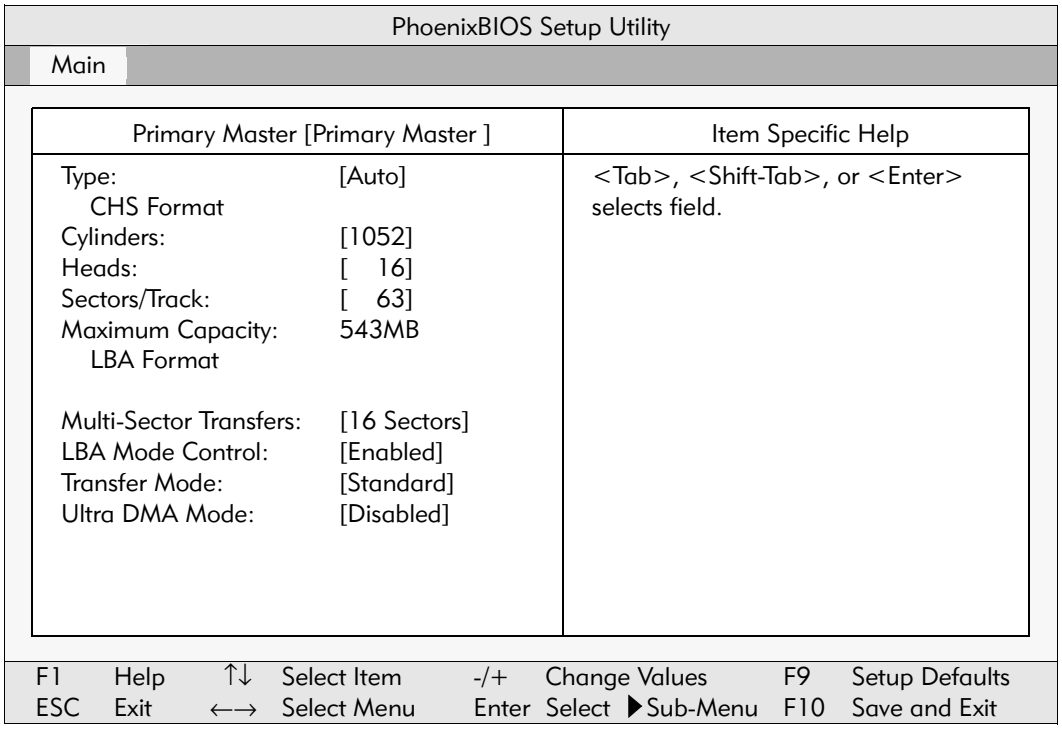
There are two sub-menus for primary hard disk controllers: a master and slave drive menu.

Access this screen to:

- See or reconfigure the detailed characteristics of the primary or secondary IDE device (select the Primary Master or Primary Slave item from the IDE Configuration screen).
- Set up new disks and allow the Setup program to determine the proper settings based on information on the disk. Note that the Setup program can detect these settings only on drives that comply with ATA/ATAPI specifications.
- Set up existing (formatted) disks. Note that you must use the same parameters used when the disk originally was formatted. You must select an option for the Type field, then enter the specific cylinder, head, and sector information listed on the label attached to the drive at the factory.

When finished, press the ESC key to return to the Main Setup menu.

Figure 3-3. Primary Master/Slave sub-menus



Field	Description
Type	Identifies the disk type. You can select one of these: • **Auto (default)**: Select this option when you want the POST to query the hard disk for its parameters whenever the POST runs. RadiSys recommends this option.

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Field	Description
Type (cont'd)	**Note**: If you set a hard disk to "Auto" but no hard disk is actually present, the BIOS queries the (non-existent) hard disk until it times out, slightly increasing the duration of the POST. • **None**: Select this option if yours is not an IDE hard disk drive. • **User**: Select this option if you have an IDE disk but cannot employ the "Autotype" feature. Then manually enter the correct drive values for cylinders, heads, sectors/track, and write precompensation. • **ATAPI Removable**: Select this option if you have a removable disk drive, including a "SuperDrive" (LS-120). • **IDE Removable**: Provides support for high-capacity disks that can be formatted as floppy or hard disks, including compact flash cards and zip drives. • **CD-ROM**: Select this option if you have a CD-ROM drive. **Note**: For disks not supplied, consult the product documentation.
Cylinders	Specifies the number of cylinders on this system. You can specify a number from 1 to 9999. **Note**: This field displays only when the Type field contains a value of [User]. You can edit this field only when the Type field contains a value of [User].
Heads	Specifies the number of heads on this system. You can specify a number from 1 to 16. Press the Space Bar to toggle between valid values. **Note**: This field displays only when the Type field contains a value of [User]. You can edit this field only when the Type field contains a value of [User].
Sectors/Track	Specifies the number of sectors in each track on this system. **Note**: This field displays only when the Type field contains a value of [User]. You can edit this field only when the Type field contains a value of [User].
Maximum Capacity	Displays the amount of disk space available on this system (i.e., the unformatted capacity of the device). **Notes**: • The value for CHS and LBA modes can be different. The difference is due to the way the device is "talked to" in each mode. Having different values is normal and does not indicate a problem with the hardware and/or BIOS. • This field displays only when the Type field contains a value of [User]. You can edit this field only when the Type field contains a value of [User].

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Field	Description
Multi-Sector Transfers	Allows the System BIOS to read ahead by the specified number of sectors during disk access. This has the effect of reading more data at once to reduce the absolute number of discrete disk reads performed by the operating system, which may increase system performance. You can select one of these: • Disabled (default if no drive is installed) • 2 Sectors • 4 Sectors • 8 Sectors • 16 Sectors (default if a drive is installed) **Notes**: • This field displays only when the Type field contains a value of [User], [IDE Removable], [ATAPI Removable], [CD-ROM], or [Auto]. You cannot edit this field if the Type field contains a value of [Auto]. • Autotyping may change this value if the hard disk reports that it supports block accesses.
LBA Mode Control	Determines how the System BIOS references hard disk data. You can use this option only if both the hard disk being configured and the operating system support LBA (Logical Block Addressing). Autotyping may change this value if the hard disk reports that it supports LBA. You can select one of these: • **Disabled (default if no drive is installed)**: Reference hard disk data using the CHS (Cylinders/Heads/Sectors) method. • **Enabled (default if a drive is installed)**: Reference hard disk data as logical blocks. **Note**: This field displays only when the Type field contains a value of [User], [IDE Removable], [ATAPI Removable], [CD-ROM], or [Auto]. You cannot edit this field if the Type field contains a value of [Auto].
Transfer Mode	Selects the mode that the System BIOS uses to access the hard disk. You can select one of these: • Standard (default) • Fast PIO 1 • Fast PIO 2 • Fast PIO 3 • Fast PIO 4 • FPIO 3 / DMA 1 • FPIO 4 / DMA 2 Older hard disks only support “Standard“. Newer hard disks adhering to “Fast ATA“ or “Enhanced IDE“ specifications may support the fast programmed I/O or DMA modes.

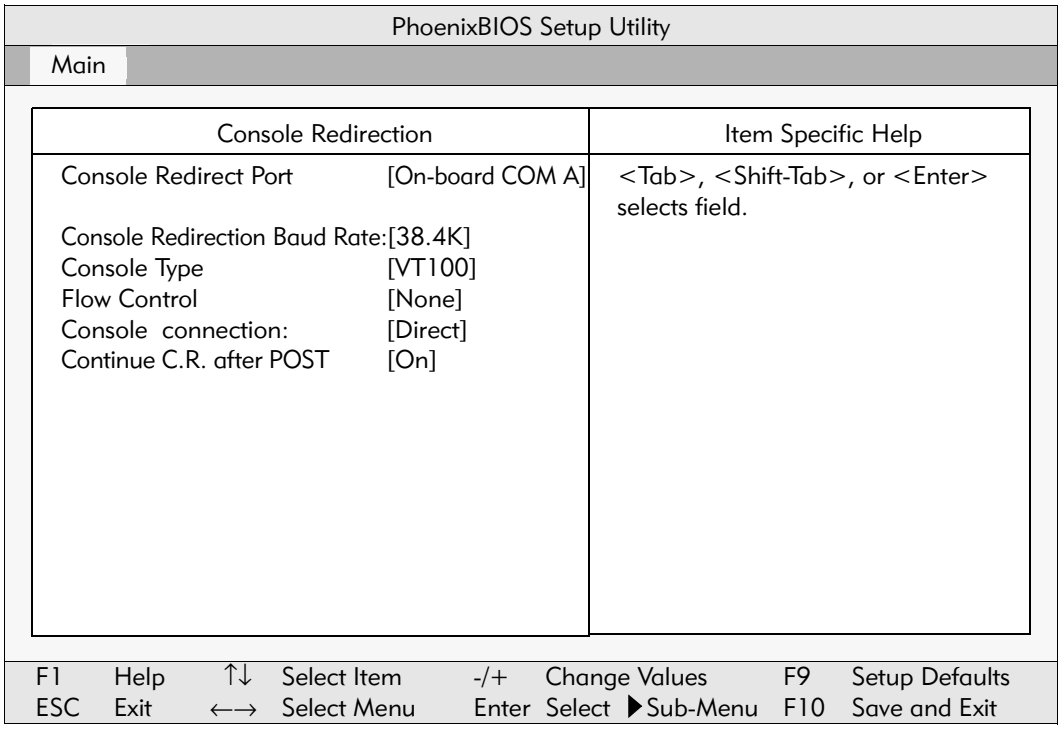
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Field	Description
Transfer Mode (cont'd)	The fast DMA modes take full advantage of the onboard bus mastering hard disk controller and should yield the highest performance when used in conjunction with multitasking operating systems that support it. **Notes**: • This field displays only when the Type field contains a value of [User], [IDE Removable], [ATAPI Removable], [CD-ROM], or [Auto]. You cannot edit this field if the Type field contains a value of [Auto]. • Autotyping may change this value depending on the transfer modes that the hard disk reports it supports.
Ultra DMA Mode	Selects the Ultra DMA Mode that the System BIOS uses to access the hard disk. You can select one of these: • Disabled (default) • Mode 2 • Mode 1 • Mode 0 **Notes**: • This field displays only when the Type field contains a value of [User], [IDE Removable], [ATAPI Removable], [CD-ROM], or [Auto]. You cannot edit this field if the Type field contains a value of [Auto]. • Autotyping derives this value from information reported by the drive. • Most CompactFlash devices do not support this mode. If a CompactFlash is installed, the entire bus transfer rate is reduced to the least common denominator.

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Console Redirection sub-menu

Figure 3-4. Console Redirection sub-menu



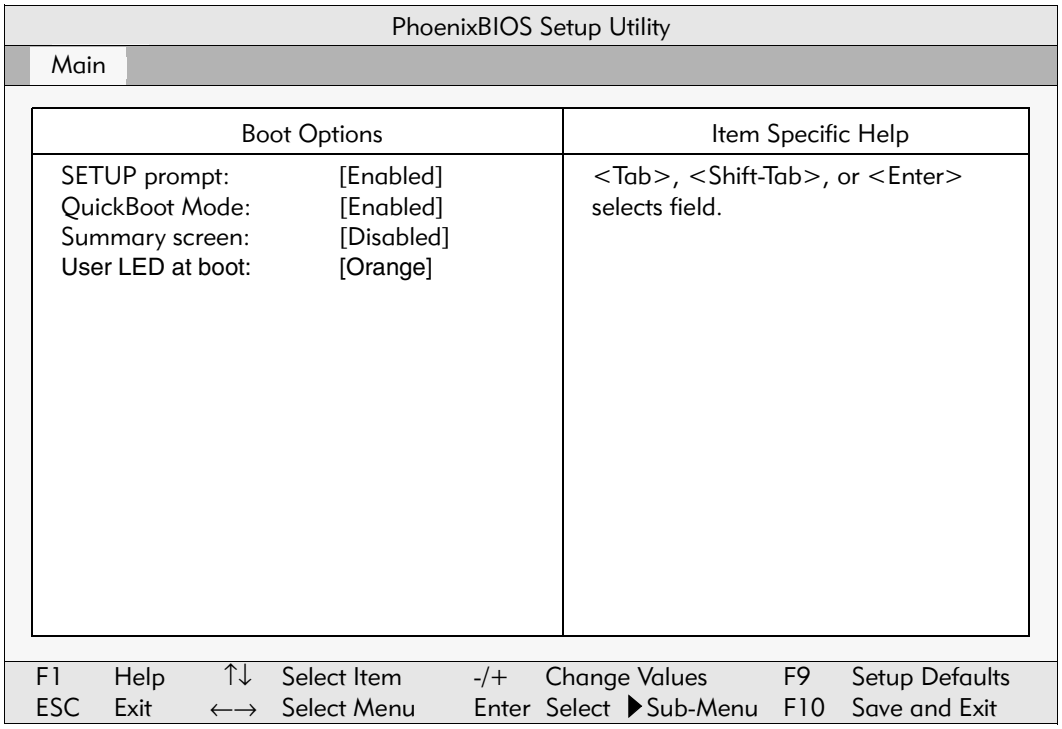
Field	Description
Console Redirect Port	Selects the serial port for console redirection. You can choose one of these: • On-board COM A (default) • Disabled
Console Redirection Baud Rate	Selects the baud rate at which the Console Redirection Port operates. You can select one of the these: • 38.4 K (default) • 19.2 K • 9600 • 4800 • 2400 • 1200 • 600 • 57.6 K • 115.2 K
Console Type	You can select one of these: • VT100 (default) • PC ANSI
Flow Control	You can select one of these: • None (default) • CTS/RTS • XON/XOFF

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Console connection	You can select one of these: • Direct (default) • Via modem
Continue C.R. after POST	Determines the state of console redirection after POST. You can select one of these: • **On (default)**: Leaves console redirection turned on at the end of POST. • **Off**: Turns off console redirection at the end of POST. Select this option if your system runs a Unix-like OS, otherwise the OS's redirection driver may not work.

Boot Options sub-menu

Figure 3-5. Boot Options sub-menu



Field	Description
SETUP prompt	You can select one of these: • **Enabled (default)**: The BIOS displays the "Press <F2> to enter SETUP" prompt. • **Disabled**: The BIOS does not display the "Press <F2> to enter SETUP" prompt. Although the message does not display, you can still access the Setup program by pressing the F2 key.

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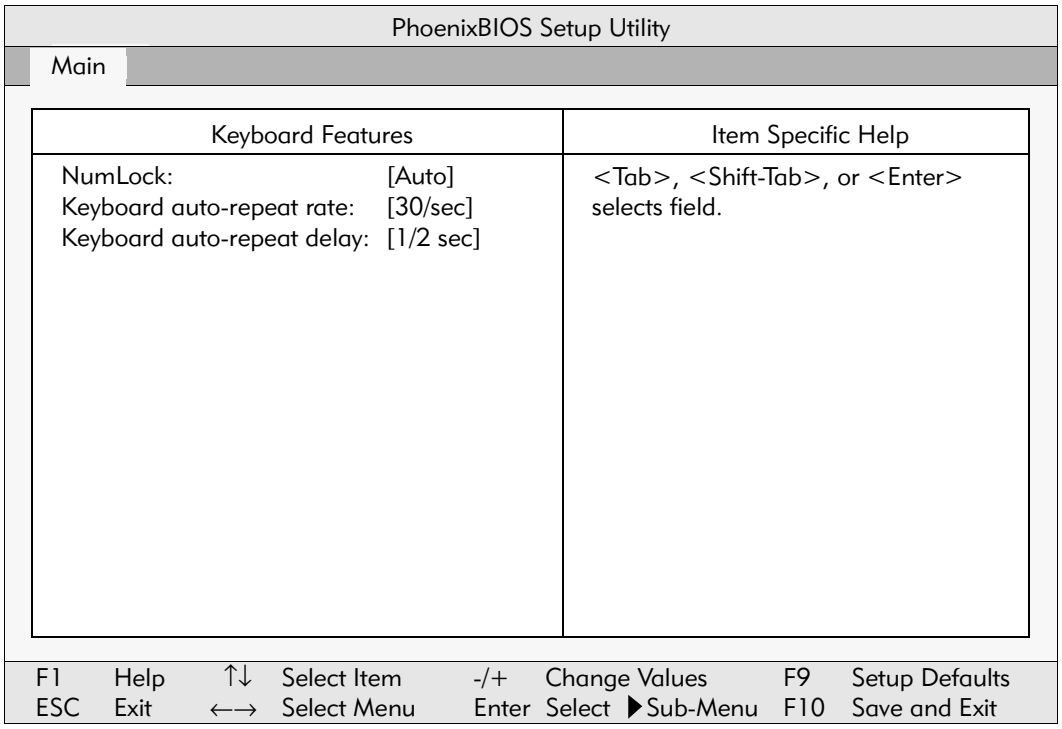
Field	Description
QuickBoot Mode	You can select one of these: • **Enabled (default)**: Allows the SBC to skip certain tests while booting. This decreases the time needed to boot the SBC. • **Disabled**: Runs all tests during boot.
Summary screens	Determines whether the system configuration displays prior to loading the operating system. You can select one of these: • **Disabled (default)**: Does not display a summary of the system configuration before the operating system starts to load. Selecting this option speeds up the boot process. • **Enabled**: Displays a summary of the system configuration before the operating system starts to load.
User LED at boot	Determines the USER LED color at the end of BIOS POST and the start of bootload: • **Orange (default)**: Sets the USER LED to orange. • **Green**: Sets the USER LED to green.

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Keyboard Features sub-menu

Options on this menu set and change keyboard settings.

Figure 3-6. Keyboard Features sub-menu



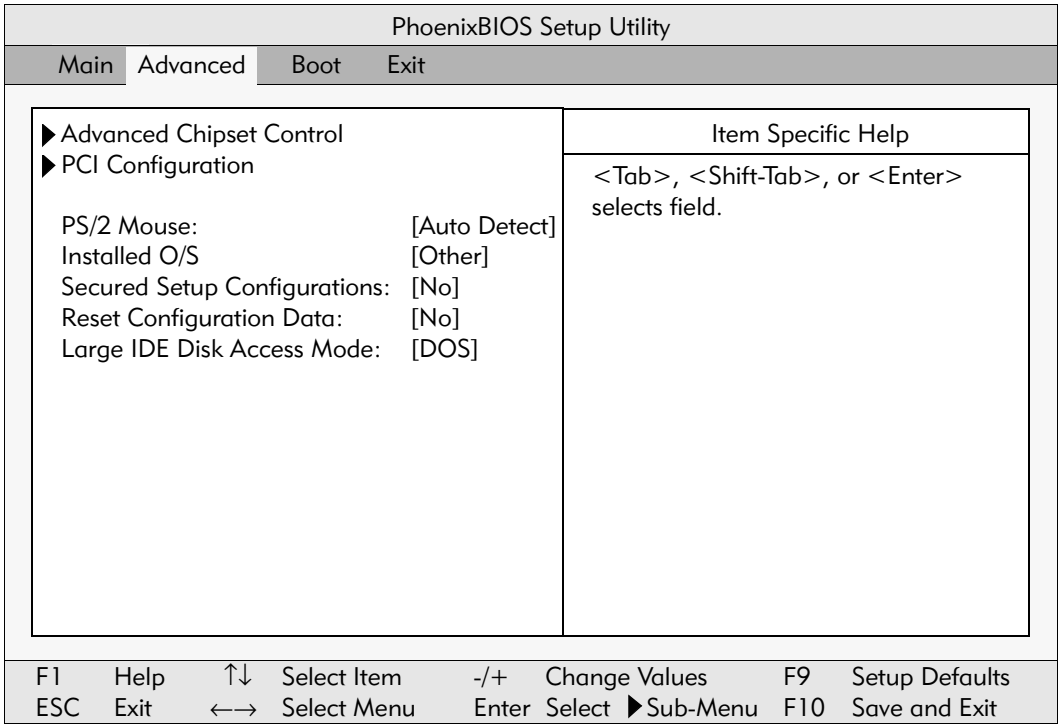
Field	Description
NumLock	Determines whether the keyboard numbers (the NumLock feature) operates. You can select one of these: • **Auto (default)** • **Off**: Disengages the NumLock key at boot. • **On**: Engages the NumLock key at boot.
Keyboard Auto-repeat Rate	Determines the number of keystrokes entered per second holding a key down on the keyboard. You can select one of these: • 30/sec (default) • 2/sec • 6/sec • 10/sec • 13.3/sec • 18.5/sec • 21.8/sec • 26.7/sec
Keyboard Auto-repeat Delay	Sets the delay between when a key is pressed and when the auto-repeat feature begins. You can select one of these: • ½ sec (default) • ¼ sec • 1 sec • ¾ sec

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Advanced menu

This menu contains settings for integrated peripherals, memory shadow, cache, and large disk access mode. You access this menu by selecting Advanced from the Main BIOS Setup menu.

Figure 3-7. Advanced menu



Field	Description
Advanced Chipset Control	Displays a menu that you use for advanced chipset control. For more information, see *Advanced Chipset Control sub-menu* on page 34.
PCI Configuration sub-menu	Displays a menu that you use to enter configuration information for PCI devices. For more information, see *PCI Configuration sub-menu* on page 36.
PS/2 Mouse	Determines whether a PS/2 mouse functions on this system. You can select one of these: • **Auto Detect (default)**: Allows the system BIOS to determine whether a PS/2 mouse exists on this system and enable it, if present. • **Enabled**: Sets the system to use a PS/2 mouse, if installed. • **Disabled**: Prevents any installed PS/2 mouse from functioning and frees IRQ 12.

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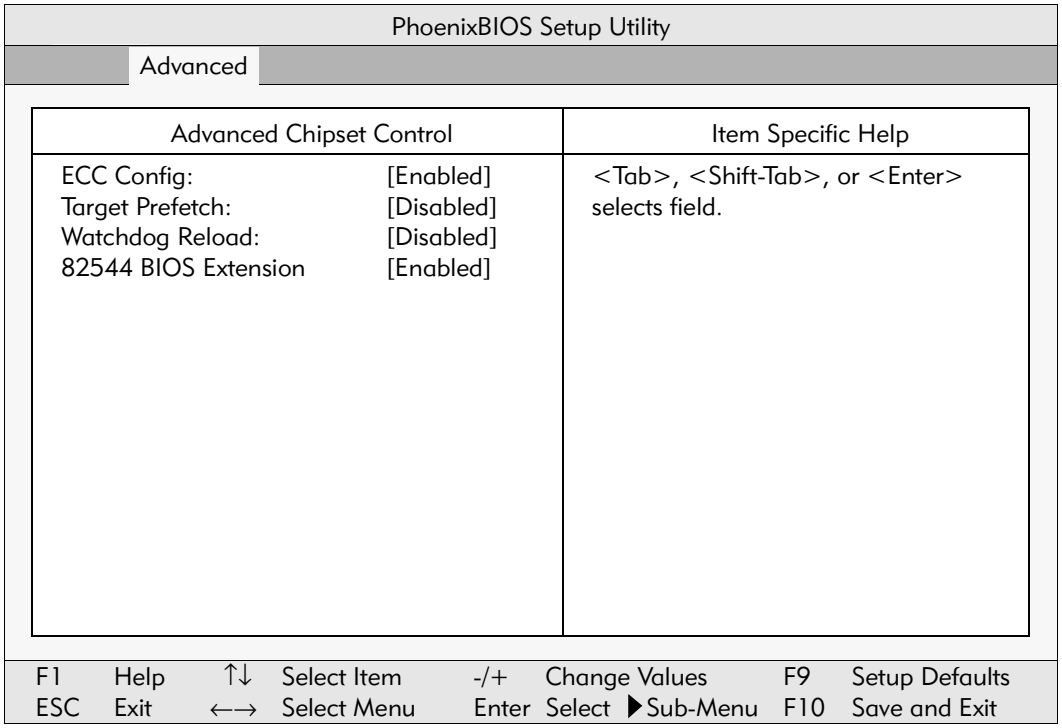
Field	Description
Installed OS	Identifies the OS you plan to use on this system. You can select one of these: • **Other (default)**: Select this option when you plan to use an OS other than Windows 95, Windows 98 or Windows 2000. • **Win95**: Select this option when you plan to use a Windows 95 or newer OS. Selecting this option informs the BIOS that this system supports Plug and Play. **Note**: Setting this to the incorrect value may produce unexpected results.
Secured Setup Configurations	You can select one of these: • **Yes (default)**: Ignores any Plug-n-Play BIOS calls requesting change to an onboard resource. • **No**:
Reset Configuration Data	Determines whether to clear the Extended System Configuration Data (ESCD) block that resides in the Flash chip. You can select one of these: • **No (default)**: Does not clear the ESCD block. • **Yes**: Clears the ESCD block. This option automatically resets to "No" after the block is cleared.
Large IDE Disk Access Mode	Specifies whether MS-DOS systems can use hard disks up to 8GB (1024C x 255H x 63S) without special drivers or LBA. If the drive fails while installing new software, change this setting and try again. You can select one of these: • **DOS (default)**: Causes the System BIOS to perform cylinder/head translation during boot, if the drive is configured in Setup to have more than 1024 cylinders. Select this option if your system uses a drive larger than 528 MB and runs DOS or MS-DOS. • **Other**: The BIOS bootloader and runtime API does not perform CHS translation. Select this option if your system uses a drive larger than 528 MB and runs Novell Netware or a Unix implementation.

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Advanced Chipset Control sub-menu

Use the options in this sub-menu to configure various chipset specific features.

Figure 3-8. Advanced Chipset Control sub-menu



Field	Description
ECC Config	Determines the state of the RadiSys 82600's ECC circuitry. You can select one of these: • **Enabled (default)**: The 82600 corrects and writes back single-bit ECC errors. The generation of ~BSERR on multiple-bit errors and NMI on single-bit errors is a feature of the 82600, but is left disabled by the BIOS. • **Disabled**: The 82600 does not correct or write back single-bit ECC errors.
Target Prefetch	Controls the RadiSys 82600 Target Prefetch bits, which include bits [1:0] of *MLPC, Miscellaneous LPCI Control,* the local PCI header register: *A=0.4C, R=00.* You can select one of these: • **Disabled (default)**: 82600 immediately invalidates an read data prefetched and not used by an LPCI access. Select this option when there are lots of masters reading small amounts of data randomly.

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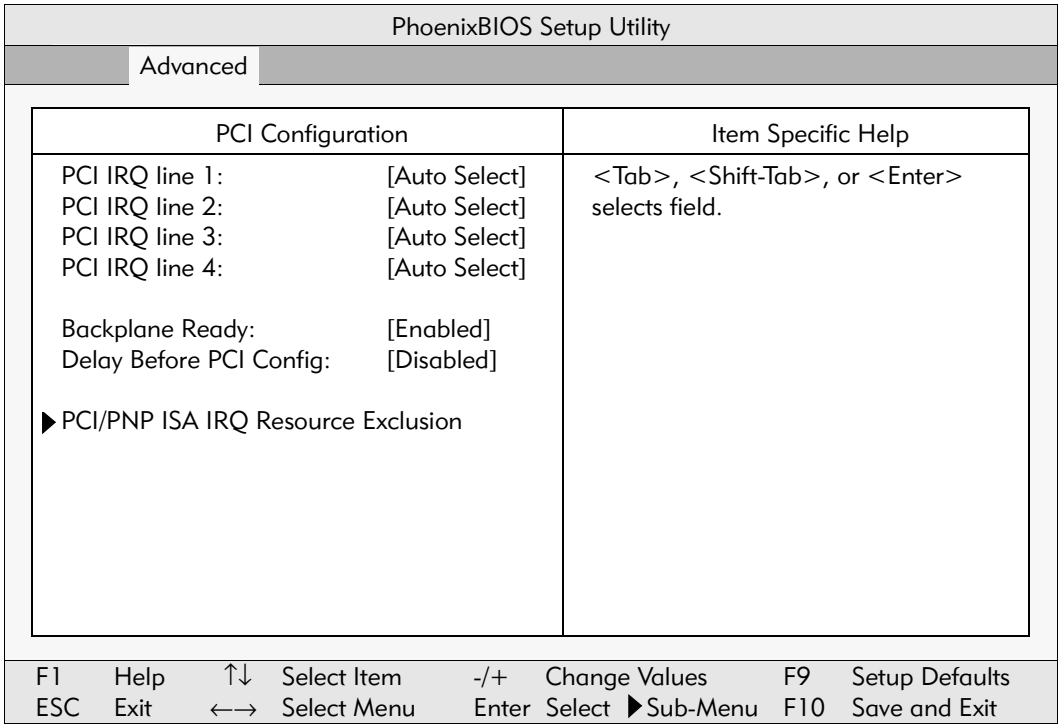
Field	Description
Target Prefetch (cont'd)	• **10b**: The 82600 retains prefetched data for all read commands until invalidated by a host bus write or consumed by an LPCI memory operation. Select this option when your system moves large volumes of data. This is the most efficient option for most situations. • **11b**: The 82600 retains prefetch data for read-multiple and read-line commands, but immediately invalidates bytes not consumed by an LPCI "memory read" command. Select this option when your system moves large volumes of data and when the masters utilize the read-line capabiliity.
Watchdog Reload	Controls the RadiSys 82600 watchdog timer. At boot time, the BIOS sets the *DGCTRL, Watchdog Control/Status Register: A=PWRBASE+1A, R=00* to the value of 0x3D, which causes a reload on the 82600 LDEV0 or LDEV1 (local device decodes) or 82600 assertion of ~BDEVSEL or ~BFRAME. You can select one of these: • Disabled (default) • 2048 seconds • 1024 seconds • 1024 seconds • 256 seconds • 128 seconds • 64 seconds • 32 seconds • 16 seconds • 8 seconds • 2 seconds • 512 seconds • 128 milliseconds • 32 milliseconds • 8 milliseconds • 2 milliseconds For detailed information, see the *82600 High Integegration Dual PCI System Controller Data Book*.
82544 BIOS Extension	Valid values include: • **Enabled (default)**: The MBA UNDI network boot BIOS extension is enabled and available. • **Disabled**: The MBA UNDI BIOS extension is not available and does not occupy BIOS extension space between 0xC8000 and 0xE0000.

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PCI Configuration sub-menu

Use the options in this sub-menu for PCI.

Figure 3-9. PCI Configuration sub-menu



Field	Description
PCI Interrupt Selection	Controls the 82600 assignments of its PCI IRQ (PIRQ) lines 1, 2, 3, and 4 to the legacy IRQs of its interrupt controller. You can select one of these: • **Auto Select (default)**: The BIOS selects from a pool of unassigned legacy IRQs. • **Disabled**: Does not assign a PIRQ line to an IRQ. • **3**, **4**, **5**, **7**, **9**, **10**, **11**, **12**, **14**, or **15**: Assigns a PIRQ line to the IRQ you specify. Assigning a PIRQ line to an occuped legacy IRQ masks that legacy IRQ.

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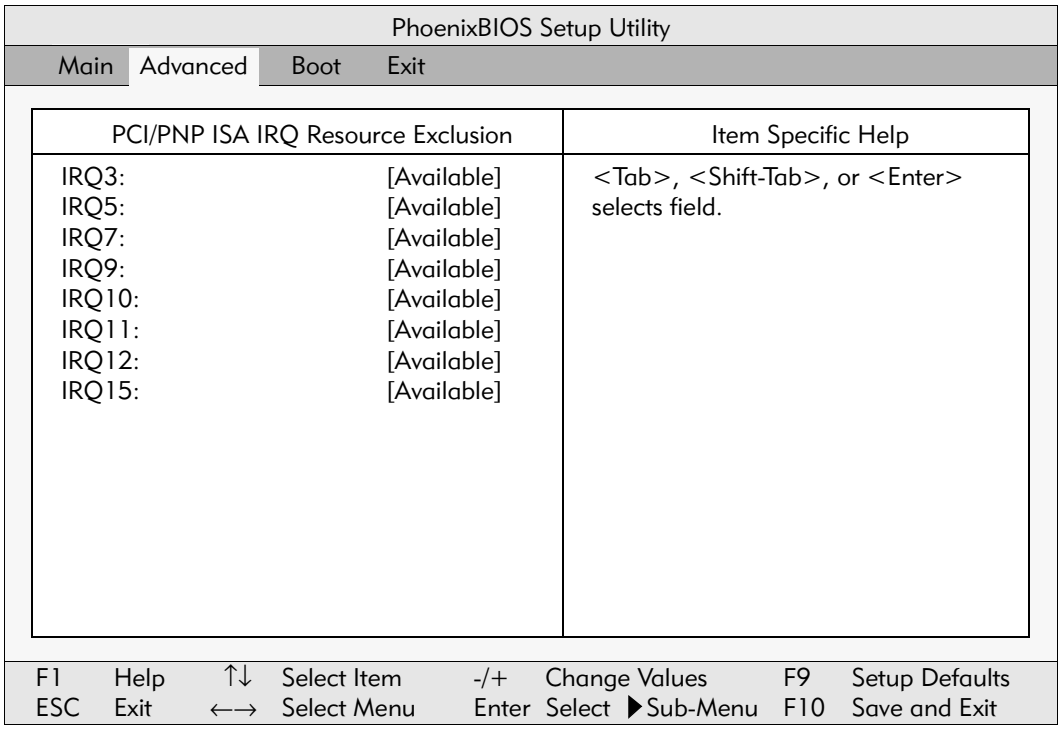
Field	Description
Backplane Ready	Determines whether resources are exported to the backplane. This is accomplished via the 82600 BPCI Ready bit. You can select one of these: • **Enabled (default)**: Does not export resources to the CompactPCI (BPCI) bus. The BIOS sets the 82600 BPCI Ready bit. • Select this option if you don't plan to export board resources to the BPCI.**Disabled**: The BIOS on the System board waits before allocating CompactPCI resources: memory, I/O, and PCI interrupt. The BIOS on the Peripheral board does not set the 82600 BPCI Ready bit; application software must configure the 82600 BPCI and set the BPCI Ready bit. Select this option for a Slave if you plan to export PCI resources (on-board SDRAM) to the BPCI.
Delay Before PCI Config	Determines how many seconds to wait after booting for the card to set up PCI configuration registers. This option appears only when the SBC is in a System (Master) slot. **Note**: Some add-in cards require more time after boot than others for PCI configuration registers to set up. You can select one of these: • **Disabled (default)**: You may want to select this option for EPC-3311s installed in Peripheral slots rather than enable this item on the System Slot board. • **2**, **4**, or **8 seconds**: Waits the specified number of seconds before enumerating the CompactPCI bus and assigning resources. If a PCI device does not work after system boot, try this option.
PCI/PNP ISA IRQ Resource Exclusion sub-menu	Displays a menu that you use to control the exclusion of PCI and ISA interrupt resources. See *"PCI/PNP ISA IRQ Resource Exclusion sub-menu"* on page 38.

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PCI/PNP ISA IRQ Resource Exclusion sub-menu

The PCI/PNP ISA IRQ Resource Exclusion Sub-Menu controls the exclusion of PCI and ISA interrupt regions.

Figure 3-10. PCI/PNP ISA IRQ Resource Exclusion sub-menu



Field	Description
Interrupts	Determines the use of each interrupt. You can select one of these: • **Available (default)**: Makes the specified ISA IRQs available for PCI use. • **Reserved**: Reserves the interrupt for ISA use.

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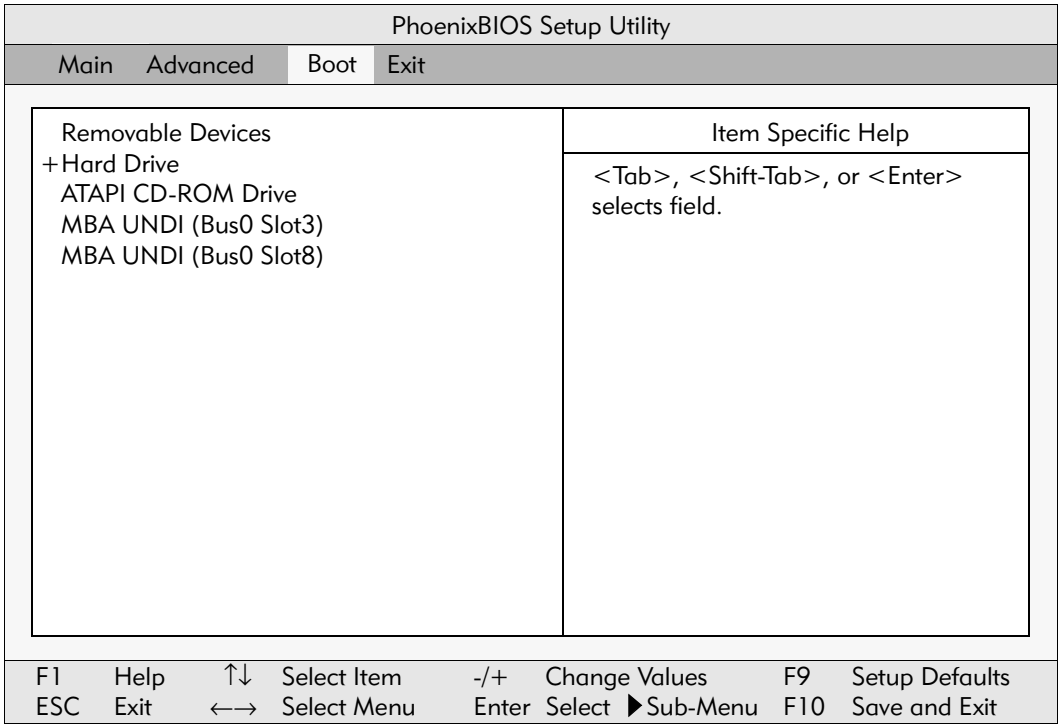
Boot menu

The Boot menu controls the order of the available boot devices. Items that display on this screen depend on installed hardware and user selections.

If you make changes in this menu, do not make changes in the IDE Configuration sub-menu. Instead, save your changes and exit the setup program, then boot. If your system doesn't boot from the appropriate drive, then go back to the Setup program and edit only the IDE Configuration sub-menu.

Pressing the Escape key during initialization displays the Boot-First pop-up menu after initialization completes. You can use this menu to override, for only this boot, the boot options. The Boot-First pop-up menu includes the same options as the Boot menu.

Figure 3-11. Boot menu



Navigation

To...	Do...
Move an item to a higher level in the list	Highlight the item and then press the + (plus) key.
Move an item to a lower level in the list	Highlight the item and then press the – (minus) key.
List all devices of a specified type available on the system	Highlight the device type and press the Enter key. A + (plus) symbol indicates devices that have sub-items.

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To...	Do...
List all boot devices under their respective device types	Press the Ctrl and Enter keys at the same time.
Disable a device or group of devices and prevent it from booting	Highlight the item and press the Shift and "I" keys. A "!" (exclamation mark) displays, indicating that the item will not boot.
Find information about fields in a menu	In addition to the information in this chapter, read the information in the help area on the right side of each screen.

Options

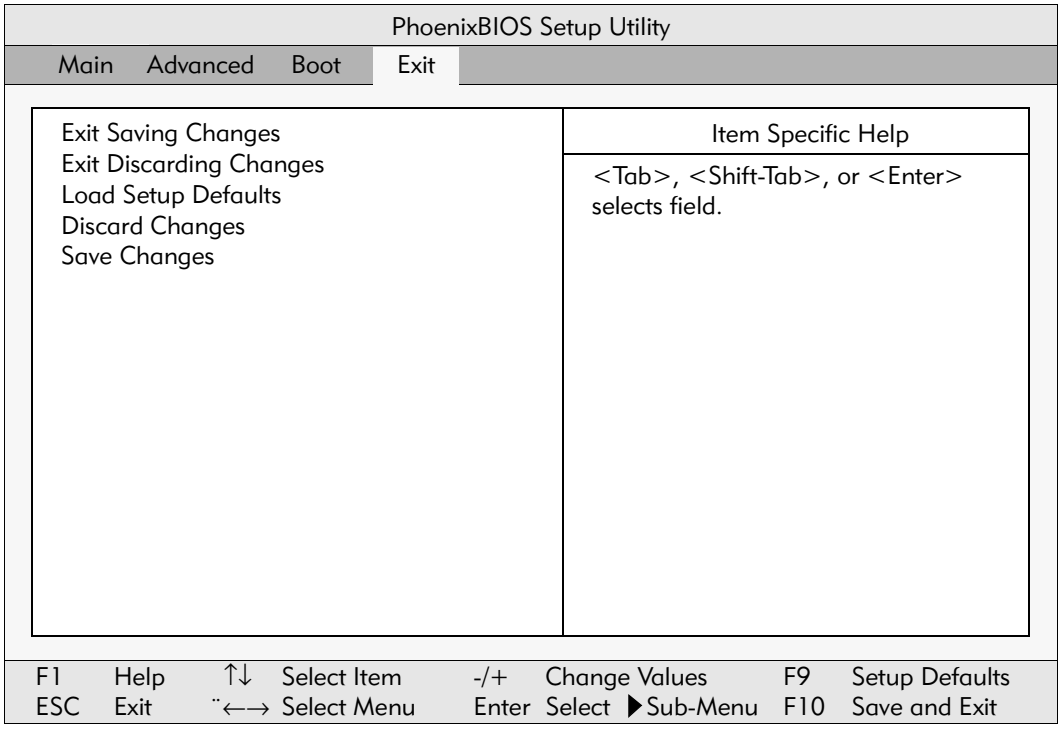
Field	Description
Removable Devices	Because the EPC-3311 does not support legacy floppy drives, this option has no effect.
Hard Drive	Specifies the order in which POST installs devices, assigning device number 80h to the first device, 81h to the second, and so on. The BIOS initially orders the list in the order it first encounters devices during POST. Phoenix MultiBoot III boots only from the first item in the list. **Note**: CompactFlash and other IDE Removable devices are "sticky". That is, if the device is originally at the top of the list, and the device is physically removed, the next device in the Hard Drive list boots. But if the removable device is replaced, it is promoted back to the top of the Hard Drive list
ATAPI CD-ROM Drive	Displays even when no ATAPI CD-ROM Drive is attached.
MBA UNDI	Determines which Ethernet to use when booting from the network. You can select one of these: • **Bus0 Slot 8**: Ethernet 1. • **Bus 0 Slot 3**: Ethernet 2. If you select either or both of these options, the MBA configuration program runs after you exit the BIOS setup program. For more information about this program, see *Chapter 4, MBA configuration*.

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Exit menu

Options in this menu save and exit, or abandon your changes and exit to the system.

Figure 3-12. Exit menu



Field	Description
Exit Saving Changes	Saves the values you just entered and exits to load the operating system. The system boots with the new values.
Exit Discarding Changes	Discards the changes you just made and reverts to the BIOS as it was before you entered the BIOS Setup program. The system boots with the old values.
Load Setup Defaults	Resets the BIOS values to the original, default values set at the factory, before any suppliers or other end users made changes.
Discard Changes	Loads the system with the values that existed before this editing session started. You do not exit.
Save Changes	Saves the edits you made during this session but does not exit.

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4 MBA configuration

The EPC-3311 includes an emBoot†, Inc. MBA (Managed PC Boot Agent), a client-based firmware which allows the EPC-3311 to perform network booting. MBA supports the PXE (Preboot Execution Environment) network boot protocol and additional boot protocols such as BOOTP, DHCP, RPL, and NCP/IPX(Netware†). It is an integrated component of the EPC-3311 Flash EEPROM.

Requirements

To implement network booting with MBA you need a network boot server or third-party client management. The MBA is a client-based component; a network boot also requires server-based software. The server system that hosts this software is typically called the *boot server.*

When configured to use the PXE protocol, MBA operates with any PXE-compliant boot server software. Many third-party client management products use network booting to perform the client management tasks and include the PXE-compliant boot server software. Examples of such products include:

- Microsoft† Windows† RIS (Remote Installation Services)
- Linux† PXE Server
- ON Command† CCM from On Technology†
- CA-Unicenter† TNG
- Symantec† Ghost† Enterprise
- Altiris† Express/Client Management Suite
- LANClient Control Manager† (LCCM) from IBM
- BXP from VenturCom Inc.
- Rembo from Rembo Technology
- HP Openview

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MBA features:

- **PXE compliant:** The PXE specification (part of the Intel Wired for Management initiative) has become the standard definition of protocols and interfaces required for network booting. PXE operation is the MBA's default mode.
- **Additional boot protocols:** In addition to PXE, MBA also supports multiple boot protocols and network environments such as traditional TCP/IP, NetWare, and RPL. It also supports protocols including DHCP, BOOTP, NCP/IPX (802.2, 802.3, Ethernet II).

MBA setup screens

When MBA UNDI is first in the System BIOS Setup program's boot order (see *Boot Options sub-menu* on page 29), MBA transfers boot files from the network server, and then transfers control to these boot files.

If MBA UNDI is not first in the boot order, it executes only if the previous devices in the boot order fail to boot.

At this point, if MBA attempts to perform a network boot and fails, your server may not be set up to support network booting. See the appropriate chapter of this guide for your network protocol.

When you turn on the EPC-3311, the following occurs:

- The EPC-3311 System BIOS performs its usual initial tests and setup, such as a memory test.
- The MBA displays this configuration message.

```
Initializing MBA. Press Ctrl+Alt+B to configure…
```



RadiSys recommends using a PS/2 keyboard. Terminal emulators used with Console Redirection may not support Control and Alt key combinations.

If you press the Control, Alt, and B keys while the message displays, the MBA-based Configuration Screen displays, and you can view or change various MBA options, including the option to disable the display of this configuration message.

Boot failure

If network booting does not succeed (for example the server is down), MBA's behavior depends on the current settings of the Boot Failure Prompt and Boot Failure options:

Setting	Action
Wait for Key	Displays a message that informs you of the next action (i.e. either reboot or continue), prompts you to press a key, and waits for you to press a key.
Wait for Timeout	MBA waits for three seconds, and then performs the action.

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The action MBA takes is based on the current setting of the Boot Failure option:

Setting	Action
Reboot	Reboots the EPC-3311.
Next Boot Device	Reboots the EPC-3311 from the next boot device in the System BIOS boot order list.



RadiSys recommends using a PS/2 keyboard. Terminal emulators used with Console Redirection may not support Control and Alt key combinations.

Key combination	Description
v or Ctrl + Alt	Displays verbose status information. During a normal boot, MBA displays minimal information on the screen. To see more status information during the boot process, set MBA to verbose mode by pressing and holding the v key or Ctrl+Alt before MBA begins to execute. On the EPC-3311 you can do this during the long pause that follows the memory test. Release the key(s) once MBA has started to execute
Shift + Shift	Displays MBA information. To display MBA information such as internal version numbers and settings, press and hold both Shift keys simultaneously before MBA begins to execute. On the EPC-3311 you can do this during the long pause that follows the memory test. MBA displays an information screen.

Navigation

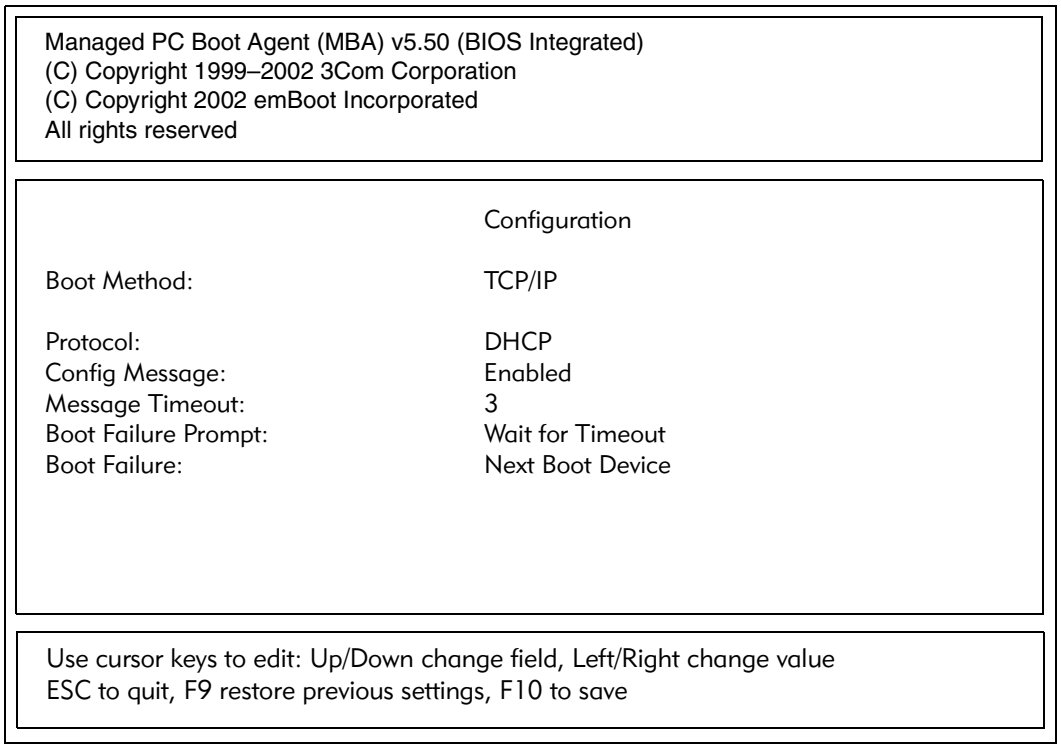
To...	Do...
Select a field	Press the up or down cursor (arrow) keys.
Select a value	Press the left or right cursor (arrow) keys.
Leave without saving	Press the ESC key.
Save changes and exit	Press the F10 key.
Restore previous settings	Press the F9 key.

The remainder of this chapter describes the MBA fields.

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MBA configuration options

Figure 4-1. MBA menu



Field	Description
Boot Method	Specifies the boot method. Valid values include: • TCP/IP • Netware • RPL • PXE
Protocol	Specifies the protocol for TCP/IP or NetWare boot method. Valid values include: • **DHCP (default)**: DHCP, BOOTP. • **NetWare**: 802.2, 802.3, Ethernet II. **Note**: This field displays only when Boot Method has a value of TCP/IP or Netware.
Config Menu	Determines whether the user can access the Configuration Screen built into the MBA ROM. You can select one of these: • **Enabled (default)**: The Configuration Message displays. • **Disabled**: The Configuration Message does not display.

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Field	Description
Config Message	Determines whether the MBA displays a message that tells the user which keys to press to access the MBA Configuration Screen. Valid values include: • **Enabled (default)**: Displays this message: `Press Ctrl+Alt+B to configure…` • **Disabled**: Hides the message. If you choose this option, users can still access the MBA Configuration Screen. Choose this option to prevent users from changing MBA options, possibly making MBA function incorrectly in your environment.
Message Timeout	Specifies the number of seconds that prompt messages display and wait for user input. Prompt messages include messages such as the Configuration Message, Local and Network Boot Messages, and Boot Failure Prompt. Changed values take affect the next time the PC boots. You can select one of these: • **3 (default)**: Displays prompt messages for three seconds. • **6**: Displays prompt messages for six seconds. • **9**: Displays prompt messages for nine seconds. • **Forever**: Applies only to Local and Network Boot Messages. If you select this option, other prompt messages display for three seconds.
Boot Failure Prompt	Determines what happens when a network boot does not complete. After completing the specified action, MBA performs as specified by the Boot Failure option. You can select one of these: • **Wait for Timeout (default)**: Wait for three seconds and then continue. • **Wait for Key**: Display a message and then wait for the user to press a key before continuing.
Boot Failure	Determines what happens when a network boot does not complete. You can select one of these: • **Next Boot Device (default):** Boot the PC from the next boot device. The next boot device is the next device in the System BIOS Setup program's boot order list. • **Reboot: R**eboots the PC.
TFTP Secure Mode	Specifies whether to use TFTP's secure mode. Valid values include: • **Enabled (default)**: Uses the secure mode feature of TFTP, sending only the filename to the TFTP Service. • **Disabled:** Does not use the secure mode feature of TFTP.

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5 Theory of operation

The EPC-3311, a 6U single-slot board, plugs into either a system or peripheral slot of a CompactPCI backplane. It can be used with either a 2.16 compliant or a non-2.16 backplane.

When reading this file online, you can immediately view information about any EPC-3311 topic by placing the mouse cursor over the topic name and clicking:

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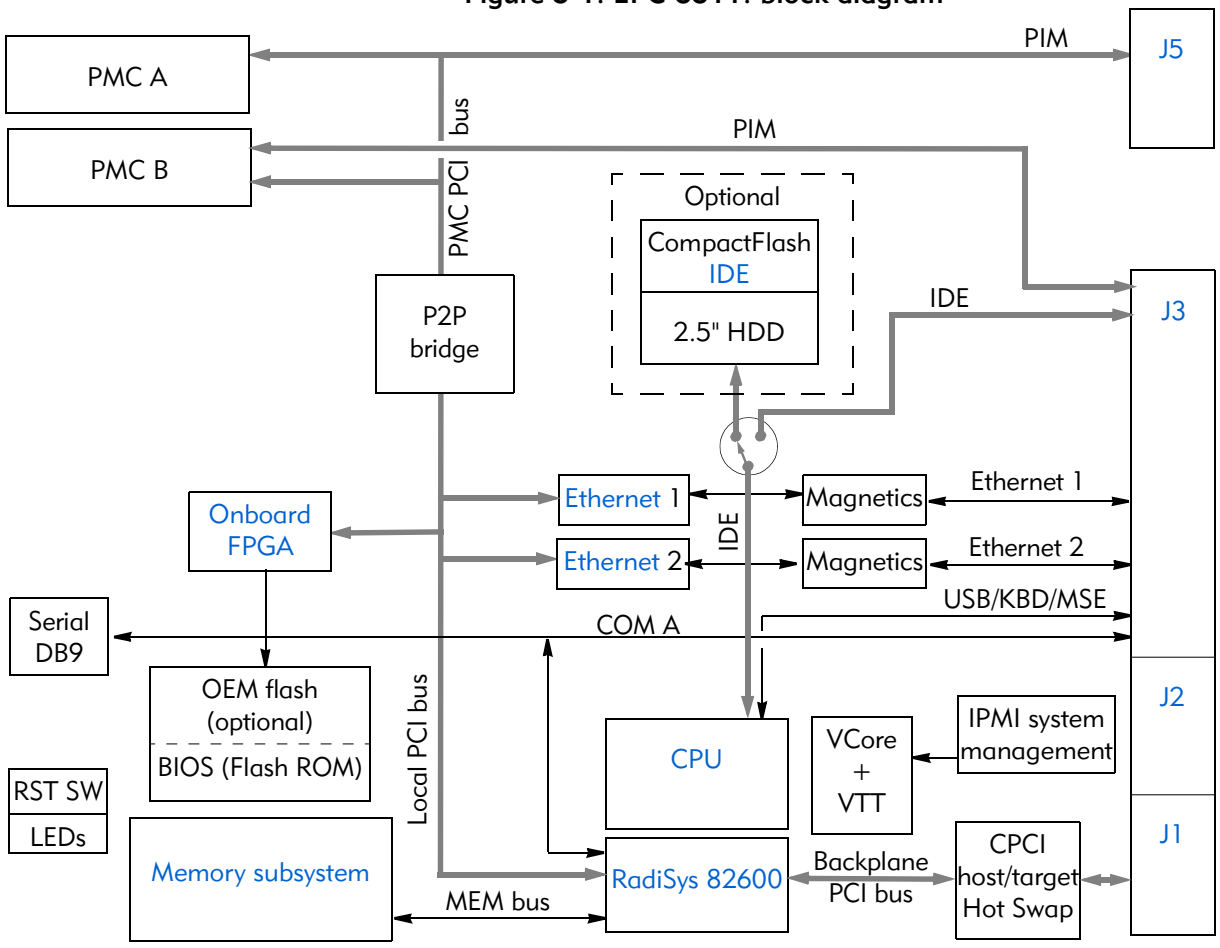
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Organization

Block diagram

The next figure shows the division and interconnection of EPC-3311 functions. The following sections provide detailed descriptions of these items.

Figure 5-1. EPC-3311: block diagram



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Features

CPU

The foundation of the EPC-3311's design consists of the Mobile Intel Pentium III Processor-M (Tualatin) with the RadiSys 82600 system controller and the connection to CompactPCI J1, J2, and J3.

RadiSys 82600

The RadiSys 82600 high integration dual PCI system controller functions as a combination north bridge, a super I/O, and a PCI-CompactPCI bridge.

The 82600 does not support the LOCK or PERR functions on the local PCI or the CompactPCI buses.

Power-up configuration

The following configuration options of the 82600 are determined during a power reset using pull-up or pull-down resistors on memory address lines.

ADDR0: Selection of general purpose I/O pins or the EIDE bus.

- 0 EIDE (Default)
- 1 General-purpose I/O, DIO[0..15]

ADDR1: Selection of general-purpose I/O pins or bus arbitration signals ~BREQ[6:3] and ~BGNT[6:3].

- 0 General-purpose I/O (Default)
- 1 Arbitration signals ~BREQ[6:3], ~BGNT[6:3].

ADDR2 and ADDR5:

ADDR2	ADDR5	Mode
0	0	System slot with central resource and arbiter enabled.
1	0	Peripheral slot (no central resource and no arbiter)

ADDR3: Determines the status of the Real Time Clock.

- 0 Enable (Default).
- 1 Disable.

ADDR4: Determines the location of the boot flash

- 0 Boot Flash on the SDRAM bus (Default).
- 1 Boot Flash on PCI bus.

ADDR6: Selection of either SDRAM ECC function or COM2

- 0 Memory ECC enabled; COM2 is disabled (Default).
- 1 COM2 is enabled; Memory ECC disabled.

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ADDR7: Selection of general-purpose I/O pins or COM1 function.

0 COM1 (Default).

1 General-purpose I/O, DIO [25..31]

ADDR8: Sets the I/O Queue depth.

0 Queue depth is 8 (default).

1 Queue depth is 1.

ADDR10 and ADDR11:
Combination determines the PSB frequency:

ADDR10	ADDR11	Mode
0	0	NA
1	0	133 MHz (Default)
0	1	66 MHz (not supported for CPU Board)
1	1	100 MHz (not supported for CPU Board)

Host bridge

The 82600 connects directly to the AGTL CPU local bus. There are CPU bus termination resistors are on the processor die. The bus length is minimized to obviate the need for termination resistors at the 82600. The 82600 segregates bus transactions as follows:

- 36 address-bit references.
- SDRAM references.
- LPCI bus cycles.
- BPCI bus cycles.
- Internal register.
- Special cycle (includes halt/shutdown, cache flush, etc.).
- Interrupt acknowledge.

The CPU board has two sets of PCI interrupts, one for the LPCI and one for the BPCI.

Memory subsystem

The CPU board supports either 512 MB or 1GB of 133 MHz ECC custom memory modules on the main board. This discrete module connects through a set of low-profile connectors (under the PMC B site) and provides all SDRAM to the CPU board.

The custom memory module provides an SPD memory with the memory configuration data. The SPD PROM connects via the SMBus serial interface on the 82600. The SPD is queried by the BIOS during POST to determine the computer's memory configuration. The SPD in the system is assigned A0h address.

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PCI interrupts

The 82600 has two sets of PCI interrupts: LPIRQ for the local bus and BPIRQ for the backplane/cPCI bus.

Interrupts from both PCI busses can route to the PCI devices through the use of the LPIRQ and BPIRQ Routing Control registers:

- You can route the four LPCI interrupt pins to any of these IRQs: IRQ[3:7, 9:12, 14:15].
- When the CPU board is in the system slot, you can route the four BPCI interrupt pins to any of these IRQs: IRQ[3:7, 9:12, 14:15].

Dual PCI bus architecture

The 82600 integrates dual PCI busses, a local and backplane PCI bus. The local PCI (LPCI) bus operate asynchronously at up-to the host processor's clock rate or down-to one quarter of this clock rate. Architecturally it can be viewed as the high speed private peripheral bus for the processor.

As such, an LPCI bus master cannot directly access the BPCI bus or vice-versa. Whereas the LPCI bus interface always acts as the LPCI central resource bridge; the BPCI interface is intended to be connected to a "backplane" bus, such as CompactPCI, and supports a peripheral bridge mode as well as a system board bridging function.

The CPU board connects to BPCI via the standard J1 and J2 CompactPCI connectors and is compliant with the *CompactPCI specification*, v2.0 r3.0, supporting system and peripheral mode accordingly. The SYS_EN signal defines whether it is a system or peripheral board.

In system mode it is the PCI bus central resource, performing PCI bus enumeration after power- up, handles interrupts, plus clock generation and arbitration.

In peripheral mode, it does not perform PCI bus enumeration but may generate interrupts on the module.

A complete listing of all PCI devices on the CPU board appears in the following table. Note that the 82600 PCI Bridge appears differently depending if the CPU board is operating as a system or peripheral. To read or write the configuration registers of a given device, a PCI configuration space access must be made with the device's corresponding IDSEL address bit set.

- **PCI device detail**

  For all PCI buses on the EPC-3311, the following table summarizes the allocation of IDSEL, Request/Grant pair, and Interrupt(s) for each device.

Table 5-1. PCI devices

Peripheral	PCI bus	IDSEL source	Device	Function	INT	LPCI ~REQ/~GNT
RadiSys 82600 system controller	LPCI	AD11	0			

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Table 5-1. PCI devices

Internal PCI bridge	LPCI			0		
EIDE	LPCI			1		
USB	LPCI			2	D	
Backplane PCI bridge (master only)	LPCI	AD12	1	0	A	
Intel 82544 Ethernet controller A	LPCI	AD19	8	0	B	3
Intel 82544 Ethernet controller B	LPCI	AD14	3	0	C	4
FPGA	LPCI	AD17	6	0	D	
PCI-to-PCI bridge	LPCI	AD15	4	0		0
PMC connector A	PMC	AD18	2	0	D	
PMC connector B	PMC	AD17	1	0	C	

- **Local PCI bus**

A +3.3V signaling level, 32-bit data path width, running at 66 MHz.

- **Ethernet**

  The EPC-3311 contains two Intel 82544EI 10/100/1000Base-T Ethernet controllers incorporating internal MAC and PHY interface support for 10Base-T, 100Base-TX, or 1000Base-T connectivity.

  The Ethernet links route through J3 to the backplane.

  - Maximum speed for 2.16 Ethernet is 100 using the ESM-3100. In a PICMG 2.16 chassis, the backplane routes these signals to the fabric board(s). In a legacy (non-2.16-compliant) chassis, these signals pass through the backplane to RJ-45 connectors on the RTML.
  - The EPC-3311 does not support the 82544's Wake-On-LAN and TCO interfaces.

- **Onboard FPGA**

  The onboard FPGA control registers monitor and control special features. These features require programmatic access and are accessed through a PCI interface to the FPGA. The FPGA does not require bus arbitration signals. With the EPC-3311, much of the chassis status (e.g., board ID and shelf address) is accessed through the HMC. The features and functions of the EPC-3311 assigned to its FPGA include:

  - Access to Boot ROM and OEM Flash ROM (on a single device).
  - RadiSys-defined BIOS Control/Status register.
  - KCS (Keyboard Controller Style) interface to system management HMC.
  - Control of certain interrupts for transmission to the 82600.
  - PCI clock detection and steering logic.

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- RadiSys-defined EPC-3311 FPGA features register set, accessed through an index-data register pair at 0x185/0x187.

For details about these and other registers, see *Appendix H, FPGA features register set*.

- **Boot ROM/Flash**

  The EPC-3311 uses a 32-Mbit (4 Mbyte) Strataflash device for field-upgradable storage of the board's BIOS and to support data flash applications. The top 1 MB of the device holds the BIOS while the remainder is available for OEM non-volatile storage. The OEM storage area is accessed in pages of 4 MB. The EPC-3311 can provide write protection on a page basis. The Strataflash dictates the sector size that is block erased, and can be written on a word-by-word basis.

  The Boot ROM/Flash device is connected to the FPGA on the Xbus. The device is organized as 16-bit words. The FPGA supports up to a 16M x16 (32 Mbyte) device. Single-byte flash write accesses are not supported. XA24-XA1 address lines hook to the A24–A1 signals on the Strataflash (because the FLASH pin byte number is pulled to +3.3V, the A0 pin on the StrataFlash is unused for 16-bit data widths). The upper and lower 512 KB are write-protected, but this can be disabled to update the BIOS. For details, see *Setting jumpers and headers* on page 11 and *Index 0A—ROM Program Control register (0x0A)* on page 120.

  Legacy addressing of boot code requires that code fetches to ROM space below the 1 Mbyte boundary be aliased to the same offset below the top of the device's address space. The alias decodes are enabled on 128 Kbyte boundaries. Coming out of reset, only the top 256 Kbytes below the 1 MB boundary (i.e., the traditional Boot ROM location), are alias-mapped to the boot ROM. Additional segments below these may be enabled through writes to the Boot ROM Access Control register (detailed on page 118).

  All accesses to boot ROM/flash are disabled if the Memory Space enable bit in the FPGA configuration header is cleared (CFG Reg 04, bit 02). When memory space is disabled, the FPGA signals this by negating its ~MEM_EN output. The EPC-3311 may use this signal to force the boot ROM device into a low power state.

- **PMC sites A and B (PMC PCI)**

  The EPC-3311 supports two 32-bit, 33MHZ, PCI +5V I/O compatible PMC sites on the board. Each PMC site uses three PMC connectors.

  - Jn1 and Jn2 carry the standard PCI signals and power.
  - Jn4 signals are routed through the backplane to the RTM PIM site(s).

  A 64-bit PMC can operate as a 32-bit device on the EPC-3311.

- **Backplane PCI bus**

  The CPU board implements a 66 or 32MHz, 32-bit backplane PCI bus. It supports both +3.3V and +5V signalling, based on VI/O. Bus speed is set by the

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state of the backplane's M66EN pin. This bus conforms to both system and peripheral board requirements of the CompactPCI base specification and the Hot Swap specification (PICMG 2.0 and PICMG 2.1).

IDE

The IDE connects to either the onboard devices (CF and header) or to the backplane (J5 or J3). The BIOS setup program configures the IDE interface. For details, see the BIOS Setup program's *IDE Configuration sub-menu* on page 22.

RTC (Real Time Clock)

The 82600 contains a non-volatile, PC-compatible RTC. A precision reference supplies the RTC power pin. A diode connects to the +3.3V supply and to a Lithium button cell to supply current to teh precision reference.

System battery

The EPC-3311 utilizes a CR2032 lithium (Li/MnO_2) coin battery. This +3V battery provides power to retain the correct date, time, and computer parameters in CMOS when the system is powered off. This information assists the BIOS in performing initialization and configuration during power-on or reset operations.

The system battery is designed to provide approximately 1.33 years of service without replacement. However, if configuration or clock-related inconsistencies occur, the battery may need to be replaced.

For information about replacing the battery, see *Replacing the battery* on page 16.

USB

The RadiSys 82600 USB controller provides enhanced support for the UHCI (Universal Host Controller Interface), Version 1.1. The controller routes to J3. When active, the USB controller uses PCI interrupt D.



This feature is not available with DOS.

Keyboard and mouse controller

CPU board provides a PC/AT compatible keyboard connection via a debug header. This is an integrated function within the 82600 chipset.

System Management bus

The 82600 has an interface to the I^2C style System Management bus. This serial bus reads status and controls some of the EPC-3311's hardware features. The I^2C bus controls clock generator outputs, CompactPIC clock control, and interfaces with the SPD on the memory module.

Each SDRAM serial-presence-detect EPROM has a three-bit address field that assigns a unique identity to each module. The EPROM data's data structure is defined in IBM's PC133 SDRAM Registered DIMM Design Specification (August 1999). With a three-bit address field, you can have eight unique DIMM addresses.

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You can also use the I2C interface to configure the AMI FS6259-01 CPU clock synthesizer . Using the I2C serial interface, unused clocks to the memory are shut down.

Table 5-2. 82600 SMbus I2C address assignments

Function	Address
Clock control, generator	1101010*x*
Clock control, CompactPCI clock buffer	1101001*x*
Memory module SPD EPROM	1010000*x*
	where *x* can be either of these:
	1 Read
	0 Write

Hot Swap and system management

The EPC-3311 meets the requirements for Full Hot Swap as defined by the CompactPCI Hot Swap specification. The EPC-3311 can functions as:

- A **host processor** by occupying a system slot in a CompactPCI backplane which may or may not have a 2.16 compliant interconnection fabric.
- A **task processor** by occupying a peripheral slot of a CompactPCI backplane with or without a 2.16 fabric.
- A **node board** in a 2.16 fabric environment which may or may not have a PCI bus linkage between boards.

Hot Swap

Hot Swap behavior depends on the slot the EPC-3311 occupies.

- **Peripheral slot**: For the EPC-3311 as a peripheral task processor, the logical requirements for Hot Swap are achieved through the 82600's Hot Swap Configuration and Status Register (HS_CSR). The operation of the HS_CSR is compliant with PICMG 2.1.
- **System slot**: When deployed in a CompactPCI system slot, the EPC-3311 swaps roles, decommissioning the HS_CSR while providing ~ENUM interrupt service. A system-slot EPC-3311 can be configured under software control to interrupt its local processor when the CompactPCI ~ENUM signal activates. The ~ENUM signal buses on the CompactPCI backplane and asserts when any card in the system, including the EPC-3311, requests enumeration or requests to be taken offline. The EPC-3311 can also produce an interrupt when the Hot Swap latch opens. These interrupts are enabled in the FPGA.

Whether in peripheral or system mode, the EPC-3311 precharges the required CompactPCI signals as defined in PICMG 2.1 during hot insertion.



The CompactPCI specification does not govern system slot Hot Swap.

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The power sequence during a Hot Swap is controlled by the HMC and a Linear Technology LTC†1643L. Upon receiving a signal from the HMC, the external N-Channel FETs switch backplane +3.3V and +5V current to the local backend power domains. The ±12V supplies are switched internally by the part. All supply voltages are ramped-up over a 10ms period. Additionally, the +3.3V and +5V supplies are current limited to 8 A during the ramp-up period. These current limits become the electronic circuit breaker trip-limits after the ramp-up period is finished.

A PWRGD output pin on the LTC1643L indicates that all of the output supply voltages are within tolerance and a FAULT output indicates an over-current condition. These two pins are used in determining the CompactPCI signal ~HEALTHY.

The chip has a built-in lookout to prevent the board from powering up if there is an undervoltage condition on the power coming in.

The power control circuit works in conjunction with the EPC-3311's system management HMC (Hardware Management Controller). However, the EPC-3311 functions normally even if the HMC has failed. A failsafe power-up sequence is defined where the power control circuit automatically proceeds to the power-up phase within a prescribed time, unless the HMC actively gains and sustains control of the power control circuit through the HMC_STROBE.

An additional consideration is when the HMC is powered, while early power is not, or a load fault disables system management power while early power is up. The interface between the power control circuit and the HMC protects against parasitic current flow when either side of the interface is unpowered.

High availability

PICMG 2.1 also defines a hardware-based HA (High Availability) Hot Swap which provides for individual control of each board's power and reset.

Managed HA features include:

- The EPC-3311 inserts into a backplane in a high–impedance, unpowered state.
- The board insertion's precharge phase is automatically controlled, but the EPC-3311 pauses between precharging and the follow-on connection phase which is the action of powering the remainder of the board.
- The HMC has an opportunity to gain control of the connection phase manage power-on and reset processes through system-level management software.
- Power and reset control can go in either direction: to power the board up, to restart the board, or to power the board down.

The RadiSys-managed HA implementation recognizes, emulates, and coexists with the high availability signals defined in PICMG 2.1. However, the activation of those signals only occurs when the EPC-3311 is installed in a chassis which implements, elsewhere in the system, the centralized, proprietary control logic required to implement PICMG 2.1 HA Hot Swap.

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IPMI management system

IPMI system management on the EPC-3311 is implemented in a flexible HMC (Hardware Management Controller).

The microcontroller implements a configurable HMC (Hardware Management Controller) that performs as a BMC (Baseboard Management Controller) or SMC (Satellite Management Controller), depending on how it is configured by the System Management Application Software.

The IPMI hardware management controller provides onboard voltage monitoring, CPU temperature monitoring, and event logging. In addition, it implements the RadiSys-managed Hot Swap architecture. The BMC and SMC are involved in board power-on, determination of powergood, and reset generation.

The EPC-3311's system management node can support dual IPMBs for use in chassis where redundant IPMBs are implemented for fault tolerant system management.

For details about Hardware Management, see *Chapter 7, Hardware management*.

Local I^2C

A second I^2C interface on the EPC-3311 connects to only the I^2C HMC controller. The CPU thermal monitor is the only device on this private I^2C interface. This monitor is an LM84 or equivalent, and allows the IPMI controller to determine the operating temperature of the processor as well as the ambient air temperature.

Power

All power for the EPC-3311 is derived from the CompactPCI backplane. The majority of power is provided on the +3.3V, +5V, +12V, and –12V domains. The backplane also provides IPMB_PWR for the system management subsystem; this potential may be active when the main power rails are not. The EPC-3311 implements appropriate isolation between the HMC and the rest of the board to comply with the PICMG 2.9 System Management Specification on system management functionality and IPMB_PWR usage, even when the chassis power is not on. The EPC-3311 also implements the necessary power isolation and precharge requirements of the PICMG 2.1 Hot Swap specification. When used as a peripheral card, the board can be inserted into a powered-up chassis and function without disrupting the active boards already present. When used as a system slot card, the EPC-3311 may be inserted into a powered backplane without damaging the board.

From a power perspective, Hot Swap insertion includes these states:

- Precharge phase.
- Disconnected state.
- "Power up" or "connection" phase.
- Connected state (connection was successful).
- Power fault state (connection was unsuccessful).

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In the precharge phase, the long pins of the CompactPCI connector provide power to charge in advance the bussed interfaces (named 'early power' by PICMG) on the board so that, when the medium pins hit, they do not represent a sudden change in voltage to the active bus.

Current surge through the long pins is limited by the board and current surge through the medium pins is limited by the matched voltages at contact. This places constraints on how much capacitance and resistive load can be placed on the early potentials.

The disconnected state occurs when the medium length pins make conact with the board. From the disconnected state, the connection phase can occur after the board is fully seated in the backplane as evidenced by BD_SEL being active. Board connection can occur an unbounded time after precharge in HA (High Availability) systems. The connection phase involves the transient of connecting the early potentials—now connected to the backplane—to the board's "backend" potentials. Surge current here is actively limited through control of FET switches that connect the domains during the connection phase. The power connection circuitry, besides limiting surge during connection, also limits the current to backend power.

When backend power is connected to early power without current limiting, the board is in the connected state. If backend power draws excess current, the power control circuit enters a fault state where the backend power is disconnected from early power. The reset mechanism removes the connection command and allows the power control circuit to revert to the disconnected state before another connection can be attempted. In managed HA systems, this can be done through system management commands; otherwise, the EPC-3311 must have ~BD_SEL cycle by external HA circuitry, or by removing and reinserting the board.

When the EPC-3311 is in the connected state, peak current is as follows:

- **+3.3V**: 8 Amps maximum. This limitation is based on a 1 amp per pin current limit (PICMG 2.1, Sec. 3.1.6) and the fact that the long pins cannot contribute current due to the series resistors isolating them from early +3.3V.
- **+5V**: Up to 8 Amps maximum. This limitation is based on a 1 amp per pin current limit (PICMG 2.1, Sec. 3.1.6) and the fact that the long pins can contribute current since there is no series resistor isolating these from early +5V.

When the EPC-3311 is in the power fault state:

- The EPC-3311 power control circuit disconnects all early voltages from backend voltages.
- The power control circuit negates its ~HEALTHY signal.
- The power control circuit signals this state with a FAULT signal.

Recovery from the power fault state is achieved by forcing a transition to the disconnected state.

System management power

The EPC-3311's CompactPCI backplane provides system management power on the IPMB_PWR pin, located on J1.A4.

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HMC hardware watchdog

The HMC implements a software-enabled watchdog as defined in the IPMI specification. This watchdog can generate a board reset to recover from the host processor's failure. This configurable watchdog is started by software commands from the host processor. If not activated by the host, this feature remains dormant.

This watchdog is independent of the hardware watchdog implemented within the 82600.

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Optional features

Optional features or accessories are available for the EPC-3311. These options include internal (board-mountable) and external (peripheral) accessories.

Optional peripheral accessories

A rear transition I/O module (RTM) plugs into a rear I/O slot of a CompactPCI system. Two RTMs are available for use with the EPC-3311:

- **EPC-3311-RTML**: works with the EPC-3311 in a legacy (non-2.16) chassis.
- **EPC-3311-RTM216**: works with the EPC-3311 in a 2.16-compliant system. The main difference between the two RTMs is that the 2.16 RTM has an additional PIM socket in place of the Ethernet connectors.

RTM peripheral connections

RTM connections include:

- One USB connector.
- Two Ethernet RJ-45 connectors (EPC-3311-**RTML only).**
- One serial port D-sub connector.
- One IDE 44-pin connector (internal).
- One PIM port (RTM216) or two PIM ports (RTML):

PMC site	Routed from	Pinout
PMC A (RTM216 only)	CompactPCI J5	PMC site (J14) to PIM (J14)
PMC B	CompactPCI J3	PMC site (J24) to PIM (J24)

- One PS/2-style combination mouse and keyboard port.



The PS/2 port on the EPC-3311's I/O bracket is configured by default for use with a PS/2 keyboard. To use this port with a PS/2 mouse also, you must first attach a "Y" splitter cable.

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Optional board-mounted accessories

- A single SDRAM memory module board may be attached to the EPC-3311. Memory modules are available in 512 MB, and 1 GB sizes.
- Three optional devices can physically mount in the top section of the EPC-3311:
  - One 2.5" hard disk drive
  - One CompactFlash device
  - One PCI Mezzanine Card “A”

Both a PMC and hard disk drive can *not* be installed in site “A.”

Hard disk drives

Hard disk drive options

Hard disk drive options for the EPC-3311 include a bootable CF (CompactFlash) hard disk drive and a factory-installed onboard IDE hard disk drive.

The CompactFlash drive is installed in an industry-standard CompactFlash Type I connector without an ejector.

The onboard IDE hard disk drive can be installed over the PMC “A” site. When it occupies the PMC space, a PMC can not be installed there. The HDD mounting bracket uses the same mounting holes as the PMC. A 2 mm ribbon cable is used.

When an onboard IDE hard disk drive is mounted over the CompactFlash connector, a CompactFlash device (if present) must be installed before you install the HDD.

Either device can be configured as master or slave. Onboard devices are controlled through the BIOS.

Alternatively, the IDE bus is available for other IDE devices through a connector on the RTM.

- You can attached up to two EIDE or IDE devices to the EIDE header on either the RTM or processor board.
- The BIOS supports up to two EIDE or IDE devices. For more information on IDE operations, see page 22.
- You cannot simultaneously access RTMs and on-board devices. There is a BIOS setup switch.

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IDE disks

There is one IDE channel present on the EPC-3311. This channel supports one master and one slave IDE device. The IDE channel is connected to local devices on the EPC-3311 only, or is connected to the RTM only. The EPC-3311, along with its RTM, can house four devices, but because the IDE channel supports only two devices, invalid IDE configurations are possible. Exercise care in ensuring that only two devices of the four possible are used at any given time. The four possible devices include:

- The internal hard disk drive mounted to the main board.
- The CompactFlash disk drive mounted on the main board.
- A remote hard disk drive (e.g., mounted in the media bay) at the end of the cable coming off the RTM.
- A second remote drive (e.g., a CDROM drive mounted in the media bay) also at the end of the cable coming off the RTM.

You cannot access an IDE device on the main board and another on the RTM at the same time. Your selection is limited to either on-board (main; two devices) or RTM (two devices).

Ultra DMA

UDMA (Ultra DMA) is a high-speed transfer mode defined in the ATA-5 specification. This specification requires that the drive be located within a stub length (2") of the electrical end of the bus. UDMA is supported with the following configurations:

- When only a hard disk drive is mounted to the main board and the IDE bus is isolated from the RTM.
- When no devices are mounted to the main board and the device on the RTM is at the end of the cable.



- Overall length (18" maximum) restrictions for UDMA may prevent support of a device at the end of the cable on the RTM.
- When using a flat cable to attach a device, the colored trace for Pin 1 on the cable must align with Pin 1 on the header/connector

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6 RTMs

This chapter describes the EPC-3311's optional RTMs (Rear Transition Modules):

- **EPC-3311 RTML**: This board features one PMC I/O site and two RJ-45 100/1000Base-T Ethernet connectors. The RTML works with the EPC-3311 and a non-packet-switched backplane in a chassis.
- **EPC-3311 RTM216**: Available for 2.16-compliant systems, this board has two PMC slots; it does not have Ethernet RJ-45 connectors. The EPC3311-RTM216 works with the EPC-3311 and a packet-switched backplane in a 2.16-compliant system.

This chapter includes the topics listed in the next table. When reading this file online, you can immediately view information about any topic by placing the mouse cursor over a topic and clicking:

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Features

The RTMs, optional, single-slot 6U CompactPCI peripherals, provide connectors that get I/O out the back of a chassis:

- Two RJ-45 100/1000Base-T Ethernet connectors with LEDs for link and activity (RTML only).
- A 44-pin, straight male IDE header that provides a connection point for a hard-disk ribbon cable.
- One PS/2 keyboard/mouse 6-pin Mini-DIN connector.
- One serial port 9-pin D-Sub male connector.
- One USB connector.
- One PIM port (RTM216) or two PIM ports (RTML):

PMC site	Routed from	Pinout
PMC A (RTM216 only)	J5	PMC site (J14) to PIM (J14)
PMC B	J3	PMC site (J24) to PIM (J24)

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Installation and configuration

This section explains how to install the rear transition module into a chassis.



Avoid causing ESD (electrostatic discharge) damage:

- Keep the card in its anti-static bag until you are ready to install.
- Install the card (as described later in this chapter) only in a static-free environment:
  - Wear an antistatic wrist strap attached to a known ground such as an antistatic lab mat.

    Um unbeabsichtigte Schäden durch elektrostatische Entladung vorzubeugen, sollte bei Arbeiten am System immer ein Erdungsarmband getragen oder andere elektrostatische Entladungs-Vorsichtsmaßnahmen verwendet werden.
  - Remove the card from its antistatic bag only in a static-free environment.
  - Avoid touching printed circuits, connector pins, and components. Where possible, hold the card only by its edges or mounting hardware.
  - Make the least possible movement with your body to minimize electrostatic charges created by contact with clothing fibers, carpet, and furniture.
  - Keep one hand on the computer chassis, if possible, as you insert or remove a card.
  - Avoid placing the card on the chassis cover or on a metal table. The cover and metal table increase the risk of damage because they provide an electrical path from your body through the card.
- During external cable installation, ensure that the cables are not active. This card is not designed for hot insertion of any interface.
- Always turn the computer off before removing a card from the chassis.

The rear transition module, like most other electronic devices, is susceptible to ESD damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

⚠ WARNING

Only qualified, experienced electronics service personnel should access and handle the equipment.

Es sollte nur qualifiziertes und erfahrenes Fachpersonal am System arbeiten.

Before you begin

The RTM requires the following:

- Adequate ventilation. Ensure that the platform complies with the environmental requirements listed in *Specifications* on page 5.
- A chassis such as the RadiSys CP50.

  To install the RTM onto a passive backplane not manufactured by RadiSys, consult the instructions provided by the backplane manufacturer.
- An already-installed EPC-3311. For information about installing the EPC-3311, see *Chapter 2, Installation and operation*.

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Inserting the RTM

To insert the RTM on the PCI bus backplane.

1. Ensure that power to your CompactPCI system is off, or that the CPU card is removed from the front of the chassis.

   You cannot hot-swap the RTM.

2. Locate the slot on the rear of the backplane directly opposite the EPC-3311.
3. Ensure that the ejector handles are in the normal (non-eject) position. (Push the top handle down and the bottom handle up so that the handles are not tilted.)
4. Slide the RTM into the slot. Use firm pressure on the handles to mate the module with the connectors.
5. Tighten the retaining screws in the top and bottom of the front panel to ensure proper connector mating and prevent the module from loosening due to vibration.
6. Connect peripherals to the RTM, if needed. Periperals typically include a keyboard, but also perhaps a mouse, modem, printer, and so on. For information about connector pinouts, see *RTM connectors* on page 70.

   Observe the following while the system is powered up:
   - Do not plug cables or connectors into the front panel connectors. Because electronics equipment generally cannot withstand fluctuations in power, damage can arise from plugging in a device or board while power is on.
   - Do not plug in a serial or parallel device, keyboard, transceiver, monitor or other component. This applies to equipment at either end of an interface cable.

7. Reconnect all power cords, then power on the system.

Removing the RTM

Occasionally you may need to remove the RTM to perform maintenance tasks.

To remove the RTM from the CompactPCI chassis:

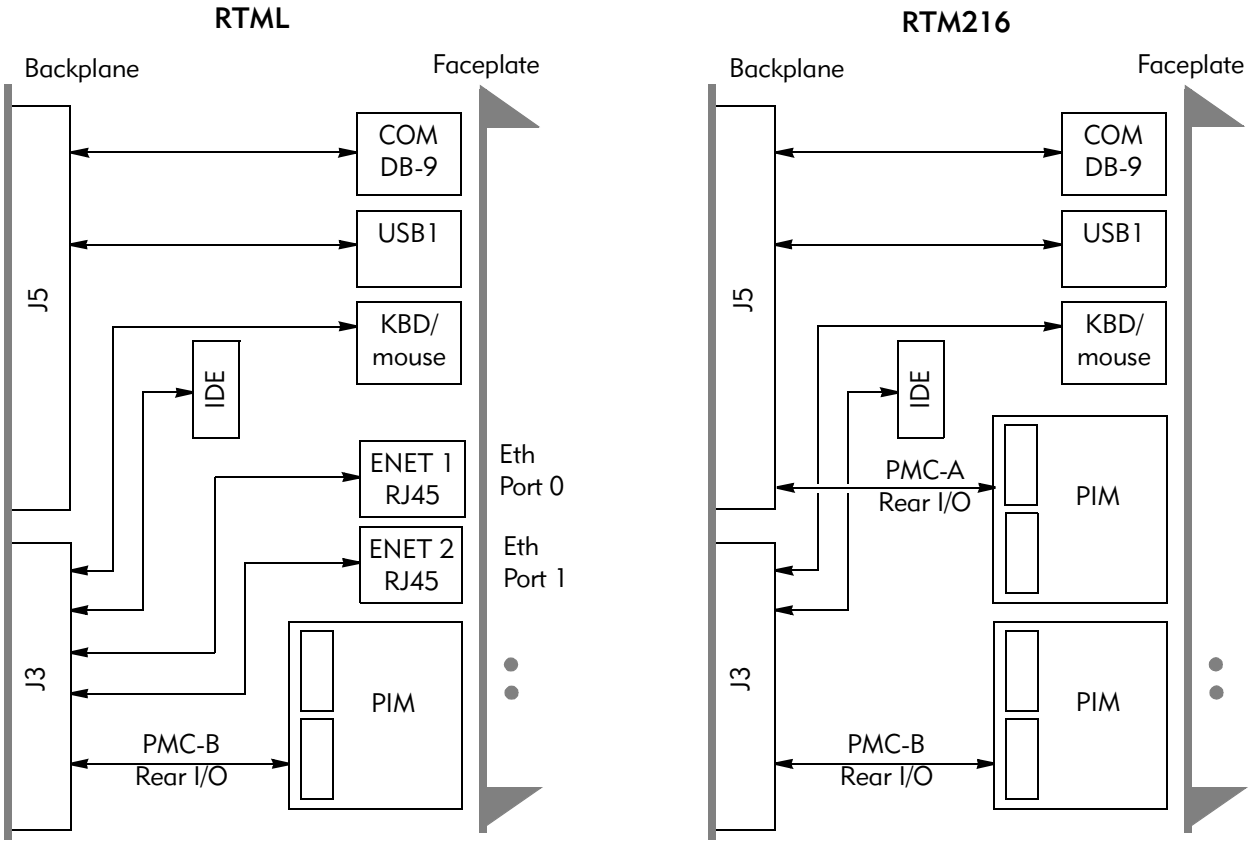
1. Ensure that power to your CompactPCI system is off, or that the CPU card is removed from the front of the chassis.
2. Press the latch part of the extractors inward until the extractor handle swings out and pivots freely.
3. Pull outward on the extractor handles until the RTM disengages from the rear connector.
4. Slide the RTM out of the CompactPCI chassis.

When finished with the tasks at hand, follow the instructions in *Inserting the RTM* on page 68 to re-install the RTM.

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Block diagram

Figure 6-1. RTMs: block diagram



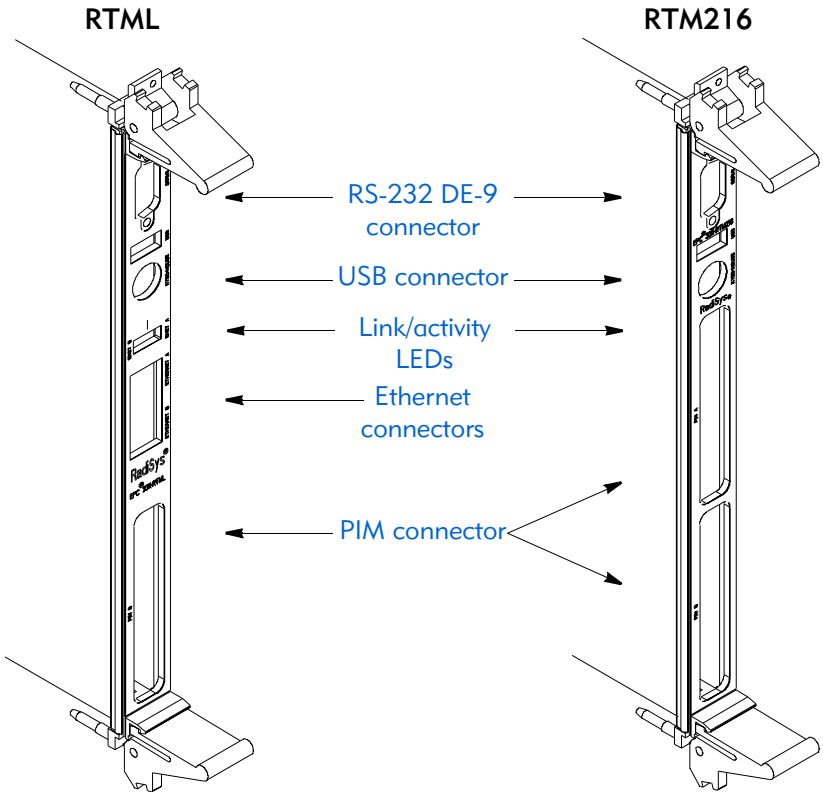
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RTM connectors

Connector locations

The next figure shows the locations of connectors on the EPC-3311 RTM:

Figure 6-2. RTM: connectors



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CompactPCI connectors (J3 and J5)

The RTM uses two {platform} connectors, J3 and J5.

J5 connector

J5 provides the connection for all T1/E1 pairs and LED control from PMC connector Jn4. J5 also provides connection paths between the RTM and the TDM2IX and the CPLD.

The four connections, labeled CAP:RTMn and CPLD:RTMn respectively, are reserved; no functions are programmed into these devices.

Table 6-1. CompactPCI J5 connector (RTM)

Pin	A	B	C	D	E	F (9)
22	~ENETA:100_LED	~ENETA:1000_LED	KBD_DAT	IDE_INTR	~IDE_RSTDRV	**GND**
21	~ENETB:100_LED	~ENETB:1000_LED	KBD_CLK	~IDE_DACK	~IDE_CS1	**GND**
20	COM_TXD	USB_DAT+	USB_DAT–	IDE_IORDY	~IDE_CS3	**GND**
19	COM_RXD	**+5V**	M_DAT	~IDE_IOW	IDE_DREQ	**GND**
18	~COM_RTS	~COM_CTS	M_CLK	~IDE_IOR	IDE_A2	**GND**
17	~IDE_PDIAG	~IDE_DASP	IDE_D15	IDE_A0	IDE_A1	**GND**
16	IDE_D10	IDE_D11	IDE_D12	IDE_D13	IDE_D14	**GND**
15	IDE_D5	IDE_D6	IDE_D7	IDE_D8	IDE_D9	**GND**
14	IDE_D0	IDE_D1	IDE_D2	IDE_D3	IDE_D4	**GND**
13	PMCA:IO5	PMCA:IO4	PMCA:IO3	PMCA:IO2	PMCA:IO1	**GND**
12	PMCA:IO10	PMCA:IO9	PMCA:IO8	PMCA:IO7	PMCA:IO6	**GND**
11	PMCA:IO15	PMCA:IO14	PMCA:IO13	PMCA:IO12	PMCA:IO11	**GND**
10	PMCA:IO20	PMCA:IO19	PMCA:IO18	PMCA:IO17	PMCA:IO16	**GND**
9	PMCA:IO25	PMCA:IO24	PMCA:IO23	PMCA:IO22	PMCA:IO21	**GND**
8	PMCA:IO30	PMCA:IO29	PMCA:IO28	PMCA:IO27	PMCA:IO26	**GND**
7	PMCA:IO35	PMCA:IO34	PMCA:IO33	PMCA:IO32	PMCA:IO31	**GND**
6	PMCA:IO40	PMCA:IO39	PMCA:1O38	PMCA:IO37	PMCA:IO36	**GND**
5	PMCA:IO45	PMCA:IO44	PMCA:IO43	PMCA:IO42	PMCA:IO41	**GND**
4	PMCA:IO50	PMCA:IO49	PMCA:IO48	PMCA:IO47	PMCA:IO46	**GND**
3	PMCA:IO55	PMCA:IO54	PMCA:IO53	PMCA:IO52	PMCA:IO51	**GND**
2	PMCA:IO60	PMCA:IO59	PMCA:IO58	PMCA:IO57	PMCA:IO56	**GND**
1	~RTM_PRSNT2	PMCA:IO64	PMCA:IO63	PMCA:IO62	PMCA:IO61	**GND**

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J3 connector

The J3 connector is a user-defined connector that routes T1/E1 and Ethernet signal pairs and LED controls to the RTM for specific use with the 8-port Serial 2-port Ethernet RTM.

J3 provides the interface for PCI Ethernet signaling and LED control as well as IX Ethernet signaling and LED control.

The four connections, labeled CAP:RTMn and CPLD:RTMn respectively, are reserved; no functions are programmed into these devices.

Table 6-2. CompactPCI J3 connector (RTM)

Pin	A	B	C	D	E	F (9)
19	RTM_ID[0]	RTM_ID[1]	~ENETA:LNK_LED	RTM_ID[2]	+5V	GND
18	LPa_DA+	LPa_DA–	**GND**	LPa_DC+	LPa_DC–	GND
17	LPa_DB+	LPa_DB–	**GND**	LPa_DD+	LPa_DD–	GND
16	LPb_DA+	LPb_DA–	**GND**	LPb_DC+	LPb_DC–	GND
15	LPb_DB+	LPb_DB–	**GND**	LPb_DD+	LPb_DD–	GND
14	**+3.3V**	**+3.3V**	**+3.3V**	**+5V**	**+5V**	GND
13	PMCB:IO5	PMCB:IO4	PMCB:IO3	PMCB:IO2	PMCB:IO1	GND
12	PMCB:IO10	PMCB:IO9	PMCB:IO8	PMCB:IO7	PMCB:IO6	GND
11	PMCB:IO15	PMCB:IO14	PMCB:IO13	PMCB:IO12	PMCB:IO11	GND
10	PMCB:IO20	PMCB:IO19	PMCB:IO18	PMCB:IO17	PMCB:IO16	GND
9	PMCB:IO25	PMCB:IO24	PMCB:IO23	PMCB:IO22	PMCB:IO21	GND
8	PMCB:IO30	PMCB:IO29	PMCB:IO28	PMCB:IO27	PMCB:IO26	GND
7	PMCB:IO35	PMCB:IO34	PMCB:IO33	PMCB:IO32	PMCB:IO31	GND
6	PMCB:IO40	PMCB:IO39	PMC:1O38	PMCB:IO37	PMCB:IO36	GND
5	PMCB:IO45	PMCB:IO44	PMCB:IO43	PMCB:IO42	PMCB:IO41	GND
4	PMCB:IO50	PMCB:IO49	PMCB:IO48	PMCB:IO47	PMCB:IO46	GND
3	PMCB:IO55	PMCB:IO54	PMCB:IO53	PMCB:IO52	PMCB:IO51	GND
2	PMCB:IO60	PMCB:IO59	PMCB:IO58	PMCB:IO57	PMCB:IO56	GND
1	~ENETB:LNK_LED	PMCB:IO64	PMCB:IO63	PMCB:IO62	PMCB:IO61	GND

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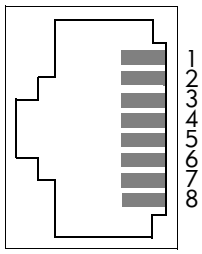
Ethernet connectors

The Ethernet links route from J3 to the RJ-45.

- The maximum speed of 2.16 Ethernet is 100. In a PICMG 2.16 chassis, the backplane routes these signals to the fabric board(s). In a legacy (non-2.16) chassis, these signals pass through to RJ-45 connectors on the RTM.
- The EPC-3311 does not support the 82544's Wake-On-LAN and TCO interfaces.

The Ethernet connector is used on the EPC3311-RTML. The EPC3311-RTM216 has an additional PIM socket in place of the Ethernet connectors.

Table 6-3. Ethernet RJ-45 10BASE-T and 100BASE-T operation



Pin	Name	Signal	Pin		Signal
1	TXP	Transmit+	5		Not used
2	TXN	Transmit–	6	RXN	Receive–
3	RXP	Receive+	7		Not used
4		Not used	8		Not used

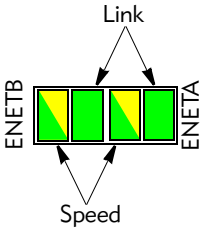
Table 6-4. Ethernet RJ-45 1000BASE-T operation

Pin	Name	Signal	Pin		Signal
1	TRD +0	Transmit+/Receive+ Data 0	5	TRD –2	Transmit–/Receive– Data 2
2	TRD –0	Transmit–/Receive– Data 0	6	TRD –1	Transmit–/Receive– Data 0
3	TRD +1	Transmit+/Receive+ Data 1	7	TRD +3	Transmit+/Receive+ Data 3
4	TRD +2	Transmit+/Receive+ Data 2	8	TRD –3	Transmit–/Receive– Data 3

Link/activity LEDs

The Ethernet connectors on the RTM have integrated bicolor LEDs that indicate link and activity.

Table 6-5. Port LEDs



LED	Signal	Description
1	Link	**Not lit**: No link.
		Green: Link active.
2	Speed	**Not lit**: 10 mbit port speed.
		Yellow: 100 mbit port speed.
		Green: 1000 mbit port speed.

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IDE header (internal)

The RTM includes one IDE channel which supports one master and one slave IDE device. It is a 44-pin, 2x22, 0.1" pitch straight male connector that provides a connection point for a hard-disk ribbon cable.

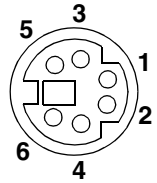
Table 6-6. IDE header pin assignments

Pin	Signal	Pin	Signal
1	IDE:~RST	2	**GND**
3	IDE:D7	4	IDE:D8
5	IDE:D6	6	IDE:D9
7	IDE:D5	8	IDE:D10
9	IDE:D4	10	IDE:D11
11	IDE:D3	12	IDE:D12
13	IDE:D2	14	IDE:D13
15	IDE:D1	16	IDE:D14
17	IDE:D0	18	IDE:D15
19	**GND**	20	Key
21	IDE:DRQ	22	**GND**
23	IDE:~IOW	24	**GND**
25	IDE:~IOR	26	**GND**
27	IDE:IORDY	28	IDE:CSEL
29	IDE:~DAK	30	**GND**
31	IDE:IRQ	32	No connect
33	IDE:A1	34	PDIAG
35	IDE:A0	36	IDE:A2
37	IDE:~CS1	38	IDE:~CS3
39	No connect	40	**GND**
41	**+5V**	42	**+5V**
43	**GND**	44	No connect

Keyboard and mouse connectors

One PS/2 style connector is used for the keyboard and mouse connections. This connector is mounted on the RTM and is accessible on the rear panel. A PS/2-style keyboard can be plugged directly into this connector, or a standard PS/2 splitter cable can be used to provide separate connections for a PS/2 keyboard or mouse.

Table 6-7. P/S 2-style keyboard and mouse pin assignments



Pin	Signal	Pin	Signal
1	Data	4	+5V
2	Mouse data	5	Keyboard clock
3	Ground	6	Mouse clock

The EPC-3311 keyboard and mouse pins are opposite the laptop industry standard. This allows a keyboard to plug in directly without "Y" splitter adapter.

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PIM connector

The EPC-3311 supports two 32-bit PCI 5 V I/O-compatible PMC sites on the board. Each PMC site uses three PMC connectors.

- Jn1 and Jn2 carry the standard PCI signals and power.
- Jn4 signals are routed through the backplane to the RTM PIM site(s).



A 64-bit PMC can operate as a 32-bit device on the EPC-3311.

Table 6-8. PIM connector pin assignments

Pn0/Jn0				Pn4/Jn4			
Pin	**Name**	**Name**	**Pin**	**Pin**	**Name**	**Name**	**Pin**
1	Signal	**+12V**[1]	2	1	I/O	I/O	2
3	Signal	Signal	4	3	I/O	I/O	4
5	**+5V**	Signal	6	5	I/O	I/O	6
7	Signal	Signal	8	7	I/O	I/O	8
9	Signal	**+3.3V**	10	9	I/O	I/O	10
11	Signal	Signal	12	11	I/O	I/O	12
13	**GND**	Signal	14	13	I/O	I/O	14
15	Signal	Signal	16	15	I/O	I/O	16
17	Signal	**GND**	18	17	I/O	I/O	18
19	Signal	Signal	20	19	I/O	I/O	20
21	**+5V**	Signal	22	21	I/O	I/O	22
23	Signal	Signal	24	23	I/O	I/O	24
25	Signal	**+3.3V**	26	25	I/O	I/O	26
27	Signal	Signal	28	27	I/O	I/O	28
29	**GND**	Signal	30	29	I/O	I/O	30
31	Signal	Signal	32	31	I/O	I/O	32
33	Signal	**GND**	34	33	I/O	I/O	34
35	Signal	Signal	36	35	I/O	I/O	36
37	**+5V**	Signal	38	37	I/O	I/O	38
39	Signal	Signal	40	39	I/O	I/O	40
41	Signal	**+3.3V**	42	41	I/O	I/O	42
43	Signal	Signal	44	43	I/O	I/O	44
45	**GND**	Signal	46	45	I/O	I/O	46
47	Signal	Signal	48	47	I/O	I/O	48
49	Signal	**GND**	50	49	I/O	I/O	50
51	Signal	Signal	52	51	I/O	I/O	52
53	**+5V**	Signal	54	53	I/O	I/O	54
55	Signal	Signal	56	55	I/O	I/O	56
57	Signal	**+3.3V**	58	57	I/O	I/O	58
59	Signal	Signal	60	59	I/O	I/O	60

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Table 6-8. PIM connector pin assignments (Continued)

Pn0/Jn0				Pn4/Jn4			
61	–12V[1]	Signal	62	61	I/O	I/O	62
63	Signal	Signal	64	63	I/O	I/O	64

[1] +12V and –12V are not connected on the RTM.

[2] Pn4/Jn4 pins correspond to the Jn4 pins of the PMC.

RS-232 DE-9 connector

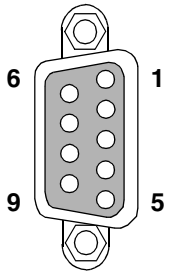


Table 6-9. RS-232 RTM connector

Pin	Signal	Pin	Signal
1	No connect	6	No connect
2	Receive data	7	Request to send
3	Transmit data	8	Clear to send
4	No connect	9	No connect
5	Signal ground		

Note: Due to pin limitations on J3 and J5, only the shown signals are actually connected.

USB connector

A 4-pin single height connector provides a USB port connection that is externally accessible.

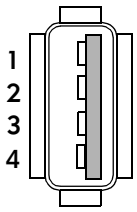


Table 6-10. USB connector

Pin	Signal
Mechanical solder lug	Shield ground
1	+5V
2	USB DATA–
3	USB DATA+
4	Ground
Mechanical solder lug	Shield ground

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7 Hardware management

This appendix describes the EPC-3311's Hardware Management features. Hardware management is an important element in computer networks and high availability systems. Remote management of software and hardware inventory, compatibility, upgrade, fault management, and maintenance offers considerable operating savings. Remote hardware management also cuts response time for these functions.

IPMI (Intelligent Platform Management Interface), used to implement hardware management on the EPC-3311, defines a standard protocol as well as a standard hardware interface for instrumentation.

Overview

An independent management controller provides local hardware management services on the EPC-3311. When installed in a managed platform, such as the RadiSys CP50, the EPC-3311 is a member of a distributed management system comprised of intelligent devices that can monitor and maintain local sensors, and alert a centralized management controller when alarm conditions occur. The HMC (Hardware Management Controller) on the EPC-3311 provides local environment monitoring for the board.

Key features of EPC-3311 hardware management

- IPMI v1.5 compliant.
- Based on PICMG 2.9 System Management Specification.
- Support for redundant management communication paths.
- Local Sensor Monitoring.
- Access to local controls.
- Support for managed hot swap.
- Fault Annunication through a Blade status LED.
- User status LED for software use.
- Software Enabled Watchdog.
- FRU Inventory Area.
- Host Interface (KCS).
- SEL (System Event Log).
- Field upgradeable firmware.

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Local management services

The HMC provides several local services for the EPC-3311. The HMC monitors local environmental sensors, such as temperature and voltage, and provides access to local controls such as power and reset. The HMC also provides hot swap services and fault annunciation for the local board.

Sensor monitoring

The HMC monitors the health of the EPC-3311 on which it resides. EPC-3311 health is determined by the monitoring of sensors located throughout the board, which range from on-board voltage readings to ambient temperatures. The next table lists local sensors that the HMC monitors.

Table 7-1. Local sensors

No.	Sensor	Reading type	Sensor type	Enable state	Nominal value
0	+12V	Threshold	Voltage	Normal	+12.00
1	+5V	Threshold	Voltage	Normal	+5.00
2	+3.3V	Threshold	Voltage	Normal	+3.3
3	VIO	Threshold	Voltage	Normal	+5
4	+2.5V	Threshold	Voltage	Normal	+2.5
5	+1.5V	Threshold	Voltage	Normal	+1.5
6	Vcore	Threshold	Voltage	Normal	+1.4
7	VTT	Threshold	Voltage	Normal	+1.25
8	Proc temp	Threshold	Temperature	Normal	40°C
9	HS pwr fault	Digital	Power unit	Normal	0
10	Board pwr off	Digital	Power unit	Normal	0
11	Core power fault	Digital	Power unit	Normal	0
12	Board reset	Digital	Chassis	Event generation disabled	0
13	PCI present	Digital	Chassis	Event generation disabled	0
14	System slot	Digital	Chassis	Event generation disabled	0[1]
15	Board sel	Digital	Chassis	Event generation disabled	0
16	Extract switch	Digital	Slot/connector	Event generation disabled	0
17	Slot number	Discrete	Slot/connector	Event generation disabled	1[1]
18	HS ENUM	Digital	Reserved	Event generation disabled	0
19	DEG	Digital	Power unit	Event generation disabled	0

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Table 7-1. Local sensors

No.	Sensor	Reading type	Sensor type	Enable state	Nominal value
20	FAL	Digital	Power unit	Event generation disabled	0
21	VSM present	Digital	Slot/connector	Event generation disabled	1[1]

[1] Indicates defaults, or slot dependent values

Controls

The HMC provides access to local controls on the board. The local controls allow the HMC to recover from faults. Through the local controls, the HMC, Platform Manager, or management software can instruct the EPC-3311 to reset or power off. The next table lists local controls provided by the HMC.

Table 7-2. Local controls

No.	Description	Type	Function	Default state
0	Reset	Digital	Blade Reset	Off
1	SMI	Digital	SMI interrupt	Off
2	Power	Digital	Blade Power	On
3	IPMB0 Enable	Digital	Enable IPMB 0	On
4	IPMB1 Enable	Digital	Enable IPMB 1	On

Managed Hot Swap

The HMC manages the hot swap aspects of the EPC-3311. This includes event generation when the ejector latch is opened or closed, and annunciating the extraction readiness of the EPC-3311 through the blue LED. Hot swap management also includes the generation of the Healthy signal on the backplane and annunciating health through an event.

Fault annunciation

The HMC supports fault annunciation through a front panel LED located near the bottom of the EPC-3311 faceplate. The LED, labeled "Blade", indicates the Healthy state of the HMC and EPC-3311. A green LED indicates that the board is healthy and that no faults exist. A red LED indicates that the board is not healthy and that a fault does exist. The next table describes Blade LED states.

Table 7-3. Blade LED

LED	State	Status
Off		Powered off
Orange	Solid	Initializing
	Blink	Extraction pending
Green		Normal operation
Red		Hardware fault

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Status LEDs

The HMC also provides access to a second LED that indicates the status of software executing on the EPC-3311. This LED, located just above the HW LED and labeled "User", indicates the Health of the software.

Table 7-4. User LED

LED	State	Status
Orange	Off	Powered off
	Blink	POST start (BIOS)
	Double-blink	BIOS setup (BIOS)
	Solid[1]	POST complete (BIOS)
Green	Solid[1]	POST complete (BIOS)
Red		Pre-POST

[1] Behavior selected by BIOS setup item.

The HMC manages and controls the blue hot swap LED, which indicates the following conditions:

Table 7-5. Hot Swap LED

LED	Status
Off	Board is powered on and active in the system.
On	Board is powered off and ready for extraction, ejector latch may or may not be opened.

Watchdog

The HMC implements a software-enabled watchdog as defined in the IPMI specification. This watchdog can generate a board reset to recover from host processor failure This watchdog is configurable and is started by software commands from the host processor. If not activated by the host, this feature remains dormant.

FRU inventory area

The HMC implements a standard IPMI FRU inventory area. The 4K FRU area is maintained in the non-volatile storage. The HMC provides access to the FRU area through the FRU inventory commands defined in the IPMI specification. The HMC supports standard areas for Board, Product, and Multi-Record Information as defined by the IPMI Platform Management FRU Information Storage Definition specification.

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Table 7-6. IPMI FRU inventory area

Area	Contents	Comments
Board	• Manufacturing date/time • Board manufacturer • Board product name • Board serial number • Board part number • Firmware creation date • Extensible information area	Board area information is defined within the scope of the firmware and contains valid default values. The Board area is designated as "Read-Only."
Product	• Manufacturer name • Product name • Product part/model number • Product version • Product serial number • Asset tag • Extensible information area	The Product area does not contain default values, and is provided for OEM or end-customer use.
Multi-record information	N/A	This area's format is defined by the FRU specification.

SEL (System Event Log)

The HMC implements a standard IPMI system event log for logging local events. The 12 K SEL is maintained in the non-volatile storage. The HMC provides access to the SEL through the SEL commands defined in the IPMI specification.

Host interface

The HMC provides a host interface to the system processor. The host interface is implemented using the KCS interface mechanism at I/O locations 0xCA2/3. The management firmware can respond to all IPMI requests over this interface.

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A Chipset and I/O map

I/O map

Table A-1. EPC-3311 I/O map

I/O address (hex)	Register description
0000 – 000F	DMA controller 1 – 8237A
0020 – 0021	Master 8259A
0022	Power management
0040 - 0043	8254A timer/counter
0060/0064	Keyboard controller data and control registers (if enabled)
0061	Port B
0070 – 0071	146818 RTC – NMI mask
0072 – 0073	Extended CMOS RAM access (72 index, 73 data)
0080	POST port
0080 – 008F	74LS612 style DMA page registers
0092	Port A
00A0 – 00A1	Slave 8259A
00C0 – 00DF	DMA controller 2 – 8237A
00F0	Clear math coprocessor busy
00F1	Reset math coprocessor
0100	BIOS features of the FPGA
0185, 0187	Index and data of the FPGA features register
01F0 – 01F7	EIDE chip select 0 region
03F6	EIDE chip select 1 region
03F8 – 03FF	Serial port registers
04D0 – 04D1	INT1/INT2 edge/level control
0CA0–0CA3	SMB interface register (in FPGA)
0CF8 (dword)	LPCI/BPCI configuration index
0CF9 (byte)	Reset control
0CFC – 0CFF	LPCI/BPCI configuration data registers.
0CF9 (byte)	Reset control
1CF8 – 1CFF	Alternate BPCI configuration index and data registers
(CFG-0.94)±0x3F	Power management/SMBUS base register/DMA
(CFG–1.20)±0xF	EIDE bus master DMA registers
(CFG–2.20)±0x1F	USB I/O space

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Memory map

The memory map shows the location of the standard DRAM, VGA, and BIOS devices. The table below describes how physical addresses from the Mobile Tualatin† map into memory.

Table A-2. EPC-3311 memory map

Range	CPU address	Region	Cached
0 to 640 KB	0000 0000 – 0009 FFFF	DRAM (640 KB)	Yes
640 KB to 1 MB	000A 0000 – 000B FFFF	VGA memory	No
	000C 0000 – 000C BFFF	Shadowed VGA BIOS (48 KB)	Yes
	000C C000 – 000D FFFF	BIOS extensions	Yes[1]
	000E 0000 – 000F FFFF	System BIOS shadow	Yes
1 MB to 512 MB	1000 0000 – 1FFF FFFF	DRAM (511 MB) Minimum EPC-3311 memory cfg	Yes
512 MB to 2 GB	2000 0000 – 7FFF FFFF	Optional DRAM and PCI bus	No
2 GB to 4 GB to 32 MB	8000 0000 – FDFF FFFF	Available for PCI	No
4 GB–32 MB to 4 GB	FE00 0000 – FFEF FFFF	Optional OEM Flash (3–31 MB)	No
	FFF0 0000 – FFFF FFFF	System BIOS (1 MB)	No

[1] If no BIOS extensions, the PCI bus is not cacheable.

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PCI I/O space

The FPGA implements several I/O mapped registers for ISA-style legacy functions. In addition, a pair of these registers is used to access a set of index-mapped registers for RadiSys-specific status and control. The direct I/O-mapped registers are in the table below. The default values shown for these registers are loaded after a POR (Power on Reset). With the single exception of the write-only Port 80 register, none of these registers can be accessed for reads or writes if the I/O Enable bit in the Command register is cleared.

Table A-3. Fixed I/O-mapped ports and registers

Name	Address	Default Value	Function
Port 80 debug port (not populated)	0x080		Write-only port to POST status register
BIOS Features[2]	0x100	0x00	Mfg. test & force re-flash
Register Set Index[2]	0x185	0x00	FPGA Features—register set index
Register Set Data[2]	0x187	0x00	FPGA Features—register data port
Sys. Mgmt. HMC port[2]	0xCA0–CA3[1]		Keyboard Controller Style interface to the system management HMC

[1] HMC interface is normally accessed through the register pair 0xCA2, 0xCA3. The pair 0xCA0, 0xCA1 is also decoded for backward compatibility with legacy software.

[2] Enable these registers for access by writing a '1' to PCI Config Register 04, bit 0.

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B Interrupts

The next table shows interrupt assignments for the EPC-3311.

Table B-1. Interrupts

Interrupt	Interrupt function	Generic capable
IRQ0	System timer (internal 82600 connection)	
IRQ1	Keyboard controller (internal 82600 connection)	Yes
IRQ2	Cascade interrupt input (internal 82600 connection)	
IRQ3	COM2 (not used; internal 82600 connection)	Yes
IRQ4	COM1 (internal 82600 connection)	
IRQ5	Not used	Yes
IRQ6	Not used	Yes
IRQ7	Not used	
IRQ8	Real time clock (internal 82600 connection)	
IRQ9	Not used	Yes
IRQ10	Not used	Yes
IRQ11	Not used	Yes
IRQ12	PS/2 mouse (internal 82600 connection)	Yes
IRQ13	Numeric coprocessor ~FERR (internal 82600 connection)	
IRQ14	Primary IDE (internal 82600 connection)	
IRQ15	Not used	Yes
NMI	~SERR, ECC	
SMI	Power management	
PIRQA		
PIRQB	Ethernet1	
PIRQC	Ethernet2	
PIRQD	PMC-A (INTA), USB (internal 82600 connection) FPGA (~ENUM, LATCH, interrupt before reset)[1]	

[1] For details, see *Index 05—Local Interrupt Control/Status register (0x05)* on page 115.



When operating as a System Controller, PIRQ[A–D] correspond directly to the Local and Backplane PCI interrupts INT[A–D].

The software may steer INT[A–D] interrupts to any of Generic Capable interrupts using the Route Control register. However, an interrupt should not be used both for legacy and PCI interrupts.

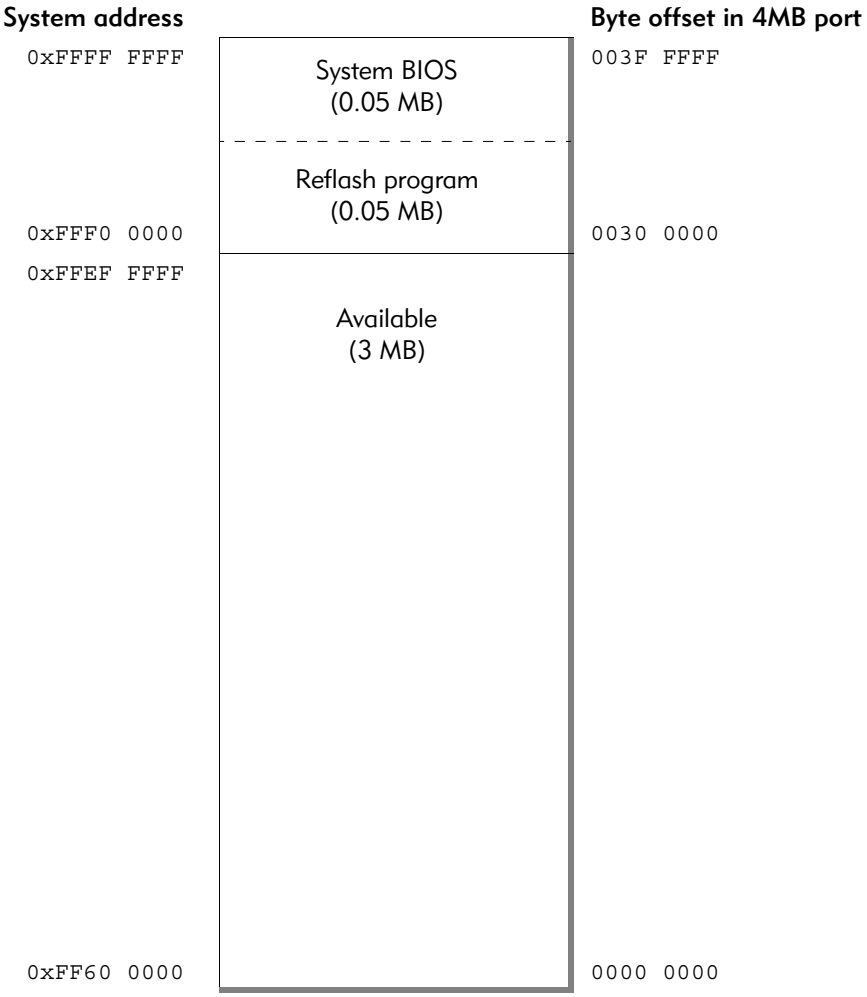
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C Flash memory addresses

The EPC-3311 4MB flash chip contains these major sections:

Figure C-1. Flash chip memory addresses



For information about re-programming the flash chip's contents, contact RadiSys as described in *Where to get more information* on page iv.

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D Connectors

This appendix details the connectors on the EPC-3311 and gives the signal pinout of each connector.



For more information about connectors on rear transition modules, see *Chapter 6, RTMs.*

This product includes the connectors listed in the table below. When reading this file online, you can immediately view information about any connector by placing the mouse cursor over a connector name and clicking.

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Serial port	100
IDE header (internal)	101
CompactFlash socket	102
Reset button	102

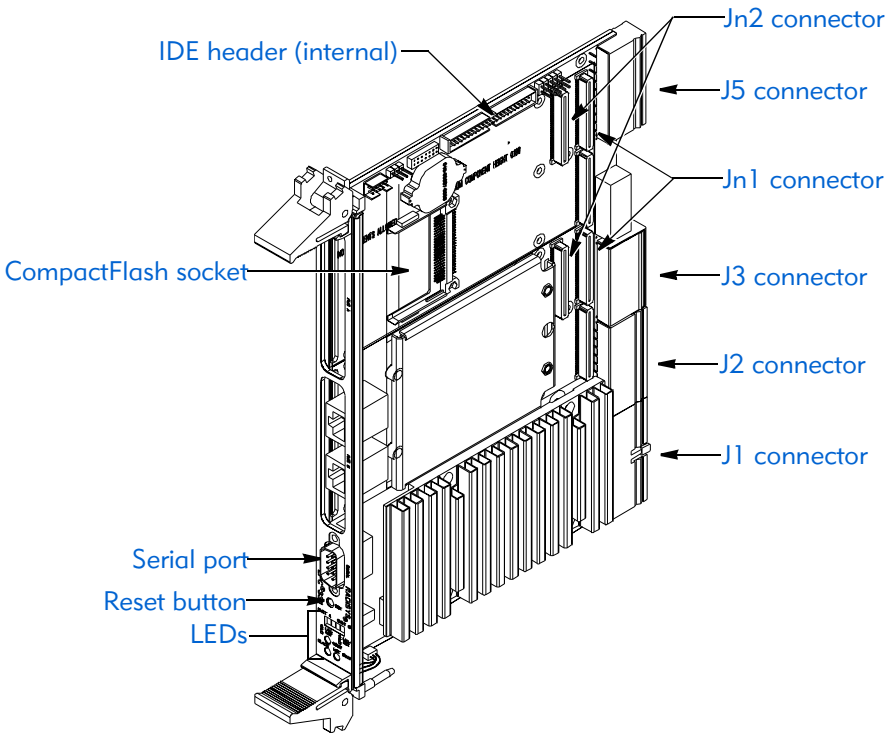
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Connector locations

Figure D-1 shows the locations of the connectors on the EPC-3311's CPU board.

For information about installing peripherals and jumper settings, see *2, Configuration and installation*.

Figure D-1. EPC-3311 connector locations



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CompactPCI connectors

CompactPCI connectors are located on the main board (EPC-3311) and the RTM.

The EPC-3311 uses a backplane for most of its I/O connection. These connections are through PICMG-defined connectors J1 through J5.

The EPC-3311 uses:

- J1 and J2, as connections for the CompactPCI bus
- J3, as custom connections for I/O going to an RTM and for PICMG 2.16 fabric connections
- J5, as custom connections for I/O going to a RTM

Note: the EPC-3311 does not include a populated J4.

The EPC-3311 is a 32-bit CompactPCI device, but the J1 and J2 connectors are treated as 64-bit CompactPCI by providing passive terminations for all 64-bit signals. This is mandated by PICMG when the EPC-3311 is used as a system slot board (i.e., installed in a system slot).

The EPC-3311's J1 and J2 connections can be either 5V or 3.3V signaling voltage. The backplane determines which voltage by its VIO connection to one of these power supplies. The EPC-3311 uses VIO as its power source for its drivers and pull-ups. Because the EPC-3311 is a universal board, no coding key is used in the J1 connector.

The following tables list the pin signals for the CompactPCI connectors of the EPC-3311. The CompactPCI J1 connector is a female 2 mm-pitch 6-column x 25-row right angle Hard Metric (HM) connector with a guide lug in the center. The CompactPCI J2 connector is the same as the J1 connector, except there are only 22 rows numbered 1–22, and the center guide lug is eliminated. All of these signals have the standard CompactPCI R2.1 bus definitions.

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J1 connector

The CompactPCI J1 connector is a female 2mm-pitch 6 column by 25 row right angle Hard Metric (HM) connector with a guide lug in the center.

Table D-1. CompactPCI J1 connector

Pin	A	B	C	D	E	F (9)
25	**+5V**	~REQ64	~ENUM	**+3.3V**	**+5V**	**GND**
24	AD[1]	**+5V**	VIO (2)	AD[0]	~ACK64	**GND**
23	**+3.3V**	AD[4]	AD[3]	**+5V**	AD[2]	**GND**
22	AD[7]	**GND**	**+3.3V**	AD[6]	AD[5]	**GND**
21	**+3.3V**	AD[9]	AD[8]	M66EN	C/~BE[0]	**GND**
20	AD[12]	**GND**	VIO	AD[11]	AD[10]	**GND**
19	**+3.3V**	AD[15]	AD[14]	**GND**	AD[13]	**GND**
18	~SERR	**GND**	**+3.3V**	PAR	C/~BE[1]	**GND**
17	**+3.3V**	SCL	SDA	**GND**	~PERR	**GND**
16	~DEVSEL	**GND**	VIO	~STOP	~LOCK	**GND**
15	**+3.3V**	~FRAME	~IRDY	**GND**	~TRDY	**GND**
12–14			Key area			
11	AD[18]	AD[17]	AD[16]	**GND**	C/~BE[2]	**GND**
10	AD[21]	**GND**	**+3.3V**	AD[20]	AD[19]	**GND**
9	C/~BE[3]	IDSEL	AD[23]	**GND**	AD[22]	**GND**
8	AD[26]	**GND**	VIO	AD[25]	AD[24]	**GND**
7	AD[30]	AD[29]	AD[28]	**GND**	AD[27]	**GND**
6	~REQ0	**GND**	**+3.3V**	CLK	AD[31]	**GND**
5	BRSV	BRSV	~RST	**GND**	~GNT0	**GND**
4	Vsm	~HEALTHY	VIO	INTP	NC	**GND**
3	~INTA	~INTB	~INTC	**+5V**	~INTD	**GND**
2	NC	**+5V**	NC	NC	NC	**GND**
1	5V	**–12V**	~SM_INTR/~TRST[17]	**+12V**	5V	**GND**

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J2 connector

The CompactPCI J2 connector is a female 2mm-pitch 6 column by 22 row right angle Hard Metric (HM) connectorCompactPCI J2 Connector

Table D-2. CompactPCI J2 connector

Pin	A	B	C	D	E	F (9)
22	GA4	GA3	GA2	GA1	GA0	**GND**
21	CLK6	**GND**	RSV	RSV	RSV	**GND**
20	CLK5	**GND**	RSV	**GND**	RSV	**GND**
19	**GND**	**GND**	NC	NC	~ALERT	**GND**
18	BRSV	BRSV	BRSV	**GND**	BRSV	**GND**
17	BRSV	**GND**	~PRST	~REQ6	~GNT6	**GND**
16	BRSV	BRSV	~DEG	**GND**	BRSV	**GND**
15	BRSV	**GND**	~FAL	~REQ5	~GNT5	**GND**
14	AD[35]	AD[34]	AD[33]	**GND**	AD[32]	**GND**
13	AD[38]	**GND**	VIO	AD[37]	AD[36]	**GND**
12	AD[42]	AD[41]	AD[40]	**GND**	AD[39]	**GND**
11	AD[45]	**GND**	VIO	AD[44]	AD[43]	**GND**
10	AD[49]	AD[48]	AD[47]	**GND**	AD[46]	**GND**
9	AD[52]	**GND**	VIO	AD[51]	AD[50]	**GND**
8	AD[56]	AD[55]	AD[54]	**GND**	AD[53]	**GND**
7	AD[59]	**GND**	VIO	AD[58]	AD[57]	**GND**
6	AD[63]	AD[62]	AD[61]	**GND**	AD[60]	**GND**
5	C/~BE[5]	**GND**	VIO	C/~BE[4]	PAR64	**GND**
4	VIO	BRSV	C/~BE[7]	**GND**	C/~BE[6]	**GND**
3(3)	CLK4	**GND**	~GNT3	~REQ4	~GNT4	**GND**
2(3)	CLK2	CLK3	~SYSEN	~GNT2	~REQ3	**GND**
1(3)	CLK1	**GND**	~REQ1	~GNT1	~REQ2	**GND**

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J3 connector

The J3 connector is a user-defined connector that routes T1/E1 and Ethernet signal pairs and LED controls to the RTM for specific use with the 8-port Serial 2-port Ethernet RTM.

J3 provides the interface for PCI Ethernet signaling and LED control as well as IX Ethernet signaling and LED control.

The four connections, labeled CAP:RTMn and CPLD:RTMn respectively, are reserved; no functions are programmed into these devices.

Table D-3. CompactPCI J3 connector

Pin	A	B	C	D	E	F
19	RTM_ID[0]	RTM_ID[1]	~ENETA:LNK_LED	RTM_ID[2]	**+5V**	**GND**
18	LPa_DA+	LPa_DA–	**GND**	LPa_DC+	LPa_DC–	**GND**
17	LPa_DB+	LPa_DB–	**GND**	LPa_DD+	LPa_DD–	**GND**
16	LPb_DA+	LPb_DA–	**GND**	LPb_DC+	LPb_DC–	**GND**
15	LPb_DB+	LPb_DB–	**GND**	LPb_DD+	LPb_DD–	**GND**
14	**+3.3V**	**+3.3V**	**+3.3V**	**+5V**	**+5V**	**GND**
13	PMCB:IO5	PMCB:IO4	PMCB:IO3	PMCB:IO2	PMCB:IO1	**GND**
12	PMCB:IO10	PMCB:IO9	PMCB:IO8	PMCB:IO7	PMCB:IO6	**GND**
11	PMCB:IO15	PMCB:IO14	PMCB:IO13	PMCB:IO12	PMCB:IO11	**GND**
10	PMCB:IO20	PMCB:IO19	PMCB:IO18	PMCB:IO17	PMCB:IO16	**GND**
9	PMCB:IO25	PMCB:IO24	PMCB:IO23	PMCB:IO22	PMCB:IO21	**GND**
8	PMCB:IO30	PMCB:IO29	PMCB:IO28	PMCB:IO27	PMCB:IO26	**GND**
7	PMCB:IO35	PMCB:IO34	PMCB:IO33	PMCB:IO32	PMCB:IO31	**GND**
6	PMCB:IO40	PMCB:IO39	PMC:1O38	PMCB:IO37	PMCB:IO36	**GND**
5	PMCB:IO45	PMCB:IO44	PMCB:IO43	PMCB:IO42	PMCB:IO41	**GND**
4	PMCB:IO50	PMCB:IO49	PMCB:IO48	PMCB:IO47	PMCB:IO46	**GND**
3	PMCB:IO55	PMCB:IO54	PMCB:IO53	PMCB:IO52	PMCB:IO51	**GND**
2	PMCB:IO60	PMCB:IO59	PMCB:IO58	PMCB:IO57	PMCB:IO56	**GND**
1	~ENETB:LNK_LED	PMCB:IO64	PMCB:IO63	PMCB:IO62	PMCB:IO61	**GND**

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J5 connector

J5 provides the connection for all T1/E1 pairs and LED control from PMC connector Jn4. J5 also provides connection paths between the RTM and the TDM2IX and the CPLD.

The four connections, labeled CAP:RTMn and CPLD:RTMn respectively, are reserved; no functions are programmed into these devices.

Table D-4. CompactPCI J5 connector

Pin	A	B	C	D	E	F
22	~ENETA:100_LED	~ENETA:1000_LED	KBD_DAT	IDE_INTR	~IDE_RSTDRV	**GND**
21	~ENETB:100_LED	~ENETB:1000_LED	KBD_CLK	~IDE_DACK	~IDE_CS1	**GND**
20	COM_TXD	USB_DAT+	USB_DAT–	IDE_IORDY	~IDE_CS3	**GND**
19	COM_RXD	**+5V**	M_DAT	~IDE_IOW	IDE_DREQ	**GND**
18	~COM_RTS	~COM_CTS	M_CLK	~IDE_IOR	IDE_A2	**GND**
17	~IDE_PDIAG	~IDE_DASP	IDE_D15	IDE_A0	IDE_A1	**GND**
16	IDE_D10	IDE_D11	IDE_D12	IDE_D13	IDE_D14	**GND**
15	IDE_D5	IDE_D6	IDE_D7	IDE_D8	IDE_D9	**GND**
14	IDE_D0	IDE_D1	IDE_D2	IDE_D3	IDE_D4	**GND**
13	PMCA:IO5	PMCA:IO4	PMCA:IO3	PMCA:IO2	PMCA:IO1	**GND**
12	PMCA:IO10	PMCA:IO9	PMCA:IO8	PMCA:IO7	PMCA:IO6	**GND**
11	PMCA:IO15	PMCA:IO14	PMCA:IO13	PMCA:IO12	PMCA:IO11	**GND**
10	PMCA:IO20	PMCA:IO19	PMCA:IO18	PMCA:IO17	PMCA:IO16	**GND**
9	PMCA:IO25	PMCA:IO24	PMCA:IO23	PMCA:IO22	PMCA:IO21	**GND**
8	PMCA:IO30	PMCA:IO29	PMCA:IO28	PMCA:IO27	PMCA:IO26	**GND**
7	PMCA:IO35	PMCA:IO34	PMCA:IO33	PMCA:IO32	PMCA:IO31	**GND**
6	PMCA:IO40	PMCA:IO39	PMCA:1O38	PMCA:IO37	PMCA:IO36	**GND**
5	PMCA:IO45	PMCA:IO44	PMCA:IO43	PMCA:IO42	PMCA:IO41	**GND**
4	PMCA:IO50	PMCA:IO49	PMCA:IO48	PMCA:IO47	PMCA:IO46	**GND**
3	PMCA:IO55	PMCA:IO54	PMCA:IO53	PMCA:IO52	PMCA:IO51	**GND**
2	PMCA:IO60	PMCA:IO59	PMCA:IO58	PMCA:IO57	PMCA:IO56	**GND**
1	~RTM_PRSNT[1]	PMCA:IO64	PMCA:IO63	PMCA:IO62	PMCA:IO61	**GND**

[1] This pin is GND on the RTM.

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PMC connectors

Jn1 connector

Table D-5. Jn1 connector (PMC 32-bit PCI interface)

Pin	Signal	Pin	Signal
01	No connect	02	No connect
03	**GND**	04	No connect
05	No connect	06	No connect
07	:~BUSMODE1 (Low)	08	**VCC**
09	No connect	10	No connect
11	**GND**	12	**+3.3V**
13	LPCI:CLK	14	**GND**
15	**GND**	16	PC/PCIDMA~GNT
17	PC/PCIDMA~REQ	18	**VCC**
19	No connect	20	LPCI:AD[31]
21	LPCI:AD[28]	22	LPCI:AD[27]
23	LPCI:AD[25]	24	**GND**
25	**GND**	26	LPCI:C/~BE[3]
27	LPCI:AD[22]	28	LPCI:AD[21]
29	LPCI:AD[19]	30	**VCC**
31	No connect	32	LPCI:AD[17]
33	LPCI:~FRAME	34	**GND**
35	**GND**	36	LPCI:~IRDY
37	LPCI:~DEVSEL	38	**VCC**
39	**GND**	40	LPCI:~LOCK
41	LPCI:~SDONE	42	LPCI:~SBO
43	LPCI:PAR	44	**GND**
45	No connect	46	LPCI:AD[15]
47	LPCI:AD[12]	48	LPCI:AD[11]
49	LPCI:AD[09]	50	**VCC**
51	**GND**	52	LPCI:C/~BE[0]
53	LPCI:AD[22]	54	LPCI:AD[05]
55	LPCI:AD[22]	56	**GND**
57	No connect	58	LPCI:AD[22]
59	LPCI:AD[02]	60	LPCI:AD[22]
61	LPCI:AD[00]	62	**VCC**
63	**GND**	64	No connect

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Jn2 connector

Table D-6. Jn2 connector (PMC 32-bit PCI interface)

Pin	Signal	Pin	Signal
01	No connect	02	No connect
03	No connect	04	No connect
05	No connect	06	**GND**
07	**GND**	08	No connect
09	SIRQ[1]	10	No connect
11	~BUSMODE2 (N/C)	12	**+3.3V**
13	LPCI:~RST	14	~BUSMODE3 (N/C)
15	**+3.3V**	16	~BUSMODE4 (N/C)
17	No connect	18	**GND**
19	LPCI:AD[30]	20	LPCI:AD[29]
21	**GND**	22	LPCI:AD[26]
23	LPCI:AD[24]	24	**+3.3V**
25	IDSEL	26	LPCI:AD[23]
27	**+3.3V**	28	LPCI:AD[20]
29	LPCI:AD[18]	30	**GND**
31	LPCI:AD[16]	32	LPCI:C/~BE[2]
33	**GND**	34	No connect
35	LPCI:~TRDY	36	**+3.3V**
37	**GND**	38	LPCI:~STOP
39	LPCI:~PERR	40	**GND**
41	**+3.3V**	42	LPCI:~SERR
43	LPCI:C/~BE[1]	44	**GND**
45	LPCI:AD[14]	46	LPCI:AD[13]
47	**GND**	48	LPCI:AD[10]
49	LPCI:AD[08]	50	**+3.3V**
51	LPCI:AD[07]	52	No connect
53	**+3.3V**	54	No connect
55	No connect	56	**GND**
57	No connect	58	No connect
59	**GND**	60	No connect
61	No connect	62	**+3.3V**
63	**GND**	64	~RadiSys_EN

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Serial port

This connector is used on the I/O panels of both the EPC-3311 main board and on the EPC3311-RTML. The pin signals for the EPC-3311 connector are listed in the next table. The pin signals for the EPC-3311-RTML and EPC-3311-RTM216 are listed in *Table 6-9, RS-232 RTM connector* on page 76.

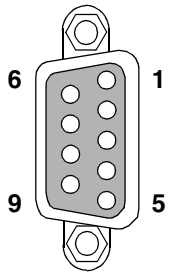
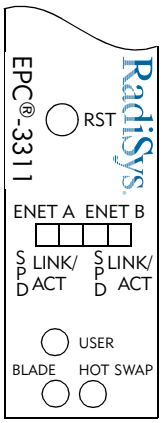


Table D-7. Serial port connector

Pin	Signal	Pin	Signal
1	DCD	6	DSR
2	Receive data (in)	7	Request to send (out)
3	Transmit data (out)	8	Clear to send (in)
4	DTR	9	No connect
5	Ground		

LEDs

Front panel



LED	No.	Link ports	Color	Purpose	State	Status
Link/activity					Off	No Link
					Blink	Link, activity
					On	Link, no activity
Speed					Off	10 Mbps
					Yellow	100 Mbps
					Green	1000 Mbps
User or software status (USER)	1		Green	Determined by BIOS, OS, or application.	On	Normal operation[1]
			Amber		On	Transitional[1]
			Red		On	Fault[1]
Blade status (BLADE)	1		Green		On	Normal operation
			Amber (red and green)		On	Transitional
			Red		On	Fault
			All colors		Blink	Active PER (ESM31XX only)
Hot Swap status (HOT SWAP)	1		Blue		On	Removal from chassis authorized

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IDE header (internal)

The secondary IDE connector is a male 44-pin 2x22, 0.1" pitch connector located on the EPC-3311 which provides a connection point for a hard-disk ribbon cable.

The pins and signals are defined as:

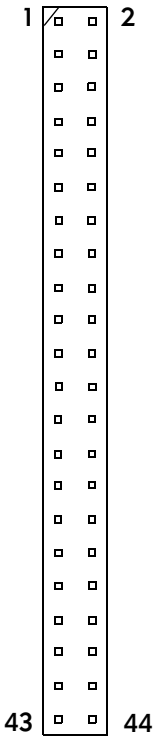


Table D-8. Primary IDE connector

Pin	Signal	Pin	Signal
1	IDE:~RST	2	**GND**
3	IDE:D7	4	IDE:D8
5	IDE:D6	6	IDE:D9
7	IDE:D5	8	IDE:D10
9	IDE:D4	10	IDE:D11
11	IDE:D3	12	IDE:D12
13	IDE:D2	14	IDE:D13
15	IDE:D1	16	IDE:D14
17	IDE:D0	18	IDE:D15
19	**GND**	20	Key
21	IDE:DRQ	22	**GND**
23	IDE:~IOW	24	**GND**
25	IDE:~IOR	26	**GND**
27	IDE:IORDY	28	IDE:CSEL
29	IDE:~DAK	30	**GND**
31	IDE:IRQ	32	No connect
33	IDE:A1	34	PDIAG
35	IDE:A0	36	IDE:A2
37	IDE:~CS1	38	IDE:~CS3
39	No connect	40	**GND**
41	**+5 V**	42	**+5V**
43	**GND**	44	No connect

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CompactFlash socket

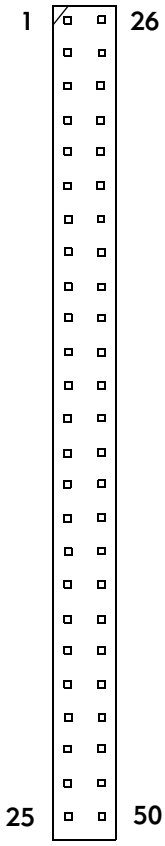


Table D-9. CompactFlash socket pinout

Pin	Signal	Type	Pin	Signal	Type
1	**GND**	Ground	26	–CD1	O
2	D03	I/O	27	D11	I/O
3	D04	I/O	28	D12	I/O
4	D05	I/O	29	D13	I/O
5	D06	I/O	30	D14	I/O
6	D07	I/O	31	D15	I/O
7	-CE1	I	32	–CE2I	I
8	A10	I	33	–VS1	NC
9	**-OE**	Ground	34	–IORD	I
10	A09	I	35	–IOWR	I
11	A08	I	36	–WE	I
12	A07	I	37	RDY/BSY	O
13	**VCC**	Power	38	**VCC**	Power
14	A06	I	39	–CSEL	I
15	A05	I	40	–VS2	NC
16	A04	I	41	RESET	I
17	A03	I	42	–WAIT	O
18	A02	I	43	–INPACK	NC
19	A01	I	44	–REG	I
20	A00	I	45	BVD2	I/O
21	D00	I/O	46	BVD1	I/O
22	D01	I/O	47	D08	I/O
23	D02	I/O	48	D09	I/O
24	WP	O	49	D10	I/O
25	**–CD2**	Ground	50	**GND**	Ground

Reset button

The reset is a momentary push-button recessed switch. It is available on the front panel to manually force reset.

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E Messages

This appendix lists the Phoenix BIOS 4.06 standard POST error codes which can generate console messages.

Table E-1. POST message codes

Class	Number	Name
Disk errors	200h	ERR_DISK_FAILED
Keyboard errors	210h	ERR_KBD_STUCK
	211h	ERR_KBD_FAILED
	212h	ERR_KBD_KCFAIL
	213h	ERR_KBD_LOCKED
Video errors	220h	ERR_VIDEO_SWITCH
Memory errors	230h	ERR_SYS_MEM_FAIL
	231h	ERR_SHAD_MEM_FAIL
	232h	ERR_EXT_MEM_FAIL
	233h	ERR_MEM_TYPE_MIX
	234h	ERR_MEM_ECC_SINGLE
	235h	ERR_MEM_ECC_MULTIPLE
	236h	ERR_MEM_DECREASED
	237h	ERR_DMI_MEM_FAIL
POS/timeout errors	240h	ERR_POS
CMOS errors	250h	ERR_CMOS_BATTERY
	251h	ERR_CMOS_CHECKSUM
Timer errors	260h	ERR_TIMER_FAILED
Real time clock errors are x70h	270h	ERR_RTC_FAILED
Invalid date/time	271h	ERR_RTC_INV_DATE_TIME
Configuration errors	280h	ERR_CONFIG_FAILED
	281h	ERR_CONFIG_MEMORY
NVRAM errors	290h	ERR_NVRAM
Diskette errors	2B0h	ERR_FLOPPYA_FAILED
	2B1h	ERR_FLOPPYB_FAILED
	2B2h	ERR_FLOPPYA_INCORRECT
	2B3h	ERR_FLOPPYB_INCORRECT
Load errors	2C0h	ERR_LOADED
Cache errors	2D0h	ERR_CACHE_FAILED

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Table E-1. POST message codes

Class	Number	Name
I/O errors	2E0h	ERR_IO_ADDRESS
	2E1h	ERR_IO_COM
	2E2h	ERR_IO_LPT
	2E3h	ERR_IO_CONFLICT
	2E4h	ERR_IO_UNSUPPORTED
	2E5h	ERR_IO_IRQ
	2E6h	ERR_IO_IDE
	2E7h	ERR_IO_FDD
Other errors	2F0h	ERR_OTHER_CPUID
	2F1h	ERR_OTHER_BIST
	2F2h	ERR_OTHER_BSP
	2F3h	ERR_OTHER_AP
	2F4h	ERR_OTHER_CMOS
	2F5h	ERR_OTHER_DMA
	2F6h	ERR_OTHER_NMI
	2F7h	ERR_OTHER_FAILSAFE

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F PMC modules

The EPC-3311 supports either one or two PCI mezzanine card (PMC) modules for a variety of task processing applications.

You cannot install a Processor PMC (such as the EPC-6315) the PMC A/B site when a CompactFlash is installed.

PMC modules have integral connectors that plug into slots on the EPC-3311. Standoffs are built into the PMC to separate the components of the PMC module from the processor board. Do not change the length of the standoffs.

Avoid causing ESD (electrostatic discharge) damage:

- Keep the card in its anti-static bag until you are ready to install.
- Install the card (as described later in this chapter) only in a static-free environment:
  - Wear an antistatic wrist strap attached to a known ground such as an antistatic lab mat.

    Um unbeabsichtigte Schäden durch elektrostatische Entladung vorzubeugen, sollte bei Arbeiten am System immer ein Erdungsarmband getragen oder andere elektrostatische Entladungs-Vorsichtsmaßnahmen verwendet werden.
  - Remove the card from its antistatic bag only in a static-free environment.
  - Avoid touching printed circuits, connector pins, and components. Where possible, hold the card only by its edges or mounting hardware.
  - Make the least possible movement with your body to minimize electrostatic charges created by contact with clothing fibers, carpet, and furniture.
  - Keep one hand on the computer chassis, if possible, as you insert or remove a card.
  - Avoid placing the card on the chassis cover or on a metal table. The cover and metal table increase the risk of damage because they provide an electrical path from your body through the card.

The PMC module, like most other electronic devices, is susceptible to ESD damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

Installing a PMC module on the main board

To install a PMC module:

1. Remove the EPC-3311 from the chassis as described in *Extracting the EPC-3311* on page 15.

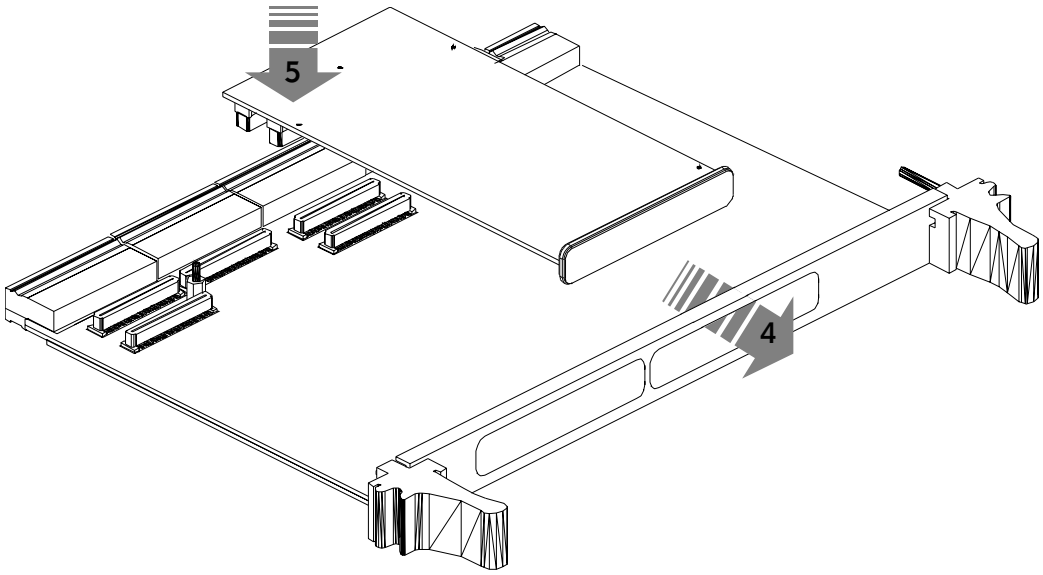
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2. Decide which PMC slot to use: slot A or slot B.

   You can install only one device in each PMC slot. When an HDD is installed in slot A, you cannot install a PMC in that slot.

3. Remove and save the blank face plate from the PMC slot in the EPC-3311 face plate.
4. Position the PMC bezel through the PMC slot on the front panel.
5. Push the rear connectors into the main board.

Figure F-1. Installing a PMC module



6. Insert and tighten the four screws on the back (underside) of the main board. Use the screws that came with the PMC module.
7. Replace the EPC-3311 in the CompactPCI chassis as described in *Inserting the EPC-3311* on page 13.

   The memory heat spreader plate extends 0.011" into the 0.024" CMC component area buffer zone between PMC "B" components and baseboard components. This is not a problem as long as the PMC card used in slot "B" does not also violate this buffer zone.

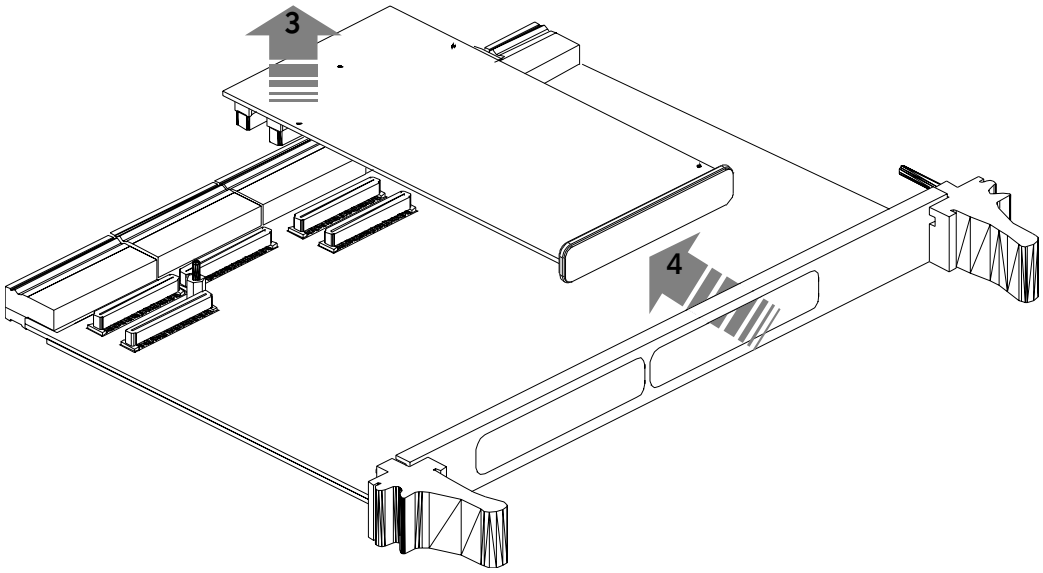
Disconnecting the PMC module

If your EPC-3311 includes an optional PMC module, you must disassemble the board before performing maintenance or upgrades on the EPC-3311.

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To separate the PMC module and the main board:

Figure F-2. Removing a PMC module



1. Remove the EPC-3311 from the CompactPCI chassis as described in *Extracting the EPC-3311* on page 15.
2. Remove screws on the back of the main board.
3. Pull the rear connectors off the main board. Continue applying force until the connectors completely disengage.
4. Retract the PMC bezel from the PMC slot on the front panel.

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G CompactFlash cards

The CompactFlash card is located on the EPC-3311 beneath the PMC "A" or hard disk drive slot.

- The CompactFlash card must be installed before installing a PMC or a hard drive in the PMC "A" slot.
- You cannot install a Processor PMC (such as the EPC-6315) the PMC A/B site when a CompactFlash is installed.

Avoid causing ESD (electrostatic discharge) damage:

- Keep the card in its anti-static bag until you are ready to install.
- Install the card (as described later in this chapter) only in a static-free environment:
  - Wear an antistatic wrist strap attached to a known ground such as an antistatic lab mat.

    Um unbeabsichtigte Schäden durch elektrostatische Entladung vorzubeugen, sollte bei Arbeiten am System immer ein Erdungsarmband getragen oder andere elektrostatische Entladungs-Vorsichtsmaßnahmen verwendet werden.
  - Remove the card from its antistatic bag only in a static-free environment.
  - Avoid touching printed circuits, connector pins, and components. Where possible, hold the card only by its edges or mounting hardware.
  - Make the least possible movement with your body to minimize electrostatic charges created by contact with clothing fibers, carpet, and furniture.
  - Keep one hand on the computer chassis, if possible, as you insert or remove a card.
  - Avoid placing the card on the chassis cover or on a metal table. The cover and metal table increase the risk of damage because they provide an electrical path from your body through the card.

The EPC-3311, like most other electronic devices, is susceptible to ESD damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

To install the CompactFlash card onto the EPC-3311, slide the CompactFlash card into the slot as shown in the figure below.

To install the CompactFlash card:

1. Turn off the power.
2. Remove the EPC-3311 from the chassis as described in *Extracting the EPC-3311* on page 15.

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3. If your EPC-3311 includes an option and it prevents you from accessing the CompactFlash socket, disassemble the board as described in *Dis-assembling the EPC-3311* on page 16.
4. Locate the CompactFlash socket on the board.
5. If your upgrade requires removal of existing CompactFlash card, pull slowly and parallel to the board to extract the CompactFlash card from the socket.
6. Add the CompactFlash card by sliding the edge fingers into the socket at almost a horizontal level, ensuring that the module is fully home.:

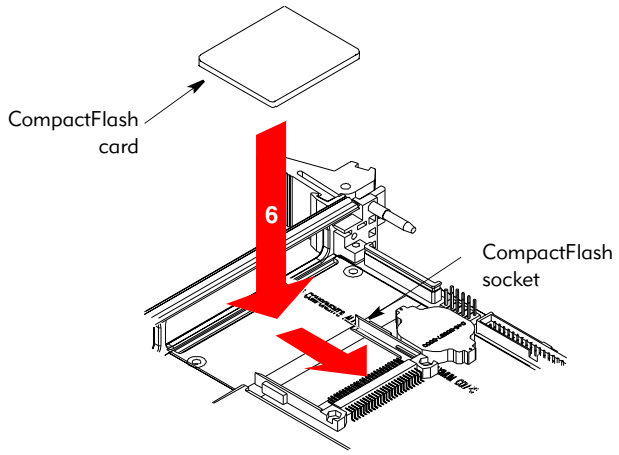


Figure G-1. Inserting a CompactFlash card

7. If your EPC-3311 includes an option, re-assemble the board as described in *Re-assembling the EPC-3311* on page 17.
8. Replace the EPC-3311 in the chassis as described in *Inserting the EPC-3311* on page 13.

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H FPGA features register set

Register	(RS)D7	(RS)D6	(RS)D5	(RS)D4	(RS)D3	(RS)D2	(RS)D1	(RS)D0	Port
BIOS Control/Status	IDE_RST	ISO_RTM	HDD_ Master	~HDD_ Present	~CF_ Present	ROM_ TOP	RSVD	RSVD	0x100
FPGA RSI (Register Set Index)	RSVD	RSVD	RSVD	RSVD	NDX3	NDX2	NDX1	NDX0	0x185
FPGA Register Set Data Port	RSD7	RSD6	RSD5	RSD4	RSD3	RSD2	RSD1	RSD0	0x187
Index 04— Reset Event	RSVD	PRST	POR	H8	FP	RSVD	CPCI_SYS	ITP	0x04
Index 05—Local Interrupt Control/Status	RSVD	ENUM_ IRQ_EN	ENUM_ IRQ	LAT_ IRQ_EN	LAT_IRQ	Bd Reset En	IBR_ IRQ_EN	IBR_IRQ	0x05
Index 06— Reset Control	RSVD	PRST_SEL	RSVD	HMC_SEL	FP_SEL	SYS_EN	CPCI_SYS _SEL	ITP_SEL	0x06
EPC-3311 General Purpose Control	RSVD	RSVD	LATCH	ENUM	RSVD	RSVD	Flash_Size[1..0]		0x07
Index 08—Boot ROM Access Control	Seg_ En_F/E	Seg_ En_D/C	Seg_ En_B/A	RSVD	RSVD	RSVD	RSVD	RSVD	0x08
Index 09—Reserved	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x09
Index 0A—ROM Program Control	BIOS_ WE	FL_PGM_ EN	BB_WEN	RSVD	RSVD	RSVD	RSVD	RSVD	0x0A

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BIOS Control/Status register (0x100)

0x100	D7	D6	D5	D4	D3	D2	D1	D0
	IDE_RST	ISO_RTM	HDD_ Master	~HDD_ Present	~CF_ Present	ROM_ TOP	RSVD	RSVD
Access:	R/W	R/W	R/W	R	R	R	R	R
POR	0	0	1	–	–	–	1	0

IDE_RST A read/write bit that asserts the output ~IDE_RST low when set to 1.

ISO_RTM Routes the EIDE bus. Values for this read/write bit include:

1 Routes to local devices.

0 Routes to RTM devices.

HDD_Master

Sets the master. Values for this read/write bit include:

1 Sets the local HDD as the master.

0 Sets the CompactFlash as the master.

~HDD_Present

Indicates whether an HDD (Hard Disk Drive) is present. Values for this read-only bit include:

1 An HDD is not installed.

0 An HDD is installed.

~CF_Present

Indicates whether a Compact Flash is present. Values for this read-only bit include:

1 A Compact Flash is not installed.

0 A Compact Flash is installed.

ROM_TOP

Reflects the ROM_TOP jumper's state. Values for this read-only bit include:

1 ROM reads access the lower-half of the ROM's top 1Mbyte.

0 ROM reads start at the top-half of the ROM's top 1Mbyte.

For information about this jumper, see *ROM_TOP (J7)* on page 12.

RSVD Reserved for internal use.

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FPGA RSI (Register Set Index) register (0x185)

	D7	D6	D5	D4	D3	D2	D1	D0
0x185	RSVD	RSVD	RSVD	RSVD	NDX3	NDX2	NDX1	NDX0
Access:	R	R	R	R	R/W	R/W	R/W	R/W
POR	0	0	0	0	1	0	1	0

RSVD Reserved for future use. These read-only bits always return a 0 (zero).

NDX[3..0] Selects the active FPGA Features register. The combined NDX bits provide this 4-bit index register.

FPGA Register Set Data Port register (0x187)

	D7	D6	D5	D4	D3	D2	D1	D0
0x187	RSD7	RSD6	RSD5	RSD4	RSD3	RSD2	RSD1	RSD0
Access:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

RSD[7..0] Transfers register contents to the FPGA Features register identified by the contents of the RSI register. Each bit of the transfer is subject to the read/write accessibility limitations of the associated bit in the target FPGA Features register. When read, this port's contents are those of the target FPGA Features register.

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Index 04—Reset Event register (0x04)

	RSD7	RSD6	RSD5	RSD4	RSD3	RSD2	RSD1	RSD0
0x04	RSVD	PRST	POR	H8	FP	RSVD	CPCI_SYS	ITP
Access:	R	R/WC	R/WC	R/WC	R/WC	R	R/WC	R/WC
POR	0	0	1	0	0	0	0	0

This register determines the source of the last reset. These bits are set when their associated input pin is detected at the active level. The action of each event is accumulative and does not change the setting of the other bits. Writing a 1 to the bit location clears the bit to a 0 (zero).

RSVD Reserved for future use. These read-only bits always return a 0 (zero).

PRST Indicates the CompactPCI pin ~PRST state. Values for this read/write-clear bit include:

- 1 ~PRST reset asserted.
- 0 ~PRST reset did not assert.

POR Indicates the board power's state. Values for this read/write-clear bit include:

- 1 The board's power cycled.
- 0 The board's power did not cycle.

HMC Indicates whether H8 asserted reset. Values for this read/write-clear bit include:

- 1 H8 reset asserted.
- 0 H8 reset did not assert.

FP Indicates whether front panel pushbutton reset is asserted. Values for this read/write-clear bit include:

- 1 Front panel reset asserted.
- 0 Front panel reset did not assert.

CPCI_SYS Indicates whether the EPC-3311, when configured as a peripheral, receives a reset from the system controller. Values for this read/write-clear bit include:

- 1 The system controller reset the board.
- 0 The system controller did not reset the board.

ITP Indicates whether the ITP issued a reset. Values for this read/write-clear bit include:

- 1 ITP issued a reset.
- 0 ITP did not issue a reset..

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Index 05—Local Interrupt Control/Status register (0x05)

0x05	D7	D6	D5	D4	D3	D2	D1	D0
	RSVD	ENUM_ IRQ_EN	ENUM_ RQ	LAT_ IRQ_EN	LAT_IRQ	Bd Reset En	IBR_ IRQ_EN	IBR_IRQ
Access:	R	R/W	R/WC	R/W	R/WC	R/W	R/W	R/WC
POR/PCI_RST	0	0	0	0	0	0	0	0

The interrupt sources from the FPGA (~ENUM, LATCH, interrupt before reset) are routed to PCI interrupt PIRQD. Unlike PCI devices these FPGA features do not have a PCI Header or PCI Interrupt Line mailbox containing the associated ISA IRQ number. A device driver or software that uses these interrupt features can discover which ISA IRQ the PCI interrupt is routed to by examining bits 3:0 of the RadiSys 82600 LIRQRC[D] Route Control Register at PCI configuration space offset 0xA3 of device 0 function 0. For detailed information about this register, see the 82600 High Integration Dual PCI System Controller Databook.

RSVD Reserved for future use. These read-only bits always return a 0 (zero).

ENUM_IRQ_EN
Determines whether an interrupt occurs when ~ENUM asserts. Values for this read/write bit include:

1 An interrupt occurs when ~ENUM asserts.

0 No interrupt occurs when ~ENUM asserts.

ENUM_IRQ
Determines whether ~ENUM assertion caused the interrupt. Values for this read/write-clear bit include:

1 ~ENUM caused an interrupt.

0 ~ENUM did not cause the interrupt.

LAT_IRQ_EN
Determines whether an interrupt occurs when the eject handle opens. Values for this read/write bit include:

1 An interrupt occurs when the eject handle opens.

0 No interrupt occurs when the eject handle opens.

LAT_IRQ Determines whether opening the lower front panel eject handle caused the interrupt. Values for this read/write-clear bit include:

1 The opened eject handle caused an interrupt.

0 The opened eject handle did not cause an interrupt.

Bd Reset En
Determines whether a reset occurs after a reset source generates an interrupt. For details about reset sources, see *Index 04—Reset Event register (0x04)* on page 114. Values for this read/write bit include:

1 A reset occurs after IBR_IRQ asserts.

0 A reset does not occur after IBR_IRQ asserts

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IBR_IRQ_EN
Determines whether an interrupt occurs when IBR_IRQ asserts. Values for this read/write bit include:

1 An interrupt occurs when IBR_IRQ asserts.

0 No interrupt occurs when IBR_IRQ asserts.

IBR_IRQ Determines whether an IBR_IRQ caused the interrupt. Values for this read/write-clear bit include:

1 The IBR_IRQ caused an interrupt.

0 The IBR_IRQ did not cause the interrupt.

Index 06—Reset Control register (0x06)

0x06	RSD7	RSD6	RSD5	RSD4	RSD3	RSD2	RSD1	RSD0
	RSVD	PRST_SEL	RSVD	HMC_SEL	FP_SEL	SYS_EN	CPCI_SYS_SEL	ITP_SEL
Access:	R	R/W	R	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

RSVD Reserved for future use. These read-only bits always return a 0 (zero).

PRST_SEL Determines what occurs when the CompactPCI ~PRST pin asserts. Values for this read/write bit include:

1 An IBR interrupt request (IBR_IRQ).

0 A board reset.

HMC_SEL Determines what occurs when an H8 reset asserts. Values for this read/write bit include:

1 An IBR interrupt request (IBR_IRQ).

0 A board reset.

FP_SEL Determines what occurs when the front-panel reset asserts. Values for this read/write bit include:

1 An IBR interrupt request (IBR_IRQ).

0 A board reset.

SYS_EN Determines what occurs when a CPCI_SYS IBR interrupt request (IBR_IRQ) asserts. Used only when the EPC-3311 is a peripheral. Values for this read/write bit include:

1 An IBR_IRQ does not occur.

0 An IBR_IRQ occurs.

CPCI_SYS_SEL
Determines what occurs when a system controller reset asserts. Used only when the EPC-3311 is a peripheral. Values for this read/write bit include:

1 An IBR_IRQ (IBR interrupt request).

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	0	A board reset.
ITP_SEL	Determines what occurs when an ITP reset asserts. Values for this read/write bit include:	
	1	An IBR interrupt request (IBR_IRQ).
	0	A board reset.

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EPC-3311 General Purpose Control register (0x07)

	RSD7	RSD6	RSD5	RSD4	RSD3	RSD2	RSD1	RSD0
0x07	RSVD	RSVD	LATCH	ENUM	RSVD	RSVD	Flash_Size[1..0]	
Access:	R	R	R	R	R	R	R	
POR/PCI_RST	0	0	X	X	0	0	XX	

LATCH Identifies the front panel latch state. Values for this read-only bit include:

1 The front panel eject handle is closed.

0 The front panel eject handle is open.

ENUM Identifies the ~ENUM state. Values for this read-only bit include:

1 ~ENUM is asserted.

0 ~ENUM is not asserted.

Flash_Size[1..0]

Indicate the size of the Boot/flash device as determined by resistor stuff options at build time. Values for these read-only bits include:

00 (4MB)
01 (8MB)
10 (16MB)
11 (32MB)

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Index 08—Boot ROM Access Control register (0x08)

	RSD7	RSD6	RSD5	RSD4	RSD3	RSD2	RSD1	RSD0
0x08	Seg_ En_F/E	Seg_ En_D/C	Seg_ En_B/A	RSVD	RSVD	RSVD	RSVD	RSVD
Access:	R/W	R/W	R/W	R	R	R	R	R
POR/PCI_RST	1	1	0	0	0	0	0	0

When the 82600 forwards memory accesses to the PCI bus, this register controls decoding of the alias region to a memory location in the ROM.

The RadiSys 82600 must be properly set for this to occur. For more information about the 82600, see the *82600 High Performance System Controller*.

Seg_En_F/E

Determines F/E access. This region, which starts at logical base address 0x000E0000, is an alias of the 128Kbyte region at 0xFFFE0000. Values for this read/write bit include:

1 Enables the ROM segment F/E control's access.

0 Disables the ROM segment F/E control's access.

Seg_En_D/C

Determines D/C access. This region, which starts at logical base address 0x000C0000, is an alias of the 128Kbyte region at 0xFFFC0000. Values for this read/write bit include:

1 Enables the ROM segment D/C control's access.

0 Disables the ROM segment D/C control's access.

Seg_En_B/A

Determines B/A access. This region, which starts at logical base address 0x000A0000, is an alias of the 128Kbyte region at 0xFFFA0000. Values for this read/write bit include:

1 Enables the ROM segment B/A control's access.

0 Disables the ROM segment B/A control's access.

RSVD Reserved for future use. These read-only bits always return a 0 (zero).

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Index 09—Reserved register (0x09)

	RSD7	RSD6	RSD5	RSD4	RSD3	RSD2	RSD1	RSD0
0x09	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Access:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR/PCI_RST	0	0	0	0	0	0	0	0

RSVD Reserved for future use. These read-only bits always return a 0 (zero).

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Index 0A—ROM Program Control register (0x0A)

	D7	D6	D5	D4	D3	D2	D1	D0
0x0A	BIOS_WE	FL_ PGM_EN	BB_WEN	RSVD	RSVD	RSVD	RSVD	RSVD
Access:	R/W	R/W	R/W	R	R	R	R	R
POR/PCI_RST	0	0	0	0	0	0	0	0

BIOS_WE Determines access for the upper 512KB of the ROM's top 1MB. Values for this read/write bit include:

1 Does not allow write access to the upper 512KB.

0 Allows write access to the upper 512KB.

FL_PGM_EN

Determines ROM access. Values for this read/write bit include:

1 Does not allow write to the ROM.

0 Allows write access to the ROM.

BB_WEN Determines access for the lower 512KB of the ROM's top 1MB. Values for this read/write bit include:

1 Does not allow write access to the lower 512KB.

0 Allows write access to the lower 512KB.



To write to the ROM's lower 512KB in the top 1MB, you must also connect pins 1 and 2 of J4 and pins 2 and 3 of J7. For information about connecting these pins, see *Setting jumpers and headers* on page 11.

RSVD Reserved for future use. These read-only bits always return a 0 (zero).

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I Re-programming the flash chip

On rare occasions, part or all of the flash chip contents may require replacement.

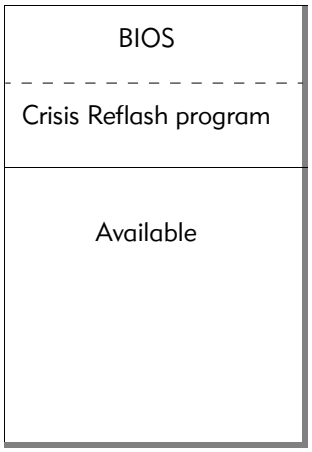
This appendix details how to update or recover your system BIOS and Crisis Reflash program. You accomplish this by re-programming all or part of the EPC-3311's flash chip.

When reading this file online, you can immediately view information about any topic by placing the mouse cursor over a task and clicking.

For information about...	Go to this page...
About the flash chip	121
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Update the BIOS program	127
Update Crisis Reflash program	127
Perform Crisis Reflash from serial port	128
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About the flash chip

Figure I-1. Flash chip memory addresses



The EPC-3311 flash chip contains these sections:

- **BIOS**: Initializes the hardware and finds a device from which to bootload. It normally resides in the upper 512KB of the top 1MB of the flash chip.

  This top 512KB block is writable when the 82600 chipset enables the memory space and a special write-enable bit in I/O space is set. You can update the BIOS using a DOS program or by activating the Crisis Reflash program.

  For details about the EPC-3311 BIOS, see *Chapter 3, BIOS configuration*.

- **Crisis Reflash program**: Performs minimal hardware setup and tries to find a file to reprogram into the System BIOS area of the flash chip.

The Crisis Reflash program resides in the lower 512KB of the top 1MB of the flash chip. This lower 512KB block is hardware-write-protected; you can't accidentally overwrite the Crisis Reflash program without inserting a special write-enable suitcase jumper.

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The rest of the flash chip is available for customer use. For more information, contact RadiSys as described in *Where to get more information* on page iv.

For details about the flash chip's sections, including addresses, see *Appendix C, Flash memory addresses*.

The location of these sections varies, depending the ROM_TOP (J7) jumper settings:

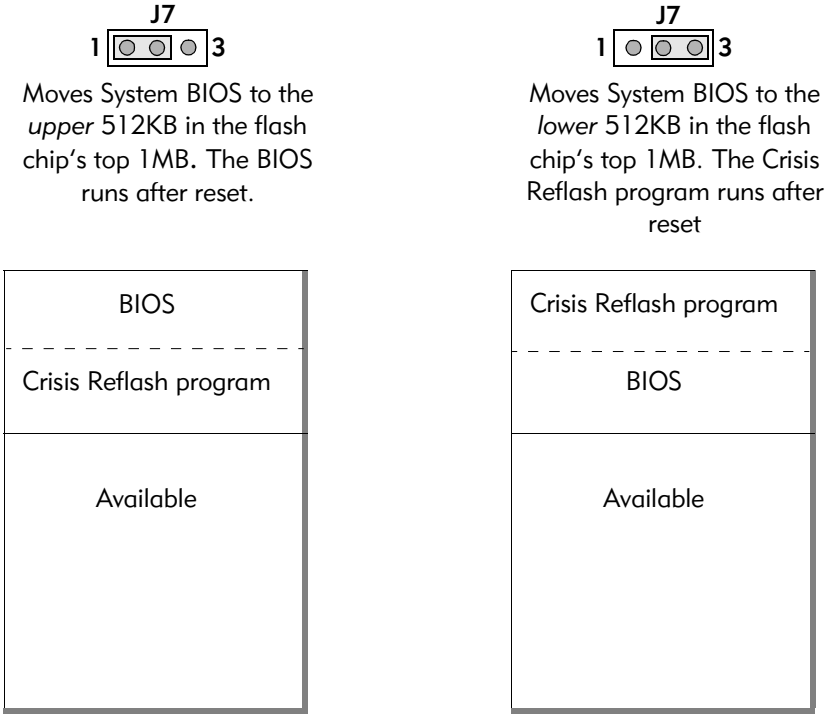


Figure I-2. Flash chip re-programming coverage

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Selecting a re-programming method

When re-programming the flash chip, use this flowchart to determine which process to use. Be sure to read *Before you begin* and *Obtain files from RadiSys* pages 124 and 125 before going to the page indicated below.

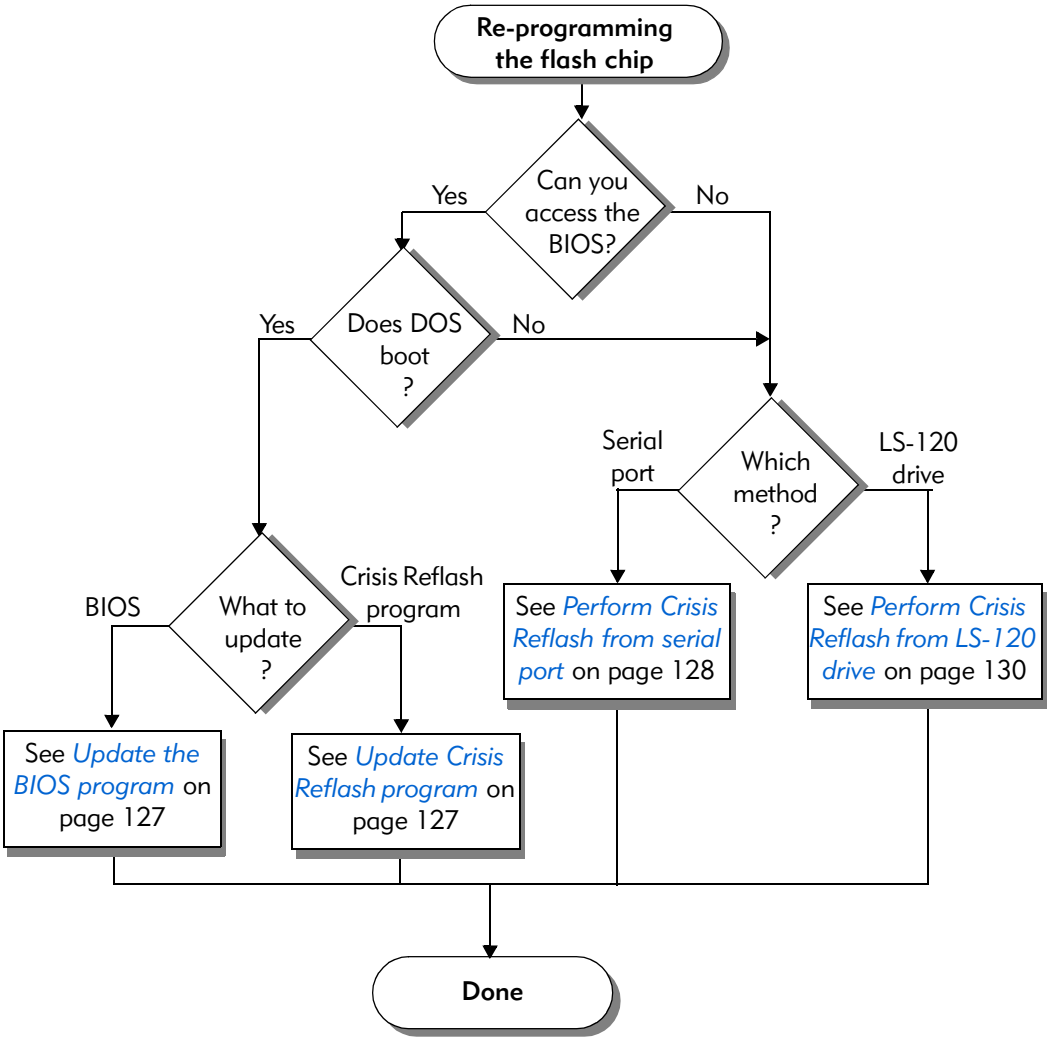


Figure I-3. Flash chip re-programming process flow

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Before you begin

- Ensure that you have the following:
  - (Optional) A RadiSys POST card.

    The EPC-3311 has a 14-pin female header, P1, which accepts a RadiSys POST card, a small PCB with two seven-segment LEDs that display the status sent to legacy PC I/O port 80h. Both phlash.exe and the BIOS send status to this port. Messages include:

    Success: 1Eh
    Failure: FFh

    For more information about obtaining a POST card, contact RadiSys as described in *Where to get more information* on page iv.
  - (Optional, but recommended) A VGA PMC.

    RadiSys recommends that you install a VGA PMC card for the BIOS update process.

    Installation of the PS/2 keyboard is optional if you have a serial console attached. You can start phlash.exe from the serial console and observe the status on the VGA monitor if you have installed a VGA PMC.

    For more information about obtaining a VGA PMC, contact RadiSys as described in *Where to get more information* on page iv.
- Decide which portion of your flash chip to re-program:
  - **BIOS**: Re-program the BIOS to fix bugs, add new features, and replace a corrupted BIOS. This is the portion of the flash chip most frequently updated. You can perform this update whether or not the BIOS can boot the system.
  - **Crisis Reflash**: Re-program Crisis Reflash when you need to replace the Crisis Reflash program. Your flash chip may require this type of update if this program requires an update or is corrupt. You can perform this update whether or not the BIOS can boot the system.

    The Crisis Reflash program block is protected by hardware. To write to this block, you must insert a jumper.
- Decide which re-programming process to use:
  - **Update the BIOS**: Use this method to re-program the BIOS from the DOS command line. RadiSys recommends this as the method that provides the most feedback during the re-programming process.

    This process is not supported on a non-DOS OS (for example: Windows NT, QNX).

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- **Update the Crisis Reflash program:** Use this method if the existing BIOS runs. RadiSys recommends this as the simplest method.

  This process is not supported on a non-DOS OS (for example: Windows NT, QNX).

- **Perform a Crisis Reflash of the BIOS:** Use this method to re-program the flash chip when you can't access the BIOS or boot to DOS. If you choose this process, you must also decide how to access the BIOS update files:
  - Serial port
  - LS-120 drive

Obtain files from RadiSys

Re-programming the flash chip requires files that contains both code to perform the task and data to place in the chip.

To obtain the files:

1. Obtain the appropriate file from RadiSys:
   - ***nnnn*updt.zip**: Select this file to update the BIOS.
   - ***nnnn*low.zip**: Select this file to update the Crisis Reflash program.
   - ***nnnn*cris.zip**: Select this file to perform a Crisis Reflash.

   The ***nnnn*** is the last four digits of the new BIOS version number.
2. Unzip the contents to a directory on your hard drive.

   When unzipped, verify that these files required to re-program the flash chip are copied successfully to your hard drive:

Filename	Description
readme.txt	Describes the transmittal and includes instructions and issues that arose too late to include in other documentation.
bios.rom	A binary file that contains the BIOS image and Boot Block.
crisboot.bin[1]	The boot sector image.
crisdisk.bat[1]	A batch file that creates the Flash Boot diskette.
makeboot.exe[1]	Creates the custom boot sector on the diskette.

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Filename	Description
phlash.exe	A 16-bit DOS program supplied by Phoenix Technologies that produces a graphic status display to the VGA console. Phlash.exe re-programs the flash chip using data from the other files. phlash.exe is a 16-bit DOS program. It cannot be used from a 32-bit Microsoft Windows command line. It has been tested on the EPC-3311 in three DOS-compatible environments. You can start phlash.exe from the serial redirection console, but the serial redirection feature may not display the graphics of phlash.exe completely.
platform.bin[2]	A file that describes the flash chip configuration, and identifies which blocks to erase and re-program. The platform.bin file contains instructions which make this a BIOS update.
minidos.sys[1]	A file that takes the place of DOS on the flash boot diskette.

[1] *nnnn*low.zip does not include these files.

[2] Do not copy or use this file elsewhere.

Now that you have the needed files, re-program your flash chip using the directions for the method you want to use:

Method	Page
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Update Crisis Reflash program	127
Perform Crisis Reflash from serial port	128
Perform Crisis Reflash from LS-120 drive	130

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Update the BIOS program

If the BIOS is working you can upgrade to a new and better BIOS by booting to 16-bit MS-DOS or a compatible DOS, like FreeDOS (http://www.freedos.org) and running an update program.

1. Ensure that you have the following:
   - The files in *nnnn*updt.zip.
   - (Optional, but recommended) An installed VGA PMC.
   - (Optional) An installed RadiSys POST card.
2. Ensure that memory managers such as HIMEM.SYS, EMS, XMS or DPMI are not loaded.

   To boot without loading memory managers, press F5 just before DOS starts. The config.sys and autoexec.bat files do not run, and memory managers do not load.

3. Go to the directory that contains phlash.exe, platform.bin and bios.rom and enter this command:

   ```
   phlash.exe
   ```

   If you installed a VGA PMC, progress displays on the VGA monitor. Follow any instructions given.

   If you do not have a VGA display and are working from the console redirection serial port, simply wait three minutes for the update to complete.

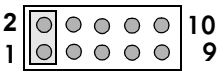
   For information about BIOS and DOS restrictions, see *DOS restrictions* on page 132.
4. Ensure that the update completed by checking the version number of the updated BIOS in the sign-on screen or BIOS Setup Main menu.

Update Crisis Reflash program

Use this method to update the Crisis Reflash program.

The Crisis Reflash program resides in the lower 512KB of the upper 1MB of FBD.

1. Ensure that you have the following:
   - The files in *nnnn*low.zip.
   - (Optional, but recommended) An installed VGA PMC.
   - (Optional) An installed RadiSys POST card.
2. Connect these J4 pins:



Pins 1 and 2 required to allows writes to the lower 512 KB of the top 1MB

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For more information about this header, see *Manufacturing header (J4)* on page 11.

3. Go to the directory that contains phlash.exe, platform.bin and bios.rom and enter this command:

   ```
   phlash.exe
   ```

   If you installed a VGA PMC, progress displays on the VGA monitor. Follow any instructions given.

   If you do not have a VGA display and are working from the console redirection serial port, simply wait three minutes for the update to complete.

   For information about BIOS and DOS restrictions, see *DOS restrictions* on page 132.

4. Ensure that the update completed by checking the version number of the updated BIOS in the sign-on screen or BIOS Setup Main menu.

5. Remove the jumper on J4 pins 1-2.

Perform Crisis Reflash from serial port

1. Ensure that you have the following:

   - The files in *nnnn*cris.zip.

     Only the file BIOS.ROM is used, but RadiSys recommends that you also copy the README.TXT file, as it has version information.

   - (Optional) An installed RadiSys POST card.

   - A 3-wire (Tx, Rx, GND) Null-Modem RS-232 serial cable.

     The Serial Reflash port is COM1 and is available either on the front panel or RTM. It has a 9-pin sub-D male connector. This is the same link as used by EPC-3311 console redirection.

     For more information about connector locations, see *RTM connectors* on page 70 or *Connectors* on page 91.

   - A host system on the other end of the serial cable.

   - A terminal emlator program that supports the XMODEM-CRC protocol running on the host system.

     The EPC-3311 does not include a host terminal emulation program; you must supply your own. RadiSys tested using HyperTerminal by Hilgrave, Inc. for Microsoft, version 5.00.2195.2722. Microsoft Windows 98, Windows NT, and Windows 2000 all supply HyperTerminal.

2. Disconnect IDE devices from the EPC-3311. This program works in the presence of some IDE devices, but not all configurations have been tested.

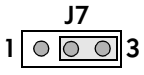
3. Connect the cable between the host system and the EPC-3311's Serial Reflash RS-232 port.

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4. Copy the bios.rom file to a location the host terminal emulation program can access.
5. Configure your host system and terminal emulation program as follows:

Baud:	38,400
Data bits:	8
Parity bits:	None
Stop bit:	8-N-1
Flow control:	None

   These settings match the System BIOS Console Redirection feature defaults.
6. Turn off the EPC-3311.
7. Connect these J7 pins:

   You must jumper pins 2 and 3 to activate the Crisis Recovery program

   For more information about this jumper, see *ROM_TOP (J7)* on page 12.
8. Power-up or reset the EPC-3311. The Crisis Reflash program runs.

   After you start the Serial Reflash, this sign-on message, which originates from the EPC-3311 Crisis Reflash program (not the host system software), displays:

```
RadiSys Flash Recovery Console, Version EPC-3311 1.0
Copyright (c) RadiSys Corporation.  All rights reserved.

Valid commands
BIOS      Reflash the System BIOS
EXIT      Exit the Flash Recovery Console
Enter Command:
```

9. Enter BIOS. A series of "C" characters display:

```
Command: BIOS

FBD Command
NOTE: Expecting File Size:  0x00080000.
Clearing DRAM:.............................
Ready to receive image
Initiate download.
CCCCCCC
```

10. As the above messages display, use the XMODEM facility of your terminal emulator to select the bios.rom file you want to download.

    For example, with Microsoft Hyperterm select Transfer>Send File and, in the Send File dialog, select the xmodem protocol and filename.

    The RadiSys Serial Reflash program does not echo download progress messages. You must rely on a progress indication from your terminal emulator program.

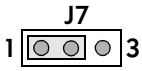
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The bios.rom file is 512KB. At 38.4K baud, the download takes about 3.5 minutes. When the download is complete, the Crisis Reflash program automatically reflashes the FBD and displays these messages:

```
Block:(MAIN BLOCK 1) Erase:Ok. Programming:Ok
Block:(MAIN BLOCK 2) Erase:Ok. Programming:Ok
Block:(MAIN BLOCK 3) Erase:Ok. Programming:Ok
Block:(MAIN BLOCK 4) Erase:Ok. Programming:Ok
Flash Update Successful!
RadiSys Flash Recovery Console, Version EPC-3311 1.0
Copyright (c) RadiSys Corporation.  All rights reserved.
Valid Commands:
    BIOS      Reflash the System BIOS
    EXIT      Exit the Flash Recovery Console

Enter Command:
```

11. Move the jumper on J7 pins back to the original position:



Re-connect pins 1 and 2 to return the header to default position.

12. Reset the system, then ensure that the update completed by checking the version number of the updated BIOS in the sign-on screen or BIOS Setup Main menu.

Perform Crisis Reflash from LS-120 drive

The EPC-3311 Crisis Reflash Program can boot and reflash from 1.44MB floppy diskette inserted in an IDE LS-120 Superdrive installed on either the on-board IDE connector or the RTM IDE connector.

1. Ensure that you have the following:
   - The files in *nnnn*cris.zip.
   - (Optional) An installed RadiSys POST card. The LS-120 crisis reflash gives no other indication of progress or completion. If you don't have a POST Card, wait 3 minutes and try the BIOS.
2. Disconnect IDE devices from all IDE connectors and busses, including devices on the MM50 and the CompactFlash.
3. Jumper the LS-120 drive as IDE Master.
4. Create a Crisis Reflash diskette:



This process is supported only on MS Windows. Linux is not supported.

   A. Insert a1.44MB 2HD IBM/DOS formatted diskette in floppy drive A: of the system where you unzipped the *nnnn*cris.zip file. Make sure the floppy is not write-protected.



Ensure that the data on the disk is either not valuable or backed up. This process will re-format the diskette and erase all previous data.

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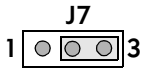
B. Run one of these programs:

crisdisk.bat	wincris.exe

1. Run wincris.exe from the command line or Explorer.
2. Ensure that Disk Options is set to "Create MiniDOS Crisis Disk".
3. Click Start. When the Format A: dialog box displays, you may elect to check the "Quick Format" checkbox.
4. Click Start, then OK. When the format finishes, close the Format A: dialog. wincris.exe copies the files.
5. Remove the diskette when prompted, then click OK.
	1. Run crisdisk.bat, either from a command line or the Explorer. The batchfile prompts you for input.
	2. Enter information as prompted. The batch file eventually displays this message:
	`QuickFormatting 1.44M`
	`Format complete.`
	`Volume label (11 characters, ENTER for none)?`
	3. Press the Enter key. The batch file displays this message:
	`Volume Serial Number is D87F-D24A`
	`QuickFormat another (Y/N)?`
	`press N.`
	The batch file copies files to the diskette and creates the special boot sector.
	4. Label the diskette:
	Recovery Diskette
	BIOS Version N.MM.LL
	Where N.MM.LL is the version number from README.TXT.

5. Boot the Crisis Reflash Diskette on the EPC-3311:

   A. Connect these J7 pins to activate the Crisis Reflash program:



You must jumper pins 2 and 3 to activate the Crisis Recovery program

For more information about this jumper, see *ROM_TOP (J7)* on page 12.

   A. Insert the special 1.44MB Crisis Reflash diskette in the LS-120 drive.

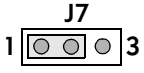
   B. Reset or power-up the EPC-3311.

   The Crisis Reflash program boots from the LS-120 drive, loads the bios.rom file, and tries to reflash the BIOS.

   C. Do one of these to ensure that boot is complete before moving to the next step:

   - Wait until the POST card indicates success by displaying "1Eh".
   - Wait three minutes.

6. Move the jumper on J7 pins back to the original position:



Re-connect pins 1 and 2 to return the header to default position.

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7. Reset the system, then ensure that the update completed by checking the version number of the updated BIOS in the sign-on screen or BIOS Setup Main menu.

DOS restrictions

Version	Comments
MS-DOS 6.22	There can be no protected mode memory management programs loaded, such as EMS, XMS or DPMI handlers. Check the config.sys and autoexec.bat files. MS-DOS 6.22 will bypass the config.sys and autoexec.bat if you press F5 when it is booting.
MS-DOS 7.x	DOS 7.x comes with Windows 9x. You must eliminate any protected mode memory managers from config.sys, autoexec.bat and dosstart.bat. A Win9x DOS 7.x command line is not a DOS box window. There are three ways to get a DOS 7.x command line. 1. From Windows GUI select Start then Shut Down then Restart the computer in MS-DOS Mode. (Make sure there are no memory management programs in c:\windows\dosstart.bat.) 2. When booting Windows press F8. The Microsoft Startup Menu should appear. Select Command Prompt Only. (Make sure there are no memory management programs in config.sys and autoexec.bat.) 3. Edit the Windows 9x c:\msdos.sys file to boot to DOS 7.x first instead of the Windows GUI. To access you must first set permissions with "attrib -r -h -s msdos.sys". Edit or add the line "BootGUI=0" under the [Options] category. Do not change the "xxxxxx" comments at the end of the file. Change the permissions back with "attrib +r +h +s msdos.sys".
FreeDOS	FreeDOS is available from http://www.freedos.org. The kernel and basic utilities are under GPL2 licence. See the site for more detail. Installation is from 1.44MB floppy media. The EPC-3311 BIOS bootloads from a 1.44MB floppy media installed in an LS-120 Superdrive IDE bus.

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Glossary

ANSI	(American National Standards Institute) An organization dedicated to advancement of national standards related to product manufacturing.
ATA	(AT Bus Attachment) An interface definition for PC peripherals. See *IDE*. An Advanced Technology Attachment drive, also known as an IDE drive, is a hard-drive with the interface built-in.
ATAPI	(AT Attachment Packet Interface) An extension to EIDE that enables support of CD-ROM, LS-120, and tape drives. The Packet interface protocol enables ATAPI devices to plug into standard IDE cable.
Autotype	A convenient method of IDE device detection whereby the system BIOS queries the IDE device to obtain operational parameters. If the device supports autotype, this information is passed to the BIOS where it is used to automatically configure the drive controller.
BDA	(BIOS Data Area) BIOS Data Area. A 256 byte block of DRAM starting at address 400h that contains data initialized and used by the System BIOS detailing the system configuration and errors encountered during POST. A PC legacy requirement.
BIOS	(Basic Input/Output System) Firmware in a PC-compatible computer that runs when the computer is powered up. The BIOS initializes the computer hardware, allows the user to configure the hardware, boots the operating system, and provides standard mechanisms that the operating system can use to access the PC's peripheral devices.
BIOS extension	An object code module that is typically integrated into the FBD or placed into a ROM that is accessible on the peripheral bus (PCI, ISA, etc.) in the address range 0C0000h through 0DFFFFh. BIOS extensions have a pre-defined header format and contain code that is used to extend the capabilities of the System BIOS.
BIOS image	Information contained in the flash boot device in binary file format consisting of initialization data, setup configuration data, diagnostic sequences, and other instructions necessary to start up a computer and prepare it to load an operating system.
BIOS update	A process whereby an existing, uncorrupted BIOS image in the flash boot device is overwritten with a new image. Also referred to as a flash update.
Bit	A binary digit.
BMC	Baseboard Management Controller.
Boot	The process of starting a computer and loading the operating system from a powered down state (cold boot) or after a computer reset (warm boot). Before the

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	operating system loads, the computer performs a general hardware initialization and resets internal registers.
Boot device	The storage device from which the computer boots the operating system.
Boot sequence	The order in which a computer searches external storage devices for an operating system to boot. The boot device must be the first in the boot sequence.
Byte	A group of 8 bits.
CAS	(Column Address Strobe) An input signal from the DRAM controller to an internal DRAM latch register specifying the column at which to read or write data. The DRAM requires a column address and a row address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of column addresses and row addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required.
Chipset	One or more integrated circuits that, along with a CPU, memory, and other peripherals, implements an IBM PC-AT compatible computer. The chipset typically implements a DRAM controller, bus, interface logic, and PC peripheral devices.
CHS	(Cylinders/Heads/Sectors) A specification of disk drive operating parameters consisting of the number of disk cylinders, disk drive read/write heads, and disk sectors.
CMOS	(Complimentary Metal Oxide Semiconductor) A fast, low power semiconductor RAM used to store system configuration data.
COM port	A bi-directional serial communication port which implements the RS-232 specification.
Conventional memory	The first 640 KB of a computer's total memory capacity. If a computer has no extended memory, conventional memory equals the total memory capacity. In typical computer systems, conventional memory can contain BIOS data, the operating system, applications, application data, and terminate and stay resident (TSR) programs. Also called system memory.
CPU	(Central Processing Unit) A semiconductor device which performs the processing of data in a computer. The CPU, also referred to as the microprocessor, consists of an arithmetic/logic unit to perform the data processing, and a control unit which provides timing and control signals necessary to execute instructions in a program.
Default	The state of all user-changeable hardware and software settings as they are originally configured before any changes are made.
DIP	(Dual In-Line Package) A semiconductor package configuration consisting of a rectangular plastic case with two rows of pins, one row on each lengthwise side.
DOS	(Disk Operating System) One or more programs which allow a computer to use a disk drive as an external storage device. These programs manage storage and retrieval of data to and from the disk and interpret commands from the computer operator.
DRAM	(Dynamic Random Access Memory) Semiconductor RAM memory devices in which the stored data does not remain permanently stored, even with the power

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	applied, unless the data are periodically rewritten into memory during a refresh operation.
Driver	A software component of the operating system which directs the computer interface with a hardware device. The software interface to the driver is standardized such that application software calling the driver requires no specific operational information about the hardware device.
ECC	(Error Checking and Correction) A chipset feature that enables it to detect single or multi-bit errors in DRAM reads and correct single bit errors.
EEPROM	(Electrically Erasable Programmable ROM) Specifically, those EPROMs which may be erased electrically as compared to other erasing methods.
ESCD	(Extended System Configuration Data) A block of nonvolatile memory that stores information on the devices found and configured by the Plug and Play BIOS.
Extended memory	The RAM address space, in a computer so equipped, above the 1 MB level.
External device	A peripheral or other device connected to the computer from an external location via an interface cable.
FBD	(Flash Boot Device) A flash memory device containing the computer's BIOS.
Fixed disk	A hard disk drive or other data storage device having no removable storage medium. Fixed disk storage devices use inflexible disk media and are sealed to prevent data loss due to media surface contamination. Fixed disks generally provide the most storage space for a given cost when compared to semiconductor, tape, and other popular mass storage technologies.
Flash memory	A fast EEPROM semiconductor memory typically used to store firmware such as the computer BIOS. Flash memory also finds general application where a semiconductor non-volatile storage device is required.
Flash update	See *BIOS update*.
FPGA	(Field Programmable Gate Array) A large, general-purpose logic device that is programmed at power-up to perform specific logic functions.
FRU	Field-Replaceable Unit. A field-replaceable unit (FRU) is part that can be quickly and easily removed and replaced by the user or by a technician without sending the entire system to a repair facility. The defective unit is found by standard troubleshooting procedures, removed, and either discarded or shipped back to the factory for repair. FRUs can minimize system downtime and optimize reliability.
GB or GByte	(Gigabyte) Approximately one billion (US) or one thousand million (Great Britain) bytes. 2^30 = 1,073,741,824 bytes exactly.
h	(Hexadecimal) A base-16 numbering system using numeric symbols 0 through 9 plus alpha characters A, B, C, D, E, and F as the 16 digit symbols. Digits A through F are equivalent to the decimal values 10 through 15.
Hang	A condition where the system microprocessor suspends processing operations due to an anomaly in the data or an illegal instruction.
Header	A mechanical pin and sleeve style connector on a circuit board. The header may exist in either a male or female configuration. For example, a male header has a

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	number and pattern of pins which corresponds to the number and pattern of sleeves on a female header plug.
HMC	(Hardware Management Controller) Describes the hardware common to the Baseboard management Controller and the Satellite Management Controller. The HMC provides the ability to monitor, quesry and log system management events on the {product name short} and in the CompactPCI system.
Host bus	The address/data bus that connects the CPU and the chipset.
I/O	(Input/Output) The communication interface between system components and between the system and connected peripherals.
IDE	(Integrated Drive Electronics) A hard disk drive/controller interface standard. IDE drives contain the controller circuitry at the drive itself, as compared to the location of this circuitry on the computer motherboard in non-IDE systems. IDE drives typically connect to the system bus with a simple adapter card containing a minimum of on-board logic.
INT	(Interrupt Request) A software-generated interrupt request.
IRQ	(Interrupt Request) In PCs, a microprocessor input from the control bus used by I/O devices to interrupt execution of the current program and cause the microprocessor to jump to a special program called the interrupt service routine. The microprocessor executes this special program, which normally involves servicing the interrupting device. When the interrupt service routine is completed, the microprocessor resumes execution of the program it was working on before the interruption occurred.
ISR	(Interrupt Service Routine) A program executed by the microprocessor upon receipt of an interrupt request from an I/O device and containing instructions for servicing of the device.
Jumper	A set of male connector pins on a circuit board over which can be placed coupling devices to electrically connect pairs of the pins. By electrically connecting different pins, a circuit board can be configured to function in predictable ways to suit different applications.
KB or KByte	(Kilobyte) Approximately one thousand bytes. 2^{10} = 1024 bytes exactly.
LBA	(Logical Block Addressing) A method the system BIOS uses to reference hard disk data as logical blocks, with each block having a specific location on the disk. LBA differs from the CHS reference method in that the BIOS requires no information relating to disk cylinders, heads, or sectors. LBA can be used only on hard disk drives designed to support it.
Logical address	The memory-mapped location of a segment after application of the address offset to the physical address.
MB or MByte	(Megabyte) Approximately one million bytes. 2^20 = 1,048,576 bytes exactly.
Memory	A designated system area to which data can be stored and from which data can be retrieved. A typical computer system has more than one memory area. See *Conventional memory* and *Extended memory*.

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Memory shadowing	Copying information from an extension ROM into DRAM and accessing it in this alternate memory location.
Offset	The difference in location of memory-mapped data between the physical address and the logical address.
OS	(Operating System) See *DOS*.
PC/AT	(Personal Computer/Advanced Technology) A popular computer design first introduced by IBM in the early 1980s.
PCI	(Peripheral Connect Interface) A popular microcomputer bus architecture standard.
Peripheral device	An external device connected to the system for the purpose of transferring data into or out of the system.
Physical address	The address or location in memory where data is stored before it is moved as memory remapping occurs. The physical address is that which appears on the computer's address bus when the CPU requests data from a memory address. When remapping occurs, the data can be moved to a different memory location or logical address.
PIM	PMC I/O module.PMC (PCI Mezzanine Card) A new standard form factor for PCI add-in modules. PMCs mate with their respective connectors on the motherboard and are secured with screws.
Pinout	A diagram or table describing the location and function of pins on an electrical connector.
PLL	(Phase-Locked Loop) A semiconductor device which functions as an electronic feedback control system to maintain a closely regulated output frequency from an unregulated input frequency. The typical PLL consists of an internal phase comparator or detector, a low pass filter, and a voltage controlled oscillator which function together to capture and lock onto an input frequency. When locked onto the input frequency, the PLL can maintain a stable, regulated output frequency (within bounds) despite frequency variance at the input.
POST	(Power On Self Test) The Phoenix System BIOS initializes on-board hardware. If it can, the BIOS reports errors to the system console and stops. The System BIOS POST does not do a comprehensive system test.
PQFP	(Plastic Quad Flat Pack) A popular package design for integrated circuits of high complexity.
Program	A set of instructions a computer follows to perform specific functions relative to user need or system requirements. In a broad sense, a program is also referred to as a software application, which can actually contain many related, individual programs.
PS/2	(Personal System 2) Computers designed with IBM's proprietary bus architecture known as Micro Channel.

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PXE	(Preboot Execution Environment) The PXE specification (part of the Intel Wired for Management initiative) has become the standard definition of protocols and interfaces required for network booting.
RAM	(Random Access Memory) Memory in which the actual physical location of a memory word has no effect on how long it takes to read from or write to that location. In other words, the access time is the same for any address in memory. Most semiconductor memories are RAM.
RAS	(Row Address Strobe) An input signal to an internal DRAM latch register specifying the row at which to read or write data. The DRAM requires a row address and a column address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of row addresses and column addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required.
Real mode	The operational mode of Intel architecture CPUs that uses a segmented, offset memory addressing method. These CPUs can address 1 MB of memory using real mode.
Real mode address	A memory address composed of two 16-bit values: a segment address and an offset quantity. A real mode address is constructed by shifting a segment address 4 bits to the left and then adding the offset value. A real mode address is a physical address.
Reflashing	The process of replacing a BIOS image, in binary format, in the flash boot device.
Register	An area typically inside the microprocessor where data, addresses, instruction codes, and information on the status on various microprocessor operations are stored. Different types of registers store different types of information.
Reset	A signal delivered to the microprocessor by the control bus, which causes a halt to internal processing and resets most CPU registers to 0. The CPU then jumps to a starting address vector to begin the boot process.
ROM	(Read Only Memory) A broad class of semiconductor memories designed for applications where the ratio of read operations to write operations is very high. Technically, a ROM can be written to (programmed) only once, and this operation is normally performed at the factory. Thereafter, information can be read from the memory indefinitely.
RS-232	A popular asynchronous bi-directional serial communication protocol. Among other things, the RS-232 standard defines the interface cabling and electrical characteristics, and the pin arrangement for cable connectors.
RTC	(Real Time Clock) Peripheral circuitry on a computer motherboard which provides a nonvolatile time-of-day clock, an alarm, calendar, programmable interrupt, square wave generator, and a small amount of SRAM. In the {product name short}, the RTC operates independently of the system PLL which generates the internal system clocks. The RTC is typically receives power from a small battery to retain the current time of day when the computer is powered down.
SDR	Sensor Data Record.
Segment	A section or portion of addressable memory serving to hold code, data, stack, or other information allowing more efficient memory usage in a computer system. A

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	segment is the portion of a real mode address which specifies the fixed base address to which the offset is applied.
SEL	Sensor Event Log.
Serial port	A physical connection with a computer for the purpose of serial data exchange with a peripheral device. The port requires an I/O address, a dedicated IRQ line, and a name to identify the physical connection and establish serial communication between the computer and a connected hardware device. A serial port is often referred to as a COM port.
Shadow memory	RAM in the address range 0xC000 through 0xFFFFF used for shadowing. Shadowing is the process of copying BIOS extensions from ROM into DRAM for the purpose of faster CPU access to the extensions when the system requires frequent BIOS calls. Typically, system and video BIOS extensions are shadowed in DRAM to increase system performance.
SMC	Satellite Management Controller
Standoff	A mechanical device, typically constructed of an electrically non-conductive material, used to fasten a circuit board to the bottom, top, or side of a protective enclosure.
System memory	See *Conventional memory*.
TB or TByte	(Terabyte) Approximately one thousand billion (US) or one billion (Great Britain) bytes. 2^40 = 1,099,511,627,776 bytes exactly.
USB	(Universal Serial Bus) A new serial data bus that is intended to eliminate the need for separate serial, parallel, mouse, keyboard, joystick, etc. ports on a PC-compatible. These ports can be conceivably replaced by a few, daisy-chained USB ports, all with identical connectors but capable of much higher throughput, upwards of 12Mbs.
VGA	(Video Graphics Adapter) A popular PC graphics controller and display adapter standard developed by IBM. The standard specifies, among other things, the resolution capabilities of the display device. Display devices meeting the VGA standard must be capable of displaying a minimum resolution of 640 horizontal pixels by 480 vertical pixels with at least 16 screen colors.
Wait state	A period of one or more microprocessor clock pulses during which the CPU suspends processing while waiting for data to be transferred to or from the system data or address buses.

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