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EPC[®] - 6

Hardware Reference

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EPC-6 HARDWARE REFERENCE

Contents

1. Getting Started	1
Specifications	2
2. Installation.....	3
EPC-6 Insertion.....	4
EXM Module Insertion	5
VME Backplane Jumpers.....	6
3. Operation.....	7
Initialization Sequence	7
ROM DOS Interaction	10
System Reset	10
Front Panel Indicators	11
Toggle Switch	12
Configuration Setup	14
4. Programming Interface.....	17
Memory Map.....	17
I/O Map.....	20
Registers Specific to EPC-6.....	24
VMEbus Accesses.....	35
Slave Accesses from the VMEbus	38
VMEbus Interrupt Handler	40
VMEbus Interrupt Response	42
VMEbus Mapped Registers	42
5. Theory of Operation	45
Processor, Coprocessor, Memory.....	46
ROM and ROM Shadowing.....	46
Cache.....	46
Flash Memory	47
Nonvolatile SRAM Memory	47
Battery	48
Interrupts and DMA Channels	49

EPC-6 HARDWARE REFERENCE

Watchdog Timer	50
EXMbus	50
8242 Microcontroller	50
VMEbus Interface	51
VMEbus System Controller Functions	52
VMEbus Timing	52
6. Connectors.....	53
7. Error Messages	55
Seven-Segment Display Codes	57
8. Support and Service	59
Replacement Parts	62
Index	63

EPC-6 HARDWARE REFERENCE

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1. Getting Started

This manual contains all the information you need to install and use the EPC-6 VMEbus controller. Additional user's and programmer's manuals discuss the use of software packages available with the EPC-6.

The EPC-6 is a high-speed VMEbus module based on the Intel 80386SX processor. The 386SX has a 32-bit programming architecture but a 16-bit external data bus architecture, combining the power of the 386 software environment with a compact and low-power hardware product.

The EPC-6 can perform VMEbus master accesses, can be a VMEbus slave (by having its dual-port DRAM mapped onto the VMEbus), can be configured as the VMEbus slot-1 system controller, and can be an interrupter and interrupt handler.

The EPC-6 is also a computer compatible with the IBM PC hardware architecture. The standard version of the EPC-6 contains, in ROM, a PC compatible BIOS and a ROM-based version of Microsoft MS-DOS. The EPC-6 also includes on-board nonvolatile flash memory supported as a DOS-compatible solid-state disk and file system. The user can store one or more embedded applications on the processor board and have them automatically invoked at system start-up.

Another feature of the EPC-6 is a slot for an EXM expansion module. This allows some of the I/O of the EPC-6 to be customized for a particular application.

EPC-6 HARDWARE REFERENCE

Specifications

The following table defines the power and environmental specifications of the EPC-6.

Characteristic		Value
Temperature	operating	0 - 60°C ambient
	storage	-40 - 125°C (without battery; 85°C max with battery)
Humidity	operating	0 - 90% noncondensing
	storage	0 - 95% noncondensing
Altitude	operating	0 - 10,000 ft (3000 m)
	storage	0 - 50,000 ft (15,000 m)
Vibration	operating	0.015 inch (0.38 mm) P-P displacement with 2.5 g peak (max) acceleration over 5-2000 Hz
	storage	0.030 inch (0.76 mm) P-P displacement with 5.0 g peak (max) acceleration over 5-2000 Hz
Shock	operating	30 g, 11 ms duration, half-sine shock pulse
	storage	50 g, 11 ms duration, half-sine shock pulse
Power	maximum	15.9 W (17.4 W with coprocessor)
	typical	12.2 W (13.7 W with coprocessor)
Current	maximum	5V @ 3A, 12V @ 100 mA, -12V @ 100 mA
	typical	5V @ 2.2A, 12V @ 5 mA, -12V @ 10 mA
Weight		13 oz (390 g)
VME	master address	A16, A24
	master transfer	D08(EO), D16, RMW
	slave address	A16, A24
	slave transfer	D08(EO),D16,RMW
	interrupter	I(1-7)
	interrupt handler	D08(O),D16 IH(1-7)
	requester	ROR,RONR
	arbiter	RRS,PRI
	system controller	SYSCLK, IACK daisy chain, bus timer
VXI	device type	message based
	protocols	cmdr/master/interrupter

2. Installation

Before installing your EPC-6, you should unpack and inspect it for shipping damage.

- ☒ **DO NOT REMOVE ANY MODULES FROM THEIR ANTI-STATIC BAGS UNLESS YOU ARE IN A STATIC-FREE ENVIRONMENT. THE EPC-6 MODULES, LIKE MOST OTHER ELECTRONIC DEVICES, ARE SUSCEPTIBLE TO ESD DAMAGE. ESD DAMAGE IS NOT ALWAYS IMMEDIATELY OBVIOUS, IN THAT IT CAN CAUSE A PARTIAL BREAKDOWN IN SEMICONDUCTOR DEVICES THAT MIGHT NOT IMMEDIATELY RESULT IN A FAILURE.**

- ☒ **MAKE SURE THAT THE INSTALLATION PROCESS DESCRIBED HERE IS ALSO PERFORMED IN A STATIC-FREE ENVIRONMENT.**

Before installing the EPC-6 in a VMEbus chassis, you need to decide whether the EPC-6 is to be the VMEbus "slot 1" system controller. Every VMEbus system needs a module that performs the system controller functions, including generation of the 16 MHz SYSCLK signal, arbitration of the bus, detection of bus timeout conditions, and initiation of the interrupt-acknowledge daisy chain. The EPC-6 is capable of serving as the system controller.

If the EPC-6 is to be the system controller,

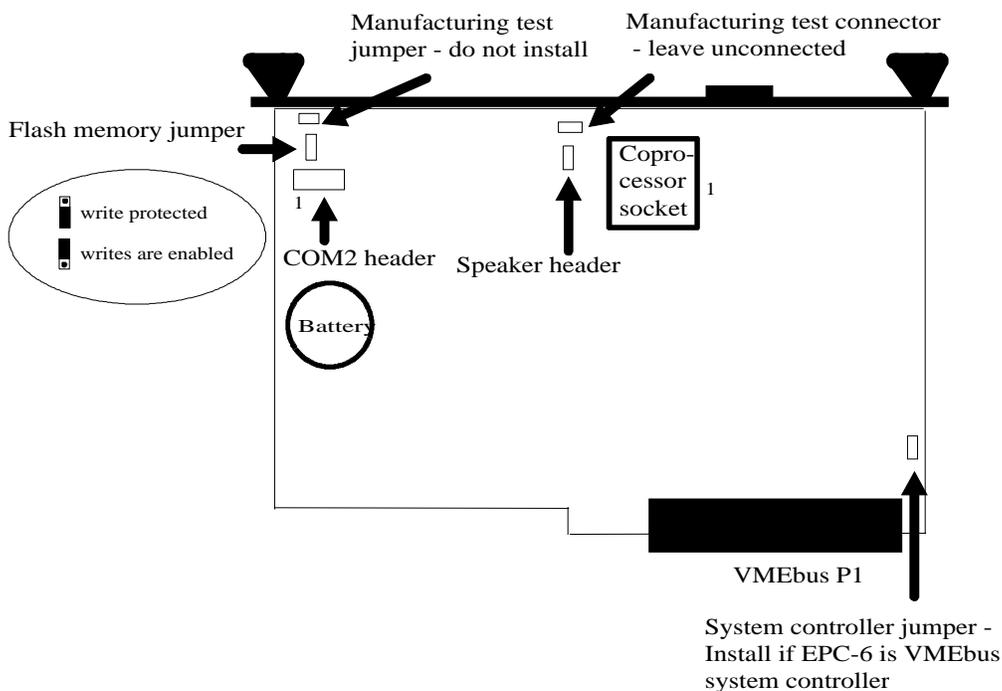
- Make sure the jumper labelled SLOT1 is installed on the EPC-6 processor board to connect the two pins
- When you install EPC-6 in the chassis, make sure it is in the leftmost slot

If the EPC-6 will *not* be the system controller,

- Make sure the jumper labelled SLOT1 on the EPC-6 processor board is removed
- When you install EPC-6 in the chassis, it needs to be somewhere to the right of the module serving as the system controller

EPC-6 HARDWARE REFERENCE

Other jumpers and headers on the board are shown in the diagram below.



The only other user-configurable jumper in the EPC-6 is one for write protection of the flash memory. If you wish to protect the flash memory from inadvertent erasure, install the jumper to connect the middle pin to the pin farthest from the front panel; otherwise install the jumper to connect the middle pin to the pin nearest the front panel.

EPC-6 Insertion

The EPC-6 is inserted into a VME chassis in the following way:

1. Make sure the ejector handles are in the normal non-eject position. (Push the top handle down and the bottom handle up so that the handles are not tilted.)

EPC-6 HARDWARE REFERENCE

3. Slide the EPC-6 module into the VME chassis, making sure the top and bottom board edges are in the chassis' card guides. Use thumb pressure on the handles to mate the module firmly with the VME backplane connector.
4. Tighten the two screws in the top and bottom of the front panel to ensure proper connector mating and prevent loosening of the module via vibration.
 - ☒ **MAKE SURE THAT POWER TO YOUR VME SYSTEM IS OFF. THE MODULE IS NOT DESIGNED TO BE INSERTED OR REMOVED FROM A LIVE BACKPLANE.**
 - ☒ **WHEN INSERTING THE EPC-6 MODULE, AVOID TOUCHING THE CIRCUIT BOARD AND CONNECTOR PINS, AND MAKE SURE THE ENVIRONMENT IS STATIC-FREE.**

EXM Module Insertion

One EXM may be optionally installed through the front panel of the EPC-6. To install an EXM,

1. Remove and save the blank face plate from the EXM slot in the EPC-6 face plate.
2. Slide the EXM into place in the card guides. Push firmly on the EXM front panel to insert its rear connector.
3. Tighten the thumb screws on the EXM's face plate.
 - ☒ **MAKE SURE THAT POWER TO YOUR VME SYSTEM IS OFF. EXMS ARE NOT DESIGNED TO BE INSERTED OR REMOVED FROM LIVE SYSTEMS.**
 - ☒ **WHEN INSERTING AN EXM, AVOID TOUCHING THE CIRCUIT BOARD, AND MAKE SURE THE ENVIRONMENT IS STATIC-FREE.**

Most EXM types can be used in the EPC-6. Those that require the presence of a disk BIOS in the EPC cannot be used with the EPC-6; this includes the EXM-3 and EXM-9.

EPC-6 HARDWARE REFERENCE

Once an EXM is installed, you will need to run the BIOS setup program to describe how the specific EXM should be dynamically configured upon power-up. This is described in Chapter 3.

VME Backplane Jumpers

The VMEbus contains several daisy-chained control signals. Almost all VMEbus backplanes contain jumpers for these control signals to allow systems to operate with empty slots. Failing to install these jumpers properly is a common source of problems in building a new VMEbus system.

There are five jumpers per VME slot, one for each of the four bus-grant arbitration levels and one for the interrupt-acknowledge daisy chain. Depending on the backplane manufacture, the jumpers may be on the rear pins of the J1 connector, or may be alongside it on the front or rear side of the backplane.

For the slot containing the EPC-6, remove the jumpers. Leave the jumpers inserted for all empty slots. For slots otherwise occupied, consult the documentation from the manufacturers of the modules.

Serial Port Cap

Your EPC-6 may have been shipped with a plastic cap over the serial port connector. This cap is a conductive cap whose purpose is to shield the exposed pins in the connector from ESD (electrostatic discharge). You should leave it installed when nothing is connected.

3. Operation

This chapter contains information about user operation of the EPC-6.

Initialization Sequence

The diagram on the following page shows the major initialization steps the EPC-6 and its BIOS go through. The seven-segment display shows information about the initialization state of the EPC-6.

The first major step is a selftest. The selftest program displays the number of the test currently being run. If a catastrophic error is detected, an error code is displayed and the initialization sequence terminates. These codes are described in Chapter 7. If the EPC-6 has a problem that inhibits even the running of the selftest program the number "8" will appear in the display.

After the selftest completes successfully, the configuration information maintained by the BIOS in a small battery-backed CMOS RAM is used. A problem at this point is regarded as non-catastrophic, but it causes the BIOS to load MS-DOS from ROM and then give DOS control. This allows the user to intervene (e.g., to run the DOS DEBUG program). The method for interacting with DOS is described in the next section. Possible problems are loss of the configuration information due to a battery failure or change, and a mismatch between the type of installed EXM versus the type expected.

Information about non-catastrophic errors is saved in the upper 2K bytes of the SRAM for use by the setup program.

If there are no errors, the BIOS looks for a boot device with a valid boot image. The boot device can be the onboard flash memory or a source specified in the CMOS configuration information (using the setup program) If a boot device is not present, the BIOS invokes the ROM DOS.

The next step is a five-second pause to check for operator intervention. During this step a rotating pattern appears on the display. If you momentarily push the toggle

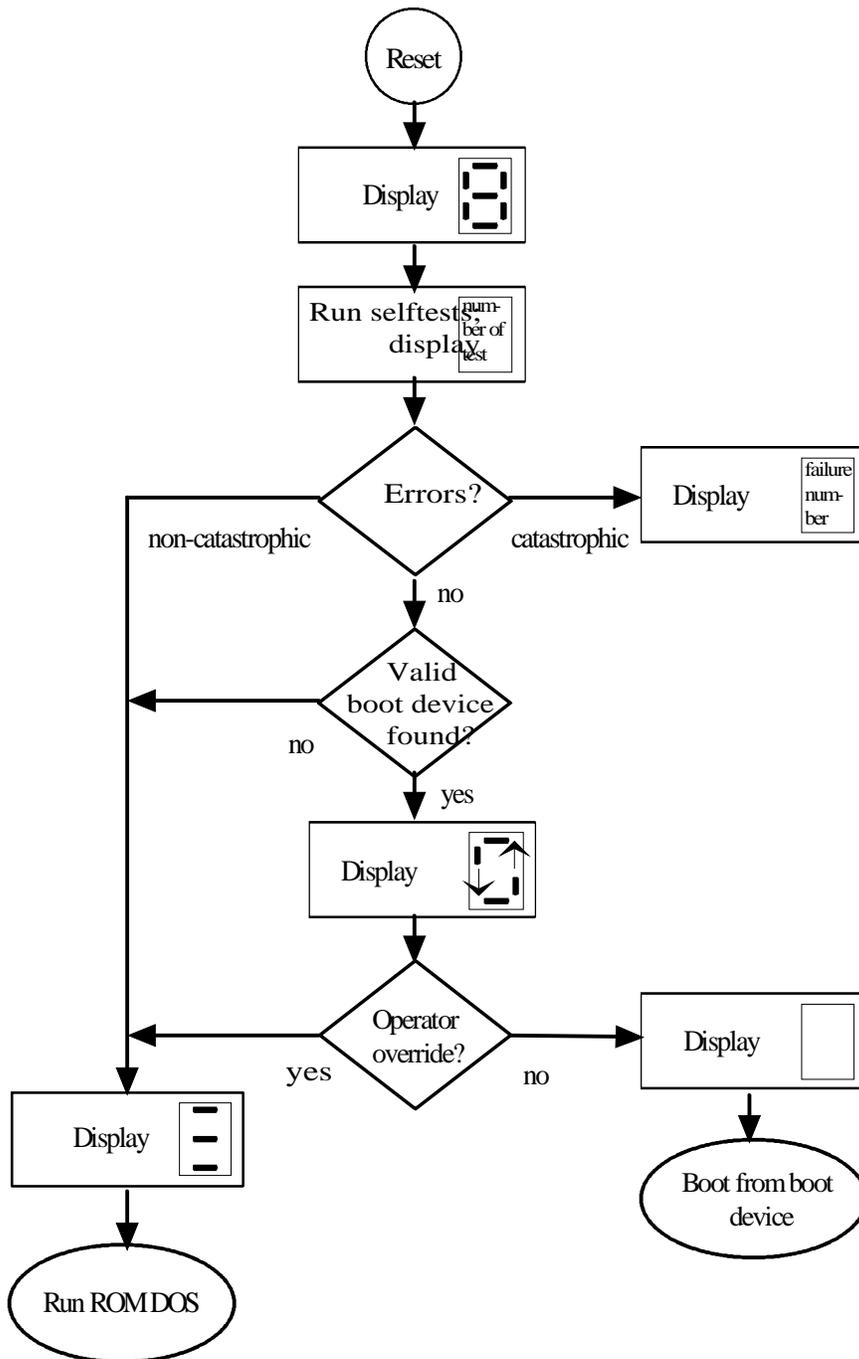
EPC-6 HARDWARE REFERENCE

switch to the abort position during this pause, the BIOS will invoke the ROM DOS instead of the program from flash memory.

If one of the above steps resulted in invocation of the ROM DOS, three horizontal bars will appear on the display and stay there while ROM DOS has control. Some programs run under ROM DOS may display something different, but the three bars will always reappear when ROM DOS has control. When ROM DOS has control, any of the built in DOS programs and commands may be run (e.g., the DEBUG program), as well as other programs that have been added to DOS specifically for the EPC-6 (e.g., programs to display and change the CMOS RAM configuration information, download code, and program the flash memory).

If the BIOS proceeds down the flash memory path, the flash memory is viewed as a bootable disk device and the BIOS starts the bootstrap process by loading the first 512 bytes into memory location 07C0:0000 and passing control to it. The display is blanked before attempting the bootstrap process. For more information about the bootstrap process and how to create a bootable image in the flash memory, see the *EPCControl Programmer's Guide*.

EPC-6 HARDWARE REFERENCE



EPC-6 HARDWARE REFERENCE

ROM DOS Interaction

Since the EPC-6 is more of a dedicated controller than an embedded PC-compatible computer, it doesn't have standard PC-compatible keyboard and display interfaces. There are two ways to interact with the ROM DOS on the EPC-6:

1. Connect a standard ASCII terminal with an RS-232 interface to the serial port connector on the front panel.
2. Use a separate full EPC (having keyboard and monitor) on the same VMEbus with supplied software that uses this EPC as a virtual console to the EPC-6(s).

The RS-232 method is provided by an action the BIOS performs before invoking the ROM DOS - it redirects the command input and output streams to the COM1 serial port. Connecting a terminal and causing the ROM DOS to be invoked will display the standard DOS prompt on the terminal. By typing the DOS DIR command you can see the programs available. A program in ROM named SETUP can be used to display and change the configuration information maintained by the BIOS.

The software needed to use another EPC as the human interface for an EPC-6 is part of the EPCControl software product. Refer to the separate documentation on this product.

System Reset

The reset switch performs a hardware reset of the EPC-6 and any EXM module and invokes the BIOS initialization process discussed in the previous sections. Removing and reapplying power to the EPC-6 also causes a hardware reset. Note that if the "dot" or decimal point in the lower right corner of the 7-segment LED display is illuminated, an EPC-6 program has disabled the reset toggle switch. In this case the only way to reset the EPC-6 is by externally signalling VMEbus SYSRESET (unless the EPC-6 program has disabled this also) or by a power-off/on cycle.

Generating VMEbus SYSRESET

The EPC-6 drives the VMEbus SYSRESET signal in accordance with the VMEbus specification upon power on. Resetting the EPC-6 via the reset switch does *not* cause the EPC-6 to assert SYSRESET. The EPC-6 contains, however, a software-controllable register bit to allow software to assert SYSRESET.

EPC-6 HARDWARE REFERENCE

Responding to VMEbus SYSRESET

A software-controllable register bit in the EPC-6 controls whether or not a hardware reset of the EPC-6 occurs when the VMEbus SYSRESET signal is asserted.

Front Panel Indicators

The EPC-6 contains the following four LEDs:

- Run** This green LED should flicker during BIOS initialization and be lit thereafter. It denotes that the 386 is performing a DRAM access. If the LED is off, the most probable causes are (1) a "hung" condition has occurred in the operating-system or application software and (2) a VMEbus access is being attempted but the EPC-6 has not received a bus-grant signal. In the latter case, the usual reasons are an error in setting the jumpers on the VMEbus backplane, not being fully seated in the backplane, or a failure in the slot-1 system controller module.
- Fail** This red LED can light only if the EPC-6 is configured as the VMEbus system controller. If lit, it indicates that some module is driving the VMEbus SYS-FAIL line.
- Master** This LED denotes the EPC-6 performing a VMEbus access. It is lit from the time the 386 processor initiates the read, to the time the bus operation completes or times out. Seeing the master LED on and the run LED off is an indication that the EPC-6 is stopped because either it can't get access to the bus or because no module is responding to the access and the access has not been timed out.
- Slave** This LED denotes that another module is performing a memory access into the EPC-6's DRAM.

The front panel also contains seven-segment LED display. The display has three purposes:

1. During BIOS initialization it describes the current stage of the initialization. If a test fails in the selftest phase, it displays a code indicating the test that caused the BIOS to abort the normal initialization flow. These codes are described in Chapter 7.

EPC-6 HARDWARE REFERENCE

2. After initialization, the display is available for use by the application program.
3. The display shows whether software has disabled the reset function of the front-panel switch. If the decimal point in the lower right corner of the display is lit, the reset function of the switch is disabled.

Toggle Switch

The front-panel toggle switch has three positions: inactive (normal position), reset, and abort. Pushing it to the reset position suspends the EPC-6 and releasing it causes a hardware reset. Pushing it in the other direction generates the IRQ11 interrupt.

The interrupt position has two purposes. An application program can install an IRQ11 interrupt handler and thus define the switch in an application-specific fashion. The second purpose is a special interpretation of the switch during BIOS initialization after a reset.

Moving the switch to the interrupt position during the five-second operator-override period (when the display shows a circling light), causes the BIOS to load MS-DOS from ROM and give control to DOS.

EPC-6 HARDWARE REFERENCE

Configuration Setup

The EPC-6 maintains certain configuration information in a small battery-backed RAM. The ROM DOS SETUP program can be used to display and change this information. The information maintained is described below.

DATE and TIME

This parameter establishes the date and time in the battery-powered TOD (time of day) clock..

DRIVES

These parameters allow you to select devices for logical drives A, B, C, and D. The setup program shows you the options for each. Drive C is the boot device unless drive A is defined as a floppy drive and a floppy diskette is present at boot time. Drive C can be defined as AT (a hard disk drive, for which you may select subtypes describing its characteristics), the flash memory on the EPC-6, a flash-memory EXM (e.g., EXM-2), and VMEbus memory. The latter initiates a search by the EPC-6 in A24 address space on specific boundaries for a valid boot image; for more information see the *EPCControl Programmer's Guide*.

ARBITRATION PRIORITY

This parameter allows you to select among the four VMEbus priority levels. This is the level at which the EPC-6 will request the bus when it performs a VMEbus access.

BUS RELEASE MODE

This parameter allows you to choose one of two bus-release modes: ROR (release on request) and RONR (request on no request, also known as the VXI fair-requester mode). ROR results in slightly better EPC-6 performance when accessing the VMEbus; RONR directs the EPC-6 to not "park" on the bus and thus slightly improves the access time of other VMEbus masters to the bus.

EPC-6 HARDWARE REFERENCE

SLOT 1 ARBITRATION MODE

This parameter selects between the two arbitration algorithms provided by the EPC-6 when it is configured as the slot-1 system controller: priority arbitration and round-robin arbitration.

VXI REGISTER BASE (ULA)

The EPC-6 has a set of configuration registers consistent with the VXIbus specification that are mapped into the VMEbus A16 address space. This parameter allows you to choose among eight locations for these registers. In VXIbus terminology, the base address is associated with the device's ULA (unique logical address).

In a system with multiple EPCs, you should configure each EPC with a unique value. The values and the corresponding base addresses are shown in the following table.

ULA	A16 base address
F8	FE00
F9	FE40
FA	FE80
FB	FEC0
FC	FF00
FD	FF40
FE	FF80
FF	FFC0

SLAVE MEMORY OFFSET

The EPC-6 is designed to be both a VMEbus master (where it generates VMEbus accesses) and VMEbus slave (where its DRAM is mapped into VMEbus memory and can be accessed by other VMEbus masters). This parameter specifies whether the EPC-6 will respond to accesses from the VMEbus and, if so, the base address of the EPC-6's DRAM in A24 space. The available base addresses are in the following table.

A24 base address
000000
400000
800000
C00000

EPC-6 HARDWARE REFERENCE

This parameter has no effect on the EPC-6's behavior as an interrupter and interrupt handler, and does not affect the EPC-6's acting as a slave to VMEbus A16 requests that access the EPC-6's configuration and message registers.

EXM CONFIGURATION

The EPC-6's CMOS RAM holds identification and configuration information for an EXM module. There are three one-byte values. The first is the unique ID expected for the installed EXM. FF denotes none. The other two columns are the EXM configuration bytes. Other than the low-order bit of the first byte, for which 1 denotes EXM enabled and 0 EXM disabled, the interpretations of the bits are dependent on the specific EXM and are defined in the EXM manuals.

If the setup program appears to support six EXMs in six slots, only slot 0 is pertinent to the EPC-6.

4. Programming Interface

This chapter describes the EPC-6 as seen by a program. Wherever possible, users should avoid direct use of most of these facilities. Hardware features in common with standard PCs should be accessed by standard BIOS calls. Hardware unique to EPC-6, such as the VMEbus interface should be accessed through a variety of software packages and drivers available with the EPC-6.

Memory Map

Memory at addresses between 0 and 1 MB (0FFFFFFh) is mapped as follows:

Range	Content
000000 09FFFF	DRAM
0A0000 0BFFFF	Uncommitted, mapped to EXMbus
0C0000 0C7FFF	DRAM or EXMbus (see bit WRPT in memory control register)
0C8000 0DFFFF	Uncommitted, mapped to EXMbus
0E0000 0EFFFF	Mappable window onto VMEbus
0F0000 0FFFFFF	DRAM or EXMbus (see bit WRPT in memory control register)

For a 1 MB EPC-6, the remaining address space is defined as

Range	Content
100000 13FFFF	DRAM
140000 F7FFFF	Uncommitted, mapped to EXMbus
F80000 FFFFFFF	BIOS ROM

For a 4 MB EPC-6, the remaining address space is defined as

Range	Content
100000 3FFFFFF	DRAM
400000 F7FFFF	Uncommitted, mapped to EXMbus
F80000 FFFFFFF	BIOS ROM



EPC-6 HARDWARE REFERENCE

Cached and Uncached Addresses

EPC-6 contains a 16 KB, two-way set associative cache. The cache is designed to cache selectively by address range, because many memory areas defined by the PC architecture, as well as memory mapped to the VMEbus and potentially some mapped to the EXMbus, cannot be safely cached. What *is* cached is the first 640 KB of memory and the 7 MB of address space above 1 MB, meaning the address ranges

000000	to	09FFFF
100000	to	7FFFFFFF

The use of a cache with dual-port memory (i.e., DRAM in the EPC-6 that is also accessible by other VMEbus masters) raises the issue of "stale data." This is prevented by the "bus watching" logic of the cache controller. As shown in the following figure, any write into EPC-6's DRAM from another VME master will cause the data at these addresses, if it happens to be in the cache, to be invalidated in the cache, meaning that a subsequent read of the data from the 386 will fetch the updated value from DRAM.

EPC-6 HARDWARE REFERENCE

I/O Map

The following defines the I/O addresses decoded by the EPC-6. It does not define addresses that might be decoded by the installed EXM.

Port	Functional group	Usage	
00	DMA	Channel 0 address	
01		Channel 0 count	
02		Channel 1 address	
03		Channel 1 count	
04		Channel 2 address	
05		Channel 2 count	
06		Channel 3 address	
07		Channel 3 count	
08		Command/status	
09		DMA request	
0A		Command register (R)	
		Single-bit DMA req mask(W)	
0B		Mode	
0C		Set byte pointer (R)	
		Clear byte pointer (W)	
0D		Temporary register (R)	
	Master clear (W)		
0E	Clear mode reg counter (R)		
	Clear all DMA req mask(W)		
0F	All DMA request mask		
20	Interrupt controller 1	Port 0	
21		Port 1	
24	83000 Controller	Data register	
26		Index register	
40	Timer	Counter 0	
41		Counter 1	
42		Counter 2	
43		Control (W)	
60	Keyboard controller	Data I/O register	
61	NMI status	NMI status	
64	Keyboard controller	Command/status register	
70	Real-time clock	RTC index reg / NMI enable	
71		RTC data register	
		0	seconds
		1	seconds alarm

EPC-6 HARDWARE REFERENCE

Port	Functional group	Usage
		2 minutes 3 minutes alarm 4 hours 5 hours alarm 6 day of week 7 date of month 8 month 9 year A status A B status B C status C D status D E RAM ... 3F RAM
81 82 83 87 89 8A 8B 8F	DMA	Channel 2 page register Channel 3 page register Channel 1 page register Channel 0 page register Channel 6 page register Channel 7 page register Channel 5 page register Refresh page register
A0 A1	Interrupt controller 2	Port 0 Port 1
C0 C2 C4 C6 C8 CA CC CE D0 D2 D4 D6 D8 DA DC DE	DMA	Channel 4 address Channel 4 count Channel 5 address Channel 5 count Channel 6 address Channel 6 count Channel 7 address Channel 7 count Command/status DMA request Command register (R) Single-bit DMA req mask(W) Mode Set byte pointer (R) Clear byte pointer (W) Temporary register (R) Master clear (W) Clear mode reg counter (R) Clear all DMA req mask (W) All DMA request mask

EPC-6 HARDWARE REFERENCE

Port	Functional group	Usage
F0	Coprocesor	Clear coprocessor busy
F1		Reset coprocessor
2F8	COM2 serial port	Receiver/transmitter buffer
2F9		Baud rate divisor latch (LSB)
2FA		Interrupt enable register
2FB		Baud rate divisor latch (MSB)
2FC		Interrupt ID register
2FD		Line control register
2FE		Modem control register
2FE		Line status register
378	LPT1 parallel port	Printer data register
379		Printer status register
37A		Printer control register
3F8	COM1 serial port	Receiver/transmitter buffer
3F9		Baud rate divisor latch (LSB)
3FA		Interrupt enable register
3FB		Baud rate divisor latch (MSB)
3FC		Interrupt ID register
3FD		Line control register
3FE		Modem control register
3FE		Line status register
8104	VME and misc control	Memory control
8130		VME A21-16 address
8132		<i>alias address of 8130</i>
8134		<i>alias address of 8130</i>
8136		<i>alias address of 8130</i>
8140		ID low
8141		ID high
8142		Device type low
8143		Device type high
8144		Status/control low
8145		Status/control high
8146		Slave offset low
8147		Slave offset high
8148		Protocol low
8149		Protocol high
814A		Response low
814B		Response high
814C		Message high low
814D		Message high high
814E		Message low low
814F	Message low high	

EPC-6 HARDWARE REFERENCE

Port	Functional group	Usage
8151		VME modifier
8152		VME interrupt state
8153		VME interrupt enable
8154		VME event state
8155		VME event enable
8156		Module status/control
8157		<i>alias address of 815F</i>
8159		<i>alias address of 8151</i>
815A		<i>alias address of 8152</i>
815B		<i>alias address of 8153</i>
815C		<i>alias address of 8154</i>
815D		<i>alias address of 8155</i>
815E		<i>alias address of 8156</i>
815F		VME interrupt generator
8380		Flash/SRAM address
8381		Flash/SRAM address
8382		Flash/SRAM address
8383		Flash data
8384		SRAM data
8385		LED register

EPC-6 HARDWARE REFERENCE

Registers Specific to EPC-6

Registers in the I/O space that are specific to the EPC-6 are defined below.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	I/O port
Memory Control Register	reserved						WPRT	CDEN	8104
VME A21-16 Address Reg	VMEbus address bits 21-16						res	res	8130
ID Register, lower	1	1	1	0	1	1	0	0	8140
ID Register, upper	1	0	0	0	1	1	1	1	8141
Device Type Reg, lower	1	1	0	0	1	1	0	0	8142
Device Type Reg, upper	0	0	0	1	1	1	1	1	8143
Status/Control Reg, lower	SRIE	RELM	ARBPRI		RDY	PASS	NOSF	RSTP	8144
Status/Control Reg, upper	SLE	1	SYSR	SYSF	ARBM	1	1	1	8145
Slave Offset Reg, lower	1	1	1	1	1	1	1	1	8146
Slave Offset Reg, upper	0	0	0	1	1	1	SLAVE BASE		8147
Protocol Register, lower	1	1	1	1	1	1	1	1	8148
Protocol Register, upper	0	1	0	1	1	1	1	1	8149
Response Register, lower	LOCK	1	ABMH	1	1	ULA			814A
Response Register, upper	0	0	0	0	1	RRDY	WRDY	1	814B
Message High Reg, lower									814C
Message High Reg, upper									814D

EPC-6 HARDWARE REFERENCE

Message Low Reg, lower									814E
Message Low Reg, upper									814F
VME Modifier Register	VME WA23-22	res	IACK	res	AM4	AM2	AM1		8151
VME Interrupt State Reg	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	MSGR	8152
VME Interrupt Enable Reg	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	MSGR	8153
VME Event State Register	1	1	1	1	WDT	ACFA	BERR	SYSF	8154
VME Event Enable Register	1	1	1	1	WDT	ACFA	BERR	SYSF	8155
Module Status/Control Reg	DONE	AS	DS0	DS1	res	res	FWDT	ENRE	8156
Interrupt Generator Register	1	1	1	1	0	INTERRUPT-OUT			815F
FSA7-0 Address Register	Flash/SRAM address bits 7-0								8380
FS A15-8 Address Register	Flash/SRAM address bits 15-8								8381
FS A19-16 Address Register	reserved				Flash/SRAM address bits 19-16				8382
Flash Data Register									8383
SRAM Data Register									8384
LED Register	TSEN	LED6	LED5	LED4	LED3	LED2	LED1	LED0	8385

Where a bit position has been described by a 0 or 1, the bit is a ROM bit, and writing to it has no effect. Unless otherwise noted below, all registers and bit values are readable and writeable.

Memory Control Register	reserved				WPRT	CDEN	8104
-------------------------	----------	--	--	--	------	------	------

EPC-6 HARDWARE REFERENCE

This register contains two control bits pertaining to the DRAM and the flash memory.

WPRT If set, write-protects the DRAM area containing the BIOS. This means that writes to the address ranges 0C0000-0C7FFF and 0F0000-0FFFFFF are mapped to the EXMbus (instead of DRAM) and reads come from DRAM. If clear, writes to these address ranges map to DRAM, reads from 0C7000-0CFFFF map to the EXMbus, and reads from 0F0000-0FFFFFF come from DRAM. This bit is used by the EPC-6 BIOS.

CDEN If set, the flash memory is accessible. If clear, writes to the flash data register have no effect and reads from it return an unpredictable value. A purpose of this bit is to allow use of the flash-memory EXM-2, which maps its data register at the same location (8383).

VME A21-16 Address Reg

VMEbus address bits 21-16	res	res
---------------------------	-----	-----

 8130

When an access is performed by the EPC-6 in its "E page" (address range 0E0000-0EFFFF), the access is mapped onto the VMEbus. The least-significant sixteen of the VME address bits are provided directly (from the 386SX), and the remaining 8 (for an A24 access) bits must come from somewhere else. Six of them come from this register. Bit 7 of this register is used as VME address bit 21, bit 6 as VME address bit 20, ..., and bit 2 as VME address bit 16.

The two low-order bits are reserved RAM bits. On writes, assign them the value 0. For compatibility with EPC-1, this register is aliased at I/O port addresses 8132, 8134, and 8136.

ID Register, lower

1	1	1	0	1	1	0	0
---	---	---	---	---	---	---	---

 8140

ID Register, upper

1	0	0	0	1	1	1	1
---	---	---	---	---	---	---	---

 8141

This read-only register adheres to the VXIbus specification. It defines the EPC-6 as a message-based device and the manufacturer as RadiSys Corporation.

EPC-6 HARDWARE REFERENCE

Device Type Reg, lower

1	1	0	0	1	1	0	0
---	---	---	---	---	---	---	---

 8142

Device Type Reg, upper

0	0	0	1	1	1	1	1
---	---	---	---	---	---	---	---

 8143

This register adheres to the VXIbus specification. The first four bits of the upper half denote that the EPC-6 maps into a 4 MB range in the A24 space when used as a slave. The remaining ROM bits define the EPC-6 as having a model code of 4044.

Status/Control Reg, lower

SRIE	RELM	ARBPRI	RDY	PASS	NOSF	RSTP
------	------	--------	-----	------	------	------

 8144

Status/Control Reg, upper

SLE	1	SYSR	SYSF	ARBM	1	1	1
-----	---	------	------	------	---	---	---

 8145

This register adheres to the VXIbus specification and also contains EPC-6 specific bits.

SRIE **SYSRESET** input enable. If set, assertion of VME **SYSRESET** generates a reset of the EPC-6. One use of this bit is having EPC-6 software reset other VME devices (via bit **SYSR**) without resetting the EPC-6.

RELM Bus release mode. If set, the bus release mode is ROR (release on request); otherwise it is the VXI **RONR** "fair requester" mode (request on no request). Altering this bit via the VME-mapped location of this register has no effect.

ARBPRI Arbitration priority. This defines the level at which the EPC-6 will arbitrate for the VMEbus. 11 means 3, 10 means 2, 01 means 1, 00 means 0. Like for **RELM**, altering this field via the VME-mapped location of this register has no effect.

RDY This is a RAM bit defined by the VXI specification. In a VXIbus software environment, if **RDY**=1 and **PASS**=1, the EPC-6 is ready to accept VXI-defined messages. The VMEbus user needn't be concerned with this and the next bit.

PASS This is a RAM bit defined by the VXI specification. If set (1), the EPC-6 has completed its selftest successfully.

NOSF **SYSFAIL** inhibit. If set, the EPC-6 cannot assert the VME **SYSFAIL** line.

RSTP Reset EPC. Setting this bit will reset the EPC-6.

SLE Slave enable. If set, the EPC-6 will respond to certain A24 accesses on the VMEbus.

SYSR **SYSRESET**. The EPC-6 asserts the VME **SYSRESET** line while this bit is 1. When using this bit, it is software's responsibility to ensure that the VME specified minimum assertion time of **SYSRESET** is met.

EPC-6 HARDWARE REFERENCE

SYSF **SYSFAIL.** The EPC-6 asserts the VME SYSFAIL line while this bit is 0. (The polarity of the bit is reversed from that of SYSRESET so that an EPC-6 reset - which clears this bit - causes SYSFAIL to be asserted until the BIOS stores a 1 in this bit.)

ARBM **Arbitration mode.** This bit is pertinent only if the EPC-6 is jumpered to be the VMEbus system controller. If set, the EPC-6 is a priority arbiter; otherwise it is a round-robin arbiter. Like for RELM, altering this field via the VME-mapped location of this register has no effect.

Slave Offset Reg, lower

1	1	1	1	1	1	1	1
---	---	---	---	---	---	---	---

 8146

Slave Offset Reg, upper

0	0	0	1	1	1	SLAVE BASE
---	---	---	---	---	---	------------

 8147

SLAVE BASE defines the base address of the EPC-6's memory in the VMEbus A24 address space as follows: 00 - 000000, 01 - 400000, 10 - 800000, 11 - C00000.

Protocol Register, lower

1	1	1	1	1	1	1	1
---	---	---	---	---	---	---	---

 8148

Protocol Register, upper

0	1	0	1	1	1	1	1
---	---	---	---	---	---	---	---

 8149

This read-only register is defined by the VXIbus specification. In VXI systems, it defines the EPC-6 as being a servant and commander, having no signal register, being a bus master, and not providing fast handshake mode.

EPC-6 HARDWARE REFERENCE

Response Register, lower	LOCK	1	ABMH	1	1	ULA			814A
Response Register, upper	0	0	0	0	1	RRDY	WRDY	1	814B

With the exception of LOCK, this register is defined by the VXIbus specification. It contains control bits associated with the message registers.

- LOCK** If set, the message register can be locked for the sending of a message. If clear, the message register has been locked.
- ABMH** This bit is cleared when the message high register is read or written. It serves as a location monitor for determining whether a message is 16 or 32 bits in length.
- ULA** Unique logical address. This determines the base of the registers in the VMEbus A16 space. 0 denotes FE00, 1 denotes FE40, 2 denotes FE80, 3 denotes FEC0, 4 denotes FF00, 5 denotes FF40, 6 denotes FF80, and 7 denotes FFC0.
- RRDY** Read ready. As defined by VXI, a 1 denotes that the message registers contain outgoing data to be read by another device. RRDY is cleared when the message low register is read.
- WRDY** Write ready. If set, the message registers are armed for an incoming message. When a write occurs into the message-low register, WRDY is cleared and the MSGR interrupt condition is asserted.

Although the intention is that the message register reads and writes that clear WRDY and RRDY come from another VMEbus processor, accesses to the message register as mapped into the EPC-6's I/O space also have the same effect.

When the response register is read from the VMEbus, the current value of the register is read, and then LOCK is cleared. The protocol for sending a message to the EPC-6, if there are multiple potential senders, is the following. The sender first reads the response register. If both WRDY and LOCK are 1, he may then proceed to send the message. For a 16-bit message, the sender writes into the message-low register. For a 32-bit message, he writes first into the message-high register and then the message-low register.

EPC-6 HARDWARE REFERENCE

Message High Reg, lower 814C

Message High Reg, upper 814D

This register is an extension of the following register for 32-bit messages. An access to this register clears flag ABMH in the response register.

Message Low Reg, lower 814E

Message Low Reg, upper 814F

This register is typically used as an incoming message register by doing a D16 write into it from the VMEbus (this register, as are many others, are mapped into the VMEbus A16 address space, as discussed later).

EPC-6 HARDWARE REFERENCE

VME Modifier Register

VME WA23-22	res	IACK	res	AM4	AM2	AM1
-------------	-----	------	-----	-----	-----	-----

 8151

This register is also used when the EPC-6 makes an access through its E page to the VMEbus. Bits 7 and 6 provide VME address bits A23 and A22, respectively. Bits 2-0 define the value placed on the associated VMEbus address-modifier lines. Register bits are not defined for the VMEbus address-modifier AM3 and AM0 lines since, for all defined address-modifier values in the VMEbus specification, AM3 is 1 and AM0 is the inverse of AM1. Therefore these two bit values are generated by hardware.

AMx These bits drive the VME address-modifier lines AM4, AM2, and AM1. The other three VME address-modifier lines are generated automatically: AM5 and AM3 are always 1 and AM0 is always the inverse of AM1. Thus these three register bits correspond to the following VMEbus functions:

000	A16 non-privileged access
001	reserved
010	A16 supervisory access
011	reserved
100	A24 non-privileged data access
101	A24 non-privileged program access
110	A24 supervisory data access
111	A24 supervisory program access

IACK This bit, when set, is used to define the VMEbus access as an interrupt acknowledge cycle. The interrupt being acknowledged must be encoded by software as a value on VME address lines A1-A3.

For compatibility with other EPCs, when writing to this register assign 0 to reserved bit 5 and 1 to reserved bit 3.

EPC-6 HARDWARE REFERENCE

VME Interrupt State Reg

IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	MSGR
------	------	------	------	------	------	------	------

 8152

This read-only register defines the state of the VMEbus and message interrupts.

IRQx If clear (0), the associated VMEbus interrupt line is asserted.

MSGR If clear (0), a message interrupt is being signalled. MSGR is clear if both of bits RRDY and WRDY in the response register are clear.

VME Interrupt Enable Reg

IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	MSGR
------	------	------	------	------	------	------	------

 8153

This is a mask of the interrupt conditions in the interrupt state register. A 1 denotes that the corresponding interrupt is enabled. If any bit in this register is a 1 and the corresponding bit in the interrupt state register is a 0, the EPC-6 IRQ10 interrupt is asserted. Software may then examine the interrupt and event state registers to determine the cause.

VME Event State Register

1	1	1	1	WDT	ACFA	BERR	SYSF
---	---	---	---	-----	------	------	------

 8154

Similar to the interrupt state register, this register defines additional conditions that may result in an IRQ10 interrupt. If the bit is 0, the condition is present.

WDT The EPC-6's watchdog timer's period has expired.

ACFA VMEbus ACFAIL is asserted.

BERR An access from the EPC-6 to the VMEbus was terminated with a BERR (bus error).

SYSF VMEbus SYSFAIL is asserted.

All bits are read-only except BERR. BERR is a sticky bit that is cleared whenever an access from the EPC-6 is terminated by a bus error, and remains clear (0) unless changed by software (by writing any value to this register).

EPC-6 HARDWARE REFERENCE

VME Event Enable Register

1	1	1	1	WDT	ACFA	BERR	SYSF
---	---	---	---	-----	------	------	------

 8155

This is a mask of the interrupt conditions in the event state register. A 1 denotes that the corresponding event is enabled as an interrupt. If any bit in this register is a 1 and the corresponding bit in the event state register is a 0, the EPC-6 IRQ10 interrupt is asserted. Software may then examine the interrupt and event state registers to determine the cause.

Module Status/Control Reg

DONE	AS	DS0	DS1	res	res	FWDT	ENRE
------	----	-----	-----	-----	-----	------	------

 8156

This register contains miscellaneous status and control bits.

DONE This read-only bit is 0 whenever the EPC-6 has a VMEbus access outstanding. It is used for determining when a pipelined VMEbus write is complete.

AS This read-only bit is 1 whenever the VMEbus AS (address strobe) signal is asserted. It may be used for bus monitoring.

DS0 This read-only bit is 1 whenever the VMEbus DS0 (data strobe) signal is asserted. It may be used for bus monitoring.

DS1 This read-only bit is 1 whenever the VMEbus DS1 (data strobe) signal is asserted. It may be used for bus monitoring.

FWDT Fast watchdog timer. If clear, the period of the watchdog timer is approximately 8 seconds. If set, the period is approximately 250 ms.

A write to the module status/control register also has a side effect of resetting the watchdog timer. Therefore, if you are using the watchdog timer, the intention is that you are required to write to this register within the defined period of the timer to prevent its generating an interrupt or reset.

EPC-6 HARDWARE REFERENCE

Interrupt Generator Register

1	1	1	1	0	INTERRUPT-OUT
---	---	---	---	---	---------------

 815F

This register is used to assert one of the VMEbus interrupt signals. If the INTERRUPT-OUT bits are zero, no interrupt line is asserted by the EPC-6. If set to 001, IRQ1 is asserted. If set to 010, IRQ2 is asserted, and so on. If and when an interrupt acknowledge cycle is sent to the EPC-6, the INTERRUPT-OUT bits are cleared.

You can also deassert a previously asserted interrupt by writing 0 into the register.

FSA7-0 Address Register

Flash/SRAM address bits 7-0

 8380

FS A15-8 Address Register

Flash/SRAM address bits 15-8

 8381

FS A19-16 Address Register

reserved	Flash/SRAM address bits 19-16
----------	-------------------------------

 8382

These read/write registers specify the address of the byte to be accessed within the flash or SRAM array when the data register is accessed. Since the SRAM contains 32 KB, only the 15 low-order address bits are pertinent to it. Since the flash memory contains 512 KB, only the 19 low-order address bits are pertinent. Address bit 19 is provided for possible future expansion.

Flash Data Register

--

 8383

This read/write register is used to access the byte in the flash memory array addressed by the FS address registers. A read returns the value of the addressed byte if bit CDEN in the memory control register is set; otherwise the read returns an unpredictable value. A write to this register writes to the addressed byte if bit CDEN is set and if the flash write-protect jumper is not installed on the board. Note however that flash memory cannot simply be written; one has to go through a complex erasing and programming sequence. To alter the flash memory, either consult Intel's datasheets on the 28F0x0 flash memory devices or use the software available with the EPC-6.

EPC-6 HARDWARE REFERENCE

SRAM Data Register



8384

This read/write register is used to access the byte in the nonvolatile SRAM array addressed by the FS address register. The BIOS and ROM DOS use the upper 2 KB of the SRAM array to communicate error messages to the setup program. Thus the user should consider the SRAM as a 30 KB array.

LED Register

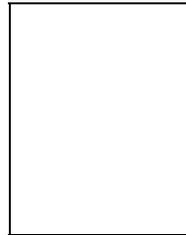


8385

The LED register is a read/write register that controls the seven-segment display and reset toggle switch on the front panel.

LEDx These bits control the segments of the LED seven-segment display as shown to the right. The segment is lit when the corresponding bit is 0.

TSEN This bit controls both the decimal point on the LED display and the front-panel toggle switch. When the bit is 0, the decimal point is lit and the front-panel switch is disabled. This bit can be used to prevent an inadvertent reset from the front-panel switch.



Register State after Reset

A hardware reset of the EPC-6 (not a keyboard CTRL+ALT+DEL reset) clears all of the register bits to 0, except for RELM, ARBM, ARBPRI, TSEN, and the registers at ports 8130 and 8151, which may be in an undefined state. (All bits, however, are cleared by a power-on reset.)

The above is not apparent, however, because the BIOS initialization sequence stores values in these register fields, largely as a result of the nonvolatile configuration information specified in the setup screen.

The BIOS clears the interrupt and event enable registers.

EPC-6 HARDWARE REFERENCE

VMEbus Accesses

Two C-language examples are given here for performing VMEbus accesses through the E page. The first performs a 16-bit read from the VMEbus A16 space. It requires setting the address modifier, relocating the A16 address into the E page (address range E0000-EFFFF), and then accessing the value pointed to by a C pointer variable.

```
#define WORD unsigned short
#define LWORD unsigned long

WORD addr; /* 16-bit A16 address */
WORD data;
WORD far * wptr;

outp(0x8151,0x0A); /* Set address modifier to A16 supervisory access */
wptr = (WORD far *) (0xE000000L + addr);
data = *wptr; /* Read through window */
```

The next example does a byte write into the VMEbus A24 space. Here the upper 8 bits of the VME address need to be stored in the appropriate registers.

```
LWORD addr; /* 32-bit A24 address */
BYTE data;
BYTE far * wptr;

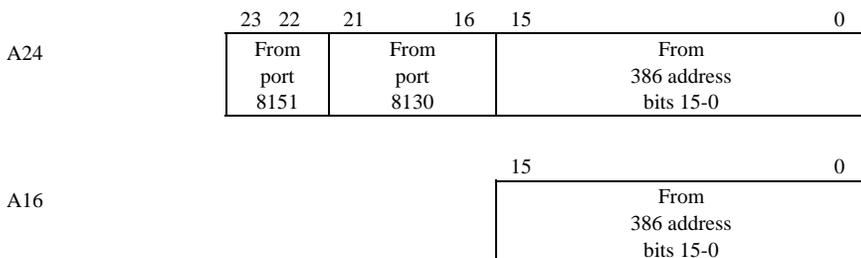
outp(0x8151,6 | (((addr << 8) >> 30) << 6));
/* A23-A22 and address modifier for A24 supervisory data access */
outp(0x8130,(WORD)((addr << 10) >> 24); /* A21-A16 */
wptr = (BYTE far *) (0xE000000L + (addr & 0X0000FFFFL));
*wptr = data; /* Write through window */
```

The success of the access can be checked either by enabling BERR as an interrupt or by looking at the BERR bit in the event state register after each access. Since writes are pipelined, software that looks at the BERR bit should first wait until the DONE bit is set.

It is recommended that rather than performing accesses in this low-level hardware dependent form, the Bus Manager component of the EPConnect software package be used instead.

The following summarizes the source of the VMEbus address lines for accesses through the E page.

EPC-6 HARDWARE REFERENCE



D32 Accesses

Although the 386SX is a 32-bit processor (e.g., 32-bit registers and operations), its external data bus is 16 bits wide. Any memory operation with an operand width of 32 bits is broken apart by logic in the processor to two 16-bit operations. As a result, the EPC-6 never performs a VMEbus D32 access.

Byte Ordering

Unlike EPCs having 32-bit buses, EPC-6 does not contain software-controlled byte-ordering hardware. The principal reason is that, as described in the previous section, EPC-6 never performs VMEbus D32 accesses, and therefore there is no feasible way in hardware to support both forms of byte ordering on what a program would see as a 32-bit access.

EPC-6 accesses the VMEbus in little-endian (Intel) byte ordering, meaning that, for a 16-bit numerical value, the least-significant byte is assumed to be at the lowest memory address. This means, for instance, that if a big-endian processor (e.g., Motorola 680x0) stored the 16-bit value 0102h, the EPC-6 would interpret its value as 0201h. If a big-endian processor stored the 32-bit value 01020304h and it were fetched by a program on the EPC-6 as a 32-bit operand (meaning, as explained above, the EPC-6 would perform two 16-bit accesses), the EPC-6 program would see the value as 04030201h.

The EPCConnect Bus Manager software provides functions for swapping byte ordering during memory-copy operations.

Read-Modify-Write Operations

VMEbus RMW (read-modify-write) cycles can be performed through use of the 386SX's LOCK instruction prefix with certain instructions. All of these instructions

EPC-6 HARDWARE REFERENCE

perform a read followed by a write. When such a read occurs that is mapped to the VMEbus, the EPC-6 treats it as the start of a VME RMW cycle. The next VME access from the 386SX is treated as the write that terminates the RMW cycle. For this reason, RMW accesses that cross a 16-bit boundary will not behave as expected (because the 386SX issues two read accesses).

EPC-6 HARDWARE REFERENCE

Slave Accesses from the VMEbus

When SLE in the status/control register is set, the EPC-6 will respond to accesses in a 4 MB range of the A24 space. All types of VME accesses (reads, writes, and read-modify-writes of all lengths) are supported, except for block transfer cycles and D32 accesses. The address modifier can specify supervisory, nonprivileged, program, or data.

The 4 MB space occupied by the EPC-6 in the VMEbus A24 space has the same view of EPC-6 memory as the 386SX, except that only those accesses that map to EPC-6 DRAM memory are valid; all others respond with BERR. The following table shows how the EPC-6 responds to the low-order 22 bits of the 24-bit VME A24 address. WPRT is the flag in the memory control register.

22-bit address from VME	Response
000000 - 09FFFF	DRAM access
0A0000 - 0BFFFF	BERR
0C0000 - 0C7FFFF	DRAM access if read and WPRT=1 or write and WPRT=0 BERR otherwise
0C8000 - 0EFFFF	BERR
0F0000 - 0FFFFFF	DRAM access if read, or if write and WPRT=0 BERR otherwise
100000 - 13FFFF	DRAM access
140000 - 3FFFFFF	DRAM access if 4 MB EPC-6 BERR if 1 MB EPC-6

Self Accesses Across the VMEbus

Since the EPC-6's DRAM can be mapped into the VMEbus A24 address space, the EPC-6 can access its DRAM in an alternate way - by generating VMEbus accesses to the appropriate addresses. This can be of use in multiple-processor systems where some of the EPC-6's DRAM is used as shared global memory; it means that the EPC-6 can access the global memory with the same addresses as used by other processors without needing to understand that the memory is actually on-board.

This ability is also useful in system checkout (i.e., checking operation of the backplane).

A24 slave accesses result in accesses to the on-board DRAM and never to the cache. Because the EPC-6's cache is a write-through cache, there is never a discrepancy

EPC-6 HARDWARE REFERENCE

between data in the cache and the DRAM. When a slave access results in a *write* into the DRAM, the EPC-6 automatically purges the cached entry, if it exists.

Given the above, another subtle use for the ability of the EPC-6 to access its own DRAM via a VMEbus access is selective purging of the cache. For instance, if the EPC-6 is mapped at address base 400000 in the A24 space and a program wishes to purge location 00AB00 from the cache, a read from local address 00AB00 followed by a write of the read data to VME address 40AB00h will accomplish the task.

Read-Modify-Write Operations

The EPC-6 provides synchronization integrity in its local DRAM between accesses from the 386SX into the DRAM and RMW VME accesses from other masters into the DRAM.

When a VMEbus slave read access occurs to the local DRAM, the EPC-6 watches the VMEbus data and address strobes to determine if the cycle is an RMW cycle. If it is, accesses by the 386SX are held up until the terminating access of the RMW cycle occurs.

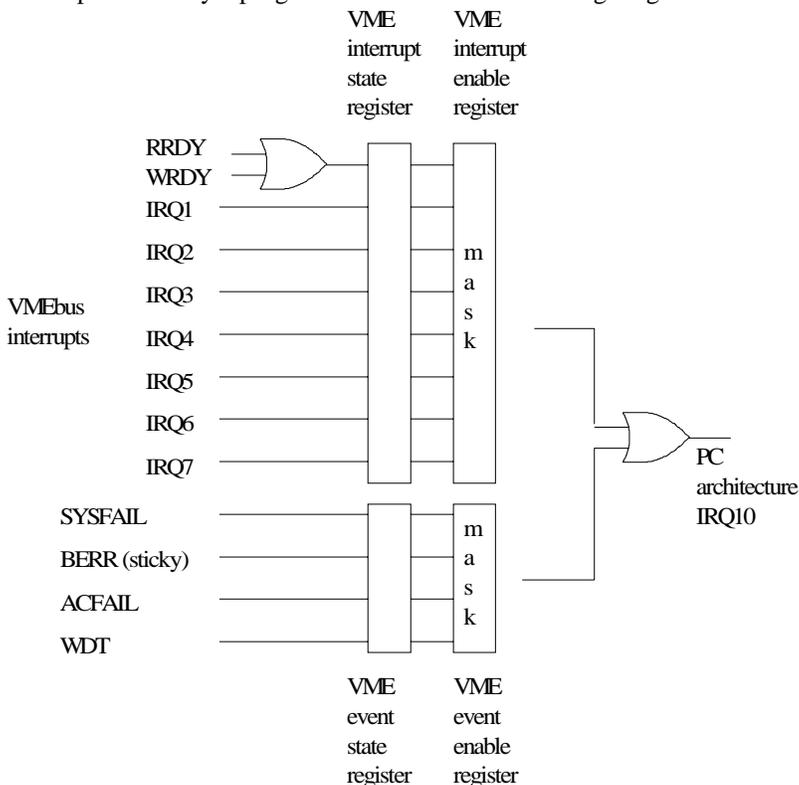
When the 386SX performs a locked access (e.g., via an instruction using the LOCK instruction prefix) to the local DRAM, VMEbus slave accesses are held up until the last locked access completes.

EPC-6 HARDWARE REFERENCE

VMEbus Interrupt Handler

Although software available for the EPC-6 shields the user from the details of interrupt handling, the following information is provided for the reader who needs further detail.

The relationship between VME interrupts (and other interrupt-causing events) and an interrupt as seen by a program is shown in the following diagram.



Interrupts and events are visible in two state registers. These are unlatched, meaning that a read of the state register shows the actual state of the signals at the instant of the read. The exception is BERR, which is a "sticky" bit, meaning that the bit signifies whether BERR had ever been asserted. The convention used is that a 0 bit signifies an asserted (interrupting) state.

The primary purpose of the state registers is to let the interrupt handler software determine which interrupts and events generated the IRQ10 interrupt to the processor.

EPC-6 HARDWARE REFERENCE

The state registers can also be read by non-interrupt-handler software to poll for the state of these signals.

The enable registers allow one to mask selectively these 12 states. A 0 state bit and a corresponding 1 enable bit causes the PC architecture IRQ10 interrupt to be asserted.

Unlike the 12 input conditions, which are level sensitive inputs, the PC architecture defines the PC interrupts, such as IRQ10, as edge sensitive. This requires special attention if you are writing your own interrupt handlers (e.g., if you are not using the functions in the Bus Manager software). Because IRQ10 is edge triggered, you could miss an incoming interrupt/event that occurs when IRQ10 is disabled, meaning that your software needs to test for and handle all pending interrupts/events before you leave from the IRQ10 interrupt handler. To do this correctly, follow the following steps. These steps assume the reader is familiar with the programming of the 8259 interrupt controller in the PC architecture.

1. When the IRQ10 interrupt occurs, acknowledge the interrupt by sending end-of-interrupt to both 8259 interrupt controllers.
2. Depending on your environment, you may wish to switch to another stack (a must under DOS), and may wish to save the state of the VME modifier and address registers if you will be using them.
3. To prevent reentry to the interrupt handler, mask off all the interrupts/events or mask off the IRQ10 interrupt. (Reenable what you have masked off at the end of the interrupt handler.)
4. Find an enabled pending interrupt/event.
5. If an enabled pending VMEbus interrupt is found, do an interrupt-acknowledge cycle by setting the IACK bit in the VME modifier register and performing a VMEbus read, setting address bits A3-A1 to denote the interrupt number. This returns the status/ID value from the interrupter. For the other controllable conditions (message, sticky BERR, watchdog timer), you may follow the instructions earlier in this chapter to remove these interrupting conditions.
6. Perform application-dependent handling of the interrupt/event.
7. If there are still enabled pending interrupts/events, go to step 4. If not, return from the IRQ10 interrupt handler.

EPC-6 HARDWARE REFERENCE

VMEbus Interrupt Response

When the EPC-6's interrupt generator register is used to assert an interrupt, the EPC-6 formulates a status/ID value that is transmitted on the bus as the response to a matching interrupt acknowledgement cycle. The EPC-6 acts as both a D08(O) and D16 interrupter. For D08 interrupt acknowledge cycles, the status/ID value is the EPC-6's logical address (1111aaa, where aaa is the value of ULA as defined in port 814A). For D16 interrupt-acknowledge cycles, the status/ID value consists of 16 bits. The upper eight bits are the upper half of the response register (the value in I/O port 814B) and the lower eight bits are the logical address.

VMEbus Mapped Registers

EPC-6 follows the lead of the VXIbus specification in defining a standard set of configuration registers that are mapped into the VMEbus A16 space and thus accessible by other VMEbus modules. These registers are 16-bit registers occupying 64 bytes of A16 space at a base address defined by the EPC-6's logical address. The base address is

1111 111a aa00 0000

where aaa is the value of the ULA field in the response register at I/O port 814A.

The VME-mapped registers are a subset of those defined previously as I/O ports in the EPC-6. The registers are dual-ported in that they are accessible both from VME and from within the EPC-6 as ports in its I/O space. The VME mapped registers are defined below.

Offset	Upper byte	Lower byte
0	ID (8141)	ID (8140)
2	Device type (8143)	Device type (8142)
4	Status/control (8145)	Status/control (8144)
6	Slave offset (8147)	Slave offset (8146)
8	Protocol (8149)	Protocol (8148)
A	Response (814B)	Response (814A)
C	Message high (814D)	Message high (814C)
E	Message low (814F)	Message low (814E)

EPC-6 HARDWARE REFERENCE

The registers occupy the first 16 bytes of the 64-byte space; the remainder of the space is undefined. (Actually, the registers are mapped into each 16-byte chunk of the 64-byte space.)

Reads and writes of the registers from VME and as I/O ports have identical results and effects except for the following:

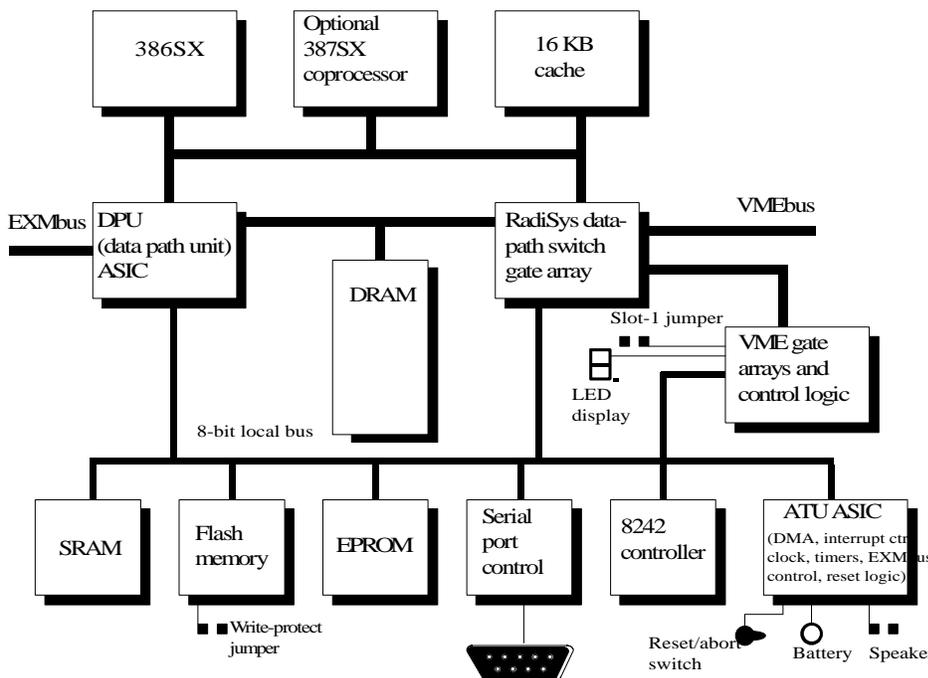
1. Changing the RELM, ARBPRI, and ARBM fields of the status/control register from VME will appear to have changed the fields (i.e., if the register is then read), but the new values will not effect the EPC-6's bus-control logic. To use these fields for their intended purpose, they must be set by I/O port accesses.
2. A read of the response register from VME clears the LOCK bit (immediately after the current value of the response register is returned).

EPC-6 HARDWARE REFERENCE

NOTES

5. Theory of Operation

This chapter specifies other information about the operation of the EPC-6 that might be useful to the system designer. The following diagram shows the major elements of the EPC-6 and data paths among them.



EPC-6 HARDWARE REFERENCE

Processor, Coprocessor, Memory

The processor is an Intel 80386SX, with an internal 32-bit architecture and an external 16-bit data bus. The optional coprocessor is an 80387SX.

There are two factory-installed DRAM options - 1 MB and 4 MB. The DRAM consists of permanently installed ZIP memory devices and thus the size cannot be altered after purchase. The DRAM has byte-wide parity.

ROM and ROM Shadowing

EPC-6 contains a 27020 byte-wide ROM or EPROM. Whether a specific EPC-6 contains a non-reprogrammable ROM or an EPROM is the choice of the manufacturer. Since the ROM/EPROM area of the address space (F80000-FFFFFF) is 512 KB and the 27020 is 256 KB, the 27020 is mapped twice, into F80000-FBFFFF and FC0000-FFFFFF. The EPROM contains the PC BIOS, selftest program, setup screen program, and a ROM version of MS-DOS.

The design can also accommodate a 512 KB 27040 ROM/EPROM.

For best possible performance, the BIOS initialization software copies the BIOS sections of the ROM into DRAM (called shadowing). DRAM at addresses 0F0000-0FFFFFF (the "F page") is used. After this copying is performed, the BIOS sets the WPRT bit in the memory control register to write-protect this area of DRAM.

Cache

The cache is a 16 KB two-way set-associative cache using the 82385SX cache controller. As described in Chapter 4, logic associated with the cache determines what to cache based on address range. Basically, things that can safely be cached are cached, and things that cannot be safely cached are not. This means that the EPC-6's DRAM is cached, but addresses mapped to the VMEbus (which could contain memory mapped I/O devices) are not cached. For the EXMbus, both capabilities are provided; addresses below 800000 are cached and addresses above 800000 are not.

EPC-6 HARDWARE REFERENCE

Since the VMEbus environment can contain multiple processors that access the EPC-6's memory, cache coherency (ensuring that the cache is truly transparent such that stale or out-of-date data isn't accessed) is vital. This is achieved in the following ways:

1. The cache is a write through cache, meaning that memory writes from the 386 that hit the cache (find the addressed location in the cache) also write into the DRAM.
2. Address ranges mapped out to the VMEbus are not cached (e.g., if memory contained on another processor module were cached upon access by the EPC-6 in the EPC-6, there would be no way to determine whether the other processor subsequently changed the memory values).
3. The cache performs "bus watching" on write accesses from another VMEbus master to the EPC-6's memory. If another processor writes into a memory location that is cached, the entry is purged from the cache (so that a subsequent read of the location from the EPC-6 fetches the updated value from memory).

Flash Memory

A 512 KB array of nonvolatile flash memory is provided in the form of two 28F020 components. The flash memory is mapped into its own address space beginning at address 0. This address space is accessible through address and data registers in the I/O space.

The intent of the flash memory is to hold application programs in a standard file-system format, as opposed to being directly user accessible. Software drivers are provided with the EPC-6 for this purpose.

Nonvolatile SRAM Memory

A 32 KB array of nonvolatile SRAM memory is provided. The SRAM is mapped into its own address space beginning at address 0. This address space is accessible through address and data registers in the I/O space.

The BIOS and ROM DOS use the upper 2 KB of the SRAM array to communicate error messages to the setup program. Thus the user should consider the SRAM as a 30 KB array. Information in the upper 2 KB of the SRAM memory runs the risk of getting

EPC-6 HARDWARE REFERENCE

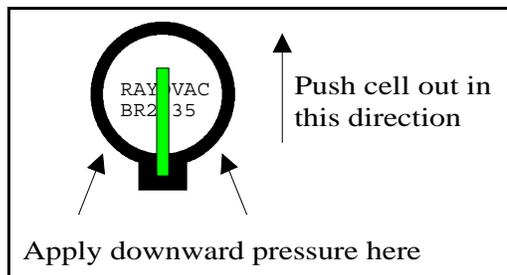
destroyed by the BIOS after a reset. Writing into the upper 2 KB of SRAM memory runs the risk of destroying error messages saved for the setup program.

Battery

The battery powers the CMOS RAM and TOD clock when system power is not present. At 60°C, the battery should have a shelf life of over four years. In a system that is powered on much of the time and where the ambient power-off temperature is less than 60°C, the battery is estimated to have a life of 10 years.

The battery holder is for a 23 mm coin cell, such as a Panasonic BR2330 or Rayovac BR2335.

To remove or replace the battery, first remove the EXM card guide above the battery by removing its three mounting screws. The battery cell is held in place by a spring lever. To remove the battery, apply downward pressure to the cell in the vicinity of the base of the spring (a small screwdriver may be used), while at the same time applying lateral pressure to the cell in the direction away from the spring base.



A new cell is installed by sliding it beneath the spring until it snaps into the holder. Ensure that the spring has not been damaged and that it is in firm contact with, and applying downward pressure on, the battery cell.

EPC-6 HARDWARE REFERENCE

Interrupts and DMA Channels

The assignment of interrupts is shown in the following table:

NMI	DRAM parity error, EXMbus I/O channel check
IRQ0	timer
IRQ1	8242 controller
IRQ3	COM2 serial port
IRQ4	COM1 serial port
IRQ5	unassigned
IRQ6	unassigned
IRQ7	unassigned
IRQ8	clock
IRQ9	unassigned
IRQ10	VME interrupt/event
IRQ11	front-panel toggle switch
IRQ12	unassigned
IRQ13	coprocessor
IRQ14	unassigned
IRQ15	unassigned

The assignment of DMA channels is shown in the following table.

0	unassigned	5	unassigned
1	unassigned	6	unassigned
2	unassigned	7	unassigned
3	unassigned		

EPC-6 HARDWARE REFERENCE

Watchdog Timer

EPC-6 contains a continually running timer having a period of approximately either 8 seconds or 250 milliseconds (software selectable). The watchdog timer event is generated whenever the period expires. This event may be enabled as a source of the IRQ10 interrupt or as a complete reset. The timer is reset to its maximum value by an I/O write to the module status/control register.

EXMbus

The EXMbus, an I/O expansion bus, is provided on a connector to allow the user to insert one EXMbus module. The EXMbus is very similar to the PC/AT ISA I/O bus. In addition, it contains a signal -EXMID used for dynamic recognition and configuration of EXMs. EXMs respond to one or more I/O addresses in the range 100h - 107h only when their -EXMID line is asserted. EXMs are required to return a unique EXM-type identification byte in response to a read from I/O address 100h. Since the EPC-6 has only a single EXM slot, its -EXMID line is wired as asserted.

Although IRQ11 is on the EXMbus, IRQ11 is also used by the reset/abort toggle switch and is driven by a totem-pole driver that has no tristate. Thus the IRQ11 interrupt is not available to EXM modules.

Further information on the EXMbus, its connectors, and standards for building EXMs is available upon request.

8242 Microcontroller

Although the EPC-6 has no PC-compatible keyboard interface, it does contain an 8242 microcontroller programmed as a keyboard controller. The reason is that the keyboard controller in the IBM PC architecture performs some other crucial roles not associated with keyboard control.

EPC-6 HARDWARE REFERENCE

VMEbus Interface

The EPC-6 connects to the VMEbus J1 connector. All of the VMEbus signals and voltages on this connector are used except for SERCLK, SERDAT, and +5V STDBY.

The EPC-6, when configured as an A24 slave, responds with BERR if another bus master attempts a D32 access into the EPC-6's memory. It also responds with BERR if another master does an access that would map to other than DRAM within the EPC-6.

The EPC-6 does address pipelining in one circumstance - when the EPC-6 has been granted the bus while some other master is performing a bus cycle. In this circumstance the EPC-6 will start its cycle (i.e., drive AS* low) before the other master has removed its data strobes (i.e., before DS0* and DS1* are driven high).

The EPC-6 performs write pipelining of 386 write cycles to the VMEbus. The VME control logic signals completion to the 386 of a write cycle that is mapped to the VMEbus as soon as the VMEbus AS* signal has been driven low and the data from the 386 has been latched.

EPC-6 HARDWARE REFERENCE

VMEbus System Controller Functions

When the EPC-6 is configured as the VMEbus system controller, it performs the standard VMEbus system controller functions. It serves as the bus arbiter (priority or round robin), drives the 16 MHz SYSCLK signal, and starts the IACK daisy chain.

The SYSFAIL LED is operable only when the EPC-6 is configured as the system controller.

When configured as the system controller, the EPC-6 also detects and terminates bus timeouts. Once it sees either of the DS0 and DS1 lines asserted, a counter is started. If the counter expires before both DS0 and DS1 are deasserted, the EPC-6 asserts the VMEbus BERR signal until both data strobes are deasserted. The duration of the counter is approximately 100 microseconds.

VMEbus Timing

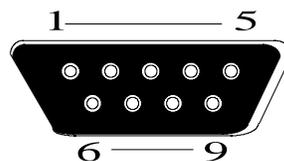
The following table contains some illustrations of the duration of VMEbus operations. The times were measured with the EPC-6 in the ROR bus-release mode.

Operation	Time
Fill VMEbus slave memory, each iteration of REP,STOSW instructions	300 ns + DS-DTACK slave's write access time
Move block of local memory to VMEbus slave memory, each iteration of REP,MOVSW instructions	400 ns + the greater of: 50 ns slave's DS-DTACK write access time
Move block of VMEbus slave memory to local memory, each iteration of REP,MOVSW instructions	650 ns + DS-DTACK slave's read access time
Write access from another master to EPC-6's DRAM	DS-DTACK time = 325 ns+ HI HI is hold-interference time, can range from 0 to 15000 ns, typically is 150 ns
Read access from another master to EPC-6's DRAM	DS-DTACK time = 450 ns + HI HI as defined above

6. Connectors

This chapter specifies the details of the connectors and headers on the EPC-6. The EXMbus connector is not defined here; its definition is available upon request.

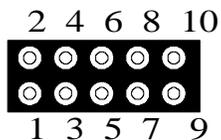
The DB-9 COM1 serial port connector is defined in the following table.



Pin	Signal	Pin	Signal
1	Carrier detect	6	Data set ready
2	Receive data	7	Request to send
3	Transmit data	8	Clear to send
4	Data terminal ready	9	Ring indicator
5	Signal ground		

A second serial port, addressable at PC serial port COM2, exists in

the form of a 10-pin header on the printed-circuit board near the bottom of the front panel. Pin 2 is the pin closest to the front panel and the bottom. The header is defined as



Pin	Signal	Pin	Signal
1	Carrier detect	6	Clear to send
2	Data set ready	7	Data terminal ready
3	Receive data	8	Ring indicator
4	Request to send	9	Signal ground
5	Transmit data		unconnected

EPC-6 HARDWARE REFERENCE

The speaker header on the EPC-6 circuit board is defined as

Pin	Signal	Pin	Signal
1	Reference voltage	2	Speaker tone

VMEbus Connectors

EPC-6 has a standard VMEbus P1 connector. It does not access the P1 pins +5VSTDBY, SERCLK, and SERDAT.

7. Error Messages

This chapter contains a summary of error and warning messages alphabetized by message text. These are messages generated by the BIOS and MS-DOS that may be related to your hardware configuration.

CMOS checksum invalid

Something in the nonvolatile CMOS RAM is incorrect. Run the BIOS setup program to determine what is wrong, and correct it. If the error occurs repeatedly, the EPC-6's battery has failed.

CMOS RAM error, check battery / run setup

Something in the nonvolatile CMOS RAM is incorrect. Run the BIOS setup program to determine what is wrong, and correct it. If the error occurs repeatedly, first try reinitializing all CMOS RAM parameters. If the problem still occurs, the EPC-6's battery has failed.

EXM configuration error

The EXM installed (or not installed) does not match the configuration information in the nonvolatile CMOS RAM. Hitting any key will allow you to continue, but doing so may cause problems later if software tries to use the EXM. To correct the problem, enter the setup program (via CTRL+ALT+ESC) to change the information on the setup screen and reboot.

Memory parity interrupt at ...

This could be a software error (reading a nonexistent memory area) or a true hardware failure.

Parity error in segment ...

This could be a software error (reading a nonexistent memory area) or a true hardware failure.

EPC-6 HARDWARE REFERENCE

Real time clock error - run setup

The battery-backed TOD clock is incorrect. Run the BIOS setup program to determine what is wrong, and correct it. If the error occurs repeatedly, the EPC-6's battery has failed.

EPC-6 HARDWARE REFERENCE

Seven-Segment Display Codes

The following list shows the two-digit codes displayed in the seven-segment display when a catastrophic selftest failure is detected. The two digits are displayed repeatedly in the following way: first digit, pause, second digit, long pause.

01	Selftest initiation	18	Memory refresh test
02	Chipset initialization	19	Interrupt vector table initialization
03	DRAM controller initialization	1A	does not occur
04	DRAM initialization	1B	does not occur
05	DRAM 0- and F-page test	1C	Interrupt controller test
06	DRAM byte enable logic test	1D	Interrupt controller test
07	Copy ROM	1E	Battery level test
08	Copy ROM	1F	CMOS checksum test
09	Copy ROM	20	Configuration byte initialization
0A	Copy ROM	21	Size system memory
0B	Copy ROM	22	System memory test
0C	Copy ROM	23	Stuck interrupt test
0D	Copy ROM	24	Stuck NMI (parity/IOCHK) bit test
0E	Clear 8042 interface	25	Interrupt controller test
0F	Reset 8042 interface	26	Size extended memory
10	PC hardware initialization	27	Extended memory test
11	Video interface initialization	28	VME interface test
12	Timer test	29	VXI register test
13	CMOS shutdown test	2A	COM1 serial port test
14	DMA test	2B	COM2 serial port test
15	DMA test	2C	Cache test
16	DMA page registers test		
17	does not occur		

EPC-6 HARDWARE REFERENCE

NOTES

8. Support and Service

In North America

Technical Support

RadiSys maintains a technical support phone line at (503) 646-1800 that is staffed weekdays (except holidays) between 8 AM and 5 PM Pacific time. If you have a problem outside these hours, you can leave a message on voice-mail using the same phone number. You can also request help via electronic mail or by FAX addressed to RadiSys Technical Support. The RadiSys FAX number is (503) 646-1850. The RadiSys E-mail address on the Internet is *support@radisys.com*. If you are sending E-mail or a FAX, please include information on both the hardware and software being used and a detailed description of the problem, specifically how the problem can be reproduced. We will respond by E-mail, phone or FAX by the next business day.

Technical Support Services are designed for customers who have purchased their products from RadiSys or a sales representative. If your RadiSys product is part of a piece of OEM equipment, or was integrated by someone else as part of a system, support will be better provided by the OEM or system vendor that did the integration and understands the final product and environment.

Bulletin Board

RadiSys operates an electronic bulletin board (BBS) 24 hours per day to provide access to the latest drivers, software updates and other information. The bulletin board is not monitored regularly, so if you need a fast response please use the telephone or FAX numbers listed above.

The BBS operates at up to 14400 baud. Connect using standard settings of eight data bits, no parity, and one stop bit (8, N, 1). The telephone number is (503) 646-8290.

EPC-6 HARDWARE REFERENCE

Repair Services

Factory Repair Service is provided for all RadiSys products. Standard service for all RadiSys products covers factory repair with customers paying shipping to the factory and RadiSys paying for return shipment. Overnight return shipment is available at customer expense. Normal turn-around time for repair and re-certification is five working days.

Quick Exchange services (immediate shipment of a loaner unit while the failed product is being repaired) or other extra-cost services can be arranged, but need to be negotiated in advance to allow RadiSys to pool the correct product configurations. RadiSys does not maintain a general "loaner" pool: units are available only for customers that have negotiated this service in advance.

RadiSys does not provide a fixed-price "swap-out" repair service, as customers have indicated that issues of serial number tracking and version control make it more convenient to receive their original products back after repair.

Warranty Repairs

Products under warranty (see warranty information in the front of this manual) will have manufacturing defects repaired at no charge. Products sent in for warranty repair that have no faults will be subject to a recertification charge. Extended Warranties are available and can be purchased at a standard price for any product still under warranty. RadiSys will gladly quote prices for Extended Warranties on products whose warranties have lapsed; contact the factory if this applies.

Customer induced damage (resulting from misuse, abuse, or exceeding the product specifications) is not covered by the standard product warranty.

Non-Warranty Services

There are several classes of non-warranty service. These include repair of customer induced problems, repairs of failures for products outside the warranty period, recertification (functional testing) of a product either in or out of warranty, and procurement of spare parts.

All non-warranty repairs are subject to service charges. RadiSys has determined that pricing repairs based on time and materials is more cost-effective for the customer than a flat-rate repair charge. When product is received, it will be analyzed and, if appropriate, a cost estimate will be communicated to the customer for authorization.

EPC-6 HARDWARE REFERENCE

After the customer authorizes the repair and billing arrangements have been made, the product will be repaired and returned to the customer.

A recertification service is provided for products either in or out of warranty. This service will verify correct operation of a product by inspection and testing of the product with standard manufacturing tests. There is a product-dependent charge for recertification.

There are only a few components that are generally considered field-repairable, but, because RadiSys understands that some customers want or need the option of repairing their own equipment, all components are available in a spares program. There is a minimum billing charge associated with this program.

Arranging Service

To schedule service for a product, please call RadiSys Technical Support directly at (503) 646-1800. Have the product model and serial numbers available, along with a description of the problem. A Technical Support representative will issue a Returned Materials Authorization (RMA) number, a code number by which we track the product while it is being processed. Once you have received the RMA number, follow the instructions of the Technical Support representative and return the product to us, freight prepaid, with the RMA number clearly marked on the exterior of the package. If possible re-use the original shipping containers and packaging. In any case, be sure you follow good ESD-control practices when handling the product, and ensure that anti-static bags and packing materials with adequate padding and shock-absorbing properties are used.

Ship the product, freight prepaid, to the following address:

Product Service Center
RadiSys Corporation
15025 SW Koll Parkway
Beaverton, Oregon 97006-6902

When shipping the product, include the following information: return address, contact names and phone numbers in purchasing and engineering, and a description of the suspected problem. Any ancillary information that might be helpful with the debugging process will be appreciated.

EPC-6 HARDWARE REFERENCE

Other Countries

Contact the sales organization from which you purchased your RadiSys product for service and support.

Replacement Parts

The following replacement parts can be ordered from the address above. When ordering parts, please include the serial number of your EPC-6.

09-0075	ESD shield for DB-9 connector
10-0071	Blank EXM face plate with thumbscrews
07-0082	EPC-6 Hardware Reference Manual
75-0268	20MHz 80387SX floating-point coprocessor
17-0020	Battery

Index

- A16 15,16,42
- A24 15,26,35
- ACFAIL 31,40
- Address modifier 30,35,38
- Address strobe 32
- Altitude 2
- Arbitration 15
- Arbitration mode 27
- Arbitration priority 26

- Backplane jumpers 6,11
- Battery
 - cell type 48
 - failure 55,56
 - header 4
 - holder 48
 - life 48
 - removal 48
 - replacement 48,60
- BERR 31,35,38,40,51,52
- Big endian 36
- BIOS 46
 - configuration data 14
 - initialization 7-9
 - ROM 17
 - use of SRAM 34,48
 - write protection 25
- Block transfer cycles 38
- Boot device 7
- Bus arbiter 52
- Bus error 31
- Bus grant 11
- Bus Manager 35,36,41
- Bus monitoring 32
- Bus release 26
- Bus timeout 3,12,52
- Bus watching 18,47
- Bus-release modes 14
- Byte ordering 36

- Cache 18,39,46-47
- CMOS RAM 7,8,48
 - error 55
- COM1 49,53
- COM2 49,53
- Commander 27
- Configuration information 7,8
- Configuration registers 42
- Configuration setup 14
- Coprocessor 46
- Current 2

- D32 access 36,51

EPC-6 HARDWARE REFERENCE

Daisy chain 6
Data strobe 32
Date 14
Debug program 8
Device type register 26
Disk 8,14
DMA channels 49
DRAM options 46
DRAM parity error 49
DRAM write protection 25
Drives 14
Dual-port memory 18

E page 25,30,35
EPC-1 25,36
EPControl 8,10,14
EPROM 46
ESD shield 60
EXM
 bus 46,50
 configuration 16
 configuration bytes 16
 configuration error 55
 ID 16
 insertion 5
 types 6
EXM configuration error 9
EXM-2 14
EXM-3 6
EXM-9 6
EXMbus 50
EXMID signal 50

F page 46
Fast handshake mode 27
Flash memory
 access protection 25,33
 address registers 33
 booting from 7,14
 components 47
 data register 25,33
 jumper 4
 programming) 8
 write protection 4
 write-protect jumper 33
Front-panel indicators 11
Front-panel switch 12
FS address registers 33

Hardware reset 10,34
Humidity 2

I/O space map 19
IACK daisy chain 52
ID register 25
Initialization sequence 7
Interrupt
 acknowledge 6,30,33,42
 assignments 49
 handler 40-42
 IRQ10 31,32,49,50
 IRQ11 12,49
 message 28,31
 MSGR 28,31
 register 31,33
Interrupt generator register 42
Interrupt handler 16
Interrupter 16
IRQ10 interrupt 31,32,40
IRQ11 interrupt 12,50

J1 connector 51
Jumpers 4,6,11

Keyboard controller 50

LED register 34
LEDs 11,52
Little endian 36
Location monitor 28
Lock 28
LOCK instruction prefix 37,39

Master 15

EPC-6 HARDWARE REFERENCE

Master LED 12
Memory control register 25,33
Memory map 17
Memory parity interrupt 55
Message high register 28,29
Message interrupt 31
Message low register 28,29
Message protocol 28
Message register 28
Message-based device 25
Model code 26
Module status/control register 32,50
MS-DOS 7,13
MSGR interrupt 28,31

NMI 49

Operator intervention 8

P1 connector 54
Parity 46
Parity error 55
Park 15
PC/AT I/O bus 50
Pipelined write 32,35
Power 2
Priority arbiter 27
Priority arbitration 15
Priority levels 14
Protocol register 27

Read ready 28
Real time clock error 56
Release on request 14,26
Repair service 59
Replacement parts 62
Request on no request 14,26
Reset 26
Reset disabled indicator 11
Reset switch 11,12,34
Response register 28,31,43
RMA 59

RMW cycle 37,39
ROM 46
ROM DOS 8
ROM DOS interaction 10
ROM shadowing 46
RONR 14,26
ROR 14,26
Round-robin arbitration 15,27

Self accesses 38
Selftest
 codes displayed 57
 execution 7
 failure codes 12
 PASS LED 26
Serial port
 cap 6
 connector 53
 ESD shield 6,60
 header 53
 terminal 10
Servant 27
Setup program 6,7,10,14,48
Seven-segment display
 decimal point 11,34
 failure codes 57
 purposes 12
 register 34
 rotating pattern 8
 usage during initialization 10
Shock 2
Signal register 27
Slave 15,38,51
Slave access 12
Slave enable 27
Slave LED 12
Slave memory offset 15
Slave offset register 27
Slot 1 3
Speaker header 4,54
SRAM
 address registers 33

EPC-6 HARDWARE REFERENCE

- BIOS usage of 7,48
 - data register 34
 - memory 47
- SRAM BIOS usage of 34
- Stale data 18
- Status/control register 26
- Status/ID value 42
- SYSCLK 3,52
- SYSFAIL 11,27,31,40,52
- SYSFAIL inhibit 26
- SYSRESET 11,27
- SYSRESET input enable 26
- System controller 3,11,15,27,52
- Technical support 59
- Temperature 2
- Time 14
- TOD clock 14,48,56
- Toggle switch 8,12,34,49
- ULA 15,28,42
- Unique logical address *see* ULA
- Vibration 2
- VME A21-16 address register 25
- VME event enable register 32,40
- VME event state register 31,40
- VME interrupt enable register 31,40
- VME interrupt generator register 33
- VME interrupt state register 31,40
- VME mapped registers 42
- VME modifier register 30,41
- VMEbus
 - accesses 35
 - address modifier 30
 - address pipelining 51
 - addressing 2
 - arbiter 2
 - booting from 14
 - connector 51,54
 - interrupt handler 2,16,40-42
 - interrupter 2,16,42
 - jumpers 6
 - master data transfer 2
 - monitoring 32
 - pipelined write 32
 - priority level 14
 - requester 2
 - RMW 37,39
 - slave access 38
 - slave data transfer 2
 - specifications 2
 - system controller 2,52
 - timing 52
 - write 32,35
- VXI
 - fair-requester mode 14
 - register 25,27,42
 - registers 15
 - unique logical address *see* ULA
- Warranty 59
- Watchdog timer 31,32,41,50
- WPRT bit 17,25,38,46
- Write pipelining 51
- Write ready 28
- Write through 47



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