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HARDWARE
REFERENCE

EPC®-6320/21



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Preface

This guide describes EPC-6320 and EPC-6321 (hereinafter referred to as the EPC-6320/21), PrPMCs (Processor PCI Mezzanine Cards) that use the RadiSys 82600 integrated chipset to bring Intel† Architecture processors into ultra-dense form factors. This guide is for hardware and software designers, engineers, and those with a electronics and/or programming knowledge who need to understand EPC-6320/21 operation.

About this Guide

Notational Conventions

This guide uses the following conventions:

`BoldText` A command or keyword.

`MonoText` Screen text and syntax strings.

`ItalicText` Variable parameters.

All numbers are decimal unless otherwise stated.

Bit 0 is the low-order bit. If a bit is set to 1, the associated description is true unless otherwise stated.

Notes	Indicates important information about the product.
Tips	Indicates alternate techniques or procedures that you can use to save time or better understand the product.
URL	Indicates a World Wide Web address.
Book/File	Indicates a book or file.
ESD CAUTION	Indicates situations that may cause damage to hardware via ESD (ElectroStatic Discharge).
CAUTION	Indicates potentially hazardous situations which, if not avoided, may result in minor or moderate injury, or damage to data or hardware. It may also alert you about unsafe practices.
WARNING	Indicates potentially hazardous situations which, if not avoided, can result in death or serious injury.
DANGER	Indicates imminently hazardous situations which, if not avoided, will result in death or serious injury.

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Where to get More Information

About the EPC-6320/21

You can find out more about EPC-6320/21 from these sources:

- Readme file: Lists features and issues that arose too late to include in other documentation.
- **World Wide Web**: RadiSys maintains an active site on the World Wide Web. The site contains current information about the company and locations of sales offices, new and existing products, contacts for sales, service, and technical support information. You can also send e-mail to RadiSys using the web site.

Note

When sending e-mail for technical support, please include information about both the hardware and software, plus a detailed description of the problem, including how to reproduce it.

URL

To access the RadiSys web site, enter this URL in your web browser:

`http://www.radisys.com`

Requests for sales, service, and technical support information receive prompt response.

- Other: If you purchased your RadiSys product from a third-party vendor, you can contact that vendor for service and support.

About Related RadiSys Products

82600 High Integration Dual PCI System Controller Data Book: This book details the RadiSys 82600 High Performance System Controller, a member of the RadiSys family of long-life embedded PC compatible core logic. The 82600 is a highly integrated single chip implementation of all requirements of a high performance Compact PCI Central Resource and Peripheral Bridge including the North Bridge, South Bridge, PCI to PCI Bridge, and a selected set of Super I/O functions targeted at embedded, PC-compatible systems. It supports Intel Celeron†, Pentium II, and Pentium III processors with 66MHz, 100MHz and 133MHz system bus frequencies.

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About Related EPC-6320/21 Components

Processor PMC standard, VITA 32-2002, Draft 0.9.

ANSI/VITA 32-2003 American National Standard for Processor PMC, Revision 1.0: .

PCI Specification, Revision 2.2.

PTMC PICMIG 2.15 Standard: .

IEEE Standard for a Common Mezzanine Card Family: CMC and IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC, IEEE, Standard No.: 1386-2001 and 1386.1-2001PICMG 2.15 R1.0:ECN 2.15-1.0-001PCI Telecom Mezzanine/Carrier Card Specification, PICMG.

PICMG 3.0 D1.0 Advanced Telecommunications Computing Architecture (ATCA), PICMG.

Other

- For MV Linux† LSPs, contact MontaVista at this URL:

  http://www.mvista.com

- For VxWorks† BSPs, contact RadiSys or WindRiver

  http://www.windriver.com
  http://www.radisys.com

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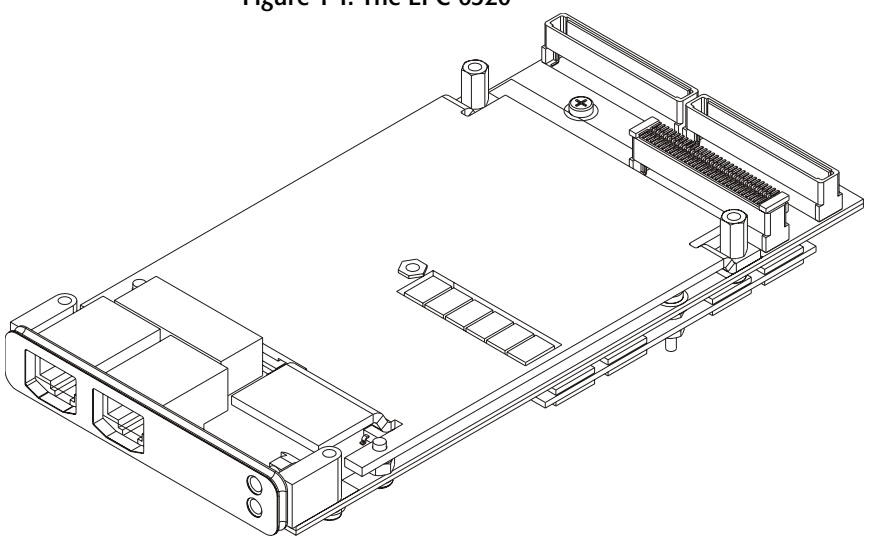
EPC-6320/21 PrPMCs (Processor PCI Mezzanine Cards) use the RadiSys 82600 integrated chipset to bring Intel Architecture processors into ultra-dense form factors.

The EPC-6320/21 includes an 933MHz Pentium† III processor with up to 1GB of on-board SDRAM. The EPC-6320/21 also features ECC protection of memory with single error correction and double error detection capability. Performance is maximized with the standard 133MHz PSB and 133MHz memory bus. For maximum flexibility, the EPC-6320/21 leverages the dual mode PCI-to-PCI bridge capability of the RadiSys 82600 to automatically configure the bridge, based on the strapping of the slot on the baseboard. This capability allows the EPC-6320/21 to become a Monarch PrPMC, and provide PCI bus enumeration and service interrupts on the PCI bus or a non-Monarch PrPMC and function as a PCI-based auxiliary processor.

The Jn1 and Jn2 connectors provide a 32-bit 33/66MHz interface to the PCI bus on the baseboard plus power and ground. The optional Jn4 connector provides a full set of I/O, which includes EIDE, COM, and keyboard interfaces.

- **EPC-6320** provides two standard IEEE 802.3 Ethernet interfaces to the front panel via RJ-45 connectors for 10/100/1000Base-T applications. The EPC-6320 complies with the *Processor PMC standard, VITA 32-2002, Draft 0.9.*
- **EPC-6321** provides two standard IEEE 802.3 Ethernet interfaces to Jn4 PMC connector and complies with the *Processor PMC standard, VITA 32-2002, Draft 0.9.* and *PTMC PICMIG 2.15 Standard.*

Figure 1-1. The EPC-6320



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The EPC-6320/21 can be ordered in these configurations:

Figure 1-2. EPC-6320/21 Ordering Configurations

Configuration		Description	Ethernet
EPC-6320	EPC6320-933-512	512 MB SDRAM	Dual Ethernet ports on the front panel.
	EPC6320-933-1G	1 GB SDRAM	Dual Ethernet ports on the front panel.
EPC-6321	EPC6321-933-512	512 MB SDRAM	Dual Ethernet ports out to Jn4 PICMIG 2.15 compatible pinout.
	EPC6321-933-1G	1 GB SDRAM	Dual Ethernet ports out to Jn4 PICMIG 2.15 compatible pinout.

Features

The EPC-6320/21 includes:

Compatibility

- Processor PMC standard, VITA 32-2002, Draft 0.9.
- PTMC PICMIG 2.15 Standard.
- ANSI/VITA 32-2003 American National Standard for Processor PMC, Revision 1.0.

Intel Tualatin LP processors in micro-FCBGA package

- 933 MHz core frequency.
- 133 MHz PSB (Processor Side Bus) frequency.
- 512 KB integrated cache on die.
- Thermal design power of 12W for 933 MHz processor.
- Switching power supply for CPU core voltage; linear supplies for interface voltages.

CPU subsystem

- RadiSys 82600 high integration dual PCI system controller:

  For detailed information about the 82600 chip, see the *82600 High Integration Dual PCI System Controller Data Book*.

  - Dual independent PCI bus architecture.
  - Monarch and non-Monarch capability on BPCI bus.
  - Memory controller.
  - Two 82C59 interrupt controllers.
  - 82C54 timer/counter.
  - 74LS612 address mapper.
  - PS/2 compatible keyboard.
  - SMBus host interface.

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- Two 82C37 DMA controllers.
- Real-Time Clock (RTC).
- COM port support with 16550 compatible UART.
- Integrated watchdog timer.

- Clock generator that supports 133 MHz host and SDRAM clocks, and 66 MHz PCI clocks.
- On-board memory capacity up to 512 MB or 1 GB of PC-133 compliant SDRAM using Unigen memory module.
- 32 Mb (4 MB) +3V Intel StrataFlash memory.
- IDE support via Jn4 connector.

I/O

- Intel PCI Ethernet controller independently supporting 10/100/1000BASE-T.

Connectors

- Carrier card
  - Jn1 and Jn2 connectors
    Provides a 32-bit 33/66 MHz interface to the PCI bus on the baseboard, plus provides power and ground state compatible with the *ANSI/VITA 32-2003 American National Standard for Processor PMC, Revision 1.0*.
  - Jn4 connector (optional)
    Provides a full set of I/O including EIDE, COM, and port signals.
- Front panel
  - 10/100/1000BASE-T Ethernet connector
    Simplifies network connections. This connector is available on the front panel.

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Specifications

Environmental

The EPC-6320/21 meets the following environmental specifications.

⚠ CAUTION

- Use the EPC-6320/21 only with compatible UL Listed computers that have installation instructions that details user installation of card cage accessories.
- Ensure that the operating environment provides sufficient airflow (200 LFM) across the CPU board to keep it within its temperature specification. Failure to provide sufficient airflow may result in CPU failure.

Note

The maximum temperature decreases when the relative humidity exceeds 30%.

Table 1-1. Environmental Specifications

Parameter	Conditions	Detailed specification
Temperature (ambient)	Operating	+0ºC to 50ºC derated 2ºC per 1000 ft (300 m) over 6600ft (2000m).
	Storage	–20ºC to +60ºC.
Relative humidity	Operating	20% to 90% non-condensing 20% per hour maximum excursion gradient. NEBS[2] requires 85% operating, 90% short-term (<96 hrs) and transitions at least 15% to 20%/hour.
	Storage	5% to 95% non-condensing 20% per hour maximum excursion gradient. NEBS[2] requires 95% and transitions at least 15% to 20%/hour.
EMC[1] radiated emission	Operating	EN 55022:1998, Class B.
Vibration	Operating	0.04g^2/Hz from 5 to1000 Hz random, 10 min per sweep cycle.
	Storage	0.06g^2/Hz from 5 to1000 Hz random, 10 min per sweep cycle.
Shock, (un-packaged)	Operating	5g, 11ms, half-sine.
	Storage	15g, 11ms, half-sine.
MTBF		373,858 hours at 50ºC using Bellcor Issue 6.
Immunity		
ESD[1]	Operating	(All performance criteria from IEC 1000-4-2/EN61000-4-2:1995): 8KV direct contact, performance criteria B. 15 KV air discharge, performance criteria B. NEBS[2] requires 8kV contact / 2kV+15kV air at performance criteria B.

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Table 1-1. Environmental Specifications

Parameter	Conditions	Detailed specification
Radiated[1]	Operating	(Performance criteria A from IEC 1000-4-3/EN61000-4-3:1995). Test Level 3V/m and 10V/m.
Surge	Operating	(Performance criteria B from IEC 1000-4-4/EN61000-4-4:1995). Test Level 0.5kV.
Voltage dips and interruptions	Operating	(From IEC 1000-4-11/EN61000-4-11:1995): >95% dip, 10ms–Performance criteria B. 30% dip, 500ms–Performance criteria C. >95% dip, 5000ms–Performance criteria C.
Conducted	Operating	(Performance criteria A from IEC 1000-4-6/EN61000-4-6:1995).
Fast transient/burst	Operating	(Performance criteria B from IEC 1000-4-4/EN61000-4-4:1995): Test Level 0.5kV.

1 These are system level tests. Conformance of the product to these specifications may be affected by the complete system's ability to conform.

2 The EPC-6320/21 is screened for NEBS compliance. NEBS certification, if required, is performed at the system level.

Additional Specifications

Table 1-2. Additional EPC-6320/21 Specifications

Characteristic	Value	
Mechanical	Dimensions[1]	74.0 mm x 149.00 mm
	Thickness	1.6 mm
	Connector height	10 mm

1 The PrPMC module's mechanical outline conforms to the dimensions defined by a single-wide, standard-length PMC module. EPC-6320/21 complies with these size standards:

- **Tall PrPMC standards**: EPC-6320/21 height falls between the limits of Standard (3.5 mm) and Tall (23.5 mm for side 2 components), as defined by *Processor PMC standard, VITA 32-2002, Draft 0.9.*
- **ATCA standards**: EPC-6320/21 mechanical height complies with carrier cards that can accomodate a PMC Side 2 height of 8MM, but does not comply with carrier cards of single front panel width (4HP), as defined by *PICMG 3.0 D1.0 Advanced Telecommunications Computing Architecture (ATCA), PICMG.*

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Power

This table includes the power requirements for the 1GB memory SDRAM module.

Table 1-3. Power Estimates

Supply	Max. power, Watts	Typical power, Watts
+5V	13	10
+3.3V	13	11
Total power:	26	21

Note

The PMC specification limits power to 0.5 A per connector pin:

- J1–6 pins +5V: 3A maximum
- J2–9 pins +3.3V: 4.5A maximum

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⚠ ESD CAUTION

Avoid causing ESD (electrostatic discharge) damage by following these conventions:

- Keep the blade in its anti-static bag until you are ready to install it.
- Install the blade (as described later in this chapter) only in a static-free environment:
  - Before touching the blade, attach an ESD wrist strap to your wrist and connect its other end to the ESD friction-lock connector at the shelf's lower left.
  - Remove the blade from its antistatic bag only in a static-free environment.
  - Avoid touching printed circuits, connector pins, and components. Where possible, hold the blade only by its edges or mounting hardware.
  - Make the least possible movement with your body to minimize electrostatic charges created by contact with clothing fibers, carpet, and furniture.
  - Keep one hand on the shelf, if possible, as you insert or remove a blade.
  - Avoid placing the blade on the shelf cover or on a metal table. The cover and metal table increase the risk of damage because they provide an electrical path from your body through the blade.

The EPC-6320/21, like most other electronic devices, is susceptible to ESD damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

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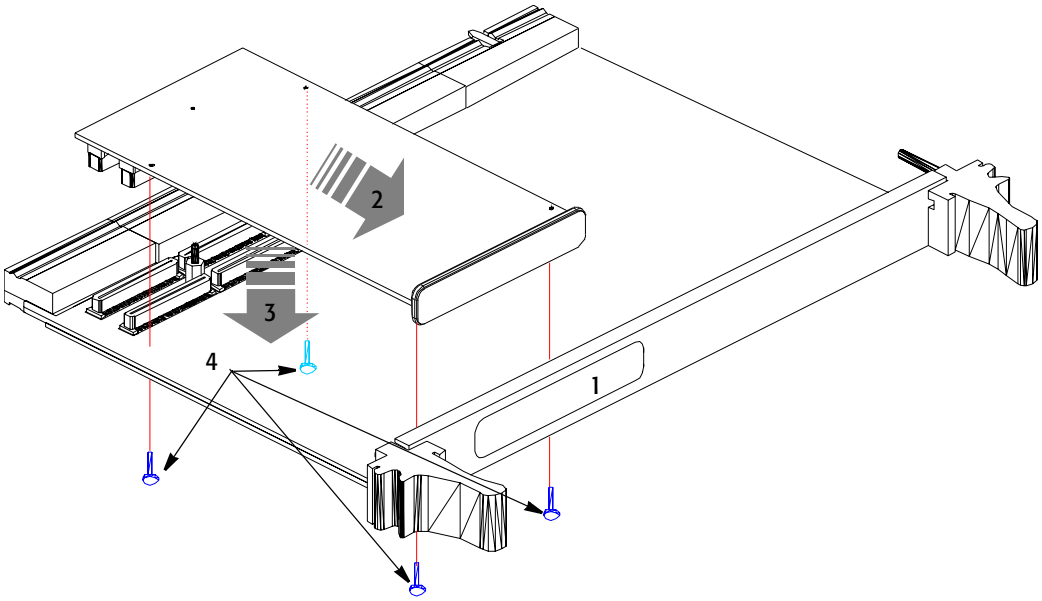
Before you Begin

The EPC-6320/21 requires a PMC carrier.

Installing the EPC-6320/21 PMC on the Carrier Card

You install the EPC-6320/21 PMC on the carrier card as shown in the next figure.

Figure 2-1. Installing a PMC Module



To install a PMC module:

1. Remove and save any blank faceplate from the PMC slot in the carrier card faceplate.
2. Position the PMC bezel through the PMC slot on the front panel.
3. Push the rear connectors into the carrier card.
4. Insert and tighten the screws on the back of the carrier card.

Using the 3-Pin Connector

The EPC-6320/21 includes a 3-pin connector that you can use to access some COM1 signals.

Before you begin, ensure that you have a null-modem cable that connects the 3-pin connector to your terminal.

Note

You must construct this cable; RadiSys does not supply a cable for the 3-pin connector. For pinout information, see *3-Pin COM Connector* on page 63.

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To use the 3-pin connector:

1. Attach the cable to the 3-pin connector and your terminal.
2. Start a terminal emulation program, such as Hyperterm or Telix, using these settings:

Baud rate:	115200
Parity:	None
Data bits:	8
Stop bits:	1
Flow control:	None

You can now access the BIOS setup program using the methods described in *Chapter 4, BIOS Configuration*.

Booting the EPC-6320/21 via MBA (Managed PC Boot Agent)

1. Set the BIOS to use MBA as the first boot device:
   A. Boot the board.
   B. Press F2 to enter the BIOS Setup program (see page 27).
   C. Go to the boot options and select MBA as your first boot choice.
   D. Save your changes
   E. Reboot the system.
2. Set network parameters:
   A. Press F1 to enter the MBA configuration when prompted to do so. The configuration menu displays.
   B. Select TCP/IP as the boot method.
   C. Select DHCP as the protocol.
   D. Press 9 to save and reboot.

The board then obtains an IP address via DHCP and boots your image via TFTP with a root filesystem via your NFS server.

Maintaining and Upgrading the EPC-6320/21

Occasionally you will want to perform maintenance or upgrades on the EPC-6320/21. When this occurs, you must remove the board from the carrier card, repair or install the

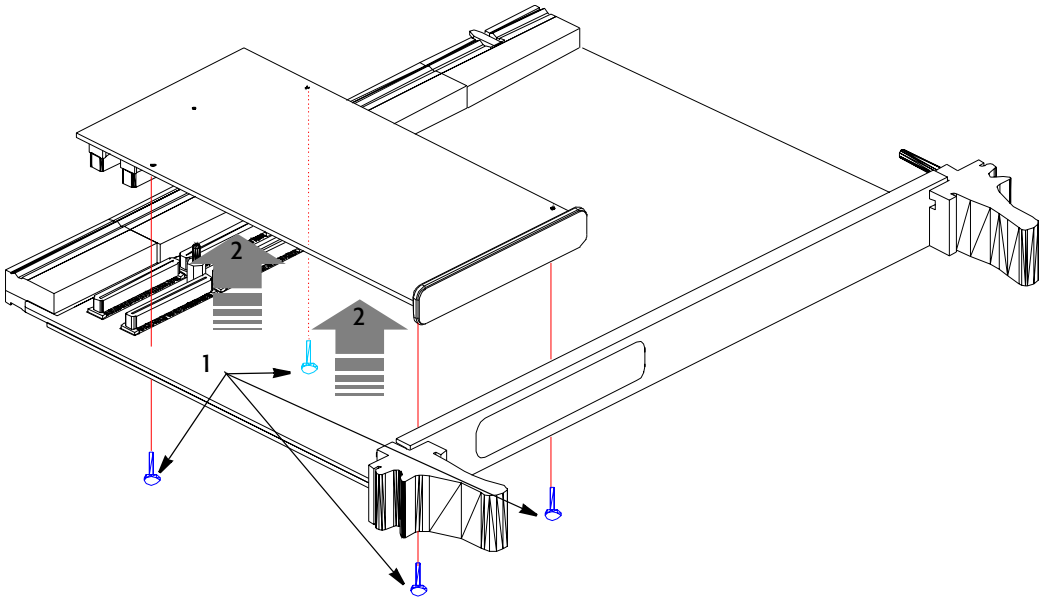
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desired option, then re-install the board on the carrier card. The following sections describes how.

Disconnecting the EPC-6320/21 PMC from the Carrier Card

To separate the EPC-6320/21 from the carrier card:

Figure 2-2. Separating a PMC Module from the Carrier Card



1. Remove the screws on the back of the carrier card.
2. Pull the boards apart while keeping them parallel. Continue applying force until the connectors completely disengage.

After performing maintenance and/or upgrades, replace the EPC-6320/21 as described in *Installing the EPC-6320/21 PMC on the Carrier Card* on page 11.

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This chapter explains how to install Linux and VxWorks operating systems on the EPC-6320/21.

Note

- For MV Linux LSPs, contact MontaVista at this URL:
  http://www.mvista.com
- For VxWorks BSPs, contact RadiSys or WindRiver
  http://www.windriver.com
  http://www.radisys.com

Installing Red Hat Linux

You can install Red Hat using either of these methods:

- Install Red Hat on a separate computer.
- Install Red Hat over the serial port.

The following sections describe how.

Installing Red Hat on a Separate Computer

To install Red Hat, you use a separate computer with a VGA card and prepare a hard drive for transfer to the EPC-6320/21:

1. Install a hard drive and CDROM drive in a PC with a VGA card. Ensure that the hard drive is the master on the primary cable.
2. Power on the system, insert the Red Hat bootable CD, and install Linux with the configuration you desire.
3. Reboot the system and log in at the Linux command prompt as “root”.

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4. Configure Linux for serial redirection. Using any editor, change these files:

File	Instructions
`/etc/inittab`	1. Change the first TTY configuration line to read: `1: 2345:respawn:/sbin/mingetty ttyS0 115200 vt100` 2. Comment out the remaining TTY configuration lines. 3. Save your changes.
`/etc/securetty`	1. Add this line at the bottom of the file: `ttyS0` This file lists TTYs that allow logins. Adding the above line allows you to log in as root over the serial port. 2. Save your changes.

`/etc/lilo.conf`	1. In your kernel entry, add a kernel "append" parameter similar to this example:
	`image="/boot/vmlinuz-2.4.7-10"`
	`label="linux"`
	`read-only`
	`root="/dev/hda1"`
	`append = "console=ttyS0,115200n8"`
	Adding this parameter to the kernel instructs it to redirect kernel messages to the serial port.
	2. Save your changes.

5. Write changes to the master boot record by entering this command at the command prompt:

   ```
   lilo
   ```

6. Shut down the system.
7. Transfer the hard drive to the EPC-6320/21.
8. Boot the EPC-6320/21.

You can now log in over the serial port as root.

Installing Red Hat 7.3 or Later over the Serial Port

Red Hat 7.3 already contains the correct TTY settings. This allows you to install Linux on the EPC-6320/21 without transferring the hard drive from another system. To install Red Hat 7.3 over the serial port:

1. Attach a hard drive and CD on an IDE cable, setting the hard drive to master and the CDROM to slave.
2. Power on the EPC-6320/21 system and immediately insert the Red Hat bootable CD-ROM.
3. Modify the BIOS settings to boot the EPC-6320/21 from the CD-ROM:
   A. Press F2 to enter the BIOS Setup program (see page 27).
   B. Make the CD-ROM the first device the EPC-6320/21 tries to boot from by moving the CD-ROM to the top of the list in the Boot Menu (see page 42).

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C. Change the console and terminal baud rates to 9600.

D. Save your changes and reboot.

The system boots over the serial port at 9600 bps, then displays the boot: prompt.

4. Enter this command:

```
linux console=ttyS0,9600n8
```

The serial port displays kernel messages.

5. Follow the instructions, configuring Linux to your liking. When prompted for kernel parameters, enter:

```
console=ttyS0,9600n8
```

Finish the installation and reboot the system. The serial port displays a login prompt at 9600 bps.

6. Log in as root.

7. To change the console baud rate to 115200, edit these files:

File	Instructions
`/etc/inittab`	1. Change the first TTY configuration line to read: `1: 2345:respawn:/sbin/mingetty ttyS0 115200 vt100` 2. Comment out the remaining TTY configuration lines. 3. Save your changes.

`/etc/lilo.conf`	1. In your kernel entry, add a kernel "append" parameter similar to this example:
	`image="/boot/vmlinuz-2.4.7-10"`
	`label="linux"`
	`read-only`
	`root="/dev/hda1"`
	`append = "console=ttyS0,115200n8"`
	2. Save your changes.

8. Write the changes to the master boot record by entering this command at the command prompt:

```
lilo
```

9. Reboot the system.

10. Change the baud rate:

A. During reboot, press F2 to enter the BIOS Setup program (see page 27).

B. Change the console and terminal baud rates to 115200 bps.

C. Exit and save changes.

The system boots over the serial port at 115200 bps, then displays the Linux login prompt.

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Installing MontaVista Linux

This section explains how to network boot MontaVista Linux from the RadiSys-supplied LSP.

Configure the Host to Boot EPC-6320/21 over the Network

The following sections provide instructions on how to configure the different components of the host system. These instructions are for only Linux hosts running Red Hat 7.3 or later.

Extract the Kernel Source and Filesystem

1. Obtain the MontaVista Linux host tools from MontaVista (http://www.mvista.com).
2. Install the tools according to the host tools instructions. When the installation prompts you to install an LSP, choose any LSP based on an Intel Pentium III processor.
3. Extract kernel source files from the RadiSys-supplied LSP archive to a work area.

Configure DHCP

⚠ CAUTION
Ensure that the DHCP server is configured correctly. An incorrect configuration may cause problems for other machines on your network.

For information about installing and configuring the DHCP server on your machine, see your system administrator.

To configure DHCP as root:

1. Make sure a DHCP server is installed and that the following file exists:

Version	Filename
Red Hat 7.x	`/var/lib/dhcp/dhcpd.leases`

If the file does not exist, create an empty one using the Unix `touch` command:

Operating system	Command
Red Hat 7.x	`touch /var/lib/dhcp/dhcpd.leases`

2. Edit the DHCP daemon configuration file:

Note
For an example of code you can use, see *Sample Code* on page 24.

A. Add the following configuration into your /etc/dhcpd.conf file:

```
allow bootp;
allow booting;
subnet SubAddress netmask NetAddress {
```


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```
default-lease-time 1209600; # two weeks
max-lease-time 31557600; # one year
group {
    next-server TFTPAddress;
    option routers Gateway;
    host Target {
        hardware ethernet MACAddress;
        fixed-address IPAddress;
        option root-path "/target";
        filename "bzImage";
        }
    }
}
```

B. Change the value of these parameters:

SubAddress The subnet address, consisting of four numbers from 0–255 separated by dots (periods).

NetAddress The netmask address, consisting of four numbers from 0–255 separated by dots (periods).

TFTPAddress The TFTP server address, consisting of four numbers from 0–255 separated by dots (periods).

Gateway The router or gateway address, consisting of four numbers from 0–255 separated by dots (periods).

Target The target name, consisting of three sections separated by dots (periods). For example:

```
test1.mvista.com
```

This name must be consistent with the host name used for DNS or host file look-up.

Note

For a Red Hat install without MontaVista tools, you must set up a "target" root filesystem.

MACAddress The target MAC (Ethernet) address, consisting of six 2-digit numbers separated by colons.

```
xx:xx:xx:xx:xx:xx
```

Note

The MAC address typically looks like this:

```
00:00:50:xx:xx:xx
```

IPAddress The target's IP address, consisting of four numbers from 0–255 separated by dots (periods).

3. Restart dhcpd by entering this command:

```
/etc/rc.d/init.d/dhcpd restart
```


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The DHCP daemon is required to service BOOTP requests when booting the target. To run the DHCP daemon (on the host) on every boot, enter this command:

```
/sbin/chkconfig dhcpd on
```

⚠ CAUTION

Use caution when running this command on a corporate network. Your DHCP server may interfere with the corporate DHCP server.

DHCP is now configured.

Configure TFTP

To configure TFTP, follow the instructions for the host you are using. The following instructions use the version of TFTP distributed with CGE.

Note

Some host distributions do not have the most recent version of TFTP and some versions of TFTP do not work correctly with CGE. For that reason, MontaVista Software distributes a version of TFTP with CGE, installed by default at /opt/mvlcge/host/bin.

Red Hat 7.x

To configure TFTP on a Red Hat 7.3 host as root:

1. Create (or edit) the file /etc/xinetd.d/tftp. Use the following format:

```
#/etc/xinetd.d/tftp
service tftp
{
   socket_type = dgram
   wait = yes
   user = root
   log_on_success += USERID
   log_on_failure += USERID
   server = /usr/sbin/in.tftpd
   server_args = -r blksize -s -v /tftpboot
   disable = no
   protocol = udp
}
```

2. Ensure that the /tftpboot directory exists. To create the directory, enter this command:

```
mkdir /tftpboot
```

3. Have xinetd re-read its configuration file by entering this command:

```
/etc/rc.d/init.d/xinetd restart
```

4. Stop any any TFTP daemons that have not timed out by entering this command:

```
killall in.tftpd
```


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Configure NFS

To configure NFS as root:

1. Add this line in /etc/exports:

```
/target *(rw, sync, no_root_squash)
```

2. Stop, then start, the NFS daemon by entering these commands:

```
/etc/rc.d/init.d/nfs stop
/etc/rc.d/init.d/nfs start
```

3. Set the NFS daemon to run during every boot by entering this command:

```
/sbin/chkconfig nfs on
```

4. Synchronize the NFS daemon by entering this command:

```
/usr/sbin/exportfs -ra
```

NFS is now set up.

Network Boot the Kernel

To network boot a kernel on the EPC-6320/21:

1. Change to the working folder (directory) where you placed the kernel sources.
2. Build the kernel by entering these commands:

```
cd /usr/src/linux-2.4
```

Note

Before running the `make dep` command:

- Ensure that you have the correct build options.
- Include support for NFS, TFTP, DHCP, and INTEL gigabit Ethernet; do not add them as modules.

You can verify your build options using one of these methods:

- In graphic mode, enter `make xconfig`.
- In text mode, enter `make config`.

```
make clean; make dep; make bzImage
```

bzImage is placed in this directory:

```
/usr/src/linux_2.4.20-8/arch/i386/boot/
```

3. Copy bzImage to /tftpboot.
4. Change the boot device:
   A. Attach:
      - An Ethernet cable to the EPC-6320/21 that allows access to your DHCP server.
      - A null modem cable from the EPC-6320/21 to a PC serial port.

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B. Open a terminal, such as minicom, and set the communications parameters to:

Baud rate:	115200
Parity:	None
Data bits:	8
Stop bits:	1
Flow control:	None

C. Power-on the EPC-6320/21.

D. Enter the BIOS Setup program (see page 27) and set the first boot device as UNDI (on-board Ethernet). Save your changes and reboot. The kernel boots over the network and displays on the serial port.

5. Log in as root.

Install MontaVista Linux to a Hard Drive

Creating a bootable hard drive requires that you network boot a kernel and NFS a filesystem, as described in the previous section. You then attach a bootable media device, prepare a filesystem on it, and copy the filesystem over NFS.

1. Prepare the bootable media:

   A. Attach an IDE hard drive to the IDE connector on your baseboard. Be sure that the hard drive is set up as the master.

   B. Network boot the system over the serial port at 115200 bps.

   C. Run fdisk:

      i. Create partitions on the drive by entering this command:

      ```
      fdisk /dev/hda
      ```

      ii. Create at least one partition to use as /root.

      iii. Tag the partition with ID 83, using the `t` command.

      iv. Mark it bootable by using the `a` command.

      v. Save your changes by entering `w`.

   For more information about fdisk, see the HOWTOs on using fdisk, available on the web.

URL
You can find out more about fdisk at this URL: www.redhat..com To locate the utility, search for fdisk on the site.

2. Prepare a filesystem:

   A. Create a filesystem by entering this command:

   ```
   mkfs-ext2 /dev/hda1
   ```

   B. Mount the filesystem to /mnt by entering this command:

   ```
   mount /dev/hda1 /mnt
   ```


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C. Copy the filesystem from NFS to the mount point /mnt by entering these commands:

```
cp -aR /bin /mnt
cp -aR /boot /mnt
cp -aR /dev /mnt
cp -aR /etc /mnt
cp -aR /home /mnt
cp -aR /lib /mnt
cp -aR /opt /mnt
cp -aR /root /mnt
cp -aR /sbin /mnt
cp -aR /tmp /mnt
cp -aR /usr /mnt
cp -aR /var /mnt
mkdir /mnt/mnt
mkdir /mnt/proc
```

3. On your host, copy the bzImage kernel you created (in step 2 of *Network Boot the Kernel* on page 20) to /root. On the EPC-6320/21 terminal, copy this image to /mnt/boot.
4. Change the current /root to the mounted drive by entering this command:

   ```
   chroot /mnt
   ```

5. Configure Linux for serial redirection. Using any editor, change this file:

File	Instructions

/etc/lilo.conf	1. Revise the file similar to this example, paying particular attention to the tty settings:
	`timeout="50"`
	`default="MVL CGE 2.1"`
	`boot=/dev/hda`
	`map=/boot/map`
	`install=/boot/boot.b`
	`append="console=ttyS0,115200n8"`
	`lba32`
	`image="/boot/bzImage"`
	`label="MVL CGE 2.1"`
	`read-only`
	`root=/dev/hda1`
	2. Save your changes.

6. Write the changes to the master boot record by entering this command at the command prompt:

   ```
   lilo
   ```

7. Reboot the system.
   A. Press F2 to enter the BIOS Setup program (see page 27).
   B. Change the first boot device to be the bootable drive.
   C. Save your changes and reboot.

You should now boot the IDE hard drive with a serial console.

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Installing VxWorks

This section explains how to install VxWorks on an IDE hard drive.

Requirements

To install a VxWorks BSP on an EPC-6320/21 you will need:

- The EPC-6320/21 VxWorks BSP from RadiSys. You can request it from RadiSys by sending email to support@radisys.com.
- A DOS boot disk with fdisk and format utilities.
- A 10MB or greater IDE hard drive.

Installation

1. Install the BSP by extracting the archive.
2. Build projects:
   A. In the Tornado environment, create a project based on the EPC-6320/21 BSP.
   B. Build bootrom_uncmp and vxWorks.st.

   For more information about creating and building files, see your VxWorks documentation.
3. Create a boot disk with the VxWorks bootloader:
   A. Install two IDE hard drives on the carrier card. Ensure that the slave hard drive has VXSYS.COM, BOOTROM.SYS, and vxWorks.st installed on it.
   B. Power up the EPC-6320/21 and configure the system to boot to the slave hard drive.
   C. Run fdisk on the master hard drive to remove all partitions and create a primary DOS partition.
   D. Reboot the system and activate the partition on the D: drive.
   E. Format and sys D: drive.

   ```
   Format d:
   Sys d:
   ```

   F. Reboot the system and configure the EPC-6320/21 to boot to the master hard drive.
   G. Boot to the master hard drive and change to D: drive. Run VXSYS on the C: drive.

   ```
   Vxsys c:
   ```

   H. Copy BOOTROM.SYS and vxWorks.st to the newly created hard drive.
   I. Reboot the system and enter the BIOS Setup program (see page 27). Configure the system to boot to the master hard drive.

   The system is now configured to boot to VxWorks.

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Table 3-1. VxWorks Command and File Descriptions

Command	Description
`vxsys c:`	Installs the master boot record and initial bootloader
`bootrom.sys`	VxWorks bootloader
`vxWorks.st`	VxWorks standalone image (contains vxWorks image and symbol table)
`Bootrom_uncmp`	VxWorks boot ROM

4. Start VxWorks:
   A. Boot the EPC-6320/21 system.

   Note
   The default is to boot from "ata0", which is the master hard drive.

   When the bootloader runs, a countdown displays.
   B. Press a key to display a prompt, then enter `c` to configure your system. Set IP information to the values you desire.

   To have VxWorks automatically initialize the on-board Ethernet, enter `gei` into the "other" field.

   After you enter the parameters, the configuration is saved automatically to flash.
   C. Boot VxWorks by entering `@`.

Sample Code

DHCP

The following is an example of /etc/dhcpd.conf written for a Red Hat 9.0 install:

Note
In the following example:
- Comment lines represent optional lines.
- Declarations in the host definitions have precedence. If you uncomment lines 15 and 17, host epc6320 has a different root-path and filename for the kernel image than hosts epc6320a,b,c.

```
not authoritative;
allow bootp;
allow booting;
ddns-update-style none;
subnet 10.100.4.0 netmask 255.255.255.0 {
   default-lease-time 1209600; #two weeks
   max-lease-time 31537600; #one year
#  option routers 10.100.4.58;
   next-server 10.100.4.58;
   option root-path "/target";
   filename "bzImage";
```


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```
host epc6320{
   hardware ethernet 00:00:50:0D:60:B4;
   fixed-address 10.100.4.59;
#     option root-path "/tftpboot";
#     option root-path "/target";
#     filename "pxelinux.0";

   }
host epc6320a{
   hardware ethernet 00:00:50:14:08:D8;
   fixed-address 10.100.4.59;
   }
host epc6320b{
   hardware ethernet 00:00:50:14:08:D9;
   fixed-address 10.100.4.59;
   }
host dc1hwlab{
   hardware ethernet 00:00:50:0D:61:24;
   fixed-address 10.100.4.61;
   }
}
```

TFTP

The following is an example of /etc/xinetd.d/tftp written for a Red Hat 9.0 install:

```
# default: off
# description: The tftp server serves files using the trivial file transfer
#  protocol.  The tftp protocol is often used to boot diskless
#  workstations, download configuration files to network-aware printers,
#  and to start the installation process for some operating systems.
service tftp
{
   socket_type= dgram
   protocol  = udp
   wait      = yes
   user      = root
   server    = /usr/sbin/in.tftpd
   server_args= -r blksize -s -v /tftpboot
   disable   = no
   log_on_success+=USERID
   log_on_failure+=USERID
}
```

Exports

The following is an example of a line added to /etc/exports written for a Red Hat 9.0 install:

```
/target *(rw, sync, no_root_squash)
```


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4 BIOS Configuration

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I/O Device Configuration Sub-Menu 41
Boot Menu 42
Exit Menu 44
CMOS Save & Restore Sub-Menu 45

The EPC-6320/21 uses the Phoenix NuBIOS to configure and select various system options. This chapter details the various menus and sub-menus used to configure the system. This chapter is written as though you are setting up each field in sequence and for the first time. Your system may be correctly pre-configured and require very little setup.

Note

To revert to the original BIOS settings, select Load Setup Defaults from the *Exit Menu* on page 44. This restores the original BIOS settings.

You may see some error messages during the execution of the BIOS initialization sequence. If errors occur during the POST (Power-On Self-Test), the BIOS displays the error on the appropriate line of the screen display and, depending on how your system is configured, either pauses or tries to continue. For information about error messages, see *Appendix D, Error Messages*.

Pressing the Escape key during POST displays the Boot-First pop-up menu after POST completes. You can use this menu to override, for only this boot, the boot options. This menu includes the same options as the Boot Menu's top level. For information about the options, see *Boot Menu* on page 42.

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BIOS Setup Screens

The EPC-6320/21's BIOS includes a setup program that displays and modifies the system configuration. The EPC-6320/21's nonvolatile CMOS RAM stores configuration information, and the BIOS uses it to initialize the EPC-6320/21 hardware.

You can enter the BIOS Setup only during the system reset process, following a power-up, front panel reset, or equivalent. To enter Setup, press the F2 key when prompted.

Note
To view BIOS setup screens, the EPC-6320/21 must be attached to a terminal.

Menu Map

You set up the BIOS by making selections from the menus shown in the next table.

When reading this file online, you can immediately view information about any menu by placing the mouse cursor over menu name and clicking:

Menu	Sub-menu
Main Setup Menu	Primary Master/Slave Sub-Menus
Advanced Menu	PCI Configuration Sub-Menu PrPMC Customizations Sub-Menu PCI/PNP ISA UMB Region Exclusion Sub-Menu PCI/PNP ISA IRQ Resource Exclusion Sub-Menu Console Redirection Sub-Menu I/O Device Configuration Sub-Menu
Boot Menu	None
Exit Menu	CMOS Save & Restore Sub-Menu

Navigation

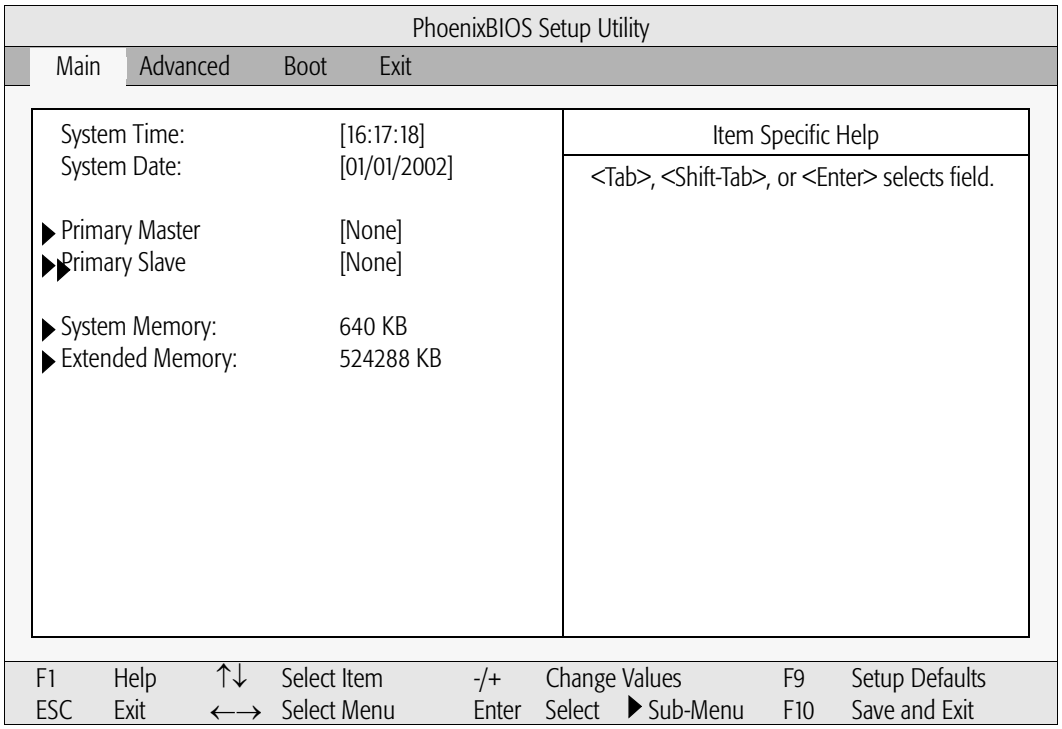
To...	Do...
Display a menu	Press the left or right cursor (arrow) keys and press the Enter key. If you use the arrow keys to leave a menu and then return, your active field is always at the beginning of the menu.
Display a submenu (fields with a triangle at left)	Move the cursor to a field with a triangle and press the Enter key. If you select a sub-menu and then return to the main menu, the active field is that sub-menu heading.
Select a field	Press the up or down cursor (arrow) keys
Select an option	Do one of these: • Press the + and – keys to rotate through available options. • In certain numeric fields, simply enter the desired number.

The remainder of this chapter describes the fields in each menu and sub-menu. Additional help information is available in the help area on the Setup screen.

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Main Setup Menu

Figure 4-1. BIOS Main Setup Menu



The far right menu in the menu bar is the Exit Menu. Use the options in the Exit menu to save your changes, re-load default BIOS settings, and so on. Press the ESC key to go immediately to the Exit Menu.

The fields in each menu and sub-menu are explained below. Additional help information is available in the help area on the BIOS setup screen.

Field	Description
System Time/System Date	Sets the system time and date. To change these values, go to each field and enter the desired value. Press the tab key to move from hour to minute to second, or from month to day to year. The default system time is 00:00; the default date is 01/01/1998.
Primary Master sub-menu	Displays a menu that you use to enter information for the master IDE drive connected to the primary IDE controller. For more information, see *Primary Master/Slave Sub-Menus* on page 29.
Primary Slave sub-menu	Displays a menu that you use to enter information for the slave IDE drive connected to the primary IDE controller.For more information, see *Primary Master/Slave Sub-Menus* on page 29.
Boot Options sub-menu	Displays a menu that you use to specify the PC's behavior during the boot process. For more information, see *Boot Menu* on page 42.
System memory	Displays the amount of conventional memory (below 1MB). This field is not editable; no user interaction is required.
Extended memory	Displays the amount of extended memory (above 1MB). This field is not editable; no user interaction is required.

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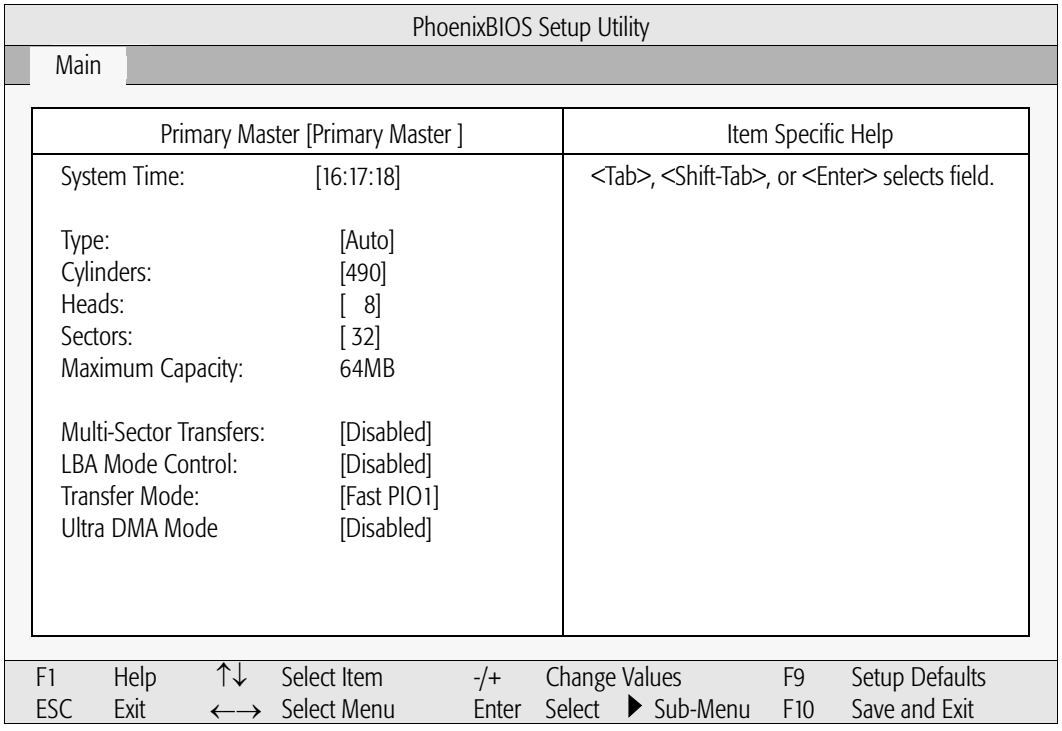
Primary Master/Slave Sub-Menus

There are two IDE adapter sub-menus for the primary hard disk controllers: a master and slave drive menu.

Access this screen to:

- See or reconfigure the detailed characteristics of the primary hard disk (select the IDE Adapter 0 Master item from the Main BIOS Setup).
- Set up new disks and allow the Setup program to determine the proper settings based on information on the disk. Note that the Setup program can detect these settings only on drives that comply with ANSI specifications.
- Set up existing (formatted) disks. Note that you must use the same parameters used when the disk originally was formatted. You must select an option for the Type field, then enter the specific cylinder, head, and sector information listed on the label attached to the drive at the factory.

Figure 4-1. Primary Master/Slave Sub-Menus



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Field	Description
Type	Identifies the disk type. You can select one of these: • **Auto (default)**: Select this option when you want the POST to query the hard disk for its parameters whenever the POST runs. RadiSys recommends this option. **Note**: If you set a hard disk to "Auto", but no hard disk is actually present, the BIOS queries the (non-existent) hard disk until it times out, slightly increasing the duration of the POST. • **None**: Select this option if yours is not an IDE hard disk drive. • **User**: Select this option if you have an IDE disk but cannot employ the "Autotype" feature. Then enter the correct drive values for cylinders, heads, sectors/track, and write precompensation. • **ATAPI Removable**: Select this option if you have a removable disk drive. • **IDE Removable**: Provides support for high-capacity disks that can be formatted as floppy or hard disks. This option may be used for compact flash cards. • **CD-ROM**: Select this option if you have a CD-ROM drive. • **1–39**: Select this option to specify a pre-determined hard-disk drive type. These drive types, found in the FDPT (Fixed Disk Parameter Table), are seldom used. RadiSys recommends that you avoid using this option. **Note**: For disks not supplied, consult the product documentation. When finished, press the ESC key to return to the *Main Setup Menu*.
Cylinders	Specifies the number of cylinders on this system. You can specify a number from 1 to 16. **Note**: This field displays only when the Type field contains a value of [User] or [1–39]. You can edit this field only when the Type field contains a value of [User].
Heads	Specifies the number of heads on this system. **Note**: This field displays only when the Type field contains a value of [User] or [1–39]. You can edit this field only when the Type field contains a value of [User].
Sectors	Specifies the number of sectors in each track on this system. **Note**: This field displays only when the Type field contains a value of [User] or [1–39]. You can edit this field only when the Type field contains a value of [User].

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Field	Description
Multi-Sector Transfers	Allows the System BIOS to read ahead by the specified number of sectors during disk access. This has the effect of reading more data at once to reduce the absolute number of discrete disk reads performed by the operating system, which may increase system performance. You can select one of these: • Disabled (default if no drive is installed) • 2 Sectors • 4 Sectors • 8 Sectors • 16 Sectors (default if a drive is installed) **Note**: This field displays only when the Type field contains a value of [User] or [1–39]. Autotyping may change this value if the hard disk reports that it supports block accesses.
LBA Mode Control	Determines how the System BIOS references hard disk data. You can use this option only if both the hard disk being configured and the operating system support LBA (Logical Block Addressing). Autotyping may change this value if the hard disk reports that it supports LBA. You can select one of these: • **Disabled (default if no drive is installed)**: Reference hard disk data using the CHS (Cylinders/Heads/Sectors) method. • **Enabled (default if a drive is installed)**: Reference hard disk data as logical blocks. **Note**: This field displays only when the Type field contains a value of [None].
Transfer Mode	Selects the mode that the System BIOS uses to access the hard disk. You can select one of these: • Standard • Fast PIO 1 • Fast PIO 2 • Fast PIO 3 • Fast PIO 4 (default) • FPIO 3 / DMA 1 • FPIO 4 / DMA 2 Older hard disks only support “Standard”. Newer hard disks adhering to “Fast ATA” or “Enhanced IDE” specifications may support the fast programmed I/O or DMA modes. Note that autotyping may change this value depending on the transfer modes that the hard disk reports it supports. The fast DMA modes take full advantage of the onboard bus mastering hard disk controller and should yield the highest performance when used in conjunction with multitasking operating systems that support it. **Note**: This field displays only when the Type field contains a value of [None].

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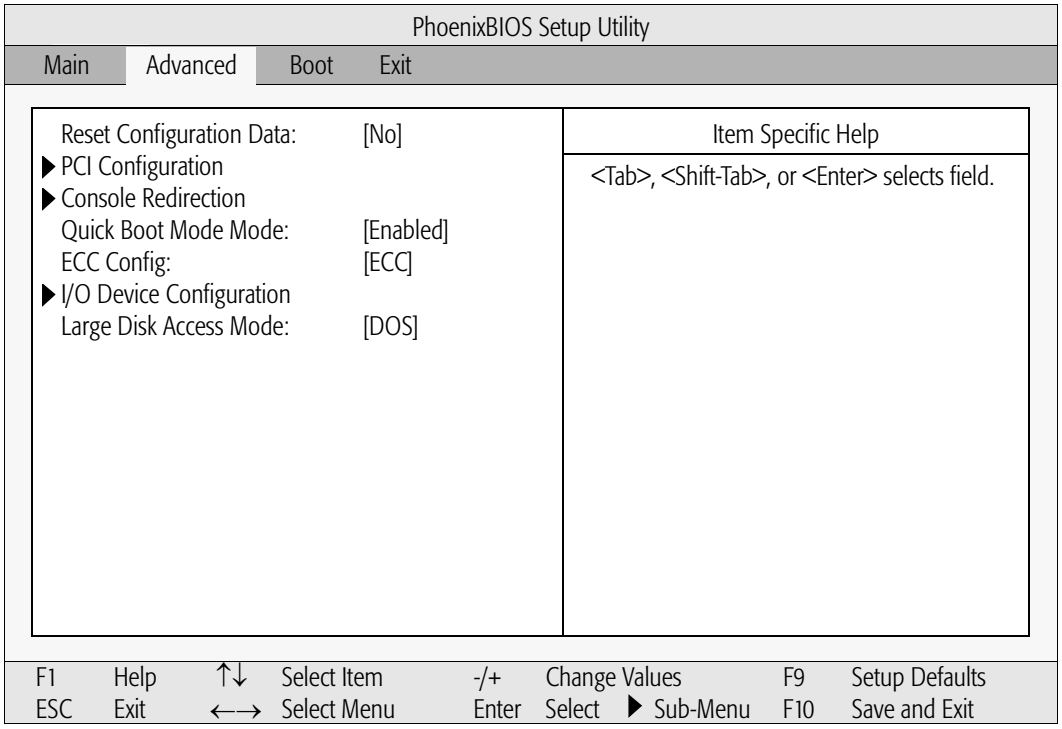
Field	Description
Ultra DMA Mode	Selects the Ultra DMA Mode that the System BIOS uses to access the hard disk. You can select one of these: • Mode 2 (default) • Mode 1 • Mode 0 • Disabled **Note**: This field displays only when the Type field contains a value of [None]. Autotyping derives this value from information reported by the drive.

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Advanced Menu

This menu contains settings for integrated peripherals, memory shadow, cache, and large disk access mode. You access this menu by selecting Advanced from the Main BIOS Setup menu.

Figure 4-2. Advanced Menu



Field	Description
Reset Configuration Data	Determines whether to clear the Extended System Configuration Data (ESCD) block that resides in the Flash Boot Device (FBD). You can select one of these: • **No (default)**: Does not clear the ESCD block. • **Yes**: Clears the ESCD block. You must clear the block the first time a system is turned on or if the ESCD becomes corrupted. This option automatically resets to "No" after the block is cleared.
PCI Configuration Sub-Menu	Displays a menu that you use to configure PCI devices. For more information, see *PCI Configuration Sub-Menu* on page 35.
Quick Boot Mode	• **Enabled**: • **Disabled**:
ECC Config	ECC

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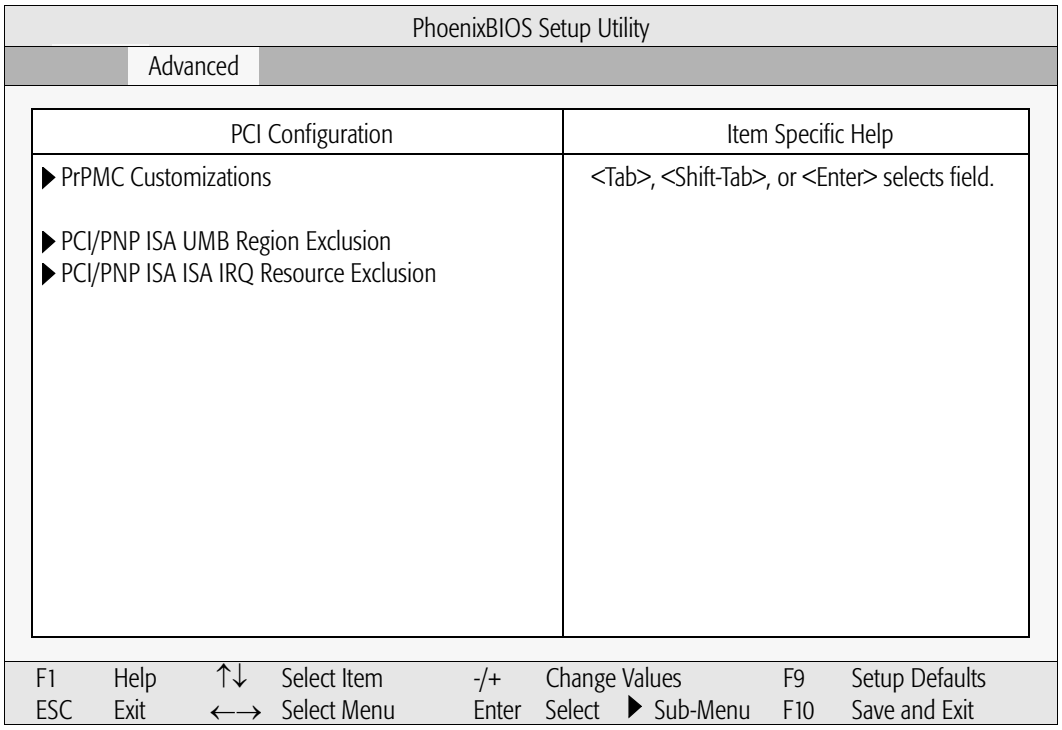
Field	Description
I/O Device Configuration Sub-Menu	Displays a menu that you use to configure peripheral devices. For more information, see *I/O Device Configuration Sub-Menu* on page 41.
Large Disk Access Mode	Specifies whether MS-DOS systems can use hard disks up to 8GB (1024C x 255H x 63S) without special drivers or LBA. If the drive fails while installing new software, change this setting and try again. You can select one of these: • **DOS (default)**: Causes the System BIOS to perform cylinder/head translation if the drive is configured in Setup to have more than 1024 cylinders. Select this option if your system uses a drive larger than 528 MB and runs DOS or MS-DOS†. • **Other**: Select this option if your system uses a drive larger than 528 MB and runs an OS other than DOS.

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PCI Configuration Sub-Menu

Use the options in this sub-menu to control the exclusion of the UMB region for PCI or ISA and the exclusion of the IRQs for PCI or ISA.

Figure 4-3. PCI Configuration Sub-Menu



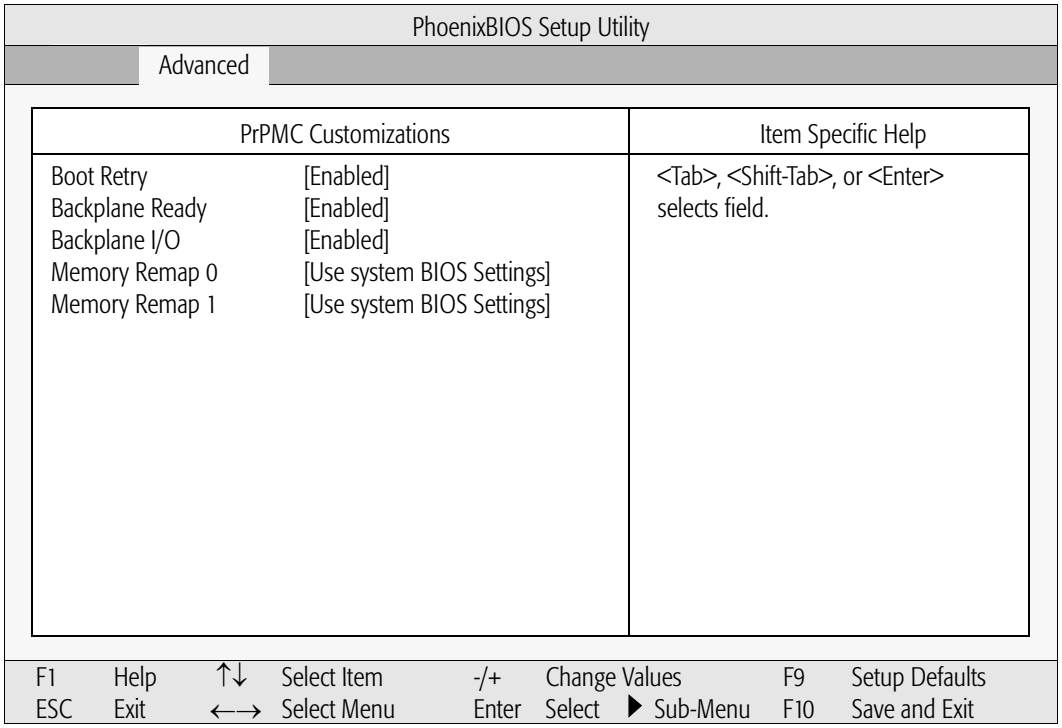
Field	Description
PrPMC Customizations sub-menu	Displays a menu that you use to customize PrPMC options. For more information, see *PrPMC Customizations Sub-Menu* on page 36.
PCI/PNP ISA UMB Region Exclusion	Displays a menu that you use to control the exclusion of PCI and ISA Upper Memory Block (UMB) regions. For more information, see *PCI/PNP ISA UMB Region Exclusion Sub-Menu* on page 37.
PCI/PNP ISA ISA IRQ Resource Exclusion	Displays a menu that you use to control the exclusion of PCI and ISA interrupt resources. For more information, see *PCI/PNP ISA IRQ Resource Exclusion Sub-Menu* on page 38.

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PrPMC Customizations Sub-Menu

Options in this menu customize PrPMC options.

Figure 4-4. PrPMC Customizations Sub-Menu



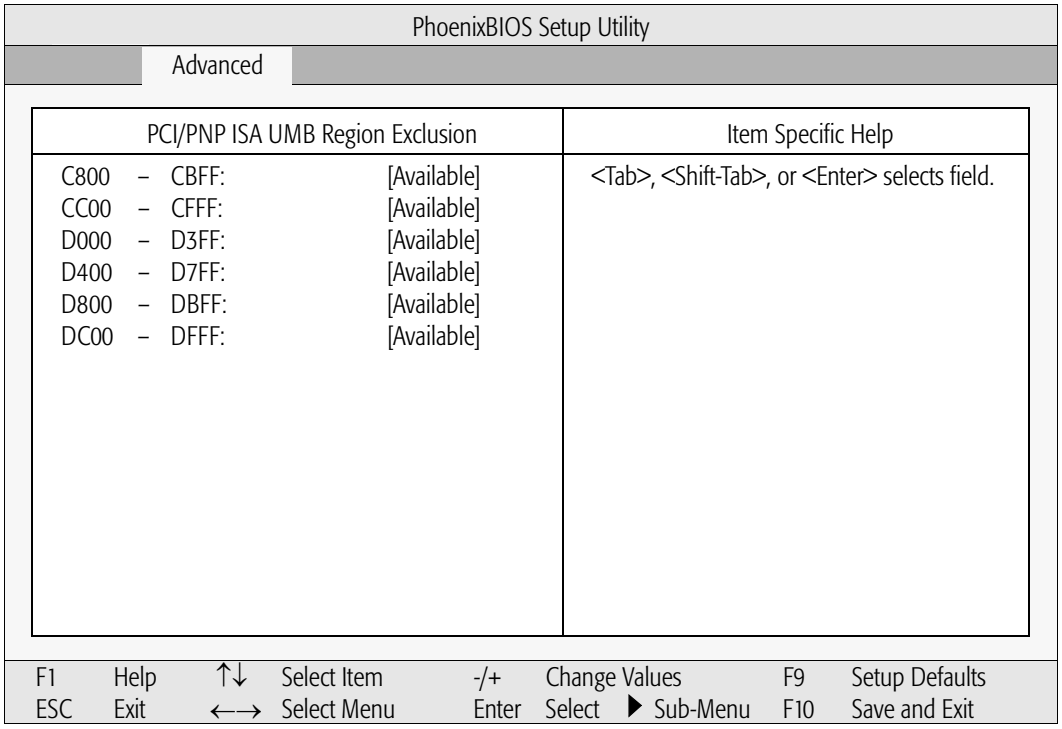
Field	Description
Backplane I/O	Determines how the backplane implements I/O. You can select one of these: • **Disabled (default)**: The local PCI bus services all I/O accesses. • **Enabled**: I/O addresses pass through to the backplane PCI bus.
Backplane Ready	Determines how resources are assigned during boot. You can select one of these: • **Enabled (default)**: Selecting this option sets the Backplane Ready bit after resources are assigned. • **Disabled**: Selecting this option prevents the Backplane Ready bit being set by the System BIOS.
Memory Remap *n*	Maps local DRAM into backplane PCI space. You can select one of these: • Use system BIOS settings • 0 • 1 MB • 16 MB • 256 MB • 512 MB (default) • 1 GB
Boot Retry	Determines what occurs when boot does not succeed. You can select one of these: • **Enabled (default)**: Selecting this option causes boot retry. • **Disabled**: Selecting this option prevents boot retry.

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PCI/PNP ISA UMB Region Exclusion Sub-Menu

The PCI/PNP ISA UMB Region Exclusion Sub-Menu controls the exclusion of PCI and ISA UMB regions.

Figure 4-5. PCI/PNP ISA UMB Region Exclusion Sub-Menu



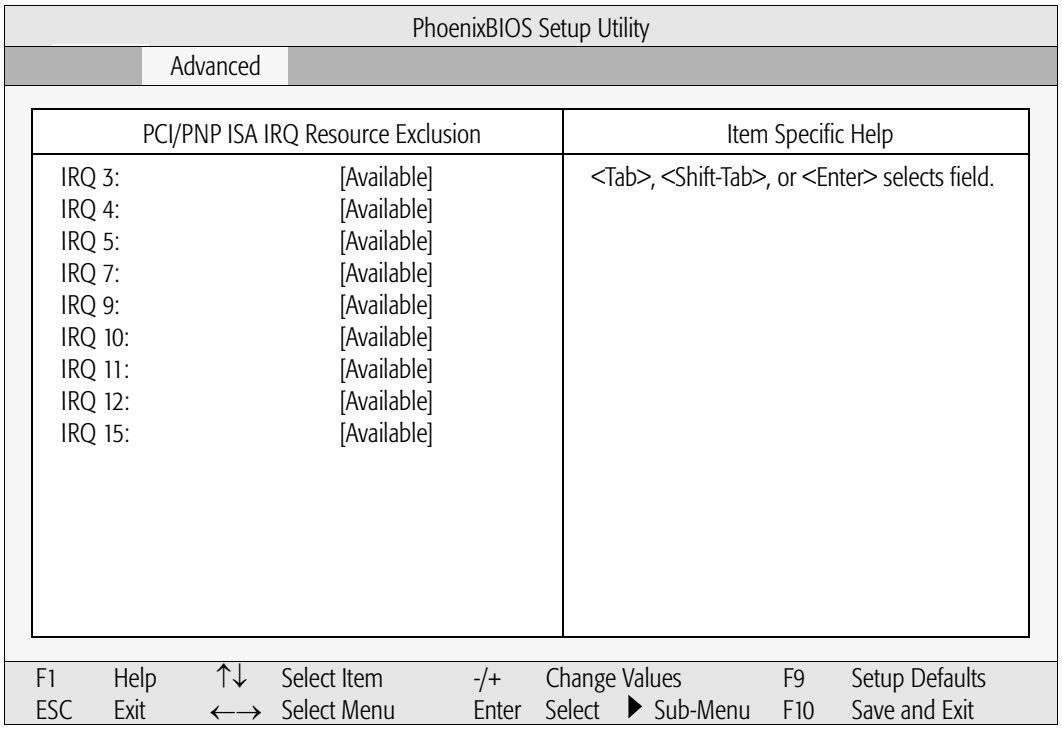
Field	Description
Memory Regions	Determines the use of each UMB region. You can select one of these: • **Available (default)**: Makes the regions available for PCI use. • **Reserved**: Reserves the specified block of upper memory regions for ISA use.

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PCI/PNP ISA IRQ Resource Exclusion Sub-Menu

The PCI/PNP ISA IRQ Resource Exclusion Sub-Menu controls the exclusion of PCI and ISA interrupt regions.

Figure 4-6. PCI/PNP ISA IRQ Resource Exclusion Sub-Menu



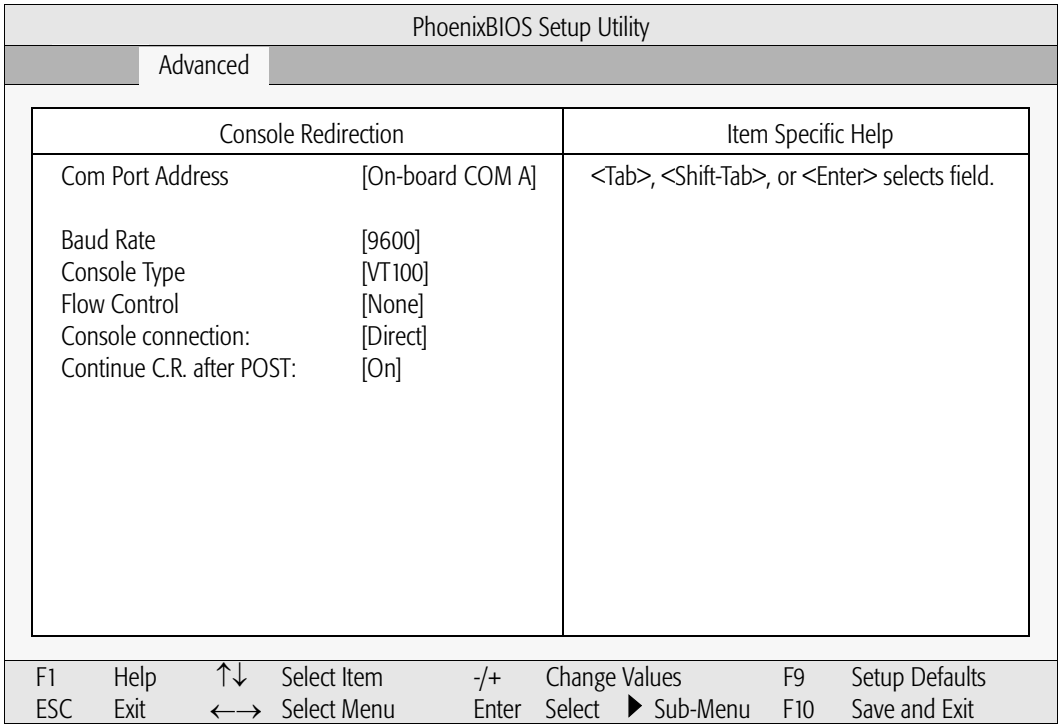
Field	Description
Interrupts	Determines the use of each interrupt. You can select one of these: • **Available (default for IRQs 3, 4, 5, 9, and 12)**: Makes the ISA IRQ available for PCI use. • **Reserved (default for IRQs 7, 10, and 11)**: Reserves the interrupt for ISA use. Select this option if the IRQ is required by an on-board ISA peripheral or an ISA card. **Note**: The IRQ10 interrupt is reserved for soft reset.

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Console Redirection Sub-Menu

Options in this menu configure console redirection.

Figure 4-7. Console Redirection Sub-Menu



Field	Description
Com Port Address	Specifies the serial port to use for console redirection. You can select one of these: • **On-board COM A (default)**: The system uses COM A for rediretion. • **Disabled**: The system does not redirect input.
Baud Rate	Specifies the baud rate at which the COM port operates. You can select one of these: • 600 • 9600 (default) • 1200 • 19.2K • 2400 • 38.4K • 4800 • 115.2K
Console Type	Identifies the console type. You can select one of these: • VT100 (default) • PC ANSI
Flow Control	Specifies flow control. You can select one of these: • None (default) • CTS/RTS • XON/XOFF

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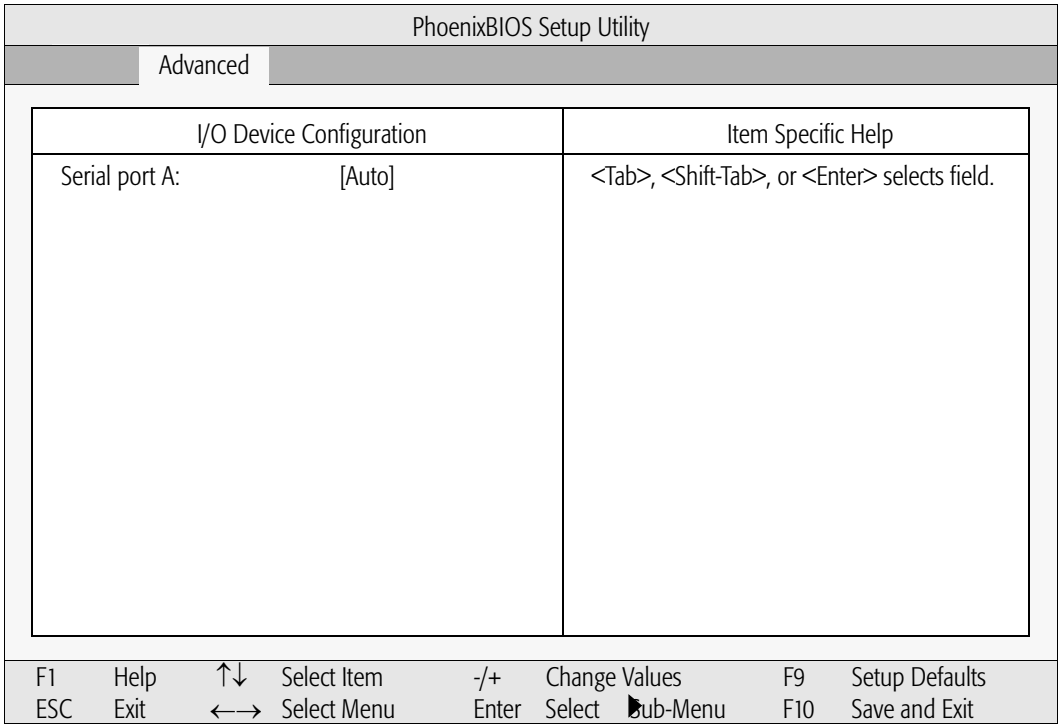
Field	Description
Console connection	Specifies how the console connects to the system. You can select one of these: • **Direct (default)**: Connects the console directly to the system. • **Via modem**: Connects the console to the system via a modem.
Continue C.R. after POST	Determines whether console redirection occurs after BIOS hands off to the OS. You can select one of these: • **On (default)**: Console redirection continues as and after the OS loads. • **Off**: Console redirection stops when the OS starts to load.

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I/O Device Configuration Sub-Menu

Use the options in this sub-menu to configure the onboard serial disk controller.

Figure 4-8. I/O Device Configuration Sub-Menu



Field	Description
Serial Port A	Configures the selected serial port. You can select one of these: • **Auto (default)**: Either the BIOS or OS configures the serial port. • **Disabled**: The serial port (COM A) is not configured. If you select this option, you must also set the Com Port Address option on the Console Redirection Sub-Menu to "On-board COM A". • **Enabled**: The user configures the serial port. If you select this option, you must also set the Com Port Address option on the Console Redirection Sub-Menu to "Disabled".

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Boot Menu

The Boot menu:

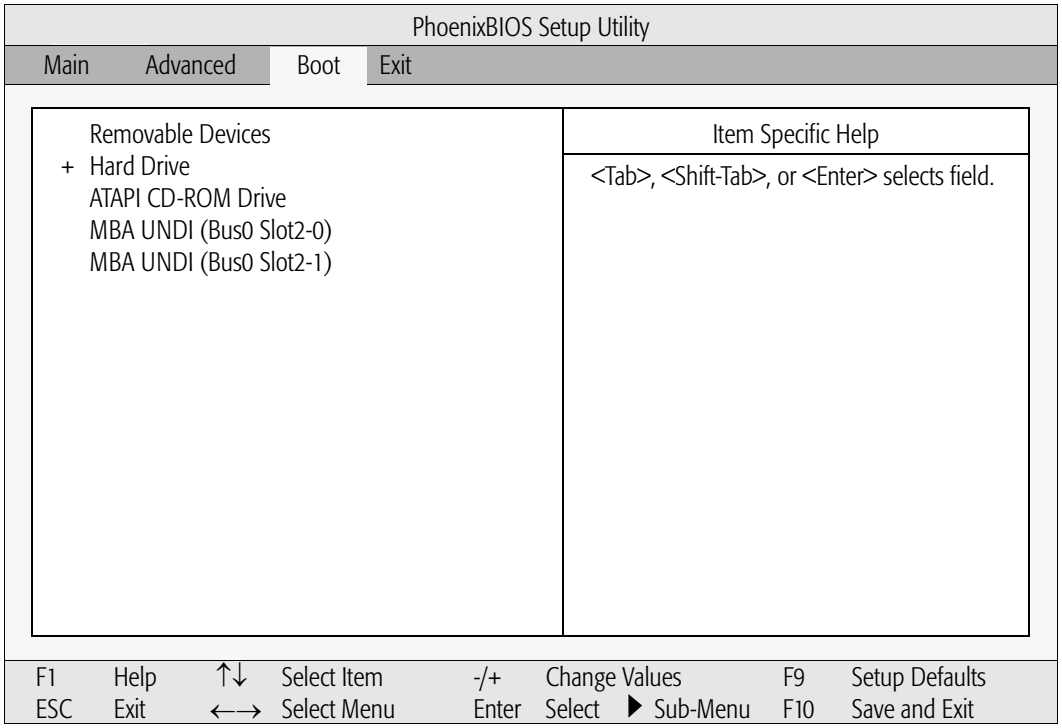
- Specifies the order in which the system tries to boot from devices attached to the system.
- Specifies the boot order of devices in the same class, such as hard drives.

Boot order is assigned from top to bottom, with the uppermost enabled boot device in each class being the boot candidate from that device class.

Note

When two devices appear in a class, only the topmost item is available as a boot device.

Figure 4-9. Boot Menu



To move an item to a higher level in the list, highlight the item and then press the "+" key. To move an item to a lower level in the list, highlight the item and then press the "–" key.

To display all boot device sub-menus under all respective device types, press the Ctrl and Enter keys at the same time.

To display a sub-menu that lists all devices of a specified type available on the system, highlight the device type and press the Enter key. If more than one device of that type exists, use the "+" and "–" keys to change the boot order within the given device type.

To enable a device, highlight the desired device and press the Shift and 1 keys. An exclamation point (!) displays to the left of enabled devices. To disable a device. highlight the device, then press the Shift and 1 keys again.

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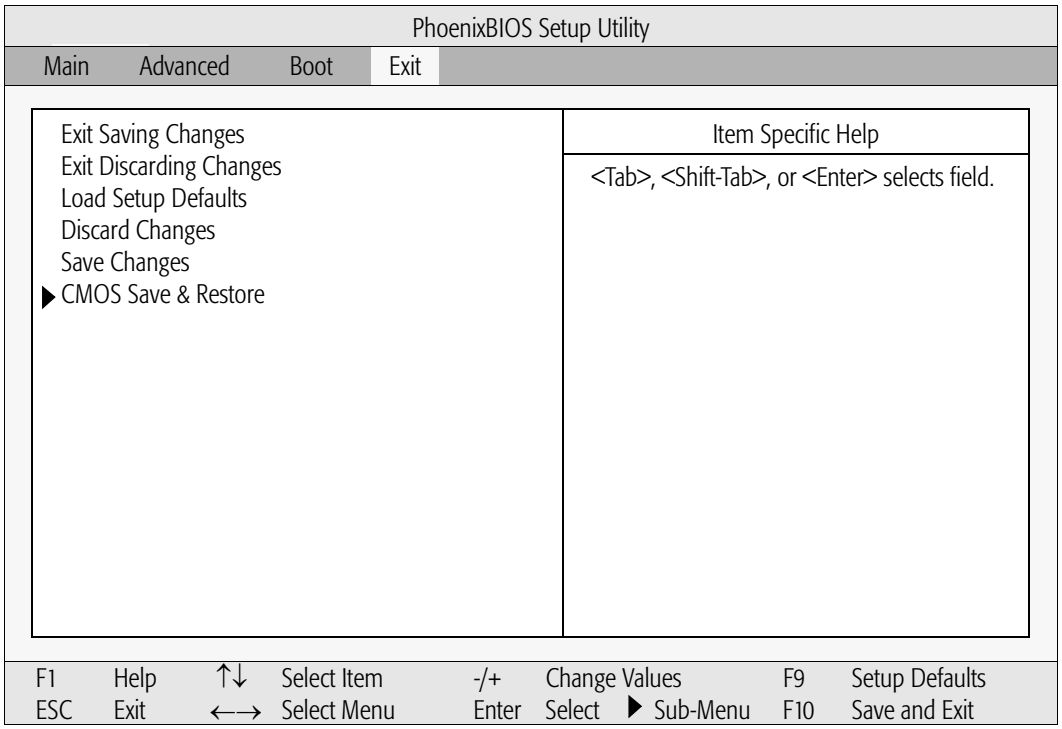
Field	Description
Boot order	Determines the boot order of boot devices. This is the default boot order: 1. Removable Devices 2. Hard Drive 3. ATAPI CD-ROM Drive 4. MBA UNDI (Bus 0 Slot 2-0) 5. MBA UNDI (Bus 0 Slot 2-1)

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Exit Menu

Use the options in this menu to save and exit, or abandon your changes and exit to the system.

Figure 4-10. Exit Menu



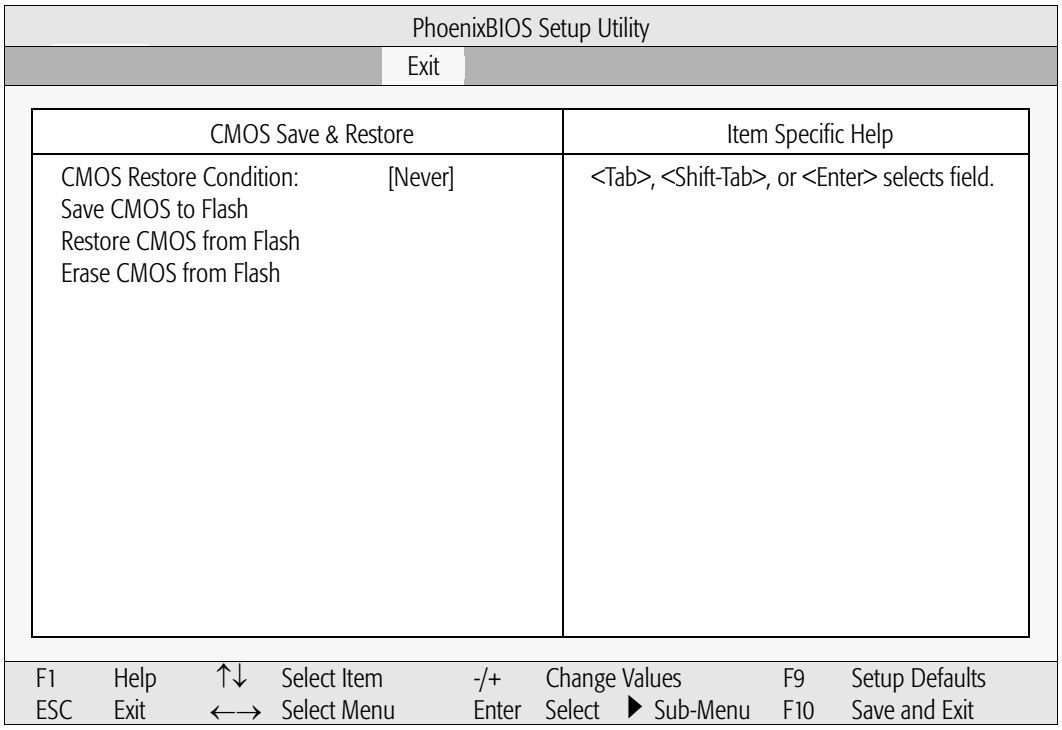
Field	Description
Exit Saving Changes	Saves into CMOS the values you just entered and exits the Setup program. The new values load, and the system reboots.
Exit Discarding Changes	Discards the changes you just made and reverts to the BIOS as it was before you entered the BIOS Setup program. The system boots with the old values.
Load Setup Values	Resets the BIOS values to the original, default values set at the factory, before any suppliers or other end users made changes.
Discard Changes	Loads the system with the values that existed before this editing session started. You do not exit.
Save Changes	Saves to CMOS the edits you made during this session but does not exit the Setup program.
CMOS Save & Restore sub-menu	Displays a menu that controls how the system handles CMOS values. For more information, see *CMOS Save & Restore Sub-Menu* on page 45.

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CMOS Save & Restore Sub-Menu

Use the options in this menu to save, restore, or erase CMOS settings in the FBD (Flash Boot Device).

Figure 4-11. CMOS Save & Restore Sub-Menu



Field	Description
CMOS Restore Condition	Determines the conditions under which the BIOS restores CMOS RAM from the FBD when booting. You can select one of these: • CMOS Corruption • Never (default) • Always. Select this option if your system does not have battery backup.
Save CMOS to Flash	Immediately saves current settings in the Setup program to CMOS RAM and into the FBD. This process may take several seconds to complete. **Note**: Always select this option *before* restoring CMOS from Flash.
Restore CMOS from Flash	Immediately restores CMOS RAM and current settings in the Setup program from the FBD. **Note**: This option is available only if the CMOS was previously saved to the FBD.
Erase CMOS from Flash	Immediately erases the CMOS image stored in the FBD.

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5 Theory of Operation

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Power and Reset 54

The EPC-6320/21 has an Intel Tualatin 512 K LV microprocessor with a maximum 933 MHz core frequency. The RadiSys 82600 chipset provides the memory, LPCI (Local PCI) and BPCI (Backplane PCI), plus IDE, I^2C, and serial port interfaces.

The EPC-6320/21 has on board an Intel 82546GB dual Gb PCI controller with two on-board Ethernet channels.

Ethernet interfaces include:

- **EPC-6320**: Provides two standard IEEE 802.3 Ethernet interfaces to the front panel via RJ-45 connectors for 10/100/1000Base-T applications. The EPC-6320 complies with the *Processor PMC standard, VITA 32-2002, Draft 0.9.*
- **EPC-6321**: Provides two standard IEEE 802.3 Ethernet interfaces to Jn4 PMC connector and complies with the *Processor PMC standard, VITA 32-2002, Draft 0.9.* and *PTMC PICMIG 2.15 Standard.*

The EPC-6320/21 interface through the BPCI bus. Along with any configuration files and other information provided by RadiSys, the CPU boards can run Microsoft† DOS† 6.22 and Monta Vista CG# 3.1 operating systems.

Note

For MV Linux LSPs, contact MontaVista at this URL:

http://www.mvista.com

The backplane PCI bus is compatible with *PCI Specification, Revision 2.2.,* with the exception of PERR.

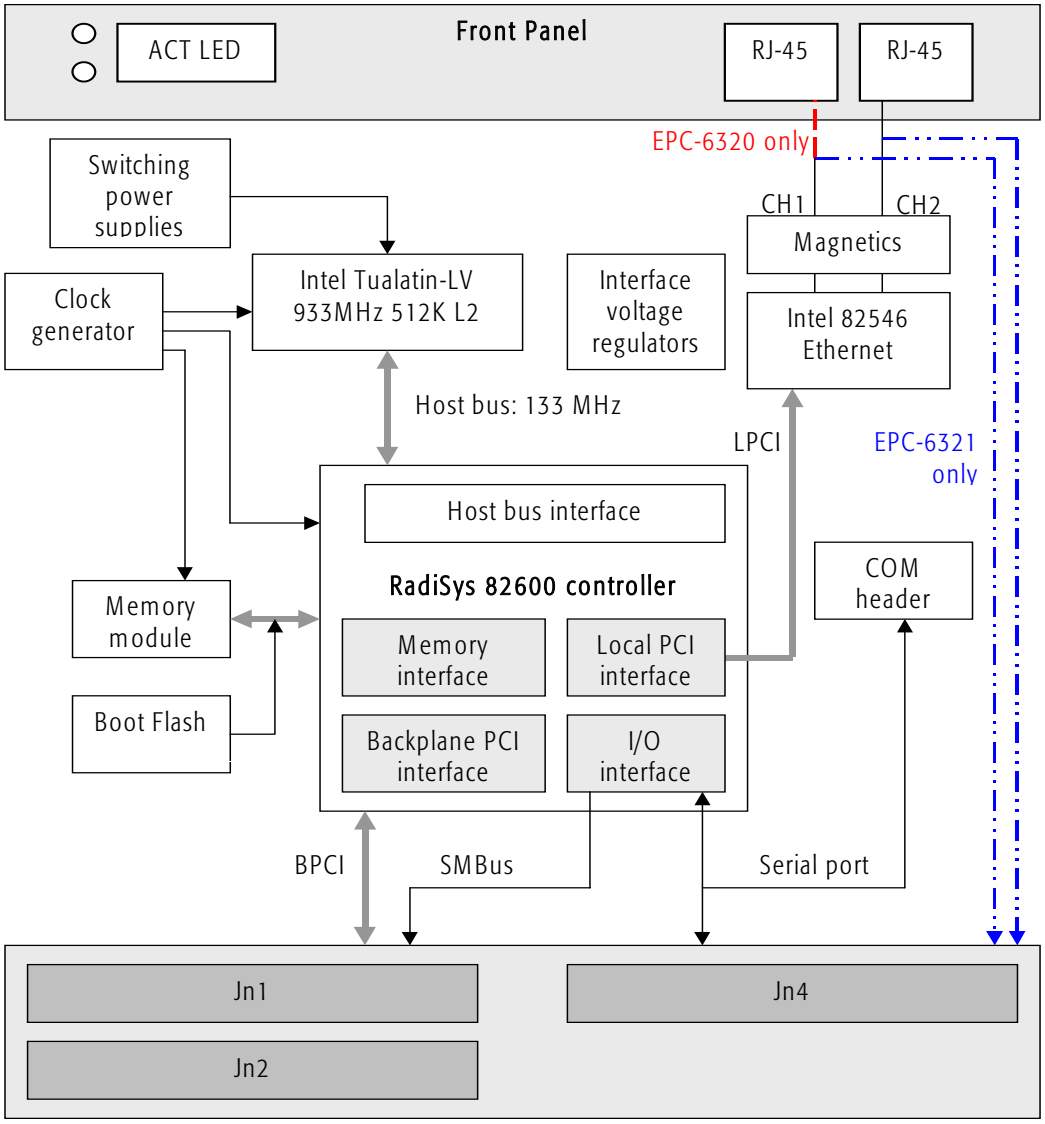
External Interfaces

The Jn1 and Jn2 connectors provide a 32-bit 33/66 MHz interface to the PCI bus on the baseboard and also provide power and ground connections compatible with the Processor PMC draft standard. The Jn4 connector provides a set of custom I/O, including EIDE, COM port signals.

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Block Diagram

Figure 5-1. Block Diagram



Description

The EPC-6320/21 has a CPU, clock generator, 82600 chipset, memory module, flash with BIOS, Ethernet, power and reset circuitry.

CPU

The EPC-6320/21 is designed around the Intel Tualatin 512K LV processor in the micro-FCBGA package, using Intel's advanced 0.13-micron process technology with copper interconnect.

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Processor internal speed is 933MHz with a 133MHz system bus frequency at +1.15V core power.

The 512 Kbit integrated L2 cache ATC with ECC architecture, runs at the processor core speed to improve performance. It complements the system bus by providing critical data faster and reducing total system power consumption.

The processor's 64-bit wide AGTL system bus provides a glueless, point-to-point interface for the RadiSys 82600 chipset.

Tualatin 512K LP processor Speed and Voltages

The Intel Tualatin 512K LV processor runs at fixed 933 MHz internal speed with 133 MHz Processor Side Bus (PSB). Speed step is not supported. Optional permanent throttling is available.

The CPU requires two distinct voltages:

- AGTL voltage (1.25V)
- Core voltage (1.15V).

The CPU also requires an AGTL reference voltage (VREF) that should be 2/3 of the AGTL termination voltage. This is accomplished using a resistor divider.

A high-efficiency switching regulator produces the appropriate processor VCORE and VCCT required. Maximum power draw for the CPU on a 933MHz Tualatin 512K LP processor is 12W. However, CPU power consumption varies, depending on CPU activities.

To prevent thermal runaway, the processor drives a ~Thermtrip signal. When this signal is driven active, both VCORE and VCCT power supplies turn off.

Clocking

The EPC-6320/21 includes two subsystems, divided by the BPCI interface:

- Devices connected to the BPCI bus have a separate, asynchronous clock generation domain.
- Devices behind the 82600 chipset all have one clock generation domain. These devices use an AMI Clock Generator to generate their clocks, which creates the following:
  - Four 133 MHz CPU bus clocks (frequency set at power-up by control inputs) provide clocking for the CPU, the 82600 chipset, the SDRAM memory card, and the ITP port.
  - One 66 MHz PCI clock (frequency set at power-up by control inputs) drives the LPCI Ethernet PCI interface.
  - One 33 MHz APIC clock is used for the 82600 internal APIC.

This clock generator has a spread-spectrum feature enabled through either SMBus programming or resistor strapping. The default is to have spread spectrum enabled.

All clock lengths are carefully routed to minimize EMI and to produce exactly the appropriate amount of skew for the design. The EPC-6320/21 supports only 100 MHz or 133 MHz processor and memory clock rates.

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The RadiSys 82600

The 82600, a highly integrated chipset, replaces these components in an embedded Intel Architecture I/O system: North Bridge, South Bridge, PCI-to-PCI Bridge and Super I/O. Packaged as a 576-pin BGA, the 82600 features include:

- Processor/host bus support
  Compatible with Intel Pentium processors.
  GTL+ bus driver technology.
  133 MHz processor side and memory bus support.
- Integrated SDRAM controller with direct Flash support
  512Mb technology support.
  512MB or 1GB of main memory.
  7.8, 15.6, and 125 microsecond refresh rates support.
  ECC support with automatic single bit error "scrub"and multiple bit error detect.
- Dual PCI bus architecture
  Independent local/backplane PCI buses with an integrated virtual PCI-to-PCI bridge.
  Isolated local and backplane peripherals.
  Asynchronous operation of both PCI buses.
- Local PCI (LPCI) bus
  33/66MHz interface, +3.3V interface.
  Internal arbiter.
- Backplane PCI (BPCI) bus
  +3.3V and 33/66MHz interface.
  All PCI central resource functions supplied.
  PCI central resource functions can be disabled for I/O processor applications.
- Integrated core PC logic
  Includes all legacy PC/AT compatible peripherals.
  Two 82C59 interrupt controllers.
  Two 82C37 DMA controllers.
  82C54 timer/counter.
  74LS612 address mapper.
- Real time clock
  256 byte battery-backed CMOS SRAM.
- Integrated peripherals
  Ultra DMA/66 EIDE interface.
  COM1 support with 16550 compatible UARTs.
  PS/2 compatible keyboard support.
  SMBus host interface.
- Integrated watchdog timer
  System lockup detection.
  Flexible hardware reset or interrupt on timeout.
- General purpose digital I/O
  Multiplexed with other pin functions.

Note

The 82600 does not support the LOCK function on the LPCI or BPCI buses. It also does not support parity checking or PERR reporting on either PCI bus.

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Power-up configuration: The following 82600 configuration options are determined during a power reset using pull-up or pull-down resistors on memory address lines.

ADDR0: Selection of general purpose I/O pins or the EIDE bus.

0 EIDE (default).

1 General-purpose I/O, DIO[0..15].

ADDR1: Selection of general-purpose I/O pins or bus arbitration signals ~BREQ[6:3] and ~BGNT[6:3].

0 General-purpose I/O (default)

1 Arbitration signals ~BREQ[6:3], ~BGNT[6:3].

ADDR2 and ADDR5:
Combination determines Monarch and non-Monarch mode:

ADDR2	ADDR5	Mode
0	0	Not allowed
1	0	Peripheral (non-Monarch)
0	1	Central resource without arbiter (Monarch)
1	1	Not allowed

ADDR3: Determines RTC status.

0 Enabled (default).

1 Disabled.

ADDR4: Determines boot flash location:

0 Boot Flash on the SDRAM bus (default).

1 Boot Flash on PCI bus.

ADDR6: Selection of either SDRAM ECC function or COM2.

0 Memory ECC enabled; COM2 is disabled (default).

1 COM2 is enabled; Memory ECC disabled.

ADDR7: Selection of general-purpose I/O pins or COM1 function.

0 COM1 (default).

1 General-purpose I/O, DIO [25..31].

ADDR8: Sets the I/O Queue depth.

0 8 (default).

1 1.

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ADDR10 and ADDR11:

Combination determines the PSB frequency:

ADDR10	ADDR11	Mode
0	0	N/A
1	0	133 MHz (default)
0	1	66 MHz (not supported for the EPC-6320/21)
1	1	100 MHz (not supported for the EPC-6320/21)

Host Bridge: The 82600 connects directly to the AGTL CPU local bus. The processor die includes CPU bus termination resistors. The bus length is minimized to obviate the need for termination resistors at the 82600. The 82600 segregates bus transactions as follows:

- 36 address-bit references.
- SDRAM references.
- LPCI bus cycles.
- BPCI bus cycles.
- Internal register.
- Special cycle (includes halt/shutdown, cache flush, etc.).
- Interrupt acknowledge.

Memory Subsystem: The EPC-6320/21 supports either 512 MB or 1GB of 133 MHz ECC custom memory modules on the main board. This discrete module connects through a set of low-profile connectors and provides all SDRAM to the EPC-6320/21.

The custom memory module provides an SPD memory with the memory configuration data. The SPD PROM connects via the SMBus serial interface on the 82600. The SPD is queried by the BIOS during POST to determine the computer's memory configuration. The SPD in the system is assigned address A0h.

BIOS Flash Support: The 4Mbyte FBD, which resides on the system board, consists of thirty-two 128KB blocks. The top 1Mbyte of the device holds the BIOS while the remainder of the device is available for OEM non-volatile storage.

For detailed information, see *Chapter 4, BIOS Configuration*.

PCI Interrupts

The CPU board has two sets of PCI interrupts, one for the LPCI and one for the BPCI.

For detailed information, see *Chapter 4, BIOS Configuration*.

Dual PCI bus architecture

The 82600 integrates dual PCI busses, a local and a backplane PCI bus. The Local PCI (LPCI) bus can be operated asynchronously at up to the host processor's clock rate or down to one quarter of this clock rate. Architecturally, it can be viewed as the high-speed private peripheral bus for the processor.

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As such, an LPCI bus master cannot directly access the BPCI bus or vice-versa. Whereas the LPCI bus interface always acts as the LPCI central resource bridge, the BPCI interface is intended to be connected to a "backplane" bus such as a baseboard and supports a peripheral bridge mode as well as a central resource bridging function.

The EPC-6320/21 connects to BPCI via the standard Jn1 and Jn2 PMC connectors and is compliant with *Processor PMC standard, VITA 32-2002, Draft 0.9.,* and supports these modes accordingly:

- **Monarch**: it is a main PCI bus processor module, performing PCI bus enumeration after power-up, and handles interrupts. Neither the clock generator nor an arbiter reside on the module.

> **Note**
> A resistor strapping option exists to provide a clock to the carrier card through the optional Jn4 connector. This allows a carrier to implement a simple clock buffer to distribute the clocks to other PCI devices on the carrier card.

- **Non-Monarch**: it does not perform PCI bus enumeration but may generate interrupts on the module.

The Monarch signal defines a Processor PMC as a Monarch or non-Monarch. The next table lists all EPC-6320/21 PCI devices.

Table 5-1. PCI Device Configuration

Peripheral	IDSEL[2]	Bus	Device	Function	INT	Arbitration
RadiSys 82600 Chipset	AD 11	0	0			Internal
Local PCI bridge			0	0		Internal
EIDE			0	1		Internal
Intel 82546 Ethernet controller, channel 1	AD13	0	2	0	A	Internal
Intel 82546 Ethernet controller, channel 2	AD13	0	2	1	B	Internal
Backplane PCI bridge[1] (Monarch)	AD 12	1	1	0		Internal
Backplane PCI bridge[1] (non-Monarch)						Set by user on the base card

1 The 82600 PCI Bridge appears differently, depending on whether the EPC-6320/21 operates as a Monarch or as a non-Monarch.

2 There is a strong correlation between the IDSEL chosen and the interrupt assigned. To read or write the configuration registers of a given device, a PCI configuration space access must be made with the device's corresponding IDSEL address bit set. For devices located on Bus 1, the IDSEL column is a recommendation to the carrier designer of which PCI address/data line to connect.

Local PCI Bus (Bus 0)

The EPC-6320/21 implements a 3.3V, 32-bit primary PCI bus, which runs at 33 or 66 MHz and has the RadiSys 82600 chipset as the central resource. The primary PCI bus has one peripheral device connected to it, an Intel 82546GB dual gigabit Ethernet controller.

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PCI Ethernet controller

The Intel 82546 dual gigabit Ethernet controller is a single compact component with two fully integrated Gigabit Ethernet MAC and PHY functions, providing a standard IEEE 802.3 Ethernet interface for 10Base-T, 100Base-TX, or 1000Base-X applications. In addition to the standard MDI interface, it provides SerDes I/O for both channels. The controller uses PCI interrupt A for one channel and PCI interrupt B for the other channel, ~REQ0/~GNT0 arbitration pairs, and has a standard PCI 2.2 compliant configuration space allowing system identification and configuration.

A 25 MHz, 50-PPM crystal provides this chip with clock generation for the internal PHY.

On the EPC-6320, an Intel-defined magnetic interface connects between the PHY and two RJ45 connectors (located on the front panel).

On the EPC-6321, an Intel-defined magnetic interfaces connects to Jn4.

A serial PROM provides nonvolatile storage for an Ethernet address and any additional necessary configuration information. The 82546GB drives the status LEDs directly.

Backplane PCI bus (Bus 1)

The EPC-6320/21 implements a +3.3V, 32-bit backplane PCI bus. The bus runs at 33 or 66 MHz and, when configured as a Monarch, has the RadiSys 82600 chipset as the central resource.

The CPU board supports a backplane via standard Jn1 and Jn2 PMC connectors.

IDE Controller

One EIDE channel is provided via the Jn4 connector, allowing connection of up to two IDE devices on the carrier card.

Note

A maximum cable link is 18" from Jn4 connector. If a second drive is added to a cable, it must be within 4" of the first drive connection.

RTC

The RadiSys 82600 provides:

- An internal RTC that tracks the time of day.
- A standard 256-byte CMOS RAM for storing system data during a system power-down.

The RTC operates on a 32.768 KHz crystal with greater than or equal to 50-PPM stability specification. No battery is provided on the CPU board. The RTC and CMOS RAM are addressable at the standard PC/AT architecture I/O addresses 70h and 71h. Interrupts are signaled on IRQ8.

Serial Port

The 82600 includes two 16C550 UARTs. The COM1 port may be configured to support IRDA at data rates up to 115 Kbaud. The default setting is 9600 baud. As in a

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standard PC, COM1 is accessed in the I/O address space at 0x3F8 to 3FF and signals interrupts on IRQ4. The COM2 configurable port shares eight pins with the SDRAM ECC pins. When the ECC function (power-on option bit) is used, COM2 port pins are not externally available and COM2 is disabled.

The SERIRQ protocol is not supported, as it responds only to the devices on for the LPCI bus.

The clock for the COM port is programmed in the COM port option register.

Keyboard Controller

The EPC-6320/21 provides a PC/AT compatible keyboard and mouse connections via the Jn4 header. These functions are an integrated function within the 82600 chipset.

Miscellaneous I/O Interrupts

The PC-AT compatible interrupt usage is detailed in the *Chapter 4, BIOS Configuration*.

GPIO pins

The system can be configured to use extra arbitration signals (~BREQ[6:3] and ~BGNT[6:3]) as general input/output pins; GPIO. Details on power up configuration are described in *Power-up configuration* on page 50.

If the system is configured to use GPIO, pins 49 to 56 of Jn4 become GPIO 16 to 23, respectively.

Power and Reset

The next table lists estimated the CPU board power consumption.

Table 5-2. Power Estimates

Voltage	RMS current		Peak current
	Type	Max	
+3.3V	3.3A	3.9A	4.2A
+5V	1.9A	2.5A	2.7A
+12V	–	–	–
–12V	–	–	–
Total power:	21W	26W	

Note

- The PMC specification limits power to 0.5 A per connector pins:
  Jn1–6 and Jn4–1 = 7 pins +5V: 3.5A maximum.
  Jn2–9 and Jn4–1 = 10 pins +3.3V: 4.5A maximum.
- Additional power pins on the Jn4 connector are provided only on the EPC-6320 and EPC-6320N.
- This data is preliminary and subject to change. This table includes the power requirements for the 1GB memory SDRAM module.

A linear regulator working from +3.3V supplies the 82600's core logic power supply (+2.5V). The expected load current is 400mA.

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Power to CPU VCORE +1.15V and Vcct +1.25V are supplied by a Linear Technologies LTC1703 dual synchronous switching regulator along with external FETs. The LTC1703's five voltage identification inputs are programmed with resistors to set output voltage VCORE to +1.15V. The other side of the controller provides the CPU AGTL termination voltage, VCCT at 1.25V using a resistor divider network. The LTC1703 design can provide up to 25A output current per channel. The current limit is set to 15A for VCORE and to 5A for VCCT. The expected maximum load current is 10.5A and 2.3A for VCORE and VCCT respectively.

Interface voltage regulators consist of a series of linear regulators generating +1.5V and +2.5V to supply CPU, clock generator, 82600 and network controller various voltage requirements.

A precision voltage reference in conjunction with a voltage comparator provides monitoring of the +5V and +3.3V supplies. The open collector outputs of the comparators connect directly to the soft-start inputs for the switching regulator that creates VCORE and VCCT. As soon as +3.3V and +5V planes are fully charged, the switcher begins to power on VCCT and, after VCCT is stable, VCORE starts. Voltage comparators also monitor the status of VCORE, VCCT, +2.5V, +1.8V, +1.5V power. The open collector outputs of the comparators are tied to the system power good line and causes system reset on any power failure. As soon as the voltages are valid, the board comes out of reset.

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A Message Codes

This appendix lists the Phoenix BIOS 4.06 standard POST error codes which can generate console messages.

Class	Number	Name
Disk errors	200h	ERR_DISK_FAILED
Keyboard errors	210h 211h 212h 213h	ERR_KBD_STUCK ERR_KBD_FAILED ERR_KBD_KCFAIL ERR_KBD_LOCKED
Video errors	220h	ERR_VIDEO_SWITCH
Memory errors	230h 231h 232h 233h 234h 235h 236h 237h	ERR_SYS_MEM_FAIL ERR_SHAD_MEM_FAIL ERR_EXT_MEM_FAIL ERR_MEM_TYPE_MIX ERR_MEM_ECC_SINGLE ERR_MEM_ECC_MULTIPLE ERR_MEM_DECREASED ERR_DMI_MEM_FAIL
POS/timeout errors	240h	ERR_POS
CMOS errors	250h 251h	ERR_CMOS_BATTERY ERR_CMOS_CHECKSUM
Timer errors	260h	ERR_TIMER_FAILED
Real-time clock errors are x70h	270h	ERR_RTC_FAILED
Invalid date time	271h	ERR_RTC_INV_DATE_TIME
Configuration errors	280h 281h	ERR_CONFIG_FAILED ERR_CONFIG_MEMORY
NVRAM errors	290h	ERR_NVRAM
Diskette errors	2B0h 2B1h 2B2h 2B3h	ERR_FLOPPYA_FAILED ERR_FLOPPYB_FAILED ERR_FLOPPYA_INCORRECT ERR_FLOPPYB_INCORRECT
Load errors	2C0h	ERR_LOADED
Cache errors	2D0h	ERR_CACHE_FAILED
System memory exceeds CPU caching limit	2D1h	ERR_L2_CACHE_RANGE
IO errors	2E0h 2E1h 2E2h 2E3h 2E4h 2E5h 2E6h 2E7h 2F0h 2F1h 2F2h 2F3h 2F4h 2F5h 2F6h 2F7h	ERR_IO_ADDRESS ERR_IO_COM ERR_IO_LPT ERR_IO_CONFLICT ERR_IO_UNSUPPORTED ERR_IO_IRQ ERR_IO_IDE ERR_IO_FDD ERR_OTHER_CPUID ERR_OTHER_BIST ERR_OTHER_BSP ERR_OTHER_AP RR_OTHER_CMOS ERR_OTHER_DMA ERR_OTHER_NMI ERR_OTHER_FAILSAFE

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B Interrupts

The next table shows {ProductNameShort} interrupt assignments. This routing is implemented by the RadiSys 82600 embedded chipset.

Table B-1. Interrupts

Interrupt	Description
IRQ0[1]	System timer (internal connection)
IRQ1[1]	Keyboard controller (internal connection)
IRQ2	Cascade interrupt input (internal connection)
IRQ3[2]	
IRQ4[1, 2]	COM1 (internal connection)
IRQ5[2]	
IRQ6	
IRQ7	
IRQ8[1]	Real-time clock (internal connection)
IRQ9[1, 2]	SMBus, reset switches, power management, DMA, BIST (via Serial IRQ)
IRQ10[2]	Soft reset is imminent via serial IRQ from Watchdog
IRQ11[2]	
IRQ12[1, 2]	PS/2 (internal connection)
IRQ13	Numeric coprocessor ~FERR (internal connection)
IRQ14[1]	Primary IDE channel
IRQ15[2]	
NMI[1]	When ~SERR or ~IOCHK is asserted (software controlled)
SMI	Power management or ECC error
PIRQA	Intel 82546 Ethernet controller, channel 1
PIRQB	Intel 82546 Ethernet controller, channel 2
PIRQC	
PIRQD[1]	

1 You cannot move these items.

2 You can include these items in the PCI interrupt pool.

Note

Note that PIRQ[A–D] correspond directly to the PCI interrupts INT[A–D]. The software may steer these interrupts to any of the 11 interrupts (IRQ[15, 14, 12–9, 7–3]) using the Interrupt Route Control register.

For detailed information, see *Chapter 4, BIOS Configuration*.

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C Connectors

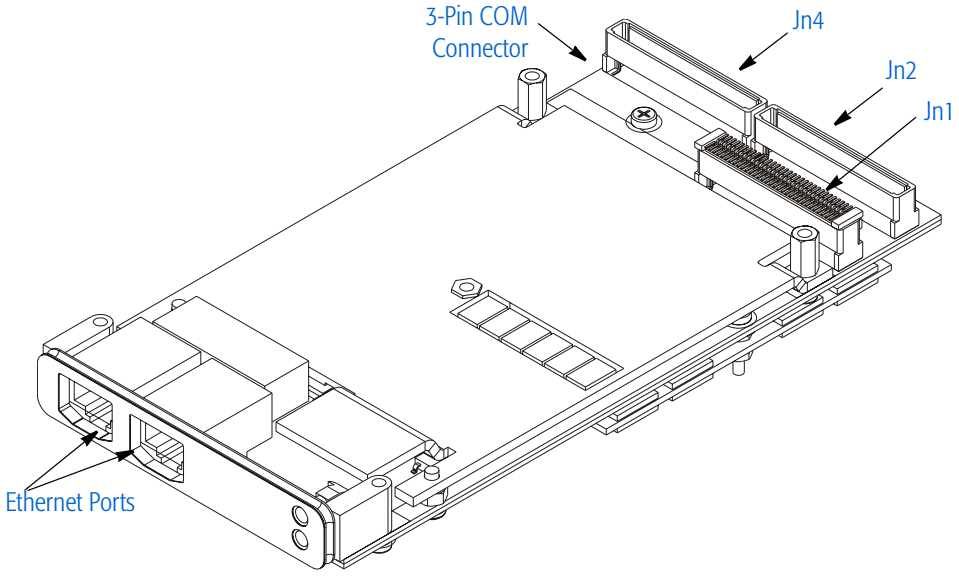
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This appendix details the connectors used by the EPC-6320/21 and gives the signal pinout of each connector.

Connector Locations

The next figure shows the locations of connectors on the EPC-6320/21:

Figure C-1. EPC-6320: Connectors



Note

Signals used for a purpose other than that identified in the appropriate specification are noted as follows:

XYZ / NC

Specified use RadiSys use

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PMC Connectors

Jn1 connector

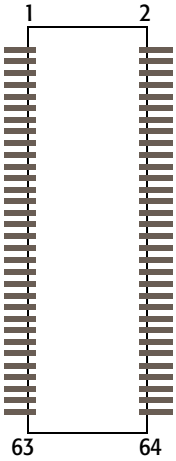


Table C-1. Jn1 Connector Pin Definitions

Pin	Signal	Signal	Pin
1	TCK/NC	–12V/NC	2
3	GND	~INTA	4
5	~INTB	~INTC	6
7	Present	+5V	8
9	~INTD	PCI-Reserved/NC	10
11	GND	+3.3V	12
13	PCICLK	GND	14
15	GND	~GNT0	16
17	~REQ0	+5V	18
19	+3.3V V(I/O)	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	GND	24
25	GND	C/~BE[3]	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	+3.3V V(I/O)	AD[17]	32
33	~FRAME	GND	34
35	GND	~IRDY	36
37	~DEVSEL	+5V	38
39	GND	~LOCK/NC	40
41	SMB_CL	SB_DT	42
43	PAR	GND	44
45	+3.3V V(I/O)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	GND	C/~BE[0]	52
53	AD[06]	AD[05]	54
55	AD[04]	GND	56
57	+3.3V V(I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	GND	~REQ64/NC	64

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Jn2 Connector

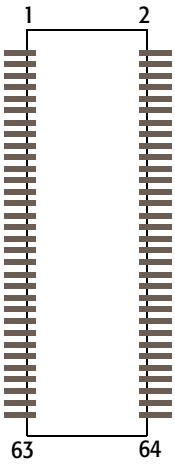


Table C-2. Jn2 Connector Pin Definitions

Pin	Signal	Signal	Pin
1	+12V/NC	~TRST/NC	2
3	TMS/NC	TDO/NC	4
5	TDI/NC	GND	6
7	GND	PCI-Reserved/NC	8
9	PCI-Reserved/NC	PCI-Reserved/NC	10
11	PUP	+3.3V	12
13	~RST	PDN	14
15	+3.3V	PDN	16
17	~PME/NC	GND	18
19	AD[30]	AD[29]	20
21	GND	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL	AD[23]	26
27	+3.3V	AD[20]	28
29	AD[18]	GND	30
31	AD[16]	C/~BE[2]	32
33	GND	IDSELB	34
35	~TRDY	+3.3V	36
37	GND	~STOP	38
39	~PERR/NC	GND	40
41	+3.3V	~SERR	42
43	C/~BE[1]	GND	44
45	AD[14]	AD[13]	46
47	M66EN	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	~REQB	52
53	+3.3V	~GNTB	54
55	NC	GND	56
57	NC	EREADY[1]/NC	58
59	GND	~RESETOUT[1]/NC	60
61	~ACK64	+3.3V	62
63	GND	~Monarch	64

[1] Not supported.

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Jn4 Connector

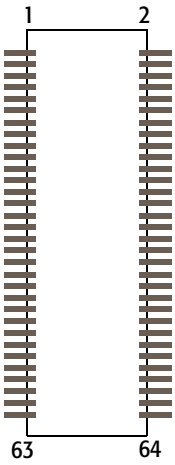
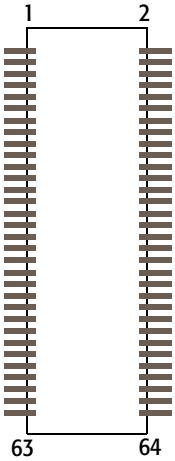


Table C-3. EPC-6320 Optional JN4 Connector Pin Definitions

Pin	Signal	Signal	Pin
1	IDE:~RST	IDE:D8	2
3	IDE:D7	IDE:D9	4
5	IDE:D6	IDE:D10	6
7	IDE:D5	IDE:D11	8
9	IDE:D4	IDE:D12	10
11	IDE:D3	IDE:D13	12
13	IDE:D2	IDE:D14	14
15	IDE:D1	IDE:D15	16
17	IDE:D0	GND	18
19	GND	IDE:CS0	20
21	IDE:~IOW	IDE:CS1	22
23	IDE:~IOR	IDE:A0	24
25	IDE:IORDY	IDE:A1	26
27	IDE:~IRQ	IDE:A2	28
29	GND	GND	30
31	NC	NC	32
33	NC	NC	34
35	GND	GND	36
37	KCLK	KDATA	38
39	COM,~DTR	COM,~DSR	40
41	COM, ~DCD	COM,~RxD	42
43	COM,~TxD	COM,~CTS	44
45	COM,~RTS	COM,~RI	46
47	+5V	NC	48
49	BPCI:~GNT3	BPCI:~REQ3	50
51	BPCI:~GNT4	BPCI:~REQ4	52
53	BPCI:~GNT5	BPCI:~REQ5	54
55	BPCI:~GNT6	BPCI:~REQ6	56
57	~DASP	~PDIAG	58
59	$BPCIREF	+3.3V	60
61	NC	PWR_BAT_IN	62
63	IDE:DMREQ	IDE:~DMACK	64

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Table C-4. EPC-6321 Optional JN4 Connector Pin Definitions



Pin	Signal	Signal	Pin
1	CHA_MDI0+	CHA_MDI2+	2
3	CHA_MDI0–	CHA_MDI2–	4
5	GND	GND	6
7	CHA_MDI1+	CHA_MDI3+	8
9	CHA_MDI1–	CHA_MDI3–	10
11	GND	GND	12
13	CHB_MDI0+	CHB_MDI2+	14
15	CHB_MDI0–	CHB_MDI2–	16
17	GND	GND	18
19	CHB_MDI1+	CHB_MDI3+	20
21	CHB_MDI1–	CHB_MDI3–	22
23	GND	GND	24
25	IDE:IORDY	IDE:A1	26
27	IDE:IRQ	IDE:A2	28
29	IDE:~IOR	IDE:A0	30
31	NC	NC	32
33	NC	NC	34
35	GND	GND	36
37	KCLK	KDATA	38
39	IDE:~RST	IDE:~CS1	40
41	IDE:D7	COM,~RxD	42
43	COM,~TxD	IDE:D9	44
45	IDE:6	IDE:D10	46
47	IDE:5	IDE:~CS0	48
49	IDE:4	IDE:D11	50
51	IDE:3	IDE:D12	52
53	IDE:2	IDE:D13	54
55	IDE:1	IDE:D14	56
57	IDE:~DASP	IDE:D8	58
59	IDE:D0	IDE:D15	60
61	IDE:~IOW	PWR_BAT_IN	62
63	IDE:DMREQ	IDE:~DMACK	64

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Ethernet Ports

The front panel RJ45 connectors provide support for two 10/100/1000Base-TX Ethernet channels. The RJ45 connectors do not contain magnetics and LEDs.

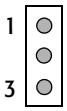
Table C-5. Ethernet Pin Definitions

Pin	Description	Pin	Description
1	MDI0+	6	MDI2–
2	MDI0–	7	MDI1–
3	MDI1+	8	MDI3+
4	MDI2+	9	MDI3–

3-Pin COM Connector

This optional 3-pin header, when connected via cable to an input device, provides access to the system BIOS.

Table C-6. 3-Pin Connector Pin Definitions



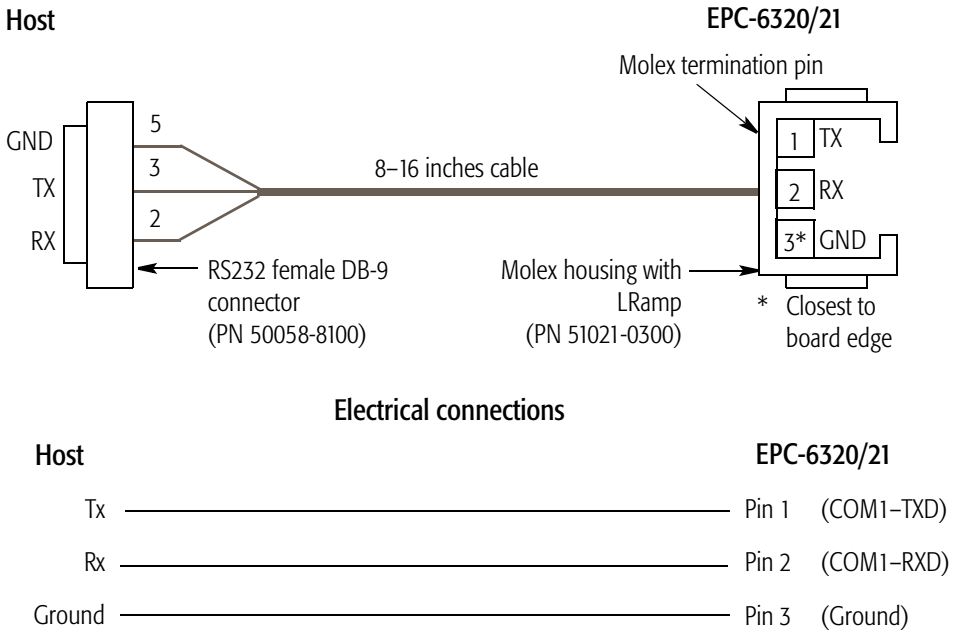
Pin	Signal
1	COM1–TXD
2	COM1–RXD
3	GND

Null-Modem Serial Cable

RadiSys does not supply the serial cable. To assemble the cable, you will need the following:

Item	Part number
3 pin connector	Molex receptacle 51021-0300
Female crimp terminal	Molex 50058-8100
RS232 connector	Standard RS323 female DB-9 serial connector
Recommended cable	Belden 8643 (Round, 3 Conductor, 30 Gage) or Molex Series 6800 (Flat, 3 Conductor, 28 Gage), cut to desired length (i.e. 8- 16 inches)

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LEDs

Two indicator LEDs are located on the front panel.

Table C-7. Front Panel LED Descriptions

Label	Color	Description
Link/Act A	Solid green	Link
	Blinking green	Ethernet activity
	Yellow	Reset
Link/Act B	Solid green	Link
	Blinking green	Ethernet activity
	Yellow	Reset

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D Error Messages

Upon encountering the following error conditions, the System BIOS tries to display a message to the console, then halts:

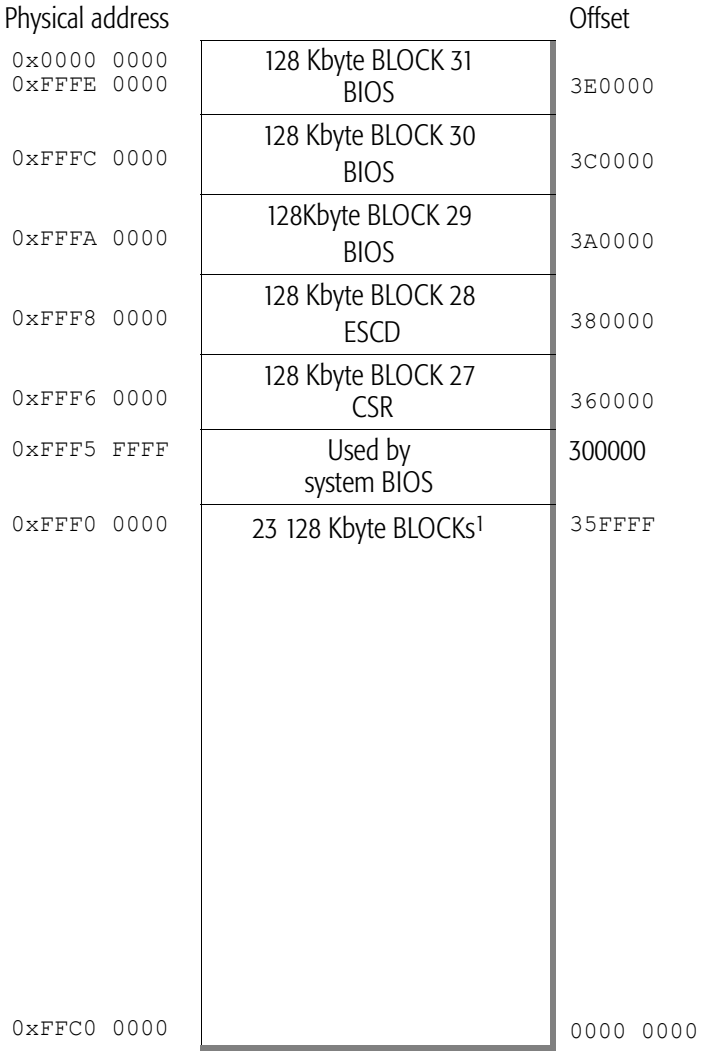
1. Fixed disk errors
    - No drive connected
    - Configured for 0 cylinders
    - Controller reset failed
    - Drive not ready
    - Track 0 seek timed out
    - Drive initialization failed
    - Drive recalibration failed
    - Last track seek failed
2. Video error
    - Color/Mono switch not set correctly
3. Timer error
    - System timer (0) failed
4. Diskette error
    - Floppy type does not match setup
5. I/O chip error
    - I/O conflicts exist for serial and parallel ports, floppy, hard disk (any or all)
6. Other error
    - IRQ conflict, unsupported COM port configuration, keyboard locked
    - Pentium cooling fan has failed
    - The System BIOS *prints* an error message *but does not halt* when it encounters the following error conditions:
        - Configuration error
        - Previous POST execution was incomplete
        - User BIOS Extension Region X exceeds DFFFFh

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Flash Memory Addresses

The EPC-6320/21 flash chip contains these major sections:

Figure E-1. Flash chip memory addresses



1 This area of the flash consists of 23 blocks, each containing 128Kbytes.

Note

For information about re-programming the flash chip's contents, see *Appendix F, Re-Programming the Flash Chip*.

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F Re-Programming the Flash Chip

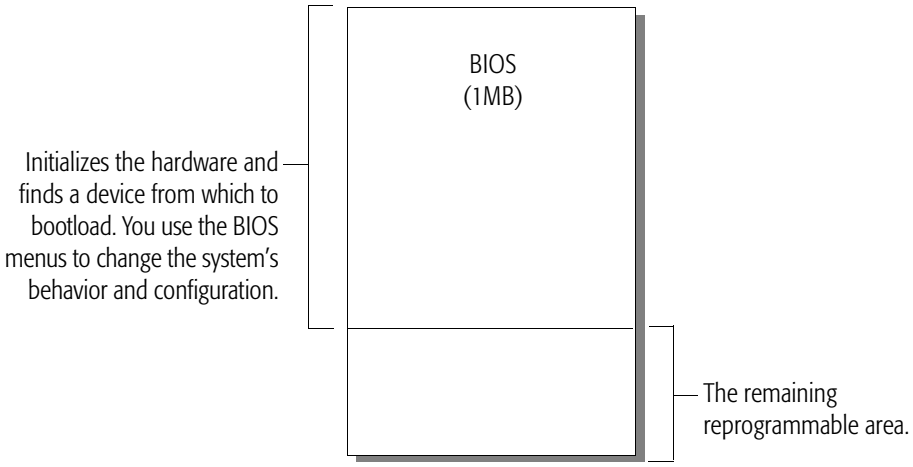
About the Flash Chip 67
About Re-Programming the Flash Chip 68
Before you Begin 68
Creating a Flash Boot Image 69
Using phlash.exe to Re-Program the Flash Chip 70

This appendix details how to update or recover your Flash Boot Device (FBD). You accomplish this by re-programming all or part of the EPC-6320/21's flash chip.

About the Flash Chip

The EPC-6320/21 flash chip contains these major sections:

Figure F-1. Flash Chip Configuration



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About Re-Programming the Flash Chip

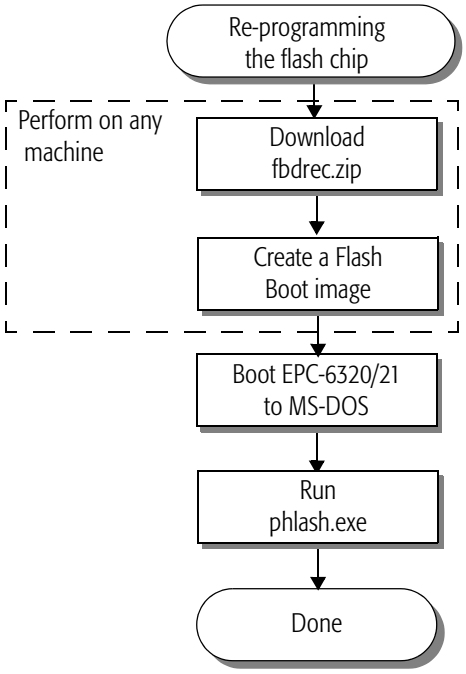
On rare occasions, part or all of the flash chip contents may require replacement.

⚠ CAUTION
Use extreme caution when re-programming the flash chip.

You can force re-programming via the phlash program, which re-programs the entire flash chip from a DOS command prompt.

When re-programming the flash chip, follow this process. The rest of this chapter includes detailed instructions for each task:

Figure F-2. Flash Chip Re-Programming Process Flow



Before you Begin

Ensure that you have the following:

- Minimum 2 MB of DRAM to run the re-flash program.
- A 3.5" 1.44 MB hard drive attached to or installed in the system.
- Access to the RadiSys web site.

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Creating a Flash Boot Image

Re-programming the flash chip requires a Flash Boot image that contains both code to perform the task and data to place in the chip.

To create the Flash Boot image on a hard drive:

1. Locate this file from the RadiSys web site and download it to your computer:

   `fbdrec.zip`

2. Unzip the contents to a directory on your hard drive.

   When unzipped, verify that these files required to re-program the flash chip are copied successfully to your hard drive:

Filename	Description
readme.txt	Describes the transmittal and includes instructions and issues that arose too late to include in other documentation
bios.rom	A binary file that contains the BIOS image and Boot Block.
phlash.exe	The program that re-programs the flash chip using data from the other files.
platform.bin	A file that describes the flash chip configuration, and identifies which blocks to erase and re-program.

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Using phlash.exe to Re-Program the Flash Chip

1. Boot the EPC-6320/21 into MS-DOS with no memory managers running.
2. Copy the Flash Boot image to the system.

> **Note**
> For detailed information about creating a Flash Boot diskette, see *Before you Begin* on page 68.

3. Start the re-programming process using one of these methods:
   - Run the phlash program using a command similar to this:

     ```
     c:\phlash /mode=3
     ```

   - Run the update batchfile.

   When finished, the phlash program displays a message, then automatically reboots the system.

> **Note**
> If using only console redirection, messages do not display. You must wait approximately three minutes for the reflash to complete. The system automatically reboots when reflash is complete.

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G

Carrier Card Design

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To use Monarch mode, you must design a carrier card that supports Monarch mode. The rest of this appendix provides guidelines for designing such a card.

PrPMC Connectors (Jn1 and Jn2)

General

Leave all reserve pins unconnected.

The PCI:~RST signal is an input to the PrPMC. It should be driven by an open collector device and it requires a pullup (1K to +5V) for the EPC-6320/21 to operate properly.

Power

The EPC-6320/21 includes the following power considerations: +5V, +3.3V, +12V, –12V, and VI/O.

VCC and +3.3V requires:

- A single bulk bypass near the power connection to the EPC-6320/21.
- A high-frequency decoupling cap at each pin.

+12 and –12V are not used on the board and only require the high-frequency decoupling cap.

VI/O requires a a high-frequency decoupling cap on each pin. VI/O can be either +5V or +3.3V.

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PCI

Design interrupt and IDSEL routing to match the *PCI-to-PCI Bridge Architecture Specification Revision 1.1*.

The ~SDONE and ~SBO signals are PCI-RSV in Vita 32, and provide optional I^2C interface to the PMC bus. Tie JTAG signals to an inactive state. That is, TCK and ~TRST low and TMS and TDI high. Leave TDO unconnected.

Tie ~BUSMODE1 and ~BUSMODE2 through a resistor to VI/O. ~BUSMODE3/NC and ~BUSMODE4/NC can be left unconnected. Although the PrPMC specification requires that these have 10K Ohm pull-down resistors, these are not required for ~BUSMODE3/NC and ~BUSMODE4/NC.

~REQ64 and ~ACK64 should be bussed and tied through a resistor to VI/O.

Jn1

Clocking

The carrier card must provide clocking to the PrPCMC.

Arbitration

The carrier card must provide arbitration to the PrPCMC.

Jn2

Processor PMC

M66EN should be bussed and pulled low for 33MHz operation, and high for 66MHz operation.

IDSELB/NC is not used and may be tied low.

Tie Monarch pin low to enable Monarch mode and high to enable non-Monarch mode. A jumper is recommended to change modes.

The The EPC-6315 does not use the ~RSTOUT/NC signal. However, RadiSys recommends that you bus this signal to all PrPMC sites.

The RadiSys PrPMC does not use the serial interrupt mechanism. However, RadiSys recommends tying ~SERIRQ signal through a resistor to VI/O.

RadiSys-Defined PrPMC Connector (Jn4)

Note

The Jn4 pinout of the EPC-6320 and EPC-6321 differ. For details, see *Jn4 Connector* on page 61.

IDE

RadiSys recommends placing series termination resistors (33.2 Ohms) next to all IDE signals on Jn4, with the exception of the ~IOR, IORDY and ~RST signals. ~IOR should

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have an AC termination (100 Ohms and 10pF) next to the IDE drive connector on the carrier card. ~IOR should have a series termination resistor (33.2 Ohms) next to the IDE drive connector on the carrier card.

RadiSys recommends adequate bulk and high-frequency decoupling near the IDE drive connector on the carrier card.

Keyboard and Mouse

Jn4 provides keyboard and mouse clock and data signals as well as +5V for systems that need to use the EPC-6315's internal keyboard and mouse controller.

Serial Port

Jn4 provides all signals needed to implement a full serial port for systems desiring to use the EPC-6320/21's embedded serial port (COM1). The EPC-6321's Jn4 connector has a 3-pin COM port only.

Clocking

You can use BPCIREF, a PCI output clock, to buffer and provide clocks to the rest of the PCI system on the carrier card. The frequency of this clock is set by the state of the M66EN signal. For more information about this signal, see *Jn2 Connector* on page 60.

Arbitration

Jn4 provides four pairs of arbitration signals that you can use in place of an arbiter on the carrier card. For more information, see Table 5-1, *PCI Device Configuration* on page 52.

RTC Battery

Jn4 provides PWR_BAT_IN, a connection for the battery. The battery provides backup power to the BIOS CMOS settings for occasions when power is not applied.

UL requires a 1K series resistor. RadiSys recommends isolating this from the +3V power supply with a low-leakage Schottky diode. RadiSys provides this series resistor and a low leakage Schottky resistor on the EPC-6320/21.

Mechanical and Thermal Design

The two mounting holes for the front panel are electrically isolated from the rest of the board. The back mounting holes (near Jn1 and Jn4) are connected to logic ground. The reference schematics do not show this properly connected.

Power consumption

The EPC-6320/21 uses a considerable amount of power from both +5.0V and +3.3V supplies. Ensure that the power supplies on the carrier card can support the full amount of current. Also, when possible, to keep the EPC-6320/21 as cool as possible, avoid placing high power dissipation components in the vicinity of the PMC.

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Airflow

Place the EPC-6320/21 in a pressurized chassis pushing air across the card. The required airflow should be 200 LFM at the carrier card. Airflow direction should be from the CPU/memory edge to the RadiSys 82600 chipset edge.

Ensure 200 LFM of airflow exists at the leading edge of the heat spreader, regardless of which carrier card PMC slot is used (this indicates no air blockage by other components on the carrier or another PMC).

The carrier card design should accommodate the specific heights of the EPC-6320/21 components:

- In the I/O region, the the PMC specification limits maximum EPC-6320/21 component height to 13.5mm.
- In the component region, the maximum component height is 8.2mm.

Of particular interest to designers is that J1 provides user access to the serial port. This 5.7mm tall connector is located where Jn3 normally sits on a carrier card. If this conflict with your carrier card's requirements, contact RadiSys.

Maximum Ambient Temperature

Maximum ambient temperature is 50°C at the EPC-6320/21.

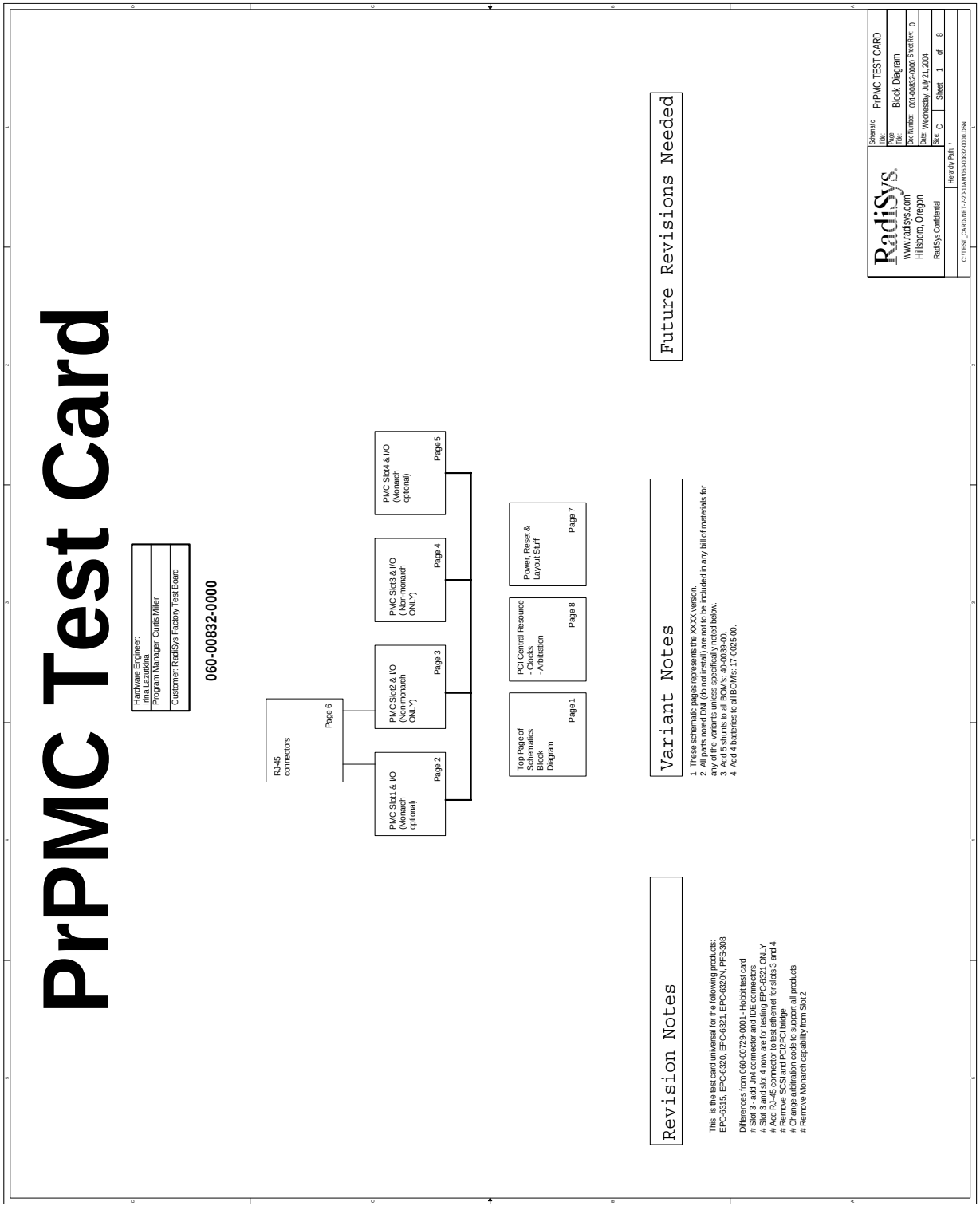
Carrier Card Schematic Samples

The remainder of this appendix includes sample schematics that you can use as reference when designing a carrier card.

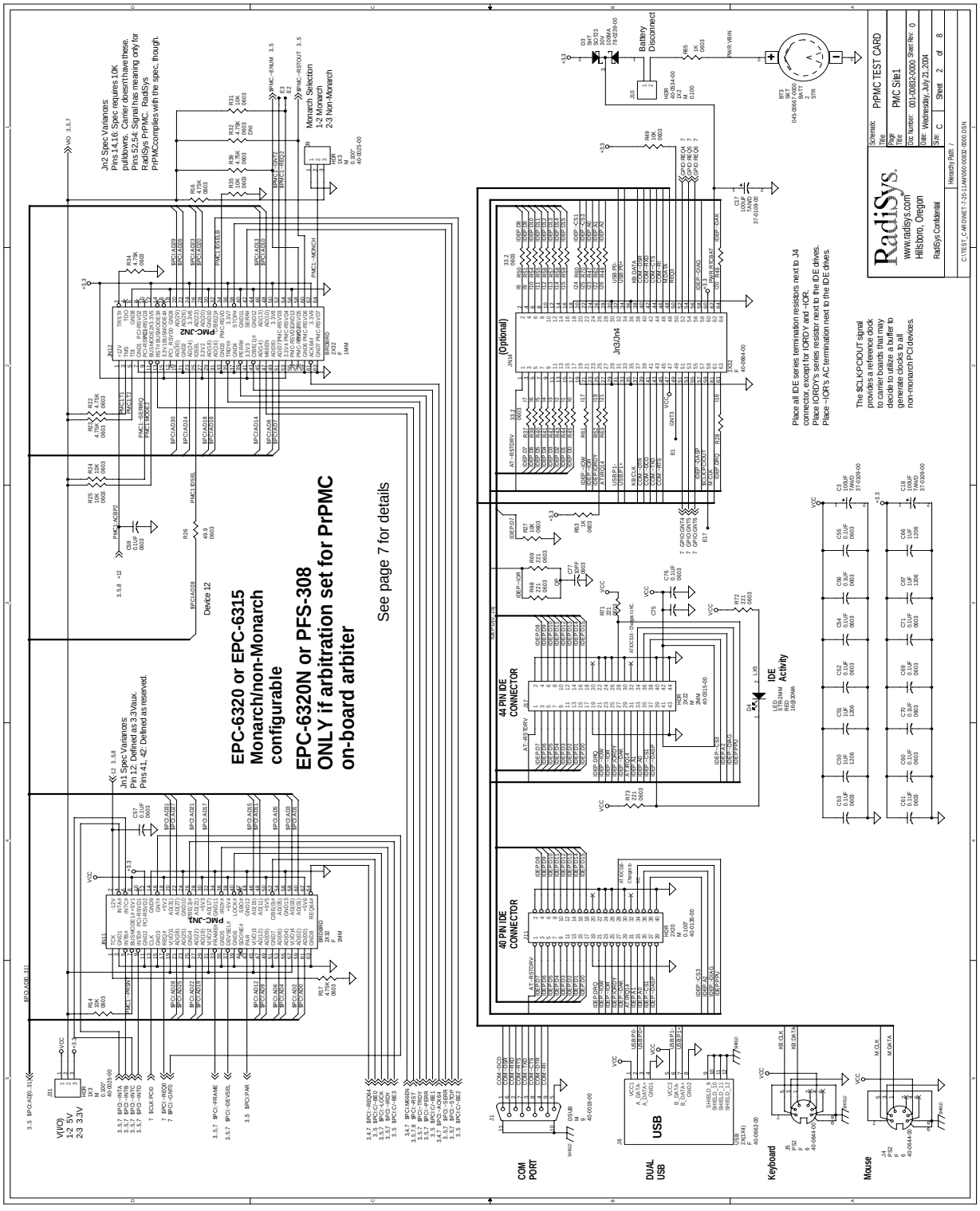
These schematics:

- Include a series resistor and diode between the battery and the Jn4 of the PMC sites; the resistor and diode are not necessary.
- Do not include pull-up resistors on the arbitration signals, located at *sheet 8* on page 75.
- Do not properly show the proper connection between the PMC mounting and keying holes and logic ground.

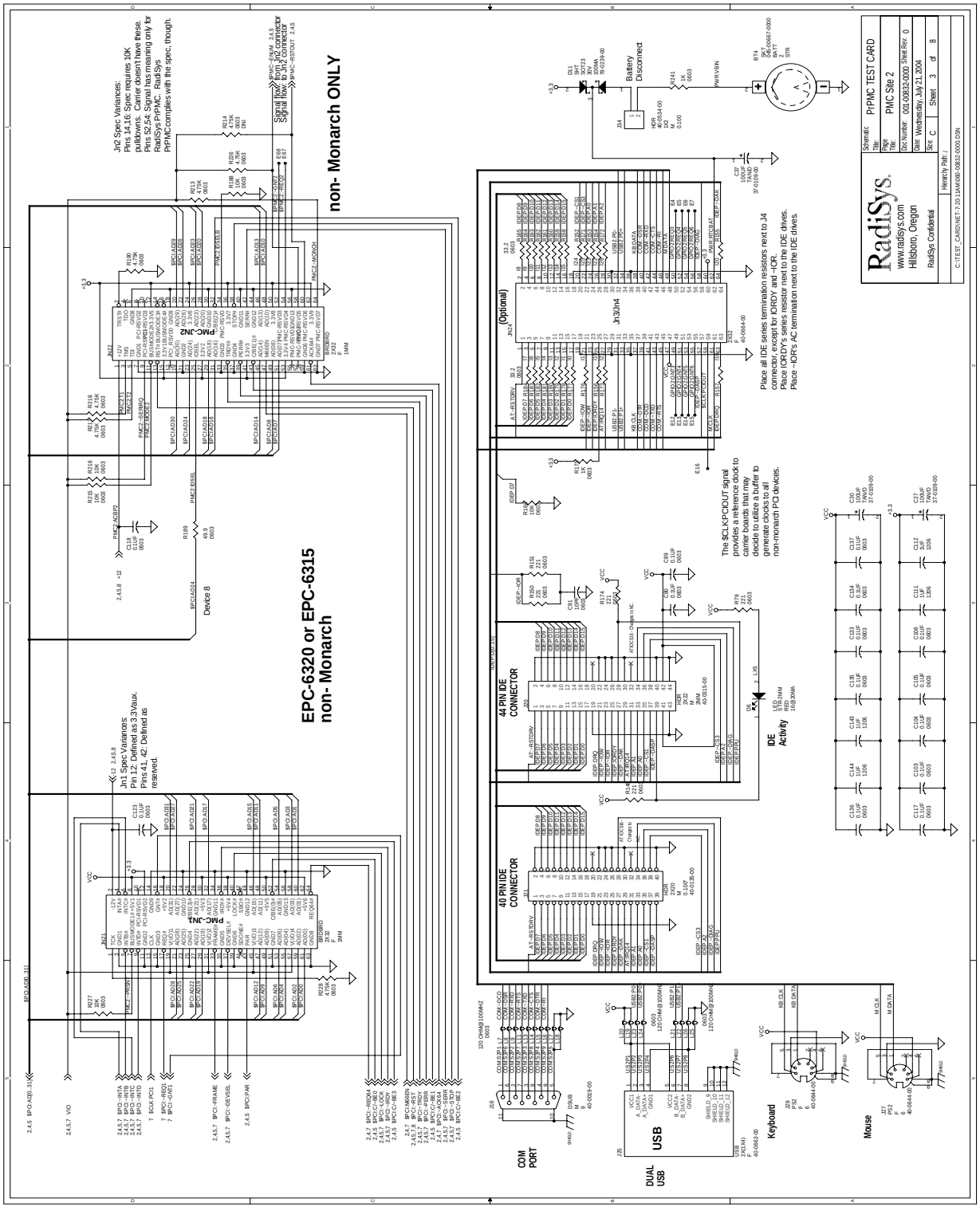
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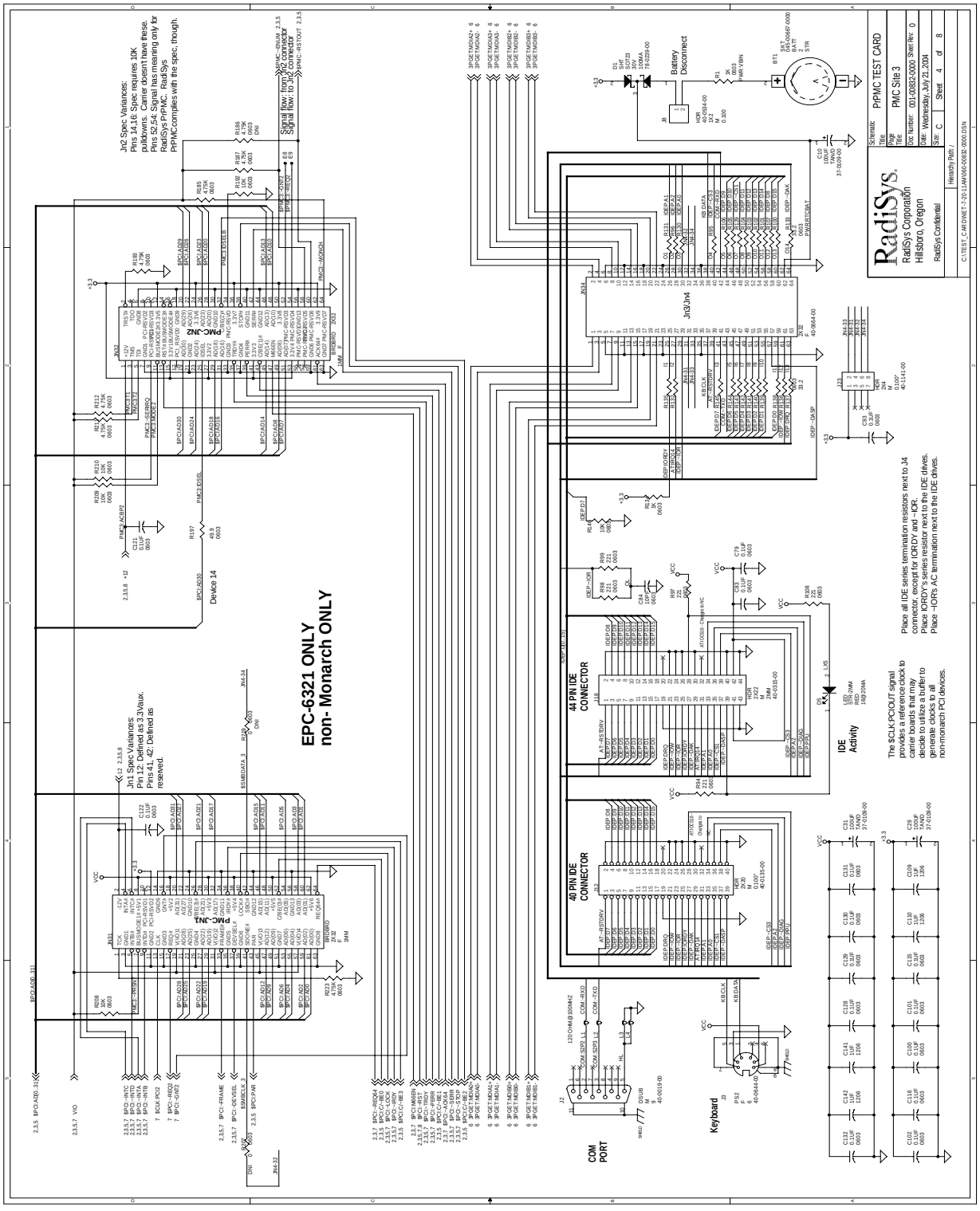
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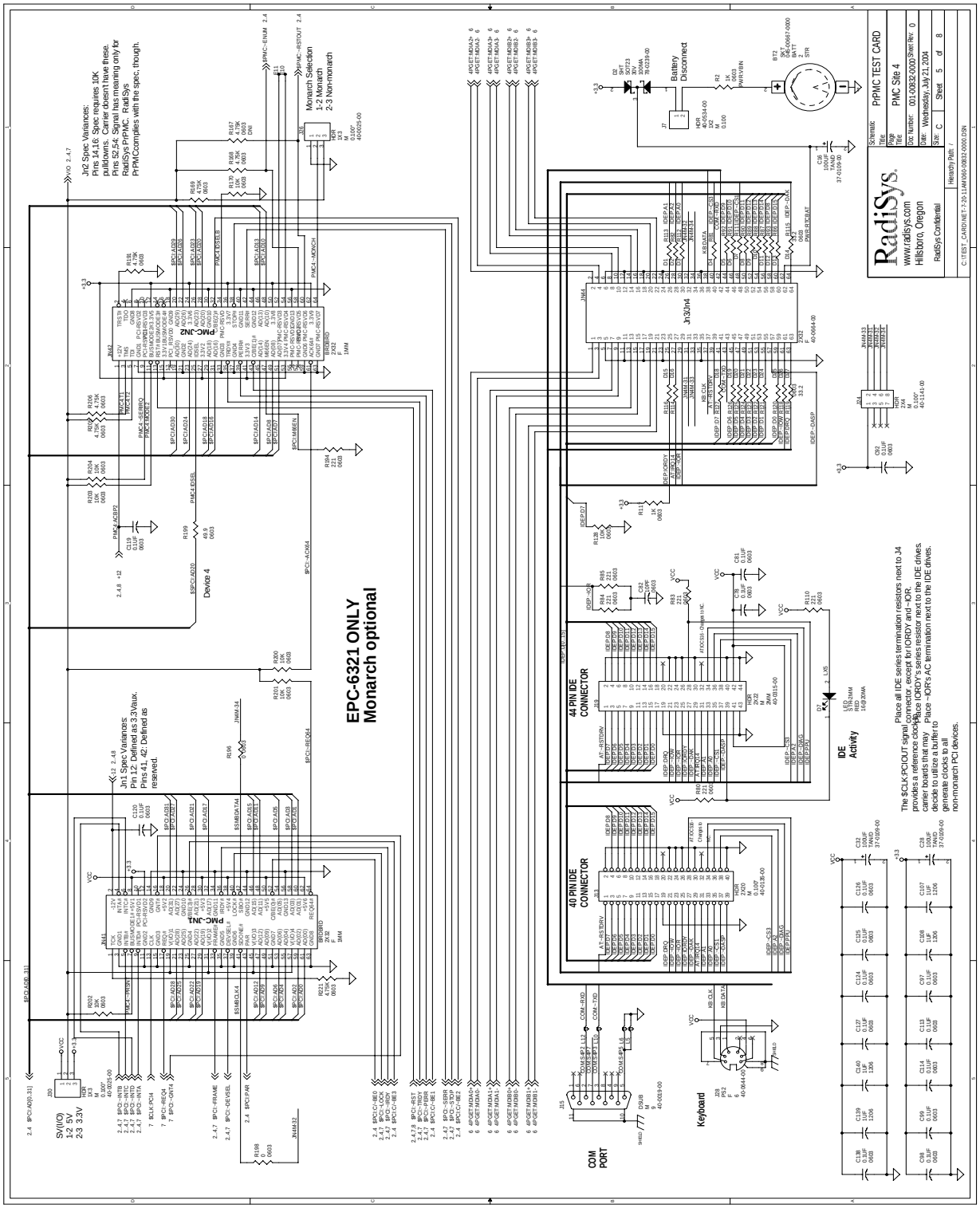
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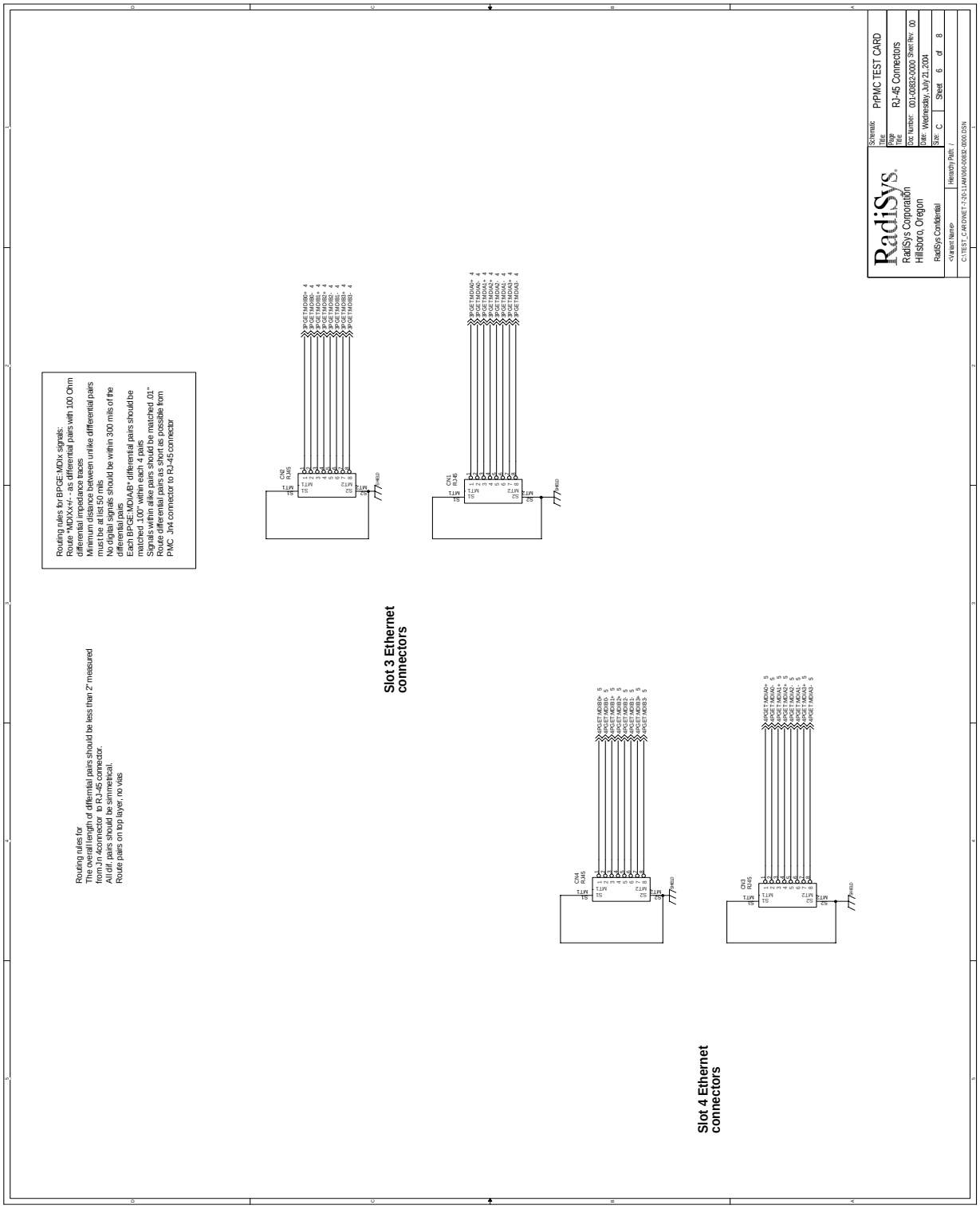
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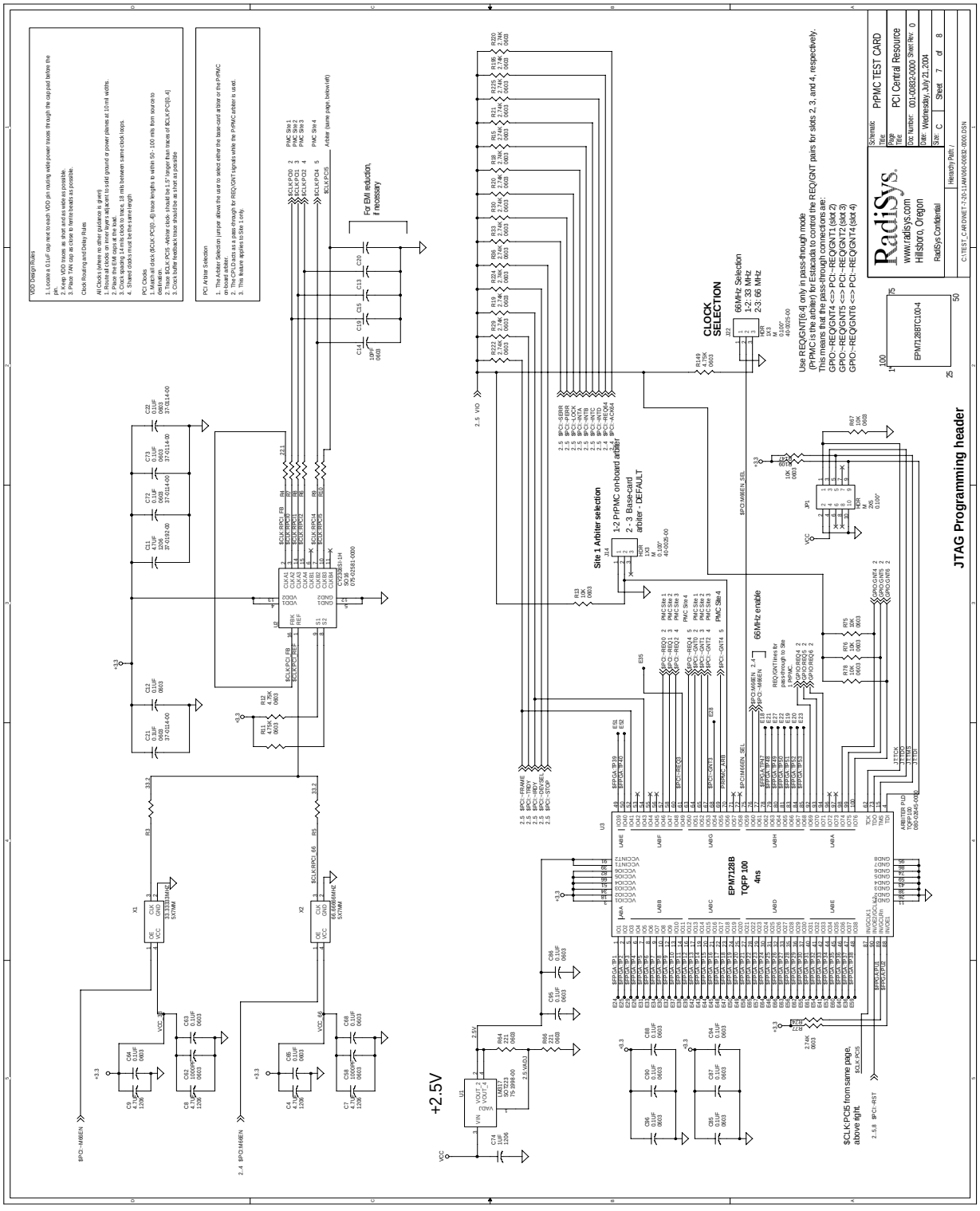
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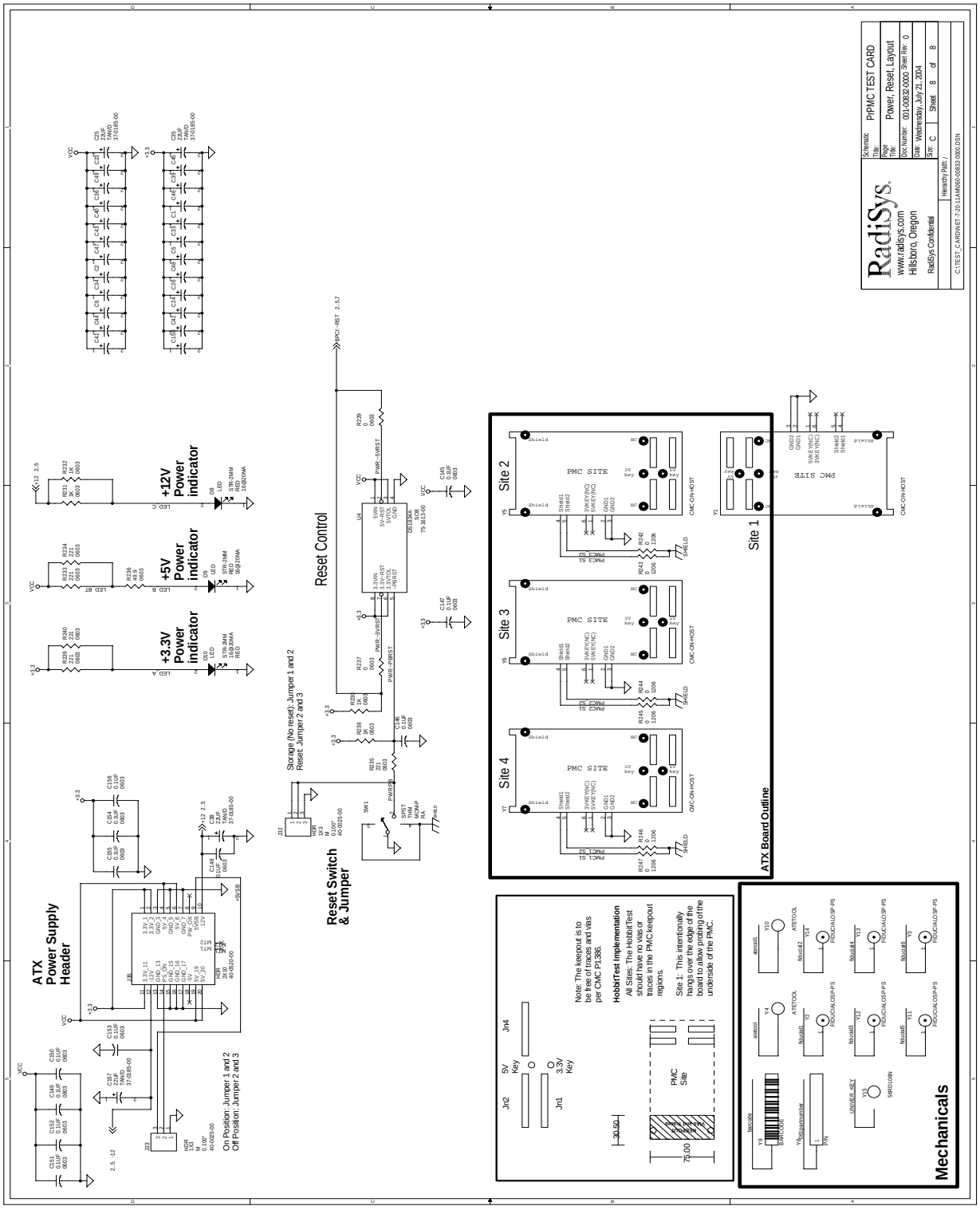
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H

EPC-6320/21 Test Board

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Physical Interfaces 85
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Interrrupts 86

The EPC-6320/21 test board (hereafter, Test Board) is a full ATX-sized, 4fourPMC site circuit board that you can use to begin production, test, and early development using the RadiSys EPC-6320/21 PrPMC.

This product assumes an intimate knowledge of the PrPMC specification, the standards governing other external interfaces to the PrPMC, and basic computer knowledge.

Features

Four 32-bit PMC sites with onboard arbitration, power reset, and clock selection of 33MHz or 66 MHz.

Feature	Description
Sites 1 and 2	• Clock speeds of 33MHz or 66MHz. • Monarch or non-Monarch site.[1] • Keyboard, mouse, serial port (DB9), IDE (40 and 44 pin), and battery interfaces via Jn4. • PMC standard Jn1, Jn2, and Jn4[1] connectors.
Site 3[2]	• Clock speeds of 33MHz or 66MHz. • Non-Monarch site. • PMC standard Jn1, Jn2, and Jn4[2] interfaces. • Battery, two Ethernet connectos KB, COM 3-pin (DB9) IDE
Site 4	• Clock speed of 33Hz or 66MHz. • Monarch or non-Monarch site. • Keyboard, 3-pin Serial Port (DB9), IDE (40 and 44 pin), and battery interfaces via Jn4. • PMC standard Jn1, Jn2, Jn4[2] (user definable) connectors.
ATX style power connector, power indicator LEDS and 3 pin power on/off jumper.	
Pushbutton and jumper resets.	

1 EPC-6320 only.

2 EPC-6321 only.

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External Interfaces

The Test Board, being a piece of lab equipment, has several connectors and jumpers available for use. The function of each connector is noted below.

Site(s)	No.	Connector
–	1	ATX power connector.
–	1	ATX 3-pin power on/off jumper.
1, 2, 3, 4	2 ea	Industry standard 40- and 44-pin IDE connectors.
3, 4	1 ea	DB9 3-pin interface.
1, 2	1 ea	DB9 serial port with full modem signals.
1, 2, 3, 4	2 ea	6-pin mini-DIN keyboard and mouse connectors.
1, 2, 3, 4	1	Battery in a socket (sites 1, 2, and 4).
–	2	3-pin jumpers for primary and secondary V I/O voltage selections (+5V or +3.3V).
–	1	3-pin jumper for clock speed selection (33MHz or 66MHz).
1, 4	2	3-pin jumpers for Monarch or non-Monarch selection.
–	1	Pushbutton switch and one three pin jumper for reset.
–	1	3-pin jumper for arbitration selection. **Note**: The only available arbitration selection is that the Test Board provides arbitration. If this presents a problem, contact RadiSys as described on *Where to get More Information* on page 2.

Specifications

The Test Board is not intended to meet any specific environmental specifications. As the board is typically used in an engineering lab environment where proper ESD procedures are followed, EMC is not considered an issue. It is assumed that the operating temperature is 20°C to 30°C, and humidity is 30% to 50%.

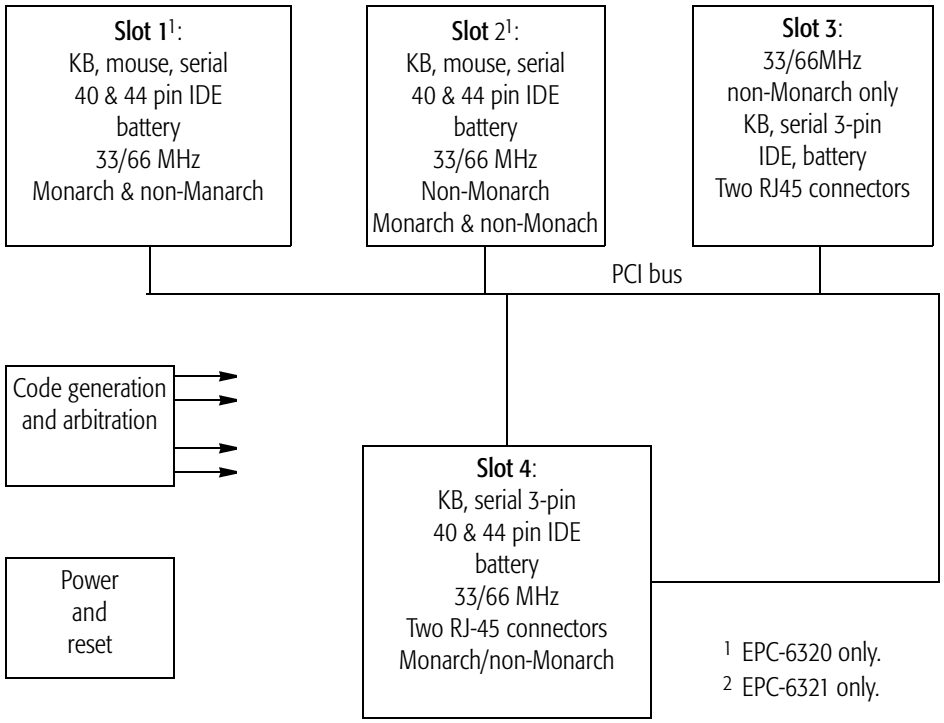
Table H-1. Environmental Specifications

Characteristic	Value
Dimensions	Full-size ATX board
Board thickness	2mm

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Block diagram

Figure H-1. Block Diagram: Test Board



Physical Interfaces

The keyboard, mouse, serial port, and IDE connectors are all common industry standard pinouts. The 3-pin interface is provided on Slots 3 and 4, and is used by DB9 connectors.

Connectors and Jumpers

The following table contains the list of all connectors and jumpers on the board and a description for each jumper.

Table H-2. Connector and Jumper Descriptions

Item	Description
J35	ATX power connector (industry standard pinout)
J33	ATX power on/off jumper (1–2 on, 2–3 off)
J11, J21, J12, J13	40 pin IDE connector (industry standard pinout)
J17, J20, J18, J19	44 pin IDE connector (industry standard pinout)
J1, J16, J2, J15	Serial port (industry standard pinout)
J4, J27	Mouse (industry standard pinout)
J5, J29, J3, J28	Keyboard (industry standard pinout)
J14	Artbiter select (us 2-3 base card)

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Table H-2. Connector and Jumper Descriptions

Item	Description
SW1	Pushbutton reset
JP1	(RadiSys only)
J30, J31	Reset (1–2 reset, 2–3 no reset)
J38	PCI bus V I/O (1–2 +5V, 2–3 +3.3V)
J22	PCI Bus clock select 1–2 33MHz, 2–3 66MHz
J9, J26	Monarch/non-Monarch selection (1–2 Monarch, 2–3 non-Monarch)

Reset Switch

SW1 is a reset pushbutton switch. Pressing it results in a reset of all PMC sites. Connecting pins 1 and 2 of J40 has the same effect.

Interrrupts

Table H-3. PCI Device Configuration

Peripheral	IDSEL	Bus	INT	Arbitration
Site1	AD28	0	A	0
Site 2	AD24	0	B	1
Site 3	AD30	0	C	2
Site 4	AD27	0	D	4

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Glossary

access time A factor in measurement of a memory storage device's operating speed. It is the amount of time required to perform a read operation. More specifically, it is the period of time between which the memory receives a read command signal and the time when the requested data becomes available to the system data bus.

address A number that identifies the location of a word in memory. Each word in a memory storage device or system has a unique address. Addresses are always specified as a binary number, although octal, hexadecimal, and decimal numbers are often used for convenience.

ANSI (American National Standards Institute) An organization dedicated to advancement of national standards related to product manufacturing.

APM 1.1 (Advanced Power Management) A software interface specification that allows operating system device drivers to control the power management functionality of a PC.

ATA (AT Bus Attachment) An interface definition for PC peripherals. See IDE.

autotype A convenient method of IDE device detection whereby the system BIOS queries the IDE device to obtain operational parameters. If the device supports autotype, this information is passed to the BIOS where it is used to automatically configure the drive controller.

BDA (BIOS Data Area) BIOS Data Area. A 256 byte block of DRAM starting at address 400H that contains data initialized and used by the System BIOS detailing the system configuration and errors encountered during POST.

BIOS (Basic Input/Output System) Firmware in a PC-compatible computer that runs when the computer is powered up. The BIOS initializes the computer hardware, allows the user to configure the hardware, boots the operating system, and provides standard mechanisms that the operating system can use to access the PC's peripheral devices.

BIOS extension An object code module that is typically integrated into the FBD or placed into a ROM that is accessible on the peripheral bus (PCI, ISA, etc.) in the address range 0C0000h through 0DFFFFh. BIOS extensions have a pre-defined header format and contain code that is used to extend the capabilities of the System BIOS.

BIOS image Information contained in the flash boot device in binary file format consisting of initialzation data, setup configuration data, diagnostic sequences, and other instructions necessary to start up a computer and prepare it to load an operating system.

BIOS recovery A process whereby an existing, corrupt BIOS image in the flash boot device is overwritten with a new image. Also referred to as a flash recovery. The {ProductNameShort} does not support this feature.

BIOS update A process whereby an existing, uncorrupted BIOS image in the flash boot device is overwritten with a new image. Also referred to as a flash update.

bit A binary digit.

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boot	The process of starting a computer and loading the operating system from a powered down state (cold boot) or after a computer reset (warm boot). Before the operating system loads, the computer performs a general hardware initialization and resets internal registers.
boot device	The storage device from which the computer boots the operating system.
boot sequence	The order in which a computer searches external storage devices for an operating system to boot. The boot device must be the first in the boot sequence.
byte	A group of 8 bits.
CAS	(Column Address Strobe) An input signal from the DRAM controller to an internal DRAM latch register specifying the column at which to read or write data. The DRAM requires a column address and a row address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of column addresses and row addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required.
chipset	One or more integrated circuits that, along with a CPU, memory, and other peripherals, implements an IBM PC-AT compatible computer. The chipset typically implements a DRAM controller, bus, interface logic, and PC peripheral devices.
CHS	(Cylinders/Heads/Sectors) A specification of disk drive operating parameters consisting of the number of disk cylinders, disk drive read/write heads, and disk sectors.
CMOS	(Complimentary Metal Oxide Semiconductor) A fast, low power semiconductor RAM used to store system configuration data.
COM port	A bi-directional serial communication port which implements the RS-232 specification.
conventional memory	The first 640 KB of a computer's total memory capacity. If a computer has no extended memory, conventional memory equals the total memory capacity. In typical computer systems, conventional memory can contain BIOS data, the operating system, applications, application data, and terminate and stay resident (TSR) programs. Also called system memory.
CPU	(Central Processing Unit) A semiconductor device which performs the processing of data in a computer. The CPU, also referred to as the microprocessor, consists of an arithmetic/logic unit to perform the data processing, and a control unit which provides timing and control signals necessary to execute instructions in a program.
CSR	(CMOS Save and Restore) A System BIOS feature that allows the user to backup the contents of CMOS RAM (contained within the real time clock) to the BIOS Flash device to be restored later if necessary (such as when the real time clock battery dies).
default	The state of all user-changeable hardware and software settings as they are originally configured before any changes are made.
DIP	(Dual In-Line Package) A semiconductor package configuration consisting of a rectangular plastic case with two rows of pins, one row on each lengthwise side.
DOS	(Disk Operating System) One or more programs which allow a computer to use a disk drive as an external storage device. These programs manage storage and retrieval of data to and from the disk and interpret commands from the computer operator.

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DRAM.	(Dynamic Random Access Memory) Semiconductor RAM memory devices in which the stored data does not remain permanently stored, even with the power applied, unless the data are periodically rewritten into memory during a refresh operation.
driver	A software component of the operating system which directs the computer interface with a hardware device. The software interface to the driver is standardized such that application software calling the driver requires no specific operational information about the hardware device.
ECP	(Extended Capabilities Port) An enhancement of the standard PC parallel port that allows high speed bi-directional data transfers and other features.
EDO	(Extended Data Out) A type of DRAM that allows higher memory system performance since the data pins are still driven when CAS# is de-asserted. This allows the next DRAM address to be presented to the device sooner than with Fast Page Mode DRAM.
EEPROM	(Electrically Erasable Programmable ROM) Specifically, those EPROMs which may be erased electrically as compared to other erasing methods.
error checking and correction	A feature of the T2 chipset that enables it to detect single or multi-bit errors in DRAM reads and correct single bit errors. This feature requires that all banks of DRAM use x36 (parity) SO DIMMs.
ESCD	(Extended System Configuration Data) A block of nonvolatile memory that stores information on the devices found and configured by the Plug and Play BIOS.
extended memory	The RAM address space, in a computer so equipped, above the 1 MB level.
external device	A peripheral or other device connected to the computer from an external location via an interface cable.
FBD	(Flash Boot Device) A flash memory device containing the computer's BIOS. In the {ProductNameShort}, a 4 MByte Intel 28F320J3A semiconductor flash memory containing the system BIOS images, the BIOS initializing code.
fixed disk	A hard disk drive or other data storage device having no removable storage medium. Fixed disk storage devices use inflexible disk media and are sealed to prevent data loss due to media surface contamination. Fixed disks generally provide the most storage space for a given cost when compared to semiconductor, tape, and other popular mass storage technologies.
Flash memory	A fast EEPROM semiconductor memory typically used to store firmware such as the computer BIOS. Flash memory also finds general application where a semiconductor non-volatile storage device is required.
Flash recovery	See BIOS recovery.
Flash update	See BIOS update.
Force update	See BIOS recovery.
FPGA	(Field Programmable Gate Array) A large, general-purpose logic device that is programmed at power-up to perform specific logic functions.
FPM	(Fast Page Mode) A "standard" type of DRAM that is lower performance than EDO.

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GB or GByte (Gigabyte) Approximately one billion (US) or one thousand million (Great Britain) bytes. 2^30 = 1,073,741,824 bytes exactly.

h (Hexadecimal) A base-16 numbering system using numeric symbols 0 through 9 plus alpha characters A, B, C, D, E, and F as the 16 digit symbols. Digits A through F are equivalent to the decimal values 10 through 15.

hang A condition where the system microprocessor suspends processing operations due to an anomaly in the data or an illegal instruction.

header A mechanical pin and sleeve style connector on a circuit board. The header may exist in either a male or female configuration. For example, a male header has a number and pattern of pins which corresponds to the number and pattern of sleeves on a female header plug.

host bus The address/data bus that connects the CPU and the chipset.

I/O (Input/Output) The communication interface between system components and between the system and connected peripherals.

IDE (Integrated Drive Electronics) A hard disk drive/controller interface standard. IDE drives contain the controller circuitry at the drive itself, as compared to the location of this circuitry on the computer motherboard in non-IDE systems. IDE drives typically connect to the system bus with a simple adapter card containing a minimum of on-board logic.

INT (Interrupt Request) A software-generated interrupt request.

IRDA or IrDA (Infra-red Data Association) A specification for high-speed data communication using infrared drivers and receivers for short-range wireless data transmission.

IRQ (Interrupt Request) In ISAbus systems, a microprocessor input from the control bus used by I/O devices to interrupt execution of the current program and cause the microprocessor to jump to a special program called the interrupt service routine. The microprocessor executes this special program, which normally involves servicing the interrupting device. When the interrupt service routine is completed, the microprocessor resumes execution of the program it was working on before the interruption occurred.

ISA (Industry Standard Architecture) A popular microcomputer expansion bus architecture standard. The ISA standard originated with the IBM PC when the system bus was expanded to accept peripheral cards.

ISR (Interrupt Service Routine) A program executed by the microprocessor upon receipt of an interrupt request from an I/O device and containing instructions for servicing of the device.

jumper A set of male connector pins on a circuit board over which can be placed coupling devices to electrically connect pairs of the pins. By electrically connecting different pins, a circuit board can be configured to function in predictable ways to suit different applications.

KB or KByte (Kilobyte) Approximately one thousand bytes. $2^{10} = 1024$ bytes exactly.

LBA (Logical Block Addressing) A method the system BIOS uses to reference hard disk data as logical blocks, with each block having a specific location on the disk. LBA differs from the CHS reference method in that the BIOS requires no information relating to disk

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	cylinders, heads, or sectors. LBA can be used only on hard disk drives designed to support it.
logical address	The memory-mapped location of a segment after application of the address offset to the physical address.
MB or MByte	(Megabyte) Approximately one million bytes. 2^20 = 1,048,576 bytes exactly.
memory	A designated system area to which data can be stored and from which data can be retrieved. A typical computer system has more than one memory area. See conventional memory and extended memory.
memory shadowing	Copying information from an extension ROM into DRAM and accessing it in this alternate memory location.
Monarch mode	A Processor PMC that acts as the main processing element. In this mode, the PPMC performs PCI bus enumeration at power-up and handles interrupts from devices requesting service. A system can have only one PPMC operating in Monarch mode. See non-Monarch mode.
non-Monarch mode	A secondary CPU that is not a main CPU, does not perform PCI bus enumeration, and may generate interrupts to the main CPU. A system can have as many non-Monarch PPMCs as the electrical interface capacity on the carrier card allows. See Monarch mode.
offset	The difference in location of memory-mapped data between the physical address and the logical address.
operating system	See DOS.
PAL	(Programmable Array Logic) A semiconductor programmable ROM which accepts customized logic gate programming to produce a desired sum-of-products output function.
PC/AT	(Personal Computer/Advanced Technology) A popular computer design first introduced by IBM in the early 1980s.
PCI	(Peripheral Connect Interface) A popular microcomputer bus architecture standard.
peripheral device	An external device connected to the system for the purpose of transferring data into or out of the system.
physical address	The address or location in memory where data is stored before it is moved as memory remapping occurs. The physical address is that which appears on the computer's address bus when the CPU requests data from a memory address. When remapping occurs, the data can be moved to a different memory location or logical address.
pinout	A diagram or table describing the location and function of pins on an electrical connector.
PMC	(PCI Mezzanine Card) A new standard form factor for PCI add-in modules. PMCs mate with their respective connectors on the motherboard and are secured with screws.
PLL	(Phase-Locked Loop) A semiconductor device which functions as an electronic feedback control system to maintain a closely regulated output frequency from an unregulated input frequency. The typical PLL consists of an internal phase comparator

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or detector, a low pass filter, and a voltage controlled oscillator which function together to capture and lock onto an input frequency. When locked onto the input frequency, the PLL can maintain a stable, regulated output frequency (within bounds) despite frequency variance at the input.

POST (Power On Self Test) A diagnostic routine which a computer runs at power up. Along with other testing functions, this comprehensive test initializes the system chipset and hardware, resets registers and flags, performs ROM checksums, and checks disk drive devices and the keyboard interface.

PQFP (Plastic Quad Flat Pack) A popular package design for integrated circuits of high complexity.

program A set of instructions a computer follows to perform specific functions relative to user need or system requirements. In a broad sense, a program is also referred to as a software application, which can actually contain many related, individual programs.

PS/2 (Personal System 2) Computers designed with IBM's proprietary bus architecture known as Micro Channel.

PSB Processor Side Bus.

RAM (Random Access Memory) Memory in which the actual physical location of a memory word has no effect on how long it takes to read from or write to that location. In other words, the access time is the same for any address in memory. Most semiconductor memories are RAM.

RAS (Row Address Strobe) An input signal to an internal DRAM latch register specifying the row at which to read or write data. The DRAM requires a row address and a column address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of row addresses and column addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required.

real mode The operational mode of Intelx86 CPUs that uses a segmented, offset memory addressing method. These CPUs can address 1 MB of memory using real mode.

real mode Address A memory address composed of two 16-bit values: a segment address and an offset quantity. A real mode address is constructed by shifting a segment address 4 bits to the left and then adding the offset value. A real mode address is a physical address.

reflashing The process of replacing a BIOS image, in binary format, in the flash boot device.

register An area typically inside the microprocessor where data, addresses, instruction codes, and information on the status on various microprocessor operations are stored. Different types of registers store different types of information.

reset A signal delivered to the microprocessor by the control bus, which causes a halt to internal processing and resets most CPU registers to 0. The CPU then jumps to a starting address vector to begin the boot process.

RFA (Resident Flash Array) The RFA represents flash memory that is resident on the hardware platform that is utilized for OS or application purposes.

ROM (Read Only Memory) A broad class of semiconductor memories designed for applications where the ratio of read operations to write operations is very high.

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	Technically, a ROM can be written to (programmed) only once, and this operation is normally performed at the factory. Thereafter, information can be read from the memory indefinitely.
RTC	(Real Time Clock) Peripheral circuitry on a computer motherboard which provides a nonvolatile time-of-day clock, an alarm, calendar, programmable interrupt, square wave generator, and a small amount of SRAM. In the NY1210, the RTC operates independently of the system PLL which generates the internal system clocks. The RTC is typically receives power from a small battery to retain the current time of day when the computer is powered down.
RS-232	A popular asynchronous bi-directional serial communication protocol. Among other things, the RS-232 standard defines the interface cabling and electrical characteristics, and the pin arrangement for cable connectors.
segment	A section or portion of addressable memory serving to hold code, data, stack, or other information allowing more efficient memory usage in a computer system. A segment is the portion of a real mode address which specifies the fixed base address to which the offset is applied.
serial port	A physical connection with a computer for the purpose of serial data exchange with a peripheral device. The port requires an I/O address, a dedicated IRQ line, and a name to identify the physical connection and establish serial communication between the computer and a connected hardware device. A serial port is often referred to as a COM port.
shadow memory	RAM in the address range 0xC000h through 0xFFFFFh used for shadowing. Shadowing is the process of copying BIOS extensions from ROM into DRAM for the purpose of faster CPU access to the extensions when the system requires frequent BIOS calls. Typically, system and video BIOS extensions are shadowed in DRAM to increase system performance.
SIMM	(Single In-Line Memory Module) A small, rectangular circuit board on which is mounted semiconductor memory ICs.
SODIMM	(Small Outline Dual Inline Memory Module) A new form factor for memory modules that is smaller and denser than SIMMs.
SRAM	(Static Random Access Memory) A semiconductor RAM device in which the data remains permanently stored as long as power is applied, without the need for periodically rewriting the data into memory.
standoff	A mechanical device, typically constructed of an electrically non-conductive material, used to fasten a circuit board to the bottom, top, or side of a protective enclosure.
symmetrically addressable SIMM	A SIMM, the memory content of which is configured as two independent banks. Each 16-bit wide bank contains an equal number of rows and columns and is independently addressable by the CPU via twin row address strobe registers in the DRAM controller.
SYSCLK	(ISAbus System Clock) The ~8.33MHz clock signal present on the ISAbus to which all bus transactions are synchronized.
system memory	See conventional memory.

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TB or TByte (Terabyte) Approximately one thousand billion (US) or one billion (Great Britain) bytes. 2^40 = 1,099,511,627,776 bytes exactly.

UED (User Editable Drive) A feature of the NY1210's Phoenix NuBIOS. When a "User" type hard disk drive setting shows in the IDE Adapter Sub-Menu the BIOS queries the hard disk drive for the purpose of retrieving disk geometry. If the hard disk drive is capable of providing this information, the BIOS uses it to automatically set up the drive for use with the system.

VESA (Video Electronics Standards Association) A group of hardware and software vendors that define specifications for hardware and software interfaces for a variety of devices.

VGA (Video Graphics Adapter) A popular PC graphics controller and display adapter standard developed by IBM. The standard specifies, among other things, the resolution capabilities of the display device. Display devices meeting the VGA standard must be capable of displaying a minimum resolution of 640 horizontal pixels by 480 vertical pixels with at least 16 screen colors.

wait wtate A period of one or more microprocessor clock pulses during which the CPU suspends processing while waiting for data to be transferred to or from the system data or address buses.

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