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EPC®-8

Hardware Reference

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07-0226-01 June 1995

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Chapter 1 - Product Description

Overview

The EPC-8 is a highly integrated PC-compatible computer designed specifically for use in the VMEbus and extended VMEbus (VXIbus) environments. It is compatible with all major PC software environments, including Microsoft DOS, Microsoft Windows 3.x, Microsoft Windows NT, and IBM OS/2, plus others.

It is available as either a one-slot or two-slot 6U VMEbus module. The two configurations are functionally identical, and differ only in that the two-slot module includes mechanical support for two EXM modules.

The PC-compatible portion of the architecture includes the following PC-standard features:

- Intel I486 DX2-50 or DX2-66 processor.
- 4, 8, or 16MB of 36-bit DRAM, using an industry standard 80-ns fast page mode 72 pin SIMM.
- Standard PC peripheral interfaces including an RS232 serial port and a bi-directional parallel port, all with standard interface connectors. The keyboard connector is PS/2 style, with an adapter included.
- All other standard PC architectural features, including an on-board speaker.
- RadiSys standard EXM expansion interface for adding PC-architecture peripherals or interfaces.

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- Phoenix BIOS with RadiSys enhancements to support the additional on-board features and VMEbus environment.

Additional features (some optional) include:

- SVGA interface. This local-bus interface is based on the Cirrus GD54xx chipset, with 512 Kbytes of video RAM providing local bus graphics performance and non-interlaced resolutions to 1024 x 768, with 16 colors. The standard 15-pin connector for this port is enhanced with a programmable output on pin 15, which is not connected on a standard VGA interface.

- 10-Base-T Ethernet interface. The interface is based on the National Semiconductor AT/LANTIC chip set, which provides emulation of Western Digital WD8013, Novell NE2000 and NE2000+ Ethernet controllers. Interface configuration (Emulation mode and address/interrupt control) is software controlled; a DOS-based application is provided to perform this operation.

- A second modified RS-422/485 PC-compatible serial port. This interface is implemented with RS-422/485 transmit and receive buffers. CTS, RTS, DSR and DTR are buffered to RS-422 levels. The Transmit lines are controlled by the RTS signal, providing RS-485 multidrop support.

- A watchdog timer. This device can be configured to generate a VMEbus SYSFAIL signal and reset the processor. The processor can be configured to reboot or halt. The timer is implemented as a software-retriggerable one-shot, with a programmable reset interval ranging from 125 mS to 8000 mS.

- The ability to boot from VMEbus memory or resident Flash memory.

- (optional) 128 Kbytes of battery-backed memory-mapped static RAM.

- (optional) 2 Mbytes of flash-EPROM based non-volatile memory. This memory can be protected against accidental overwriting by removing a shorting jumper. Software is available to support this in the DOS/Windows environment. This memory can also be configured as a bootable disk.

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VMEbus

The VMEbus implementation provides a complete bus interface with enhancements for multiprocessor environments. This is described in three sections covering the system controller functions, the VMEbus master interface, and VMEbus extended register set.

System controller functions

A single hardware configuration jumper allows the EPC-8 to provide full VME slot-1 arbitration functions. When enabled, the functions provided include priority and round-robin bus arbitration, IACK and bus grant daisy-chain driving, SYSRESET and SYSCLK generation and bus time-out detection. ROR (release-on-request) or a fair-requester, RONR (release-on-no-request) bus release mechanism is software selectable.

VMEbus master interface

The VMEbus master interface provides a full 32-bit data path to the 16, 24, and 32-bit address spaces of the VMEbus. The bus interface is designed with a minimum number of state registers, which maximizes performance in a multitasking or interrupt driven environment.

Programmable hardware byte-swapping is provided for ease of communication with other processor architectures that may share the VMEbus. All the VMEbus address spaces can be addressed from both protected-mode and real-mode operating systems.

The EPC-8 can generate or respond to all 7 standard VMEbus interrupts, and can also receive the VMEbus signals ACFail, BERR, and Sysfail as interrupts. When it is used to generate interrupts, it implements 16-bit IACK cycles.

VMEbus extended register set

As an extension to the VMEbus interface, the EPC-8 implements the set of VXIbus (IEEE 1155-1992) standard multiprocessor support registers in the A16 space.

These registers provide a set of standard identification, status, control and communication functions that are useful in multiprocessor environments. They allow dynamic system configuration by providing for board identification, and provide well-defined multi-processor communications channels and protocols.

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The EPC-8 includes a complete set of VXIbus-defined message-based device registers. These registers, implemented in a proprietary gate array and mapped into the VMEbus A16 address space, include a device-type identifier register (supporting geographic addressing), bus status and control registers, and a register-based message passing facility.

Specifications

The following are the environmental specifications for the EPC-8.

Characteristic		Value
Temperature	operating	0°C - 65°C at point of entry of forced air derated 2°C per 1000 ft (300 m) over 6600 ft (2000m) 2°C per hour max excursion gradient
	storage	-40°C - 85°C 5°C per hour max excursion gradient
Humidity	operating	5% - 95% noncondensing
	storage	5% - 95% noncondensing
Altitude	operating	0 - 10,000 ft (3000 m)
	storage	0 - 40,000 ft (12,000 m)
Vibration	operating	0.015 inch (0.38 mm) P-P displacement with 2.5 g peak (max) acceleration over 5-300 Hz
	storage	0.030 inch (0.76 mm) P-P displacement with 5.0 g peak (max) acceleration over 5-300 Hz
Shock	operating	30 g, 11 mS duration, half-sine shock pulse
	storage	50 g, 11 mS duration, half-sine shock pulse
Airflow		12 Liters/sec. for the two-slot module 6 Liters/sec. for the one-slot module

Table 1-1. EPC-8 Environmental Specifications.

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The following table contains additional specifications.

Characteristic		Value
Electrical		
Current	+5V	4.0A typical
	+12V	0.2A typical
	-12V	0.2A typical
Other		
Weight	without EXMs	2.7 lb. (1.3 kg)
VME	master address	A16, A24, A32
	master transfer	D08(EO), D16, D32, RMW
	slave address	A16
	slave transfer	D08(EO), D16, RMW
	interrupter	I(1-7)
	interrupt handler	D08(O),D16 IH(1-7)
	requester	ROR, RONR
	arbiter	RRS, PRI
	system controller	SYSCLK, IACK and bus grant daisy chains, bus time-out error (BERR)
VXI	device type	message based
	protocols	commander/master/interrupter
	manufacturer code	4076 - RadiSys Corporation
	model code	196 (if configured for slot 0) 452 (if configured for other than slot 0)

Table 1-2. Additional EPC-8 Specifications.

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Chapter 2 - Configuration and Installation

2 2

In order to configure and install the EPC-8, the following steps must be completed:

1. Set jumpers as needed for Flash, BIOS, and Slot-1
2. Select the slot location
3. Install VMEbus backplane jumpers
4. Insert subplane into mainframe
5. Insert EPC-8 into mainframe
6. Connect peripherals
7. Power-up
8. Configure BIOS
9. Boot operating system
10. Install software/configure system

Unpack the EPC-8 and inspect it for shipping damage.

✉ **DO NOT REMOVE THE EPC-8 MODULE FROM ITS ANTI-STATIC BAG UNLESS YOU ARE IN A STATIC-FREE ENVIRONMENT.**

The EPC-8, like most electronic devices, is susceptible to electrostatic discharge (ESD) damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

✉ **DURING ALL OF THIS INSTALLATION PROCESS, MAKE SURE THAT POWER TO YOUR SYSTEM IS OFF.**

The EPC-8 is not designed to be inserted or removed while the chassis is powered up.

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2 2

Configuring the EPC-8

Slot-1 Functionality

Every VMEbus system must have a System (Slot-1) Controller. The Slot-1 controller provides the following functionality:

- Serves as the bus arbiter (priority or round-robin)
- Drives the 16 MHz SYSCLK signal
- Starts the IACK and bus grant daisy chains.
- Provides bus timeout error (BERR) function

The EPC-8 can be user-configured to provide standard VMEbus Slot-1 functionality. The Slot-1 configuration option is enabled (default) by installing the Slot-1 shunt (jumper) on the processor board (see Figure 2-1). Removing the jumper disables Slot-1 functionality. When the EPC-8 is configured as the Slot-1 controller, it performs all the standard VMEbus system control functions.

Jumpers JP2 and JP3 are reserved for use by RadiSys and should not be installed.

The BIOS Jumper (JP4) enables the BIOS Flash memory for writing. This should not be installed except in the rare instance when the BIOS is being upgraded.

The Flash Jumper (JP5) enables the resident Flash memory for writing and must be installed when using software such as the **XFORMAT** utility.

The Recovery Jumper (JP6) must be installed only in order to recover a corrupted BIOS -- for example, if the power source was interrupted during a BIOS upgrade, and the corrupt BIOS can only be reflashed using the serial port connection to another computer.

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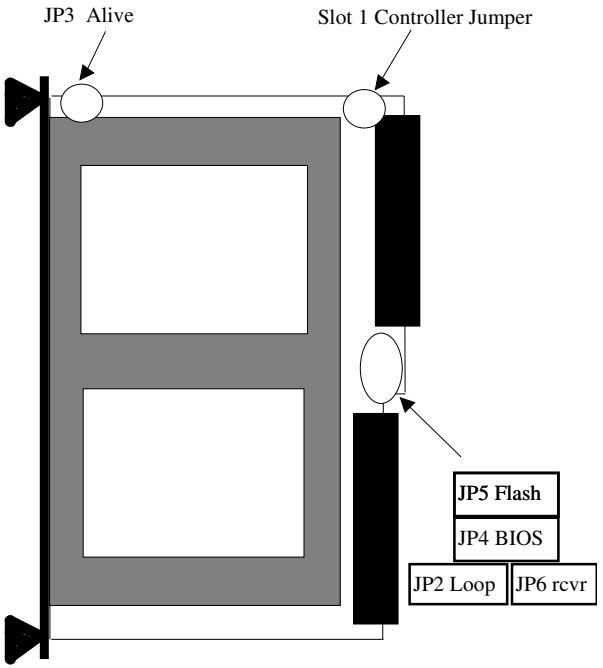


Figure 2-1. Jumper Locations.

Selecting the EPC-8 Slot Location

There are two main considerations in determining where the EPC-8 should be positioned in the chassis.

- Per the VMEbus specification (Rule 3.3), the Slot-1 controller must be in Slot 1. All other boards must be to the right of the Slot-1 controller.
- The EPC-8 connects to its peripherals via a subplane which extends to the right of the EPC-8. Make sure that the location you choose provides sufficient room for all the attached peripherals (EXMs and mass storage module).

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2 2

The EPC-8 plus EXM expansion modules plus any mass storage module can be considered together as a single subsystem. Use the following worksheet in Table 2-1 to determine the total number of VME slots your particular subsystem configuration requires.

Product	VME Slots	Total
Double-slot EPC-8 (Includes first two EXM modules)	2	
Additional EXP-MC(s) (Holds additional two EXM modules)	1 each	
EXP-AM	2	
Mass Storage Module (EXP-MX)	2	
Total VMEbus slots used		

Table 2-1. VME Slots Available.

Once you have determined where the EPC-8 subsystem will be physically located in the chassis, the VME backplane must be jumpered appropriately.

Installing the VMEbus Backplane Jumpers

The VMEbus propagates four bus grant signals (`BG0 - BG3`) and one interrupt acknowledge signal (`IACK`) via daisy-chain lines. Per the VMEbus specifications, all boards (that plug into the backplane) are required to correctly handle these signals. All slots that do not have a board plugged into the backplane (i.e. empty slots and slots occupied by EXMs or mass storage modules), need to be jumpered to allow the signals to pass through to other boards in the system.

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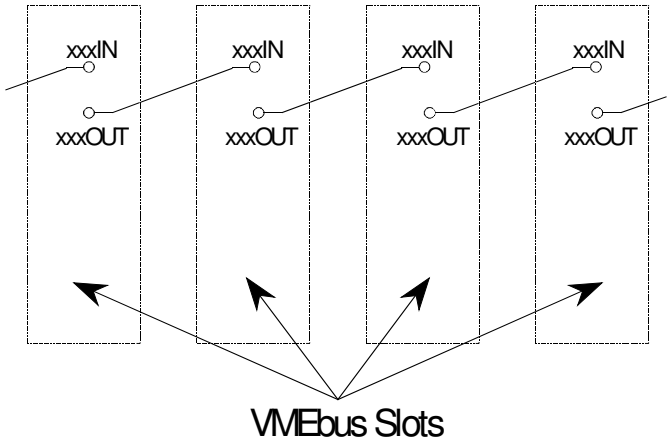


Figure 2-2. Daisy-Chain Signal Concept.

The daisy-chain signal concept is shown in Figure 2-2. The Slot-1 controller board initiates each daisy-chain signal. Each VMEbus slot to the right of the Slot-1 controller must pass through each of the daisy-chain signals. For each VMEbus slot, `xxxIn` pin must be connected to its corresponding `xxxOut` pin (e.g. `BG0In` to `BG0Out`, `BG1In` to `BG1Out`,...,`IackIn` to `IackOut`) either through the board in that slot or by jumpers. (Boards that meet VMEbus specifications correctly handle the signals and do not need backplane jumpers. However, many early designs may not propagate these signals correctly.) may not handle any of these signals. Check the manual for each board to be installed to determine if these signals are passed through correctly. If they are not, or if the VMEbus slot is empty, all (or some) of these signals must be jumpered. See Figures 2-3 and 2-4 on the following pages for examples.

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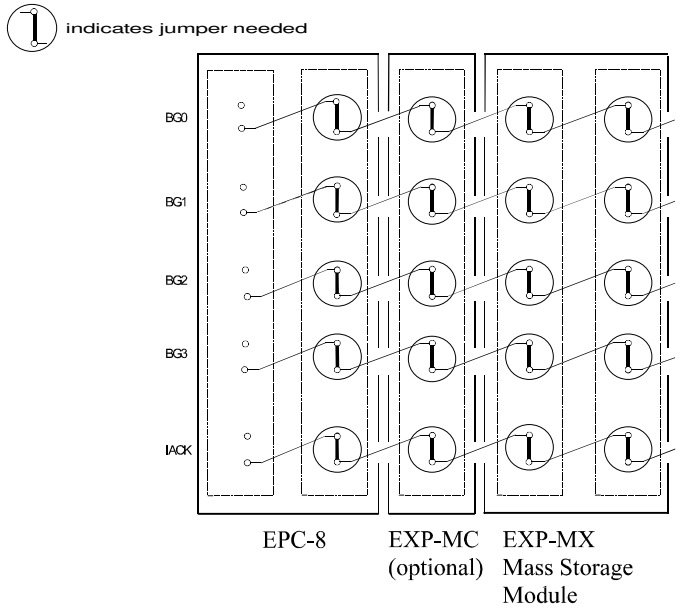


Figure 2-3. Backplane Jumpers Required for EPC-8 Subsystem.

The figure above shows the jumpers required for a five-slot EPC-8 subsystem, consisting of a two-slot EPC-8, an EXP-MC module carrier for two additional EXM modules, and an EXP-MX storage module. Note that the left-most slot does not require any jumpers. All other slots occupied by the subsystem require all five jumpers be installed.

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Once you have determined where the jumpers need to be, you must determine how to jumper your particular backplane. Different backplane manufacturers handle this in different ways; some provide stake pins on the rear of the backplane while others provide stake pins on the front of the backplane. These stake pins can be located in several different places.

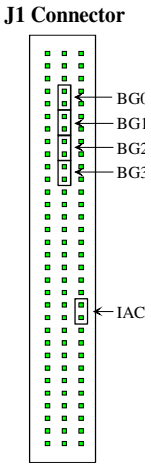


Figure 2-4. VMEbus Jumpers on Rear Wirewrap Pins.

If the stake pins are on the rear of the backplane, the most common location is in the middle of the J1 connector as shown in Figure 2-4. The connector may have wire-wrap tails on all pins, or just on the bus-grant and IAC pins.

Stake pins (front or rear) can also be located adjacent to the slot being jumpered as shown in Figure 2-5. Typically, the stake pins are located between the slot being jumpered and the next lower-numbered slot (e.g. jumpers for Slot 6 would be located adjacent to Slot 6 between Slots 5 and 6).

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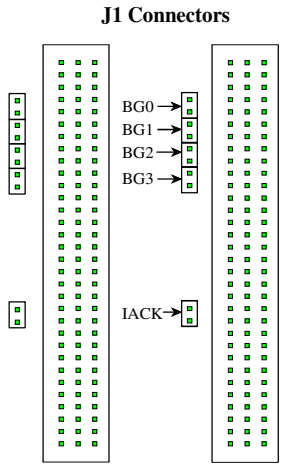


Figure 2-5. VMEbus Jumpers on Front Stake Pins.

Consult your VME chassis reference manual or contact the chassis manufacturer if you are unsure where to jumper your particular system.

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EPC-8 Insertion

The EPC-8 must be installed onto a subplane that fits between the EPC-8 and the VMEbus backplane. Subplanes are discussed in more detail in Appendix E.

The subplane is installed first, connecting to the backplane. After installing the subplane, the EPC-8 processor module can be inserted into the VMEbus chassis.

✉ **MAKE SURE THAT POWER TO YOUR VME SYSTEM IS OFF. THE EPC-8 MODULE IS NOT DESIGNED TO BE INSERTED OR REMOVED FROM LIVE BACKPLANES.**

✉ **WHEN INSERTING THE EPC-8 MODULE, AVOID TOUCHING THE CIRCUIT BOARD AND CONNECTOR PINS, AND MAKE SURE THE ENVIRONMENT IS STATIC-FREE.**

√ Make sure the ejector handles are in the normal (non-eject) position. (Push the top handle down and the bottom handle up so that the handles are not tilted.)

√ Slide the EPC-8 module into the left-most slot occupied by the subplane. Use firm pressure on the handles to mate the module with the connectors.

√ Tighten the retaining screws in the top and bottom of the front panel to ensure proper connector mating and prevent loosening of the module due to vibration.

Connecting Peripherals to the EPC-8

WARNING!

DO NOT PLUG IN ANY CABLE OR CONNECTOR INTO THE FRONT PANEL CONNECTORS WHILE THE SYSTEM IS POWERED UP. IN GENERAL, ELECTRONICS EQUIPMENT IS NOT DESIGNED TO WITHSTAND POTENTIAL DAMAGE THAT COULD ARISE FROM FLUCTUATIONS IN POWER. **NEVER** PLUG IN A SERIAL OR PARALLEL DEVICE, KEYBOARD, TRANSCEIVER, MONITOR OR OTHER COMPONENT WHILE THE SYSTEM IS ON.

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The next step of installation is connecting peripherals, typically a video display and keyboard, but also perhaps a mouse, modem, printer, etc. Pin-outs for the EPC-8 front-panel connectors are specified in Appendix C, *Connectors*.

2 2

Remaining Steps

The remaining configuration steps may include BIOS configuration, driver software installation and application software installation. Your system may be preconfigured by your supplier or you may be required to perform these tasks yourself.

Chapter 3 of this manual describes the BIOS set up program. Many of the hardware setups are accomplished using the BIOS.

Other features of the EPC-8, such as the Ethernet port, graphics controller, and optional Flash memory require drivers and are configured using DOS programs or specific operating system functions and utilities. Installation of other software drivers that are optionally available with the EPC-8 is described in the appropriate sections of this manual. These include the following:

- a resident Flash memory utility *(Appendix G - XFORMAT)*
- an Ethernet configuration utility (*Appendix H - AUTOSET)*
- SVGA display drivers *(Appendix I - SVGA).*
- Ethernet drivers *(Appendix K - Configuring the Ethernet Drivers)*

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Chapter 3 - BIOS Configuration

3 3

Introduction

The EPC-8 uses the Phoenix BIOS to configure and select various system options. This section details the various menus and sub-menus that are used to configure the system. While the section is written as though you are encountering each field in sequence and for the first time, your system may be pre-configured and require very little intervention.

Some error messages might occur during the execution of the BIOS initialization sequence. If errors occur during the power-on self-test (POST), the BIOS will display the error on the appropriate line of the screen display and, depending on how your system is configured, will either pause or attempt to continue. Refer to Appendix J - *Error Messages & Diagnosis.*

BIOS Setup Screens

The EPC-8's BIOS contains a setup function to display and alter the system configuration. This information is maintained in the EPC-8's nonvolatile CMOS RAM and is used by the BIOS to initialize the EPC-8 hardware.

The BIOS Setup can only be entered during the system reset process, following a power-up, front panel reset, or equivalent. Press the F2 key when prompted to enter Setup.

NOTE: The prompt to press the F2 key to enter the BIOS setup can optionally be suppressed in the BIOS setup. However, you can still press the F2 key to enter the BIOS setup screens, even if the prompt is suppressed.

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Use the up and down cursor (arrow) keys to move from field to field. Use the right and left arrows to move from menu to menu, as noted in the menu bar at the top of the screen. If you use the arrow keys to leave a menu and then return, your active field is always at the beginning of the menu. If you select a sub-menu and then return to the main menu, you return to that sub-menu heading.

Fields with a triangle to the left are actually sub-menu headings; press Enter when the cursor rests on one of these headings to reach that sub-menu. For most fields, position the cursor at the field and from the numeric keypad, press the + and - keys to rotate through the available choices. Certain numeric fields can also be entered via the keyboard. Once the entry has been changed to appear as desired, use the up and down arrow to move to the next field.

3 3

Main BIOS Setup Menu

The main BIOS setup menu is shown below:

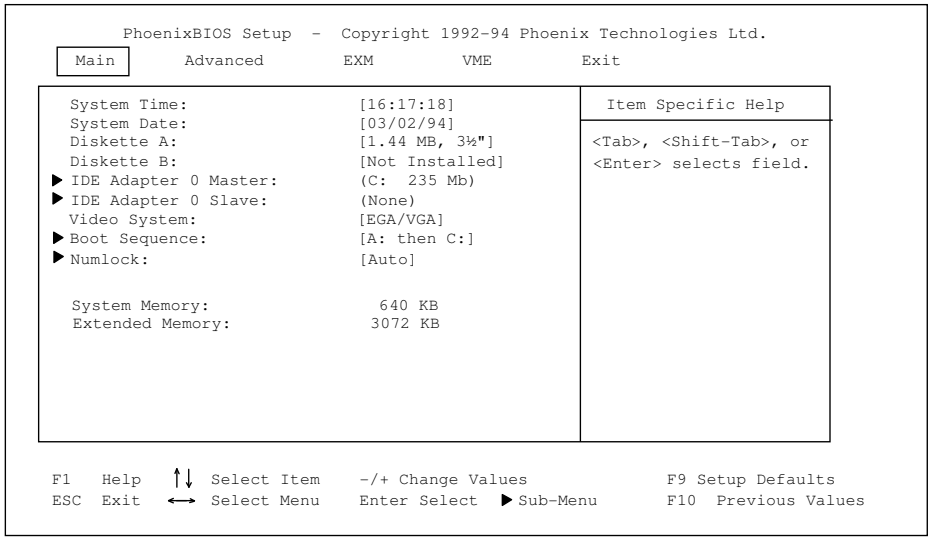


Figure 3-1. Main Menu.

The far right menu in the menu bar is the Exit Menu. Use the options in this menu to save your changes, re-load default BIOS settings, etc. By pressing the ESC key, you jump immediately to the Exit Menu.

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The fields in each menu and sub-menu are explained below. Additional help information is available in the help area on the BIOS setup screen.

System Time:/System Date:

These values are changed by moving to each field and typing in the desired entry. Use the tab key to move from hour to minute to second, or month to day to year.

Diskette A:/Diskette B:

This field identifies the type of floppy disk drive installed as the A drive. If the EPC-8 has a floppy drive installed, the proper setting is usually for a 1.44 MB floppy disk drive. Other options include 360K, 720K, 1.2 Mbyte, and 2.88 Mbytes. If no drive is installed, the proper setting is NOT INSTALLED.

IDE Adapter 0 Master/Slave Sub-Menus:

These fields are headings for menus that allow you to enter complete disk drive information. Once the information is entered for the drive, the entry in the Main Menu shows the drive selected. For more information, turn to the section concerning the IDE Adapter Menus.

Video System

Use this field to select among the different video options available. Select from EGA/VGA, CGA 80x25, or monochrome. The EPC-8's onboard video is VGA.

Boot Sequence Sub-Menu

The Boot Sequence Sub-Menu allows you to change the boot delay, boot sequence, and disable several displays during the boot process, such as the SETUP prompt, POST errors, floppy drive check, and summary screen. Once you have set the boot sequence, your choice displays in this entry in the Main menu. For more information, turn to the section concerning the Boot Sequence Sub-Menu.

Keyboard Features (Numlock) Sub-Menu

Use this menu to enable or disable various keyboard features, including enabling the Numlock key, enabling the key click, and setting the keyboard auto-repeat rate and delay. The Numlock setting displays for this entry in the Main Menu. For more information, turn to the section concerning the Keyboard Features Sub- Menu.

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There are two more lines on the Main BIOS Setup Screen: "System Memory" and "Extended Memory." These are display-only fields set by the BIOS. No user interaction is required.

IDE Adapter Sub-Menus

There are two IDE adapter sub-menus: one for the master drive and one for the slave drive. To use an EXM-HD, EXM-MX, or EXP-MX series mass storage unit, you must configure a master adapter; the slave is optional, and not relevant to most RadiSys hardware. To see the detailed characteristics of the device or to change the device, choose the IDE Adapter 0 Master Sub-Menu to configure the fixed disk. The following screen displays:

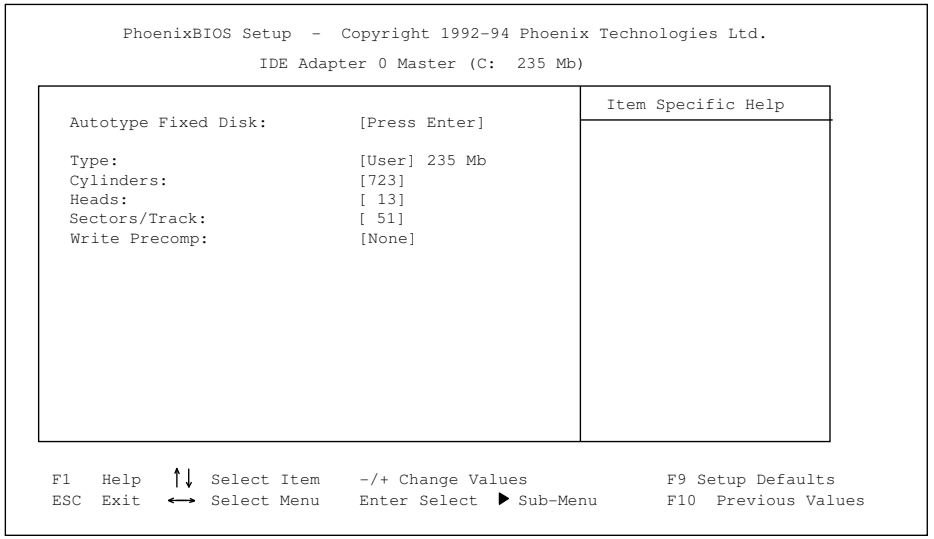


Figure 3-2. IDE Adapter Sub-Menu.

Autotype Fixed Disk

Use this option when setting up new disks. This option allows the BIOS to determine the proper settings of the disk based on information on the disk, which is detected by the EPC-8 BIOS for drives that comply with ANSI specifications. Use the ENTER key to invoke this function.

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Existing (formatted) disks must be set up using the same parameters that were used originally when the disk was formatted. You must enter the specific cylinder, head, sector information as listed on the label attached to the drive at the factory. Use the "User" type described below.

Type

For the majority of users who are using a system that was pre-configured, you probably have an IDE hard disk drive. Select "None" if you are not using an IDE hard disk drive. In the case for which you have an IDE disk but cannot employ the "Autotype" feature, then select "User" for the Type and enter the correct drive values for cylinders, heads, sectors/track, and write precomp from the label attached by RadiSys at the factory. For disks not supplied by RadiSys, consult the product's documentation.

Note that there are some restrictions when setting up devices on the EPC-8. If you plan to boot from a non-IDE device, such as the resident Flash memory or VMEbus, set the C: drive as None and use the BIOS extension. Flash and VMEbus BIOS extensions are enabled and configured in the Advanced Menu.

Once you have completed the setup for the IDE Master, you can choose the IDE Adapter 0 Slave Sub-menu to configure your second drive. When finished, press the ESC key to return to the Main Menu.

Boot Sequence Sub-Menu

The Boot Sequence Sub-Menu allows you to change the boot sequence options. The following displays:

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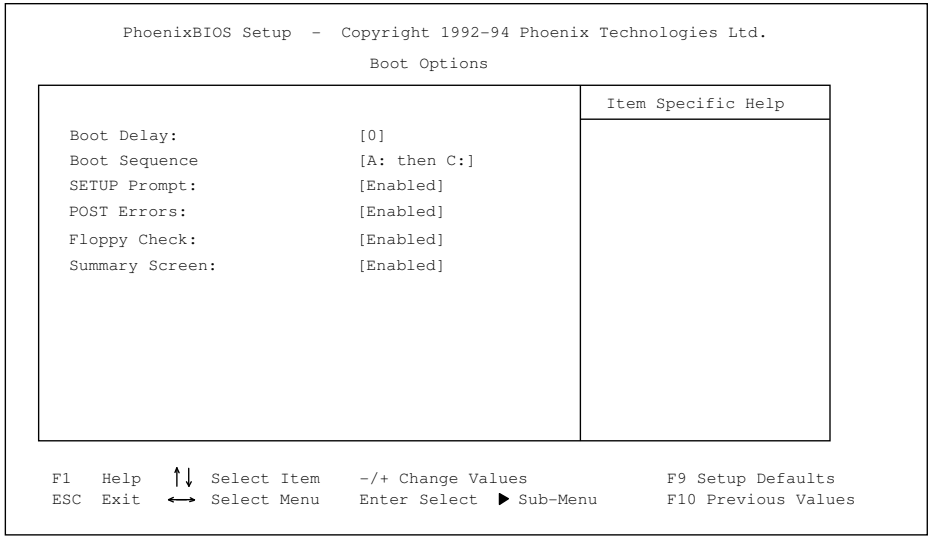


Figure 3-3. Boot Sequence Sub-Menu.

Boot Delay:

Use this option to set the system to delay booting for a time period in seconds that you set. This allows for long start up times on boot devices that spin up slowly. The default is zero.

Boot Sequence:

Use this option to define how the system treats floppy drive A: when booting. You can boot from a floppy in the A: drive or boot directly from the fixed disk drive. To reduce the amount of time required to boot, set the boot sequence to use the **C: drive only**. Note that the C: drive may be an IDE drive, Flash memory, a disk image on the VMEbus, or a SCSI drive. The options are as follows:

1. **A: then C:** Used to boot from the floppy disk drive, or if no floppy is present in the A: drive, boot from the C: drive.

2. **C: then A:** Used to boot from the C: drive, whether Flash or IDE, or if none is present, boot from the A: drive.

3. **C: only** Used to boot from the C: drive without searching for an A: drive.

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The default is C: then A:. The setting chosen here displays in the Boot Sequence Sub-Menu prompt.

About Drive Letter Assignment

The BIOS determines the boot device algorithmically. First it determines where the floppy drive fits into the sequence; however, for simplicity here, assume no A: drive. The BIOS starts by determining if an IDE controller is enabled. If so, this becomes the C: drive and is expected to be the boot device.

The BIOS searches memory for enabled mass-storage devices, and builds a device table. The first device it finds will be the C: drive, and thus the boot device. The second device found will be the D: drive; only two physical drives are supported.

If an IDE drive is specified in the BIOS setup, it becomes the C: drive. Next, the BIOS looks for BIOS extensions at addresses C8000, CC000, D000, D4000, D8000 and DC000 for more devices, up to the maximum of two.

There are many different boot options. Two supported directly on the EPC-8 hardware and BIOS are booting from a Flash ROMdisk and booting from a VME ROM disk. For more information on booting from a VME ROMdisk or a Flash ROMdisk, refer to setups in the Advanced Menu and Appendix G, **XFORMAT** Software.

Setup Prompt:

Use this option to enable or disable the message "Press F2 to enter Setup." Even if the message is disabled, you can still press F2 to enter the Setup Menu. The default is to enable this prompt.

POST Errors:

Use this option to stop during the boot if the system encounters error messages. Otherwise, the system will continue to attempt to boot despite any startup error messages that display. The default is to enable this option.

Floppy Check:

Use this option to enable or disable the floppy drive search during the boot. To speed up booting, you can disable the floppy check. It is still possible to boot from the A: drive even with the floppy check disabled. The default is to enable the floppy check.

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Summary Screen:

Use this option to enable or disable a summary of the system configuration, which displays before the operating system starts to load. To save time, you can disable the summary screen. The default is to enable the summary screen display.

When you have completed the Boot Options Menu, exit back to the Main BIOS Setup Menu using the ESC key and complete the Keyboard Features Sub-Menu.

Keyboard Features Menu

Use this sub-menu to enable or disable various keyboard features.

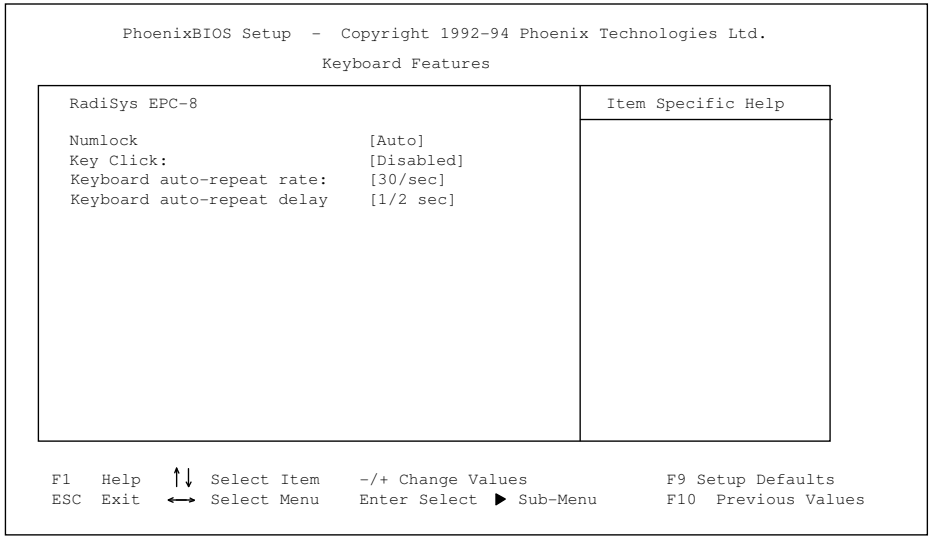


Figure 3-4. Keyboard Features Sub-Menu.

Numlock

Use this option to enable or disable the Numlock feature of the keyboard. This enables the use of the keypad numbers. The default is to automatically engage the Numlock key at boot-up.

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Key Click

Use this option to enable or disable the key click feature on the keyboard. If enabled, the keyboard produces an audible click each time a key is pressed.

Keyboard auto-repeat rate:

Use this option to set the auto-repeat rate if holding a key down on the keyboard. The rates are from 2-30 per second.

Keyboard auto-repeat delay:

Use this option to set the delay between when a key is pressed and when the auto-repeat feature begins. Options are 1/4, 1/2, 3/4, and one second.

When you are finished with this menu, press ESC to exit back to the main BIOS Setup Menu.

Advanced Menu

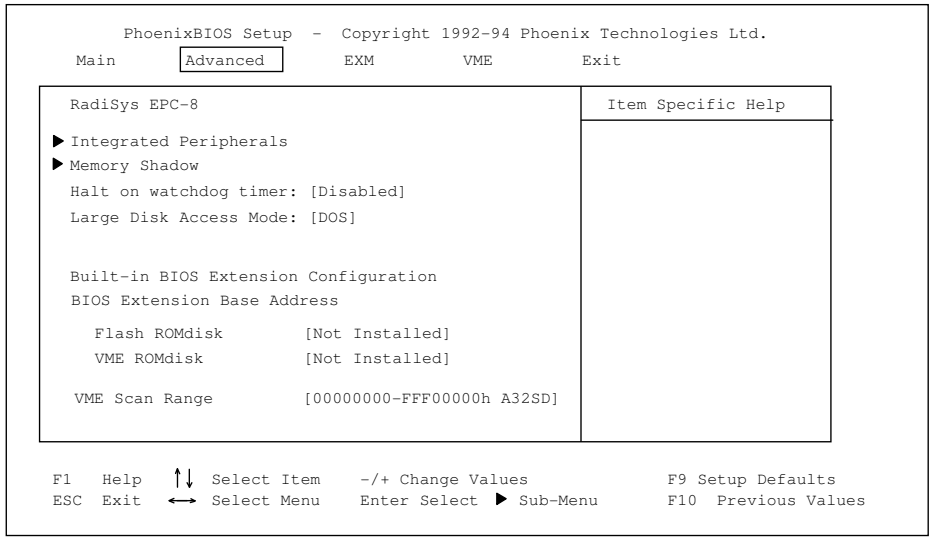


Figure 3-5. Advanced Menu.

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The Advanced Menu contains settings for integrated peripherals, memory shadow, watchdog timer, large disk access mode, and setting the Flash and VME ROMdisk BIOS extension base addresses.

Integrated Peripherals Sub-Menu

Use this option to select the Integrated peripherals sub-menu, in order to configure the COM and LPT ports. This does not configure Ethernet, video, or Flash memory. For more information, turn to the section concerning the Integrated Peripherals Sub-Menu.

Memory Shadow Sub-Menu

The term "Memory Shadow" refers to the technique of copying information from ROM into RAM and accessing it in this alternate memory location. For more information, turn to the section concerning the Memory Shadow Sub-Menu.

Halt on watchdog timer:

This sets the action for the BIOS to take following a hardware reset condition caused by a timeout of the watchdog timer on the EPC-8. When such a timeout occurs, first the system generates a VMEbus SYSRESET. The EPC-8 will then either halt, displaying an error message, or will simply reboot, depending on the entry here.

Large Disk Access Mode:

If using a drive larger than 512 Mbytes, set this to DOS if you are running DOS, or set this to Other if using a different operating system.

Built-in BIOS Extension Configuration
BIOS Extension Base Address
Flash ROMdisk:

Use this option to enable Flash memory on the EPC-8. This must be selected for the Flash memory to appear as a drive. The base address you select defines where the Flash ROMdisk BIOS extension is installed.

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Options are the following:

DC000-DFFF0h
D8000-DBFF0h
D4000-D7FF0h
D0000-D3FF0h
CC000-CFFF0h
C8000-CBFFFh
Not Installed

An important implication is that you cannot have an IDE drive if the resident Flash memory is the boot device. For more information, refer to "*About Drive Letter Assignment*" on page 3-7.

VME ROMdisk:

Use this option to enable VME memory on the EPC-8. This must be selected for the VME memory to appear as a drive. The base address you select defines where the VME ROMdisk BIOS extension is installed.

DC000-DFFF0h
D8000-DBFF0h
D4000-D7FF0h
D0000-D3FF0h
CC000-CFFF0h
C8000-CBFFFh
Not Installed

Make sure you do not choose an address used for Flash devices. The address chosen affects whether or not this is the boot device.

VME Scan Range:

This option is used for VME booting. To boot from VME, use **XFORMAT** with the **/F** option to first create a file that looks like a FAT/boot record. Then upload the file to VME memory on a 100000h boundary in one of the memory ranges below. Set the scan range to match where in VME memory the file was placed. Be sure to enable the VME ROMdisk BIOS extension to enable scanning.

00000000-FFF00000h A32SD
00000000-00F00000h A24SD
FF000000-FFF00000h A24SD

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3 3

Integrated Peripherals Sub-Menu

Use the options in this sub-menu to configure the COM and LPT ports.

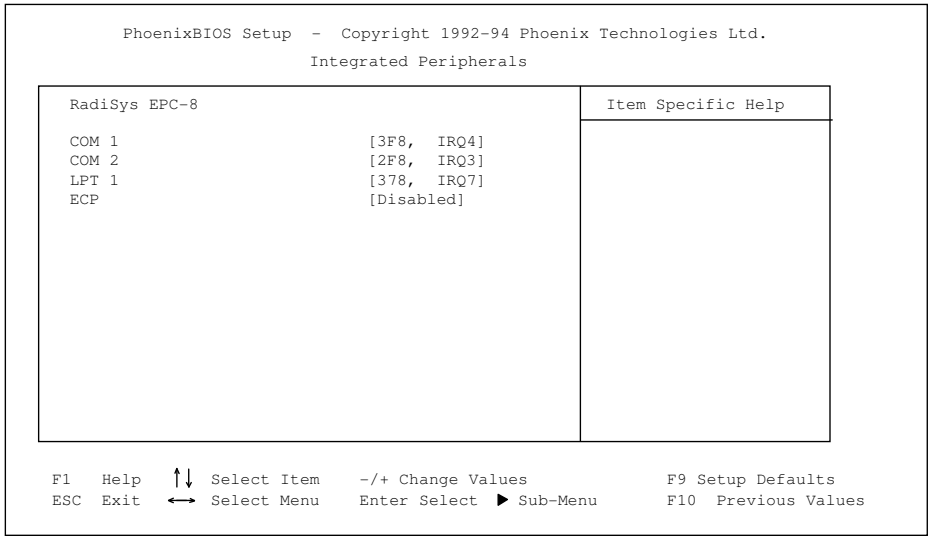


Figure 3-6. Integrated Peripherals Sub-Menu.

COM PORT/COM PORT

Use this option to enable or disable the COM1 and COM2 ports. The default for COM1 is 3F8 and IRQ4; the default for COM2 is 2F8 and IRQ3.

LPT PORT

Use this option to enable or disable the LPT port address and IRQ. The default is 378 and IRQ7.

ECP

Use this option to enable or disable the **E**xtended **C**apabilities **P**ort feature of the parallel port. When this feature is enabled the parallel port becomes bi-directional.

When you are finished, press ESC to exit back to the Advanced Menu.

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Memory Shadow Sub-Menu

The term "Memory Shadow" refers to the technique of copying information from ROM into RAM and accessing it in this alternate memory location. The Memory Shadow Sub-Menu is discussed below.

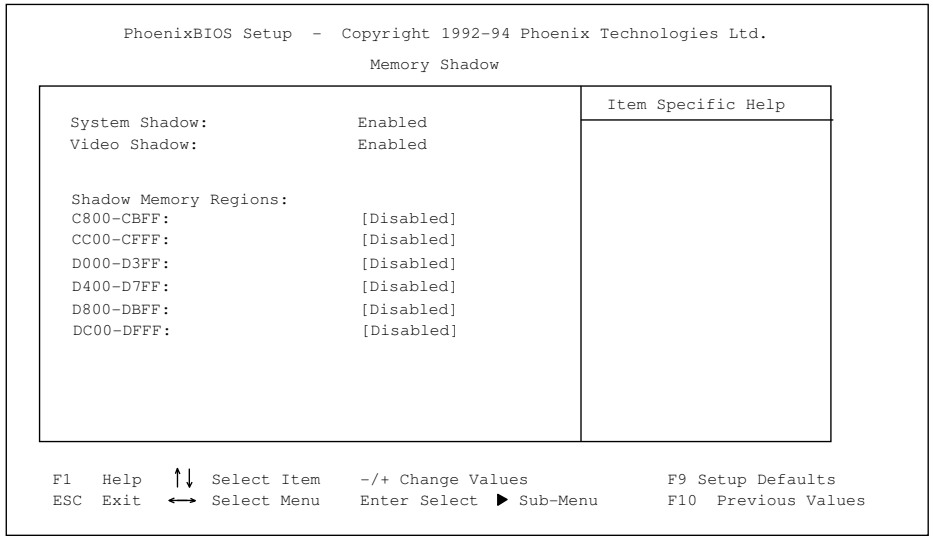


Figure 3-7. Memory Shadow Sub-Menu.

About Shadow Memory Regions:

The shadow regions should be used only if an EXM module is installed in the system that contains a BIOS ROM. Enabling shadowing for the region occupied by the ROM will increase system performance.

Do not enable shadowing for the region you may have specified for installing Flash or VME disks. When these ROMs are installed, they are automatically shadowed.

This completes the setups for the Advanced Menu.

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EXM Menu

Use this menu to set up the optional EXM expansion modules in your EPC-8. Enter the EXM-ID, plus option byte information for OB1 and OB2. This information is found in the hardware reference manual shipped with each EXM expansion module.

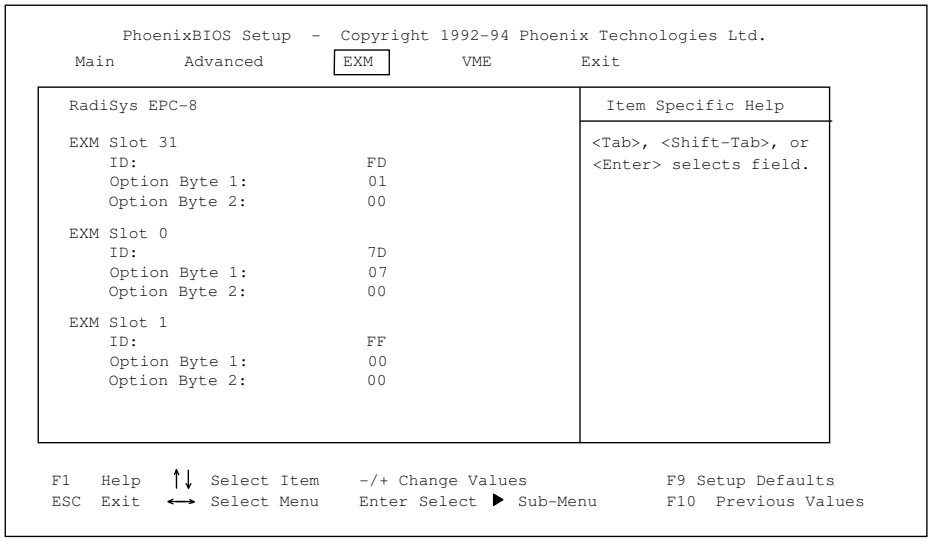


Figure 3-8. EXM Menu.

Note the following when installing EXMs:

SLOT	indicates the EXM slot in which the EXM is installed.
ID	is a hard-wired ID value. Each type of EXM has a unique ID value.
OB1/OB2	are two "option" bytes of configuration information.

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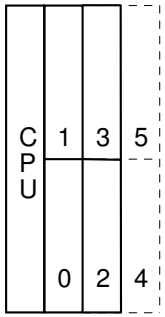


Figure 3-9. Slot Numbering.

All slots **not** occupied by an EXM module should show an ID of FF and OB1/OB2 of 00 00 indicating that no EXM is present

ID:

Enter the EXM-IDs for the EXMs you intend to install in this system. Up to six EXMs can be installed.

Option Byte 1:/ Option Byte 2:

Each EXM expansion module has values you must enter for the option byte 1 and option byte 2 configuration data. When you are finished with this menu, press the right arrow key to move to the VME Menu, or press ESC.

EXM Slot 31

Slot 31 refers to the optional resident Flash memory. The ID should be set to FF if your EPC-8 does not have this feature. If present, then set the ID to "FD" and Option Byte 1 to "01".

Slots 0 through 8

Consult the appropriate EXM manual for the correct configuration information for each EXM expansion module installed. Note, however, that most EXM hardware reference manuals depict a different setup BIOS from the EPC-8. The ID/OB1/OB2 information is valid.

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When using EXMs with configurable interrupts, DMA channels, I/O addresses, and/or memory addresses, avoid conflicts with built-in functions of the EPC-8. Guidelines are:

1. If an interrupt is needed, use IRQ3, IRQ5, IRQ9, IRQ12, or IRQ15. IRQ7 can be used if the printer port is not being used. IRQ3 should not be used if the COM2 port is being used.
2. Use DMA channels 1, 3, 6, and 7.
3. Do not select I/O addresses that conflict with those in the EPC-8. A complete list appears in Appendix A. For instance, I/O addresses in the 300-33F range can be used.
4. If the EXM needs to use upper memory addresses, they must be in the 0C8000-0DFFFF range. Note that the E-page is used for VMEbus access and is not available.

VME Menu

Use the options in this menu to configure the VMEbus interface and addressing.

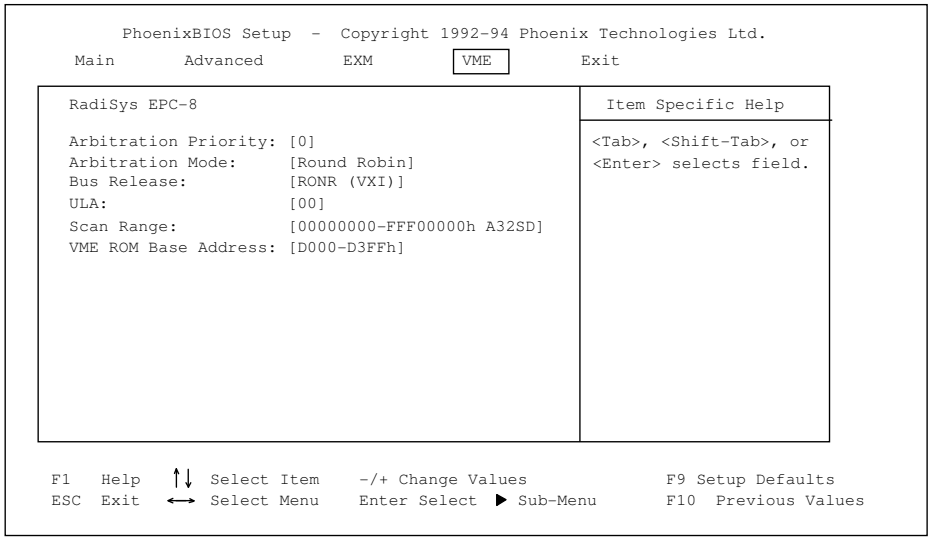


Figure 3-10. VME Menu.

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Arbitration Priority:

Use this option to set the arbitration priority. Possible values are 0, 1, 2, and 3, with a value of 0 indicating the highest priority. This determines which VMEbus request signal the EPC-8 uses when it accesses the VMEbus.

Arbitration Mode:

Use this option to select the arbitration mode. Possible values are "Round Robin" or "Priority." This determines how the EPC-8 performs bus arbitration when it is the VMEbus Slot-1 controller. If round-robin is selected, the four bus request lines have equal priority. If Priority is selected, bus request 0 has highest priority.



Bus Release:

Use this option to select the Bus Release mechanism. Possible values are RONR (VXI) and ROR (VME).

ULA:

Use this option to select the unique logical address (ULA). Possible values range from 00 through FF.

The logical address controls where in the VME A16SD space the EPC-8 extended registers are mapped. If the ULA=0, the registers are at C000. If the ULA=FF, the registers are at FFF0. In general, the registers map to [C000 + (ULA*20)] (all numbers in hexadecimal).

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3 3

Exit Menu

Use the options in this menu to save and exit, or abandon your changes and exit to the system.

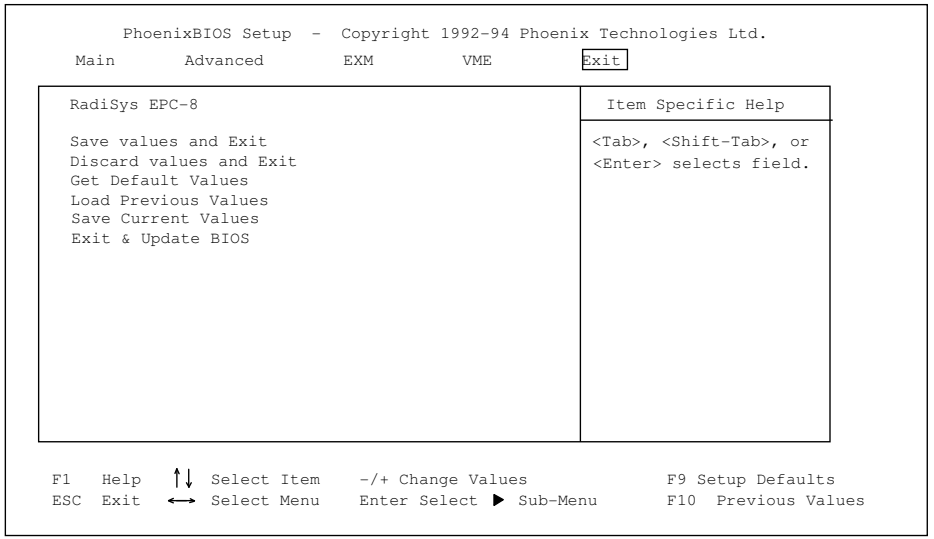


Figure 3-11. Exit Menu.

Save Values and Exit

Use this option if you want to save the values you have just entered and exit in order to load the operating system. The new values are loaded, and you exit and reboot.

Discard Values and Exit

Use this option if you want to discard the changes you just made and revert to the BIOS as it was before you started. The system boots with the old values.

Get default values

Use this option if you need to reset the BIOS values to the original, default values that were set at the factory, before any suppliers or other end users made changes.

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Load previous values

Use this option if you want to load the system with the previous values before this editing session started. You do not exit.

Save Current values

Use this option to save the edits you have made during this session. You do not exit.

Exit and Update BIOS

This option is only for users who plan to update their BIOS from a floppy disk.

NOTE: Do not select this exit option unless you have obtained BIOS update replacement software from your supplier and have reviewed the documentation and procedures provided with that distribution.

If you select this option by mistake, any changes made to the BIOS are lost unless you have already saved them using the **Save Current Values** option. The system automatically begins searching for the update program that should be on the floppy disk inserted in drive A. If there is no floppy, you get two series of beep codes: a long and two short beeps, followed by three short beeps that repeat. Cycle the power to reset the system to its previous state.

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NOTES

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Chapter 4 - Theory of Operation

Overview

The EPC-8 is a PC/AT compatible computer with standard PC peripherals, a VMEbus interface, and modular expansion capability via the EXM expansion interface. Figure 4-1 provides an diagrammatic overview of the system functional blocks. Most of the standard functions of the PC architecture are embodied in the VLSI 82C486 chipset. DRAM and VGA are interfaced to the 486 processor by a 32-bit local bus. The customary PC peripheral interfaces for keyboard, two serial ports, a parallel port, and a battery-backed real-time clock are connected by the EXM expansion interface which is electrically similar to the standard PC ISA bus. An Ethernet controller is built onto the EPC-8 board.

The VMEbus interface includes special VME byte swapping hardware to aid the software when dealing with different processor and memory organization. This is described in detail later in this chapter.

The EPC-8 maps a standard set of VXI configuration registers onto the VMEbus A16 space. These are dual-ported and accessible both by other VMEbus modules and the EPC-8 in its I/O space.

Resident Flash memory (on the EPC-8 board) is I/O mapped and appears as an EXM expansion module as if in EXM slot 31. SRAM is memory mapped. The PC BIOS is shadowed into main memory at start-up.

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4 4

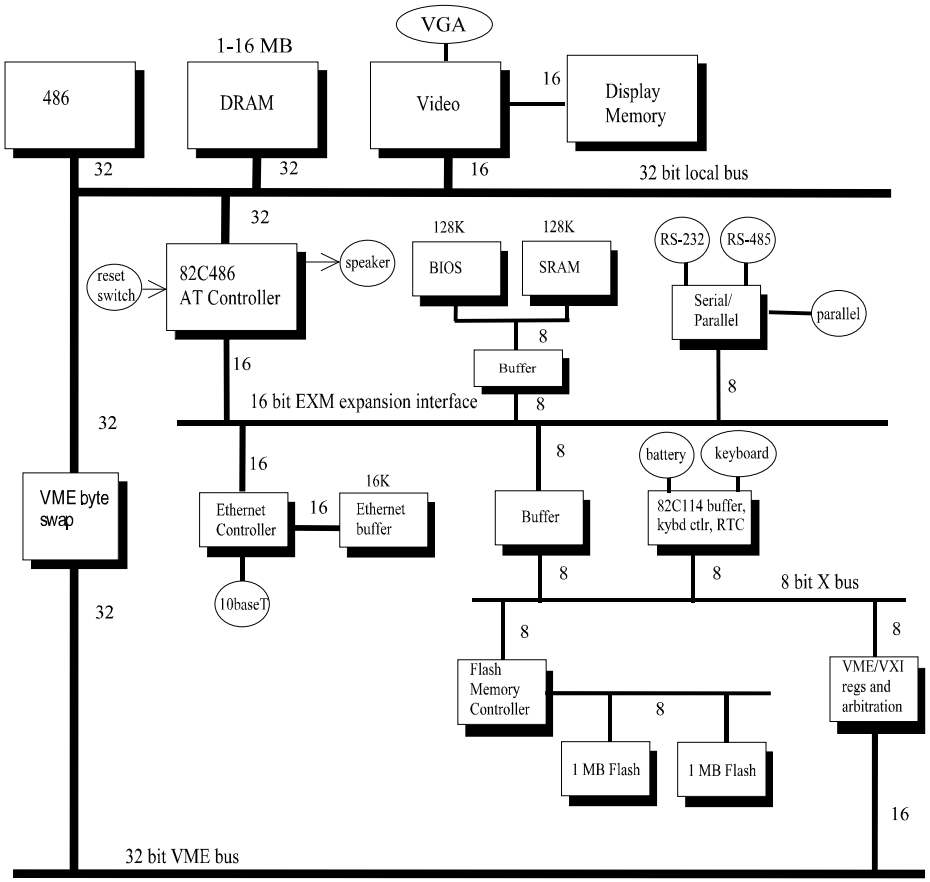


Figure 4-1. EPC-8 Block Diagram.

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Processor board

The EPC-8 processor board conforms with the VMEbus standard 6U form-factor.

Processor and Coprocessor

There are two processor options for the EPC-8. There may be an Intel486 DX2 (32-bit bus interface) running at 50 MHz, or an Intel486 DX2 running at 66 MHz.

The 50 MHz DX2 and 66 MHz DX2 each have a built-in math coprocessor.

Memory

The following memory options are supported: 4 Mbytes, 8 Mbytes, and 16 Mbytes. One SIMM socket is available. See Appendix D, *Memory* for memory upgrade instructions.

Memory Map

The 2^{32} byte physical address space seen by the Intel486 occupies three areas:

1. Addresses between 0 and 1 Mbytes, which are largely defined by the IBM PC/AT architecture.
2. Addresses between 1 Mbytes and 256 Mbytes, which largely depend on how much DRAM is installed in the EPC-8.
3. Addresses above 256 Mbytes, which provide direct mapping to the VMEbus with a variety of address modifiers and byte orderings. See Chapter 5, *Programming Interface* for more information about this feature.

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Memory at addresses between 0 and 1 MB (0FFFFFh) is mapped as follows:

Range		Content
000000	- 09FFFF	DRAM (first 640 KB)
0A0000	- 0BFFFF	Almost always used by a video controller as video RAM.
		If the onboard VGA is populated and enabled, then this memory is accessed over the CPU local bus. Otherwise, it is mapped to the EXM interface.
0C0000	- 0C7FFF	Write-protected DRAM containing video BIOS
0C8000	- 0DFFFF*	Uncommitted; mapped to EXM interface.
0E0000	- 0EFFFF	Either is mapped to EXM interface or is window into the VMEbus. Mapping controlled by bit-1 of register 8102.
0F0000	- 0FFFFF	Write-protected DRAM containing system BIOS

* 0C8000 - 0DFFFF may be used either as page frames (i.e. for Ethernet, etc.) or may be used by DOS as upper memory blocks if an EMM driver is installed or may be used for BIOS extensions.

For a 4 MB EPC-8, the extended memory address space is defined as follows:

00100000	003FFFFF	3 Mbytes DRAM extended memory
00400000	00FFFFFF	Uncommitted; mapped to EXM interface

For an 8 MB EPC-8, the extended memory address space is defined as follows:

00100000	007FFFFF	7 Mbytes DRAM extended memory
00800000	00FFFFFF	Uncommitted; mapped to EXM interface

For a 16 MB EPC-8, the extended memory address space is defined as follows:

00100000	00FFFFFF	15 Mbytes DRAM extended memory

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BIOS ROM and ROM Shadowing

The EPC-8 contains a Flash boot device (chip) as its BIOS ROM. The BIOS ROM is mapped into the top of the processor's 32-bit address space. The BIOS consists of an 8 Kbytes boot block and a System BIOS combined with a VGA BIOS in a 112 Kbytes partition. The Flash boot device is memory addressed and resides in the last 128 Kbytes of system memory at address FFFE0000H to FFFFFFFFH. The layout is described in Figure 4-2.

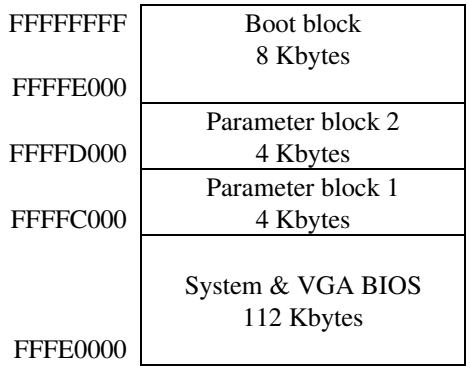


Figure 4-2. Flash Boot Device Memory

The BIOS initialization software copies the ROM contents into DRAM (a process called *shadowing*) at addresses 0F0000-0FFFFF (also called the "F" page). The VGA BIOS is copied into 0C0000-0C7FFF of DRAM. If the user has configured an EXM VGA card (e.g., an EXM-13A) and enabled it, the EXM's BIOS is used for the copy. Otherwise, the internal VGA BIOS is copied and enabled.

After copying into these areas, the BIOS write-protects them. Subsequent writes to these areas complete successfully but do not alter the data in DRAM. However, the proper sequence of writes will alter data in the Flash boot device (BIOS ROM) itself, if the jumper is installed.

There are two parameter blocks, each 4 Kbytes in size. The first parameter block is used by the utilities program **CMOSTOOL.EXE**, located on the EPC-8 **File/Utilities** diskette. The use of this program is discussed below. The second parameter block is unused. Access to this memory is complex. Your should consult the Intel *Memory Products* data book for details on programming parameter block 2 if this is required.

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Be aware that the contents of this block are included in the BIOS checksum so any modification to this area also requires a modification to the checksum value itself.

CMOS Backup and Restore

Use the **CMOSTOOL.EXE** function to copy and restore CMOS parameters into the 4 Kbyte-sized "parameter block 1" on the Flash boot device chip. This is useful if battery life becomes an issue, or for backup.

To **Save** your CMOS parameters into a partition block in the Flash memory, type the following:

```
CMOSTOOL /S
```

Jumper JP4 ("BIOS") must be installed for **Save** to work. Be sure to remove this jumper after using this function.

To **Load** the saved CMOS parameters in the Flash memory *back* into CMOS, type the following:

```
CMOSTOOL /L
```

Video Controller

The EPC-8 hardware includes a VGA graphics controller implemented using the Cirrus Logic GD54xx. This is connected to the CPU local bus to give the best possible graphics performance. VGA memory is 512 Kbytes, resulting in the following resolutions:

640 x 480	16 or 256 colors
800 x 600	16 or 256 colors
1024 x 768	16 colors

The BIOS will not enable (using bit 2 of register 8102) the VGA controller if another VGA controller is enabled on the EXM expansion interface.

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Ethernet Controller

The EPC-8 contains an on-board Ethernet controller connected through the 16-bit EXM expansion interface, which is compatible with Western Digital 8013, Novell NE2000 and NE2000+ cards through the use of National Semiconductor's DP83905 (AT/LANTIC chip). The default configuration for the Ethernet port is as a WD8013-compatible card. The I/O base address is 240. Interrupts are signaled on IRQ5. These parameters can be changed by running the **AUTOSET.EXE** program that is optionally available from your supplier. The possible alternative interrupts are IRQ3, IRQ9 and IRQ15.

The EPC-8 Ethernet port has two 8 Kbytes x 8 RAM chips for packet buffering and a 10 Base-T interface. Eight-bit network drivers cannot be used with the EPC-8.

For more information about the **AUTOSET.EXE** program, refer to Appendix H.

Resident Flash/SRAM Memory

The EPC-8 can optionally be built with 2 Mbytes of Flash memory and 128 Kbytes of Static RAM resident on the processor board.

Resident Flash Memory

The resident Flash memory is accessed via 8-bit read/write registers and physically appears on the EXM expansion interface as if it is in slot 31. It is enabled as if it were a standard RadiSys EXM expansion card in that slot.

The EPC returns an ID of FD to a read of address 100. This is the same ID that would be returned from a RadiSys EXM-2A card. You can use the optional **XFORMAT.EXE** utility to format and load the resident Flash memory under MS DOS. The EXM-2A and the resident Flash memory cannot both be used in a single EPC-8 system. Note: You must set jumper JP5 ("FLASH") before the Flash can be written. Jumper locations are described in Figure 2-1.

SRAM

The battery-backed SRAM is memory mapped. The resident SRAM resides on the EXM expansion interface and, when populated, can be accessed at 0xFX3XXXXX or 0xFXBXXXXX. If there is less than 16 Mbytes of DRAM, it may also be accessed at 0x00BXXXXX. A battery low indicator (low when 0) is returned in bit 0 of register 8387.

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4 4

Watchdog Timer

The watchdog timer is a binary counter which, upon overflow, will signal a watchdog timer event. The counter will cause a watchdog event after approximately 125 mS, 1 second or 8 seconds (depending on the value of FWDT and SWDT, bits 2 and 1 in register 815D) if the application software does not reset the timer.

An I/O read to address 815D resets the counter. If WDTR (bit 3 of register 815D) is set, the following occurs in response to a timeout event:

WDT (bit 3 of register 8154) is set. A local ‘‘warm’’ hardware reset occurs (SYSRESET* is not driven unless ENSYSO bit has been set, bit 6 of 0x815D). Bits 1, 2, and 3 of register 815D are cleared to prevent the watchdog timer from expiring on a warm reset that is initiated from a source othe than a watchdog timeout. ENSYSO (bit 6 of 815D) is cleared by the BIOS in response to warm resets to keep from losing the watchdog timeout bit while setting the BTOE bit. VME SYSFAIL* is also asserted. When exiting a hardware reset condition, the BIOS can check the WDT bit. If this bit is set (0), then a watchdog timeout caused the hardware reset (as opposed to SYSRESET or power-on reset). Then depending on the value of a setup option the BIOS will either HALT the CPU or allow the boot process to continue. At this point, software may deassert the VME SYSFAIL* condition by reading the register at 0x815D.

Note that a watchdog hardware reset results in a "warm" hardware reset. A warm hardware reset clears all register bits except for the upper four bits of the Configuration register (these control Slot-1 arbitration functions) and bits 4 and 6 of the Module Status/Control registers (these control bus timeout function and watchdog timer functions). A warm reset does clear WDTR (bit 3 of the Module Status/Control register) to allow the hardware to be released from the warm reset state, but SYSFAIL will continue to be driven until the WDT bit is cleared by either reading the Module Status/Control Register or by a power-on reset.

If WDTR is clear, WDT mask (bit 3 of register 8155) enables an interrupt if a timeout event occurs (SYSFAIL is not driven). The clock is disabled to the counter if the interrupt is pending and not serviced. Service of the interrupt is signaled to the counter by reading register 815D. This will reset the counter value and resume counting. The interrupt is signaled on IRQ10. The timer event also clears WDT bit in the BES register (bit 3 of register 8154).

Application software that utilizes this timer should take care to reset the counter just prior to enabling the interrupt bit in register 8155. This will inhibit a spurious timer event from occurring just after enabling the timer.

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Battery

The battery powers the CMOS RAM and TOD clock when system power is not present. At 60°C, the battery should have a shelf life of over four years. In a system that is powered on much of the time and where the ambient power-off temperature is less than 60°C, the battery is estimated to have a life of 10 years.

If system power is present, the VME +5V STDBY voltage also powers the CMOS RAM and TOD clock. This is done with isolation diodes, so that either the onboard battery or the VME voltage will supply power. Neither power source will affect the other.

The 3.0V lithium battery supplied with the EPC-8 is a Panasonic BR2330 "coin cell" or equivalent. It is mounted behind the reset button at the top of the EPC-8. Should the battery fail, you may obtain and install a replacement.

Replacing the battery is a simple task. However, removing the battery **will** invalidate the CMOS setup parameters if you do not put the new battery into the empty socket within about 60 seconds. It is recommended that all setup parameters be written down while the battery is still good, or saved using the **CMOSTOOL.EXE**. See the description of the CMOSTOOL utility software in this chapter for a method to backup CMOS parameters into a Flash memory parameter block.

To replace the battery, lay the EPC-8 flat on an ESD-protected surface. Remove the SIMM module, following proper ESD protection procedures. Now slide the battery out and quickly place the new battery into the empty socket. Replace the SIMM module and reinsert the EPC-8 into the system.

Peripheral Ports

The I/O address and IRQ of the peripheral ports are determined by the CMOS parameters established by default and modified via BIOS Setup screens.

RS-232 Port

The RS-232 port is a standard PC COM port based on the 16450 architecture. It is normally configured as COM1 (I/O address = 3F8-3FF, IRQ4). "COM1" is an alias for an address and is determined by the first COM port found. If not needed, COM1 can be disabled in the BIOS Setup screen to free up the I/O address and interrupt for usage by other expansion products.

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RS-422/485 Port

The modified RS-422/RS-485 port is normally configured as COM2 (I/O address = 2F8-2FF, IRQ3). This port is also a standard PC COM port based on the 16450 architecture. If not needed, COM2 can be disabled in the setup screen to free up the I/O address and interrupt for usage by other expansion products. The RXD and TXD signals are RS422 compatible with differential receiver and driver, respectively. Handshake signals RTS, DTR, CTS and DSR are single-ended RS422 compatible. Outputs TXD+ and TXD- are tristated if RTS is unasserted for RS485 multidrop compatibility. The port has 10K ohm termination.

Parallel Port

The printer port is a standard PC printer port. The parallel port supports bi-directional communication compatible with the PS/2 definition. It is configured as LPT1 (I/O address 378-37F, IRQ7). If not needed, LPT1 can be disabled in the setup screen to free up the I/O address and interrupt for usage by other expansion products.

Keyboard

The keyboard controller is integrated into the VLSI PC chip set. It can interface to most standard PC keyboards with a PS/2-style connector. An adapter cable is shipped with the EPC-8 to allow use of standard PC/AT keyboards with larger 5-pin connectors.

Front Panel LEDs

The EPC-8 has three LEDs in the top left corner of the front panel. These LEDs are described below:

RUN — This LED is lit whenever a write access to DRAM is made. This provides a normally lit LED indicating that the CPU is operating. This LED is not lit if the CPU is halted or is executing entirely out of the on-chip cache.

FAIL — This LED is lit whenever the VME SYSFAIL line is asserted if the EPC-8 is jumpered to be the Slot-1 controller. This occurs independent of which VME board is driving the SYSFAIL line. It comes on whenever the system receives a hardware reset and remains on until the initial power-on self-tests have completed.

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TEST This LED is lit whenever the system is running its power-on self-test, as reflected in the PASS bit in the VXI registers. If PASS is 0, then this LED is lit. This only occurs during a hardware reset.

Resetting the EPC-8

There are a number of ways to reset (reboot) the EPC-8.

Power-off, Power-on

Known as a cold hardware reset. This causes all boards in the VMEbus to reset. The system runs the power-on self-tests and reboots the OS.

Power low

"Warm" hardware reset. When power is detected between ~3.0 and ~4.5V, the system runs the Power On Self Test (POST) and reboots the operating system. When power is less than ~3.0V, the system performs a cold hardware reset.

Front-panel Reset button

"Warm" hardware reset. The Reset button causes the EPC-8 to perform a hardware reset. The system runs the power-on self-tests and reboots the operating system.

Ctrl+Alt+Del

"Warm" software reset. This keyboard sequence is also called a "warm boot". The EPC-8 does not reinitialize all of the processor's hardware. The power-on self-test does not run. However, the operating system is reloaded.

VMEbus SysReset

"Warm" hardware reset. The EPC-8 can be software-configured to respond or not respond to the VMEbus SYSRESET* line. Asserting bit 7(SRIE) of register 8144 allows the VME SYSRESET* signal to reset the EPC-8. The reset semantics are the same as the front panel reset.

Watchdog Timer

"Warm" hardware reset. Same as a front panel reset button except that SYSFAIL is asserted until the watchdog timer is cleared.

Resets are summarized in the table below.

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Power-On Reset	Power Low < 3.0 V	Power Heading Lower 3-4.5 V	Front-Panel Reset Button	Ctrl-Alt-Del	VME bus SysReset Line Asserted	Watch dog Timer
"Cold" reset	"Cold" reset	"Warm reset	"Warm" reset	Soft ware reset	"Warm" reset	"Warm" reset
POST runs	POST runs	POST runs	POST runs	No POST	POST runs	POST runs
80C486, 82C486, all VXI registers reset	80C486, 82C486, all VXI registers reset	80C486, 82C486, most VXI registers reset	80C486, 82C486, most VXI registers reset		80C486, 82C486, most VXI registers reset	80C486, 82C486, most VXI registers reset
		bits 4-7 of 8102 not reset; bits1,2,4 & 6 of 815D not reset	bits 4-7 of 8102 not reset; bits1,2,4 & 6 of 815D not reset		bits 4-7 of 8102 not reset; bits1,2,4 & 6 of 815D not reset	bits 4-7 of 8102 not reset; bits1,2,4 & 6 of 815D not reset
AT. RESET generated	AT. RESET generated	AT. RESET generated	AT. RESET generated	No AT. RESET	AT. RESET generated	AT. RESET generated
SYS RESET* generated	SYS RESET* generated	SYS RESET* not generated unless bit 6 of 815D is set	SYS RESET* not generated unless bit 6 of 815D is set	No SYS RESET *	SYS RESET* not generated unless bit 6 of 815D is set	SYS RESET* not generated unless bit 6 of 815D is set
						SYS FAIL asserted until watch dog timer is reset

Table 4-1. Reset Conditions.

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Register State after Reset

A "cold" or hardware reset of the EPC-8 (not a keyboard CTRL+ALT+DEL reset) clears all of the register bits to 0, except for RELM, ARBM, and ARBPRI, which may be in an undefined state. (All bits, however, are cleared by a power-on reset.) However, this may not be apparent because the BIOS initialization sequence then reinitializes values in these register fields, largely as a result of the non-volatile configuration information specified in the setup screen.

VME/VXI Soft RESET state and SYSRESET

"Soft Reset" is a capability that allows another VME master to disable the EPC-8's connection to the VME bus, without interrupting (or resetting) the 486 processor on the EPC-8.

The Soft Reset state is entered when the SRST bit is set. In this state the EPC-8 removes any asserted interrupts (clears the Interrupt Generator register, disables its VME master logic, asserts both the VMER and BERR sticky bits in the VME Event State register, disables watchdog timer resets and interrupts, and clears the PASS bit. SYSFAIL will also be asserted if the NOSF (SYSFAIL inhibit) bit is clear. The Slot-1 arbitration and control logic and the bus timeout function, if it is enabled, is unaffected by the SRST bit. Software on the EPC-8 can detect that another board has set the EPC-8 into Soft Reset state by several different methods:

(1) Enable the interrupt events associated with either the VMER bit or BERR bit.

(2) After each VME master access poll the BERR bit. If this bit is set either a true bus timeout occurred (VMER will not be asserted in this case) or the Soft Reset state has been entered (both VMER and the BERR bits are asserted).

The Soft Reset state can be exited by a push-button reset, a power-on reset, by simply writing a 0 to the SRST bit, or by the assertion of SYSRESET when the SRIE bit is also set. When SRST is cleared by writing the bit to 0, the VMER and BERR bits should also be cleared by writing to the VME Event State register, VME master accesses will again be enabled (if they were enabled prior to SRST being asserted), and the watchdog functions, that were enabled prior to SRST being asserted, resume (with the counter starting in the cleared state).

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The EPC-8's reaction to SYSRESET* being asserted on the VME bus depends upon whether the SRIE bit (SYSRESET Input Enable, bit 7 of the Status/Control register) is set or clear. When SRIE is asserted (set), the assertion of SYSRESET* results in the same "warm" hardware reset that a watchdog timer reset causes. When SRIE is not asserted, the EPC-8 responds to the assertion of SYSRESET* by placing the EPC-8 into a state almost identical to the Soft Reset state. The only difference between the two states is that the PASS bit (bit 2 of Status/Control register) is not cleared by the assertion of SYSRESET* (as long as SRIE is 0 - to avoid a warm reset), but the PASS bit is cleared by the assertion the SRST bit.

Signal Register FIFO

To spell out the operation of the Signal Register FIFO and associated control bits, the operations are explained in algorithmic fashion. SIG, FSIG and LSIG are fields in the Response register. The signal FIFO, called SRFIFO henceforth, is a two-element array with indexes.

A write to VPR from the VXI is a write to the signal register (and FIFO), and does the following:

```
if (SIG && (FSIG != LSIG)) {    /* FIFO full */
  assert BERR;
}
else {
   if (SIG) LSIG = !LSIG;
   SRFIFO[LSIG] = data_bus;
...SIG = 1
}
```

A read from SRFL returns the low-order byte of SRFIFO(FSIG). In all cases of accesses to SRFL and SRFH, if SIG = 0 (empty FIFO), the result is an access to SRFIFO(0). A read from SRFH returns the high-order byte of SRFIFO(FSIG), and does the following:

```
if (FSIG == LSIG) {SIG = LSIG = FSIG = 0}
   else FSIG = !FSIG;
```

Writes to SRFL and SRFH (I/O address 0x8148,0x8149) are identical to reads except for the direction of the data flow (e.g., writing to SRFH alters the high-order byte of

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SRFIFO(FSIG) and does the above action). The only apparent purpose of these writes is testability.

EXM Expansion Interface

The EXM expansion interface is electrically similar to the PC/AT ISA (16-bit data) bus. In addition, it contains a signal EXMID* used for dynamic recognition and configuration of EXMs. EXMs respond to one or more I/O addresses in the range 100h - 105h only when their EXMID* line is asserted. EXMs are required to return a unique EXM ID byte in response to a read from I/O address 100h.

This ID byte is the same identification byte discussed earlier in Chapter 3, *BIOS Configuration* in the section on the *EXM Menu*.

The EXM expansion interface is provided on rows A, C, and D of the EPC-8's 4-row DIN P2 connector. The subplane carries the EXM interface to other modules, such as to EXM modules and the EXP-MX Mass Storage module. These EXM interface signals are not passed through to the VMEbus.

Further information on the EXM expansion interface, its connectors, and standards for building EXMs is available upon request.

VME Interface

Connectivity

The EPC-8 module connects to the VMEbus J1 connector directly and uses all of the defined VMEbus lines except SERCLK, and SERDAT. Connection to the J2 connector is through the subplane's 4-row DIN connector B row. Connections to the VME J2 backplane are on the B row and are power and ground, address lines A31-A24, data lines D16-D31.

VMEbus System (Slot-1) Controller Functions

Every VMEbus system must have a System (Slot-1) Controller. The Slot-1 controller provides the following functionality:

- Serves as the bus arbiter (priority or round-robin)

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- Drives the 16 MHz SYSCLK signal
- Starts the IACK bus grant daisy chain.
- Provides Bus time-out function

When configured as the Slot-1 controller, the EPC-8 detects and terminates data transfer bus timeouts. Once it sees either the DS0 or DS1 lines asserted, a counter is started. If the counter expires before both DS0 and DS1 are deasserted, the EPC-8 asserts the VMEbus BERR signal until both data strobes are deasserted. The duration of the VMEbus timeout counter is approximately 100-120 µsecs.

When the EPC-8 is configured as the slot-1 controller, this timeout cannot be disabled and the duration cannot be changed.

4 4

VMEbus Access

VMEbus accesses are available either by mapping a 64 Kbytes segment of the VMEbus through the 0E0000-0EFFFF "E page" window or by direct mapping above 256 Mbytes.

Byte Ordering

There are two fundamentally different ways of storing numerical values in byte locations in memory:

- Little endian, characteristic of Intel microprocessors, where the **least**-significant data byte (LSB) is stored in the lowest byte address

Address + 3	Address + 2	Address + 1	Address
Byte 3	Byte 2	Byte 1	Byte 0
MSB			**LSB**

- Big endian, characteristic of Motorola microprocessors and the VMEbus environment in general, where the **most**-significant data byte (MSB) is stored in the lowest byte address

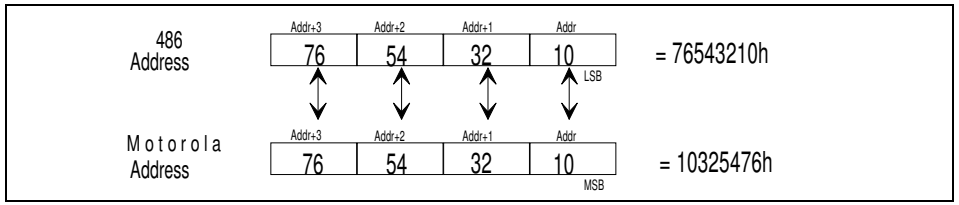
Address + 3	Address + 2	Address + 1	Address
Byte 3	Byte 2	Byte 1	Byte 0
LSB			**MSB**

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The EPC-8 contains programmable byte-swapping hardware to allow programs to read or write VMEbus memory in either byte order. When using the E-page to access the VMEbus, the order is selected by bit 5 (BORD) in the VME modifier register (8151). When using direct memory mapping, the order is address-range dependent (e.g., E0000000-E0FFFFFF accesses the A24 space with big endian byte ordering, and 20000000-20FFFFFF accesses the A24 space with little endian byte ordering).

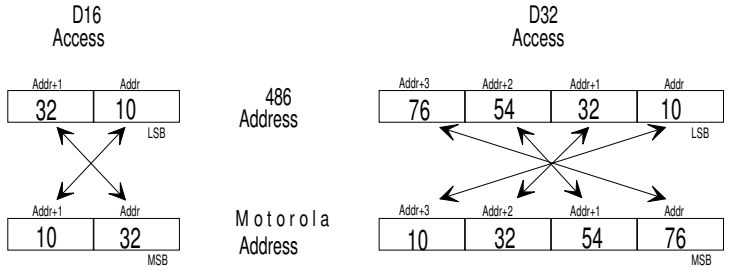
When performing a single byte (D08) access, the byte order makes no difference. However, word (D16) or double-word (D32) accesses may require byte-swapping.

When little-endian is selected, bytes pass straight through unchanged. Little endian should only be used when reading or writing data between two Intel processor systems. The results of using little-endian byte ordering to transfer a double-word integer between an Intel processor and a Motorola processor are shown below.



Since the 486 processor uses Addr as the least-significant byte and the Motorola processor uses Addr as the most-significant byte, the processor receiving the data gets a "scrambled" value.

When big-endian is selected, the bytes are swapped between the 486 and VME. See the diagram below.



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When using big-endian byte ordering, care must be taken to assure that the VME address is aligned on a boundary; for D16 accesses the VME address must be on a word boundary (address evenly divisible by 2) and for D32 accesses the VME address must be on a double-word boundary (evenly divisible by 4). If this is not done, the results will be "scrambled" data. Although the VMEbus address must be boundary-aligned to match the data width (word or double-word), the 486 address does not need to be boundary-aligned.

Another consideration is the compiler being used. Some compilers produce two 16-bit accesses when a 32-bit access is desired. When this occurs, again the data will be "scrambled."

When transferring a 32-bit floating-point number, special care must be taken to assure that both processors use the same floating-point format; that both systems expect the mantissa and exponent in the same byte locations. As long as this is correct, transferring a floating-point number will work correctly. Since transferring a 64-bit floating-point number is not supported in hardware, two 32-bit transfers must be used with little-endian byte order and then byte-swapping must be accomplished in software.

The EPConnect Bus Manager software provides a means of selecting the byte ordering during memory-copy operations.

VMEbus Interrupt Response

When the EPC-8's Interrupt Generator register (815F) is used to assert an interrupt, the EPC-8 formulates a status/ID value that is transmitted on the bus as the response to a matching interrupt acknowledge cycle. The EPC-8 acts as both a D08(O) and D16 interrupter. For D08 interrupt acknowledge cycles, the status/ID value is the EPC-8's logical address (11111aaa, where aaa is the value of ULA as defined in port 814A). For D16 and D32 interrupt acknowledge cycles, the status/ID value consists of 16 bits. The upper eight bits are the upper half of the response register (the value in I/O port 814B) and the lower eight bits are the logical address.

VME Extension Registers (VXI)

The EPC-8 maps a standard set of VXI configuration registers onto the VMEbus A16 space and thus accessible by other VMEbus modules. These registers are 16-bit registers occupying 64 bytes of A16 space at a base address defined by the EPC-8's logical address. The VME-mapped registers are a subset of those defined as I/O ports in the EPC-8. The registers are dual-ported in that they are accessible both from VME and from within the EPC-8 as ports in its I/O space.

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Refer to Appendix F, *VMEbus Mapped Registers* for additional information.

Passing VME Interrupts and Events to the CPU

The diagram below shows how VME interrupts and VME events are generated and passed to the CPU:

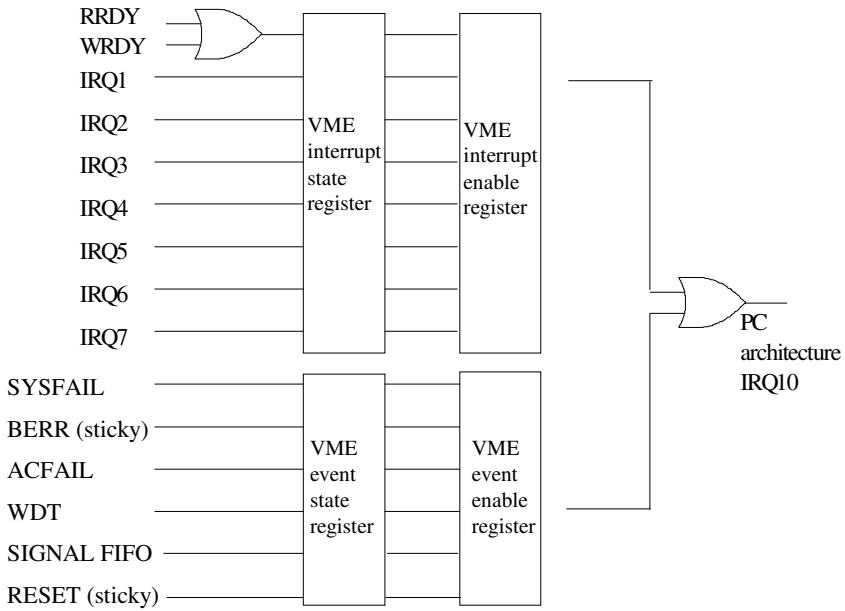


Figure 4-3. Passing VME Interrupts and Events to the CPU.

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Interrupt-causing signals are visible in two state registers. Most of these are unlatched, meaning that a read of the state register shows the actual state of the signals at the instant of the read. The exceptions are (1) BERR, which is a "sticky" bit, meaning that the bit signifies whether BERR had ever been asserted (the SBER register bit), and (2) RESET, another sticky bit. The convention used is that a 0 bit signifies an asserted (interrupting) state.

The primary purpose of the state registers is to let the interrupt handler software determine which interrupts and events generated the IRQ10 interrupt to the processor. The state registers can also be read by non-interrupt-handler software to poll for the state of these signals.

The enable registers allow one to mask selectively these 14 states. A 0 state bit and a corresponding 1 enable bit causes the PC architecture IRQ10 interrupt to be asserted.

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Chapter 5 - Programming the VMEbus Interface

This chapter describes the EPC-8 VMEbus interface as seen by a program. Users should avoid direct use of most of these facilities. Whenever possible, the VMEbus interface should be accessed through the EPConnect software or other higher level programming facilities.

The EPC-8 VMEbus interface registers are defined in Appendix F. For specific bit definitions, refer to that Appendix.

Concepts

The VMEbus interface on the EPC-8 is primarily for master accesses out onto the VMEbus. The only exceptions to this are the VXI-defined registers accessible in the A16 space discussed in the previous chapter. There is no slave memory accessible in the A32 or A24 address spaces.

VMEbus accesses are performed in either of two ways. For real-mode operating systems, a 64K “window” is provided in high memory accessed at 0E0000-0EFFFF. Any 64K region of the VMEbus (all address spaces) can be mapped behind this “E page” window such that the VMEbus address space is visible to the operating system memory map. For protected mode operating systems, the EPC-8 provides direct mapping of the VMEbus into the PC memory space above 256 MB.

Atomic access

The EPC-8 supports atomic access to the VMEbus data for data lengths not greater than 32 bits and only then if it is aligned to its natural boundary; for instance, 32-bit data must be aligned on a 32-bit address.

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Read-Modify-Write Operations

VMEbus RMW (read-modify-write) cycles can be performed through use of the LOCK instruction prefix with certain instructions. All of these instructions perform a read followed by a write. When such a read occurs that is mapped to the VMEbus, the EPC-8 treats it as the start of a VME RMW cycle. The next VME access from the CPU is treated as the write that terminates the RMW cycle. Keep in mind that accesses that cross a 32-bit boundary are actually performed as two accesses. For this reason, RMW accesses that cross a 32-bit boundary will not behave as expected. Also, many compilers will not actually generate a 32-bit access. Instead, two 16-bit accesses are generated. This can also cause an 32-bit RMW cycle to terminate prematurely with unexpected results.

Setting the VMEbus Access Bit

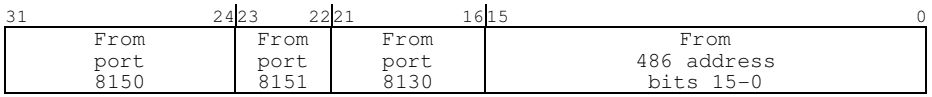
Before any VMEbus accesses can occur, the VMEbus access bit must be set. The EPC-8 provides two separate VMEbus access bits corresponding to the two access methods described above. Both of these access bits are part of the configuration register at port 8102h. In both cases setting the bit (1) enables accesses and clearing the bit (0) disables accesses. Bit 0 is used to enable direct VMEbus accesses above 256 MB. Bit 1 enables E-page accesses. In some cases, the programmer may wish to enable both access methods. However, if bit 1 is set (E-page accesses enabled), then the 64K of upper memory located from E000:0000 to EFFF:FFFF will not be available for use as system memory. If the application program is going to enable the E-page window, care must be taken to ensure that the Operating System will not be using this address space. Otherwise a memory conflict will occur that will cause the Operating System to fail at some point.

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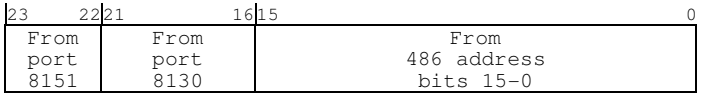
Real-Mode “E-page” VMEbus Accesses

The following summarizes the source of the VMEbus address lines for accesses through the “E” page.

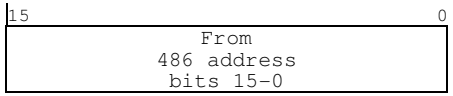
A32



A24



A16



It should be noted that the EPC-8 drives all 32 address lines even when performing an A24 or A16 access. Although the VME specification states that boards should not decode address lines outside their respective address spaces, some boards do anyway. Because of this, all “unused” high address lines should be set via their respective registers to all 1’s before a VME data transfer is executed.

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5 5

Supported Address Modifiers

The table below lists supported address modifiers:

29h	A16 non-privileged
2Dh	A16 supervisor
39h	A24 non-privileged data
3Ah	A24 non-privileged program
3Dh	A24 supervisor data
3Eh	A24 supervisor program
09h	A32 non-privileged data
0Ah	A32 non-privileged program
0Dh	A32 supervisor data
0Eh	A32 supervisor program

Table 5-1. Supported Address Modifiers.

Low-Level Programming “E” Page Accesses

Two examples are given here including both a verbal description and the Microsoft C source code for performing VMEbus accesses through the "E" page.

Example #1

Example #1 performs a 16-bit read from the VMEbus A16 space.

1. Set the VME E-page enable bit in Register 8102.

2. Determine the correct address modifier for A16 supervisory access (2Dh)

3. The unused address lines A31-A16 will be driven to unspecified levels when not being used.

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4. Set the access mode in the VME Modifier Register (8151) as follows:

VME WA23-22	BORD	IACK	AM5	AM4	AM2	AM1

(Note that register bits are not defined for the VMEbus address modifier lines AM3 and AM0 since, for all defined address modifier values in the VMEbus specification, AM3 is 1 and AM0 is the inverse of AM1. Therefore these two bit values are generated by hardware.)

Bits 7 & 6 Since the A16 space does not use VMEbus address lines A23 & A22, set these values to 1.

VME WA 23-22 = 11

Bit 5 Set the byte order to "little endian".

BORD = 0

Bit 4 Clear the IACK bit so this is not an interrupt acknowledge cycle.

IACK = 0

Bits 3-0 Use the address modifier (in binary form) to determine the appropriate values for these bits. 2Dh = 00**10**1**10**1b

Bit 3 (Address Modifier bit 5) = 1
Bit 2 (Address Modifier bit 4) = 0
Bit 1 (Address Modifier bit 2) = 1
Bit 0 (Address Modifier bit 1) = 0

Thus, 8151 should be set to 1100 1010 or CAh.

5. Map the address.

Add the A16 address to the "E page" address

Addr ← segment:offset + A16 address

6. Read the data.

Data ← value pointed to by Addr

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Microsoft C code for Example 1 -

```
#define WORD  unsigned short
#define LWORD unsigned long

WORD addr;   /* 16-bit A16 address */
WORD data;
WORD far * wptr;

outp(0x8102,(inp(0x8102)|2)); /* set VME E-page enable access bit */
outp(0x8151,0xCA);  /* Set address modifier to A16 supervisory access */
wptr = (WORD far *) (0xE0000000L + addr);
data = *wptr;       /* Read through window */
```

Example #2

Example #2 performs a byte (8-bit) write into the VMEbus A32 space. Here the upper 16 bits of the VME address need to be stored in the appropriate registers.

1. Set the VME E-page enable bit in Register 8102.
2. Set register 8150 with the value corresponding to the 8 high-order address bits.

VMEbus Address bits 31-24 WA31-24

3. Determine the correct address modifier for A32 supervisory access.
4. Calculate the value and set register 8151 as follows:

VME WA23-22	BORD	IACK	AM5	AM4	AM2	AM1

Bits 7 & 6	VME address bits 23-22
Bit 5	BORD = 0
Bit 4	IACK = 0
Bits 3-0	Bit 3 (Address Modifier bit 5)
	Bit 2 (Address Modifier bit 4)
	Bit 1 (Address Modifier bit 2)
	Bit 0 (Address Modifier bit 1)

5. Set register 8130 with the value corresponding to bits 21-16 of the VMEbus address with the two low order bits of the register set to 0.

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VMEbus Address bits 21-16	Res	Res

6. Map the address.

7. Write the data

Microsoft C code for Example 2 -

```
LWORD addr;   /* 32-bit A32 address */
BYTE  data;
BYTE  far * wptr;


outp(0x8102,(inp(0x8102)|2));   /* set VME E-page enable bit */
outp(0x8150,(WORD)(addr >> 24));        /* A31-A24 */
outp(0x8151,2 | (((addr << 8) >> 30) << 6));
  /* A23-A22 and address modifier for A32 supervisory data access */
outp(0x8130,(WORD)((addr << 10) >> 24);             /* A21-A16 */
wptr = (BYTE far *) (0xE0000000L + (addr & 0X0000FFFFL));
*wptr = data;                           /* Write through window */
```

The success of the access can be checked either by enabling BERR as an interrupt or by looking at the BERR bit in the event state register (8154) after each access.

Low-Level Handling of VMEbus Interrupts

The following is a description of how VMEbus interrupts (IRQ1-IRQ7), VXIbus message interrupts and error interrupts (BERR, ACFAIL, WDTG, etc.) should be handled on the EPC-8. Note that, in general, the use of EPConnect is highly recommended for handling interrupts.

- Enable the appropriate registers (VME Interrupt enable (8153) and VME Event enable (8155) registers) to allow the interrupts you want to respond to.

- Enable IRQ10 on the EPC's equivalent of the 8259 interrupt controller.

- A VXIbus message interrupt is generated when a master (this EPC-8 or another master) writes to the Message Low register (16-bit) from the VMEbus. A message interrupt does not occur when the EPC-8 writes to its own message register(s) from the PC I/O space.

- Keep in mind that while PC/AT interrupts are edge sensitive, VMEbus interrupts are level sensitive. As such, you must ensure that

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1) The 8259 interrupt controller is enabled to capture interrupts before a VMEbus interrupt occurs (otherwise VMEbus interrupts will be totally missed) and

2) You must handle all pending VMEbus interrupts before returning from the interrupt handler.

- When an interrupt occurs, first acknowledge the interrupt to the PC/AT 8259 interrupt controllers by sending both interrupt controllers an End-of-Interrupt (EOI).

- You must make sure that your interrupt handler code is not re-entered while dispatching interrupts. Either all interrupts should be disabled or IRQ10 should be masked after doing the EOI to the interrupt controller. Remember to re-enable them prior to leaving the interrupt handler.

- If you are using DOS, you may need to switch to an internal stack. This may or may not be necessary in other environments and applications. You should also store the state of the VMEbus (i.e., current byte ordering, bus mappings and address modifiers) if you expect the state to change. Be sure to restore the state before leaving the interrupt handler.

Start of Loop

- Determine the source of the interrupt or event. This can be done by reading the VME Interrupt State register which should be ANDed with the VME Interrupt Enable register. As described above, the VME Event State register and VME Event enable register may also be potential sources for the generation of IRQ10. Keep in mind that all pending interrupts must be handled.

- If the interrupt is a VMEbus interrupt 1-7;

  Acknowledge the interrupt to the VMEbus device generating the interrupt as follows:

  1- Set the IACK bit in the VME Modifier register.

  2- Establish a byte-ordering for the status/ID to be read. Whether this is an 8-bit or 16-bit read is dependent on the card issuing the interrupt.

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3- The address modifiers and transfer length are dependent on the hardware generating the interrupt.

4- Perform a read of the VMEbus where the address being read reflects the interrupt level being responded to. Address lines A3-A1 must reflect the interrupt level in binary form. Multiply the interrupt level by 2 and use that as the address of the read operation.

5- After the read operation, clear the IACK bit in the VME Modifier register.

- If the interrupt is a VXIbus message interrupt, the interrupt is acknowledged and cleared by reading the appropriate register(s), followed by setting the WRDY bit in the VME Response register.

- Call your interrupt handling routine.

- Upon returning from the interrupt handling routine, go back to the beginning of the loop until no more interrupts are active. In other words, you must handle all other active interrupts. This includes all other interrupts and errors which come in prior to calling the interrupt handling routine as well as any new interrupts and errors which may occur during this process. Only when all interrupts and error conditions are handled may you return from the overall interrupt handler. Again, if you miss any interrupts or errors, no other interrupts or errors will be recognized.

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5 5

Protected-Mode Direct VMEbus Accesses

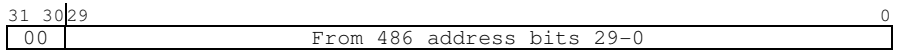
Addresses above 256 MB map directly onto the VMEbus. When direct "protected-mode" addressing of A24 or A16 space, the high-order nibble is used to define the access mode and byte ordering. For A32 space, the high-order 2 bits define the access mode leaving 30 bits available for addressing. Thus, only the first 1 Gigabyte of VMEbus A32 space is directly addressable. All A24 and A16 space is directly addressable. The chart following shows how this direct mapping is used.

VME access is enabled by two bits in register 8102. Bit 1, if set, enables the E-page access mechanism, and bit 0, if set, enables the 32-bit access mechanism. If the E-page mechanism is disabled, then the E-page is available for EXMbus options that require more DOS memory below 1MB. The type of VME access performed by the EPC-8 is a function of the address supplied.

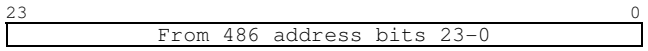
Address Range	Access Mode & Access Modifiers	Byte Order
1xxx0000 - 1xxxFFFF	A16M, AM = 1,0,1,~A25,A24,~A24	little endian
2x000000 - 3xFFFFFF	A24M, AM = 1,1,1,~A25,A24,~A24	little endian
40000000 - 7FFFFFFF	A32M-Supervisor (AM = 001101)	little endian
80000000 - BFFFFFFF	A32M-Supervisor (AM = 001101)	big endian
Cxxx0000 - CxxxFFFF or DxxxFFFF - DxxxFFFF	A16M, AM = 1,0,1,~A25,A24,~A24	big endian
Ex000000 - ExFFFFFF	A24M, AM = 1,1,1,~A25,A24,~A24	big endian

When accessing the VMEbus in this manner, the source of the VMEbus address lines is defined below.

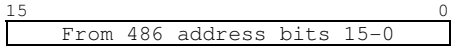
A32



A24



A16



The main purpose of the direct VMEbus access mechanism, as opposed to the E-page mechanism, is for multitasking 32-bit operating-system environments, where multiple tasks need to make VMEbus accesses. Without this, the tasks would have to coordinate their use of the E-page mapping registers.

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When using the EPC-8 this way to perform VMEbus accesses, you would typically set up the E-page window for interrupt acknowledge accesses. Also note that the direct access mappings do not cover the entire VMEbus A32 address range and do not provide all VMEbus-defined address modifier encodings, but you can use the E-page mechanism if needed to provide these.

Generating IACKs in Protected Mode

As noted in the description of protected mode direct VMEbus accesses, the values of address bits 24 and 25 determine the access mode. Setting bit 26 will cause an IACK (if the high-order address nibble is 1, C, or D, i.e., only in A16 direct access mode). Note that an IACK will override any of the other access modes.

With the EPC-8 programmers are not restricted to using the E-page in order to signal an IACK; direct VME memory access is possible. In protected mode you cannot access physical addresses -- only virtual addresses. Thus for addressing, map the flat 32-bit physical address to a virtual pointer.

To acknowledge a VME interrupt and acquire its 16-bit status/id:

Multiply the VME interrupt number by two and add the result to 0xC4000000.

Map the resulting physical address 0xC4000000 to a protected mode address.

Read the 16-bit status/id value from the resulting virtual mode address.

Whether or not a protected mode environment uses virtual memory is an attribute of the operating system, not of being in protected mode. There are protected mode environments that do not use virtual memory (like most DOS extenders).

Programming the Watchdog Timer

The watchdog timer on the EPC-8 can be set to either halt the system or reboot when a watchdog timer event occurs. The counter will cause a watchdog event after a specified time.

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Bits 1 and 2 of the Module Status/Control register (0x815D) are cleared by a ‘‘warm reset’’. This keeps the watchdog timer from expiring on a ‘‘warm reset’’ that is not initiated from a source other than a watchdog timeout. ENSYSO (bit 6 of 0x815D) also has to be cleared by the BIOS in response to warm resets to keep from losing the watchdog timeout bit while setting the BTOE bit (the VME Bus Timeout Enable bit).

The watchdog timer is enabled by setting the WDTR bit (bit 3 of register 815D). Note that a watchdog hardware reset results in a "warm" hardware reset. An I/O read to address 815D resets the counter.

To program the watchdog timer, follow these steps:

1. Determine if you want the watchdog timer to reset the EPC-8 or signal a watchdog timer event using IRQ 10. Use bit 3 in the Module Status/Control Register (815D). If set to 1, the EPC resets. If set to 0, the event is signaled.
2. Determine if you want the system to 1) halt or 2) continue rebooting on the watchdog timer event. From the EPC-8 BIOS Advanced Menu, choose which option you prefer enabled.
3. Set the speed of your watchdog timer. Options are 8.2 seconds, 128 mS, or 1.02 seconds. Use bits 1 and 2 of register 815D. Bit 1 is the slow timer and bit 2 is the fast timer. When used in conjunction, the settings are as follows:

   01 = 8.2 seconds
   10 = 128 mS
   11 = 1.02 seconds

The timer is reset to its maximum value by an I/O read of the module status/control register. Application software that utilizes this timer should take care to reset the counter just prior to enabling the interrupt bit in register 8155. This will inhibit a spurious timer event from occurring just after enabling the timer.

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Appendix A - Chip Set & I/O Map

The following defines the I/O addresses decoded by the EPC-8. It does not define addresses that might be decoded by EXMs and the EXP-MX.

First (8-bit) DMA controller: VLSI 82C486 chip emulating 8237 of PC/AT		
I/O Addr	Functional group	Usage
000	DMA	Channel 0 address
001		Channel 0 count
002		Channel 1 address
003		Channel 1 count
004		Channel 2 address
005		Channel 2 count
006		Channel 3 address
007		Channel 3 count
008		Command/status
009		DMA request
00A		Command register (R)
		Single-bit DMA req mask(W)
00B		Mode
00C		Set byte pointer (R)
		Clear byte pointer (W)
00D		Temporary register (R)
		Master clear (W)
00E		Clear mode reg counter (R)
		Clear all DMA req mask(W)
00F		All DMA request mask

First Interrupt controller: VLSI 82C486 emulating 8259 of PC/AT		
I/O Addr	Functional group	Usage
020	Interrupt controller 1	Port 0
021		Port 1

83443 controller:		
I/O Addr	Functional group	Usage
024	83443 Controller	Data register
026		Index register

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A A

Counter-Timer functions: VLSI 82C113A/114 emulating 8254 of PC/AT		
I/O Addr	Functional group	Usage
040	Timer	Counter 0
041		Counter 1
042		Counter 2
043		Control (W)

Keyboard Port: Intel 8242 emulating 8742 of PC/AT		
I/O Addr	Functional group	Usage
060	Keyboard controller	Data I/O register
061	NMI status	NMI status
064	Keyboard controller	Command/status register

Time-of-Day Clock: VLSI 82C486 emulating MC6818 of PC/AT			
I/O Addr	Functional group	Usage	
070	Real-time clock	RTC index reg / NMI enable	
071		RTC data register	
		0	seconds
		1	seconds alarm
		2	minutes
		3	minutes alarm
		4	hours
		5	hours alarm
		6	day of week
		7	date of month
		8	month
		9	year
		A	status A
		B	status B
		C	status C
		D	status D
		E	RAM
		...	
		3F	RAM

DMA Page Registers: VLSI 82C486 emulating 74LS612 of PC/AT		
I/O Addr	Functional group	Usage
081	DMA	Channel 2 page register
082		Channel 3 page register
083		Channel 1 page register
087		Channel 0 page register
089		Channel 6 page register
08A		Channel 7 page register
08B		Channel 5 page register
08F		Refresh page register

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Port A		
I/O Addr	Functional group	Usage
092	Port A	Fast A20 and reset control

EXM Configuration		
I/O Addr	Functional group	Usage
096	EXM Config	EXM slot register (part of the subplane)

Second Interrupt Controller: VLSI 82C486 emulating 8259 of PC/AT		
I/O Addr	Functional group	Usage
0A0	Interrupt controller 2	Port 0
0A1		Port 1

Second (16-bit) DMA Controller: VLSI 82C486 emulating 8237 of PC/AT		
I/O Addr	Functional group	Usage
0C0	DMA	Channel 4 address
0C2		Channel 4 count
0C4		Channel 5 address
0C6		Channel 5 count
0C8		Channel 6 address
0CA		Channel 6 count
0CC		Channel 7 address
0CE		Channel 7 count
0D0		Command/status
0D2		DMA request
0D4		Command register (R)
		Single-bit DMA req mask(W)
0D6		Mode
0D8		Set byte pointer (R)
		Clear byte pointer (W)
0DA		Temporary register (R)
		Master clear (W)
0DC		Clear mode reg counter (R)
		Clear all DMA req mask (W)
0DE		All DMA request mask
0EC		82C486 index register
0ED		82C486 data register

Coprocessor Interface: For the EPC-8 DX, DX replaces the 80287 of PC/AT		
I/O Addr	Functional group	Usage
0F0	Coprocessor	Clear coprocessor busy
0F1		Reset coprocessor

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Miscellaneous		
I/O Addr	Functional group	Usage
0EE	Fast A20	Dummy read enables Fast A20, dummy write disables Fash A20
0EF	Fast CPU reset	Dummy read resets the CPU
0F4	Slow CPU reset	Dummy write enables slow clock and non-turbo mode
0F5	Fast CPU register	Dummy write enables Fast clock and turbo mode
0F9	Configuration disable	Dummy write disables access to configuration registers
0FB	Configuration enable	Dummy write enables access to configuration registers

EXM Configuration		
I/O Addr	Functional group	Usage
100	EXM Configuration	EXM IDs (on each EXM module)
102		EXM option byte 1
103		EXM option byte 2

Ethernet		
I/O Addr	Functional group	Usage
240-25F	Default Ethernet registers (programmable)	

Serial I/O (Com2) Port: VLSI 37C651/6531 emulates 8251 of PC/AT		
I/O Addr	Functional group	Usage
2F8	COM2 serial port	Receiver/transmitter buffer
		Baud rate divisor latch (LSB)
2F9		Interrupt enable register
		Baud rate divisor latch (MSB)
2FA		Interrupt ID register
2FB		Line control register
2FC		Modem control register
2FD		Line status register
2FE		Modem status register

Parallel I/O (LPT1) Port: VLSI 37C651/653 emulates 8255 of PC/AT		
I/O Addr	Functional group	Usage
378	LPT1 parallel port	Printer data register
379		Printer status register
37A		Printer control register

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VGA		
I/O Addr	Functional group	Usage
3B4	VGA	CRT Controller index
3B5		CRT Controller data
3BA		Feature control output, Input status
3C0		Attribute controller Index/Data
3C1		Attribute controller Index/Data
3C2		Miscellaneous output, Input status
3C3		Sleep
3C4		Sequencer Index
3C5		Sequencer Data
3C6		Video DAC pixel mask, Hidden DAC register
3C7		Pixel address read mode, DAC state
3C8		Pixel mask write mode
3C9		Pixel data
3CA		Feature control readback
3CC		Miscellaneous output readback
3CE		Graphics controller index
3CF		Graphics controller data
3D4		CRT controller index
3D5		CRT controller data
3DA		Feature control, pinput status
3F0		Configuration 37C651 Super I/O Combo chip
3F1		Configuration 37C651 Super I/O Combo chip
46E8	VGA	Adapter Sleep

Serial I/O (Com1) Port: VLSI 37C651/653 emulates 8552 of PC/AT		
I/O Addr	Functional group	Usage
3F8	COM1 serial port	Receiver/transmitter buffer
		Baud rate divisor latch (LSB)
3F9		Interrupt enable register
		Baud rate divisor latch (MSB)
3FA		Interrupt ID register
3FB		Line control register
3FC		Modem control register
3FD		Line status register
3FE		Modem status register

EPC Registers		
I/O Addr	Functional group	Usage
8102	EPC-8	Peripheral Enables

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VME Registers		
I/O Addr	Functional group	Usage
8130	VME and Misc	VME map WA21-16

VXI Registers		
I/O Addr	Functional group	Usage
8140	VXI Registers	ID low
8141		ID high
8142		Device type low
8143		Device type high
8144		Status/Control low
8145		Status/Control high
8148		Protocol low
8149		Protocol high
814A		Response low
814B		Response high
814C		Message low low
814D		Message low high
814E		Message high low
814F		Message high high

VME and Misc		
I/O Addr	Functional group	Usage
8150	VME and Misc	VME map WA31-24
8151		VME modifier
8152		VME interrupt state
8153		VME interrupt enable
8154		VME event state
8155		VME event enable
8158		VME interrupt generator
815C		Unique Logical Address Register
815D		Module status control
815E		Signal FIFO lower
815F		Signal FIFO upper
8380		Flash low order address (if present)
8381		Flash low-middle address (if present)
8382		Flash high-middle address (if present)
8383		Flash data address
8384		Reserved
8385		Reserved
8386		Flash high order address (reserved)
8387		Battery status

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Appendix B - Interrupts and DMA Channels

B B

Interrupts

The assignment of interrupts for the EPC-8 is shown in the following table:

NMI	DRAM parity error, EXM expansion interface I/O channel check
IRQ0	timer
IRQ1	keyboard
IRQ2	IRQ8 - IRQ15 cascade through IRQ2
IRQ3	COM2 serial port
IRQ4	COM1 serial port
IRQ5	unassigned
IRQ6	usually needed for floppy disk controller
IRQ7	LPT1 parallel port
IRQ8	clock
IRQ9	unassigned
IRQ10	VME interrupt/event
IRQ11	unassigned
IRQ12	unassigned
IRQ13	coprocessor
IRQ14	used by IDE disk controller
IRQ15	unassigned

Table B-1. Interrupts.

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B B

DMA Channels

The assignment of DMA channels for the EPC-8 is shown in the following table.

0	unassigned (8-bit)
1	unassigned (8-bit)
2	usually needed for floppy disk (8-bit)
3	usually needed for SCSI disk (8-bit)
4	(Channel 0 - Channel 3 cascade through Channel 4)
5	unassigned (16-bit)
6	unassigned (16-bit)
7	unassigned - not connected to EXM expansion interface (16-bit)

Table B-2. DMA Channels.

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Appendix C - Connectors

This Appendix specifies the details of the connectors on the EPC-8. Please note, however, that all the connectors adhere to existing standards. The EXM expansion interface connectors are not defined here; their definition is available upon request. Connectors on EXMs and the EXP-MX are described in the separate manuals for those products.

Pins are labeled from the point of view of looking into the front of the connector on the EPC-8.

RS-232 Port (COM1)

The RS-232 serial port is a male DB-9 DTE connector.

Pin	Signal	Pin	Signal
1	Carrier detect	6	Data set ready
2	Receive data	7	Request to send
3	Transmit data	8	Clear to send
4	Data terminal ready	9	Ring indicator
5	Signal ground		

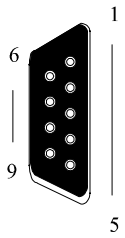


Table C-1. DB-9 Pin-Out.

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C C

RS-422/485 Port (COM2)

The modified RS-422/485 serial port is a female DB-9 connector.

Pin	Function
1	RTS
2	DTR
3	RXD-
4	TXD-
5	GND
6	CTS
7	DSR
8	RXD+
9	TXD+

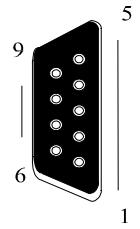


Table C-2. COM2 RS-422/RS485 Port Pin-out.

Parallel Port

The DB-25 LPT1 parallel port connector is defined as:

Pin	Signal	Pin	Signal
1	Strobe	14	Auto line feed
2	DB0	15	Error
3	DB1	16	Initialize printer
4	DB2	17	Select in
5	DB3	18	Signal ground
6	DB4	19	Signal ground
7	DB5	20	Signal ground
8	DB6	21	Signal ground
9	DB7	22	Signal ground
10	Acknowledge	23	Signal ground
11	Busy	24	Signal ground
12	Paper end	25	Signal ground
13	Select		

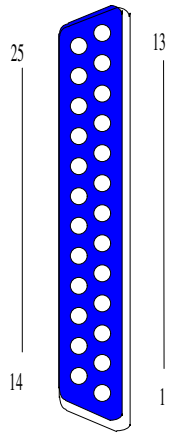


Table C-3. DB-25 Pin-Out.

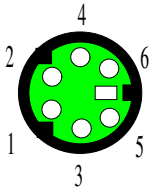
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Keyboard

The keyboard connector is a 6-pin DIN defined as:

Pin	Signal	Pin	Signal
1	Data	4	+5V
2	not used	5	Clock
3	Ground	6	not used
1	Reference voltage	2	Speaker tone

Table C-4. Keyboard Pin-Out.



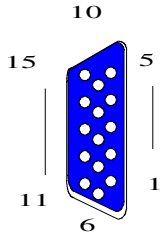


VGA Connector

The SVGA DB-15 monitor connector is defined as follows:

Pin	**Signal**	**Pin**	**Signal**
1	Red	9	(key)
2	Green	10	Ground
3	Blue	11	(not used)
4	(not used)	12	(not used)
5	Ground	13	Horizontal sync
6	Ground	14	Vertical sync
7	Ground	15	programmable output
8	Ground		

Table C-5. DB-15 Pin-Out.



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RJ45 Connector

The DTE RJ45 phone jack that supplies the 10-Base-T interface to the ethernet controller is defined in the following table:

Pin	Signal
1	Tx+
2	Tx-
3	Rx-
4	No connect
5	No connect
6	Rx+
7	No connect
8	No connect

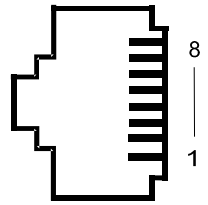


Table C-6. RJ45 Phone Jack Pin-out.

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Appendix D - Memory

☛ **DO NOT HANDLE THE EPC-8 OR MEMORY MODULES UNLESS YOU ARE IN A STATIC-FREE ENVIRONMENT.**

Memory

The EPC-8 has a single SIMM socket that can handle a SIMM as large as 16 MB. The memory configurations use a SIMM with the following specifications:

- 72 pin
- fast page mode
- 80 nanosec. (or better)
- single-sided or double-sided

For 4 MB,	Use a 1 MB x 36 SIMM. RadiSys P/N 70-0042 We recommend Toshiba THM361000ASG-80
For 8 MB,	Use a 2M x 36 SIMM. RadiSys P/N 70-0041 We recommend Toshiba THM362020ASG-80
For 16 MB,	Use a 4M x 36 SIMM. RadiSys P/N 70-0053 We recommend Toshiba THM364020SG-70

After upgrading the memory, reboot the system. An error message displays concerning memory. Press F2 to enter the Main Setup Menu. Verify that the memory size on this screen shows the correct amount of memory.

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NOTES



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Appendix E - Subplanes

Subplane Installation

A subplane is a printed-circuit board with connectors on both sides. A subplane provides several functions. Primarily it acts as the PC/AT bus. Additionally, it provides power from the VMEbus backplane to the EPC-8 and expansion modules.

Depending on the particular EPC-8 subsystem configuration, a specific subplane will need to be installed. Locate the appropriate subsection for the subplane you are using either by name or by picture. Follow the directions in the appropriate subsection.

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E E

EXP-BP1 Subplane

This subplane is used in the smallest configuration, where a single-slot EPC-8 processor is used by itself.

The EXP-BP1 is a rectangular-shaped board with two connectors, on on each side.

No backplane jumpers are required.

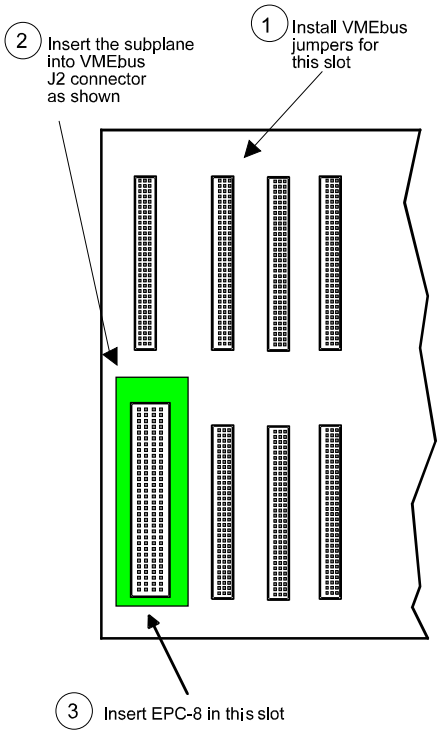


Figure E-1. EXP-BP1 Subplane.

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EXP-BP2 Subplane

This subplane is to provide connectivity for the processor and two EXM modules.

The EXP-BP2 is an L-shaped board with three connectors on each side.

After jumpering the backplane, plug the subplane into the VMEbus backplane such that the P2 connector on the back of the 4-row DIN is pressed into the J2 connector of the left-most VMEbus slot that the EPC-8 subsystem will occupy.

The lower EXM connector is denoted as EXM slot 0 and the upper as slot 1 as shown in the diagram. This information will be needed later when configuring the installed EXMs.

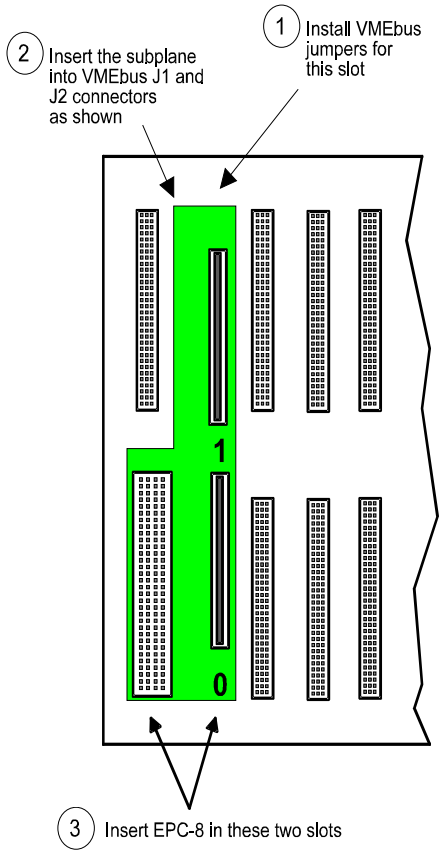


Figure E-2. EXP-BP2 Subplane.

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EXP-BP4 Subplane

The EXP-BP4 subplane is used to couple an EPC-8 processor module, two TXM modules, and an EXP-MX Mass Storage module.

The EXP-BP4 is a T-shaped board with four connectors on the front side and three on the rear.

After jumpering the backplane, plug the subplane into the VMEbus backplane such that the P2 connector on the back of the 4-row DIN is pressed into the J2 connector of the left-most VMEbus slot that the EPC-8 subsystem will occupy.

The EXM slot numbers are shown in the drawing.

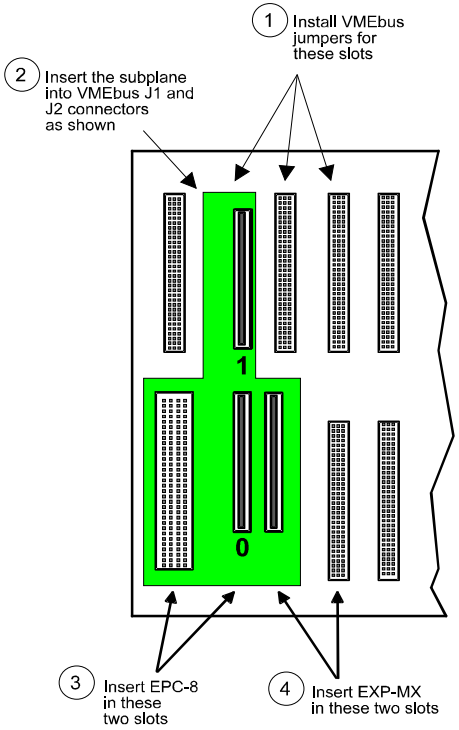


Figure E-3. EXP-BP4 Subplane.

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EXP-BP3A Subplane

The EXP-BP3A subplane allows for a processor and a total of four EXM modules.

The EXP-BP3A has five connectors on each side.

After jumpering the backplane, plug the subplane into the VMEbus backplane such that the P2 connector on the back of the 4-row DIN is pressed into the J2 connector of the left-most VMEbus slot that the EPC-8 subsystem will occupy.

The EXM slot numbers are shown in the drawing.

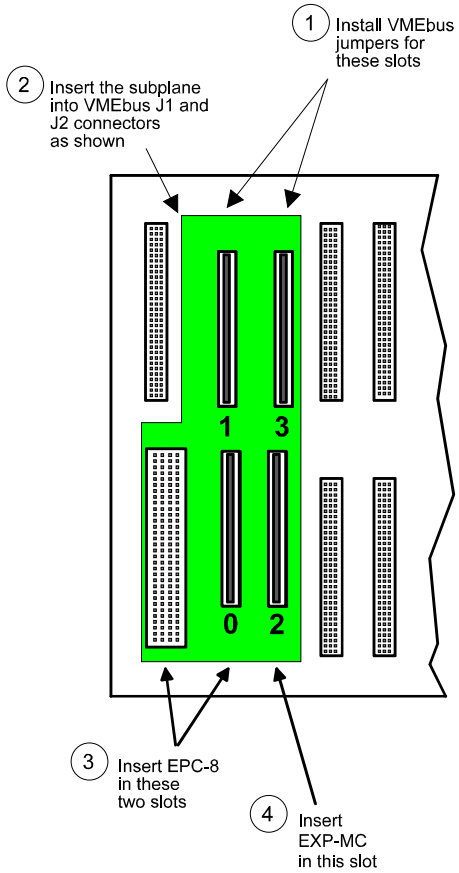


Figure E-4. EXP-BP3A Subplane.

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E E

EXP-BP5 Subplane

The EXP-BP5 subplane is used to build a system with a processor, four EXM modules, and an EXP-MX Mass Storage module. The EXP-BP5 has six connectors on the front side and five on the rear.

After jumpering the backplane, plug the subplane into the VMEbus backplane such that the P2 connector on the back of the 4-row DIN is pressed into the J2 connector of the left-most VMEbus slot that the EPC-8 subsystem will occupy.

The EXM slot numbers are shown in the drawing.

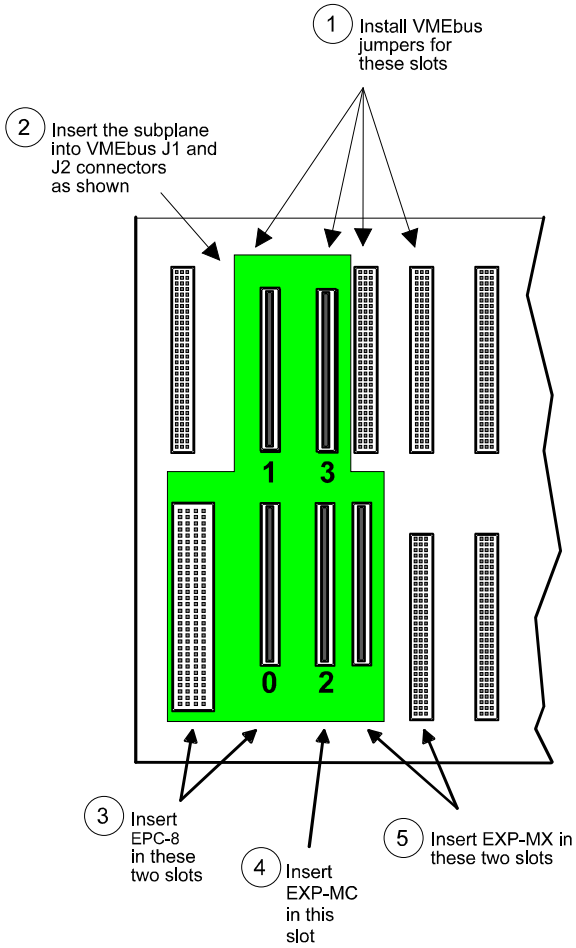


Figure E-5. EXP-BP5 Subplane.

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EXP-BP4A Subplane

The EXP-BP4A subplane is used in systems needing a CPU and six EXM modules.

The EXP-BP4A has seven connectors on each side.

After jumpering the backplane, plug the subplane into the VMEbus backplane such that the P2 connector on the back of the 4-row DIN is pressed into the J2 connector of the left-most VMEbus slot that the EPC-8 subsystem will occupy.

The EXM slot numbers are shown in the drawing.

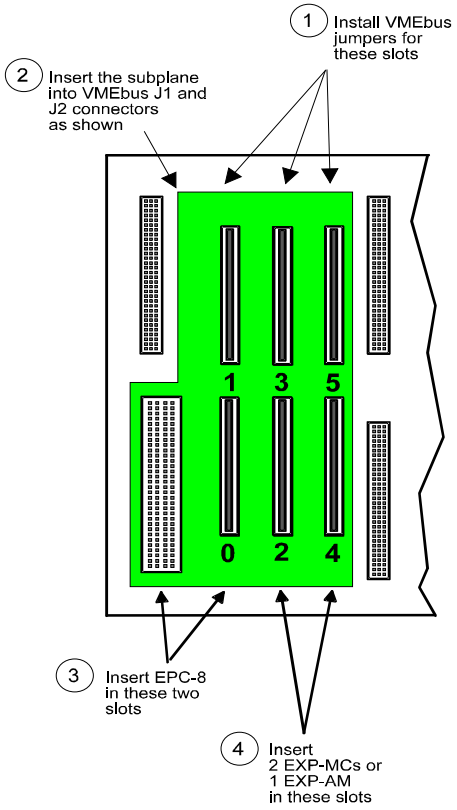


Figure E-6. EXP-BP4A Subplane.

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E E

EXP-BP6 Subplane

The EXP-BP6 subplane is used in a configuration with an EPC-8 processor module, six EXM modules, and an EXP-MX Mass Storage module.

The EXP-BP6 has eight connectors on the front side and seven on the rear.

Plug the subplane into the VMEbus backplane such that the P2 connector on the back of the 4-row DIN is pressed into the J2 connector of the left-most VMEbus slot that the EPC-8 subsystem will occupy.

The EXM slot numbers are shown in the drawing.

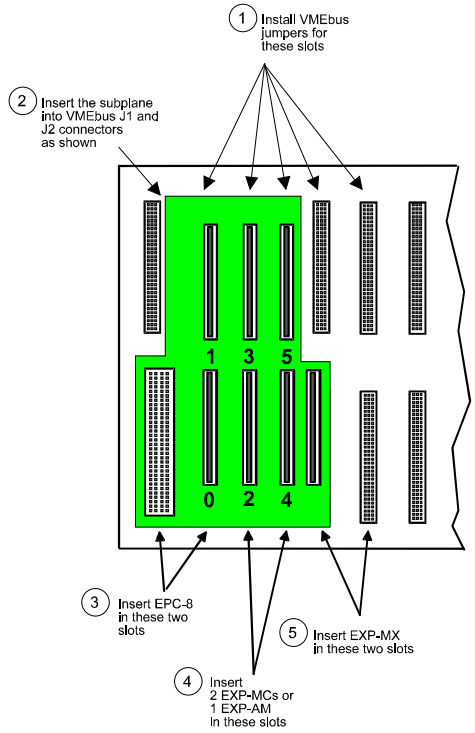


Figure E-7. EXP-BP6 Subplane.

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Appendix F - Registers

Registers Specific to the EPC-8

Registers in the I/O space that are specific to the EPC-8 are defined below. Only registers 0x8140-0x814F are "dual-ported" to both the PC and VME bus. The addresses shown below are used by the PC port. The VME addresses for the registers 0x8140-0x814F are described later.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	I/O Port
ARBPRI		RELM	ARBM	GPO	VGA	VME-E	VME-32	8102

Configuration

VMEbus Address bits 21-16						Res	Res	8130

VME A21-16 Address Register

1	1	1	0	1	1	0	0	8140

ID Register, lower

1	0	1	1	1	1	1	1	8141

ID Register, upper

1	1	0	0	0	1	0	0	8142

Device Type Register, lower

0	0	0	0	0	0	0	S	8143

Device Type Register, upper

SRIE	1	SYSC	1	READY	PASS	NOSF	SRST	8144

Status/Control Register, lower



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F F

0	MODID	SYSR	R	RESDET	1	1	1	8145

Status/Control Register, upper

1	1	1	1	1	1	1	1	8146

Reserved, lower

1	1	1	1	1	1	1	1	8147

Reserved, upper

1	1	1	1	1	1	1	1	8148

Protocol Register (read)/Signal FIFO (write), lower

0	0	0	1	1	1	1	1	8149

Protocol Register (read)/Signal FIFO (write), upper

R	RRIEN	1	SIG	MLCK	WRCP	FSIG	LSIG	814A

Response Register, lower

0	1	DOR	DIR	ERR	RRDY	WRDY	1	814B

Response Register, upper

1	1	1	1	1	1	1	1	814C

Reserved, lower

1	1	1	1	1	1	1	1	814D

Reserved, upper

RAM	814E

Message Low Register, lower (UART model)

RAM	814F

Message Low Register, upper (UART model)

VMEbus A31-24 Address register (WA31-24)	8150

Message A31-24 Address Register

VME WA23-22	BORD	IACK	AM5	AM4	AM2	AM1	8151

VME Modifier Register

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IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	MSGR	8152

VME Interrupt State Register

IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	MSGR	8153

VME Interrupt Enable Register

1	1	VMER	SIGR	WDT	ACFA	BERR	SYSF	8154

VME Event State Register

1	1	VMER	SIGR	WDT	ACFA	BERR	SYSF	8155

VME Event Enable Register

SLOT1*	1	1	1	1	INTERRUPT-OUT	8158

Interrupt Generator Register

ULA	815C

Unique Logical Address Register

DONE	ENSYSO	1	BTOE	WDTR	FWDT	SWDT	1	815D

Module Status/Control Register

RAM	815E

Signal FIFO, lower (read-only address)

RAM	815F

Signal FIFO, upper (read-only address)

Where a bit position has been described by a 0 or 1, the bit is a ROM bit, and writing to it has no effect. Unless otherwise noted below, all registers and bit values are readable and writeable.

Configuration (8102)

ARBPRI	RELM	ARBM	GPO	VGA	VME-E	VME-32

This register controls enables of the VGA controller and the VMEbus. Only the lower four bits in this register are cleared by an "AT reset" (that is, when the RESET button is pushed or WDT reset occurs or SYSRESET occurs). All eight bits are cleared by a power-on reset.



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VME-32 — VME 32-bit enable. If set (1), this bit enables VME accesses through the 32-bit addressing mechanism. When clear (0), this mechanism is disabled. This bit is automatically set by the BusManager software when using EPConnect. Please note the VMER bit (bit 5 of the VME Event State register), if asserted, will also disable this function, but does not clear the VME-32 bit.

VME-E — VME E-page enable. If set (1), this bit enables VME accesses through the DOS "E page". When clear (0), the E page is available for DOS use. This bit is automatically set by the BusManager software when using EPConnect. Please note the VMER bit (bit 5 of the VME Event State register), if asserted, will also disable this function, but does not clear the VME-32 bit.

VGA — VGA enable. If set (1), this bit enables the VGA controller. This bit powers up clear and if the BIOS detects another VGA controller in the system it is not set. Once this bit is set via write of "1" to this register only a hardware reset can clear it.

GPO — VGA General Purpose output control. This inversion of this bit is tied to pin 15 of the VGA connector through a 150 ohm resistor.



ARBPRI — Arbitration priority. This defines the level at which the EPC-8 will arbitrate for the VMEbus. 11 means 3, 10 means 2, 01 means 1, 00 means 0.

RELM — Bus release mode. If set, the bus release mode is ROR (release on request); otherwise it is the VXI RONR "fair requester" mode (request on no request).

ARBM — Arbitration mode. This bit is pertinent only if the EPC-8 is jumpered to be the slot 1 controller. If set, the EPC-8 is a priority arbiter; otherwise it is a round-robin arbiter.

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VME A21-16 Address Register (8130)

VMEbus Address bits 21-16	1	1

When an access is performed by the EPC-8 in its "E page" (address range 0E0000-0EFFFF), the access is mapped onto the VMEbus. The least-significant sixteen of the VME address bits are provided directly (from the 486), and the remaining 8 (for an A24 access) or 16 (for an A32 access) bits must come from somewhere else. Six of them come from this register. Bit 7 of this register is used as VME address bit 21, bit 6 as VME address bit 20, ..., and bit 2 as VME address bit 16.

The two low-order bits are ROM bits. For compatibility with older EPC's, this register is aliased at I/O port addresses 8132, 8134, and 8136.

ID Register (8140 & 8141)

1	1	1	0	1	1	0	0	Lower
1	0	1	1	1	1	1	1	Upper

This read-only register adheres to the VXIbus specification. It defines the EPC-8 as a message-based device and the manufacturer as RadiSys Corporation.



Device Type Register (8142 & 8143)

1	1	0	0	0	1	0	0	Lower
0	0	0	0	0	0	0	S	Upper

This register adheres to the VXIbus specification. The value defines the EPC-8 as having a model code of 0C4h if it is a slot 0 controller and 1C4h if it is not a slot 0 controller). Note that the S bit is a read/write bit that is configured by BIOS very early in the boot sequence. This bit may also be read/written from the VME port as well.

Status/Control Register (8144 & 8145)

SRIE	1	SYSC	1	READY	PASS	NOSF	SRST	Lower
0	MODID	SYSR	R	RESDET	1	1	1	Upper

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This register adheres to the VXIbus specification and also contains EPC-8 specific bits.

SRIE — SYSRESET input enable. If set, assertion of VME SYSRESET generates a reset of the EPC-8. One use of this bit is having EPC-8 software reset other VME devices (via bit SYSR) without resetting the EPC-8. This bit may be read/written from the PC port, but is read-only from the VME port.

SYSCLK — SYSCLK status bit. Only PC port writes to this register have the effect of clearing this bit. The bit is then set if four rising edges of the SYSCLK signal are detected. This bit is intended to be used to detect that SYSCLK is being generated on the backplane.

READY — This is a RAM bit defined by the VXI specification. In a VXIbus software environment, if READY=1 and PASS=1, the EPC-8 is ready to accept VXI-defined messages. This bit is read-only from the VME port and may be read/written from the PC port. This bit is also held clear while the SRST bit is asserted. When deasserting SRST via an I/O write to this register, a second write will be required to be able to reassert the READY bit since the READY bit is held in reset until just after the first write completes.

PASS — If set (1), the EPC-8 has completed its self test successfully. If this bit is clear, the Test LED on the EPC-8 front panel is lit. This bit is read-only from the VME port and may be read/written from the PC port. This bit is also held clear while the SRST bit is asserted. When deasserting SRST via an I/O write to this register, a second write will be required to be able to reassert the PASS bit since the PASS bit is held in reset until just after the first write completes.

NOSF — SYSFAIL inhibit. If set, the EPC-8 will not assert the VMEbus SYSFAIL line due to the PASS bit being cleared. If the PASS bit is clear and this bit is clear, then SYSFAIL will be asserted. SYSFAIL is also asserted when a Watchdog timeout reset occurs, independent of the setting of this bit. This bit may be read/written from both the VME and PC ports.

SRST — Soft Reset. Setting this bit places the EPC8 into the soft reset state. This bit may be read/written from both the VME and PC ports.

MODID — This read-only bit is connected to pin 30 in row A of the VMEbus P2 connector. If clear (0), it denotes that the pin is being pulled high. (This is used in VXI systems for module identification.) Note, this bit is defined but not implemented in the EPC-8 and will always return a value of 1. If future versions of the product need this capability it can be provided by installing a resistor.

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SYSR SYSRESET. The EPC-8 asserts the VME SYSRESET line while this bit is 1. When using this bit, it is the software's responsibility to ensure that the VME-specified minimum assertion time of SYSRESET is met. This bit may be read/written from the PC port, but is read-only from the VME port.

R A read/write bit that is available for software use (e.g. SURM).

RESDET This bit is cleared by a hardware reset. Once this bit is written to "1" from the PC-port (read-only from the VME port) it can only be set to zero by a hardware reset. This bit is used by the firmware to determine if a software or hardware reset is in progress and it set to "1" before any OS or application is invoked.

Reserved (8146 & 8147)

These registers are reserved and return all ones if read.

Protocol Register/Signal FIFO (8148 & 8149)

1	1	1	1	1	1	1	1	Lower
0	0	0	1	1	1	1	1	Upper



A read of this register from either the PC or VME ports reads the ROM constants stored in the protocol register. A write from either the PC or VME port writes the signal register.

The protocol register (the read value) defines the EPC-8 as being a servant and commander, having a signal register, being a bus master and an interrupter, not providing the shared-memory protocol, and not providing fast handshake mode.

When written from the VXIbus, this register is the signal register. The value written enters the signal FIFO (two deep) or returns a bus error (BERR) if the FIFO is already full.

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A write to the signal register is a happening of some significance for the EPC8, since it potentially asserts an EPC interrupt, shuffles a signal-register FIFO, and may return BERR if the FIFO is already full. For these reasons, the full semantics of writing to the signal register are discussed separately in a later section.

Response Register (814A & 814B)

R	RRIEN	1	SIG	MCLK	WRCP	FSIG	LSIG	Lower
0	1	DOR	DIR	ERR	RRDY	WRDY	1	Upper

This register contains some VXI-defined state bits associated with message handling, and several EPC-8 dependent bits. All of these bits may read/written (except where noted below) from both the PC and VME ports. Some of this bits may also be cleared by certain hardware events as described below.

DOR RAM bit available to software for VXI communication protocols.

DIR RAM bit available to software for VXI communication protocols.

ERR RAM bit available to software for VXI communication protocols.

RRDY Read ready. A 1 denotes that the message registers contain outgoing data to be read by another device. RRDY is cleared when the message low register is read.

WRDY Write ready. If set, the message registers are armed for an incoming message. When a write occurs into the message-low register, WRDY is cleared and the MSGR interrupt condition is asserted.

R RAM bit available to software.

RRIEN This EPC-8 specific bit is used to enable RRDY interrupt signaling. When clear (hardware reset state), only the deassertion of WRDY will cause the MSGR interrupt to be asserted. When set, the "OR" of the deasserted RRDY, WRDY bits is used to assert the interrupt. This bit would normally only be set for protocols that require multiple reply data to be sent in response to a single command.

SIG If this EPC-8 specific bit is 0, the signal register FIFO is empty. This bit is read-only.

MLCK This EPC-8 specific bit is used for synchronization of messages from multiple senders, something not provided for in the VXI specification. If 1, the message register can be locked for the sending of a message. If 0, the message register has been locked.

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WRCP This EPC-8 specific bit is a read-only copy of the WRDY bit.

FSIG Defined only when SIG=1, in which case FSIG is the number (0 or 1) of the register in the FIFO holding the earliest signal. This is a read-only bit.

LSIG Defined only when SIG=1, in which case LSIG is the number (0 or 1) of the register in the FIFO holding the most recent signal. This is a read-only bit

FSIG and LSIG have no utility to software. They exist as read-only bits for tests of the EPC-8 during manufacture.

The protocol for sending a message to the EPC, if there are multiple potential senders, is the following. The sender first reads register ABR (described in greater detail later). If both WRDY and MLCK are 1, he may then proceed to send the message; if not, he must spin or wait for this condition. For 16-bit messages, he writes into the Message Low register.

The bits RRDY, WRDY, and MLCK in the response register are altered by hardware-detected conditions. A read from the message-low clears RRDY. A write into all or the lower 8 bits of the message low register clears WRDY. A read from the VME bus port of the Alternate Bus Response register clears MLCK if WRDY is set. A read from the Alternate Bus Response register also returns the value in the Response register. Please note that the Alternate Bus Response register is accessed at offset 0x2A from the VME A16 base address of these registers.



Bits MLCK, DIR, DOR, ERR can be set or cleared by using a write to the response register from either the PC or VME ports. RRDY and WRDY may only set via a write to the response register. For these two bits, a 0 written into the respective bit position will not change the value of the register bit. A

1 written into the respective bit position will set the value of the register bit to 1.

Supporting software on the EPC must be aware of how to set the bits initially. The valid states are

RRDY	WRDY	MLCK	State
X	1	1	Write ready (awaiting incoming msg)
X	1	0	Write ready, locked by a sender
1	X	X	Read ready (outgoing data present)
0	0	X	Not ready for write or read

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Reserved (814C & 814D)

These registers are reserved and return 1s when read. Writes to these registers have no effect.

Message Low Register (814E & 814F)

RAM	Lower
RAM	Upper

There are actually two 16 bit registers at this address , outgoing and incoming 16 bit registers (UART model). A write from the PC side fills the outgoing register. This register can only be read from the VME port and when this occurs the RRDY bit is deasserted in the Response register. A read from the PC side reads the incoming register. The incoming register can only be written to from the VME bus port and when this occurs, the WRDY bit is deasserted in the Response register.

VME A31-24 Address Register (8150)



VMEbus A31-24 Address register (WA31-24)

This register is one of several that supply the VMEbus address bits when the EPC-8 makes an access in its "E page." This register supplies VME address bits A31-A24.

VME Modifier Register (8151)

VME WA23-22	BORD	IACK	AM5	AM4	AM2	AM1

This register is also used when the EPC-8 makes an access through its E page to the VMEbus. Bits 7 and 6 provide VME address bits A23 and A22, respectively. Bits 3-0 define the value placed on the associated VMEbus address-modifier lines. Register bits are not defined for the VMEbus address-modifier AM3 and AM0 lines since, for all defined address-modifier values in the VMEbus specification, AM3 is 1 and AM0 is the inverse of AM1. Therefore these two bit values are generated by hardware. Note that because AM3 and AM0 are hardware generated, the EPC-8 does not support user-defined address-modifiers.

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BORD Byte order. This bit controls the ordering of data bytes for D16 and D32 VMEbus accesses. If 0, the bytes are transmitted in little endian (Intel) order; if 1, byte-swapping hardware transmits the bytes in big endian (Motorola) order. Refer to the previous section in this chapter on byte ordering.

IACK This bit, when set, is used to define the VMEbus access as an interrupt acknowledge cycle. The interrupt being acknowledged must be encoded by software as a value on VME address lines A1-A3.

VME Interrupt State Register (8152)

IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	MSGR

This read-only register defines the state of the VMEbus and message interrupts.

IRQx If clear (0), the associated VMEbus interrupt line is asserted.

MSGR If clear (0), a message interrupt is being signaled. MSGR is clear if both bits RRDY and WRDY in the response register are clear.

VME Interrupt Enable Register (8153)

IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	MSGR

This is a mask of the interrupt conditions in the interrupt state register. A 1 denotes that the corresponding interrupt is enabled. If any bit in this register is a 1 and the corresponding bit in the interrupt state register is a 0, the EPC-8 IRQ10 interrupt is asserted. Software may then examine the interrupt and event state registers to determine the cause.

VME Event State Register (8154)

1	1	VMER	SIGR	WDT	ACFA	BERR	SYSF

Similar to the interrupt state register, this register defines additional conditions that may result in an IRQ10 interrupt. If the bit is 0, the condition is present. All bits are read-only except for the VMER and BERR signals.

ACFA VMEbus ACFAIL is asserted.



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BERR This bit is cleared (asserted low) when an access from the EPC-8 to the VMEbus is terminated with a BERR (bus error). It is also held clear when the SRST bit is set. This bit may be deasserted by writing a "1" (provided SRST is not asserted) into this bit position.

SYSF VMEbus SYSFAIL is asserted.

WDT Watchdog timer expired

VMER A SYSRESET or soft reset has occurred. This bit is held clear while SYSRESET is asserted or the SRST bit is asserted. This bit may be deasserted by writing a "1" into it once the reset conditions have been removed.

SIGR Signal register FIFO is not empty.

All bits are read-only except BERR and VMER. BERR is a sticky bit that is cleared whenever an access from the EPC-8 is terminated by a bus error or is held clear, and remains clear (0) unless changed by software (by writing any value to this register).

VME Event Enable Register (8155)

		VMER	SIGR	WDT	ACFA	BERR	SYSF

The low-order six bits are a mask of the interrupt conditions in the event state register. A 1 denotes that the corresponding event is enabled as an interrupt. If any bit in this register is a 1 and the corresponding bit in the event state register is a 0, the EPC-8 IRQ10 interrupt is asserted. Software may then examine the interrupt and event state registers to determine the cause.

VME Interrupt Generator Register (8158)

SLOT1*	1	1	1	1	INTERRUPT-OUT

This register is used to assert one of the VMEbus interrupt signals. If the INTERRUPT-OUT bits are zero, no interrupt line is asserted by the EPC-8. If lower three bits are set to 001, VMEbus IRQ1 is asserted. If set to 010, VMEbus IRQ2 is asserted, and so on. If and when an interrupt acknowledge cycle is sent to the EPC-8, the INTERRUPT-OUT bits are cleared. You can also deassert a previously asserted interrupt by writing 0 into the register. Finally, this register is cleared whenever SYSRESET* is asserted or when the SRST (soft reset) bit is asserted.

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Bit 7 of register 8158 is read-only and returns the value of the slot1 jumper setting . If the slot 1 shunt is installed (slot1 operation), then 0 is returned. If the slot1 shunt is not installed, then 1 is returned.

Unique Logical Address Register (815C)

ULA

This register contains the EPC-8's ULA. The ULA contents are used to map the EPC8's register set into VME A16 space as described below in the VMEbus Mapped Registers section. The ULA is changed by writing into this register or into the ID register.

Module Status/Control Register (815D)

DONE	ENSYSO	1	BTOE	WDTR	FWDT	SWDT	1

This register contains the following miscellaneous status and control bits: Only bit 3, WDTR, is cleared by a warm reset. All bits of this register, except for the read-only DONE status bit, are cleared by a power-on reset.

DONE This read-only bit is 0 whenever the EPC-8 has a VMEbus access outstanding. It is used for determining when a pipelined VMEbus write is complete.

ENSYSO This register bit, if set, will cause SYSRESET* to be asserted when any "warm" hardware reset (push-button reset, watchdog reset, SYSRESET* input, or low +5V resets) occurs on the EPC8. This bit is cleared during power-on reset only. Warm hardware resets do not clear it.

BTOE Bus timeout enable. Enables the slot-0 bus timeout timer. This is used by the BIOS.

WDTR Watchdog timer reset enable. If 1, expiration of the watchdog timer generates a reset of the EPC-8. If 0, only the WDT event is signaled. A read of the module status register should be performed before enabling the watchdog timer reset. This clears the watchdog counter to zero so that a PC reset does not occur immediately after enabling the watchdog timer reset.

FWDT Fast watchdog timer.



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SWDT Slow watchdog timer. FWDT and SWDT produce the following timeout values: 00 - disables events from the watchdog timer , 01 - 8.2 s, 10 - 128ms, 11 - 1.02 s.

A read of the module status/control register also has a side effect of resetting the watchdog timer. Therefore, if you are using the watchdog timer, the intention is that you are required to read this register within the defined period of the timer to prevent its generating an interrupt.

VMEbus Mapped Registers

The EPC-8 maps a standard set of VXI configuration registers onto the VMEbus A16 space and thus accessible by other VMEbus modules. These registers are 16-bit registers occupying 64 bytes of A16 space at a base address defined by the EPC-8's logical address.

The base address is

11aa aaaa aa00 0000

where aaaaa aaaa is the value of the ULA field in the response register at I/O port 815C.



The VME-mapped registers are a subset of those defined previously as I/O ports in the EPC-8. The registers are dual-ported in that they are accessible both from VME and from within the EPC-8 as ports in its I/O space. The VME mapped registers are defined below. Please note that the odd addresses from VME port will access the lower byte (registers addressed by even PC I/O addresses). The registers may be accessed using D08 and/or D16 accesses from the VME port.

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Offset from ULA	Upper byte	Lower byte
0	ID (8141)	ID (8140)
2	Device type (8143)	Device type (8142)
4	Status/control (8145)	Status/control (8144)
6	Reserved (8147)	Reserved (8146)
8	Protocol/Signal (8149)	Protocol/Signal (8148)
A	Response (814B)	Response (814A)
C	Message high (814D)	Message high (814C)
E	Message low(814F)	Message low(814E)
2A	Alternate Response	Alternate Response

The registers occupy the first 16 bytes of the 64-byte space, but DTACK (BERR in the case of an LWORD or Signal FIFO overflow access) will be signaled for accesses within the entire 64 byte region. Note that the registers may only be written by using the lower 16 addresses. Writes between address offsets 16-64 have no effect. For reads, the registers are aliased every 16 bytes (e.g. a read at offset 0x10,0x20,0x30 will return the data in the ID register). The lone exception to this rule occurs when accessing the Alternate Response register.

Reads and writes of the registers from VME and as I/O ports have identical results and effects except where noted in the register descriptions above.



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Appendix G - XFORMAT Software for the EPC-8

XFORMAT Software

XFORMAT is a utility program used to build DOS file structures on the EPC-8's optional resident flash memory. **XFORMAT** is also used to build file system images that can be used in VME RAM disks.

For complete information about **XFORMAT**, refer to *the XFORMAT Software User's Manual*.



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Appendix H - AUTOSET Software

AUTOSET Software

The **AUTOSET** program is used to configure the Ethernet controller. Since this may be set up by your supplier, you may never be required to use this program. The software is contained on the optional **Net 1** software diskette that is an optional item for the EPC-8. The **AUTOSET** program must be run from DOS or a DOS shell and enables the following actions:

- Select one adapter to be configured. Up to four adapters may be installed.
- Manually select configuration options (such as I/O base address and IRQ) for a specific installation.

If configuring multiple Ethernet controller cards in a single system, refer to the section, "Configuring Additional Ethernet Controllers."

Installing the Software

Under DOS 5.0 or higher, or in a DOS window, insert the optional **Net1** distribution diskette in the floppy drive and switch the command line to that floppy drive.

The DOS **INSTALL.BAT** file creates a subdirectory on the hard disk and copies the collection of software drivers and configuration files from the distribution disks to the hard disk. Type **Install** and press Enter. Note that **AUTOSET** can be run from a floppy disk drive.

The **Net1** distribution diskette contains the setup program **AUTOSET**, and a collection of drivers for various network interfaces and operating systems.

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Using the AUTOSET Program

Make sure that network software is **NOT** currently running on the computer system. If network software is running, reboot or unload the network software.

To start the program, move to the Ethernet controller subdirectory and type **AUTOSET**, then press Enter. The menu depicted in the figure below displays.

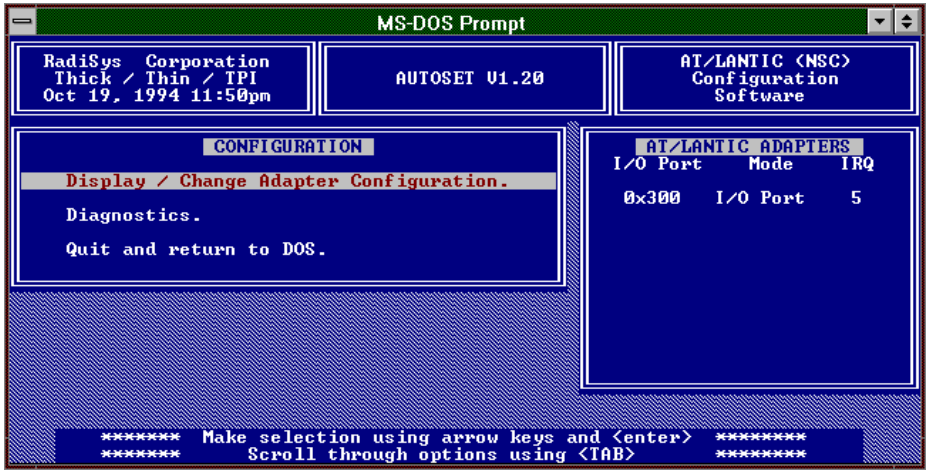


Figure H-1. AUTOSET Program Main Menu.

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The following options are in the main menu: Display/Change Adapter Configuration, Diagnostics, and Quit.

To initialize an Ethernet controller for the first time, to change the configuration, or to configure multiple Ethernet controllers, select "Display/Change Adapter Configuration" in the main menu.

To diagnose problems or verify the configuration, select "Diagnostics."

Note: If more than one Ethernet controller requires configuration for the first time, see the section *Configuring Additional Ethernet Controllers*.

Configuring an Ethernet controller with AUTOSET

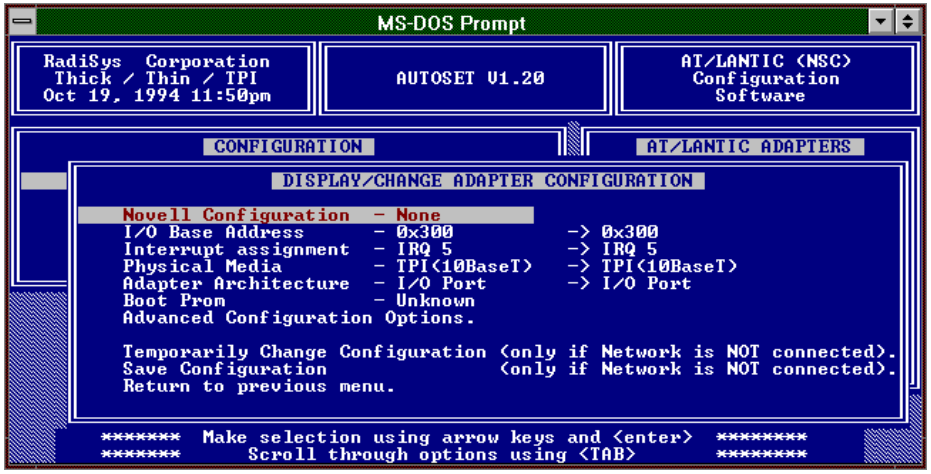


Figure H-2. Manual Configuration Menu.

For a single Ethernet controller installation, follow these steps:

1. From the **AUTOSET** program, select "Display/Change Adapter Settings" to set up the Ethernet controller just installed.
2. Skip the Novell Configuration prompt. It does not apply to the EPC-8.
3. Select the I/O base address. Use the tab key to change the Ethernet controller's I/O base address to any available location. **Note: 300**h is recommended because it allows the use of most network software drivers without modification.

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4. Select the Interrupt Assignment. Be sure to avoid any interrupts used by other interfaces in the system.
5. Select the Physical Media cabled up: only 10-Base-T is available for the EPC-8.
6. Select the Adapter architecture. Use "I/O Port" for NE2000 mode, or use "Shared Memory" for Western Digital mode.
7. Skip the Boot PROM prompt. It does not apply to the EPC-8.
8. Save the configuration to the on-board memory only if your system is currently not connected to the network. If you are experiencing difficulties, save as *temporary* changes to determine if they work correctly, then run **AUTOSET** again and save the changes as *permanent*.
9. Run Diagnostics to verify the setup. If using Western Digital mode, specify a shared memory base address to be used during diagnostics. Also, to guard against conflicts, exit Diagnostics and check that any EMM386 entries in the **CONFIG.SYS** file and **SYSTEM.INI** file (if using Windows) both exclude the memory assignment to the Ethernet controller. The default memory exclusion range is DC00-EFFF. If the system does not pass the Diagnostics, try again, changing the indicated parameters.
10. Press ESC to return to the previous menu.

If only one Ethernet controller is to be installed, the configuration procedure is complete. Exit the **AUTOSET** program and turn to Appendix K, *Configuring the Ethernet Drivers*.

The responses entered from the **AUTOSET** configuration menu depicted in the previous figure are discussed in detail below.

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Novell Configuration

There are several pre-set Novell Configuration options programmed into the **AUTOSET** program that are not applicable to the EPC-8. The Novell Configuration option must be set to None.

I/O Base Address

The Ethernet controller uses 32 bytes in I/O space. The I/O Base Address **must** be selected using the **AUTOSET** program. The **AUTOSET** program can only access the Ethernet controller when the I/O space occupied by the Ethernet controller does not conflict with I/O space previously assigned. In addition, the network interface drivers used with the Ethernet controller must use the same I/O base address parameter as the Ethernet controller.

The Ethernet controller is programmed at the factory with a default I/O base address of **300**h. If necessary, use the tab key to choose an optional address according to the guidelines set out in the following sections. **AUTOSET** allows selection of the following I/O base addresses: 240h, 280h, 2C0h, 300h, 320h, and 340h.

> **Warning:** If the Ethernet controller is mistakenly programmed to use an I/O address that conflicts with another I/O device, the **AUTOSET** program will not pass the diagnostics test. In this case, disable the other device or select a different I/O address for the Ethernet controller. For example, an Ethernet controller installed in an EPC system that also contains an EXM-16 SCSI controller must not be set to I/O base address **340**h.

Adapter Architecture

The Ethernet controller has up to 16K bytes of shared memory buffer. The default shared memory base on the Ethernet controller is DC00h.

If using the DOS expanded memory manager or Microsoft Windows, be sure to exclude the area of memory reserved for the Ethernet controller base memory.

For instance, if the Ethernet controller shared memory selected is 16K bytes and is located at DC00h, when you finish using **AUTOSET**, include the following statement in the **CONFIG.SYS** file:

device=c:\dos\emm386.exe x=dc00-dfff ... *other parameters* ...



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For Microsoft Windows, include the following statement in the [386Enh] section of the **SYSTEM.INI** file:

```
EMMExclude=dc00-dfff
```

Note that the area excluded may be greater than that required by the Ethernet controller due to other system requirements. For example, VME and VXI EPCs also require excluding the E page (E000 to EFFF).

If you are unsure how to make these changes, refer to the *Microsoft DOS User's Guide and Reference* and *Microsoft Windows Operating System* manuals.

Interrupts

Use the tab key to scroll through the displayed options and select one of the listed interrupts. Note that **AUTOSET** lists all interrupts, not simply those that are available. Use the Diagnostics routine in **AUTOSET** to detect invalid interrupts and IRQs.

Physical Media

The only physical media option for the Ethernet controller on the EPC-8 is 10-Base-T.

Adapter Architecture

There are two options for the method of data exchange between the CPU and the Ethernet controller. Use the tab key to toggle the displayed option and choose the I/O Port or Shared Memory for data exchange.

NE2000 and NE2000+ users should select the I/O Port mode.
WD8003 and WD8013 users should select the Shared Memory mode.

Systems with limited amounts of memory should select I/O Port mode to avoid conflicts with other memory-mapped devices.

Systems with ample memory, where increased performance is important, should select Shared Memory mode.

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Boot PROM

(This option is for systems with an EXM-10A installed. The EPC-8 does not support the boot PROM option of **AUTOSET**. Refer to the *EXM-10A Hardware Reference Manual* for more information.)

Configuring Additional Ethernet Controllers

To configure multiple Ethernet controllers for use in a single EPC, each Ethernet controller must be inserted in the computer and configured, **one at a time**, *before* inserting the next Ethernet controller. EXM-10A Ethernet controllers are shipped with the default I/O base address of 240h. A conflict occurs if more than one unmodified Ethernet controller is installed at a time. If I/O base address 240h is not available, disable the conflicting EXM and configure the Ethernet controller. To install more than one Ethernet controller, follow these steps:

1. Turn the EPC off, install one Ethernet controller, and turn the EPC on.
2. Modify the EXM configuration data using the BIOS setup screen.
3. Invoke the AUTOSET program and select "Display/Change Configuration."
4. Manually select an available I/O base address.
5. Specify the other configuration options for this Ethernet controller.
6. Run Diagnostics to validate the configuration options.
7. Save the configuration, then exit the **AUTOSET** program.

Repeat this procedure until all Ethernet controllers are installed and configured. Make sure that no parameter conflicts occur among the Ethernet controllers. With the exception of the last Ethernet controller configured, each card must be set to an I/O address other than 240h. That way, as each succeeding Ethernet controller is installed with its factory default of 240h, no conflict occurs with preceding Ethernet controllers. The software driver for each Ethernet controller must be configured to match that Ethernet controller's actual IRQ and I/O base address.

A unique I/O address for each Ethernet controller is required so that **AUTOSET** can distinguish which card is to configure. Two cards cannot share the same I/O base address; if they do, neither will be configurable. If this occurs, remove one card and change the I/O address on the one still in the system, then return the first card.

When using an EPC-8 with an EXM-10A installed, you cannot start **AUTOSET** while already connected to the network. The system will have to be logged off.



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Diagnostics

Once the LAN adapter is installed and cabled, use the **AUTOSET** diagnostic program to check the adapter installation.

Note that the **AUTOSET** diagnostic program test requires that the adapter be attached to a properly-terminated network or to a BNC "T" connector that has two terminators connected (if thin Ethernet is used). Once the cable is installed, use the **AUTOSET** diagnostic program to check the network interconnection.

Select the Diagnostics option in the **AUTOSET** menu. The Initialization and Diagnostics menu displays. The configuration options currently chosen are listed in parentheses. The following displays while several options are checked:

Network Interface Controller (12-byte node address)..... OK
Buffer Memory Check ..... OK
Check Cable Connection (Cable Connected)..... OK
Interrupt Assignment (5)..... OK
Boot PROM Check (No Boot PROM) ..... OK

Press ESC to return to the previous menu. If Diagnostics reveals an error, return to the Display/Change configuration menu and make the necessary changes. Run Diagnostics again.

Error Messages

The **AUTOSET** software has several associated error messages that may display during operation. These error messages are explained below.

Out of memory error

This message displays only during development and should never display during normal operation. If this message displays, contact RadiSys Technical Support.

No adapter at this address

This message displays when the address selected does not have an Ethernet controller network adapter card attached. Check the hardware to make sure the Ethernet controller is properly seated and functioning. If the message continues to display, select another address such as 300h, 280h, etc. If an address change does not fix the problem, the Ethernet controller should be replaced.

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Error - multiple boot ROM's detected
This error has been automatically corrected
Please re-power the PC to enable the corrections

This message displays when more than one installed Ethernet controller adapter has enabled a boot ROM. Only one network boot ROM should ever be installed in a PC.

To correct this, the adapter at the lowest address should remain enabled, and all other adapters should be set for no boot ROM. After saving the changes in the software, invoke a hardware reset - either push the reset button, or turn the system off, wait ten seconds, then turn it back on.

Boot PROM changes occur only after cold boot of PC

This message displays following a saved change to the boot ROM configuration. Boot ROM changes are not in effect until a hardware reset is initiated - either push the reset button, or turn the system off, wait ten seconds, then turn it back on.

Error - no new adapter

This message displays when the user has attempted to enable a disabled Ethernet controller, but the software never found the disabled adapter. Either the address is wrong or the adapter card is faulty.

No interrupt available for configuration

This message displays when there is no free interrupt to assign to the Ethernet controller. The only solution is to determine where all the interrupts are configured, and to free an interrupt that is redundant or unnecessary.

Cannot initiate an adapter with a disabled interrupt

This message displays when a disabled interrupt has been selected. Retry with a valid interrupt selection.

No NIC. DMA Failure

These messages display when a fault is detected in the AT/LANTIC ™ chip on the Ethernet controller. This is a fatal hardware error. Contact RadiSys Technical Support.



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Incorrect PROM ID Byte

This message displays when there is a hardware problem in the EEPROM. I/O mode is thus disabled. Contact RadiSys Technical Support.

(xfer to memory)
(xfer from memory)

Failed after X bytes with X

These messages display if there is a problem during the Buffer Memory test. The first two messages highlight errors in the transfer of data. The third message identifies where the data transfer error occurred. This is a fatal hardware error. Contact RadiSys Technical Support.

Cable Disconnected
Cable Unterminated

These messages indicate faults in the cabling or connection. Check to see if the network cable is in proper working order, properly connected and terminated. If the connections are proper and the termination is acceptable, the cables are faulty. If the cable tests good in another system, the connection is faulty.

No Interrupt

This message displays during the Interrupt Assignment test if the interrupt selected is not active. Return to the setup function and select another interrupt listed as available.

Boot ROM Failed

This message displays during the Boot ROM Check if the boot ROM does not pass the checksum test. The user must replace the boot ROM.

Using AUTOSET on Large Systems

If you are using **AUTOSET** on a system with more than eight (8) EXM slots, you must use a switch when starting **AUTOSET** to tell it how many slots are present. For example, on a system with 20 EXM slots, enter the following:

```
AUTOSET /20
```


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Appendix I - SVGA

Video Controller Hardware

The EPC-8 contains an SVGA graphics controller using the Cirrus Logic SVGA GD54xx. This is connected to the CPU local bus to give the best possible graphics performance. SVGA memory is 512 Kbytes, resulting in the following resolutions:

640 x 480	16 colors
640 x 480	256 colors
800 x 600	16 colors
800 x 600	256 colors
1024 x 768	16 colors

The BIOS will not enable (using bit 2 of register 8102) the SVGA controller if another VGA/SVGA controller is enabled on the EXM expansion interface.

Display Drivers and Utilities Software

The SVGA Driver and Utilities Software is supplied by Cirrus Logic and has the following nomenclature (where X is the version number):

Product: GDS54XX-X-D143P
Software revision: 1.43
Document release date: March 28, 1994
Document revision: 1.43



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Introduction

This section provides operating instructions for user utilities and installation instructions for the display drivers supplied with your Cirrus Logic SVGA for the RadiSys EPC-8.

Before you begin

The following instructions assume that the user is familiar with DOS and certain DOS commands. Please review the associated DOS commands before performing the installation.

Notational conventions

Throughout this manual, the term 'DOS' refers to both MS-DOS and PC-DOS, except when noting features that are unique to one or the other.

Table I-1 shows the typographic conventions that are used throughout this section:

Type Style	Description
User Input	This text must be typed exactly as it appears. Text within brackets indicates certain keyboard keys (such as [Enter], [F10], etc.).
Bold	System output. Any message that is displayed by the computer.
ALL CAPITALS	Directory names, files and acronyms.

Table I-1. Notational Conventions.



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Easy installation

The installation utility is provided to facilitate the smooth installation of the display drivers and utility software. The installation program is menu-driven and allows you to select and install only those display drivers for software and applications currently in use.

It is important to note that some display drivers need to have the associated vendor's application program already installed on the system prior to loading the Cirrus Logic SVGA display drivers. In other cases, the loading of the display driver may be an integral part of the vendor's product installation process. Please review the driver product section below for specific instructions prior to running the installation program.

The installation utility is located on the diskette labeled **VGA Disk 1 of 2**. To install the desired display drivers and utilities, insert the diskette into the A: drive, type the following:

```
A:
INSTALL
```

Follow the instructions on the screen to install the listed display drivers. At any time you may press [ESC] to abort the installation process and go back to DOS.

Selected drivers are simply copied to the specified disk and directory. Applications may require additional installation as described in the Display drivers section of this manual.

Cirrus Logic BBS

If there are any newer versions of the software provided with your SVGA adapter, they will be available on the Cirrus Logic BBS. It is a WILDCAT! BBS. The phone number is (510) 440-9080. It can handle modems running up to 9600 baud. The modem should be set to NO parity, 8 data bits, 1 stop bit. Before you are able to download software, you must join the conference(s) for the product(s) that you are interested in.



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Utility software

Several utility programs are supplied with you Cirrus Logic SVGA software. The following section describes these utilities and how to use them.

CLMode is a program used to configure it's various options.

SetRES lets the user change the operating resolution and the number of colors from within Windows.

The Display Power Manager for Windows 3.1 provides a mechanism to control the amount of power used by a computer's monitor.

CLMode

The CLMode utility allows the user to configure the panel options, define the type of monitor attached, and set the video modes supported by the Cirrus Logic chipset.

Using CLMode's menu-driven interface

At the DOS prompt type: CLMODE

The main popup window consists of a number of buttons. Each button represents a different option or menu. The underlined letter of a button name specifies the hot key combination for that item. For example, press the [ALT] and the underlined letter keys simultaneously or just the underlined letter key to select an option. Note that to use a mouse, a mouse driver should be installed prior to running the CLMode utility in order to use the mouse pointer for button selection.

Choosing the attached monitor type

Selecting the proper monitor type will allow the Cirrus Logic chipset to display the highest quality output that it is capable of with the attached monitor. The monitor type determines what video modes will be available to your system. It will also determine the vertical refresh rates available. Generally, the higher the refresh, the better the screen will look. A description of the available monitor types is given in the table at the end of this section.

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Select the Monitor Type button. The Monitor Type setup window will be displayed. The current monitor type will be highlighted initially. Use the cursor keys or the mouse to choose the type of monitor attached. Selecting the Advanced monitor type will enable you to customize the monitor timings for the monitor you are using.

To customize the monitor timings, use the mouse or the tab key to select the gray Set Advanced button. It will only be available if the Advanced monitor type is selected. This will bring up a new dialog box with drop down menus for each available resolution. Select the desired refresh rate for each resolution. Consult the manual for your monitor to discover the correct rate. When all of the settings are correct, select the OK button. If there are any problems or you change your mind, select the Cancel button.

Before saving the new monitor type, you may want to select the Verify button to view each of the new video timings that you have selected to verify that they are compatible with your monitor. After each test screen is displayed, press [Enter] or the left mouse button to see the next video mode. If there is a problem, press [ESC] or the right mouse button will return you to the Monitor Type Setup dialog box. Try a slower setting for the resolution that did not work and try verifying your choices again.

Once you are sure that everything is correct, press the Save button to set the new monitor type. Press the Cancel button to discard any changes. Press the Help button to get a detailed explanation on the monitor types and the VGA refresh rates.

On some systems the monitor type will be remembered from one session to the next. To test this, select a monitor type and exit the CLMode program. Turn the computer off for ten seconds. After rebooting the computer, run CLMode and verify whether or not the monitor that you selected is still enabled. If it is, it should not ever need to be set again in normal use. If the monitor type was not kept then you should select the option to have CLMode save the monitor type in your **AUTOEXEC.BAT** file. You will be given this choice after selecting the Save button.

Available video modes

Select the Video Modes button. The Video Modes Preview window displays all the modes supported according to the monitor type attached and the amount of video memory present. This list of video modes will tell you which are available in your current configuration for use with extended resolution drivers. To see what different video modes look like on your monitor, select the Preview button. After each test screen is displayed, press [Enter] or the left mouse button to see the next video mode. If you don't want to see any more video modes press [ESC] or the right mouse button will return you to the Video Modes Preview window.



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Centering adjust

Centering is available while in Video Modes Preview (only for extended Graphics modes 58h and greater). While in Preview, you have the option to use the Right/Left/Up/Down arrow keys to adjust your screen accordingly. The screen adjustments have predefined limits, and in some cases, the limit for the right side adjustment for some modes will have already been reached when entering the Preview mode. In that case, no right side adjustment will be allowed. Once a mode has been adjusted, the new values for horizontal and/or vertical positioning are saved within CLMode. When exiting from CLMode, you are prompted on whether you want to save these new parameters to TSR (**CENTER.COM**). If you choose to do this, the values to be used for the adjusted modes are stored in **CENTER.COM** on exit. **CENTER.COM** can then be loaded outside of CLMode. Once this is accomplished, all the modes which you have adjusted will be the active modes set when that mode request is made. To unload **CENTER.COM**, you must change the MONTYPE currently set in CLMode. This will unload **CENTER.COM** and uninstall all centering adjustments previously redefined. To save new centering adjustments for a different MONTYPE, repeat the above procedure as before. Your new adjustments will be written into **CENTER.COM** over the previously defined adjustments.

An additional adjustment for monitor SYNC POLARITY is also available while centering is active. To adjust the polarity of the current mode, simply press the PgUp or PgDn keys (while in Preview) to cycle through the available options, (Vertical Sync Polarity/Horizontal Sync Polarity):

+/+, +/-, -/+, -/-

Note: Centering will not be allowed if **CENTER.COM** has been loaded. You must unload **CENTER.COM** before attempting to save new adjustments.

Limitations: You may only adjust and save 16 modes at a time to **CENTER.COM**. You must use BIOS version 1.30 or greater or centering will not be made available.

Retrieving the current controller status

The information in the main window displays the controller type, the BIOS version number and the amount of video memory present.

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Getting help

CLMode provides Help for the following items: Configuration, Monitor Type, Video Modes, Mouse, Keyboard and About CLMode. The Configuration help window explains the flat panel configuration options. The Monitor Type help window explains the different capabilities of each monitor type. The Video Modes help window defines the information given in the Video Mode window. The Keyboard and Mouse help windows explain how to use the keyboard and the mouse to make selections. The About window displays the Cirrus Logic copyright message and the CLMode version number.

Exiting the CLMode

To exit CLMode at any time, press the [Alt] and [F4] keys simultaneously, or click the left mouse button on the system button of the main window (i.e., the top left corner button of the window which is shown as a dot), or select the Exit button. When the CLMode utility exits, the current video mode, monitor type, and VGA refresh rate will be displayed.

Using CLMode's command line options

When command line options for **CLMODE.EXE** are given at the DOS prompt, the menu-driven windows will not be displayed. Instead, configuration, monitor type, video mode and refresh rate will be set at the DOS prompt. The command line options for **CLMODE.EXE are** listed below:

```
CLMODE {modenum} {m{montype} | {s n} }
```



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Where:

`{modenum}` mode number

`{montype}` monitor type

Valid monitor types:
0 VGA
1 8514
2 Super VGA
3 Extended Super VGA
4 Multifrequency
5 Extended Multifrequency
6 Super Multifrequency
7 Extended Super Multifrequency

`{montype}`	monitor type
t6=x(Hz)	640x480 @ (0 = 60, 1 = 72)
t8=x(Hz)	800x600 @ (0 = 56, 1 = 60, 2 = 72)
t1=x(Hz)	1024x768 @ (0 = 87i, 1 = 60, 2 = 70)
t2=x(Hz)	1280x1024 @ (0 = 87i, 1 = Not available)
s	List status information.

For example, to set video mode 3:

```
CLMODE 3
```

For example, to select custom monitor timings with 640x480 at 60Hz and 800x600 at 72Hz refresh type:

```
CLMODE t6=0 t8=2
```



Typing an invalid option will display the command line help text. Typing [S] as a command line option will display the current CLMode settings.

On the next page is a table of common monitor types and their associated values.

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Monitor Type	Examples	Horizontal Frequency (kHz)	Vertical Frequency (Hz)	Display Resolutions
0	IBM 8512, 8513, 8503	31.5	60	640x480
1	IBM 8514, 8515	31.535.5	60 43.5 - interlaced	640x480 1024x768
2	NEC 2A	31.535.2	60 56	640x480 800x600
3	NEC II	31.535.235.5	60 56 43.5 - interlaced	640x480800x 600 1024x768
4	NEC 3D	31.537.837.8	606043.5 - interlaced	640x480 800x6001024 x768
5	Sony CPD-1304, NEC 3FGx, Nanao 9065S, 9070U	31.5 48.0 48.048.0	60 72 6043.5 - interlaced	640x480 800x600 1024x768 1280x1024
6	NEC 4D, 4FG, Nanao T240i	31.5 48.0 56.048.0	60 72 7043.5 - interlaced	640x480 800x600 1024x768 1280x1024
7	NEC 5D, 5FG, 6FG, Nanao T550i, T560i, T660i, F550i, F750i,	31.5 48.0 58.348.0	60 72 7243.5 - interlaced	640x480 800x600 1024x768 1280x1024

Table I-2. Monitor Type Examples.



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SetRES

The SetRES utility runs under Windows 3.1 and allows the user to change the screen resolution, number of available colors, and to select either large or normal size fonts and system resources.

After new options have been selected, the user can either immediately restart Windows, in which case the new resolution will take effect immediately, or continue working in the current resolution, in which case the new resolution will take effect the next time Windows is started.

This application assumes that the Windows drivers have been correctly installed and configured using **Windows Setup**.

Installation

1. Start Windows.
2. In the **Program Manager**, choose **File Run**. Specify the diskette drive where the Windows Drivers and Utilities Diskette is inserted, and run the install program. For instance if the floppy is in drive A:, type A:\INSTALL
3. When prompted, specify the Windows directory.
4. Install and configure the actual Windows driver following the instructions in the Windows 3.1 section of this manual.

SetRES may now be run by selecting the **SetRES** icon. The first time that you run SetRES, the settings for the current driver won't be correct, but go ahead and set them once, and they will be correct from then on.

If you are unsure what resolutions and colors your video card can support, refer to the section of this manual on CLMode for information on how to determine available resolutions.

For help on the SetRES utility, select **Help** from the program menu.



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Power management screen saver

About the screen saver

The Display Power Manager for Windows 3.1 provides a mechanism to control the amount of power used by a computer's monitor. It provides a total of 5 levels of power savings.

The first level is a conventional screen saver that turns the screen black and bounces a logo around. The black screen provides substantial power savings and the animation lets you know that the computer is still active.

The other four levels of power savings are...

Reduced on mode - Reduced on mode is an optional power saving state that allows the computer to use some power savings while still fully operational. Currently this is limited to some portable computers that can lower the power usage on their LCD displays. This causes some degradation of display quality.

Stand by mode - Stand by mode is an optional power saving state that gives minimal power savings, but provides the fastest recovery time. It is enabled by blanking the screen and lowering the horizontal rate to less than 10 Hz with less than a 25% duty cycle. There is no change to vertical timing.

Suspend mode - Suspend mode is a mandatory state in which substantial power savings are achieved by the display. The trade off is that recovery times are longer than from stand by mode. It is enabled by blanking the screen and lowering the vertical rate to less than 10 Hz with less than a 25% duty cycle. There is no change to horizontal timing.

Off mode - Off mode provides the highest level of power savings and the longest recovery times. With this mode the display is actually turned off so that recovery times are equivalent to switching the monitor on. It is enabled by blanking the screen and lowering both the horizontal and vertical rates to less than 10 Hz with less than a 25% duty cycle.

They match the power saving modes defined by the VESA VBE/PM (see below) standard. As you move down from one mode to the next, the amount of power being saved is greater, but so is the amount of time that it takes for a monitor to recover and be ready to display data.



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The screen saver will cycle through all of the selected power saving modes one after another until the maximum selected power saving mode has been reached. The number of minutes that is specified for each level is the number of minutes after the previous mode has been enabled. It is not the total time before entering that mode.

Please refer to your Windows User's Guide for information on how to install screen savers in Windows.

PM.EXE

VGA BIOS versions prior to v1.40 do not include the function calls required to fully support the Display Power Management screen saver. To use these BIOS's with power management software requires that **PM.EXE** be executed before starting Windows 3.1. To run **PM.EXE** type

```
C:\WINDOWS\PM
```

Where C:\WINDOWS is the directory where Windows 3.1 is installed on your computer. For convenience, **PM.EXE** may be put into your **AUTOEXEC.BAT** file.

Special considerations

Some of these power saving modes are intended for specific display types, so not all of them are available on all video controllers. On some controllers, only the animated logo will be available.

For the power saving modes to have any effect beyond just blanking the screen, the monitor being used must have specific power saving features.

Note that if the screen saver is in any of the power saving modes, moving the mouse will not wake it up. This is different from normal screen savers and is used to keep the monitor from waking up because of accidents such as bumping the desk that the computer is sitting on. This is especially important if the password option is enabled, since once the password dialog box pops up, it stays there until the user turns it off. This is a limitation of the Windows 3.1 screen saver interface.

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Using the screen saver

When the screen saver is started, it will initially display a bouncing logo on a black background. To enable additional levels of power savings, select them from the **Screen Saver Mode** section of the Setup dialog box**.**

Screen saver mode

The **Screen Saver Mode** section has four check boxes in it. They are ReducedOn, StandBy, Suspend and Off. The screen saver detects the type of graphics controller that is being used and the types of power savings that it is capable of.

If the text immediately to the right of any of the check boxes is grayed out, that option is not available. If a power saving mode is available, then the text immediately to the right of the check box is black. If the box is selected with the mouse or the keyboard, the rest of the fields on the line will also turn black. If the check box is deselected, the other fields will turn gray.

The minutes field for each line can be changed only if the check box for that line is selected. The amount of time can be set for any number between 1 and 60. The number can either be typed directly, or by clicking on the up or down arrow next to the number. Holding the mouse button down on the arrow will quickly increase or decrease the minutes field.

The number of minutes that is specified for each level is the number of minutes after the previous mode has been enabled. It is not the total time before entering that mode.

Screen saver animation speed

The scroll bar controls how fast the animation moves. The checkbox controls whether or not a bouncing sound will be played whenever the logo hits an edge of the screen.

Password options

If the password checkbox is enabled, then the screen saver will prompt the user for a password before it quits. The password is the same one that is used for other Windows 3.1 screen savers.



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Display drivers

The Cirrus Logic video controller is 100% VGA compatible. The display drivers described in this manual are supplied to improve the resolution for each supported software application package.

The installation instructions for each display driver will follow the introduction section. Follow the instructions carefully to be sure that each display driver is correctly installed. All of the installation instructions assume that **VGA Disk 1 of 2** is located in drive A:. If drive B: is used, the instructions should be changed appropriately.

Before you begin

Not all video modes will be available on all systems. If an extended mode driver is installed for a video mode that is not available, the application program will not function properly. There are a number of things that determine the list of available video modes. Some of these include the current monitor type, the amount of installed memory, and the revision of the controller. To determine which modes are available before beginning the driver installation, it is recommended that the user run the CLMode program and examine the list of available video modes.

Microsoft Windows 3.1

Before upgrading from a previous release

Before installing the new drivers you should use Windows Setup to select the VGA or SUPERVGA video driver so that when you install the new drivers, there is no chance of overwriting the driver that Windows is using to control your screen. Next go to the system directory, and find a file that is named **OEM?.INF** where the question mark is a number. There may be more than one of these. These files are the different **OEMSETUP.INF** files that have been used to configure Windows for different devices. Using a text editor, such as Notepad or Edit, look at them until you find the one that is for the previous version of the Cirrus Logic video drivers and delete it. This is not completely necessary, but if you don't delete old files the drop down box for Setup soon becomes very cluttered with different versions of the same files. Also, in many cases the old files have been overwritten by newer ones, so no longer exist anyway.

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Installing Windows 3.1 display drivers

If you haven't already installed the SetRES utility program, these instructions will install a single driver for a single resolution. If you want to be able to easily switch between different resolutions, you should install SetRES before this procedure.

To install the Windows 3.1 drivers from the DOS prompt, proceed as follows:

1. Insure that Windows 3.1 is already installed on your computer.

2. From your Windows directory, at the DOS prompt, type SETUP to run the Windows **SETUP.EXE** program. Follow the instructions on the screen. When you come to the screen which lists the hardware and software components such as display adapter (e.g. VGA, CGA, etc.), keyboard type, mouse type, etc., go to the **Display** selection by using cursor keys to move the highlighted bar and press [Enter].
3. From the next menu listing of display options, scroll to the bottom of the list, and highlight the following text:

   Other (Requires disk provided by a hardware manufacturer)
   Press [Enter], and when prompted, insert the Windows Display Driver diskette into drive A:\ or B:\ and type A:\ or B:\[Enter].

4. You will see the list of drivers and their associated resolutions, such as:
   CIRRUS 54XX V1.4, 1280X1024X16
   CIRRUS 54XX V1.4, 1024X768X16
   CIRRUS 54XX V1.4, 640X480X16
   CIRRUS 54XX V1.4, 640X480X256
   CIRRUS 54XX V1.4, 640X480X64K
   CIRRUS 54XX V1.4, 800X600X16
   CIRRUS 54XX V1.4, 800X600X256

5. Highlight the desired choice by moving the cursor to the correct display driver, and then press [Enter].
6. Continue with the remainder of the setup procedure.



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To install the Windows 3.1 drivers from within Windows, proceed as follows:

1. Ensure that Windows 3.1 is already installed on your computer and start Windows.
2. From the **Main** window of the Program Manager run the Windows 3.1 Setup program.
3. Select **Change Systems Settings...** from the **Options** menu of Setup.
4. Click on the down arrow at the right side of the **Display**: line. Scroll to the end of the list of available display drivers and select **Other display (Requires disk from OEM)....**
5. Insert the Windows display driver diskette into drive A: and type A:\ as the pathname, then click on **OK.**
6. You will see the list of available drivers and their associated resolutions, such as:
   CIRRUS 54XX V1.4, 1280X1024X16
   CIRRUS 54XX V1.4, 1024X768X16
   CIRRUS 54XX V1.4, 640X480X16
   CIRRUS 54XX V1.4, 640X480X256
   CIRRUS 54XX V1.4, 640X480X64K
   CIRRUS 54XX V1.4, 800X600X16
   CIRRUS 54XX V1.4, 800X600X256
7. Highlight by moving the cursor to the desired display driver, and then click on **OK.**
8. Continue with the remainder of the setup procedure. The changes will not take effect until Windows is restarted.



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Appendix J - Error Messages & Diagnosis

Troubleshooting

This section deals with problems that you may encounter that do not provide an error message. If an error message is displayed, see the next section of this Appendix, *Common Error Messages*.

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Symptoms	Possible cause(s)	Solution
System appears to boot (evidenced by RUN LED being on, floppy and hard disk being accessed) but provides no video.	If not using the built-in VGA, then the EXM-based video adapter may not be fully seated in subplane.	Remove the video adapter. If the subplane is secured to the VMEbus backplane by retaining screws, verify that the subplane is not warped from over tightening the screws. Reinsert the video adapter and verify seating into the subplane.
	Monitor or cable problem (with or without onboard video).	Verify that the cable pins are not bent and the cable is fully seated in the video adapter. If necessary, try the monitor on another system to verify that the monitor is good.
	Subplane failure or other hardware failure (with or without onboard video).	Call RadiSys Technical Support.
	EPC-8 cannot talk to EXM expansion interface.	Call RadiSys Technical Support.

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Symptoms	Possible cause(s)	Solution
System fails at power-up -will not run power-on self-test. May be accompanied by combinations of beep tones from the speaker.	The system is not getting power.	Check the backplane and verify that +5V power is good. Verify that the subplane is fully seated in the VME backplane and the EPC-8 is fully seated in the subplane.
	BIOS detected a failure	See *BIOS Beep Codes* table below.
	SIMM missing or loose.	Check that the SIMM is still present or connected.
	Hardware failure.	This cannot be diagnosed in the field. Call RadiSys Technical Support.
Serial port(s) do not work.	Bad power.	Verify that backplane +12V and -12V are good.
	Interrupt conflicts	An EXM module is using the same interrupts as COM1 and/or COM2. Verify that no other card in the EPC-8 subsystem is using IRQ3 or IRQ4.
	Port hardware failure.	Call RadiSys Technical Support.
System hangs during boot process (Master LED on; RUN LED off)	VMEbus has no Slot-1 controller providing bus timeout.	You are probably loading an expanded memory manager (for example, **EMM386.EXE**) in your **CONFIG.SYS** file. This can cause the system to hang if - there is no Slot-1 controller - the Slot-1 controller is not providing the proper bus timeout - the Bus Grant jumpers are not installed.

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Symptoms	Possible cause(s)	Solution
System will not talk across VMEbus.	The VMEbus backplane may not be jumpered correctly.	See the section *Installing the VMEbus Backplane Jumpers* in Chapter 2.
	More than 1 master may be set to provide Slot-1 functions.	Make sure that only 1 system is configured as the Slot-1 controller and that it is the left-most system in the chassis.
	There may be no Slot-1 controller providing bus arbitration.	Determine if the system is in the left-most position and that the Slot-1 controller jumper is set.
	EPC-8 or subplane may have bent pins.	Remove the EPC-8 and the subplane and verify that no pins are bent. Then reinsert the subplane and the EPC-8.
	VMEbus interface failure.	Call RadiSys Technical Support.

Table J-1. Troubleshooting Error Messages.

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BIOS Beep Codes

If the BIOS detects a critical error condition while running the Power On Self Test (POST) code, it may halt after issuing a beep code and attempting to display the error code in the upper left corner of the screen. The audible codes consist of patterns of beeps and pauses. If this occurs, you should contact your supplier for technical support.

Code	Beep Pattern	Condition
	1 short	POST OK
	2 short	POST error, such as EXM configuration or keyboard error. Refer to the message on the screen to determine the cause
	one long, two short	Insert BIOS update disk now.
	one long, three short	No video BIOS detected. Install a video EXM (EXM-13A, for example).
	3 short	BIOS update disk missing. Either insert the BIOS update disk or turn the system off and then back on.

Table J-2. BIOS Troubleshooting Beep Codes.

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Common Error Messages

This section contains a summary of error and warning messages alphabetized by message text. These are messages generated by the BIOS and MS-DOS that may be related to your hardware configuration.

Bad or missing command interpreter

Problem: The DOS operating system cannot find the Command line interpreter.

Solution(s): Either **COMMAND.COM** is not present at the specified (or default) directory level of the boot disk or the "SHELL=" statement in your **CONFIG.SYS** lists the file incorrectly (wrong directory or misspelled).

Operating system not found

Problem: No boot disk could be found.

Solution(s): This could occur in several different ways.

Your hard disk may not have been partitioned into logical drive(s). PCs look for logical drives to boot from. Hard disks are physical drives; partitions are logical drives.

Your BIOS setup screen has all disks disabled, or if your hard disk is disabled and no floppy diskette is inserted in the A: drive. Or the hard disk drive has no active partition set. Run the BIOS setup program and verify that all disk parameters are correct. If they are, insert a bootable floppy disk in the A: drive and press enter. If a hard disk is present, verify that it is properly partitioned and formatted as a system disk and one partition is set active.

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Diskette drive A error or **Diskette drive B error**

Problem: The floppy diskette(s) installed in the system do not match the configuration information listed in the BIOS setup screen. This may be due to incorrect entries in the BIOS setup screen or one or both drives may not be responding at power-up.

Solution(s): Run the BIOS setup program. Make sure the BIOS setup entries relating to floppy drives correctly reflect the attached floppy drives. If you are using the EXP-MX module, drive A should be set to "1.4M". If no second floppy drive is attached, set drive B to NONE. If you have no floppy drives, both drive A and drive B should be set to none.

Also, verify that all floppy drives are firmly connected (via subplane or ribbon cable) and that each drive has power.

If you are using an external floppy drive via a front panel connector, verify that the end of the ribbon cable is not shorting to the front panel and pin 1 on the front panel connector is connected to pin 1 on the drive.

Failure - Fixed Disk 0

Problem: The IDE disk controller for drive C cannot be initialized.

Solution(s): If you are using an EXP-MX mass storage module, ensure that the module is fully seated in the subplane and that the +5V and +12V LEDs indicate that the module has power.

If you are using the EXM-9 to cable to an external disk, make sure that you have power to the disk, the ribbon cable is good and correctly oriented, and that the end of the ribbon cable is not shorting to the front panel of the EXM-9.

If you are not using an IDE drive, run the BIOS setup program. Change the drive type to match the device being used.

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EXM configuration error (with two short beeps)

Problem: The EXMs installed (or not installed) do not match the configuration information in the CMOS Setup.

Solution(s): Run the BIOS setup program. Enter the EXM menu. Verify the information listed on the screen, save any changes and reboot. If necessary, refer to the Chapter 3, *BIOS Configuration* of this manual and/or your EXM manual(s) for more details.

General failure reading drive ...

Problem: This almost always indicates the presence of an unformatted hard disk partition or diskette.

Solution(s): Format the partition or diskette using the utilities supplied by your operating system.

Incorrect Drive A type - run SETUP or **Incorrect Drive B type - Run SETUP**

Problem: Type of floppy drive (A: or B:) not correctly identified in BIOS Setup.

Solution(s): Run BIOS Setup and validate correct settings. Also, see "Diskette drive A error" above.

Invalid drive specification

Problem: You are trying to access a logical drive (e.g., A:, B:, ...) that is not known to the operating system.

Solution(s): Select a different logical drive. If you are trying to access a hard disk, you may need to create the logical partition.

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Keyboard error (with two short beeps)

Problem: This message indicates that the system did not recognize a keyboard at power-up or you pressed a key during the power-on self test.

Solution(s): Check the integrity of the keyboard connector.

If you think you pressed a key during power-up, reboot the system using the front panel reset button.

Some keyboards are designed with a switch (or jumper) to allow the user to configure the keyboard for use with an AT machine or an XT machine. If this is the case with your keyboard, verify that the switch is in the AT position.

The keyboard may not be a valid PC/AT keyboard (e.g., it is a PC/XT-only or PS/2 keyboard). If this is the case, replace the keyboard with a PC/AT style keyboard.

Memory parity interrupt at ...

Problem: This could be a software error (reading a nonexistent memory area) or a true hardware failure.

Solution(s): Attempt to repeat the error. If the error occurs during the execution of your own proprietary software, verify that the memory location specified in your software is valid.



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Missing operating system

Problem: Although the system could read the hard disk and find the active partition, the operating system files could not be found.

Solution(s): This is can be caused by using a drive type number or head/cylinder combination in the EPC-8's IDE Adapter 0 Master Menu that does not match the type number used to format the hard disk. Run the BIOS setup program. Select the Autotype fixed disk option, or if known, correct drive type or User Editable parameters to match the type used to format the disk originally. Save the changes and reboot the system.

This can also occur if the hard disk is partitioned and one partition is set active, but the partition does not contain the operating system files..

Non-system disk or disk error
Replace and press any key when ready

Problem: This is caused by an attempt to boot from a disk or diskette that is not recognized as a system disk; that is no system files exist on the disk or diskette.

Solution(s): Most often it results when you reboot with a non-system diskette in the floppy drive, because the BIOS always attempts to boot from the floppy drive if a diskette is installed.

If you are trying to boot from the hard disk, make sure that you do not have a diskette in the A: drive and press any key.

If you are trying to boot from floppy, insert a known good bootable system diskette in the A: drive and press any key.

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Not ready reading drive ...

Problem: This is usually caused by not fully inserting a diskette into the floppy drive.

Solution(s): Eject the floppy diskette and reinsert making sure that the diskette seats completely into the floppy drive.

Parity error in segment ...

Problem: This could be a software error (reading a nonexistent memory area) or a true hardware failure.

Solution(s): Attempt to repeat the error. If the error occurs during the execution of your own proprietary software, verify that the memory location specified in your software is valid.

Previous boot incomplete - Default configuration used

Problem: Previous Power On Self Test did not complete successfully

Solution(s): Run BIOS Setup and verify the settings and reboot.

Real time clock error

Problem: The battery-backed TOD clock fails the BIOS test.

Solution(s): Run the BIOS setup program to determine what is wrong, and correct it. If the error occurs repeatedly, the EPC-8's battery may have failed.

System CMOS checksum bad - run SETUP

Problem: Something in the nonvolatile CMOS RAM is incorrect. It has been corrupted or modified incorrectly, possibly by an application program that changes stored data in CMOS.

Solution(s): Run the BIOS setup program to determine what is wrong, and correct it. If the error occurs repeatedly, the EPC-8's battery has failed.



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System battery is dead - Replace and run SETUP

Problem: The CMOS clock battery indicator shows the battery is dead.

Solution(s): Run the BIOS setup program to determine what is wrong, and correct it. If the error occurs repeatedly, the EPC-8's battery has failed and needs to be replaced.

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Appendix K - Configuring the Ethernet Drivers

After the EPC-8 is installed, cabled and configured, follow the instructions in this chapter to configure the network interface drivers. The distribution diskettes supplied with the EPC-8 contain drivers for IPX, ODI, NDIS and a packet driver under DOS/Windows and OS/2.

The majority of users running DOS/Windows select the ODI driver in 16-bit mode, if supported by their network software.

Most OS/2 users select the ODI driver.

EPC-8 Ethernet support under other operating systems, such as SCO UNIX, LynxOS, VentureCom VENIX, QNX, etc., is built into the operating system itself and does not require additional drivers. Use the instructions provided with the network software package.

The I/O base address, shared memory base address, and IRQ channel used by each LAN adapter must agree with the values for those parameters that are used by the adapter's network interface driver. The method used to change the driver parameters depends on the network operating system software in use.

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NetWare IPX Driver for DOS Installation

The Internet Packet Exchange (IPX) drivers provided with the EPC-8 distribution diskettes are **NE2000.COM** and **ATLANTIC.COM**. The **NE2000.COM** driver is used in 8-bit, NE2000 mode with the IPX interface. Once the EPC-8 is configured using **AUTOSET**, and the distribution diskettes are loaded onto the system, use a text editor to modify the **AUTOEXEC.BAT** file, entering these commands at the end of the file:

```
ne2000 /o0      (run ne2000 /d to display available options)
netx.com        (provided by network software or operating
                 system distribution diskettes)
```

The **NE2000.COM** driver supplied on the EPC-8 distribution diskettes is preconfigured for use with the Ethernet 802.3 interface. If your network requires operating **multiple** protocols on top of a single card, use the **ECONGIF** program provided by Novell to change the **NE2000.COM** interface setting to Ethernet II.

The **ATLANTIC.COM** driver is used in 16-bit Western Digital mode with the IPX interface. Once the EPC-8 is configured using **AUTOSET**, and the distribution diskettes are loaded onto the system, modify the **AUTOEXEC.BAT** file by entering these commands at the end of the file:

```
atlantic /o0    (run atlantic /d to display available options)
netx.com        (provided by network software or operating
                 system distribution diskettes)
```

ODI Driver for DOS Installation

The Open Data-Link Interface (ODI) adds functionality to NetWare and network computing environments by supporting multiple protocols and multiple LAN adapters in a single workstation. Refer to the Novell *NetWare ODI Shell for DOS* manual for additional installation instructions.

Once the EPC-8 is configured using **AUTOSET**, and the distribution diskettes are loaded onto the system, use a text editor to modify the **NET.CFG** file to match the **AUTOSET** parameters. The interrupt, I/O address, mode, and interface type must all match.

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Then add the following programs into the **AUTOEXEC.BAT** file:

LSL.COM	Link support layer
ATLANTIC.COM	Multiple Link Interface Driver
IPXODI.COM	IPX/SPX Protocol
NETX.COM	(provided by operating system or workstation distribution diskettes)

While editing the **AUTOEXEC.BAT** file, make sure that the path= statement includes the directory containing the **NET.CFG** file.

The **ATLANTIC.COM** driver is used for the ODI interface in 16-bit Western Digital mode and 16-bit NE2000 mode.

The ODI interface does not support IRQ15.

ODI Driver for OS/2 Installation

The steps below outline a typical procedure for accessing the Novell NetWare Requester using the ODI interface running under OS/2:

1. Open a DOS window.
2. Run **AUTOSET**. Set the IRQ=3, I/O port address=300, and select the adapter architecture.
3. Save and exit **AUTOSET**.
4. Install the OS/2 Workstation Service Requester (1 disk) and the OS/2 Utilities (2 disks) supplied with the Novell Network software.
5. Run **INSTALL** from **C:\NETWARE** to select and load **NE2000.SYS**. After the installation **CONFIG.SYS** should contain the following section:

```
device=c:\netware\lsl.sys
run c:\netware\ddaemon.exe
device=c:\netware\ne2000.sys
device=c:\netware\ipx.sys
device=c:\netware\spx.sys
run c:\netware\spdaemon.exe
device=c:\netware\nwreq.sys
ifs=c:\netware\nwifs.ifs
run=c:\netware\nwdaemon.exe
```


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6. Modify/create **NET.CFG** according to the environment. For example:

```
Link Driver NE2000
        Frame Ethernet_802.3
        Protocol IPX
        Port 300 f
```

7. Reboot the system.

NDIS Driver for DOS Installation

The NDIS ethat2 driver is used for 16-bit Western Digital mode and 16-bit NE2000 mode for the NDIS interface. It is used by various protocol stacks and applications, such as Windows for Workgroups (WFW). NDIS 3.0 protected mode support is already included in WFW. The steps below would be part of a typical setup for NDIS 2.0 real mode.

1. Set up **PROTOCOL.INI** according to the environment. To set up ethat2 for NE2000 using IRQ3 and I/O base address 300, refer to the example below.

```
[EXM10A]
DriverName=ETHAT20$
IOBASE=0x300
INTERRUPT=3

[MS$NETBEUI]
DriverName=netbeui$
SESSIONS=10
NCBS=32
LANABASE=1
BINDINGS=EXM10A
[NETBEUI]
LANABASE=1
BINDINGS=EXM10A
```

2. At the command line, enter NET START WORKSTATION.

3. At the command line, enter NET VIEW to verify access to other computers.

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Packet Driver Installation

The diskettes distributed with the EPC-8 contain two packet drivers named **ATDRIVE.COM** (for 16-bit NE2000 mode) and **WD8003E.COM** (for 16-bit Western Digital mode). RadiSys also supplies files named **TELBIN** (a Telnet terminal emulation) and FTPBin (an FTP or File Transfer Program) that work with TCP/IP.

In order to install the packet drivers, first run **AUTOSET** to initialize the adapter (IRQ, I/O port, shared memory base, etc.)

Once **AUTOSET** has been run, install the packet driver. Add the following lines to the end of the **AUTOEXEC.BAT** file:

For WD8003:

```
REM WD8003 <s/w interrupt> <IRQ> <IO_Base> <shared memory base>
wd8003e 0x60 5 0x240 0xDC000
ipxpkt.com          (supplied with EPC-8 distribution diskettes)
netx.com            (supplied with network software or operating system)
```

For NE2000:

```
REM ATDrive -i <software interrupt> -b <I/O Base> -q <IRQ> -n
ATDrive -i 60 -b 240 -q 5 -n
ipxpkt.com          (supplied with EPC-8 distribution diskettes)
netx.com            (supplied with network software or operating system)
```

Windows NT Driver Installation

This section explains how to use the NE2000 driver provided with Windows NT to access the network using the EPC-8. Be sure to use a 16-bit data width, and run **AUTOSET** first (in DOS) to set up the hardware parameters in I/O Port mode.

1. Log on to Windows NT.
2. Select the Network icon in the Control Panel.
3. Select the Adapters button and install the NE2000 adapter.
4. Select and install the **NE2000.SYS** driver. When completed, restart the system in order for the changes to take effect.

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5. Select the File Manager icon. Select "Network Connection" under the Disk Menu. Additional drives that are now available display in the list, verifying the installation.

SCO UNIX Installation

This section describes instructions for properly installing the TCP/IP drivers of SCO Open Desktop version 1.1 and 2.0 and the equivalent SCO UNIX/386 version.

First, configure the EPC-8 using the methods described in the previous sections. Do this under DOS. The **AUTOSET** program is a DOS program only.

After installation of the SCO UNIX/386 or SCO Open Desktop environment, proceed with the installation of the WD8013E and TCP/IP drivers as detailed in SCO's documentation. Use the values defined in the **AUTOSET** program for I/O base address, IRQ number, memory address and size. Note that SCO UNIX has built-in support for Western Digital cards. All other aspects of installing TCP/IP or other protocol stacks and communicating with remote workstations are identical to that outlined in the SCO documentation.

Configuring an EPC-8

To configure an EPC-8, execute the **AUTOSET** program. This program configures the EPC-8's interrupt vector, I/O base address, and RAM buffer addresses. Executing this program requires that the EPC be booted in DOS (not SCO UNIX), either from a DOS floppy or a DOS partition on the hard disk.

If IRQ3 is chosen as the EPC-8 interrupt vector, the COM2 serial port driver must be disabled (see "Disabling the COM2 Serial Port Driver", below

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Disabling the COM2 Serial Port Driver.

The SCO UNIX COM2 serial port driver can be disabled in version 2.0 by running makdev serial and uninstalling the IBM-COM2 "board." COM2 can also be disabled manually by editing two kernel configuration files and rebuilding the kernel:

1. Edit the file /etc/conf/sdevice.d/sio. The file contains two lines:

   sio Y 1 7 1 4 3F8 3FF 0 0
   sio Y 1 7 1 3 2F8 2FF 0 0

   The line with a "3" in the sixth column specifies a serial I/O device driver on IRQ3. Change the "Y" in the second column of the line to "N" to remove the device driver from future kernel builds:

   sio Y 1 7 1 4 3F8 3FF 0 0
   sio N 1 7 1 3 2F8 2FF 0 0

2. Edit the file /etc/conf/pack.d/sio/space.c. In the section of this file defining non-microchannel devices is the line:

   {1,IBM_BOARD,1,3,1,sd(0x2f8),0,0,MCRBIT3}, /* ibm COM2 */

   This line defines the COM2 port in the serial I/O driver device table. Using "C" comment symbols, remove the line from the file:

   /*{1,IBM_BOARD,1,3,1,sd(0x2f8),0,0,MCRBIT3},*//* ibm COM2 */

3. The final step in disabling the COM2 serial port driver is to rebuild the kernel:

   a. Log in as root and execute **sysadmsh**, or simply log in as **sysadmsh**.

   b. Select the "System" option.

   c. Select the "Configure" option.

   d. Select the "Kernel" option.

   e. Select the "Rebuild" option to build a kernel. When prompted, specify that the new kernel should boot by default, and that a new kernel environment should be built.

   f. Exit **sysadmsh**.

g. Reboot the system ("**shutdown -g0**" or "**init 6**").

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VenturCom VENIX Installation

Configuring an EPC-8 Ethernet controller to work with VenturCom VENIX requires that the EPC-8 be configured to execute effectively with the other devices in the system. VenturCom VENIX may also require re-configuration, depending on the EPC-8's configuration parameters.

Configuring an EPC-8

To configure an EPC-8, execute the **AUTOSET** program. This program configures the EPC-8's interrupt vector, I/O base address, and RAM buffer addresses. Executing **AUTOSET** requires that the EPC be booted to DOS (not VENIX), either from a DOS floppy or a DOS partition on the hard disk.

If IRQ3 is chosen as the EPC-8 interrupt vector, the COM2 serial port driver must be disabled (see "Disabling the COM2 Serial Port Driver", below

Disabling the COM2 Serial Port Driver.

The VenturCom VENIX COM2 serial port driver can be disabled manually by editing a kernel configuration file and rebuilding the kernel:

1. Edit the file /etc/conf/sdevice.d/asy. The file contains two lines:

```
asy   Y   1   7   1   4   3F8   3FF   0   0
asy   Y   1   7   1   3   2F8   2FF   0   0
```

   The line with a "3" in the sixth column specifies a serial I/O device driver on IRQ3. Change the "Y" in the second column of the line to "N" to remove the device driver from future kernel builds:

```
asy   Y   1   7   1   4   3F8   3FF   0   0
asy   N   1   7   1   3   2F8   2FF   0   0
```

2. To remove the COM2 serial port driver from the kernel, a new kernel must be built and rebooted:

   a. Log in as root and execute **kconfig**.

   b. Select the "BUILD A KERNEL" option.

c. When prompted, specify that the new kernel should be installed, specify the shutdown warning time, and confirm that a shutdown should occur.

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LynxOS Installation

The EPC-8 must be configured by the **AUTOSET** program in Shared Memory (WD8013-compatible) mode.

For more information on driver data structure editing and building the kernel to operate correctly, reference the *LynxOS TCP/IP Installation and Configuration Manual*.

There are three basic steps to the installation of LynxOS TCP/IP:

1. Retrieve TCP/IP from the floppies or tape.
2. Configure the EPC-8 in Western Digital mode.
3. Install TCP/IP into the kernel.

Retrieve TCP/IP

Install the appropriate LynxOS floppy or tape onto the drive. Make sure you are in the root directory by typing cd / . Retrieve the data with the following command:

```
tar xvf /dev/r Device_Name
```

For example, if the system contains a 3.5" disk, use the following command:

```
tar xvf /dev/rfd1440.0
```

Configure the EPC-8 Parameters

Follow these steps to set up the configurable parameters for the EPC-8 Ethernet adapter to work under LynxOS.

1. Boot up DOS.

2. Run the **AUTOSET** program and set the I/O base address and the IRQ. Set the shared memory base to a 16K byte boundary such as 0xCC00.

If you have purchased your EPC with LynxOS installed, the shared memory base address specified in the kernel matches that of the supplied EPC-8. If you change the EPC-8's shared memory base address, the drive information must be modified. Edit the **/SYS/DEVICES/IF_WD3EINFO.C** file to reflect the new value and remake the kernel.

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Install TCP/IP into the Kernel

Before starting the install script, decide on a host name and check with the Network Administrator to guarantee that the selected host name is unique.

The script **INSTALL.TCPIP** adds TCP/IP to the driver library and device library and then rebuilds the kernel. It will also prompt for the system's host name. To install TCP/IP into the kernel, type the following:

```
/usr/bin/Install.tcpip
```

For more information about this installation, refer to the *LynxOS TCP/IP for 386/AT & PS/2 Systems Installation and Configuration Manual.*

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