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EPC®-9

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Chapter 1 - Product Description

Purpose

This manual was written to provide detailed hardware reference information for OEMs, system integrators, and others who use the EPC-9 as a component of their VMEbus systems. The reader should be able to install the EPC-9 and configure the BIOS and the PMC-1 Video Module based on the information in this manual.

About this Manual

This manual assumes that the reader has good familiarity with PC sytems based on the Intel x86 architecture and some familiarity with VMEbus architecture. For more information about EPConnect, which is a C/C++ programming interface to the Microsoft Windows NT API, consult the *EPConnect for Windows NT/4.0 Programmer's Reference Guide*, available from Radisys.

The information in this manual is organized into the following sections:

Front Matter Table of Contents, List of Figures, List of Tables

Chapter 1 *Product Description*. Provides an introduction to the EPC-9, a brief description of the features provided, and a table of specifications.

Chapter 2 *Configuration and Installation*. Covers the details of installing the EPC-9 in a VME mainframe.

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Chapter 3 *BIOS Configuration*. Describes the process of BIOS configuration using the built-in BIOS setup menus.

Chapter 4 *Theory of Operation*. Describes how the components of the EPC-9 operate to provide a ISA/PCI/VMEbus compatible embedded computer with standard PC peripherals and PCI, VME, and EXMbus interfaces.

Chapter 5 *Programming the VMEbus Interface*. Describes initializing and programming the VMEbus interface using the system BIOS and the Tundra Universe™ PCI-VME bridge chip.

Chapter 6 *Support and Service*. Provides sources of technical support and service contacts.

Appendix A *Chipset and I/O Map*. Maps the addresses used for I/O and by the chipset registers.

Appendix B *Interrupts and DMA Channels*. Shows the DMA channel and IRQ assignments to the peripherals supported by the EPC-9.

Appendix C *Connector*s. Details the location, form, and pin-outs of the connectors used in the EPC-9.

Appendix D *Subplane*s. Describes the use of the interconnect subplanes used to connect the EPC-9 with EXM expansion modules.

Appendix E *Register*s. Maps the address space used by EPC-9 and VMEbus registers.

Appendix F *Glossary*. Describes the terminology and acronyms used in this manual.

Appendix G *SVGA and the PMC-1 Video Module*. Describes the installation and configuration of the PMC-1 mezzanine card.

Appendix H *Error Messages and Diagnosis*. Provides explanations of common error messages and start-up codes.

Appendix I *Using an External Floppy Disk Drive*. Describes the process of installing and configuring an external floppy disk drive.

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Overview

The EPC-9 is a highly integrated PC-compatible computer designed for use in the VMEbus and has VXIbus (VMEbus Extensions for Instrumentation) extensions, with interfaces to the PCIbus and EXMbus. It is a two-slot 6U VMEbus module, with support for two PCI Mezzanine Cards (PMC). It is compatible with all major PC software environments, including Microsoft DOS, Microsoft Windows NT, and IBM OS/2, plus others.

The PC-compatible portion of the architecture includes the following PC-standard features:

- Intel Pentium 100, 133, 166, or 200 MHz processors.
- 256 KB secondary (L2) cache (512KB optional).
- 8, 16, 32, 64, 128, or 256MB of memory, using dual socket SODIMM DRAM.
- Standard front panel PC peripheral interfaces include two RS232 serial ports, an IEEE-1284 bi-directional parallel port, two USB ports, a PCI-based SCSI-2 interface, and 10BASE-T/100BASE-TX Ethernet ports, all with standard interface connectors. The mouse and keyboard connectors are PS/2 style.
- All other standard PC architectural features, including an onboard speaker.
- Two RadiSys PMC sites for add-on devices such as SVGA graphics, video capture, or network interfaces.
- RadiSys standard EXM expansion interface for adding PC-architecture peripherals or interfaces.
- Phoenix NuBIOS with RadiSys enhancements to support the additional onboard features and VMEbus environment.

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Additional features (some optional) include:

- SVGA interface. This PCIbus interface is based on the Cirrus Logic GD5446 chip, with up to 2MB of video RAM providing local bus graphics performance and resolutions up to 1280x1024, with 64K colors. The standard 15-pin connector for this port is enhanced with a programmable output on pin 15, which is not connected on a standard VGA interface.

- 10BASE-T and 100BASE-TX Ethernet interfaces. The interface is based on the Digital 21143 Ethernet controller. Interface configuration (emulation mode and address/interrupt control) is software controlled.

- A watchdog timer. This device can be configured to generate a VMEbus SYSFAIL signal and either halt or perform a warm reboot of the processor, depending on a BIOS setup option. The timer is implemented as a software-retriggerable one-shot, with a programmable reset interval ranging from 128 ms to 8.2 sec.

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VMEbus

The VMEbus is controlled by the Tundra Universe VME/PCI Bridge chip with enhancements for multiprocessor environments. This is described in the next three sections, covering system controller functions, the VMEbus master interface, and the VMEbus extended register set.

System controller functions

The Tundra Universe VME/PCI Bridge allows the EPC-9 to provide full VME slot-1 arbitration functions. When enabled, these functions include priority and round-robin bus arbitration, IACK and bus grant daisy-chain driving, SYSRESET and SYSCLK generation and bus time-out detection. ROR (release-on-request) or a fair-requester, RONR (release-on-no-request) bus release mechanism is software selectable.

VMEbus master interface

The VMEbus master interface provides a full 32-bit data path to the 16, 24, and 32-bit address spaces of the VMEbus. The bus interface is designed with a minimum number of state registers, which maximizes performance in a multitasking or interrupt driven environment.

Programmable hardware byte-swapping is provided for ease of communication with other processor architectures that may share the VMEbus. All the VMEbus address spaces can be addressed from both protected-mode and real-mode operating systems.

The EPC-9 can generate or respond to all 7 standard VMEbus interrupts, and can also receive the VMEbus signals ACFAIL, BERR, and SYSFAIL as interrupts. The EPC-9 implements 16-bit IACK cycles when it generates interrupts.

VMEbus extended register set

As an extension to the VMEbus interface, the EPC-9 implements the set of VXIbus (IEEE 1155-1992) standard multiprocessor support registers in the A16 space.

These registers provide a set of standard identification, status, control and communication functions that are useful in multiprocessor environments. They allow dynamic system configuration by providing for board identification, and provide well-defined multi-processor communications channels and protocols.

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The EPC-9 includes a complete set of VXIbus-defined message-based device registers. These registers are implemented in a proprietary gate array and mapped into the VMEbus A16 address space and include a device-type identifier register, bus status and control registers, and a register-based message passing facility.

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Specifications

Environmental Specifications

The following are the environmental specifications for the EPC-9.

Characteristic		Value
Temperature	operating	100MHz: 0-60°C at point of entry of forced air derated 2°C per 1000 ft (300 m) over 6600 ft (2000 m) 133MHz: 0-60°C at point of entry of forced air derated 2°C per 1000 ft (300 m) over 6600 ft (2000 m) 166MHz: 0-45°C at point of entry of forced air derated 2°C per 1000 ft (300 m) over 6600 ft (2000 m) 200MHz: 0-40°C at point of entry of forced air derated 2°C per 1000 ft (300 m) over 6600 ft (2000 m) 2°C per hour max excursion gradient
	storage	-40°C - 85°C 5°C per hour max excursion gradient
Humidity	operating	5% - 95% noncondensing
	storage	5% - 95% noncondensing
Altitude	operating	0 - 10,000 ft (3000 m)
	storage	0 - 40,000 ft (12,000 m)
Vibration	operating	2.5 g acceleration over 5-300 Hz sine wave, 1 oct/min sine sweep
	storage	5 g acceleration over 5-2K Hz sine wave, 1 oct/min sine sweep
Shock	operating	30 g, 11 ms duration, half-sine shock pulse
	storage	50 g, 11 ms duration, half-sine shock pulse
Airflow		300 linear feet per minute

Table 1-1. EPC-9 Environmental Specifications.

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Power Supply Requirement Specifications

The following table contains power supply requirement specifications.

Power Supply Requirements	
+5V Vcc Current (ma)	11.6 A Max. (166MHz Processor, 256MB DRAM)
+12V	0.2 A Max.

Table 1-2. EPC-9 Power Supply Requirement Specifications.

Additional Specifications

The following table contains other specifications:

Characteristic		Value
Mechanical		
Weight	with PMC-1	2.7 lb. (1.3 kg)
Dimensions	two-slot 6U VMEbus module	
Safety		
	UL 1244	
	IEC 1010-1 (1990) Incl. Amend 1 (1992)/EN61010 (1993)	
	CSA C22. #1010.1 (1992)	
EMC		
	CE Mark	
	CISPR 11:1990/EN 55011(1991): Group 1 Class A	
	IEC 801-2:1991/EN50082-1 (1992): 4kV CD, 8kV AD	
	IEC 801-3:1984/EN50082-1 (1992): 3V/m	
	IEC 801-4:1988/EN50082-1 (1992): 1kV Power Line	
	EMC Directive (89/336/EEC)	

Table 1-3. Additional EPC-9 Specifications.

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Other		
VME	master address	A16, A24, A32
	master transfer	D08(EO), D16, D32, RMW
	slave address	A16
	slave transfer	D08(EO), D16, RMW
	interrupter	I(1-7)
	interrupt handler	D08(O),D16 IH(1-7)
	requester	ROR, RONR, RWD
	arbiter	RRS, PRI
	system controller	SYSCLK, IACK, bus grant daisy chain drivers, and bus time-out error (BERR)
VXI	device type	message based
	protocols	servant/commander/master/interrupter
	manufacturer code	4076 - RadiSys Corporation
	model code	101Fh (if configured for slot 0) 111Fh (if configured for other than slot 0)

Table 1-3 (continued). Additional EPC-9 Specifications.

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Notes

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Chapter 2 - Configuration and Installation

2 2

In order to configure and install the EPC-9, the following steps must be completed:

Step	Action	See Chapter
1	Select the slot location	2
2	Install VMEbus backplane jumpers	2
3	Insert subplane into mainframe	2
4	Insert EPC-9 into mainframe	2
5	Connect peripherals	
6	Power-up	
7	Configure BIOS	3
8	Boot operating system	
9	Install software/configure system	

DO NOT REMOVE THE EPC-9 MODULE FROM ITS ANTI-STATIC BAG UNLESS YOU ARE IN A STATIC-FREE ENVIRONMENT.

The EPC-9, like most electronic devices, is susceptible to electrostatic discharge (ESD) damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

DURING ALL OF THIS INSTALLATION PROCESS, MAKE SURE THAT POWER TO YOUR SYSTEM IS OFF.

The EPC-9 is not designed to be inserted or removed while the chassis is powered up.

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2 2

Configuring the EPC-9

Slot-1 Functionality

Every VMEbus system must have a System (Slot-1) Controller. The Slot-1 controller provides the following functionality:

- Serves as the bus arbiter (priority or round-robin)
- Drives the 16 MHz SYSCLK signal
- Starts the IACK and bus grant daisy chains.
- Provides bus timeout error (BERR) function

The EPC-9 is automatically configured to provide standard VMEbus Slot-1 functionality when it is inserted in Slot-1. The Slot-1 configuration option is enabled automatically by detecting the VMEbus BG3IN* signal if the board is the system controller (Slot-1). If BG3IN* is sampled low immediately after reset, the EPC-9 is installed in Slot-1 and becomes the system controller. The EPC-9 will always power up in non- system controller mode and sample BG3IN* to determine whether or not it is to be system controller. When the EPC-9 is configured as the Slot-1 controller, it performs all the standard VMEbus system control functions.

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Selecting the EPC-9 Slot Location

Two main considerations determine where the EPC-9 should be positioned in the chassis.

- If the EPC-9 is to function as system controller, it must be placed in Slot-1. The VMEbus specification, Rule 3.3, states that the Slot-1 controller must be in Slot 1. All other boards must be to the right of the Slot-1 controller.
- The EPC-9 connects to its peripherals via a subplane which extends to the right of the EPC-9, as viewed form the front. The location you choose must provide sufficient room for all the attached peripherals (EXMs and mass storage modules).

The EPC-9 plus EXM expansion modules plus any mass storage module can be considered together as a single subsystem. When you have determined all of the EXMs and PMCs to be used, check the total power requirements against the power supply ratings of your VMEbus system and the other modules to ensure that the power supply can handle the total power required.

Once you have determined the EPC-9 subsystem physical location in the chassis, the VMEbus backplane must be jumpered appropriately, as described in the following section.

Installing the VMEbus Backplane Jumpers

The VMEbus propagates four bus grant signals (BG0 - BG3) and one interrupt acknowledge signal (IACK) via daisy-chain lines. Per the VMEbus specifications, all boards (that plug into the backplane) are required to handle these signals correctly. All slots that do not have a board plugged into the backplane (i.e. empty slots and slots occupied by EXMs or mass storage modules), need to be jumpered to allow the signals to pass through to other boards in the system.

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2 2

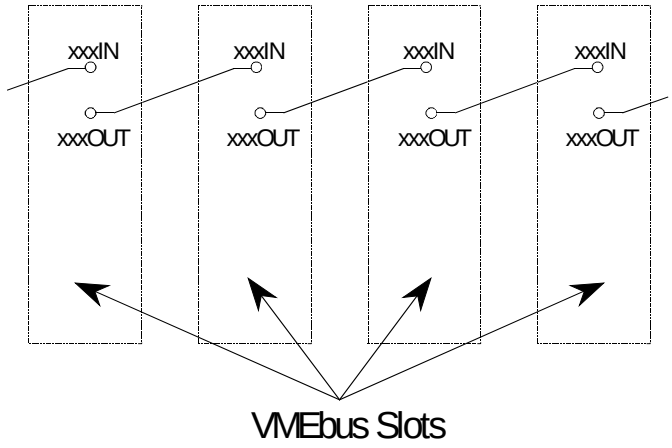


Figure 2-1. Daisy-Chain Signal Concept.

The daisy-chain signal concept is shown in Figure 2-2. The Slot-1 controller board initiates each daisy-chain signal. Each VMEbus slot to the right of the Slot-1 controller, as viewed from the front, must pass through each of the daisy-chained signals. For each VMEbus slot, xxxIn pin must be connected to its corresponding xxxOut pin (e.g. BG0In to BG0Out, BG1In to BG1Out,...,IackIn to IackOut) either through the board in that slot or by jumpers. (Boards that meet VMEbus specifications correctly handle the signals and do not need backplane jumpers. However, many early designs may not handle any of these signals. Check the manual for each board to be installed to determine if these signals are passed through correctly. If these signals are not handled correctly by the board in question, or if the VMEbus slot is empty, all (or some) of these signals must be jumpered to the next location in the daisy-chain. See Figures 2-3 and 2-4 on the following pages for examples.

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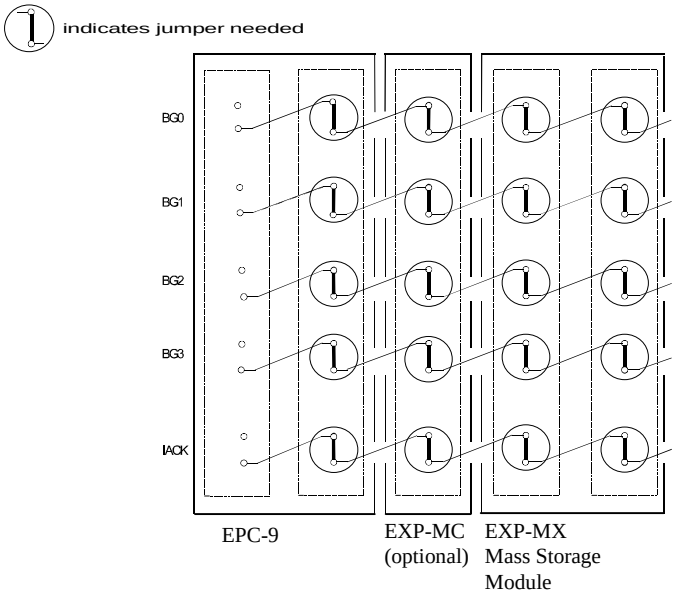


Figure 2-2. Backplane Jumpers Required for EPC-9 Subsystem.

The figure above shows the jumpers required for a five-slot EPC-9 subsystem, consisting of a two-slot EPC-9, an EXP-MC module carrier for two additional EXM modules, and an EXP-MX storage module.

Note that the use of an EXP-MX storage module requires that the "Local Bus IDE Controller" field in the "Integrated Peripherals" BIOS setup menu be set to "Disabled". See *Chapter 3, BIOS Configuration* for more information.

Note that the left-most slot does not require any jumpers. All of the other slots occupied by the subsystem require that all five jumpers be installed.

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Once you have determined where the jumpers need to be, you must determine how to add jumpers to your particular backplane. Different backplane manufacturers handle this in different ways; some provide stake pins or wirewrap pins on the rear of the backplane while others provide pins on the front of the backplane. These pins can be located in several different places.

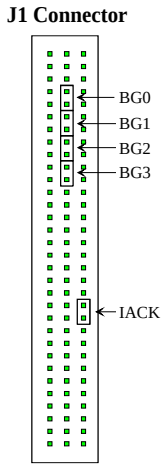


Figure 2-3. VMEbus Jumpers on Rear Wirewrap Pins.

If the pins are on the rear of the backplane, the most common location is in the middle of the J1 connector as shown in Figure 2-3. The connector may have wire-wrap tails on all pins, or just on the bus-grant and IACK pins.

Stake pins (front or rear) can also be located adjacent to the slot being jumpered as shown in Figure 2-4. Typically, the stake pins are located between the slot being jumpered and the next lower-numbered slot (e.g. jumpers for Slot 6 would be located adjacent to Slot 6 between Slots 5 and 6).

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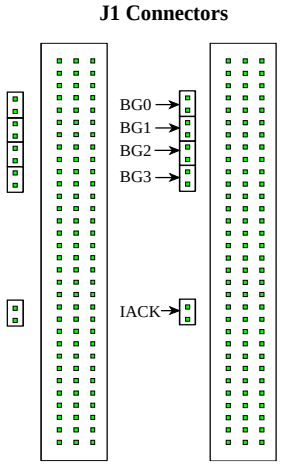


Figure 2-4. VMEbus Jumpers on Front Stake Pins.

Consult your VMEbus chassis reference manual or contact the chassis manufacturer if you are unsure where to jumper your particular system.

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2 2

EPC-9 Insertion

The EPC-9 must be installed onto a subplane that fits between the EPC-9 and the VMEbus backplane. Subplanes are discussed in more detail in *Appendix D - Subplanes.*

The subplane is installed first, connecting to the backplane. After installing the subplane, the EPC-9 processor module can be inserted into the VMEbus chassis.

- **MAKE SURE THAT POWER TO YOUR VME SYSTEM IS OFF. THE EPC-9 MODULE IS NOT DESIGNED TO BE INSERTED OR REMOVED FROM LIVE BACKPLANES.**

- **WHEN HANDLING OR INSERTING THE EPC-9 MODULE, AVOID TOUCHING THE CIRCUIT BOARD AND CONNECTOR PINS, AND MAKE SURE THE ENVIRONMENT IS STATIC-FREE.**

√ Make sure the ejector handles are in the normal (non-eject) position. (Push the top handle down and the bottom handle up so that the handles are not tilted.)

√ Slide the EPC-9 module into the left-most slot occupied by the subplane. Use firm pressure on the handles to mate the module with the connectors.

√ Tighten the retaining screws in the top and bottom of the front panel to ensure proper connector mating and prevent the module from loosening due to vibration.

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Connecting Peripherals to the EPC-9

WARNING!

DO NOT PLUG IN ANY CABLE OR CONNECTOR INTO THE FRONT PANEL CONNECTORS WHILE THE SYSTEM IS POWERED UP. ELECTRONICS EQUIPMENT IS GENERALLY NOT DESIGNED TO WITHSTAND FLUCTUATIONS IN POWER. THUS DAMAGE COULD ARISE FROM PLUGGING IN A DEVICE OR BOARD WHILE POWER IS ON. **NEVER** PLUG IN A SERIAL OR PARALLEL DEVICE, KEYBOARD, TRANSCEIVER, MONITOR OR OTHER COMPONENT WHILE THE SYSTEM IS **ON**.

The next step of installation is connecting peripherals, typically a video display and keyboard, but also perhaps a mouse, modem, printer, etc. Pin-outs for the EPC-9 front-panel connectors are specified in *Appendix C - Connectors and Jumpers.*

SCSI Termination

When you configure SCSI peripherals to work with the EPC-9, you need to consider the placement of the EPC-9 in the SCSI chain. The EPC-9 is must be the last device in the SCSI chain, and thus is terminated.

Remaining Steps

The remaining configuration steps may include BIOS configuration, driver software installation and application software installation. Your system may be preconfigured by your supplier or you may be required to perform these tasks yourself.

Chapter 3 of this manual describes the process of setting up the BIOS configuration. Much of the hardware setup is accomplished by configuring the BIOS.

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Notes

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Chapter 3 - BIOS Configuration

3 3

Introduction

The EPC-9 uses the Phoenix NuBIOS to configure and select various system options. This section details the various menus and sub-menus that are used to configure the system. This section is written as though you are setting up each field in sequence and for the first time. Your system may be correctly pre-configured and require very little setup.

Some error messages might occur during the execution of the BIOS initialization sequence. If errors occur during the power-on self-test (POST), the BIOS will display the error on the appropriate line of the screen display and, depending on how your system is configured, will either pause or attempt to continue. Refer to *Appendix H - Error Messages & Diagnosis.*

BIOS Setup Screens

The EPC-9's BIOS contains a setup function to display and modify the system configuration. This information is maintained in the EPC-9's nonvolatile CMOS RAM and is used by the BIOS to initialize the EPC-9 hardware.

The BIOS Setup can only be entered during the system reset process, following a power-up, front panel reset, or equivalent. Press the F2 key when prompted to enter Setup.

Note: The "Press F2 to enter Setup" prompt may be suppressed (see *Boot Options Sub-Menu, SETUP Prompt*) , but the F2 key still invokes the BIOS Setup program during system reset.

BIOS setup is accomplished by making selections from a series of menus, shown in Figure 3-1.

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3 3

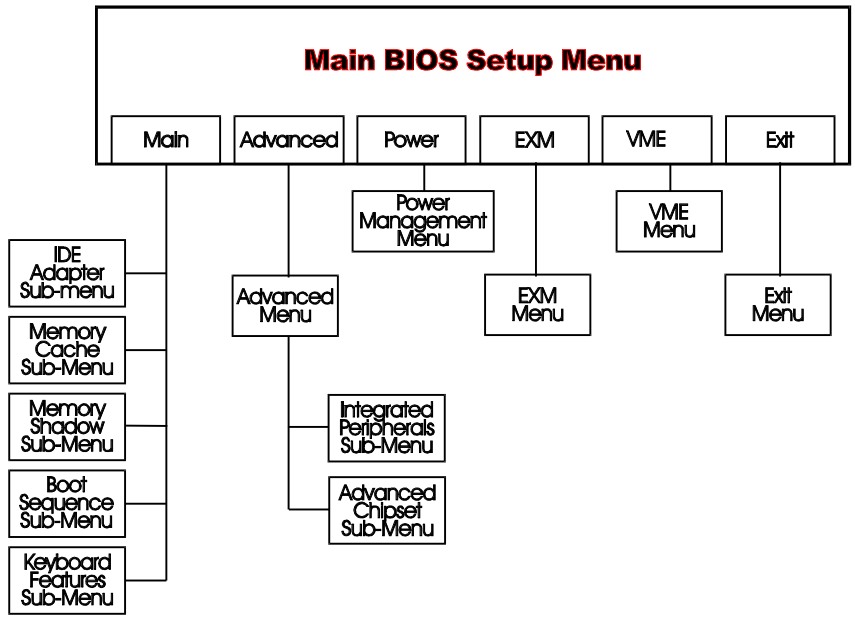


Figure 3-1. BIOS Setup Menu Map.

NOTE: The prompt to press the F2 key to enter the BIOS setup can be suppressed in the BIOS setup. See the Keyboard Features Sub-Menu for details. However, you can still press the F2 key to enter the BIOS setup, even if the prompt is suppressed.

Use the up and down cursor (arrow) keys to move from field to field. Use the right and left arrows to move between the menus shown in the menu bar at the top of the screen. If you use the arrow keys to leave a menu and then return, your active field is always at the beginning of the menu. If you select a sub-menu and then return to the main menu, you return to that sub-menu heading.

Fields with a triangle to the left are actually sub-menu headings; press Enter when the cursor rests on one of these headings to reach that sub-menu. For most fields, position the cursor at the field and from the numeric keypad, press the + and - keys to rotate through the available choices. Certain numeric fields can also be entered via the keyboard. Once the entry has been changed to appear as desired, use the up and down arrow to move to the next field.

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Main BIOS Setup Menu

The Main Setup Menu is shown below, in Figure 3-2:

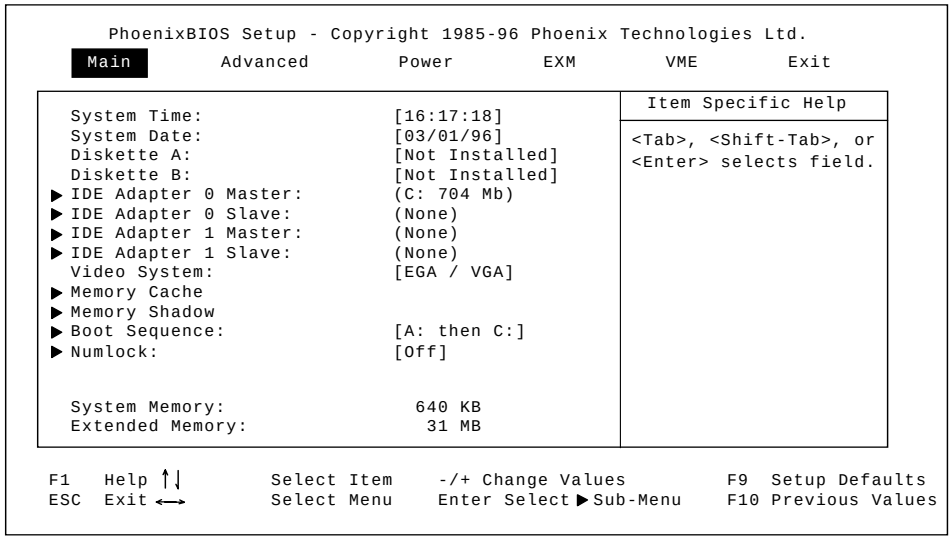


Figure 3-2. Main BIOS Setup Screen.

The far right menu in the menu bar is the Exit Menu. Use the options in the Exit menu to save your changes, re-load default BIOS settings, etc. Press the ESC key to jump immediately to the Exit Menu.

The fields in each menu and sub-menu are explained below. Additional help information is available in the help area on the Setup screen.

System Time:/System Date:

These values are changed by moving to each field and typing in the desired entry. Use the Tab key to move from hours to minutes to seconds, or from months to days to years. There is no default value.

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Diskette A:/Diskette B:

This field identifies the type of floppy disk drive installed as the A:/B: drive. Possible settings are **Not Installed**, **360 KB, 5¼"**, **720 KB, 3½"**, **1.2 MB, 5¼"**, **1.44 MB, 3½"**, and **2.88 MB, 3½"**. The BIOS defaults to **Not Installed** for drives A: and B:.

IDE Adapter 0 Master/Slave: Sub-Menus

These fields are headings for menus that allow entering complete disk drive information. Once the information is entered for the drive, the entry in the Main Menu shows the drive selected. See *IDE Adapter Sub-Menus* for more information.

Video System

Use this field to select among the different video options available. Select from EGA/VGA, CGA 80x25, or monochrome. The default is "EGA/VGA". The EPC-9's video is VGA, supplied by the PMC1 Video Module.

Memory Cache Sub-Menu

The term "Memory Cache" refers to the technique of caching BIOS images. See *Memory Cache Sub-Menu* for more information.

Memory Shadow Sub-Menu

The term "Memory Shadow" refers to the technique of copying information from an extension ROM into DRAM and accessing it in this alternate memory location. The EPC-9 restricts what memory is available for shadowing because of the special requirements for SCSI and the Universe™ PCI/VME bridge. See *Memory Shadow Sub-Menu* for more information.

Boot Sequence Sub-Menu

The Boot Sequence Sub-Menu allows you to change the boot delay, the boot sequence, and to disable several displays during the boot process, such as the SETUP prompt, POST errors, floppy drive check, and summary screen. When the boot sequence has been specified in the Boot Sequence Sub-Menu, the sequence is displayed in the Boot Sequence field of the Main menu.

Keyboard Features (Numlock) Sub-Menu

Use this menu to enable or disable various keyboard features, including the Numlock key, the key click, and the keyboard auto-repeat rate and delay. The Numlock entry in the Main Menu displays the Numlock setting.

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System Memory

This field is not editable and displays the amount of conventional memory (below 1MB). No user interaction is required.

Extended Memory

This field is not editable and displays the amount of extended memory (above 1MB). No user interaction is required.



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IDE Adapter Sub-Menus

There are a total of four IDE adapter sub-menus for the primary and secondary hard disk controllers, each having a master and slave drive menu. The EPC-9 uses an internal (primary) hard disk that is controlled by the settings for IDE Adapter 0 Master. In addition, a secondary controller connector is provided, capable of supporting two external IDE hard disks. To see or reconfigure the detailed characteristics of the primary hard disk, select the IDE Adapter 0 Master item from the Main BIOS Setup. The IDE Adapter 0 Master Sub-Menu is shown below, in Figure 3-3:

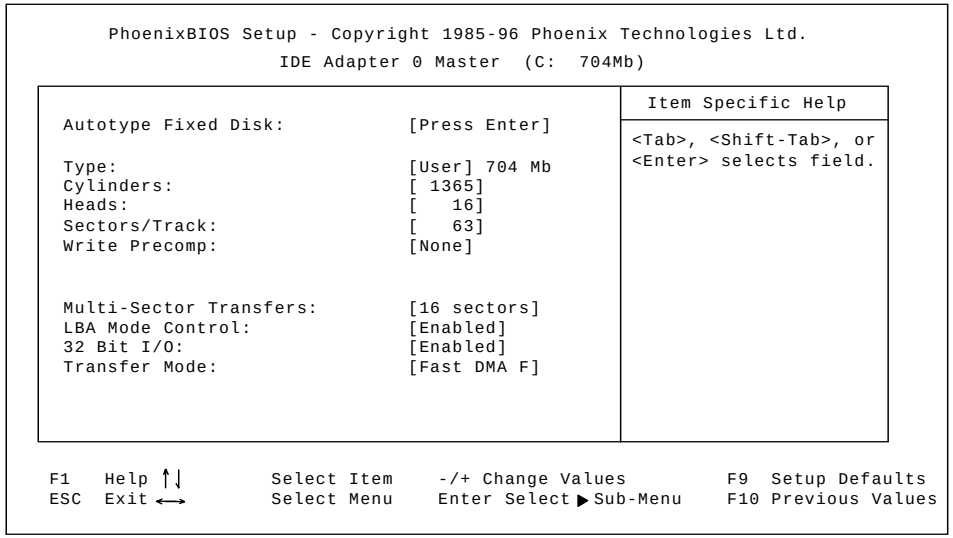


Figure 3-3. IDE Adapter Sub-Menu.

Autotype Fixed Disk

Use this option when setting up new disks. This option allows the BIOS to determine the proper settings of the disk based on information on the disk, which is detected by the EPC-9 BIOS for drives that comply with ANSI specifications. Press the Enter key to invoke this function.

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Existing (formatted) disks must be set up using the same parameters that were used originally when the disk was formatted. You must enter the specific cylinder, head, and sector information. This information is usually listed on the label attached to the drive at the factory. Select the "User" type described below to describe an existing formatted disk.

Type

If you are using a pre-configured system, you probably have an IDE hard disk drive. Select "None" if you are not using an IDE hard disk drive. In the case for which you have an IDE disk but cannot employ the "Autotype" feature, then select "User" for the Type and enter the correct drive values for cylinders, heads, sectors/track, and write precompensation from the label attached at the factory. For disks not supplied by RadiSys, consult the disk drive's documentation.

If you specify "Auto" for the hard disk type, the BIOS will query the hard disk for its parameters whenever the POST runs. If a hard disk type is set to "Auto", but no hard disk is actually present, the BIOS will continue to query the (non-existent) hard disk until it times out, adding a number of seconds to the duration of the POST.

Note that there are some restrictions when setting up devices on the EPC-9. If you plan to boot from a non-IDE device, such as a SCSI hard disk, set the C: drive type as "None" to allow the BIOS extension to find and boot from the bootable device with the lowest SCSI ID number.

Multi-Sector Transfers

This option allows the user to configure the System BIOS to read ahead by the specified number of sectors whenever a disk access is performed. This has the effect of reading more data at once to reduce the absolute number of discrete disk reads performed by the operating system, which may increase system performance. The possible selections are "Disabled", "2 sectors", "4 sectors", "8 sectors", or "16 sectors". Note that autotyping may change this value if the hard disk reports that it supports block accesses. The default is "Disabled".

LBA Mode Control

When enabled, this option allows the System BIOS to reference hard disk data as logical blocks instead of using the traditional Cylinders/Heads/Sectors (CHS) method. This option can only be used if both the hard disk being configured and the operating system support Logical Block Addressing (LBA). If disabled, then CHS mode is

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used. Note that autotyping may change this value if the hard disk reports that it supports LBA. The default is "Disabled".

32-bit I/O

This option allows the System BIOS to access the hard disk controller with 32-bit I/O accesses, increasing system performance. This selection is not affected by autotyping. If the onboard PCI IDE controller is being used, then this option should be set to "Enabled" to maximize system performance. If an EXM-MX or EXP-MX is installed in the system, then this option should be set to "Disabled". The default is "Disabled".

Transfer Mode

This option selects the mode that the System BIOS uses to access the hard disk. The selections are:

Standard (default)

Fast PIO 1

Fast PIO 2

Fast PIO 3

Fast PIO 4

Fast DMA A

Fast DMA B

Fast DMA F

Older hard disks only support "Standard". Newer hard disks adhering to "Fast ATA" or "Enhanced IDE" specifications may support the fast programmed I/O or DMA modes. Note that autotyping may change this value depending on the transfer modes that the hard disk reports it supports. The fast DMA modes take full advantage of the onboard bus mastering hard disk controller and should yield the highest performance when used in conjunction with multitasking operating systems that support it. The default is "Standard".

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Memory Cache Sub-Menu

The options in this screen allow controlling the cacheability of certain memory regions and also the settings of the Level 2 (L2) cache. The Memory Cache Sub-Menu is shown below.

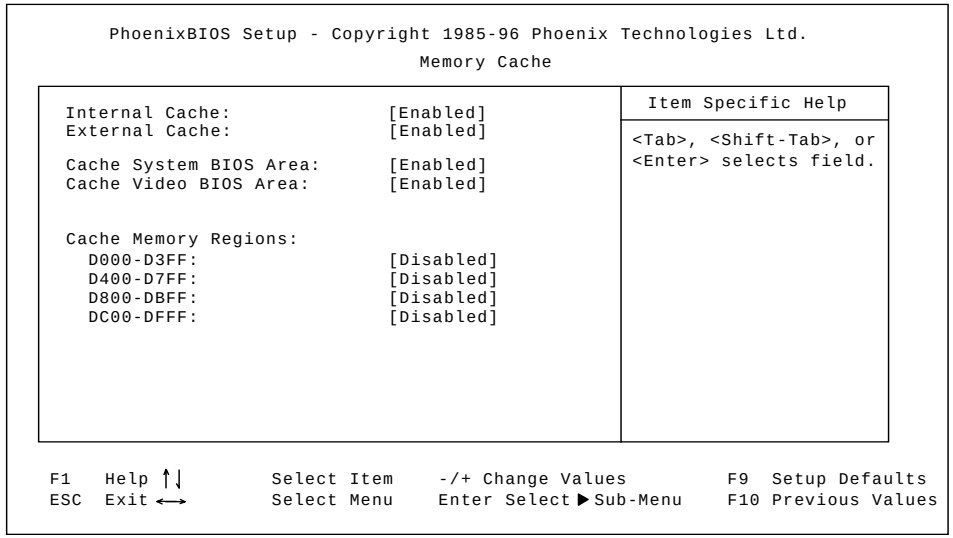


Figure 3-4. Memory Cache Sub-Menu.

Internal Cache

This option enables or disables the Level 1 (L1) cache. The default is "Enabled".

External Cache

This option enables or disables the Level 2 (L2) cache. The default is "Enabled".

Cache System BIOS Area

This option enables or disables caching of the System BIOS area in the 0E0000h through 0FFFFFh DRAM area. The default is "Enabled".

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Cache Video BIOS Area

This option enables or disables caching of the VGA BIOS area in the 0C0000h through 0C7FFFh region. The default is "Enabled".

Cache Memory Regions

These options enable or disable caching of the associated memory regions. When BIOS extensions are present in these regions, enabling caching for that region increases performance. The default is "Disabled".

Memory Shadow Sub-Menu

The term "shadowing" refers to the technique of copying BIOS extensions from ROM into DRAM and accessing them from DRAM. This allows the CPU to access the BIOS extensions much more quickly and generally increases system performance if many calls to the BIOS extensions are made. The Memory Shadow Sub-Menu is shown below.

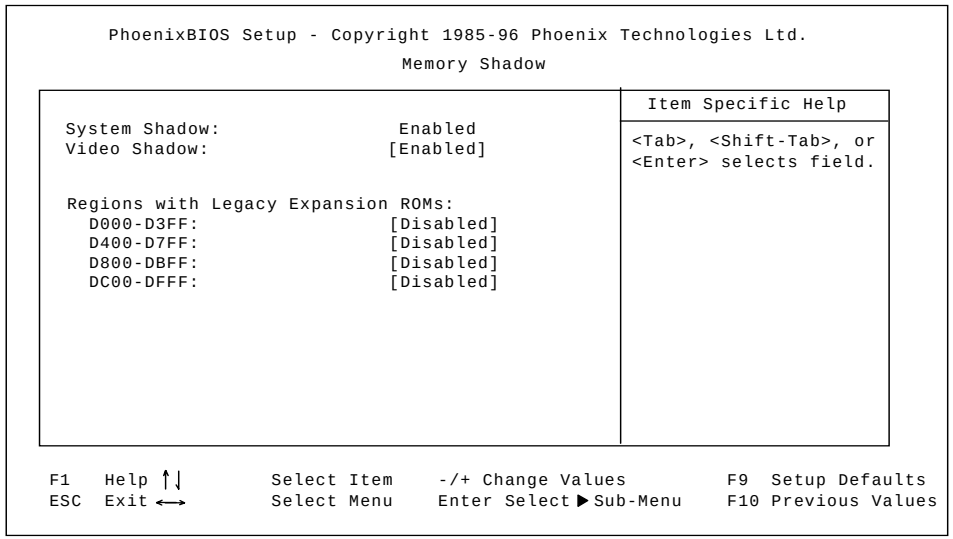


Figure 3-5. Memory Shadow Sub-Menu.

The shadow regions should be used only if an EXMbus card is installed in the system that contains a BIOS extension (ROM) although there is no effect on the system if a

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region is shadowed that does not contain a BIOS extension. Note that each shadow region in the setup menu is 16KB in size. Multiple shadow regions may have to be enabled if the BIOS extension to be shadowed is larger than 16KB.

System Shadow

This option is not editable since the System BIOS is always shadowed.

Video Shadow

Enable this option to increase video BIOS performance. The default is "Enabled".

Shadow Memory Regions

These options enable or disable shadowing for the associated memory region. The default is “Disabled”.



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Boot Options Sub-Menu

Use the Boot Options Sub-Menu to change the boot sequence options. Select the Boot Options Sub-Menu by clicking on the Boot Sequence item in the Main Bios Setup screen. The Boot Options Sub-Menu appears:

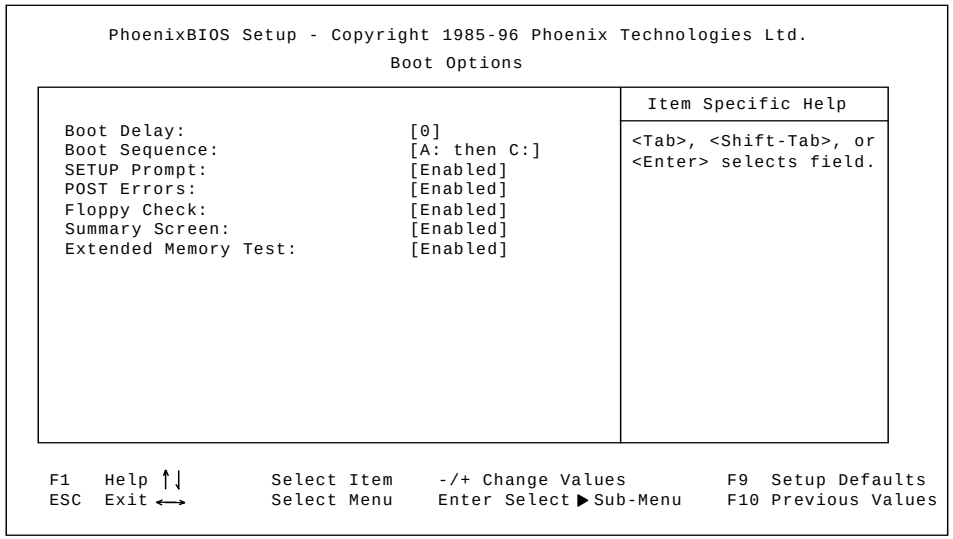


Figure 3-6. Boot Options Sub-Menu.

Boot Delay:

Use this option to set the system to delay booting for a time period from 0 through 255 seconds. This allows for long start up times on boot devices that spin up slowly. The default is "0" seconds.

Boot Sequence:

This option is used to define how the system treats floppy drive A: when booting. Booting can occur from a floppy in the A: drive or directly from the fixed disk drive. To reduce the amount of time required to boot, the boot sequence should be set to "C: only". Note that the C: drive may be either an IDE or SCSI drive. The options are as follows:

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1. A: then C: Used to boot from the floppy drive, or if no floppy disk is present in the A: drive, boot from the C: drive.

2. C: then A: Used to boot from the C: drive, or if none is present, boot from the A: drive.

3. C: only: Used to boot from the C: drive without searching for an A: drive.

The default is “A: then C:”.

The setting chosen here displays in the Boot Sequence Sub-Menu prompt in the Main BIOS Setup screen.

Setup Prompt:

This option is used to enable or disable the message “Press F2 to enter Setup.” Even if the message is disabled, the F2 key can still be pressed at the appropriate time to enter the Setup Menu. The default is “Enabled”.

POST Errors:

This option is used to stop during the boot process if the POST encounters errors. Otherwise, the system continues to attempt to boot despite any startup error messages that display. Note that this option only affects those errors defined as boot failures. See *AppendixH: Error Messages and Diagnosis* for a list of those failures are defined as boot failures that are configured to halt the system. The default is “Enabled”.

Floppy Check:

This option is used to enable or disable the floppy drive search during the boot. To speed up booting, the floppy check should be disabled. It is still possible to boot from the A: drive even with the floppy check disabled. The default is “Enabled”.

Summary Screen:

This option is used to enable or disable a summary of the system configuration, which displays before the operating system starts to load. To speed up booting, disable the summary screen. The default is “Enabled”.

Extended Memory Test:

This option is used to enable or disable the extended memory test portion of the power-on self-test (POST). To speed up booting, disable the extended memory test. The default is “Enabled”.

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Keyboard Features Sub-Menu

The Keyboard Features Sub-Menu allows you to enable or disable various keyboard features. To access the keyboard Features menu, select Numlock in the Main Bios Setup screen.

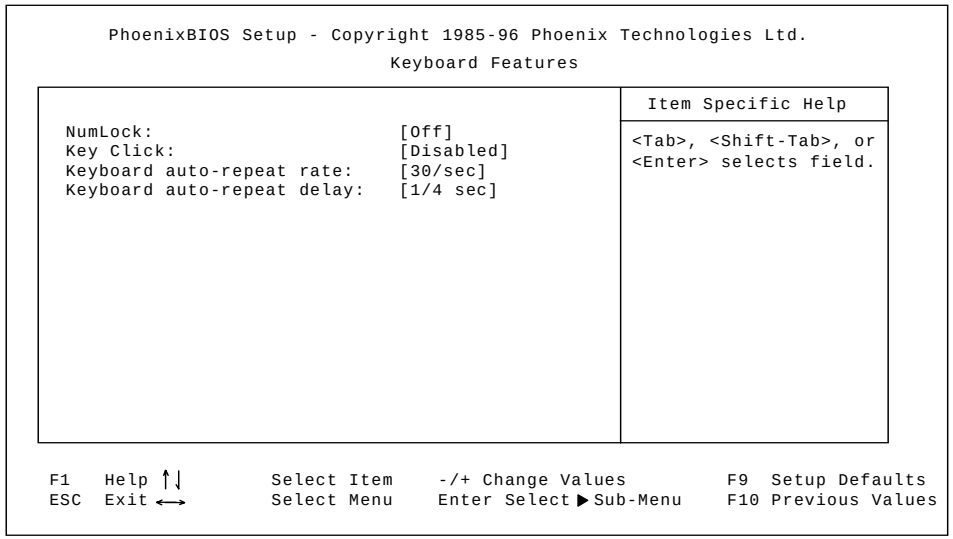


Figure 3-7. Keyboard Features Sub-Menu.

Numlock

Use this option to enable or disable the Numlock feature of the keyboard. Numlock on enables the use of the keypad numbers. The default is "Off".

Key Click

Use this option to enable or disable the key click feature on the keyboard. If enabled, the keyboard produces an audible click each time a key is pressed. The default is "Disabled".

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Keyboard auto-repeat rate:

Use this option to set the auto-repeat rate if you hold a key down on the keyboard. The rate can be set to one of: "2/sec", "6/sec", "10/sec", "13.3/sec", "18.5/sec", "21.8/sec", 26.7/sec", and "30/sec". The default rate is "30/sec".

Keyboard auto-repeat delay:

Use this option to set the delay between when a key is pressed and when the auto-repeat feature begins. The options are "1/4 sec", "1/2 sec", "3/4 sec", and "1 sec". The default delay is "1/4 sec".

When you are finished with this menu, press ESC to exit back to the Main BIOS Setup screen.



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Advanced Menu

This menu controls advanced setup features, such as memory use, those items contained in integrated chipset architectures, plug-and-play capability, watchdog timer effects, large disk access modes, and user BIOS extension addresses. You access this menu by selecting Advanced from the Main BIOS Setup menu.

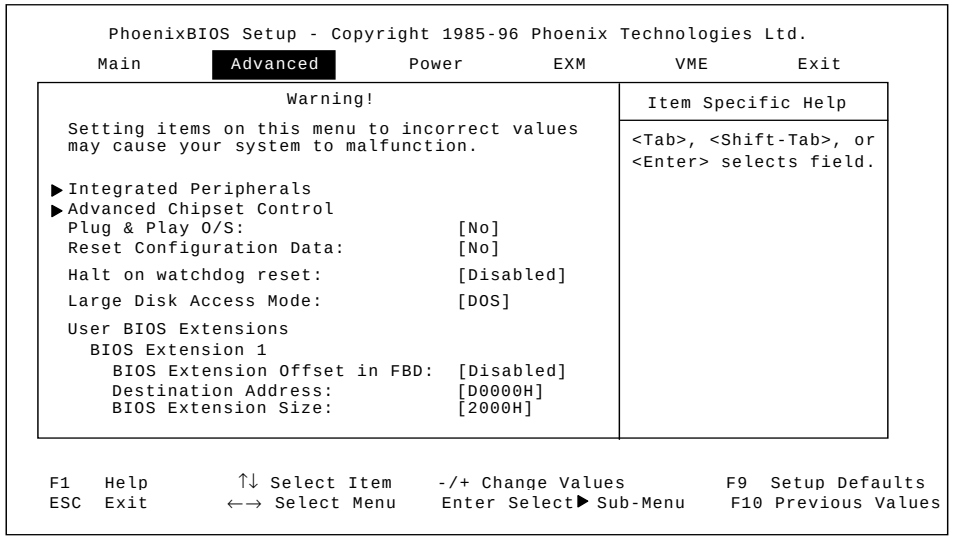


Figure 3-8. Advanced Menu.

Integrated Peripherals Sub-Menu

This option is used to select the Integrated Peripherals Sub-Menu in order to configure the onboard I/O ports, IDE controller, and Ethernet controller.

Advanced Chipset Control Sub-Menu

This option is used to select the Advanced Chipset Control Sub-Menu in order to configure the chipset.

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Plug & Play OS

If enabled, this option informs the System BIOS that the operating system that is booted supports Plug and Play. This has the effect of forcing the Plug and Play portion of the System BIOS to only configure motherboard devices and those peripherals that are necessary for booting (display, hard disk, etc.), the rest being left to the operating system to configure. The default is "No".

Reset Configuration Data

If enabled, this option clears the Extended System Configuration Data (ESCD) block residing in Flash Boot Device (FBD) main block #2. This is necessary the first time a system is turned on or if the ESCD becomes corrupted. The default is "No". This option is automatically reset to "No" after the ESCD is cleared.

Halt on watchdog reset

If enabled, this option causes the System BIOS to halt the boot process if it detects that a watchdog timer reset occurred. The default is "Disabled".

Large Disk Access Mode:

If a hard disk larger than 528MB is being used, this selection should be set to "DOS" if running MS-DOS, or set to "Other" if using a different operating system. When set to "DOS", this selection causes the System BIOS to perform cylinder/head translation if the drive is configured in Setup to have more than 1024 cylinders. This allows MS-DOS systems to use hard disks up to 8GB (1024C x 255H x 63S) in size without special drivers or LBA. The default is "DOS".

User BIOS Extensions

These items control the loading (shadowing) of BIOS extensions contained in the FBD main block #3. Note that there are actually three groups of Setup items to control the shadowing of up to three BIOS extensions. The screen graphic only shows the first group.

BIOS Extension Offset in FBD:

This option selects the source address of the BIOS extension located in the FBD. The address is an offset from the base of the FBD. The offset range is between 46000h through 5FFFFh in 8KB increments. The default is "Disabled".

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Destination Address:

This option selects the target address of the BIOS extension which can range from D0000h through DFFFFh in 8KB increments. The default is "D0000h".

BIOS Extension Size:

This option selects the number of bytes to copy from the FBD into shadow memory. BIOS extension sizes can be selected in 8KB increments from 2000h through 10000h. The default is "2000h".

Integrated Peripherals Sub-Menu

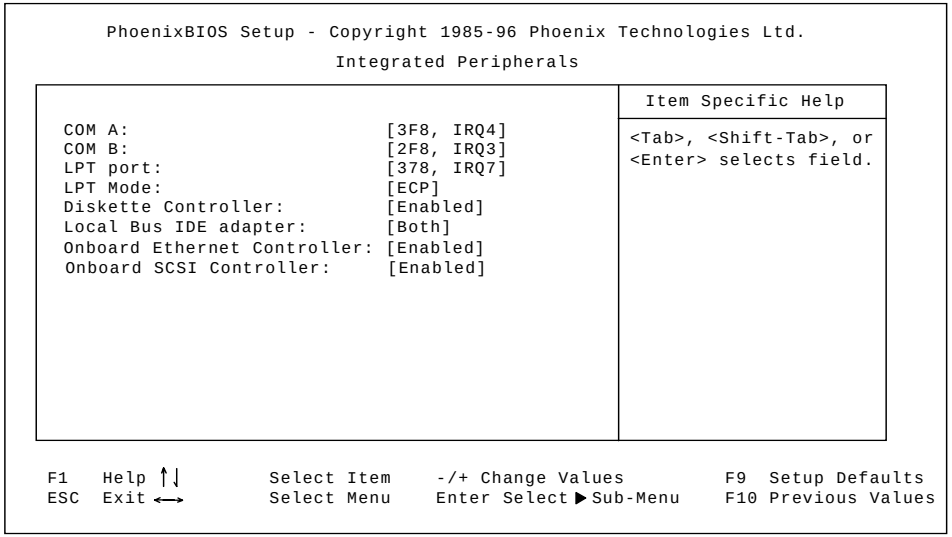


Figure 3-9. Integrated Peripherals Sub-Menu.

COM A

This option is used to configure the serial port labeled on the front panel as "COM A". The selectable I/O base addresses and IRQs are: "Disabled", "3F8h, IRQ4", "2F8h, IRQ3", "3E8h, IRQ4", "2E8h, IRQ3", and "Auto". "Auto" causes the System BIOS to choose a base address and IRQ setting that avoids conflicting with the other ports. The default I/O base and IRQ for this COM port are "3F8h, IRQ4".

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COM B

This option is used to configure the serial port labeled on the front panel as "COM B". The selectable I/O base addresses and IRQs are: "Disabled", "3F8h, IRQ4", "2F8h, IRQ3", "3E8h, IRQ4", "2E8h, IRQ3", and "Auto". "Auto" causes the System BIOS to choose a base address and IRQ setting that avoids conflicting with the other ports. The default I/O base and IRQ for this COM port are "2F8h, IRQ3".

LPT port

This option is used to configure the parallel port labeled on the front panel as "LPT". The selectable I/O base addresses and IRQs are: "Disabled", "378h, IRQ7", "278h, IRQ5", and "Auto". "Auto" causes the System BIOS to choose a base address and IRQ setting that avoids conflicting with the other ports. The default I/O base and IRQ for this LPT port are "378h, IRQ7".

LPT Mode

This option sets the mode under which the LPT port operates. The selections are:

Output only

Bi-directional

ECP

Diskette Controller

This option enables or disables the onboard floppy disk controller. The default is "Enabled".

Local Bus IDE adapter

This option enables or disables the onboard PCIbus IDE hard disk controller. This option must be set to "Disabled" if an EXM-MX hard disk module is installed in the system. The default is "Enabled".

Onboard Ethernet Controller

Use this option to enable or disable the onboard PCIbus Ethernet controller. This option must be set to "Disabled" if a PMC or EXMbus Ethernet controller is installed in the system that conflicts with the resources used by the onboard controller. The default is "Enabled".

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Onboard SCSI Controller

Use this option to enable or disable the onboard PCIbus SCSI controller. This option must be set to "Disabled" if a PMC or EXMbus SCSI controller is installed in the system that conflicts with the resources used by the onboard controller. The default is "Enabled".

Advanced Chipset Control Sub-Menu

Use the options on this screen to control selected chipset settings that affect system performance and function. The Advanced Chipset Control Sub-Menu is shown below.

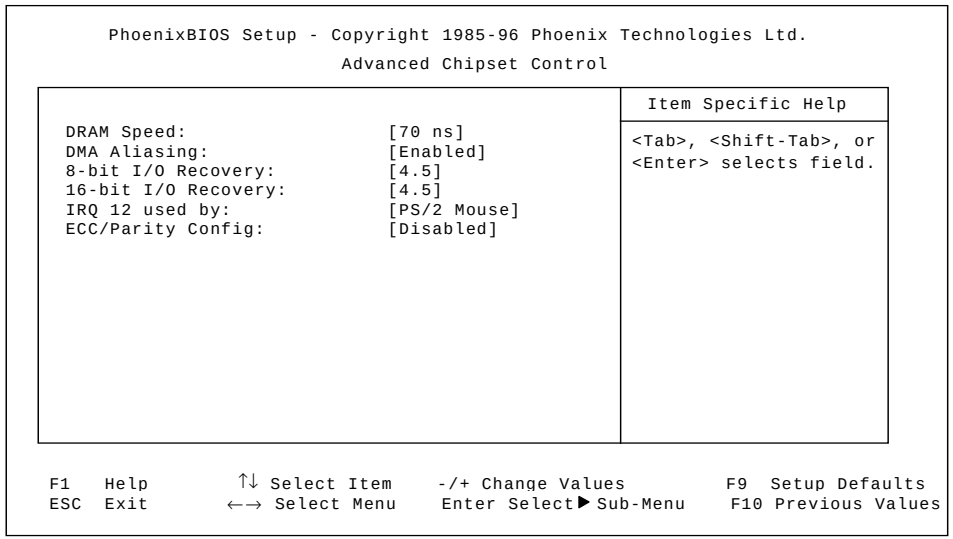


Figure 3-10. Advanced Chipset Sub-Menu.

DRAM Speed

This option selects the speed of the installed DRAM SODIMMs. Selecting 70ns for 60ns SODIMMs decreases performance. Selecting 60ns for 70ns SODIMMs is invalid. The default is "70 ns".

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DMA Aliasing

This option allows I/O accesses to the range 90-9Fh (except 92h) to alias to 80-8Fh. If an ISAbus device uses the address range 90-9Fh, then this option must be disabled to access the device. The default is "Enabled".

8-bit I/O Recovery

This option selects the number of ISAbus SYSCLKs to be inserted by the chipset between 8-bit back-to-back I/O accesses. Increasing the number of clocks decreases I/O performance but may allow slow devices to be accessed properly. This option can range from 3.5 through 11.5 SYSCLKs in 1 SYSCLK increments. The default is "4.5" SYSCLKs.

16-bit I/O Recovery

This option selects the number of ISAbus SYSCLKs to be inserted by the chipset between 16-bit back-to-back I/O accesses. Increasing the number of clocks decreases I/O performance but may allow slow devices to be accessed properly. This option can range from 3.5 through 7.5 SYSCLKs in 1 SYSCLK increments. The default is "4.5" SYSCLKs.

IRQ 12 used by

This option selects the routing of IRQ12. For systems without a PS/2 mouse, this option may be set to "ISA bus" to allow an ISAbus peripheral to use this interrupt line. Systems using a PS/2 mouse must have this option set to "PS/2 Mouse" for the mouse to operate correctly. Since the EPC-9 has a PS/2 mouse connector, the default is "PS/2 Mouse".

ECC/Parity Config

This option configures the DRAM controller to use no parity ("Disabled"), parity ("Parity"), or Error Checking and Correction ("ECC") when accessing DRAM. Use of parity or ECC may improve system reliability since DRAM errors are likely to be detected by the chipset. Use of ECC allows for the detection of single and dual bit errors and the correction of single bit errors during DRAM reads. The parity and ECC selections require that all SODIMMs be x36 instead of x32. The "Disabled" selection can use either x32 or x36 SODIMMs. The default is "Disabled".

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Power Management Menu

Use the options in this menu to control the power management facilities. Only about one-half of the Power Management Menu Screen entries are visible at any one time, however, for completeness, all of the Power Management Menu entries are listed below.

System BIOS Power Management supported states are: Fully On, Standby Mode (partial power reduction), and Suspend Mode (maximum power reduction).

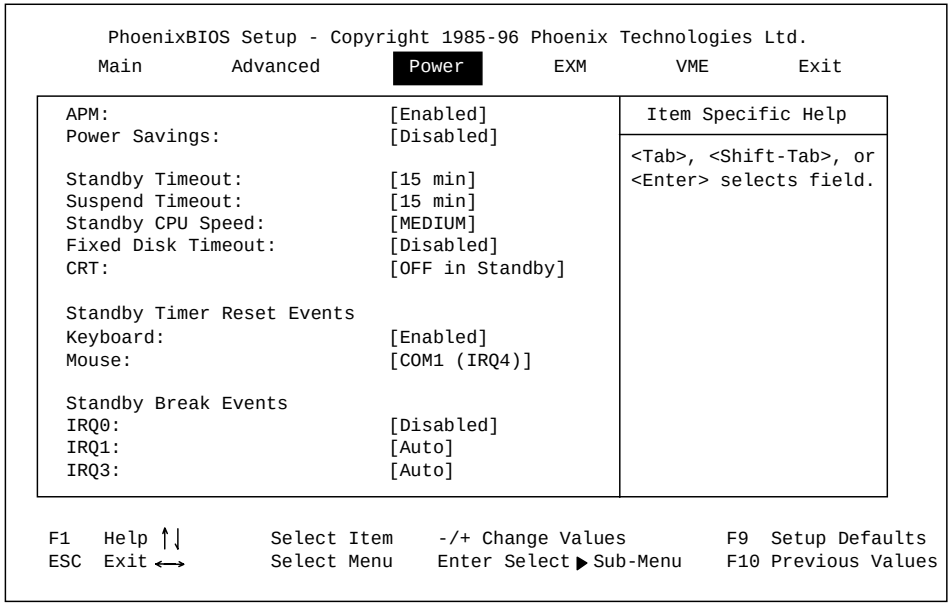


Figure 3-11. Power Management Menu.

APM

This option enables or disables Advanced Power Management (APM). The default is "Enabled".

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Power Savings

This option enables and selects the kind of power management, or it disables power management. The options are: "Disabled", "Customize", "Maximum", "Medium", and "Minimum". The default is "Disabled".

Standby Timeout

This option enables and sets the inactivity duration required to elapse before the system is placed into Standby Mode, or it disables the Standby Timeout. The options are: "Disabled", "2 min", "15 min", "30 min", "1 hour", "2 hours", "3 hours", and "4 hours". The default is "15 min".

Suspend Timeout

This option enables and sets the inactivity duration required to elapse before the system goes into Suspend Mode from Standby Mode, or it disables the Suspend Mode. The options are the same as for the Standby Timeout, shown above. The default is "15 min".

Standby CPU Speed

Use this option to enable or disable the changing of the CPU speed based upon the current power management state. The options are: "Disabled", "LOW", "MEDIUM", "HIGH", and "MAX". The default is "MEDIUM".

Fixed Disk Timeout

Use this option to enable and set the fixed disk access inactivity period required to tell the system to shut off the fixed disk drive, or to disable Fixed Disk Timeout. The options are: "Disabled", "1 min", "2 min", "3 min", "4 min", "5 min", "10 min", and "16 min". The default is "Disabled".

CRT

This option enables or disables power management of the CRT during system entry/exit into/from Standby Mode. The options are "OFF in Standby" and "ON". The default is "OFF in Standby".

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Standby Timer Reset Events

Use these options to enable or disable resetting the Standby Timer, based on activity from the specified device.

Keyboard

Use this option to enable or disable Standby Timer reset, based on keyboard activity. The default is “Enabled”.

Mouse

Use this option to enable or disable Standby Timer reset, based on mouse activity. The options are "Disabled", “PS/2 (IRQ12)”, “COM1 (IRQ4)”, and “COM2 (IRQ3)”. The default is “PS/2 (IRQ12)”.

Standby Break Events

Use this option to enable or disable a Standby Break Event based on the occurrence of the specified IRQ. A Standby Break Event allows the system to run at full speed for the duration of the specified IRQ. Note: No such event is associated with IRQ2.

IRQ0

Use this option to enable or disable the Standby Break Event for IRQ0. The options are: “Disabled” and “Auto”. The default is “Disabled”.

IRQ1

Use this option to enable or disable the Standby Break Event for IRQ1. The options are: “Disabled” and “Auto”. The default is “Auto”.

IRQ3

Use this option to enable or disable the Standby Break Event for IRQ3. The options are: “Disabled” and “Auto”. The default is “Auto”.

IRQ4

Use this option to enable or disable the Standby Break Event for IRQ4. The options are: “Disabled” and “Auto”. The default is “Auto”.

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IRQ5

Use this option to enable or disable the Standby Break Event for IRQ5. The options are: “Disabled” and “Auto”. The default is “Disabled”.

IRQ6

Use this option to enable or disable the Standby Break Event for IRQ6. The options are: “Disabled” and “Auto”. The defau lt is “Disabled”.

IRQ7

Use this option to enable or disable the Standby Break Event for IRQ7. The options are: “Disabled” and “Auto”. The default is “Disabled”.

IRQ8

Use this option to enable or disable the Standby Break Event for IRQ8. The options are: “Disabled” and “Auto”. The default is “Disabled”.

IRQ9

Use this option to enable or disable the Standby Break Event for IRQ9. The options are: “Disabled” and “Auto”. The default is “Disabled”.

IRQ10

Use this option to enable or disable the Standby Break Event for IRQ10. The options are: “Disabled” and “Auto”. The default is “Disabled”.

IRQ11

Use this option to enable or disable the Standby Break Event for IRQ11. The options are: “Disabled” and “Auto”. The default is “Disabled”.

IRQ12

Use this option to enable or disable the Standby Break Event for IRQ12. The options are: “Disabled” and “Auto”. The default is “Disabled”.

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IRQ13

Use this option to enable or disable the Standby Break Event for IRQ13. The options are: "Disabled" and "Auto". The default is "Disabled".

IRQ14

Use this option to enable or disable the Standby Break Event for IRQ14. The options are: "Disabled" and "Auto". The default is "Disabled".

IRQ15

Use this option to enable or disable the Standby Break Event for IRQ15. The options are: "Disabled" and "Auto". The default is "Disabled".

Standby Wakeup Events

Use this option to cause a Standby Wakeup Event based on keyboard or mouse activity. A Standby Wakeup Event allows the system to return to full speed.

Keyboard

Use this option to enable or disable the Standby Wakeup Event, based on keyboard activity. The default is "Enabled".

Mouse

Use this option to select the mouse/IRQ binding for mouse activity detection for power management, or to disable mouse activity as a. Standby Wakeup Event. The options are: "PS/2 (IRQ12)", "COM A (IRQ4)", "COM B (IRQ3)", and "Disabled". The default is "PS/2 (IRQ12)".

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EXM Menu

Use the options in this menu to select and configure the available EXM slots. Since the EPC-9 uses modified EXM backplanes, the first 2 slots are physically covered by the PMC module(s). Therefore, EXM slots 0 and 1 will not be configurable in Setup and only slots 2 through 5 are available.

The required configuration information is found in the hardware reference manual shipped with each EXM expansion module.

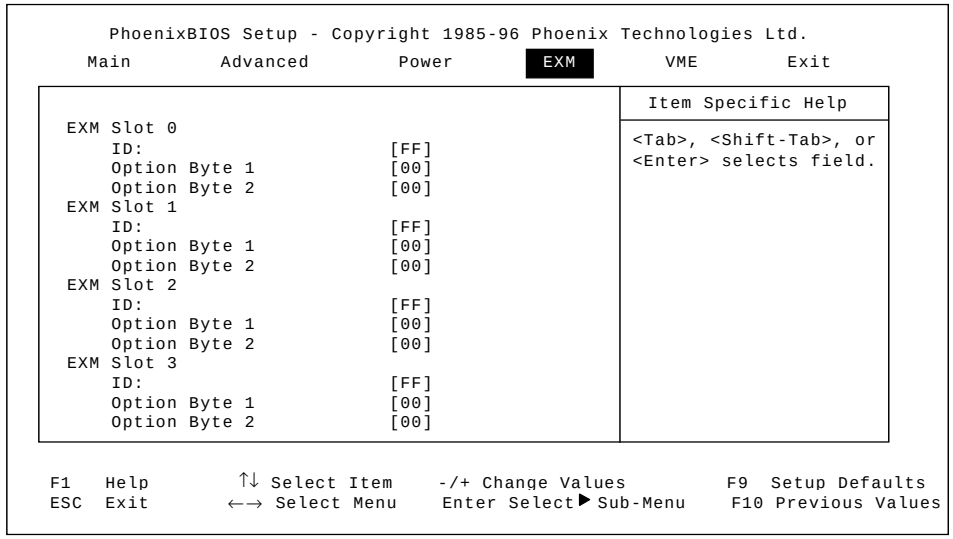


Figure 3-12. EXM Menu.

ID

This option is used to select the EXM ID byte value for the EXM card intended to reside in this slot. If the POST finds that the ID set with this option does not agree with the ID of the card actually installed in the slot, an EXM configuration error occurs and the card is not configured. For a slot with no EXM card installed, enter 0FFh, the default value.

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Option Byte 1

This option is used to select the first option byte value for the EXM card intended to reside in this slot. Option byte 1 typically defines bit 0 as the card enable bit. Other bits in the option byte are defined by the particular EXM card installed. The proper value of this option for a slot with no EXM card installed is not defined. The value typically used is 00h, the default value.

Option Byte 2

This option is used to select the second option byte value for the EXM card intended to reside in this slot. Option byte 2 is defined by the particular EXM card installed. The proper value of this option for a slot with no EXM card installed is not defined. The value typically used is 00h, the default value.

NOTE: Since the EPC-9 uses existing EXM backplanes, the first 2 slots will be covered by the PMC card(s). To compensate for this, EXM slot 0 and slot 1 are non-editable.

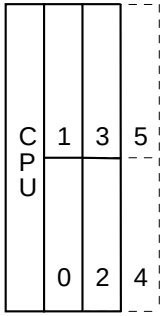


Figure 3-13. Slot Numbering.

All slots **not** occupied by an EXM module should show an ID of FF and OB1/OB2 of 00 00 indicating that no EXM is present.

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Consult the appropriate EXM manual for the correct configuration information for each EXM expansion module installed. Note: Most EXM hardware reference manuals depict a different BIOS Setup Screen than the one shown here. The ID/OB1/OB2 information is valid.

When using EXMs with configurable interrupts, DMA channels, I/O addresses, and/or memory addresses, avoid conflicts with built-in functions of the EPC-9. Guidelines are:

1. If an interrupt is needed, use IRQ3, IRQ4, IRQ5, or IRQ15. IRQ7 can be used if the printer port is not being used. IRQ3 and IRQ4 should not be used if either onboard COM port is being used. IRQ 15 should not be used if the secondary IDE channel is being used. IRQ9 is used by the Universe chip.
2. Use DMA channels 1, 3, 6, and 7.
3. Do not select I/O addresses that conflict with those in the EPC-9. A complete list appears in Appendix A. For instance, I/O addresses in the 300-33F range can be used.
4. If the EXM needs to use upper memory addresses, they must be in the 0D0000h-0DFFFFh range. Note that 0E0000h-0EFFFFh is used for the BIOS and is not available. The bottom 16KB of this range (0E0000h-0E3FFFh) is used for VME interface chip control and the remainder (0E4000h-0EFFFFh) is used for BIOS.

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3 3

VME Menu

The options in this menu are used to configure the EPC-9's VME interface:

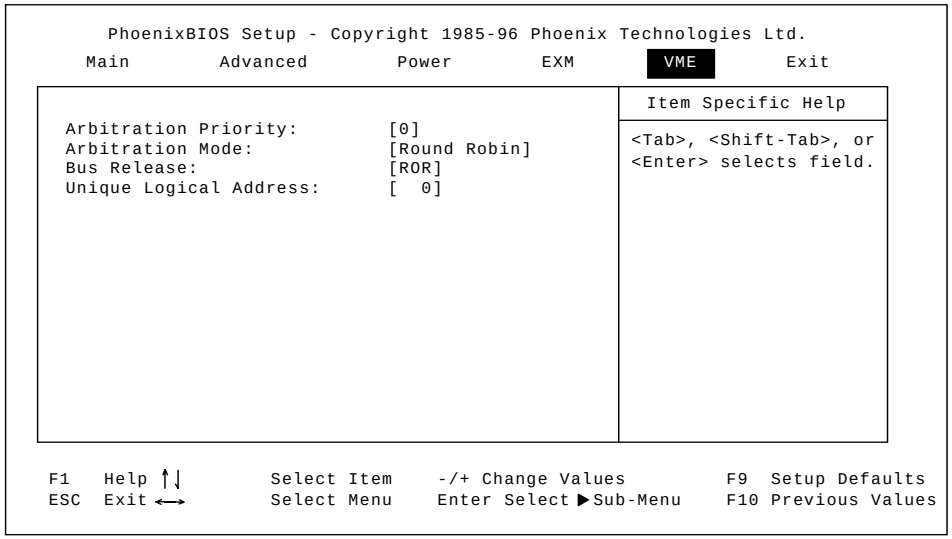


Figure 3-14. VME Setup Menu.

Arbitration Priority

This option is used to select among the four (0 through 3) VMEbus priority levels used when the EPC-9 requests the bus for a VME access. Priority level 0 is the lowest priority while priority level 3 is the highest priority. The default is priority level "0".

Arbitration Mode

This option is used to select the arbitration algorithm that the EPC-9's VMEbus arbiter uses when the EPC-9 is the slot 1 controller. Selecting "Round Robin" configures the arbiter to "scan" the bus request lines from highest priority down to lowest priority and grant the bus to the first requester it finds. Selecting "Priority" configures the arbiter to grant the bus to the highest priority requester at any time. The default is "Round Robin".

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Bus Release

This option is used to select the method that the EPC-9 uses to release the VMEbus for other bus masters to use. Selecting "ROR" (Release on Request) allows the EPC-9 to perform better since it releases the VMEbus only if another bus master requests the bus. Selecting "RONR" (Release on No Request) causes the EPC-9 to release the VMEbus when its current bus access has completed. This has the effect of increasing the performance of other bus masters. Selecting "RWD" (Release When Done) causes the EPC-9 to behave the same as RONR except it does not delay 50ns before attempting to regain control of the bus. The default is "ROR (VME)".

Unique Logical Address

This option is used to select the ULA for the EPC-9. This logical address is used to uniquely identify and access the EPC-9 in a VXI system. The default is ULA "0".

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Exit Menu

The options in this menu allow saving settings and exiting, or abandoning changes and exiting to the system, or controlling the backup and restoration of CMOS RAM to the FBD.

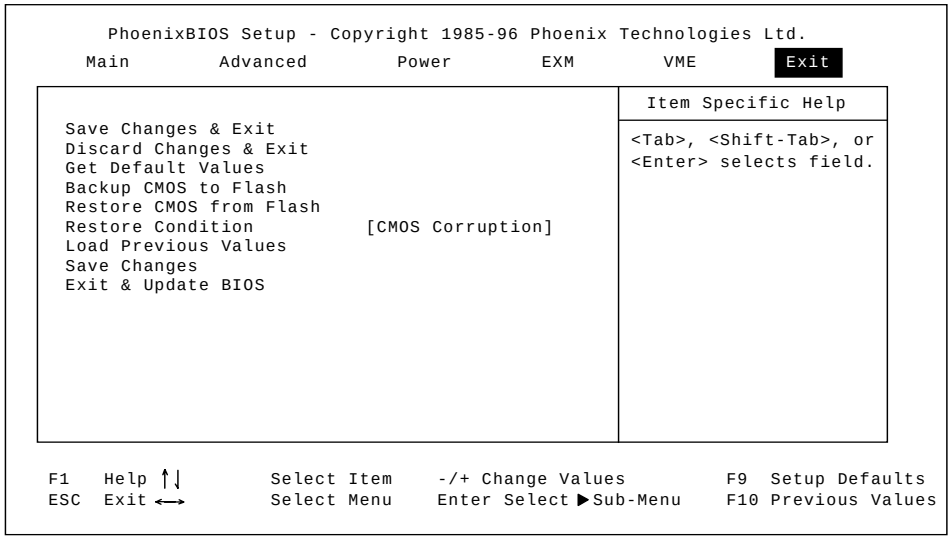


Figure 3-15. Exit Menu.

Save Changes & Exit

This option is used to save into CMOS the values that have been entered and reboot.

Discard Changes & Exit

This option is used to discard the changes just made and revert to the state when Setup was entered. The system reboots with the old values.

Get Default Values

This option is used to reset the Setup values to the original, default values that were set at the factory, before any suppliers or other end users made changes.

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Backup CMOS to Flash

This option is used to immediately save current Setup settings to CMOS RAM and into FBD main block #1.

Restore CMOS from Flash

This option is used to immediately restore CMOS RAM and update current Setup settings from FBD main block #1.

Restore Condition

This option is used to determine under what conditions the System BIOS restores CMOS RAM from FBD main block #1 when booting. The restore conditions are: "Always", "Never", and "CMOS Corruption". The default is "CMOS Corruption".

Load previous values

This option is used to load the system with the previous values before an editing session started.

Save Changes

This option is used to save the edits made during a session.

Exit & Update BIOS

This option is used to initiate a System BIOS update.

NOTE: Do not select this exit option unless you have obtained BIOS update replacement software from your supplier and have reviewed the documentation and procedures provided with that distribution.

If you select this option by mistake, reset the EPC-9 to regain control. The system automatically begins searching for the update program that should be on the floppy disk inserted in drive A. If there is no floppy, you get two series of beep codes: a long and two short beeps, followed by three short beeps that repeat. Cycle the power to reset the system to its previous state.

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Notes

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Chapter 4 - Theory of Operation

Overview

4 4

The EPC-9 is a PCI/ISA/VME bus-compatible computer with standard PC peripherals, and PCI, VME, and EXM bus interfaces.

Physically, the EPC-9 occupies 2 VME slots. A 6U-sized I/O board serves as a motherboard for a processor daughterboard containing the Pentium CPU, system memory, cache memory, a cache and memory controller, a PCI/ISA/IDE bridge chip, a Flash Boot Device, a real-time clock, and a keyboard and mouse controller.

The I/O board connects to the Processor board via PCI and ISA buses, and contains the remaining I/O functions including a Tundra Universe PCI/VME bridge, 10BASE-T and 100BASE-TX Ethernet, two serial ports, two Universal Serial Bus (USB) connectors, an IEEE-1284 bi-directional parallel port, a SCSI-2 port, and connectors for two PCI Mezzanine Cards (PMC) conforming to IEEE specification P1386.1 PMC. The RadiSys PMC-1 Video Module provides VGA resolutions to 1280 x 1024 with 256 colors.

Figure 4-1 provides a diagrammatic overview of the system functional blocks. Most of the standard functions of the PC architecture are embodied in the Intel 82430HX(T2) PCI-based chipset. PC peripheral interfaces for monitor, keyboard, mouse, two serial ports, a parallel port, two Universal Serial Bus (USB) ports, PCI-based SCSI-2, and an RJ45 Ethernet connector are provided at the front panel. An enhanced IDE hard disk controller supports an onboard 2.5" hard disk drive, with provision for two external hard disk drives. An onboard floppy drive connector supports an external floppy disk drive that can be used for installing software and loading and updating flash ROM BIOS and BIOS extensions. A Phoenix NuBIOS with flash update capability allows updating and addition of BIOS extensions. An

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EXM bus, electrically similar to the standard PC ISA bus, is supported through a backplane extender. A watchdog timer and a speaker are provided.

The VMEbus interface uses the Tundra Universe PCI/VME bridge and includes special PAL-based VME byte-order swapping hardware to deal with the difference between Intel and Motorola data representations. Byte-swapping of D16 and D32 accesses only occurs when desired.

4 4

EPC-9 Organization

Block Diagram

The block diagram in Figure 4-1 shows the division and interconnection of EPC-9 functions. These are described below.

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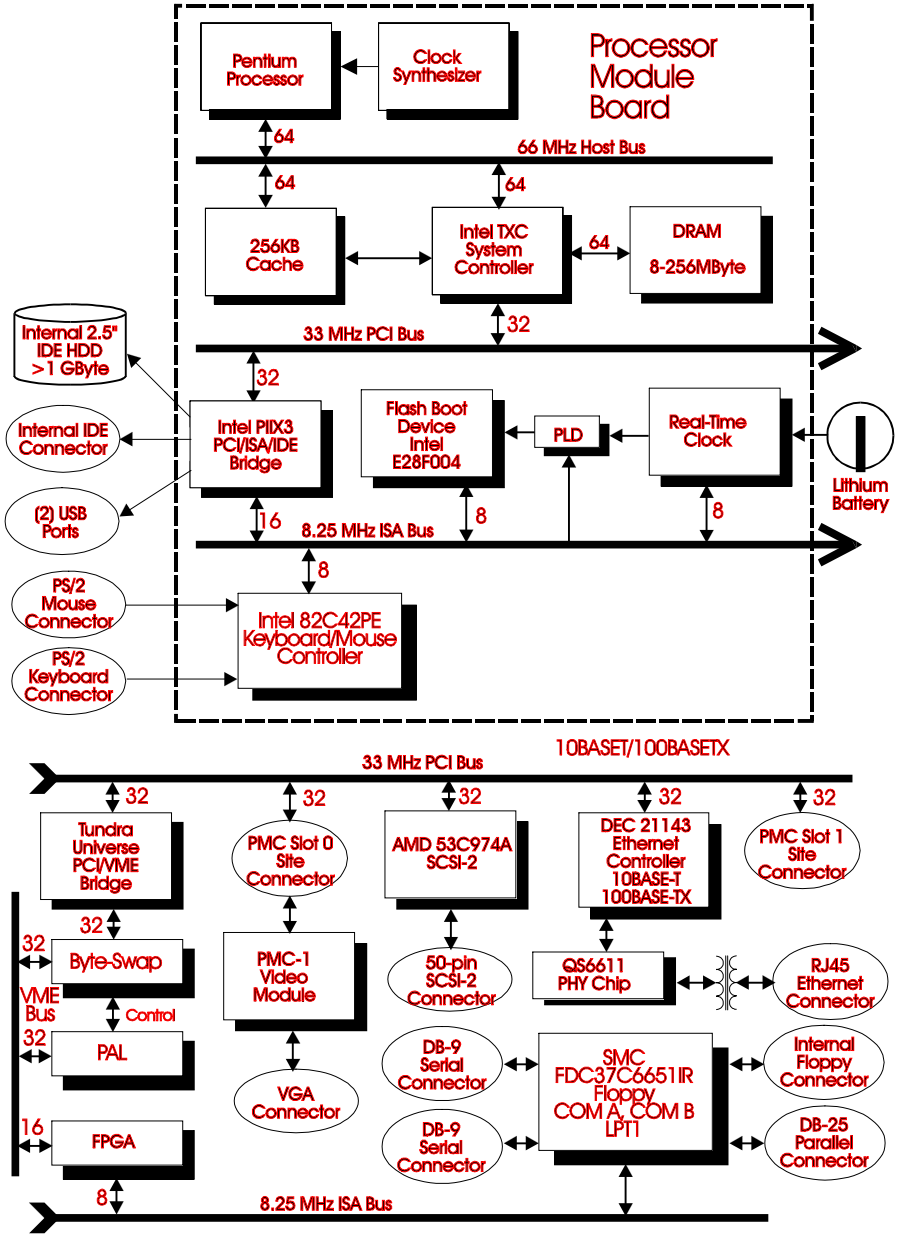


Figure 4-1. EPC-9 Block Diagram.

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4 4

Processor Module Daughterboard

An Intel Pentium processor (with integral FPU) runs at 100, 133, 166, or 200 MHz. The processor, the TXC system controller, and the L2 cache all operate on a 66MHz local bus. The PCIbus runs at half the local bus speed (33MHz) and the ISA bus runs at one quarter the PCI bus speed (8.25 MHz).

Cache Memory

A second-level (L2) write-back 256KByte main-memory cache is implemented by the Intel 82430HX chipset's TXC system controller.

Main System Memory

Main memory is implemented as SODIMM 72-pin socketed 3.3 volt DRAM. The main memory controller supports up to 256MB of 60 or 70 ns Fast Page Mode or EDO DRAM in two dual 72-pin SODIMM sockets. The CPU memory bus is 64 bits wide, so the SODIMM sockets must be populated with identical pairs of 32 bit DRAM modules. The TXC controller generates all of the required control signals, such as RAS#, CAS#, and WE#, as well as the multiplexed addresses for the DRAM array.

Upgrading Main System Memory

At the time of writing, the the following sizes of 60 or 70ns Fast Page Mode or EDO DRAM were useable:

Type	Row/Column	Total Size (MB)	Number of SODIMMs
512Kx32	10/9	4	2
1Mx32	10/9 or 10/10	8	2
2Mx32	10/10 or 10/11	16	2
4Mx32	11/10, 11/11, or12/10	32	2
4Mx32	11/10, 11/11, or12/10	64	4
8Mx32	12/11	128	4
16Mx32	12/12	256	4

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Memory Map

The 2^{32} byte physical address space seen by the Intel Pentium occupies three areas:

1. The area between 0 and 1 MB is largely defined by the IBM PC/AT architecture.
2. The area between 1 MB and 256 MB depends on how much DRAM is installed in the EPC-9.
3. The area above 256 MB, provides direct mapping to the VMEbus with a variety of address modifiers and byte orderings.

Memory at addresses between 0 and 1 MB (0FFFFFh) is mapped as follows:

Range	Content
000000 - 09FFFF	First 640 KB of DRAM (DOS memory)
0A0000 - 0BFFFF	VGA video DRAM, mapped to the PMC-1 Video Module
0C0000 - 0C7FFF	Write-protected DRAM containing shadowed video BIOS
0C8000 - 0CFFFF	SCSI BIOS extension
0D0000 - 0DFFFF	EXMbus
0E0000 - 0E3FFF	Universe bridge registers
0E4000 - 0FFFFF	Shadowed system BIOS

Watchdog Timer

The watchdog timer is a binary counter which, upon overflow, will signal a watchdog timer event. The counter will cause a watchdog event after approximately 125 ms, 1 second or 8 seconds (depending on the value of WDTV, bits 2 and 1 in register 8150h) if the application software does not reset the timer.

An I/O read to address 8150h resets the counter. If WDTR (bit 3 of register 815Dh) is set, the following occurs in response to a timeout event:

WDT (bit 0 of register 8153h) is set. A local "warm" hardware reset occurs and VME SYSFAIL* is asserted. When exiting a hardware reset event, the BIOS checks the condition of WDT. If WDT is set (0), then a watchdog timeout caused the hardware reset. Then, depending on whether the "Halt on watchdog reset" option of the Advanced BIOS Setup menu is enabled, the BIOS will either HALT the CPU or

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allow the boot process to continue. At this point, the software may de-assert VME SYSFAIL* by reading 8150h.

Note that a watchdog hardware reset results in a "warm" hardware reset. A warm hardware reset clears all register bits except for the upper four bits of the Configuration register (these control slot1 arbitration functions) and bit 4 and 6 of the Module Status/Control register. Bit 4 enables the VME bus time-out function and bit 6 enables asserting VME SYSRESET*, if set. A warm reset does clear WDTR (bit 0 of the Module Status) to allow the hardware to be released from the warm reset state, but SYSFAIL will continue to be driven until the WDT bit is cleared by either reading the Module Status/Control Register or by a power-on reset.

If WDTR is clear, WDT mask (bit 0 of register 8153h) enables an interrupt if a time-out event occurs (SYSFAIL is not driven). The clock input to the counter is disabled if the interrupt is pending and not serviced. Service of the interrupt is signaled to the counter by reading register 8150h. This will reset the counter value and resume counting. The interrupt is signaled on IRQ10. The timer event also clears WDT bit in the VME event register (bit 0 of register 8153h).

Application software that utilizes this timer should take care to reset the counter just prior to enabling the interrupt bit in register 8155h. This will inhibit a spurious timer event from occurring just after enabling the timer.

Flash Boot Device

The Intel E28F004BX-T is used as a Flash Boot Device (FBD). This is flash-updatable BIOS containing the boot, main, and parameter blocks shown in Figure 4-2 and shadowed at the top of 32-bit address space. The use of the FBD allows reprogramming of the main and parameter blocks of the BIOS.

The Plug-and-Play ESCD is also stored in the Boot-Block FLASH device in the block addressed from FFFA0000h-FFFBFFFFh. This block is always accessible for re-programming.

The boot block is NEVER reprogrammed by the user, even when the main and parameter blocks are reprogrammed. The capability to program the boot block is provided to facilitate changes by RadiSys manufacturing.

A “forced recovery” jumper is provided that is connected to the P1-3 input of the 82C4PE keyboard controller. This jumper is readable by the boot block and can force the boot block to initiate a recovery sequence at power-up should other methods of initiating the sequence become inaccessible. (i.e. crisis recovery)

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The system BIOS is shadowed in write protected DRAM at 000E4000h-000FFFFFh during system boot.

The flash BIOS device is memory addressed and resides in the last 512KByte of system memory at address FFF80000h to FFFFFFFFh.

Keyboard/Mouse Controller

The Intel 82C42PE mouse/keyboard controller can interface to most standard PC mice and keyboards with PS/2-style connectors. The keyboard controller uses interrupt IRQ1 and the mouse uses IRQ12. An adapter cable is shipped with the EPC-9 to allow standard PC/AT keyboards with larger 5-pin connectors to plug into PS/2 connectors.

BIOS ROM and ROM Shadowing

The EPC-9 utilizes a Flash Boot Device (FBD) as its BIOS ROM. The BIOS ROM is mapped into the top of the processor's 32-bit address space. The BIOS consists of a 16 KByte boot block and the System BIOS in the 96KB Main block and both 8KB parameter blocks. The layout is described in Figure 4-2.

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Physical Address		Device Offset
FFFFFFFFh	Boot Block 16 KB	7FFFFh
FFFFC000h	BIOS Recovery Code	7C000h
	Parameter Block 2 8 KB	7BFFFh
FFFFA000h	System BIOS	7A000h
	Parameter Block 1 8 KB	79FFFh
FFFF8000h	System BIOS	78000h
	Main Block 4 96 KB System BIOS, PCI BIOS	77FFFh
FFFE0000h	Plug n Play BIOS	60000h
	Main Block 3 128 KB User Extensions (88KB) Manufacturing BIOS (8KB)	5FFFFh
FFFC0000h	SCSI BIOS (32KB)	40000h
	Main Block 2 128 KB	3FFFFh
FFFA0000h	ESCD (4KB)	20000h
	Main Block 1 128 KB	1FFFFh
FFF80000h	CMOS Data (1KB)	00000h

Figure 4-2. Flash Boot Device Memory

The BIOS initialization software copies the ROM contents into DRAM (a process called *shadowing*) at addresses 0E0000h-0FFFFFh. The VGA BIOS is copied into 0C0000h-0C7FFFh of DRAM. After copying into these areas, the BIOS write-protects them. Subsequent writes to these areas complete successfully but do not alter the data in DRAM.

There are two parameter blocks, each 8 KB in size, used for BIOS code.

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CMOS Backup and Restore

CMOS memory is backed up to and restored from Main Block 1 of the FBD as determined by the settings in the BIOS Setup Exit Menu. This allows you to save your settings to nonvolatile flash memory and to specify the conditions under which CMOS is to be restored from the FBD. For more information, see the Exit Menu section of *Chapter 3 - BIOS Configuration.*

I/O Motherboard

Ethernet Controller

The EPC-9 implements 10/100BaseT Ethernet communications by using the DEC 21143 10BASE-T and 100BASE-TX Ethernet Controller coupled to a QSI 6611 Physical Interface (PHY) chip. The 21143 chip interfaces to the 32-bit PCI bus and the QS6611 provides the line driver and receiver for a 10BASE-T and 100BASE-TX Fast Ethernet connection to Category 5 unshielded twisted-pair cable via an RJ45 connector. The QS6611 also provides wave shaping and line filtering for both 10- and 100-Mbps operation, adaptive equalization, baseline wander compensation, 10/100 switching, and clock generation and recovery.

This controller uses PCI INTB and Bus Arbitration channel 0, which are shared with PMC slot 0. It is configured through the PCI Configuration Space. The internal Ethernet controller must be disabled (via the BIOS setup Integrated Peripherals menu) whenever a PMC requiring PCI bus mastering is installed in PMC slot 0.

The Ethernet driver for Windows NT/4.0 is supplied by Digital Equipment Corporation and is supplied on a separate floppy diskette.

Product: DC21X4.SYS
Software revision: 4.15
Document release date: 1-6-97

Battery

The battery powers the CMOS RAM and TOD clock when system power is not present. At 60°C, the battery should have a shelf life of over four years. In a system that is powered on much of the time and where the ambient power-off temperature is less than 60°C, the battery is estimated to have a life of 10 years.

If system power is present, the +5V voltage also powers the CMOS RAM and TOD clock. This is done with the RTC chip's internal isolation diodes, so that either the

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onboard battery or the +5V power supply voltage can supply power and neither power source affects the other.

The 3.0V lithium battery supplied with the EPC-9 is a Ray-O-Vac BR2335 "coin cell" or equivalent. It is mounted at the rear of the Main I/O Board, beneath the EPC-9 Carrier Board. Should the battery fail, you may obtain and install a replacement.

Write down all of the CMOS setup parameters while the battery is still good, or save them, using the CMOS save and restore feature of the BIOS configuration Exit Menu.

To replace the battery:

1. Turn off the power and remove the EPC-9 from the VME chassis.

IMPORTANT: You should perform all of these steps in a static-free or ESD-protected environment.

1. Refer to the procedures in *Appendix G - SVGA and the PMC-1 Video Module*, and remove the PMC-1, then remove the EPC-9 Carrier Board.

2. Locate the battery, then lift the top retaining contact clip slightly and slide the old battery out in the direction shown in Figure 4-3.

3. Slide the new battery into place, positive (+) side up

4. Reassemble the EPC-9.



Figure 4-3. Replacing the Lithium CMOS Battery.

Peripheral Ports

The I/O address and IRQ of the peripheral ports are determined by the CMOS parameters established by default and modified via BIOS Setup screens. These include

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(2) RS-232 Serial Ports, a bidirectional parallel port, and (2) Universal Serial Bus (USB) ports. The RS-232 ports and the parallel ports, along with the floppy disk controller, are implemented by the SMC FDC37C665IR Super I/O Chip.

RS-232 Ports

The RS-232 ports are standard PC COM serial ports based on the 16550 architecture. COM A is normally mapped to I/O address 3F8h-3FFh and uses interrupt IRQ4. If not needed, COM B can be disabled in the BIOS Setup Integrated Peripherals Sub-Menu to free up the I/O address and interrupt for usage by other expansion products. COM B is mapped to I/O address 2F8h-2FFh and uses interrupt IRQ3.

Parallel Port

The printer port is a bi-directional IEEE1284-C PC parallel port. The parallel port supports bi-directional communication compatible with the PS/2 definition. It is configured as LPT1 and mapped to I/O address 378h-37Fh and uses interrupt IRQ7. If not needed, LPT1 can be disabled in the BIOS Setup Integrated Peripherals Sub-Menu to free up the I/O address and interrupt for usage by other expansion products.

USB Ports

The Universal Serial Bus (USB) controller is a host/hub controller and moves data between the main system memory and devices on the serial bus. The USB controller also includes the first level hub. This permits connection of two USB peripheral devices directly to the PIIX3 without an external hub. If more devices are required, an external hub can be connected to any one of the built in ports.

USB architecture has the concept of all devices connected to it being serviced through two software layers known as SBS (serial bus services) and HCS (host controller services). SBS allocates the necessary bandwidth for every device connected on the bus and builds a scheduler to service these devices at the required intervals. SBS passes the schedule information to the HCS layer. The HCS uses this information to build a schedule table and command blocks that hardware understands. The schedule table and command blocks are located in the system memory and contain information including the addresses for data movements to/from system memory. The current implementation of the USB support software may not support these features at initial product availability.



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Two host-side USB ports are provided on the front panel. The USB root hub is built into the PIIX3 chip as part of the 82430HX chip set. The USB's PCI configuration registers are located as function 2 of the PIIX3 configuration space.

Floppy Controller

The SMC FC37C665IR Super I/O chip, used to implement the serial and parallel ports, is also used to implement a standard PC floppy disk port. The device resides on the ISA bus, and is accessed at the standard PC I/O addresses of 3F0h-3F7h. Interrupts are signaled on IRQ6.

The floppy interface connector is located on the I/O board and is not available at the front panel because it is normally only used for diagnostics or for initializing the hard disk(s).

PCI/VME Bridge

The VMEbus interface on the EPC-9 is controlled by a single chip: the Tundra Semiconductor, Universe PCI/VME bridge. The Universe controls a layer of buffers between it and the VMEbus, and has a glueless interface to the PCIbus.

The VMEbus interface uses both the P1 and P2 connectors to allow an addressing space of A16/A24/A32 with D08/D16 and D32 data accesses. It uses PCI INTD and bus mastering lines. The VME bus interface includes the following features:

1. Full VMEbus System Controller (Slot 1) features including bus arbiter, bus timeout, IACK daisy chain driver, SYSCLK driver.

2. Master control in A16/A24/A32 address spaces for D08/D16 and D32 data widths

3. Responds as D08/D16 and D32 slave in A16/A24/A32 address spaces.

4. Generates and responds to all 7 VMEbus interrupts.

5. VME registers can be accessed from either the Pentium or VMEbus.

The EPC-9 presents a single load on all VMEbus signals.

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For more information about programming the VMEbus interface, see *Chapter 5 - Programming the VMEbus Interface.*

PMC-1 Video Module

The EPC-9 uses the PMC-1 Video Module for SVGA support. The PMC-1 uses a Cirrus Logic CL-GD5446. The video module connects to the PCIbus and has 2MB of VGA memory, and resolutions from 640 x 480 (256 colors) to 1280 x 1024 (256 colors). The PMC-1 is described in full detail in *Appendix G - SVGA and the PMC-1 Video Module.*

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Front Panel LEDs

The EPC-9 has eight LEDs in the top left corner of the front panel. These LEDs are described below:

TEST(yellow)	This LED is lit whenever the system is running its power-on self-test, as reflected in the PASS bit in the VXI registers. If PASS is 0, then this LED is lit. This only occurs during a hardware reset.
SYSFAIL(red)	This LED is lit whenever the VME SYSFAIL line is asserted if the EPC-9 is jumpered to be the Slot-1 controller. This occurs independent of which VME board is driving the SYSFAIL line. It comes on whenever the system receives a hardware reset and remains on until the initial power-on self-tests have completed.
RUN(green)	This LED is lit whenever a write access to DRAM is made. This provides a normally lit LED indicating that the CPU is operating. This LED is not lit if the CPU is halted or is executing entirely out of the on-chip cache.
MASTER (green)	This LED is lit whenever the EPC-9 is bus master.
SCSI (green)	This LED is lit when the SCSI port is active.
SLAVE (green)	This LED is lit whenever the EPC-9 is accessed as slave on the VME bus.
IDE (green)	This LED is lit whenever the IDE bus is active. This indicates a read or write to or from the onboard hard disk or other device connected to the IDE controller.
ETHERNET	This LED is lit when the Ethernet port is active.

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Resetting the EPC-9

There are a number of ways to reset (reboot) the EPC-9.

Power-off, Power-on

Known as a cold hardware reset. This causes all boards in the VMEbus to reset. The system runs the power-on self-tests and reboots the OS.

Power low

"Warm" hardware reset. When power is detected between ~3.0 and ~4.5V, the system runs the Power On Self Test (POST) and reboots the operating system. When power is less than ~3.0V, the system performs a cold hardware reset.

Front panel Reset button

"Warm" hardware reset. The Reset button causes the EPC-9 to perform a hardware reset. The system runs the power-on self-tests and reboots the operating system.

Ctrl+Alt+Del

"Warm" software reset. This keyboard sequence is also called a "warm boot". The EPC-9 does not reinitialize all of the processor's hardware. However, the operating system is reloaded.

VMEbus SYSRESET

"Warm" hardware reset. The EPC-9 can be software-configured to respond or not respond to the VMEbus SYSRESET* line. Asserting bit 7(SRIE) of register 8144h allows the VME SYSRESET* signal to reset the EPC-9. The reset semantics are the same as the front panel reset.

Watchdog Timer

"Warm" hardware reset. Same as a front panel reset button except that SYSFAIL is asserted until the watchdog timer is cleared.



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EXM Expansion Interface

The EXM expansion interface is electrically similar to the PC/AT ISA (16-bit data) bus. In addition, it contains a signal EXMID* used for dynamic recognition and configuration of EXMs. EXMs respond to one or more I/O addresses in the range 100h - 105h only when their EXMID* line is asserted. EXMs are required to return a unique EXM ID byte in response to a read from I/O address 100h.

This ID byte is the same identification byte discussed earlier in *Chapter 3 - BIOS Configuration* in the section on the *EXM Menu*.

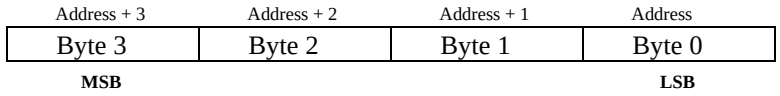
The EXM expansion interface is provided on rows A, C, and D of the EPC-9's 4-row DIN P2 connector. The subplane carries the EXM interface to other modules, such as to EXM modules and the EXP-MX Mass Storage module. These EXM interface signals are not passed through to the VMEbus.

Further information on the EXM expansion interface, its connectors, and standards for building EXMs is available upon request.

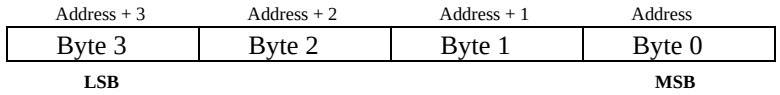
Notes on Byte Ordering

There are two fundamentally different ways of storing numerical values in byte locations in memory:

- Little endian, characteristic of Intel microprocessors, where the **least**-significant data byte (LSB) is stored in the lowest byte address



- Big endian, characteristic of Motorola microprocessors and the VMEbus environment in general, where the **most**-significant data byte (MSB) is stored in the lowest byte address



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The EPC-9 contains programmable byte-swapping hardware to allow programs to read or write VMEbus memory in either byte order. The EPC-9 uses the Tundra Universe supervisor address modifier bit, AM bit 2, to control byte-swapping. This bit is emitted by the Universe chip and intercepted by the EPC-9 byte-swap control hardware which uses it to control whether or not byte-swapping occurs. The EPC-9 always asserts AM bit 2 to the VMEbus, so only supervisor accesses are possible.

The four slave images written to VMEbus memory are controlled by setting the Universe's SUPER bitfield (bits 12 and 13) of the four Slave Image Control Registers (LSI0_CTL through LSI3_CTL). Setting SUPER to 01 disables swapping, producing an Intel (little-endian) image, while setting SUPER to to 00 enables swapping, producing a Motorola (big-endian) image. You use little-endian images to map VMEbus memory to another Intel processor and big-endian images to map VMEbus memory to a Motorola processor.

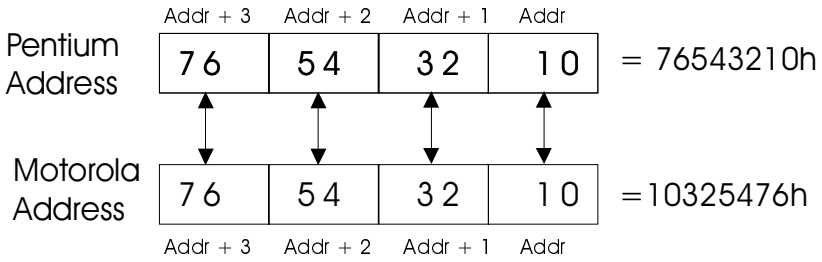
The Slave Image Control Registers are described in the *Universe User's Manual*, available on the world-wide web at: http://www.newbridge.com/Tundra/Products/Bus/BPI/Univdn.html. The particular control registers for each image are described in *Appendix A.*

Slave Image Control Register	**Offset**
LSI0_CTL	100h
LSI1_CTL	114h
LSI2_CTL	128h
LSI3_CTL	13Ch

When you perform a single byte (D08) access, the byte order makes no difference. However, word (D16) or double-word (D32) accesses may require byte-swapping.

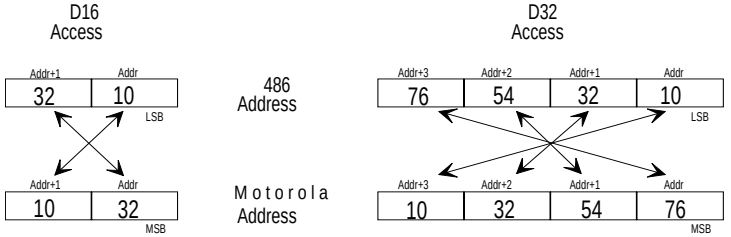
When you select little-endian, bytes pass straight through unchanged. You should only use little endian when you read or write data between two Intel processor systems. The result of using little-endian byte ordering to transfer a double-word integer between an Intel processor and a Motorola processor are shown below.

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Since the Pentium processor uses Addr as the least-significant byte and the Motorola processor uses Addr as the most-significant byte, the processor receiving the data gets a "scrambled" value.

When big-endian is selected, the bytes are swapped between the Pentium and VME. See the diagram below.



When using big-endian byte ordering, take care to assure that the VME address is aligned on a boundary. For D16 accesses, the VME address must be on a word boundary (address evenly divisible by 2). For D32 accesses, the VME address must be on a double-word boundary (evenly divisible by 4). Failure to properly align addresses results in "scrambled" data. Although the VMEbus address must be boundary-aligned to match the data width (word or double-word), the Pentium address does not need to be boundary-aligned.

You must also consider the compiler you are using, because some compilers produce two 16-bit accesses when a 32-bit access is desired, resulting in scrambled data.

When transferring a 32-bit floating-point number, take care to assure that both processors use the same floating-point format and that both systems expect the mantissa and exponent in the same byte locations. As long as these match, floating-point number transfers will work correctly. Since 64-bit floating-point number transfers are not supported in hardware, use two 32-bit transfers with little-endian byte order and then accomplish the byte-swap in software.

The EPConnect Bus Manager software provides a means of selecting the byte ordering during memory-copy operations.

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Chapter 5 - Programming the VMEbus Interface

Overview

The VMEbus is controlled by the Tundra Universe PCI-VME bridge chip. Active access to the VMEbus is achieved by reading and writing to registers in the Universe memory space. Because of dependencies between the PCI and VME sides of those registers which are ported to both busses, considerable care must be exercised in both reading and writing to these registers. For all but the most basic programming, try using the programming interface provided by the RadiSys EPConnect software instead of working directly with the VMEbus registers.

Register Initialization

At power-on-self-test (POST) time, a subset of the VME registers is initialized by the BIOS. The Universe chip then initializes the remainder of the VME registers. This is controlled by how the Universe chip is programmed.

Programming the Universe

The Universe chip can become system controller if the EPC-9 is in slot 1. It does this by sampling the VME signal BG3IN*. If BG[3:0] is low after reset, which it is, due to the Universe's internal pull-down, then the EPC-9 is in slot 1 and the Universe becomes system controller. When the Universe is the System Controller, its IACK daisy chain driver and SYSCLK driver are also activated.

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VMEbus Arbitration

The bus arbiter supports the following arbitration modes:

- Fixed Priority Arbitration (PRI)
- Single Level arbitration (SGL), which is a subset of PRI
- and Round Robin arbitration (RRS), which is the default setting.

The arbitration mode is selected in the Universe MISC_CTL register. The arbiter can be programmed to timeout if the requester does not assert BBSY* within a specified period. The timeout can be set to 16 us, 256 us, or disabled also via the MISC_CTL register. 16 us is the default.

VMEbus Timeout

A programmable bus timer allows the VMEbus timeout period to be selected via the MISC_CTL register. It can be programmed to 16 us, 32 us, 64 us, 128 us, 256 us, 512 us, 1024 us, or disabled. The default setting is 64 us. If a bus transaction times out, the timer asserts the VMEbus BERR* signal.

VMEbus Requester

The Universe is software-configurable to request bus ownership on all VMEbus request levels: BR3*, BR2*, BR1*, and BR0*. The default request level is BR3*. Demand Mode is the default request mode.

The VMEbus requester can be configured in either Release-When-Done (RWD) or Release-On-Request (ROR) mode. The default bus release mode is RWD.

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VMEbus Master Accesses

The EPC-9 becomes VMEbus Master in the following situations:

1. When the Pentium accesses resources on the VMEbus
2. When the Universe DMA controller performs block-transfer operations.
3. When the Universe generates interrupt-acknowledge cycles as the VMEbus interrupt handler
4. When the Universe VMEbus ownership bit (VOWN in the MSTR_CTL register) is set.

The board can perform master accesses in A16, A24 and A32 address spaces using D08/D16 and D32 data widths. Read accesses to the VMEbus are always coupled, while write accesses may either be posted or coupled. Write accesses default to coupled.

The Universe provides four programmable windows into VMEbus memory (PCI Slave images). The characteristics of the these windows are programmed in the LSIn_CTL, LSIn_BS, LSIn_BD, and LSIn_TO registers of the Universe chip. Please refer to the *Universe User Manual* for programming details.

VMEbus block transfers are supported by the Universe using its on-chip DMA controller.

The EPC-9 can respond as a VMEbus Slave in either A24 or A32 address spaces. It responds to either D08, D16 or D32 accesses. Read accesses from the VMEbus to onboard memory may be either coupled or prefetched (for block transfers), while write accesses may either be posted or coupled. Both reads and writes default to coupled.

The Universe provides four programmable windows into PCI memory (VME Slave images). The characteristics of the these windows are programmed in the VSIn_CTL, VSIn_BS, VSIn_BD, and VSIn_TO registers of the Universe chip. Please refer to the *Universe User Manual* for programming details.

By default, none of the Universe slave images are used or programmed in the EPC-9.

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VMEbus Locked Accesses (RMW)

Each of the four PCI Slave images support VMEbus Read-Modify-Write (RMW) cycles, if so programmed. This causes a non-block VMEbus RMW read cycle to generate a coupled PCI locked read cycle. PCI ~LOCK is then asserted on the PCI bus until AS* is negated on the VMEbus.

VMEbus Interrupter

The Universe VME controller provides a flexible scheme to map interrupts to either the PCI bus or the VMEbus. This mapping is controlled in the LINT_EN, LINT_MAP0, LINT_MAP1, VINT_EN, VINT_MAP0, and VINT_MAP1 registers.

The following interrupts can be mapped to any of the VMEbus IRQ* pins.

- PCI bus errors
- VMEbus errors
- DMA interrupts
- Software interrupts

If a software and a hardware source are both mapped to the same IRQ*, the software source has higher priority.

When an IACK cycle on the VMEbus is detected that matches an interrupt level that the EPC-9 is asserting (and the IACKIN daisy chain is asserted into the EPC-9), the Universe responds by supplying an 8-bit STATUS/ID vector. This vector is programmable through the STATID register. When the IACK cycle is complete, the Universe releases the VMEbus and the interrupt vector is passed to the PCI master (Pentium). Software interrupts are Release-On-Acknowledge (ROAK), while hardware and internal interrupts are Release-On-Register-Access (RORA).

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VMEbus Access to Universe Registers

As mentioned earlier, the Universe can be programmed to make its registers accessible from the VMEbus. The Universe will power-up with VMEbus access to its registers disabled, and it can be later programmed by application software to enable them for VMEbus access. This functionality is controlled by programming the VRAI_CTL and VRAI_BS registers.

PCIbus Access to Universe Registers

The Universe is defined as a PCI device, therefore it must provide a standard set of 64 DWORD-wide registers within the PCI Configuration Space. They are selected by asserting the Universe IDSEL signal on a Configuration Space access. Since the Universe registers consume a 4K block of memory, only the first 256 registers can be accessed through Configuration Space. The remaining registers must be accessed through memory or I/O space.

This 4KB block is also larger than the available area left in the I/O space. Therefore, the registers are memory mapped. The base address of the registers must reside on a 64KB boundary, so they are placed at E0000h. The entire register set is accessible in the E0000h-E3FFFh range.

For More Programming Information…

Complete programming information about the Tundra Universe chip is maintained in the most current version of the *Universe User Manual*, available online at http://www.newbridge.com/Tundra/Products/Bus/BPI/Univdn.html

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Notes

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Chapter 6 -
Support and Service

In North America

Technical Support

RadiSys maintains a technical support phone that is staffed weekdays (except holidays) between 8:00 AM and 5:00 PM Pacific time. If you require assistance outside these hours, you can leave a message on voice-mail using the same phone number. You can also request help via electronic mail or by FAX addressed to RadiSys Technical Support Department. See the cover of this manual for the RadiSys telephone and FAX numbers. The RadiSys e-mail address on the internet is ***support@radisys.com***. If you are sending e-mail or a FAX, please include information on both the hardware and software being used and a detailed description of the problem, specifically how the problem can be reproduced. We will respond by e-mail, phone or FAX by the next business day.

Technical support services are designed for customers who have purchased their products from RadiSys or an authorized sales representative. If your RadiSys product is part of a piece of OEM equipment, or was integrated by someone else as part of a system, support will be better provided by the OEM or system vendor that did the integration and understands the final product and environment.

World Wide Web

RadiSys maintains an active site on the world wide web. The home-page URL is *http://www.radisys.com*. The site contains current information about the company and locations of sales offices, new and existing products, contacts for sales, service, and technical support information. You can also send e-mail to RadiSys using the web site. Requests for sales, service, and technical support information receive prompt response.

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Repair Services

RadiSys provides Factory Repair Service for the entire RadiSys product line. Standard service for all RadiSys products covers factory repair with customers paying shipping to the factory and RadiSys paying for return shipment. Overnight return shipment is available at customer expense. Normal turn-around time for repair and re-certification is five working days.

Quick Exchange services (immediate shipment of a loaner unit while the failed product is being repaired) are available. Negotiate these or other extra-cost services in advance to allow RadiSys to pool the correct product configurations. RadiSys does not maintain a general "loaner" pool: units are available only for customers who have negotiated this service in advance.

RadiSys does not provide a fixed-price "swap-out" repair service. Many customers indicate that issues of serial number tracking and version control make it more convenient to receive their original products back after repair.

Warranty Repairs

RadiSys will repair at no charge products having manufacturing defects during the warranty period. See the warranty information at the front of this manual. Products without fault sent in for warranty repair will be subject to a recertification charge. Extended warranties are available at a standard price for any product still under original warranty. RadiSys will gladly quote prices for extended warranties on products with lapsed original warranties; contact the factory if this applies.

Customer induced damage (resulting from misuse, abuse, or exceeding the product specifications) is not covered by warranty.

Non-Warranty Services

There are several classes of non-warranty service. These include repair of customer induced problems, repairs of failures for products outside the warranty period, recertification (functional testing) of a product either in or out of warranty, and procurement of spare parts.

All non-warranty repairs are subject to service charges. RadiSys has determined that pricing repairs based on time and materials is more cost-effective for the customer than a flat-rate repair charge. RadiSys analyzes the product after it is received. When instructed to do so, RadiSys informs the customer of repair costs for authorization.

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After the customer authorizes repairs and makes billing arrangements, RadiSys repairs the product and returns it to the customer.

RadiSys provides a recertification service for products either in or out of warranty. This service verifies correct operation of a product by inspecting and testing the product using standard manufacturing tests. There is a product-dependent charge for recertification.

Generally, very few components are field-repairable. However, since RadiSys understands that some customers want or need the option of repairing their own equipment, all components are available in a spares program. RadiSys charges a minimum billing for this program.

Arranging Service

To schedule service for a product, please call the RadiSys Technical Support Department. The telephone number appears on the cover of this manual. Have the product model and serial numbers available, along with a description of the problem. A technical support representative will issue a Returned Materials Authorization (RMA) number, a code number by which RadiSys tracks the product while it is being processed. Once you receive the RMA number, follow the instructions of the technical support representative and return the product to RadiSys, freight prepaid. Mark the RMA number clearly on the exterior of the package. If possible, re-use original shipping containers and packaging. In any case, be sure you follow good ESD-control practices when handling the product. Use anti-static bags and packing materials with adequate padding and shock-absorbing properties.

Before you ship the product, include the following information: return address, contact names and phone numbers in purchasing and engineering, and a description of the problem. If available, include ancillary information related to the problem.

Ship the product, freight prepaid, to the RadiSys Product Service Center at the address shown on the front cover of this manual.

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Other Countries

Use the RadiSys world wide web site to contact us, or contact the sales organization from which you purchased your RadiSys product for service and support. The RadiSys world wide web URL is *http://www.radisys.com*.

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Appendix A - Chipset & I/O Map

The following defines the I/O addresses decoded by the EPC-9. Only the A9-A0 bits are decoded for the registers between 200h and 3FFh. For the I/O addresses above 8000h, A15 and A9-A0 are decoded.

First (8-bit) DMA controller		
I/O Addr	Functional group	Usage
000	DMA	Channel 0 address
001		Channel 0 count
002		Channel 1 address
003		Channel 1 count
004		Channel 2 address
005		Channel 2 count
006		Channel 3 address
007		Channel 3 count
008		Command/status
009		DMA request
00A		Command register (R)
		Single-bit DMA req mask(W)
00B		Mode
00C		Set byte pointer (R)
		Clear byte pointer (W)
00D		Temporary register (R)
		Master clear (W)
00E		Clear mode reg counter (R)
		Clear all DMA req mask(W)
00F		All DMA request mask

First Interrupt controller		
I/O Addr	Functional group	Usage
020	Interrupt controller 1	Port 0
021		Port 1

Counter-Timer functions		
I/O Addr	Functional group	Usage
040	Timer	Counter 0
041		Counter 1
042		Counter 2
043		Control (W)

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A A

Keyboard Port		
I/O Addr	Functional group	Usage
060	Keyboard controller	Data I/O register
061	NMI status	NMI status
064	Keyboard controller	Command/status register

Time-of-Day Clock			
I/O Addr	Functional group	Usage	
070	Real-time clock	RTC index reg / NMI enable	
071		RTC data register (64 bits)	
		0	seconds
		1	seconds alarm
		2	minutes
		3	minutes alarm
		4	hours
		5	hours alarm
		6	day of week
		7	date of month
		8	month
		9	year
		A	status A
		B	status B
		C	status C
		D	status D
		E-3F	RAM

Phoenix NuBIOS		
I/O Addr		Usage
080		Phoenix BIOS Status Information

DMA Page Registers		
I/O Addr	Functional group	Usage
081	DMA	Channel 2 page register
082		Channel 3 page register
083		Channel 1 page register
087		Channel 0 page register
089		Channel 6 page register
08A		Channel 7 page register
08B		Channel 5 page register
08F		Refresh page register

Port A		
I/O Addr	Functional group	Usage
092	Port A	Fast A20 and reset control

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EXM Configuration		
I/O Addr	Functional group	Usage
096	EXM Config	EXM slot register (part of the subplane)
100		EXM IDs (on each EXM module)
102		EXM option byte 1 (slot specific)
103		EXM option byte 2 (slot specific)

Second Interrupt Controller		
I/O Addr	Functional group	Usage
0A0	Interrupt controller 2	Port 0
0A1		Port 1

Power Management Controller		
I/O Addr	Functional group	Usage
0B2	Power Management	Control
0B3		Status

DMA Controller		
I/O Addr	Functional group	Usage
0C0	DMA	Channel 4 address
0C2		Channel 4 count
0C4		Channel 5 address
0C6		Channel 5 count
0C8		Channel 6 address
0CA		Channel 6 count
0CC		Channel 7 address
0CE		Channel 7 count
0D0		Command/status
0D2		DMA request
0D4		Command register (R)
		Single-bit DMA req mask(W)
0D6		Mode
0D8		Set byte pointer (R)
		Clear byte pointer (W)
0DA		Temporary register (R)
		Master clear (W)
0DC		Clear mode reg counter (R)
		Clear all DMA req mask (W)
0DE		All DMA request mask
0E0		Phoenix BIOS Status Information

Coprocessor Interface		
I/O Addr	Functional group	Usage
0F0	Coprocessor	Clear coprocessor busy
0F1		Reset coprocessor

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IDE Control		
I/O Addr	Functional group	Usage
1F0	IDE Control	Data Register
1F2		Sector Count
1F3		Sector Number
1F4		Cylinder LSB
1F5		Cylinder MSB
1F6		Drive/ Head
1F7		Status/ Command

ISA Plug and Play		
I/O Addr	Functional group	Usage
279	Plug and Play	
A79		Data Register
CF8		Configuration Address Register
CF9		Turbo reset control register
CFC		Configuration data register

Serial I/O (COM B) Port		
I/O Addr	Functional group	Usage
2F8	COM B serial port	Receiver/transmitter buffer
		Baud rate divisor latch (LSB)
2F9		Interrupt enable register
		Baud rate divisor latch (MSB)
2FA		Interrupt ID register
2FB		Line control register
2FC		Modem control register
2FD		Line status register
2FE		Modem status register

Parallel I/O (LPT1) Port		
I/O Addr	Functional group	Usage
378	LPT1 parallel port	Printer data register
379		Printer status register
37A		Printer control register

EPP Registers		
I/O Addr	Functional group	Usage
37B	EPP	Address Port
37C		Data Port 0
37D		Data Port 1
37E		Data Port 2
37F		Data Port 3

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VGA		
I/O Addr	Functional group	Usage
3B4	VGA	CRT Controller index
3B5		CRT Controller data
3BA		Feature control output, Input status
3C0		Attribute controller Index/Data
3C1		Attribute controller Index/Data
3C2		Miscellaneous output, Input status
3C3		Sleep
3C4		Sequencer Index
3C5		Sequencer Data
3C6		Video DAC pixel mask, Hidden DAC register
3C7		Pixel address read mode, DAC state
3C8		Pixel mask write mode
3C9		Pixel data
3CA		Feature control readback
3CC		Miscellaneous output readback
3CE		Graphics controller index
3CF		Graphics controller data
3D4		CRT controller index
3D5		CRT controller data
3DA		Feature control, pinput status
3F0		Configuration 37C651 Super I/O Combo chip
3F1		Configuration 37C651 Super I/O Combo chip
46E8	VGA	Adapter Sleep

Serial I/O (COM A) Port		
I/O Addr	Functional group	Usage
3F8	COM A serial port	Receiver/transmitter buffer
		Baud rate divisor latch (LSB)
3F9		Interrupt enable register
		Baud rate divisor latch (MSB)
3FA		Interrupt ID register
3FB		Line control register
3FC		Modem control register
3FD		Line status register
3FE		Modem status register

Interrupt Control Registers		
I/O Addr	Functional group	Usage
4D0	Interrupt	Edge/ level control - Int1
4D1		Edge/ level control - Int2

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ECP Registers		
I/O Addr	Functional group	Usage
778	ECP	Data FIFO/ Config Register A
779		Data FIFO/ Config Register B
77A		Extended Control Register

VME and Misc		
I/O Addr	Functional group	Usage
814C	VME and Misc	Message High register
814D		Message High register
814E		Message Low register
814F		Message Low register
8150		Control
8151		ULA register
8152		VME Event State register
8153		VME Event Enable register
8154-8155		Status/ control register
8156		Model register
8158-8159		Signal FIFO register
8162-8163		IACK latch 1 register
8164-8165		IACK latch 2 register l
8166-8167		IACK latch 3 register
8168-8169		IACK latch 4 register
816A-816B		IACK latch 5 register
816C-816D		IACK latch 6 register
816E-816F		IACK latch 7 register

ULA - Relative VXI Registers in VME Address Space		
I/O Addr	Functional group	Usage
0-1	VXI	ID/ULA register
2-3		Device type register
4-5		Status/ Control register
6-7		Reserved
8-9		Protocol register
A-B		Response register
C-D		Message High Register
E-F		Message Low Register

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Appendix B - Interrupts and DMA Channels

B B

Interrupts

The assignment of interrupts for the EPC-9 is shown in the following table:

NMI	DRAM parity error, EXM expansion interface I/O channel check asserted
IRQ0	timer
IRQ1	keyboard controller
IRQ2	IRQ8 - IRQ15 cascade through IRQ2
IRQ3	COM B serial port if enabled
IRQ4	COM A serial port if enabled
IRQ5	Ethernet or unassigned
IRQ6	floppy disk controller if enabled
IRQ7	LPT1 parallel port
IRQ8	real-time clock
IRQ9	Universe Bridge (routed to INTD)
IRQ10	One of (11) interrupts or events: (7) VME interrupts, VME ACFAIL, VME SYSFAIL, VME BERR, watchdog timer event
IRQ11	SCSI or unassigned
IRQ12	mouse
IRQ13	numeric coprocessor
IRQ14	Primary IDE
IRQ15	Secondary IDE
SMI	Power Management
INTA	PMC1
INTB	PMC0, Ethernet)
INTC	SCSI (Routed to IRQ11)
INTD	Universe Bridge (Routed to IRQ9) - One of (11) interrupts or events: (7) VME interrupts, VME ACFAIL, VME SYSFAIL, VME SYSRESET, PCI Bus Fail

Table B-1. Interrupts.

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B B

Note: Interrupts 3,4,5,6,7,9,11,14, and 15 are available on the EXMbus. The INTB interrupt is shared by the on-board Ethernet controller and PMC-1. This means that if the PMC-1 card needs DMA, or the use of INTB, then the on-board Ethernet must be disabled.

DMA Channels

The assignment of DMA channels for the EPC-9 is shown in the following table.

Channel	Assignment	Available on EXM Bus
0	unassigned (8-bit)	No
1	unassigned (8-bit)	Yes
2	usually needed for floppy disk (8-bit)	Yes
3	usually needed for SCSI disk (8-bit)	Yes
4	(Channel 0 - Channel 3 cascade through Channel 4)	No
5	unassigned (16-bit)	Yes
6	unassigned (16-bit)	Yes
7	unassigned (16-bit)	No

Table B-2. DMA Channels.

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Appendix C - Connectors and Jumpers

C C

This Appendix specifies the details of the connectors and jumpers used on the EPC-9. The locations of the connectors on the EPC-9 I/O board are shown in Figure C-1. The location of connectors on the front panel are shown in Figure C-2. The optional PMC-1 Video Module is shown. Your system may or may not include the PMC-1 module, depending on ordered options. The JP1 header (primary EIDE) is located under the optional PMC-1 Video Module.

Pins are labeled from the point of view of looking at the front of the connector.

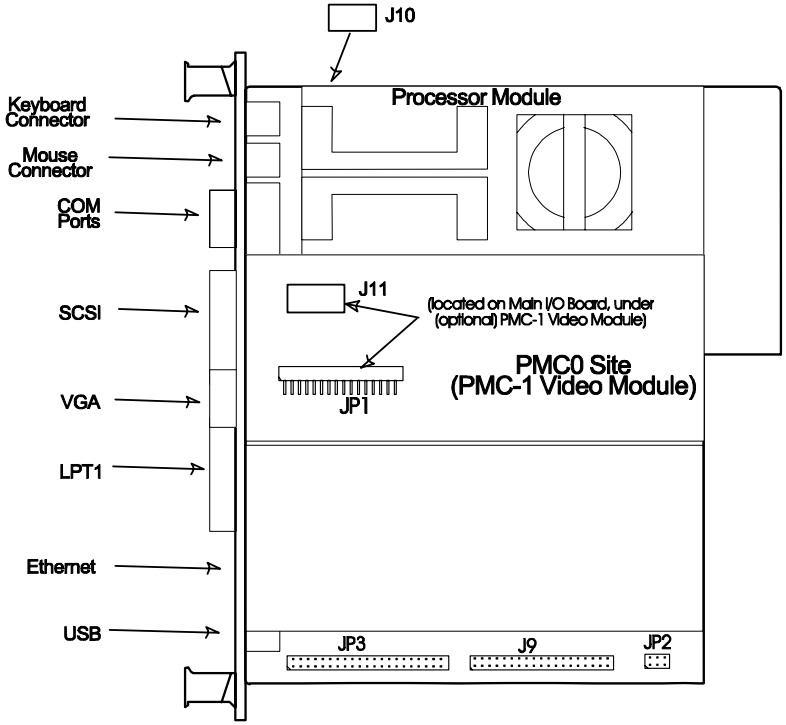


Figure C-1. EPC-9 Assembly.

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C C

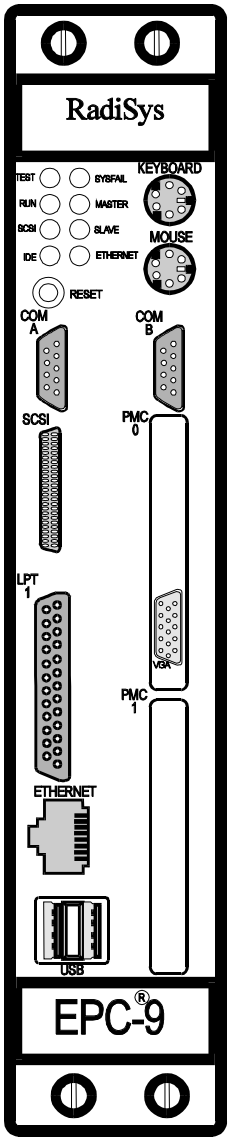


Figure C-2. EPC-9 Front Panel.

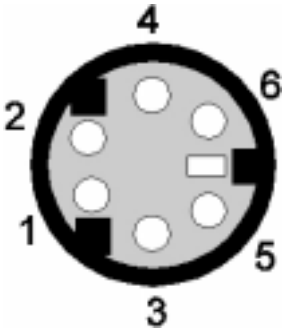
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Keyboard Connector

The PS/2 keyboard connector is a 6-pin mini-DIN connector defined as follows:

Pin	Signal	Pin	Signal
1	Data	4	+5V
2	not used	5	Clock
3	Ground	6	not used

Table C-1. Keyboard Pin-Out.



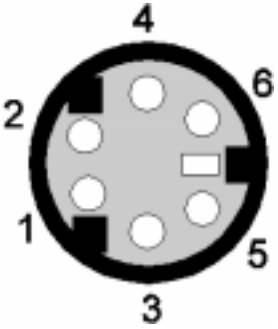


Mouse Connector

The PS/2 mouse connector is a 6-pin mini-DIN connector defined as follows:

Pin	Signal	Pin	Signal
1	Data	4	+5V
2	not used	5	Clock
3	Ground	6	not used

Table C-2. Mouse Pin-Out.

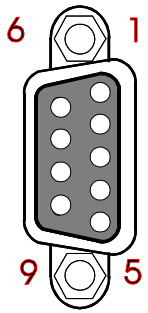


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C C

RS-232 Ports (COM A, COM B)

The RS-232 serial port male DB-9 DTE connectors are defined as follows:

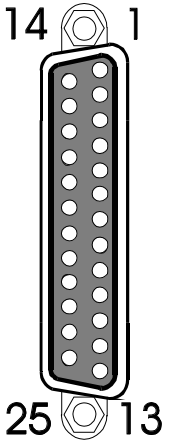


Pin	Signal	Pin	Signal
1	Carrier detect	6	Data set ready
2	Receive data	7	Request to send
3	Transmit data	8	Clear to send
4	Data terminal ready	9	Ring indicator
5	Signal Ground		

Table C-3. DB-9 Pin-Out.

Parallel Port

The LPT1 parallel port female DB-25 connector is defined as follows:



Pin	Signal	Pin	Signal
1	Strobe	14	Auto line feed
2	DB0	15	Error
3	DB1	16	Initialize printer
4	DB2	17	Select in
5	DB3	18	Signal ground
6	DB4	19	Signal ground
7	DB5	20	Signal ground
8	DB6	21	Signal ground
9	DB7	22	Signal Ground
10	Acknowledge	23	Signal ground
11	Busy	24	Signal ground
12	Paper End	25	Signal ground
13	Select		

Table C-4. DB-25 Pin-Out.

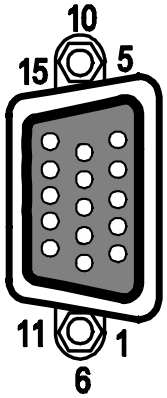
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SVGA Connector (on the Front Panel of the optional PMC-1 Video Module)

The SVGA monitor port is a DB-15 connector defined as follows:

Pin	Signal	Pin	Signal
1	Red	9	(key)
2	Green	10	Ground
3	Blue	11	(not used)
4	(not used)	12	(not used)
5	Ground	13	Horizontal sync
6	Ground	14	Vertical sync
7	Ground	15	programmable output
8	Ground		

Table C-5. DB-15 Pin-Out.



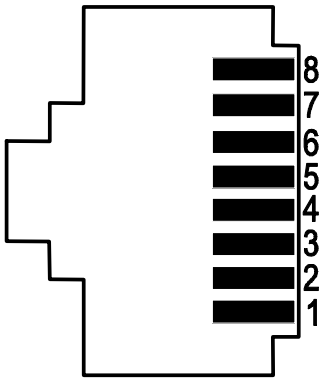


RJ45 Connector

The DTE RJ45 phone jack that supplies the 10Base-T/100Base-TX interface to the Ethernet controller is defined as follows:

Pin	Signal
1	Tx+
2	Tx-
3	Rx-
4	No connect
5	No connect
6	Rx+
7	No connect
8	No connect

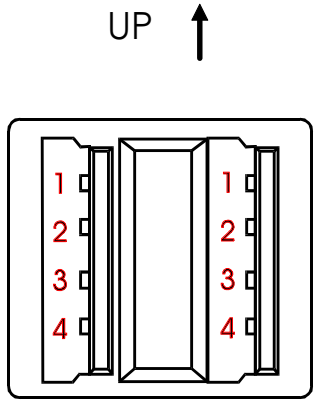
Table C-6. RJ45 Phone Jack Pin-Out.



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Dual USB Connector

The USB (Universal Serial Bus) connector is a dual, stacked 4-pin connector defined as follows:



Pin	Description
Mechanical Solder Lug	Shield Ground
1	VCC (1Amp Fused)
2	DATA-
3	DATA+
4	Signal Ground
Mechanical Solder Lug	Shield Ground

Table C-7. Dual USB Connector

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SCSI-2 Connector

The SCSI-2 port is a female 50-conductor .050 center mini-D style connector defined in the following table. To disable the SCSI terminator, see *SCSI Terminator Disable Jumper*, later in this appendix.

Pin	Signal	Pin	Signal
1	Signal GND	26	Terminator Power
2	~DB0	27	Signal GND
3	Signal GND	28	Signal GND
4	~DB1	29	Signal GND
5	Signal GND	30	Signal GND
6	~DB2	31	Signal GND
7	Signal GND	32	~ATN
8	~DB3	33	Signal GND
9	Signal GND	34	Signal GND
10	~DB4	35	Signal GND
11	Signal GND	36	~BSY
12	~DB5	37	Signal GND
13	Signal GND	38	~ACK
14	~DB6	39	Signal GND
15	Signal GND	40	~RST
16	~DB7	41	Signal GND
17	Signal GND	42	~MSG
18	~DBP	43	Signal GND
19	Signal GND	44	~SEL
20	Signal GND	45	Signal GND
21	Signal GND	46	~C/D
22	Signal GND	47	Signal GND
23	Signal GND	48	~REQ
24	Signal GND	49	Signal GND
25	N/C	50	~I/O

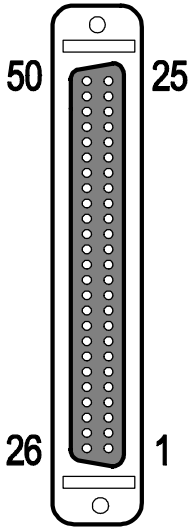


Table C-8. SCSI-2 Connector

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C C

EIDE (Primary) Connector

The Primary EIDE Connector is a male 44-pin right-angle header designated JP1, located on the Main I/O board, under the optional PMC-1 SVGA Board. The pins and signals are defined in the following table:

Pin	Signal	Pin	Signal
1	~RST	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	N.C.
21	DRQ	22	GND
23	~IOW	24	GND
25	~IOR	26	GND
27	IORDY	28	PPU
29	~DAK	30	GND
31	IRQ	32	IOCS16
33	A1	34	N.C.
35	A0	36	A2
37	~CS0	38	~CS1
39	ACT	40	GND
41	Vcc	42	Vcc
43	GND	44	GND

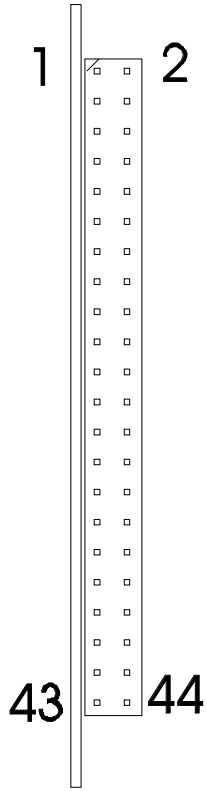


Table C-9. Primary EIDE Connector

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EIDE (Secondary) Connector JP3

The Secondary EIDE Connector is a male 40-pin header designated JP3, located at the front of the bottom edge of the Main I/O board. The pins and signals are defined in the following table:

Pin	Signal	Pin	Signal
1	~RST	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	N.C.
21	DRQ	22	GND
23	~IOW	24	GND
25	~IOR	26	GND
27	IORDY	28	SPU
29	DAK	30	GND
31	IRQ	32	IOCS16
33	A1	34	N.C.
35	A0	36	A2
37	CS0	38	CS1
39	ACT	40	GND

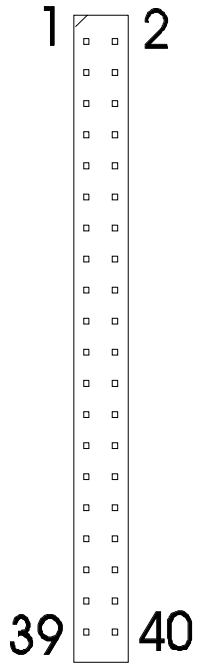


Table C-10. Secondary EIDE Connector.

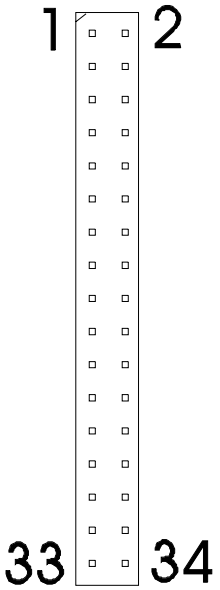
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C C

Floppy Disk Drive Connector

The Floppy disk drive connector is a male 34-pin header designated J9, located at the rear of the bottom edge of the Main I/O board. The pins and signals are defined in the following table:

Pin	Signal	Pin	Signal
1	GND	2	DENSEL
3	N.C.	4	N.C.
5	N.C.	6	RATE0
7	Vcc*	8	INDEX
9	Vcc*	10	MTR1
11	Vcc*	12	DS0
13	GND	14	DS1
15	GND	16	MTR0
17	GND	18	DIR
19	GND	20	STEP
21	GND	22	WDATA
23	GND	24	WGATE
25	GND	26	TRK0
27	GND	28	WRPRT
29	GND	30	RDATA
31	GND	32	HDSEL
33	GND	34	DSKCHG



* - Vcc if jumper JP2 is installed (RadiSys floppy drive)
N.C. if jumper JP2 is not installed.

Table C-11. Floppy Disk Drive Connector.

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Fan Failure Detect Enable Jumper (J10)

The Fan Failure Detect Enable Jumper (J10) is located at the front of the top of the Main I/O board, behind the front panel LEDs as shown in Figure C-1. The jumper is installed for the EPC-9, but is removed when the EPC-9 is upgraded to an EPC-10, which uses the Pentium Pro Processor Module.

SCSI Terminator Disable Jumper (J11)

The SCSI Terminator Disable Jumper (J11) is located behind the battery on the Main I/O board, under the optional PMC1 SVGA Module, as shown in Figure C-1. To disable the SCSI terminator, apply a jumper to J11. The last module in a SCSI chain must have an active terminator, while all other modules must have the terminator disabled. The EPC-9 is shipped with the jumper removed, enabling the SCSI terminator.

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Notes

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Appendix D - Subplanes

Subplane Installation

A subplane is a printed-circuit board with connectors on both sides. Subplanes extend the PC/AT bus and provide power from the VMEbus backplane to the EPC-9, any EXM expansion modules, and an optional EXP-MX Mass Storage Module. Depending on the particular EPC-9 subsystem configuration, a specific subplane will need to be installed.

For systems that have no EXP-MX Mass Storage Module, the subplanes are designated BP9E0, BP9E2, and BP9E4 and provide zero, two, and four EXM connectors, respectively.

For systems that have the EXP-MX Mass Storage Module, the subplanes are designated BP9E0M, BP9E2M, and BP9E4M and provide zero, two, and four EXM connectors, respectively, plus the connector for the EXP-MX Mass Storage Module.

Each subplane is described in the subsections that follow. Locate the appropriate subsection for the subplane you are using either by name or by picture. Follow the installation instructions in the appropriate subsection.

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D D

BP9E0 Subplane

This subplane is used in the smallest configuration, where the EPC-9 processor is used by itself, occupying two VME slots. Note that no EXM modules or EXP-MX Mass Storage Modules can be used with this configuration.

The BP9E0 is an L-shaped board with one connector on the front and three on the back.

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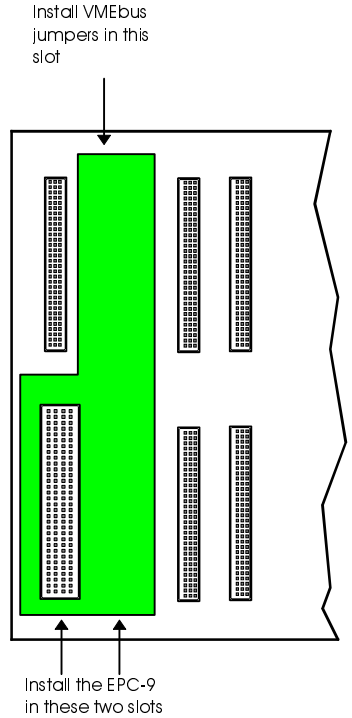


Figure D-1. BP9E0 Subplane.

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BP9E0M Subplane

The BP9E0M subplane is used in a configuration with an EPC-9 processor, no EXM modules, and an EXP-MX Mass Storage module.

The EXP-BP4 is a T-shaped board with two connectors on the front side and four on the rear.

After jumpering the backplane, plug the subplane into the VMEbus backplane such that the P2 connector on the back of the 4-row DIN is pressed into the J2 connector of the left-most VMEbus slot that the EPC-9 subsystem will occupy.

The EXM slot numbers are shown in the drawing.

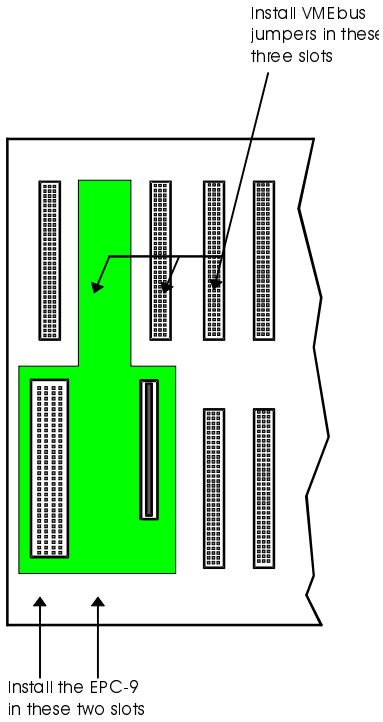




Figure D-2. BP9E0M Subplane.

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D D

BP9E2 Subplane

The BP9E2M subplane is used in a configuration with an EPC-9 processor module and one or two EXM modules.

The BP9E2 has five connectors on the back and three connectors on the front.

After jumpering the backplane, plug the subplane into the VMEbus backplane such that the P2 connector on the back of the 4-row DIN is pressed into the J2 connector of the left-most VMEbus slot that the EPC-9 subsystem will occupy.

The EXM slot numbers are shown in the drawing.

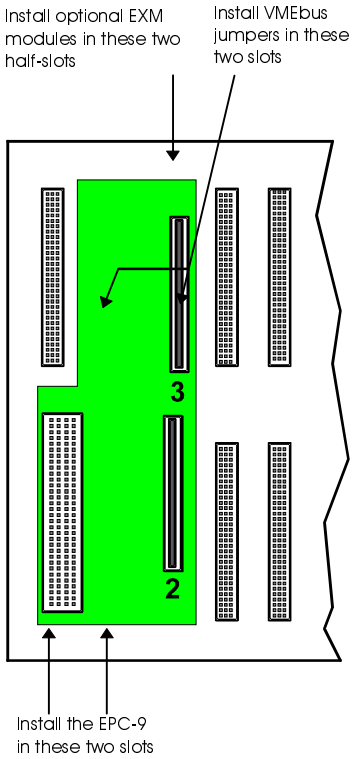


Figure D-3. BP9E2 Subplane.

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BP9E2M Subplane

The BP9E2M subplane is used in a configuration with an EPC-9 processor module, one or two EXM modules, and an EXP-MX Mass Storage module. The BP9E2M has four connectors on the front side and six on the rear.

After jumpering the backplane, plug the subplane into the VMEbus backplane such that the P2 connector on the back of the 4-row DIN is pressed into the J2 connector of the left-most VMEbus slot that the EPC-9 subsystem will occupy.

The EXM slot numbers are shown in the drawing.

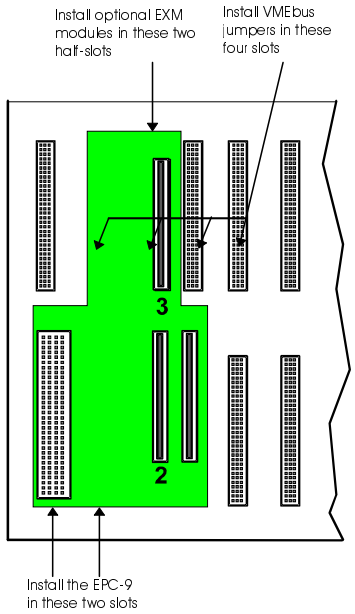




Figure D-4. BP9E2M Subplane.

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D D

BP9E4 Subplane

The BP9E4 subplane is used in a configuration with an EPC-9 processor module and up to four EXM modules.

The BP9E4 has five connectors on the front side and seven on the rear.

After jumpering the backplane, plug the subplane into the VMEbus backplane such that the P2 connector on the back of the 4-row DIN is pressed into the J2 connector of the left-most VMEbus slot that the EPC-9 subsystem will occupy.

The EXM slot numbers are shown in the drawing.

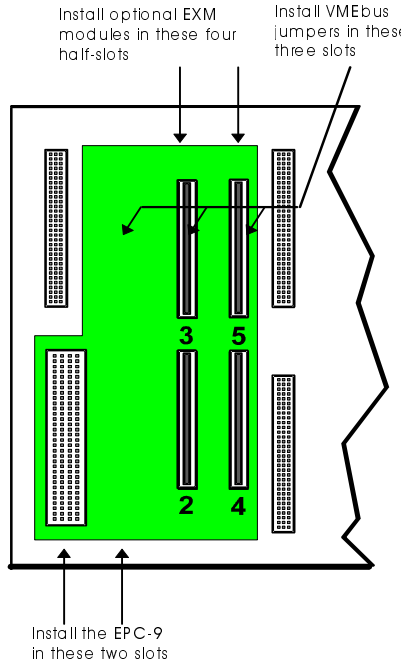


Figure D-5. BP9E4 Subplane.

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BP9E4M Subplane

The BP9E4M subplane is used in a configuration with an EPC-9 processor module, four EXM modules, and an EXP-MX Mass Storage module.

The BP9E4M has six connectors on the front side and seven on the rear.

After jumpering the backplane, plug the subplane into the VMEbus backplane such that the P2 connector on the back of the 4-row DIN is pressed into the J2 connector of the left-most VMEbus slot that the EPC-9 subsystem will occupy.

The EXM slot numbers are shown in the drawing.

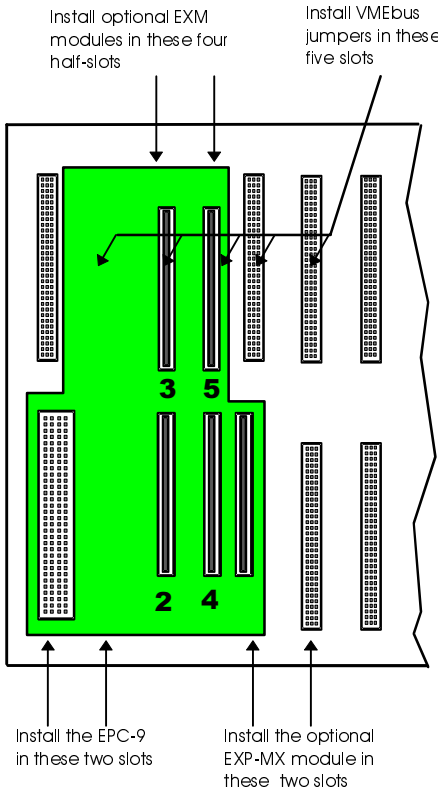


Figure D-6. BP9E4M Subplane.



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Notes

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Appendix E - Registers

Registers Specific to the EPC-9

Registers in the I/O space that are specific to the EPC-9 are defined below. Only registers 814Ch-814Fh are "dual-ported" to both the PC and VMEbus. The addresses shown below are used by the PC port. The VME addresses for the registers 814Ch-814Fh are described later.

Message High Register	MH[7..0]								814Ch
Message High Register	MH[15..8]								814Dh
Message Low Register	ML[7..0]								814Eh
Message Low Register	ML[15..8]								814Fh
Control Register		SLOT1		RONR	WDTR	WDTV			8150h
ULA	ULA[7..0]								8151h
VME Event Register	11111				MSGE	SIGE	WDTE		8152h
VME Event Enable Register	LRRY	LWRY	11	IACK	MSGIE	SIGIE	WDTIE		8153h
Status/Control Register	SRIE	1	SYSC	1	RDY	PASS	NOSF	RSTP	8154h
Status/Control Register	0	MODI	SYSR		1	1	1	1	8155h
Model Register	MODEL								8156h
Signal FIFO Low	SRFL								8158h
Signal FIFO High	SRFH								8159h
Response Register	LOCK	RRIE	ABMH	SIG	MLK	WRC	FSIG	LSIG	815Ah
Response Register	0	1	DOR	DIR	ERR	RRY	WRY	1	815Bh
IRQ Register	0	0	0	0	0	IRQ_2	IRQ_1	IRQ_0	8161h

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E E

IACK Latch 1 Low	IACK1[7..0]								8162h
IACK Latch 1 High	IACK1[15..8]								8163h
IACK Latch 2 Low	IACK2[7..0]								8164h
IACK Latch 2 High	IACK2[15..8]								8165h
IACK Latch 3 Low	IACK3[7..0]								8166h
IACK Latch 3 High	IACK3[15..8]								8167h
IACK Latch 4 Low	IACK4[7..0]								8168h
IACK Latch 4 High	IACK4[15..8]								8169h
IACK Latch 5 Low	IACK5[7..0]								816Ah
IACK Latch 5 High	IACK5[15..8]								816Bh
IACK Latch 6 Low	IACK6[7..0]								816Ch
IACK Latch 6 High	IACK6[15..8]								816Dh
IACK Latch 7 Low	IACK7[7..0]								816Eh
IACK Latch 7 High	IACK7[15..8]								816Fh
MODID Lower Register	MODID[4..0]					Reserved			8178h
MODID Upper Register	MODID[12..5]								8179h

VXI Register Offsets - see *VXI Register Base Address Decoding*, below, for base address determination

ID/ULA Register	ECh								0h
ID/ULA Register	8Fh								1h
Device Type Register	MM								2h
Device Type Register	0001 000S								3h
Status/Control Register	SRIE	1	SYSC	1	RDY	PASS	NOSF	RSTP	4h
Status/Control Register	0	MODI	SYSR	1	1	1	1	1	5h
Protocol Low Register	FFh								8h
Protocol High Register	1Fh								9h
Response Register	LOCK	RRIE	ABMH	SIG	MLK	WRC	FSIG	LSIG	Ah
Response Register	0	1	DOR	DIR	ERR	RRY	WRY	1	Bh
Message High Register	MH[7..0]								Ch
Message High Register	MH[15..8]								Dh
Message Low Register	ML[7..0]								Eh
Message Low Register	ML[15..8]								Fh

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Register Details

Message Registers (814Ch)

Message High Register	MH[7..0]	814Ch
Message High Register	MH[15..8]	814Dh
Message Low Register	ML[7..0]	814Eh
Message Low Register	ML[15..8]	814Fh

This is the PC-port side of the VXI message registers.

Each of the 16-bit Message registers is actually two registers, an inbound register and an outbound register. There are actually four 16-bit locations: message high in, message high out, message low in and message low out. Writing from the PC port writes to the outbound register. Reading from the PC port reads the inbound register. Writing from VME writes to the inbound register. Reading from VME reads the outbound register.

ABMH in the Response register, described below, is cleared when the low byte of Message High register is read or written from VME. It serves as a location monitor for determining whether a message is 16 or 32 bits in length. Access from the PC port has no effect on ABMH.

When the low byte of Message Low is read from VME, RRY in the Response register is cleared. When the low byte of Message Low is written from VME, WRY in the Response register is cleared. Access from PC port has no effect on RRY and WRY.

The low byte of Message-Low-out register is driven onto the VMEbus D[15:8] during an IACK response cycle. VME D[7:0] is driven from the ULA register.

Control Register (8150h)

	SLOT1	RONR	WDTR	WDTV	8150h

Only WDTR is cleared by a warm reset. All bits are cleared by a reset.

SLOT1 — Read only bit that indicates that state of the slot1 detect.

RONR — Bus release mode. If set, the bus release mode is RONR (request on no request); otherwise it is controlled by the bus request bits in the Tundra Universe chip.

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WDTR — Watchdog timer reset enable. If 1, expiration of the watchdog timer causes a reset. If 0, only the WDT event is signaled. A read of the this register should be performed before enabling the watchdog timer reset. This clears the watchdog counter to zero so that a PC reset does not occur immediately after enabling the watchdog timer.

WDTV — Watchdog timer value. This field produces the following time-out values: 00 - disables events from the watchdog timer, 01 - 8.2 s, 10 - 128ms, 11 - 1.02 s.

A read of the this register also has a side effect of resetting the watchdog timer. Therefore, if using the watchdog timer, it is required to read this register within the defined period of the timer to prevent generating an interrupt.

ULA (8151h

ULA[7..0]	8151h

This register is set to all 1's by a PCI reset.

The ULA register is an 8-bit value that represents the Unique Logical Address of the VXI registers. This register is driven onto the VME bus D[7:0] during an IACK response cycle. VME D[15:8] is driven from the lower 8 bits of the Message Low register. ULA is only readable from this port. It is written when accessed from the VME port at offset 0.

VME Event Register (8152h)

11111	MSGE	SIGE	WDTE	8152h

This register defines conditions that may result in an interrupt. If the bit is 0, the condition is present.

WDTE Watchdog timer expired

SIGE Signal FIFO is not empty.

MSGE If clear, a message interrupt is being signaled. MSGE is cleared if both of bits RRDY and WRDY in the response register are clear.

All bits are read-only.

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VME Event Enable Register (8153h)

LRRY	LWRY	11	IACK	MSGIE	SIGIE	WDTIE	8153h

The LRRY and LWRY are used as latching bits which hold the event of a RRY or WRY transition from a high to a low state. Thus if RRY transitions from a high to a low state (indicates a read of the VME message register occured), then LRRY will be set to a one. The same is true for the LWRY in the instance of a write to the message register. These bits can individually be reset to a zero state by writing a one to the respective bit field. Thus to clear LRRY, write a one in the MSB by ORing the current state of the register with the value of 80h. In the case of the LWRY a 40h would be ORed with the current value of the register.

If the MSGE bit is asserted and LRRY or LWRY is set, then an interrupt from the FPGA will be signaled to the processor. (i.e., AT interrupt 10 will be asserted to the processor)

The IACK bit indicates when an interrupt acknowedge is occuring. It indicates the actual value of the IACK signal line on the VME bus.

These bits are a mask of the interrupt conditions in the event state register. A one denotes that the corresponding event is enabled as an interrupt. If any bit in this register is a one, and the corresponding bit in the event state register is a zero, the INT pin is asserted. Software may then examine the interrupt and event state registers to determine the cause. Reset clears this register.



Status/Control Register (8154h)

SRIE	1	SYSC	1	RDY	PASS	NOSF	RSTP	8154h

Status/Control Register (8155h)

0	MODI	SYSR	1	1	1	1	1	8155h

These registers adhere to the VXIbus specification and also contains EPC-9 specific bits. Bits RSTP and NOSF are writeable only from the VME port. Bits SRIE, RDY, PASS, SYSR are writeable only from the PC Port. All bits are readable from both ports. See the VXI register description for details of each bit definition.

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Model Register (8156h)

MODEL	8156h

This register is a write once register after reset. The intent is for the BIOS to load this with the model number based on the EPC model. Once written, it is read only as the low 8 bits of the device type register in the VXI register space. Hardware reset enables writing the register again.

Signal FIFO Low (8158h)

SRFL	8158h

Signal FIFO High (8159h)

SRFH	8159h

To spell out the operation of the signal register FIFO, and associated control bits, the operations are explained in algorithmic fashion. SIG, FSIG and LSIG are fields in the Response register.

The signal FIFO (SRFIFO) is a two-element array with indexes. A write to the Protocol register from the VXI bus (see *VXI Register Details*, below) is a write to the signal FIFO, and does the following:

```
if (SIG && (FSIG != LSIG)) {        /* FIFO full */
            Assert BERR
      }

      else {
            if (SIG) LSIG = !LSIG;
            SRFIFO[LSIG] = write data;
            SIG = 1
      }
```

A read from SRFL returns the low-order byte of SRFIFO(FSIG). In all cases of accesses to SRFL and SRFH, if SIG = 0 (empty FIFO), the result is an access to SRFIFO(0). A read from SRFH returns the high-order byte of SRFIFO(FSIG), and does the following:

```
      if (FSIG == LSIG) { SIG = LSIG = FSIG = 0 }
      else FSIG = !FSIG;
```


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Response Register (815Ah)

LOCK	RRIE	ABMH	SIG	MLK	WRC	FSIG	LSIG	815Ah

Response Register (815Bh)

0	1	DOR	DIR	ERR	RRY	WRY	1	815Bh

The Response Register is described below, in the Response Register description in *VXI Register Details*.

IRQ Register (8161h)

0	0	0	0	0	IRQ_2	IRQ_1	IRQ_0	8161h

This register specifies which VME interrupt is to be asserted. 000 indicates none. 001 means assert IRQ1, 010 means assert IRQ2, … 111 means assert IRQ7. The register is cleared at reset or whenever an IACK to the interrupt asserted by this module occurs. Clearing the register de-asserts any interrupt that was asserted.

IACK Latches (8162h- 816Fh)

IACK Latch 1 Low	IACK1[7..0]	8162h
IACK Latch 1 High	IACK1[15..8]	8163h
IACK Latch 2 Low	IACK2[7..0]	8164h
IACK Latch 2 High	IACK2[15..8]	8165h
IACK Latch 3 Low	IACK3[7..0]	8166h
IACK Latch 3 High	IACK3[15..8]	8167h
IACK Latch 4 Low	IACK4[7..0]	8168h
IACK Latch 4 High	IACK4[15..8]	8169h
IACK Latch 5 Low	IACK5[7..0]	816Ah
IACK Latch 5 High	IACK5[15..8]	816Bh
IACK Latch 6 Low	IACK6[7..0]	816Ch
IACK Latch 6 High	IACK6[15..8]	816Dh
IACK Latch 7 Low	IACK7[7..0]	816Eh
IACK Latch 7 High	IACK7[15..8]	816Fh

All bits are cleared by a PCI reset.

IACK Latch is a 16-bit value latched from the VME-bus during an IACK cycle generated by this VME module. This value allows one to claim the full 16-bit data



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value of an IACK cycle. This is useful because, for some reason, the Universe chip strips off the upper 8 bits and flips bit 0. Each IACK Latch register corresponds to a different VME interrupt.

VXI Register Details

The addresses shown are offsets relative to a base address. See *VXI Register Base Address Decoding*, below, for the method for determining the base address.

If a bit is shown as 0 or 1, the bit is a ROM bit, and writing to it has no effect. Except as otherwise noted below, all registers and bit values can be read and written.

ID/ULA Register (offset 0h)

ECh	0h

ID/ULA Register (offset 1h)

8Fh	1h

This register adheres to the VXIbus specification. It defines EPC-9 as a message-based device and the manufacturer as RadiSys. When read, the ID is returned. When written, the lower 8 bits define the unique logical address (ULA). The upper 8 bits are ignored. The ULA is not valid as an addressing mechanism until the register is written the first time. Until then, one must use the MODID address mechanism (i.e., ULA of FFh with MODID asserted) to address the VXI registers.

Device Type Register (offset 2h)

MM	2h

Device Type Register (offset 3h)

0001 000S	3h

These registers adhere to the VXIbus specification. The value defines EPC-9 as having a model code of 10MMh if it is a slot 0 controller and 11MMh if it is not a slot 0 controller. MM is the value in the Model register.

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Status/Control Register (offset 4h)

SRIE	1	SYSC	1	RDY	PASS	NOSF	RSTP	4h

Status/Control Register (offset 5h)

0	MODI	SYSR	1	1	1	1	1	5h

These registers adhere to the VXIbus specification and also contains EPC-9 specific bits. Bits RSTP and NOSF are writeable only from the VME port. Bits SRIE, RDY, PASS, SYSR are writeable only from the PC Port. All bits are readable from both ports.

SRIE SYSRESET input enable. If set, assertion of VME SYSRESET generates a reset of the EPC-9. One use of this bit is having EPC-9 software reset other VME devices (via bit SYSR) without resetting EPC-9.

SYSC SYSCLK status bit. All writes to this register have the effect of clearing this bit. The bit is then set if four rising edges of the VXI SYSCLK signal are detected. This bit is intended to be used to detect that SYSCLK is being generated on the backplane.

RDY This is a RAM bit defined by the VXI specification. In a VXIbus software environment, if RDY=1 and PASS=1, EPC-9 is ready to accept VXI-defined messages.

PASS If set (1), EPC-9 has completed its self-test successfully. If this bit is cleared (0), the Test LED on EPC-9 front panel is lit, indicating that self-test failed.

NOSF SYSFAIL inhibit. If set (1), EPC-9 will not assert the VME-bus SYSFAIL line due to the PASS bit being cleared. If the PASS bit is cleared and this bit is cleared (0), then SYSFAIL will be asserted. SYSFAIL is also asserted when a Watchdog time-out reset occurs, independent of the setting of this bit. Assertion of SYSFAIL can also be accomplished by application software writing to bit 30 of the Universe VCSR_SET and VCSR_CLR registers.

RSTP Reset processor. Setting this bit to a 1 resets the EPC-9.

MODI If clear (0), it denotes that the MODID pin is being asserted.

SYSR SYSRESET. EPC-9 asserts the VME SYSRESET line while this bit is 1. When using this bit, it is the software's responsibility to ensure that the VME-specified minimum assertion time of SYSRESET is met. This function can also be performed by bit 22 of Universe register MISC_CTL.

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Protocol Low Register (offset 8h)

FFh	8h

Protocol High Register (offset 9h)

1Fh	9h

A read of these registers reads the ROM constants stored in the protocol register. A write to this register location writes the signal register.

The protocol register (the read value) defines EPC-9 as being a servant and commander, having a signal register, being a bus master and an interrupter, not providing the shared-memory protocol, and not providing fast handshake mode.

Response Register (offset Ah)

LOCK	RRIE	ABMH	SIG	MLK	WRC	FSIG	LSIG	Ah

Response Register (offset Bh)

0	1	DOR	DIR	ERR	RRY	WRY	1	Bh

These registers contain some VXI-defined state bits associated with message handling, and several EPC-9 dependent bits. These registers are read-only from VME and are read/write from the PC port. Note that some of these bits (ABMH, MLK, RRY and WRY) can be cleared by hardware when access is made to the message registers from the VME port. Software protocols as defined by the VXI specification guarantee that this does not happen at the same time as a write from the PC port to these bits. If software violates this protocol, unpredictable results will occur.

LOCK RAM bit available to software for VXI communication protocols.

RRIE This bit is used to enable RRY interrupt signaling. When clear (reset state), only the deassertion of WRY will cause the MSGR interrupt to be asserted. When set, the "OR" of the deasserted RRY, WRY bits is used to assert the interrupt.

ABMH This bit is cleared when the message high register is read or written from the VXIbus. It serves as a location monitor for determining whether a message is 16 or 32 bits in length.

SIG If this bit is 0, the signal FIFO is empty.

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MLK This bit is used for synchronization of messages from multiple senders, something not provided for in the VXI specification. If 1, the message register can be locked for the sending of a message. If 0, the message register has been locked. See the discussion of message sending protocol, below.

WRC This bit is a read-only copy of the WRY bit.

FSIG Defined only when SIG=1, in which case FSIG is the number (0 or 1) of the register in the FIFO holding the earliest signal.

LSIG Defined only when SIG=1, in which case LSIG is the number (0 or 1) of the register in the FIFO holding the most recent signal.

DOR RAM bit available to software for VXI communication protocols.

DIR RAM bit available to software for VXI communication protocols.

ERR RAM bit available to software for VXI communication protocols.

RRY Read ready. A 1 denotes that the message registers contain outgoing data to be read by another device. RRY is cleared when the message-low register is read from VME. RRY can only be set by writing to this register from the PC port.

WRY Write ready. If set, the message registers are armed for an incoming message. When a write occurs into the message-low register, WRY is cleared and the MSGR interrupt condition is asserted. Wry can only be set by writing to this register from the PC port.



FSIG and LSIG are not used for programming. They are read-only bits used for tests during manufacturing.

The protocol for sending a message, when there are multiple potential senders, is as follows:

Read the Alternate Response register (offset 2A).

If both WRY and MLK are 1, then proceed to send the message.

If not, repeat reads until both WRY and MLK are 1.

For 16-bit messages, write into the Message Low register.

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For 32-bit messages, write first into Message High register and then into the Message Low register.

The bits RRY, WRY, ABMH, and MLK in the Response register are altered by hardware-detected conditions. A read from the Message Low clears RRY. A write into all or the lower 8 bits of the Message Low register clears WRY. A read from the VME bus port of the Alternate Response register clears MLK if WRY is set. A read or write to all or the lower 8 bits of the Message High register clears ABMH. A read from the Alternate Response register also returns the value in the Response register. Note that the Alternate Response register is accessed at offset 0x2A from the VME A16 base address of these registers.



LOCK, RRIE, MLK, ABMH, DIR, DOR, ERR can be set or cleared by using a write to the response register. RRY and WRY may only set via a write to the Response register. For these two bits, a 0 written into the respective bit position will not change the value of the register bit. A 1 written into the respective bit position will set the value of the register bit to 1.

Supporting software on the controller must be aware of how to set the bits initially. The valid states are:

RRY	WRY	MLK	State
X	1	1	Write ready (awaiting incoming msg)
X	1	0	Write ready, locked by a sender
1	X	X	Read ready (outgoing data present)
0	0	X	Not ready for write or read

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Message High Register (offset Ch)

MH[7..0]	Ch

Message High Register (offset Dh)

MH[15..8]	Dh

Message Low Register (offset Eh

ML[7..0]	Eh

Message Low Register (offset Fh)

ML[15..8]	Fh

See the description above for the operation of these registers.



VXI Register Base Address Decoding

To determine the VXI Register Base Address:

1. Read ULA as the lower 8 bits at 8151h. (xxxx xxxx aaaa aaaa).

2. Form the base address as 11aa aaaa aa00 0000, where aaaa aaaa are the lower 8 bits at 8151h.

3. The result is the binary representation of the VXI Register Base Address.

4. Thus the lowest possible base address is C000h (1100 0000 0000 0000) and the highest possible base address is FFC0h (1111 1111 1100 0000). Note that the range consists of base addresses separated by 40h.

5. Another view:

   Base_addr = (ULA * 40h) + C000h

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Notes

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Appendix F - Glossary

— A —

Access Time: A factor in measurement of a memory storage device's operating speed. It is the amount of time required to perform a read operation. More specifically, it is the period of time between which the memory receives a read command signal and the time when the requested data becomes available to the system data bus.

Address: A number that identifies the location of a word in memory. Each word in a memory storage device or system has a unique address. Addresses are always specified as a binary number, although octal, hexadecimal, and decimal numbers are often used for convenience.

Advanced Power Management (APM 1.1): A software interface specification that allows operating system device drivers to control the power management functionality of a PC.

American National Standards Institute (ANSI): An organization dedicated to advancement of national standards related to product manufacturing.

AT Bus Attachment (ATA): An interface definition for PC peripherals. See IDE.

Autotype: A convenient method of IDE device detection whereby the system BIOS queries the IDE device to obtain operational parameters. If the device supports autotype, this information is passed to the BIOS where it is used to automatically configure the drive controller.

— B —

Basic Input/Output System (BIOS): Firmware in a PC-compatible computer that runs when the computer is powered up. The BIOS initializes the computer



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hardware, allows the user to configure the hardware, boots the operating system, and provides standard mechanisms that the operating system can use to access the PC's peripheral devices.

BIOS Data Area (BDA): BIOS Data Area. A 256 byte block of DRAM starting at address 400H that contains data initialized and used by the System BIOS detailing the system configuration and errors encountered during POST.

BIOS Extension: An object code module that is typically integrated into the FBD or placed into a ROM that is accessible on the peripheral bus (PCI, ISA, etc.) in the address range 0C0000H through 0DFFFFH. BIOS extensions have a pre-defined header format and contain code that is used to extend the capabilities of the System BIOS.

BIOS Image: Information contained in the flash boot device in binary file format consisting of initialzation data, setup configuration data, diagnostic sequences, and other instructions necessary to start up a computer and prepare it to load an operating system.

BIOS Recovery: A process whereby an existing, corrupt BIOS image in the flash boot device is overwritten with a new image. Also referred to as a *flash recovery*.

BIOS Update: A process whereby an existing, uncorrupted BIOS image in the flash boot device is overwritten with a new image. Also referred to as a *flash update*.

Bit: A binary digit.

Boot: The process of starting a computer and loading the operating system from a powered down state (cold boot) or after a computer reset (warm boot). Before the operating system loads, the computer performs a general hardware initialization and resets internal registers.

Boot Block: A write-protected 16KB section of the flash boot device located at physical address FFFFC000h to FFFFFFFFh which contains code to perform rudimentary hardware intitialization at system power up. The boot block also contains code to recover the BIOS via floppy disk.

Boot Device: The storage device from which the computer boots the operating system.

Boot Sequence: The order in which a computer searches external storage devices for an operating system to boot. The boot device must be the first in the boot sequence.

Byte: A group of 8 bits.

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— C —

Central Processing Unit (CPU): A semiconductor device which performs the processing of data in a computer. The CPU, also referred to as the microprocessor, consists of an arithmetic/logic unit to perform the data processing, and a control unit which provides timing and control signals necessary to execute instructions in a program.

Chipset: One or more integrated circuits that, along with a CPU, memory, and other peripherals, implements an IBM PC-AT compatible computer. The chipset typically implements a DRAM controller, bus, interface logic, and PC peripheral devices.

Column Address Strobe (CAS): An input signal from the DRAM controller to an internal DRAM latch register specifying the column at which to read or write data. The DRAM requires a column address and a row address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of column addresses and row addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required.

COM Port: A bi-directional serial communication port which implements the RS-232 specification.

Complimentary Metal Oxide Semiconductor (CMOS): A fast, low power semiconductor RAM used to store system configuration data.

Conventional Memory: The first 640 KB of a computer's total memory capacity. If a computer has no extended memory, conventional memory equals the total memory capacity. In typical computer systems, conventional memory can contain BIOS data, the operating system, applications, application data, and terminate and stay resident (TSR) programs. Also called *system memory*.

CMOS Save and Restore (CSR): A System BIOS feature that allows the user to backup the contents of CMOS RAM (contained within the real time clock) to the BIOS Flash device to be restored later if necessary (such as when the real time clock battery dies).

Cylinders/Heads/Sectors (CHS): A specification of disk drive operating parameters consisting of the number of disk cylinders, disk drive read/write heads, and disk sectors.



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F F

— D —

Default: The state of all user-changeable hardware and software settings as they are originally configured before any changes are made.

Disk Operating System (DOS): One or more programs which allow a computer to use a disk drive as an external storage device. These programs manage storage and retrieval of data to and from the disk and interpret commands from the computer operator.

Driver: A software component of the operating system which directs the computer interface with a hardware device. The software interface to the driver is standardized such that application software calling the driver requires no specific operational information about the hardware device.

Dual In-Line Package (DIP): A semiconductor package configuration consisting of a rectangular plastic case with two rows of pins, one row on each lengthwise side.

Dynamic Random Access Memory (DRAM): Semiconductor RAM memory devices in which the stored data will not remain permanently stored, even with the power applied, unless the data are periodically rewritten into memory during a *refresh* operation.

— E —

Electrically Erasable Programmable ROM (EEPROM): Specifically, those EPROMs which may be erased electrically as compared to other erasing methods.

Error Checking and Correction: A feature of the T2 chipset that enables it to detect single or multi-bit errors in DRAM reads and correct single bit errors. This feature requires that all banks of DRAM use x36 (parity) SO DIMMs.

Extended Capabilities Port (ECP): An enhancement of the standard PC parallel port that allows high speed bi-directional data transfers and other features.

Extended Data Out (EDO): A type of DRAM that allows higher memory system performance since the data pins are still driven when CAS# is de-asserted. This allows the next DRAM address to be presented to the device sooner than with Fast Page Mode DRAM.

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Extended Memory: The RAM address space, in a computer so equipped, above the 1 MB level.

Extended System Configuration Data (ESCD): A block of nonvolatile memory that stores information on the devices found and configured by the Plug and Play BIOS.

External Device: A peripheral or other device connected to the computer from an external location via an interface cable.

— F —

Fast Page Mode (FPM): A "standard" type of DRAM that is lower performance than EDO.

Fixed Disk: A hard disk drive or other data storage device having no removable storage medium. Fixed disk storage devices use inflexible disk media and are sealed to prevent data loss due to media surface contamination. Fixed disks generally provide the most storage space for a given cost when compared to semiconductor, tape, and other popular mass storage technologies.

Field Programmable Gate Array (FPGA): A large, general-purpose logic device that is programmed at power-up to perform specific logic functions.

Flash Boot Device (FBD): A flash memory device containing the computer's BIOS. In the EPC-9, a 512 KB Intel 28F004BV-T semiconductor flash memory containing the system and video BIOS images, the BIOS initializing code and the recovery code which allows self hosted reflashing.

Flash Memory: A fast EEPROM semiconductor memory typically used to store firmware such as the computer BIOS. Flash memory also finds general application where a semiconductor non-volatile storage device is required.

Flash Recovery: See *BIOS Recovery*.

Flash Update: See *BIOS Update*.

Force Update: See *BIOS Recovery*.

— G —

Gigabyte (GB or GByte): Approximately one billion (US) or one thousand million (Great Britain) bytes. 2^30 = 1,073,741,824 bytes exactly.



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— H —

Hang: A condition where the system microprocessor suspends processing operations due to an anomaly in the data or an illegal instruction.

Header: A mechanical pin and sleeve style connector on a circuit board. The header may exist in either a male or female configuration. For example, a male header has a number and pattern of pins which corresponds to the number and pattern of sleeves on a female header plug.

Hexadecimal (h): A base 16 numbering system using numeric symbols 0 through 9 plus alpha characters A, B, C, D, E, and F as the 16 digit symbols. Digits A through F are equivalent to the decimal values 10 through 15.

Host Bus: The address/data bus that connects the CPU and the chipset.

— I —

Industry Standard Architecture (ISA): A popular microcomputer expansion bus architecture standard. The ISA standard originated with the IBM PC when the system bus was expanded to accept peripheral cards.

Input/Output (I/O): The communication interface between system components and between the system and connected peripherals.

Integrated Drive Electronics (IDE): A hard disk drive/controller interface standard. IDE drives contain the controller circuitry at the drive itself, as compared to the location of this circuitry on the computer motherboard in non-IDE systems. IDE drives typically connect to the system bus with a simple adapter card containing a minimum of on-board logic.

Infra-red Data Association (IRDA or IrDA): A specification for high-speed data communication using infrared drivers and receivers for short-range wireless data transmission.

Interrupt Request (INT): A software-generated interrupt request.

Interrupt Request (IRQ): In ISAbus systems, a microprocessor input from the control bus used by I/O devices to interrupt execution of the current program and cause the microprocessor to jump to a special program called the *interrupt service routine*. The microprocessor executes this special program, which normally involves servicing the interrupting device. When the

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interrupt service routine is completed, the microprocessor resumes execution of the program it was working on before the interruption occurred.

Interrupt Service Routine (ISR): A program executed by the microprocessor upon receipt of an *interrupt request* from an I/O device and containing instructions for servicing of the device.

— J —

Jumper: A set of male connector pins on a circuit board over which can be placed coupling devices to electrically connect pairs of the pins. By electrically connecting different pins, a circuit board can be configured to function in predictable ways to suit different applications.

— K —

Kilobyte (KB or KByte): Approximately one thousand bytes. 2^10 = 1024 bytes exactly.

— L —

Logical Address: The memory-mapped location of a segment after application of the address offset to the physical address.

Logical Block Addressing (LBA): A method the system BIOS uses to reference hard disk data as logical blocks, with each block having a specific location on the disk. LBA differs from the CHS reference method in that the BIOS requires no information relating to disk cylinders, heads, or sectors. LBA can be used only on hard disk drives designed to support it.

— M - N —

Megabyte (MB or MByte): Approximately one million bytes. 2^20 = 1,048,576 bytes exactly.

Memory: A designated system area to which data can be stored and from which data can be retrieved. A typical computer system has more than one memory area. See *Conventional Memory* and *Extended Memory*.



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— O —

Offset: The difference in location of memory-mapped data between the physical address and the logical address.

Operating System: See *Disk Operating System*.

— P - Q —

PCI Mezzanine Card (PMC): A new standard form factor for PCI add-in modules. PMCs mate with their respective connectors on the motherboard and are secured with screws.

Peripheral Connect Interface (PCI): A popular microcomputer bus architecture standard.

Peripheral Device: An external device connected to the system for the purpose of transferring data into or out of the system.

Personal Computer/Advanced Technology (PC/AT): A popular computer design first introduced by IBM in the early 1980s.

Personal System 2 (PS/2): Computers designed with IBM's proprietary bus architecture known as Micro Channel.

Phase-Locked Loop (PLL): A semiconductor device which functions as an electronic feedback control system to maintain a closely regulated output frequency from an unregulated input frequency. The typical PLL consists of an internal phase comparator or detector, a low pass filter, and a voltage controlled oscillator which function together to capture and lock onto an input frequency. When locked onto the input frequency, the PLL can maintain a stable, regulated output frequency (within bounds) despite frequency variance at the input.

Physical Address: The address or location in memory where data is stored before it is moved as memory remapping occurs. The physical address is that which appears on the computer's address bus when the CPU requests data from a memory address. When remapping occurs, the data can be moved to a different memory location or *logical address*.

Pinout: A diagram or table describing the location and function of pins on an electrical connector.

Plastic Quad Flat Pack (PQFP): A popular package design for integrated circuits of high complexity.

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Power On Self Test (POST): A diagnostic routine which a computer runs at power up. Along with other testing functions, this comprehensive test initializes the system chipset and hardware, resets registers and flags, performs ROM checksums, and checks disk drive devices and the keyboard interface.

Program: A set of instructions a computer follows to perform specific functions relative to user need or system requirements. In a broad sense, a program is also referred to as a software application, which can actually contain many related, individual programs.

Programmable Array Logic (PAL): A semiconductor programmable ROM which accepts customized logic gate programming to produce a desired sum-of-products output function.

— R —

Random Access Memory (RAM): Memory in which the actual physical location of a memory word has no effect on how long it takes to read from or write to that location. In other words, the access time is the same for any address in memory. Most semiconductor memories are RAM.

Read Only Memory (ROM): A broad class on semiconductor memories designed for applications where the ratio of read operations to write operations is very high. Technically, a ROM can be written to (programmed) only once, and this operation is normally performed at the factory. Thereafter, information can be read from the memory indefinitely.

Real Mode: The operational mode of Intelx86 CPUs that uses a segmented, offset memory addressing method. These CPUs can address 1 MB of memory using real mode.

Real Mode Address: A memory address composed of two 16-bit values: a segment address and an offset quantity. A real mode address is constructed by shifting a segment address 4 bits to the left and then adding the offset value. A real mode address is a *physical address*.

Real Time Clock (RTC): Peripheral circuitry on a computer motherboard which provides a nonvolatile time-of-day clock, an alarm, calendar, programmable interrupt, square wave generator, and a small amount of SRAM. In the EPC-30, the RTC operates independently of the system PLL which generates the internal system clocks. The RTC is typically receives power from a small battery to retain the current time of day when the computer is powered down.



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Reflashing: The process of replacing a BIOS image, in binary format, in the flash boot device.

Register: An area typically inside the microprocessor where data, addresses, instruction codes, and information on the status on various microprocessor operations are stored. Different types of registers store different types of information.

Reset: A signal delivered to the microprocessor by the control bus, which causes a halt to internal processing and resets most CPU registers to 0. The CPU then jumps to a starting address vector to begin the boot process.

Resident Flash Array (RFA): The RFA represents flash memory that is resident on the hardware platform that is utilized for OS or application purposes.

RS-232: A popular asynchronous bi-directional serial communication protocol. Among other things, the RS-232 standard defines the interface cabling and electrical characteristics, and the pin arrangement for cable connectors.

Row Address Strobe (RAS): An input signal to an internal DRAM latch register specifying the row at which to read or write data. The DRAM requires a row address and a column address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of row addresses and column addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required.

F F

— S —

Segment: A section or portion of addressable memory serving to hold code, data, stack, or other information allowing more efficient memory usage in a computer system. A segment is the portion of a real mode address which specifies the fixed base address to which the offset is applied.

Serial Port: A physical connection with a computer for the purpose of serial data exchange with a peripheral device. The port requires an I/O address, a dedicated IRQ line, and a name to identify the physical connection and establish serial communication between the computer and a connected hardware device. A serial port is often referred to as a *COM port*.

Shadow Memory: RAM in the address range 0xC000h through 0xFFFFFh used for shadowing. Shadowing is the process of copying BIOS extensions from ROM into DRAM for the purpose of faster CPU access to the extensions

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when the system requires frequent BIOS calls. Typically, system and video BIOS extensions are shadowed in DRAM to increase system performance.

Single In-Line Memory Module (SIMM): A small, rectangular circuit board on which is mounted semiconductor memory ICs.

Small Outline Dual Inline Memory Module (SO DIMM): A new form factor for memory modules that is smaller and denser than SIMMs.

Standoff: A mechanical device, typically constructed of an electrically non-conductive material, used to fasten a circuit board to the bottom, top, or side of a protective enclosure.

Static Random Access Memory (SRAM): A semiconductor RAM device in which the data will remain permanently stored as long as power is applied, without the need for periodically rewriting the data into memory.

Symmetrically Addressable SIMM: A SIMM, the memory content of which is configured as two independent banks. Each 16-bit wide bank contains an equal number of rows and columns and is independently addressable by the CPU via twin row address strobe registers in the DRAM controller.

SYSCLK: ISAbus System Clock. The ~8.33MHz clock signal present on the ISAbus to which all bus transactions are synchronized.

System Memory: See *Conventional Memory*.

— T —

Terabyte (TB or TByte): Approximately one thousand billion (US) or one billion (Great Britain) bytes. 2^40 = 1,099,511,627,776 bytes exactly.



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— U —

Universal Serial Bus (USB): A new serial data bus that is intended to eliminate the need for separate serial, parallel, mouse, keyboard, joystick, etc. ports on a PC-compatible. These ports can be conceivably replaced by a few, daisy-chained USB ports, all with identical connectors but capable of much higher throughput, upwards of 12Mbs.

User Editable Drive (UED): A feature of the EPC-9's Phoenix NuBIOS. When a "User" type hard disk drive setting shows in the IDE Adapter Sub-Menu the BIOS queries the hard disk drive for the purpose of retrieving disk geometry. If the hard disk drive is capable of providing this information, the BIOS uses it to automatically set up the drive for use with the system.

— V —

Video Electronics Standards Association (VESA): A group of hardware and software vendors that define specifications for hardware and software interfaces for a variety of devices.



Video Graphics Adapter (VGA): A popular PC graphics controller and display adapter standard developed by IBM. The standard specifies, among other things, the resolution capabilities of the display device. Display devices meeting the VGA standard must be capable of displaying a minimum resolution of 640 horizontal pixels by 480 vertical pixels with at least 16 screen colors.

— W - X - Y - Z —

Wait State: A period of one or more microprocessor clock pulses during which the CPU suspends processing while waiting for data to be transferred to or from the system data or address buses.

— —

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Appendix G - SVGA and the PMC-1 Video Module

Video Controller Hardware

The PMC-1 Video Module uses the Cirrus Logic SVGA GD5446 video graphics controller connected to the 33MHz PCI bus to give the best possible graphics performance. The PMC-1 conforms to the PC Mezzanine Card (IEEE-P1386) form factor.

The available resolution depends upon the amount of installed memory. Table G-1 shows the available resolutions.

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Resolution	No. of Colors	Bits per Pixel	Memory Required
640x480	256	8	512KB
640x480	32K	15/8	1MB
640x480	64K	16	1MB
640x480	16M	24	1MB
640x480	16M	32	2MB
800x600	16	4	512KB
800x600	256	8	512KB
800x600	32K	15/8	1MB
800x600	64K	16	1MB
800x600	16M	24	2MB
800x600	16M	32	2MB
1024x768	16	4	512KB
1024x768	256	8	1MB
1024x768	32K	15/8	2MB
1024x768	64K	16	2MB
1024x768	16M	24	2MB
1280x1024	16	4	1MB
1280x1024	256	8	2MB

Table G-1. Video Resolutions Available.

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Installing the PMC-1 SVGA Video Module

Warning: Normally, the PMC-1 Video Module is ordered as part of the EPC-9 and installed at the factory. The procedure below requires careful work by a trained technician working in an ESD-controlled environment. If, after reading the procedure, you have any doubt about successfully performing the procedure, please contact your RadiSys representative for assistance.

To install the PMC-1 in the EPC 9:

1. Remove the PMC-1 from its static shielding envelope. Place the PMC-1 and the EPC-9 on a static-free work surface. You must carefully maintain a static-free environment throughout this procedure.

2. Locate the package containing 4 small screws and an O-ring. It came with the PMC-1. The screws will be used to mount the PMC-1 to the EPC-9 Carrier Board. The O-ring will be used to seal the PMC-1 Front Panel into the PMC0 opening in the EPC-9 Front Panel.

3. Locate and remove the two screws that secure the front panel to the PMC-1 circuit board. Remove the two jack screws that attach the front panel to the VGA connector. Remove the front panel. Save the screws. They will be used to re-attach the PMC-1 circuit board to the front panel.

4. Locate and remove the two screws that secure the stand-offs to the PMC-1 circuit board. Remove the stand-offs. Save the screws. They will be used to re-attach the PMC-1 circuit board to the stand-offs.

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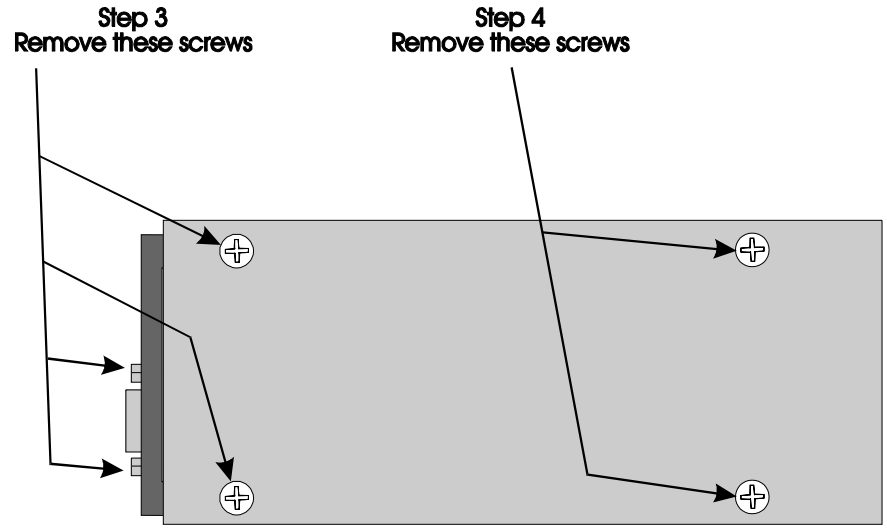


Figure G-1. SVGA Module Installation Steps 3 and 4

5. Remove the front panel of the EPC-9 by removing the 6 jack screws - 2 each at the COM A, COM B, and LPT1 connectors. Then remove the (2) long screws, nuts, and sleeves that attach the VME ejector handles.

6. Remove the three screws that secure the EPC-9 Carrier Board to the EPC-9 Main Board.

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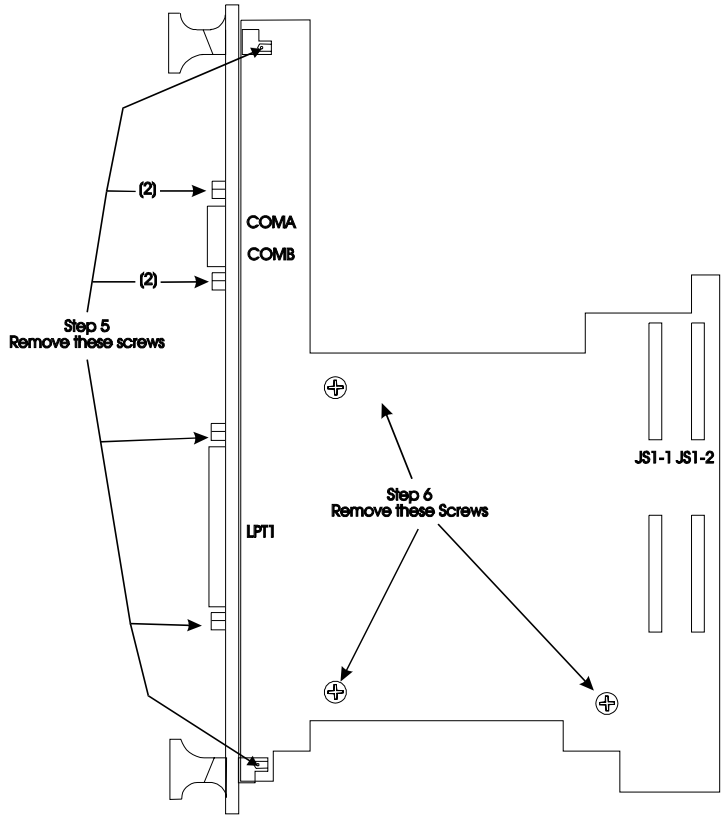


Figure G-2. SVGA Module Installation Steps 5 and 6.

7. Remove the Carrier Board by carefully unplugging the connector labeled J1. Pull straight up until the Carrier Board is separated from the Main Board.

8. Use two of the screws mentioned in step 2 to secure the PMC-1 Front Panel to the Carrier Board. Be sure to mount the Front Panel so that the opening for the VGA connector is located at the lower side of the EPC-9 Front Panel opening labeled PMC0.

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9. Use the other two screws mentioned in step 2 to secure the standoffs (mentioned in step 4) to the Carrier Board.

10. Re-attach the Carrier Board to the Main Board by pressing them together at the connector labeled J1. Align the male and female halves of the connector carefully before you press them together. Install the two screws you removed in step 6.

11. Install PMC-1 circuit board by plugging it into JS1-1 and JS1-2. Install screws through the circuit board into the front panel lugs and the standoffs.

12. Install the O-ring in the groove in the PMC-1 Front Panel.

13. Re-install the EPC-9 Front Panel by sliding it carefully over the PMC-1 Front Panel O-ring and the O-ring in the blank panel.

14. Install the 6 jack screws you removed in step 5 and the two jack screws you removed in step 3.

15. Install the 2 long screws, nuts, and sleeves you removed in step 6.

Display Drivers and Utilities Software

The SVGA Driver for Windows NT/4.0 is supplied by Cirrus Logic and has the following nomenclature:



Product: GDS5446
Software revision: 1.14
Document release date: 11-1-96

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Cirrus Logic Support

If there are any newer versions of the Cirrus driver software provided with your PMC-1, they will be available from Cirrus Logic support. They maintain a web page at http://www.cirrus.com/support/. Also, if you need answers to questions about the Cirrus chip, you can contact them at e-mail: ui-support@corp.cirrus.com, phone: 510-623-8300, or FAX: 510-252-6020.



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Notes

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Appendix H - Error Messages & Diagnosis

Boot Failures

The System BIOS halts and attempts to display an error message on the VGA monitor when it encounters the following error conditions:

1. Fixed disk error
   - No drive connected
   - Configured for 0 cylinders
   - Controller reset failed
   - Drive not ready
   - Track 0 seek timed out
   - Drive initialization failed
   - Drive recalibration failed
   - Last track seek failed



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2. Video error
   - Color/Mono switch not set correctly
3. Timer error
   - System timer (0) failed
4. Diskette error
   - Floppy type does not match setup
5. I/O chip error
   - I/O conflicts exist for serial and parallel ports, floppy, hard disk (any or all)
6. Other errors
   - IRQ conflict, unsupported COM port configuration, keyboard locked
   - Pentium cooling fan failure

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Troubleshooting

This section deals with problems that you may encounter that do not provide an error message.

Symptoms	Possible cause(s)	Solution
System appears to boot (RUN LED is on, IDE LED blinks) but no video.	The PMC-1 Video Module may not be properly seated or, if used, the EXM-based video adapter may not be fully seated in subplane.	Remove the EXM-based video adapter, if used. If the subplane is secured to the VMEbus backplane by retaining screws, verify that the subplane is not warped from over-tightening the screws. Re-insert the video adapter and verify proper seating into the subplane.
	Monitor or cable problem (with or without onboard video).	Verify that the cable pins are not bent and the cable is fully seated in the video adapter. If necessary, try the monitor on another system to verify that the monitor is good.
	Subplane failure or other hardware failure (with or without onboard video).	Call RadiSys Technical Support.
	If EXM-based video is used, the EPC-9 cannot talk to EXM expansion interface.	Call RadiSys Technical Support.



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Symptoms	Possible cause(s)	Solution
System fails at power-up -will not run power-on self-test. May be accompanied by combinations of beep tones from the speaker.	The system is not getting power.	Check the backplane and verify that +5V power is good. Verify that the subplane is fully seated in the VME backplane and the EPC-9 is fully seated in the subplane.
	BIOS detects a failure	Note BIOS Beep Code. Refer to *BIOS Beep Codes*, below.
	SODIMM memory module missing or loose.	Check that the SODIMMs are still present and connected. Remove and re-seat SODIMM modules in sockets.
	Hardware failure.	This cannot be diagnosed in the field. Call RadiSys Technical Support.
Serial port(s) do not work.	Bad power.	Verify that backplane +12V and -12V are good.
	Interrupt conflicts	An EXM module is using the same interrupts as COM1 and/or COM2. Verify that no other card in the EPC-9 subsystem is using IRQ3 or IRQ4.
	Port hardware failure.	Call RadiSys Technical Support.
System hangs during boot process (MASTER LED on; RUN LED off)	VMEbus has no Slot-1 controller providing bus timeout.	You are probably loading an expanded memory manager (for example, **EMM386.EXE**) in your **CONFIG.SYS** file. This can cause the system to hang if there is no Slot-1 controller or the Slot-1 controller is not providing the proper bus timeout.

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Symptoms	Possible cause(s)	Solution
System will not talk across VMEbus.	The VMEbus backplane may not be jumpered correctly.	See the section *Installing the VMEbus Backplane Jumpers* in Chapter 2.
	There may be no Slot-1 controller providing bus arbitration.	Determine that the controller is in the left-most position and that the Slot-1 controller jumper is set.
	EPC-9 or subplane may have bent pins.	Remove the EPC-9 and the subplane and verify that no pins are bent. Then reinsert the subplane and the EPC-9.
	VMEbus interface failure.	Call RadiSys Technical Support.

Table H-1. Troubleshooting Error Messages.



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BIOS Beep Codes

If the BIOS detects a critical error condition while running the Power On Self Test (POST) code, it may halt after issuing a beep code and attempting to display the error code in the upper left corner of the screen. The audible codes consist of patterns of beeps and pauses. If this occurs, you should contact your supplier for technical support.

Beep Pattern	Condition
1 short	POST OK
2 short	POST error, such as EXM configuration or keyboard error. Refer to the message on the screen to determine the cause
one long, two short	Insert BIOS update disk now.
one long, three short	Video memory error.
3 short	BIOS update disk missing. Either insert the BIOS update disk or turn the system off and then back on.

Table H-2. BIOS Beep Codes.

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