

ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Visit our website - *Click HERE*



PROMENTUM™

SINGLE BOARD COMPUTER

TECHNICAL PRODUCT SPECIFICATION

MPCBL0040

RadiSys
THE POWER OF WE

www.radisys.com

007-03222-0000 • April 2008

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Release History

Date	Revision	Description
November 2005	001	Initial release of this document
May 2006	002	Revised for production release of MCPBL0040 product
August 2006	003	Major updates to the “Serial Over LAN” and “Firmware Update Utilities” chapters
April 2007	004	Miscellaneous edits throughout the document
May 2007	005	Added “Sensor Device Record (SDR) Threshold Management” section
October 2007	006	“IPMC Hardware Sensor and Events” table updated “Analog Sensor and Threahold” table updated Reliability information added Auxiliary OEM IPMI Commands sections added
April 2008	0000	Document and part number converted to RadiSys format

Where to get more product information

Please visit the RadiSys Web site at www.radisys.com for product information and other resources. Downloads (manuals, release notes, software, etc.) are available via the Technical Support Library product links at www.radisys.com/support or the product pages at www.radisys.com/products.

Copyright © 2008 by RadiSys Corporation. All rights reserved.
RadiSys is a registered trademark and Promentum is a trademark of RadiSys Corporation.
All other trademarks, registered trademarks, service marks, and trade names are the property of their respective owners.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Contents

Release History 2

Where to get more product information 2

1.0 Introduction 11

1.1 Document Organization 11

1.2 Glossary 12

2.0 Feature Overview 15

2.1 Application 15

2.2 MPCBL0040 Functional Description 15

2.2.1 Rear Transition Module 17

2.2.2 Dual-Core Intel® Xeon® Processor LV 2.0 GHz Processors 18

2.2.3 Chipset 18

2.2.3.1 Intel® E7520 Memory Controller Hub 18

2.2.3.2 Intel® 6300ESB I/O Controller Hub 19

2.2.3.3 Intel® 82571EB Gigabit Ethernet Controller 19

2.2.4 Memory 20

2.2.5 I/O 21

2.2.5.1 Gigabit Ethernet 21

2.2.5.2 Serial Attached SCSI (SAS) Controller 22

2.2.5.3 USB 2.0 22

2.2.5.4 Serial Ports 22

2.2.6 AdvancedMC Slot 23

2.2.7 Firmware Hub 24

2.2.7.1 FWH 0 (Main BIOS) 24

2.2.7.2 FWH 1 (Backup/Recovery BIOS) 24

2.2.7.3 BIOS Backup Mechanism 24

2.2.8 On-board Power Supplies 25

2.2.8.1 Power Input Module 25

2.2.8.2 Tyco QBW 12 V Isolated Converter 26

2.2.8.3 IPMC Standby Power 26

2.2.8.4 3.3 V Isolated Converter 26

2.2.8.5 Processor Voltage Regulator Down (VRD) 26

2.2.9 Intelligent Platform Management Controller 27

2.2.10 128 MByte Flash Drive 27

2.2.11 Real-Time Clock 27

2.2.12 Timers 28

2.2.12.1 Timer Accuracy 28

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

3.0 Operating the Unit 29
3.1 Ejector Handles 29
3.2 Removing Hard Disk Drive and DIMM Covers 30
3.3 Memory (DIMM) Installation 31
3.4 Serial Attached SCSI (SAS) Hard Drive Installation 32
3.5 AdvancedMC Module Installation 33
3.6 Rear Transition Module (RTM) Installation 34
3.7 BIOS Configuration 34
3.8 Remote Access Configuration 34
3.9 Boot Devices 34
3.9.1 Booting from a SAS Hard Disk 34
3.9.2 Booting from a PATA Flash (On-board) 34
3.9.3 Booting from a USB Device 35
3.9.4 Booting from a LAN (PXE Boot) 36
3.10 Digital Ground to Chassis Ground Connectivity 37
3.11 Identifying MPCBL0040 Ethernet MAC Addresses 38
3.12 Cable Information 39
3.13 Firmware Updates 39
3.14 Operating System Install Tips 39

4.0 Connectors and LEDs 41
4.1 Backplane and Front Panel Connectors 41
4.2 Front Panel Connectors 43
4.2.1 USB Connector (J3) 44
4.2.2 Serial Port Connector (J4) 44
4.2.3 Ethernet 10/100/1000 Connectors (J34, J36) 46
4.2.4 Front Panel SAS Connector (J8) 47
4.2.5 Front Panel Reset Button 47
4.2.6 Front Panel LEDs 47
4.3 DIP Switches 50
4.4 On-Board Connectors 53
4.4.1 AdvancedMC Connector (J2) 53
4.4.2 Serial Attached SCSI (SAS) Connector (J8) 55
4.4.3 Extended ITP700 Debug Port Connector (J7) 57
4.5 Backplane Connectors 58
4.5.1 Power Distribution Connector (P10) 58
4.5.2 AdvancedTCA Data Transport Connector (J23) 60
4.5.3 Zone 3 Rear Transition Module Power Connector (J30) 62
4.5.4 Zone 3 Rear Transition Module Data/Control Connector (J31) 63
4.5.5 Zone 3 Rear Transition Module Data Connector (J32) 65
4.5.6 Alignment Blocks 65

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.0 Hardware Management 67
5.1 Supervision 69
5.2 Sensor Data Record (SDR) 69
5.2.1 Sensor Type 70
5.2.2 Event/Reading Type 70
5.2.3 Event Thresholds/Triggers 70
5.2.4 Assertion/De-assertion Enables 70
5.2.5 Readable Value/Offsets 70
5.2.6 Event Data 70
5.2.7 Health LED On/Off 71
5.2.8 Rearm Sensors 71
5.2.9 Standby 71
5.2.10 Polling Time 71
5.2.11 Managing Device 71
5.3 System Event Log (SEL) 85
5.3.1 Analog Sensors 86
5.3.2 Temperature Sensor Locations 88
5.3.3 Processor Events 89
5.3.4 DIMM Memory Events 89
5.3.4.1 DIMM Configuration Mismatch 89
5.3.4.2 Correctable Errors 89
5.3.4.3 Single-Bit ECC Errors 90
5.3.4.4 Uncorrectable Errors 90
5.3.5 System Firmware Progress (POST Error) 90
5.3.6 Port 80h POST Codes 91
5.3.7 Critical Interrupts 91
5.3.8 IPMB Link Sensor 91
5.3.9 FRU Hot Swap 91
5.3.10 Ethernet Link Status 91
5.3.11 Power Feeds 92
5.3.12 IPMC Watchdog Timer Reset 92
5.4 Field Replaceable Unit (FRU) Information 92
5.4.1 Common Header 92
5.4.2 Board Area 93
5.4.3 Product Area 93
5.4.4 Multirecord Area 93
5.4.4.1 BIOS, Firmware, CPU and RAM Information 94
5.4.5 MPCBL0040 FRU Record 94
5.4.6 FRU Area for Customer-Specific Information 103
5.4.7 Writing to the Customer FRU MRA 103
5.5 E-Keying 104
5.6 IPMC Platform Event Filtering (PEF) 106
5.7 IPMC Firmware Code Organization 106
5.7.1 Functional Description 107
5.7.2 IPMC Boot Block 107
5.8 IPMC Firmware Updates 108
5.9 Ejector Mechanism 108
5.10 Hot Swap LED 109
5.11 ACPI 110

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.12 Reset Types 110
5.12.1 Reset Control Sources 111
5.12.2 Payload Reset Diagram 112
5.12.3 Front Panel Payload Reset 112
5.12.4 IPMI Commanded Reset 112
5.12.5 Watchdog Timer Expiration 113
5.12.6 FRB3 Failure 113
5.13 IPMC Reset Control 113
5.13.1 Standby Power On Reset 113
5.13.2 IPMC Exit Firmware Update Mode 113
5.13.3 IPMI BMC Cold Reset Command 114
5.14 Watchdog Timers (WDTs) 114
5.14.1 WDT #1 (IPMI Watchdog Timer) 114
5.14.2 WDT #2 (IPMC Hardware Watch Dog Timer) 115
5.15 FRU Payload Control 115
5.15.1 Cold Reset 115
5.15.2 Warm Reset 115
5.15.3 Graceful Reboot 116
5.15.4 Diagnostic Interrupt 117
5.16 OEM IPMI Commands 118
5.17 Auxiliary OEM IPMI Commands 131
5.17.1 Pausing Board CPU Startup 131
5.17.2 Pausing FRU Startup: AMCStartupPause 132
5.17.3 Fake AMC Removal 133

6.0 BIOS Features 135
6.1 Introduction 135
6.2 BIOS Flash Memory Organization 135
6.3 Complementary Metal-Oxide Semiconductor (CMOS) RAM 135
6.4 Redundant BIOS Functionality 135
6.5 Language Support 136
6.6 Recovering BIOS Data 136
6.7 Fast Booting Systems 136
6.7.1 Quick Boot 136
6.8 BIOS Security Features 137
6.9 Remote Access Configuration 138
6.10 Boot Device Priority 139
6.11 Progressive Boot Support 139
6.11.1 Progressive Boot Mechanism 139
6.12 Diagnostics Boot Sequence Configuration 140
6.13 Pre-Defined Resources for AdvancedMC Modules 141
6.14 Legacy USB Support 142

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.0 BIOS Setup 143
7.1 Introduction 143
7.2 Main Menu 144
7.3 Advanced Menu 145
7.3.1 CPU Configuration Submenu 147
7.3.2 IDE Configuration Submenu 149
7.3.3 ACPI Configuration Submenu 151
7.3.4 System Management Submenu 152
7.3.5 PCI Configuration Submenu 153
7.3.6 Diagnostics Boot Sequence Configuration Submenu 155
7.3.7 Event Logging Configuration Submenu 156
7.3.8 PCI Express* Configuration Submenu 157
7.3.9 Ethernet Ports Direction Configuration Submenu 158
7.3.10 Progressive Boot Configuration 160
7.3.11 SMBIOS Configuration Submenu 161
7.3.12 Remote Access Configuration Submenu 162
7.3.13 USB Configuration Submenu 164
7.4 PCIPnP Menu 165
7.5 Boot Menu 166
7.5.1 Boot Settings Configuration Submenu 166
7.5.2 OS Load Watchdog Timer Configuration Submenu 167
7.5.3 Boot Device Priority Submenu 167
7.6 Security Menu 170
7.7 Chipset Menu 171
7.7.1 NorthBridge Configuration Submenu 171
7.7.2 SouthBridge Configuration Submenu 171
7.8 Exit Menu 172

8.0 Error Messages and Checkpoints 173
8.1 BIOS Error Messages 173
8.2 Port 80h POST Codes 174

9.0 Serial Over LAN 179
9.1 References 179
9.2 SOL Architecture 179
9.2.1 Architectural Components 181
9.2.1.1 IPMC 181
9.2.1.2 Ethernet Controller 181
9.3 Theory of Operation 182
9.3.1 Front Panel Serial Port or RTM 182
9.3.2 Serial Over LAN 182
9.4 Serial Over LAN Client 183
9.5 Reference Configuration Script 183
9.6 Supported Usage Model 184
9.6.1 Configuring the Blade for SOL 184
9.7 Reference Script (reference_cfg) 185
9.7.1 SOL Configuration Reference Script (reference_cfg) 185
9.7.2 Default Behavior 185
9.7.3 SOL User Information 185
9.7.4 LAN Parameters 186
9.7.5 SOL Parameters 186
9.7.6 Channel Parameters 186
9.7.7 Command Line Options 187

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

9.8 Setting up a Serial Over LAN Session 187
9.8.1 Target Blade Setup 187
9.8.1.1 BIOS Configuration 188
9.8.1.2 Operating System Configuration 189
9.8.1.3 sbcutils RPM Installation 190
9.8.1.4 Execute the reference_cfg Script 191
9.8.2 Client Blade Setup 193
9.8.2.1 Configure Ethernet Port 193
9.8.2.2 Installing ipmitool 194
9.8.2.3 Starting an SOL Session 194
9.8.2.4 Checking SOL Configuration 195
9.8.2.5 Ending an SOL Session 195
9.8.2.6 Recovering SOL Session if ipmitool Segfaults 196
9.9 Operating Systems for SOL Client (ipmitool) 196

10.0 Firmware Update Utilities 197
10.1 Firmware and BIOS Locations 197
10.2 BIOS Image Updates 197
10.2.1 Updating BIOS under MS-DOS 197
10.2.2 Updating BIOS under Linux (Interactive mode) 198
10.2.3 Updating BIOS under Linux (Quiet Mode) 198
10.2.4 Synchronizing BIOS Image and Settings from FWH0 (Main) to FWH1 (Backup) .. 199
10.2.5 Copying and Saving BIOS (Including CMOS Settings) 200
10.2.5.1 Copying BIOS.bin from the SBC 200
10.2.5.2 Saving BIOS.bin to the SBC 200
10.2.6 BIOS Utility Command Line Options 201
10.3 Updating IPMC Firmware 201
10.3.1 Updating IPMC Boot Block 202
10.3.2 Updating RTM Boot Block 206
10.4 SBC Utilities Installation Procedure 206
10.4.1 Contents of SBC Utilities RPM Package 207
10.4.2 Remove Existing Packages 207
10.4.3 Installing the sbcutils Package 207
10.5 System Configuration 208
10.5.1 Introduction 208
10.5.2 Configuring the Promentum™ MPCMM0001/0002 CMM 209
10.6 SBC Update Utility 211
10.6.1 Communication Interfaces 211
10.6.2 IPMC Operational Code Firmware Update Modes 212
10.6.3 Staged Update Process 213
10.6.4 Firmware Naming Scheme 214
10.6.5 Utility Invocation 215
10.6.6 Automatic Firmware Update 218
10.6.6.1 Automatic Firmware Update using KCS Interface 218
10.6.6.2 Automatic Firmware Update via RMCP Bridging 219
10.6.7 Direct Firmware Update 219
10.6.7.1 Direct Firmware Update Using the KCS Interface 220
10.6.7.2 Direct Firmware Update to RTM via KCS 220
10.6.7.3 Direct Firmware Update via RMCP Bridging 221
10.6.7.4 Direct Firmware Update to RTM via RMCP Bridging 222
10.6.8 Staged Firmware Update 223
10.6.8.1 Staged Firmware Update Using KCS Interface 223
10.6.8.2 Creating a Pending Staged Firmware Update 224
10.6.8.3 Staged Firmware Update via RMCP Bridging 224

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.9 Canceling Staged Firmware Update 225
10.6.9.1 Cancel Staged Firmware Update via KCS Interface 225
10.6.9.2 Cancel Staged Firmware Update via RMCP Bridging 226
10.6.10 Setting Manual Rollback of the Firmware 226
10.6.10.1 Manual Rollback via KCS Interface 226
10.6.10.2 Manual Rollback via RMCP Bridging 227
10.6.11 Retrieving FRU and SDR Data 227
10.6.11.1 Retrieving FRU and SDR via KCS Interface 227
10.6.11.2 Retrieving FRU and SDR Information Using the -o Option 228
10.6.11.3 Retrieving FRU and SDR via RMCP Bridging 228
10.6.12 Updating FRU Data 229
10.6.13 Writing Data to the FRU on the SBC or RTM 230
10.6.13.1 Incremental FRU Update via KCS 230
10.6.13.2 Incremental FRU Update via RMCP Bridging 230
10.6.14 Full FRU Update via KCS 231
10.6.15 Full FRU Update via RMCP Bridging 232
10.6.16 Writing SDR Data 233
10.6.16.1 SDR Update via KCS 233
10.6.16.2 RTM SDR Update via KCS 233
10.6.16.3 SDR Update via RMCP Bridge 234
10.6.17 RTM SDR Update via RMCP Bridge 234
10.6.18 Writing Asset Tag Information 234
10.6.19 Output from the –M info Option 235
10.7 Sensor Device Record (SDR) Threshold Management 236
10.7.1 Reading Thresholds Using KCS Interface 236
10.7.2 Reading Thresholds via RMCP Bridging 238
10.7.3 Changing Thresholds Values Using KCS Interface 238
10.7.4 Changing Thresholds Values via RMCP Bridging 239
10.7.5 Restoring Factory Default Thresholds Values Using KCS Interface 239
10.7.6 Restoring Factory Default Thresholds Values via RMCP Bridging 240
10.8 Displayed Messages 240

11.0 Specifications 255
11.1 Mechanical Specifications 255
11.1.1 Board Outline 255
11.1.2 Backing Plate and Primary Side Top Cover 256
11.2 Environmental Specifications 257
11.3 Reliability Specifications 258
11.3.1 Mean Time Between Failure (MTBF) Specifications 258
11.3.1.1 Environmental Assumptions 258
11.3.1.2 General Assumptions 258
11.3.1.3 General Notes 258
11.4 Power Consumption 259
11.5 Board Layer Specifications 260
11.6 Cooling Requirements 260
11.7 Thermals 261
11.8 Weight 262
11.9 Compliance 262

12.0 Agency Information 263
12.1 North America (FCC Class A) 263
12.2 Canada – Industry Canada (ICES-003 Class A) 263
12.3 European Union 263

13.0 Certifications 265

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

14.0 Safety Warnings 267
14.1 Safety Precautions 267
A: Supported IPMI Commands 269
B: Reference Documents 275

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

1.0 Introduction

1.1 Document Organization

This document gives technical specifications related to the Promentum™ MPCBL0040 Single Board Computer (SBC).

The following summarizes the focus of each section in this document.

Chapter 1.0, "Introduction" gives an overview of the information contained in the MPCBL0040 Technical Product Specification as well as a glossary of acronyms and important terms.

Chapter 2.0, "Feature Overview" introduces key features of the MPCBL0040.

Chapter 3.0, "Operating the Unit" provides specifics for configuring the MPCBL0040, including BIOS configuration and jumper settings.

Chapter 4.0, "Connectors and LEDs" includes an illustration of LEDs, connector locations, connector descriptions, and pinout tables.

Chapter 5.0, "Hardware Management" provides a high-level overview of the IPMI implementation based on the PICMG* 3.0 and IPMI 2.0 specifications.

Chapter 6.0, "BIOS Features" provides an introduction to the BIOS, and the System Management BIOS, stored in flash memory on the MPCBL0040 SBC.

Chapter 7.0, "BIOS Setup" describes the interactive menu system of the BIOS Setup program, which allows users to configure the BIOS for a given system.

Chapter 8.0, "Error Messages and Checkpoints" lists BIOS error messages, Port 80h POST codes, and bus initialization checkpoints, and provides a brief description of each.

Chapter 9.0, "Serial Over LAN" describes the installation and configuration of Serial Over Lan (SOL), a specification for transmitting serial port data over an Ethernet connection, which allows the viewing of serial port data, thus providing a virtual remote terminal server for accessing a blade's serial port.

Chapter 10.0, "Firmware Update Utilities" describes how to use the board firmware utilities to update firmware on the board.

Chapter 11.0, "Specifications" contains the mechanical, environmental, and reliability specifications for the MPCBL0040.

Chapter 12.0, "Agency Information", Chapter 13.0, "Certifications" and Chapter 14.0, "Safety Warnings" document important safety precautions as well as regulatory requirements the MPCBL0040 is designed to meet.

Appendix A:, "Supported IPMI Commands" lists the IPMI commands supported by the MPCBL0040.

Appendix B:, "Reference Documents" lists related documentation.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

1.2 Glossary

The following is a list of the acronyms used in this document.

ACPI	Advanced Configuration and Power Interface
AdvancedMC	Advanced Mezzanine Card
AdvancedTCA	Advanced Telecommunications Compute Architecture
ASL	ACPI Source Language
BIOS	Basic Input/Output Subsystem. ROM code that initializes the computer and performs some basic functions.
Blade	An assembled PCB card that plugs into a chassis
DIMM	Dual Inline Memory Module
DMI	Desktop Management Interface
ECC	Error Correcting Code
EEPROM	Electrically Erasable Programmable Read-Only Memory
Fabric Board	A board capable of moving packet data between Node Boards via the ports of the backplane. This is sometimes referred to as a switch.
Fabric Slot	A slot supporting a link port connection to/from each Node Slot and/or out of the chassis
FPGA	Field Programmable Gate Array
FRB	Fault Resilient Booting
FWH	Firmware Hub
GPIO	General Purpose I/O
Hyper-Threading Technology (HT Technology)	Allows a single (or dual) physical processor, to appear as two (or quad) logical processors to a HT Technology-aware operating system.
I^2C	Inter-Integrated Circuit. A two-wire interface commonly used to carry management data.
IBA	Intel® Boot Agent. Software that allows your networked client computer to boot using a program code image supplied by a remote server.
ICH	I/O Controller Hub
IDE	Integrated Device Electronics. A common, low-cost disk interface.
IPMB	Intelligent Platform Management Bus. A physical two-wire medium to carry IPMI information.
IPMC	Intelligent Platform Management Controller. An ASIC on the baseboard responsible for low-level system management.
IPMI	Intelligent Platform Management Interface. A programming model for system management.
KCS	Keyboard Controller Style interface
LPC Bus	Low Pin Count Bus. A legacy I/O bus that replaces ISA and X-bus. Refer to the *Low Pin Count (LPC) Interface Specification*.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

MCH	Memory Controller Hub
MTBF	Mean Time Between Failure. A reliability measure based on the probability of failure.
NEBS	Network Equipment Building System. A set of telco standards for equipment emissions, thermal, shock, contaminants, and fire suppression requirements.
NMI	Non-Maskable Interrupt. A low-level PC interrupt.
Node Board	A board capable of providing and/or receiving packet data to/ from a Fabric Board via the ports of the networks. The term is used interchangeably with SBC in this document.
MPCBL0040	A high-performance single board computer with an AdvancedMC slot
MPRTM0040	A Rear Transition Module (RTM) that can be used with the MPCBL0040
Node Slot	A slot supporting port connections to/from one or more Fabric slots. A Node slot is intended to accept a Node Board.
Physical Port	A port that physically exists. It is supported by one of many physical (PHY) type components.
POST	Power On Self Test
ROM	Read-Only Memory
RTM	Rear Transition Module. This term is used interchangeably with MPRTM0040 in this document.
SBC	Single Board Computer. This term is used interchangeably with Node Board and MPCBL0040 in this document.
SEL	System Event Log. Actions logged by the management controller.
SMBus	System Management Bus. Similar to I^2C.
SMI	System Management Interrupt. A low-level PC interrupt which can be initiated by the chipset or management controller. Used to service IPMC or handle things like memory errors.
SMS	System Management Software or Standard Microsystems Corporation*
SoL	Serial Over LAN
USB	Universal Serial Bus. A general-purpose peripheral interconnect. USB 1.1 operates up to 12 Mbps. USB 2.0 operates up to 480 Mbps.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

2.0 Feature Overview

2.1 Application

The AdvancedTCA* standards define open architecture modular computing components for carrier-grade, communications network infrastructure. The goals of the standards are to enable blade-based modular platforms to be:

- Cost effective
- High-density
- Highly available
- Scalable

These systems use a fabric I/O network for connecting multiple, independent processor boards, I/O nodes (for example, line cards), and I/O devices (for example, a storage subsystem).

2.2 MPCBL0040 Functional Description

This section describes the architecture of the MPCBL0040 SBC through functional block descriptions. Figure 1 shows the functional blocks of the MPCBL0040 SBC. The MPCBL0040 is a hot-swappable SBC with backplane connections to Gigabit Ethernet (GbE) ports on the base and fabric interface. The fabric interface of the MPCBL0040 board supports option 2 of the PICMG 3.1 specification.

On the front panel, the MPCBL0040 offers an AdvancedMC* slot, one USB port, one serial console port, two SAS ports (one physical SAS connector) and two Gigabit Ethernet ports.

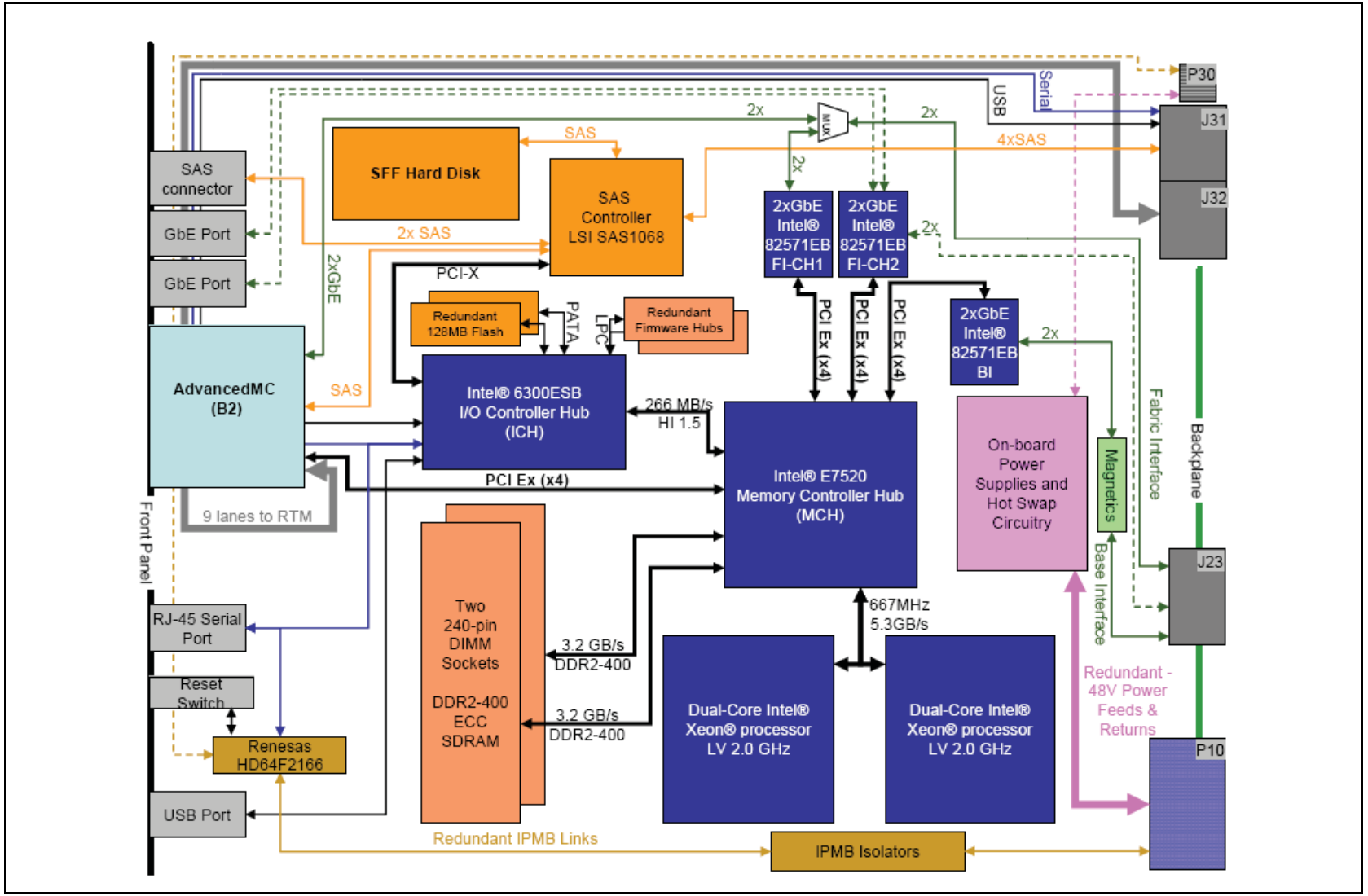
For storage, the board itself also supports an on-board Serial Attached SCSI (SAS) small form factor (SFF) hard disk and a two 128 MBytes of flash memory for user applications. In addition, there is a front panel SAS connector for external SAS drive connections and SAS connections to the RTM.

The SBC incorporates an Intelligent Platform Management Controller (IPMC) that monitors critical hardware functionality of the board such as temperature and voltage, responds to commands from the shelf manager, and reports events.

Power is supplied to the MPCBL0040 SBC through two redundant power supply connections. The board is fully operational over a supply voltage range of –43 VDC to -72 VDC.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Figure 1. MPCBL0040 SBC Block Diagram



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

2.2.1 Rear Transition Module

The MPCBL0040 board supports Rear Transition Modules.

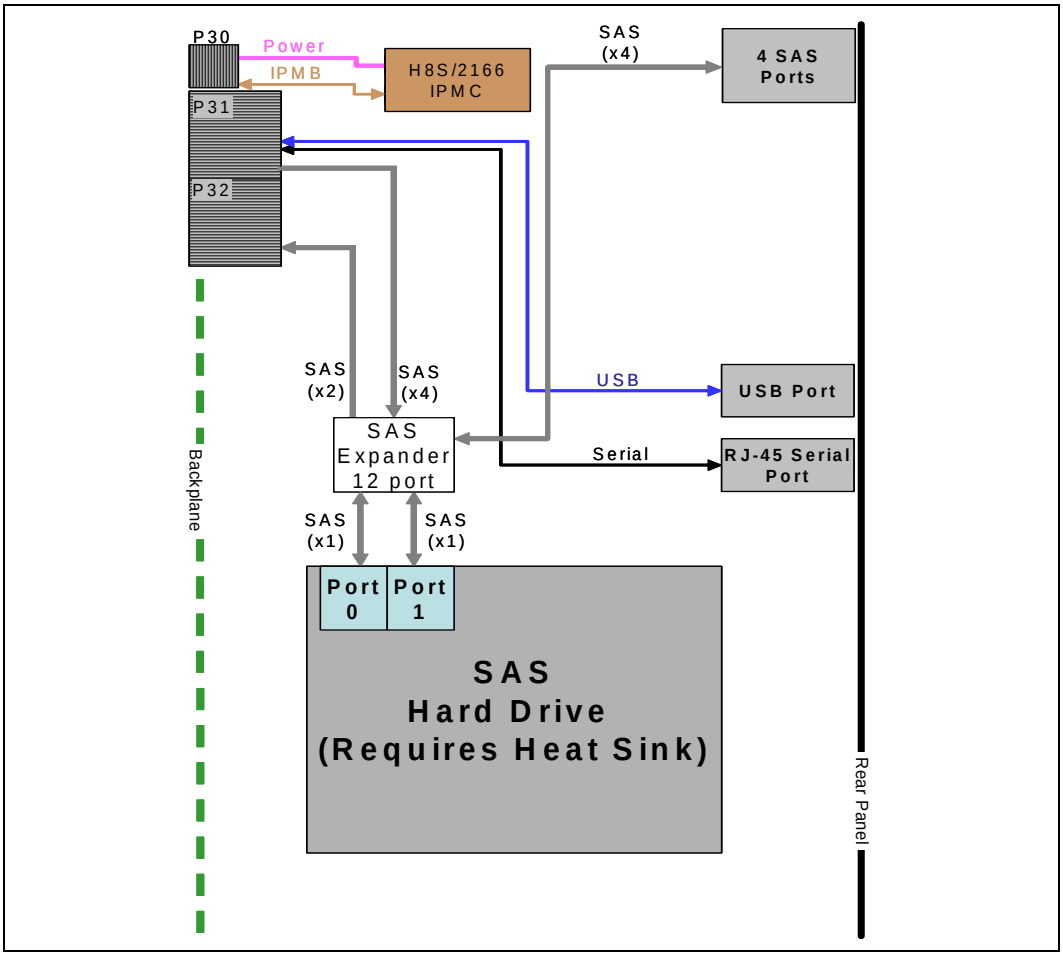
Intel has an RTM with product code MPRRTM0040, that supports the following interfaces:

- One USB port (this port complies with USB 1.1 specification only)
- One Serial console interface
- Four Serial Attached SCSI (SAS) ports for remote storage connectivity
- One on-board SAS hard drive.

Note: NOTE: Using the hard drive on the RTM requires the use of a heat sink in order to cool properly. For more details, refer to the *Promentum™ MPRTM0040 Rear Transition Module Technical Product Specification.*

Figure 2 shows a block diagram of the RTM developed for the MPCBL0040 SBC. Refer to the *Promentum™ MPRTM0040 Rear Transition Module Technical Product Specification* for detailed information.

Figure 2. MPRTM0040 RTM Block Diagram



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

2.2.2 Dual-Core Intel® Xeon® Processor LV 2.0 GHz Processors

The MPCBL0040 SBC supports two Dual-Core Intel® Xeon® processor LV 2.0 GHz processors with 667 MHz front side bus with the following benefits:

- Dual processor support, including an enhanced bus arbitration protocol, power-optimized 667 MHz front-side bus (FSB), and a 2 MB shared L2 cache per processor, that enables up to four high-performance cores per platform
- 36-bit memory addressing that supports more than 4 GBytes of memory
- FSB address, data parity, and an enhanced error reporting mechanism through the MCA (Machine Check Architecture) that ensures reliability and data integrity

For further details, refer to the *Dual-Core Intel® Xeon® processor LV 2.0 GHz Datasheet*.

2.2.3 Chipset

The MPCBL0040 uses the Intel® E7520 Chipset which comprises the following major components:

- Intel® E7520 Memory Controller Hub (MCH)
- Intel® 6300ESB I/O Controller (ICH)
- Intel® 82571EB Gigabit Ethernet Controller

Although a brief overview is provided here, detailed component information can be found in the documentation for the respective devices.

2.2.3.1 Intel® E7520 Memory Controller Hub

The architecture of the Intel® E7520 Memory Controller Hub (MCH) provides the performance and feature set required for servers, with configuration options facilitating optimization of the platform for workloads characteristic of communication, presentation, storage, performance computation, or database applications. To accomplish this, the MCH has numerous RASUM (Reliability, Availability, Serviceability, Usability, and Manageability) features on multiple interfaces.

The front side bus supports a base system bus frequency of 200 MHz. The address and request interface is double-pumped to 400 MHz, while the 64-bit data interface (+ parity) is quad-pumped to 800 MHz. This provides a matched system bus address and data bandwidths of 6.4 GBytes/s. The MCH provides an integrated memory controller for direct connection to registered DDR2-400 memory.

When used with the Dual-Core Intel® Xeon® processor LV 2.0 GHz processor, the maximum frequency is 133 MHz operating at 667 MT/s over the front side bus.

The MCH is compatible with the PCI Express* Interface Specification, Rev 1.0a. The MCH provides three configurable x8 PCI Express interfaces each with a max theoretical bandwidth of 4 GBytes. The MCH supports PCI Express Hot Swap. The MCH is a root class component as defined in the PCI Express Interface Specification, Rev1.0a.

The MCH interfaces with the Intel® 6300ESB ICH via a dedicated Hub Interface 1.5 supporting a peak bandwidth of 266 MByte/s using a x4 base clock of 66 MHz with parity protection.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

2.2.3.1.1 PCI Express Hot Swap

Support for PCI Express hot swap is divided into two parts:

- First, the MCH supports the standard software interface for hot-swap capability management as defined for PCI and PCI Express.
- Second, the MCH supports a mechanism for providing external hardware connectivity required to implement the standard register interface.

PCI Express ports B0 and C0 have Hot Swap support. The Hot-Swap signals from both of these ports communicate to a common Hot-Swap controller within the MCH using an external PCA9555 I/O expander, which is accessed by the MCH through SMBus 5. It is this external I/O expander that interfaces with Hot-Swap signals on the PCI Express slots.

The MCH assumes that it is actually connecting to a PCI Express add-in slot, which the MPCBL0040 does not have. The MPCBL0040 provides this hot-swap capability on the AdvancedMC slot instead. The AdvancedMC slot does not have all the extra signals such as the push button, sensors, and LEDs. Therefore, the IPMC on the MPCBL0040 board provides these type of signals to the MCH through the use of the PCA9555 I/O expander.

The PCI Express port mapping is given in Table 1.

Table 1. PCI Express Port Mapping

Port	Function
A0	Connects to Fabric Interface (Port 0, Channel 1 & 2) Gigabit Ethernet Controller 82571
A1	Connects to Fabric Interface (Port 1, Channel 1 & 2) Gigabit Ethernet Controller 82571
B0	Not used
B1	Connects to Base Interface Gigabit Ethernet Controller 82571
C0	Connects to AdvancedMC slot B2 (supports PCI Express hot-swap)
C1	Not used

2.2.3.2 Intel® 6300ESB I/O Controller Hub

The Intel® 6300ESB I/O Controller Hub (ICH) provides legacy function support similar to that of previous ICH-family devices, but with extensions in Serial ATA technology and 64-bit/66 MHz PCI-X support. The 6300ESB ICH also includes integrated USB 2.0 and USB 1.0 support, an LPC interface, a system management interface, a power management interface, integrated IOxAPIC and 8259 interrupt controllers, and an integrated DMA controller.

2.2.3.3 Intel® 82571EB Gigabit Ethernet Controller

The Intel® 82571EB Gigabit Ethernet Controller is a single, compact component with two fully integrated Gigabit Ethernet Media Access Control (MAC) and physical layer (PHY) ports. This device uses the PCI Express* architecture (Rev. 1.0a). The Intel 82571EB Gigabit Ethernet Controller provides two IEEE 802.3* Ethernet interfaces for 1000BASE-T, 100BASE-TX, and 10BASE-T applications. Both ports also integrate a Serializer-Deserializer (SerDes) to support Gigabit backplane applications. In addition to managing MAC and PHY Ethernet layer functions, the controller manages PCI Express packet traffic across its transaction, link, and physical/logical layers.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

2.2.4 Memory

The memory subsystem is designed to support Double Data Rate2 (DDR2) Synchronous Dynamic Random Access Memory (SDRAM) using the Intel® E7520 MCH. The MCH provides two independent DDR channels, which support DDR2 400 DIMMs. The peak bandwidth of each DDR2 branch channel is 3.2 GByte/s (8 Bytes x 400 MT/s) with DDR2-400. The two DDR2 channels from the MCH operate in lock step; the effective overall peak bandwidth of the DDR2 memory subsystem is 6.4 GByte/s for DDR2-400. Two 25 degrees 240-pin DIMM sockets support memory configuration up to 8 GByte of PC2-3200 registered DDR2-400 SDRAM. Table 2 summarizes the DIMM memory features and Table 3 gives the supported memory configurations.

Table 2. DIMM Memory Features

Feature	Parameter
DIMM slots	Two
Rank Structure	Single or Dual
Max DIMM speed	400MHz
Device width	x4 or x8
Parity Required	Yes

Note: DIMMs must be installed in matched pairs. DIMMs need to be identical in rank, size, device width and memory timing. For best performance 3-3-3 timing should be used.

Refer to the MPCBL0040 Compatibility Report for a list of DIMMs validated for the board.

Table 3. Supported Memory Configurations

Total Memory	J9 (DIMM 2)	J10 (DIMM 1)
2 GBytes	1 GByte DDR2-400 DIMM	1 GByte DDR2-400 DIMM
4 GBytes	2 GBytes DDR2-400 DIMM	2 GBytes DDR2-400 DIMM
8 GBytes	4 GBytes DDR2-400 DIMM	4 GBytes DDR2-400 DIMM

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

2.2.5 I/O

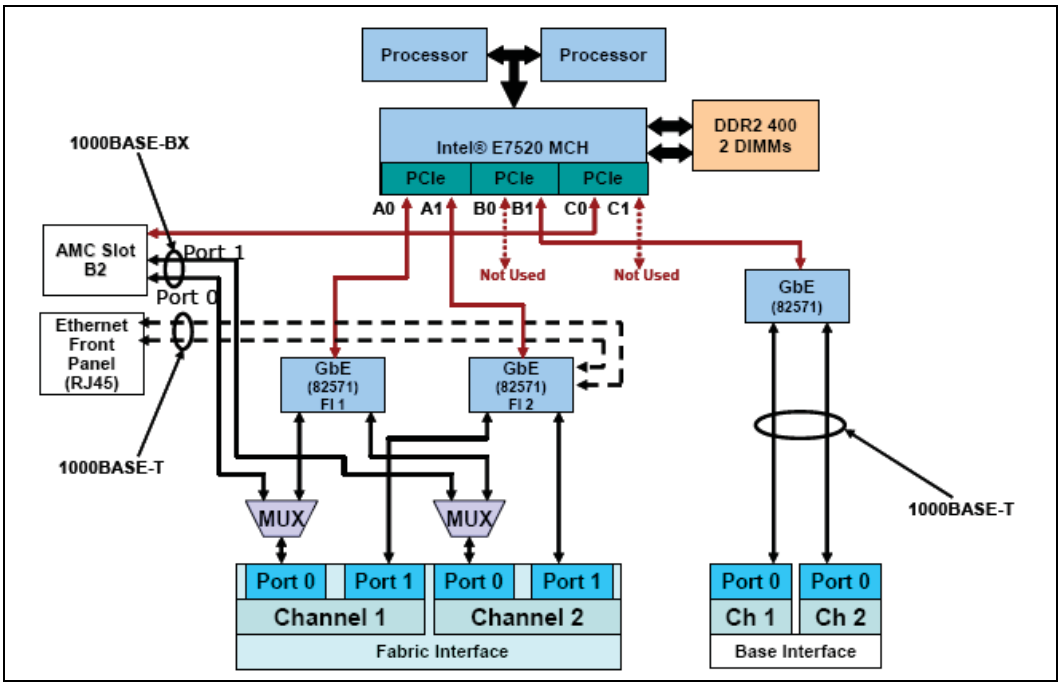
2.2.5.1 Gigabit Ethernet

The MPCBL0040 SBC implements six Gigabit Ethernet (GbE) interfaces from three separate Gigabit Ethernet controllers (Intel® 82571EB Gigabit Ethernet Controller). Two of these interfaces are routed to the base interface, and the other four are routed to the fabric interface on the AdvancedTCA backplane to support the PICMG* 3.0 (base) and 3.1 option 2 (fabric) specifications.

The user has the flexibility to route two of the fabric interface GbE ports (Port 1, Channel 1 & 2) to the front panel instead of the backplane fabric interface. This can be done by sending an OEM IPMI command via the Shelf Manager or by changing the direction in BIOS. Both ways require a payload reset for the direction change to take effect.

In addition, when an AdvancedMC module (type AMC.2) is installed that has GbE ports, these can be connected to the backplane fabric interface (Port 0, Channel 1 & 2) by changing the input of the the multiplexer (MUX).

Figure 3. Gigabit Ethernet Interface Block Diagram



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

2.2.5.2 Serial Attached SCSI (SAS) Controller

The MPCBL0040 has an 8-port Serial Attached SCSI (SAS) controller that supports one on-board SAS hard drive. The SAS controller is connected to the PCI-X bus of the Intel® 6300ESB I/O Controller Hub. All SAS ports have a serial point-to-point interface using a differential transmit/receive pair. The SAS controller has a flash device that is used to store it's firmware.

The SAS physical ports are mapped as follows:

- Port 0: On-board SAS hard disk drive
- Port 1: AdvancedMC Slot
- Port 2: Front Panel SAS Connector (see Table 12 for pinout information).
- Port 3: Front Panel SAS Connector (see Table 12 for pinout information).
- Port 4: Rear Transition Module 0
- Port 5: Rear Transition Module1
- Port 6: Rear Transition Module 2
- Port 7: Rear Transition Module 3

With SAS Firmware 1.15.00.03 and SAS BIOS 6.08.05, the SAS SCSI ID ports are mapped as follows:

- ID0: Reserved for user to specify. This setting can be changed by entering LSI SAS BIOS during boot cycle.
- ID1: On-board SAS hard disk drive
- ID2: AdvancedMC Slot
- ID3: Front Panel SAS Connector
- ID4: Front Panel SAS Connector
- ID11 - ID14: 4X SAS Connection to the Rear Transmission Module

Note: The hard drive is independent of the on-board IPMC circuitry, so in order to monitor the status of the hard drive, use SMART (Self-Monitoring, Analysis and Reporting Technology) software recommended by the hard drive vendor.

2.2.5.3 USB 2.0

The MPCBL0040 SBC has one front panel USB connector that supports USB 2.0 and 1.1. USB supports Plug & Play* and hot swapping operations (OS level) which allows USB devices to be automatically attached, configured, and detached, without rebooting. There is a second USB port which is routed to the Rear Transition Module (RTM).

Note: The default USB speed in BIOS is set to Full Speed (USB 1.1 data rate). The reason is the USB port on the Rear Transition Module can only operate at USB 1.1 data rates. If the MPCBL0040 is used without the MPRTM0020 RTM or if the external USB port on the RTM is not used, the BIOS can setting can be changed to HiSpeed (USB 2.0 data rate).

2.2.5.4 Serial Ports

The MPCBL0040 supports one serial port connected to the Intel® 6300ESB I/O Controller Hub. The serial port is routed to the front panel RJ-45 connector for normal operation. The serial port is also connected to the RTM. Both are active, but only one port can be used at a time.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

2.2.6 AdvancedMC Slot

The MPCBL0040 SBC has one single-width, full-height AdvancedMC slot in location B2. The MPCBL0040 SBC does not support Double-Width, Half-Height, or stacked Half-Height AdvancedMC modules.

Below is an overview of the AdvancedMC slot connections:

- One x4 PCI Express port that connects to the MCH. The port may train with a link width of x4 or x1. The PCI Express basic “x1” per pair link has a raw bit-rate of 5.0 Gbit/s bidirectional (2.5 Gbit/s each direction). This results in maximum bandwidth per pair of 250 MBytes/s given the 8b/10b encoding used to transmit data across this interface. For a x4 port, the maximum theoretical realized bandwidth is 1 GBytes/s in each direction or an aggregate of 2 GBytes/s.
- Two Gb Ethernet ports that connects to the fabric interface on the backplane through a multiplexer (MUX).
- One SAS port that connects to the on-board SAS controller
- 9 ports (12 to 20) connect to the RTM connector on the rear of the board (Zone 3).

The MPCBL0040 SBC supports AdvancedMC modules with a maximum power consumption of 25 watts and has independent hot swap circuitry for +12 V and +3.3 V connections.

Table 4 shows the port mapping from the AdvancedMC connector.

Table 4. AdvancedMC Connections

Link #	Function	Description
0	GEth0	AMC.2 Gigabit Ethernet connection to backplane fabric interface through a MUX: • GEth0 connects to port 0, channel 1 • GEth1 connects to port 0, channel 2
1	GEth1	
2	SAS	AMC.3 SAS/SATA connection to port 1 on the SAS hard drive controller
3		Not used
4	x4 PCIEx	AMC.1 PCI Express connection to interface C0 on the Memory Controller Hub (MCH)
5		
6		
7		
8		Not used
9		
10		
11		
12		To/From Rear Transition Module (RTM) Connector J32 Note: Signals are routed to J32 RTM connector on the MPCBL0040 board, but the MPRTM0040 Rear Transition Module does not use these signals.
13		
14		
15		
16		
17		
18		
19		
20		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Caution: Do not ship the MPCBL0040 SBC with any AdvancedMC modules installed. Shipping the MPCBL0040 SBC with an AdvancedMC modules installed may cause damage to the SBC or AdvancedMCs. Damage that occurs to the MPCBL0040 due to an AdvancedMC module installed during shipment will not be covered by the MPCBL0040 product warranty.

Caution: Do not operate the MPCBL0040 SBC without the AdvancedMC filler panel or AdvancedMC module installed. The AdvancedMC module slot should not be left open or uncovered when the MPCBL0040 SBC is in use. The MPCBL0040 SBC includes one AdvancedMC filler panel (Schroff* filler panel part # 20849-024 or equivalent), which is provided to optimize cooling and radiated emissions for the SBC.

2.2.7 Firmware Hub

The MPCBL0040 SBC has two physically separate 1 MByte BIOS flash devices:

- Primary BIOS flash (FWH0)
- Recovery BIOS flash (FWH1)

The flash is allocated for storing the binary code of the BIOS.

The SBC boots from the primary flash FWH0 under normal circumstances. During the boot process, if the BIOS determines that the contents of the primary flash FWH0 are corrupted, a hardware mechanism automatically changes the flash device select logic to boot from the recovery flash FWH1.

For instructions on how to update the BIOS, refer to Section 10.2, “BIOS Image Updates” on page 197. After completing the BIOS update, the user must reset the system in order for the new BIOS image to take effect.

2.2.7.1 FWH 0 (Main BIOS)

The BIOS executes code off of the flash device and performs checksum validation of its operational code. This checksum occurs in the boot block of the BIOS. The BIOS image is also stored in FWH0. When the user performs a BIOS update, the BIOS image is stored in FWH0 only. FWH0 also stores the factory default CMOS settings and user-configured CMOS settings.

2.2.7.2 FWH 1 (Backup/Recovery BIOS)

FWH 1 stores the recovery BIOS. In the event of checksum failure on the primary BIOS operational code, the BIOS requests the IPMC to switch flash device, so that the board is able to boot from FWH1 for recovery.

2.2.7.3 BIOS Backup Mechanism

The on-board Intelligent Platform Management Controller (IPMC) manages which of the two BIOS flash devices is selected during the boot process. The IPMC can change the BIOS flash device selection from FWH0 to FWH1 and reset the processor.

The default state of this control configures the primary Firmware Hub (FWH0) device ID to be the boot device; the secondary FWH1 is assigned the next ID. The secondary FWH1 responds to the address range just below the primary FWH0 in high memory.

The IPMC sets the ID for both FWH devices. Boot accesses are directed to the FWH with ID = 0000; unconnected ID pins are pulled low by the FWH device. In this way, the IPMC may select which flash device is used for the boot process.

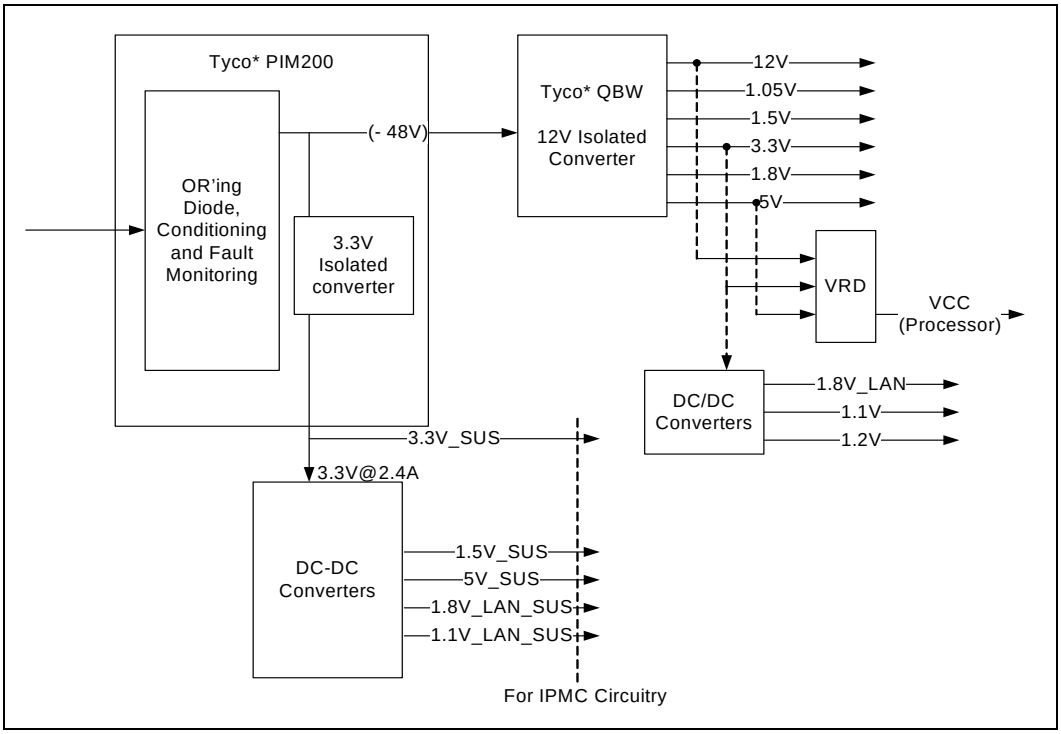
Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

2.2.8 On-board Power Supplies

The main power supply rails on the MPCBL0040 SBC are powered from dual-redundant -48 V power supply inputs from the backplane power connector (P10).

Figure 4 shows high-level power distribution on the SBC.

Figure 4. Power Conversion Diagram



2.2.8.1 Power Input Module

As required by the PICMG 3.0 specification, the MPCBL0040 SBC provides fuses on each of the -48 V power feeds and on the RTN connections. The fuses on the return feeds are critical to prevent over-current situations if an ORing diode in the return path fails and there is a voltage potential difference between the A and B return paths.

A Power Input Module (Tyco* PIM200 or equivalent) is used to interface directly to the chassis power feeds.

The main features of the PIM200 are as follows:

- Can support dual -48V inputs and provide 200W power output to the board
- Hot swap and inrush current limiting (per the PICMG 3.0 specification)
- Isolated Management Power Output, 8W of 3.3 VDC for IPMC circuitry
- ORing function for Feed A and B and their returns
- EMI filtering for conducted emissions
- 72 VDC charging current for external holdup storage capacitors to meet the holdup requirement in the PICMG 3.0 specification
- Feed A and B loss alarms

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

The input fusing from the AdvancedTCA backplane is not included on the module and is implemented on the baseboard. This is for ease of replacement and also to ensure that they are placed next to the Zone 1 connector. The other external components needed for this module are the holdup capacitors that are charged with 72 VDC created by the PIM module. In order to meet the 10 ms holdup time required by the PICMG 3.0 specification, capacitors of ~1900 µF are required. This translates to four 470 µF capacitors. Two parallel 5.1 KΩ resistors connect between the hold-up capacitor bank and AdvancedTCA power to ensure that they can be safely discharged below 60 VDC within 1 second to meet the safety requirements.

The output from this module is a single combined -48V output (48V_A and 48V_B are wire-ORed) that is filtered and used to drive the QBW power brick.

2.2.8.2 Tyco QBW 12 V Isolated Converter

The QBW power brick from Tyco performs the -48 V to 12 V isolation conversion. It is an Industry Standard Quarter Brick which is capable of delivering up to 18 A of output current with high efficiency.

2.2.8.3 IPMC Standby Power

The IPMC circuitry is powered by the sustaining voltages (5V_SUS, 3.3V_SUS, 1.5V_SUS, 1.8V_LAN_SUS, 1.1V_LAN_SUS), and is operational before power up of the rest of the components. In addition, the base interface 82571EB Ethernet controller is powered by 1.8V_LAN_SUS and 1.1V_LAN_SUS so that Serial over LAN functionality will work even if board payload power is not yet turned on.

2.2.8.4 3.3 V Isolated Converter

A 3.3 V management voltage is provided to the board. This voltage is used to generate the other required sustaining voltages. They are 5V_SUS and 1.5V_SUS for the ICH and 1.8V_LAN_SUS and 1.1V_LAN_SUS for the base interface Gigabit Ethernet controller. The sustaining voltages are always enabled and are used to power up the IPMC circuitry.

When the board is in the M1 state, no more than 10 W is drawn from the -48 V input (as specified in PICMG 3.0). All other outputs are enabled under IPMC control.

2.2.8.5 Processor Voltage Regulator Down (VRD)

The Voltage Regulator Down (VRD) provides power to the dual Dual-Core Intel® Xeon® processor LV 2.0 GHz processors. The input to the VRD is connected to the 5 V and 12 V power rails.

The VRD controller is designed to support the processor voltages selected by the voltage identification (VID) pins on the processor. The voltage regulator module is designed to support up to 27 A.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

2.2.9 Intelligent Platform Management Controller

The MPCBL0040 uses the Renesas* HD64F2166 processor, as the Intelligent Platform Management Controller (IPMC). The IPMC is a management subsystem providing monitoring, event logging, and recovery control. The IPMC serves as the gateway for management applications to access the platform hardware. Some of the key features are:

- Compliance with PICMG 3.0 and IPMI v2.0
- Automatic rollback capability if an operational image upgrade fails
- Upgradable from both IPMI interface (KCS and IPMB)
- Support for serial port redirection over LAN via IPMI Over LAN
- Supports the initiation of a graceful shutdown on the host CPU

The IPMC circuitry also utilizes an Altera* EP1C4 FPGA for glue-logic and to control the power-up and power-down sequencing of the on-board voltage regulators. It is powered by 3.3V_SUS and 1.5V_SUS and is clocked at 32.768 KHz. The FPGA controls resets, the enabling and monitoring of power good signals from all the on-board power converters and power sequencing to ensure that all of the converters power up in the correct order to prevent latch-up or damage to a device.

The FPGA is also used to extend the GPIO interconnects required by the IPMC, and to monitor the Port 80 POST codes during BIOS execution.

The National Semiconductor LM93 is used as of the IPMC subsystem to monitor on-board power supplies and processor thermal diodes.

2.2.10 128 MByte Flash Drive

The board has two128 MByte flash devices. Each flash device functions in a manner similar to an IDE hard drive. The user can utilize each of the 128 MByte flash drives to store anything that can be kept on a normal hard drive.

The flash device characteristics are:

- NAND technology, Single-Level Cells (SLC)
- Maximum number of program/erase cycles per erase block: 100,000
- Erase block size is 128 KBytes

In addition, the ATA controller has a wear leveling algorithm to improve the longevity of the flash device.

2.2.11 Real-Time Clock

The MPCBL0040 SBC real-time clock is integrated into the ICH. It is derived from a 32.768 kHz crystal.

The real-time clock is powered by a total capacitance of 0.47 F when main power is not applied to the board. This capacitor powers the real-time clock for a minimum of 2 hours while external power is removed from the MPCBL0040 SBC.

If the capacitor fully discharges, then the only affect this happens is that the RTC time will not be valid and will need to be reset the next time the board is inserted. The RTC clock is usually set using the Network Time Protocol once the operating system has loaded.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

2.2.12 Timers

The 6300ESB ICH provides three timers. The three timers are implemented as a single counter, each with its own comparator and value register. Each timer's counter increases monotonically. Each individual timer may generate an interrupt when the value in its value register matches the value in the main counter. Some of the timers may be enabled to generate a periodic interrupt.

The registers associated with these timers are mapped to a memory space (much like the I/O APIC). However, it is not implemented as a standard PCI function. The BIOS reports the location of the register space to the operating system. The hardware may support an assignable decode space; however, the BIOS sets this space prior to handing it over to the OS. It is not expected that the OS will move the location of these timers once it is set by the BIOS.

One timer block is implemented in the 6300ESB ICH. The timer block has one counter and three timers (comparators). Various capabilities registers indicate the number of timers and the capabilities of each.

2.2.12.1 Timer Accuracy

The timers are accurate over any 1 ms period to within 0.005% of the time specified in the timer resolution fields. Within any 100 ms period, the timer reports a time that is up to two ticks too early or too late. Each tick is less than or equal to 100 ns, so this represents an error of less than 0.2%. The timer is monotonic. It does not return the same value on two consecutive reads (unless the counter has rolled over and reached the same value). The main counter is clocked by the 14.31818 MHz clock, synchronized into the 66.666 MHz domain. This results in a non-uniform duty cycle on the synchronized clock, but does have the correct average period. The main counter is as accurate as the 14.3818 MHz clock.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

3.0 Operating the Unit

3.1 Ejector Handles

The MPCBL0040 SBC has two ejector handles to help insert and eject the board from a chassis.

To insert the board into the chassis, open the ejector handles and push the board into the chassis. Once the ejector handles slide into the top and bottom notches in the chassis, push both ejector handles toward the faceplate of the board until the handles click into place. The ejector handles provide a positive cam action, which ensures that the blade is properly seated. Once the bottom ejector handle is closed, the Hot Swap switch is engaged and this starts the normal power on sequence.

To eject the board from the chassis, slide the bottom ejector handle mechanism so it releases from the faceplate and then gently pull the bottom ejector handle away from the faceplate. When the lower ejector handle is disengaged from the faceplate, the Hot Swap switch is released and this starts the normal board shutdown process. This power down process is identified by the blinking blue hot swap LED. Once the hot swap LED turns solid blue, slide the top ejector handle mechanism so that it releases from the faceplate and use both ejector handles to disengage from the backplane.

See Section 5.10, “Hot Swap LED” on page 109 for detailed information on the function and operation of the hot swap LED.

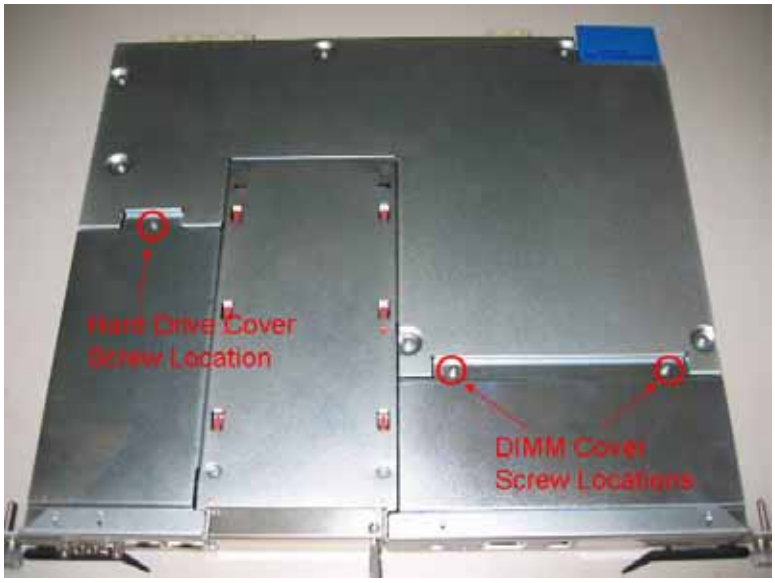
Warning: Removing the SBC before Hot Swap LED is solid blue can lead to device corruption or failure.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

3.2 Removing Hard Disk Drive and DIMM Covers

The top cover of the board has separate covers to allow easy access to the hard drive and DIMMs. The screw locations are show in Figure 5. These are captive screws, meaning that they do not need to be fully unscrewed to remove the hard drive and DIMM top covers.

Figure 5. Top Cover Screw Locations



The maximum torque for the hard drive cover, DIMM cover and all top cover screws is 4 in-lb (0.45 N-m).

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

3.3 Memory (DIMM) Installation

Install the DIMM modules as follows:

1. Unscrew the top metal cover where the DIMMs will be installed. Refer to Figure 5 for the location of the DIMM cover screws.
2. Open the DIMM ejector handles.
3. Install two DIMMs. DIMMs must be installed in matched pairs. DIMMs need to be identical in rank, size, device width and memory timing.
4. Re-attach the hard drive sheet metal cover. Torque top cover screws to 4 in-lb (0.45N-m) using a torque screwdriver.

Note: Memory is not included with the MPCBL0040 board and must be purchased separately. Refer to the MPCBL0040 Compatibility Report for a list of devices validated.

Caution: After the DIMM cover is removed, ensure that the DIMM ejector latches are closed. If they are left open and the board is installed in a chassis, there is a danger that the DIMM latches will be broken off when the board is extracted from the chassis. Figure 6 shows the latches left in the open (incorrect) position.

Figure 6. DIMM Latches Left in Open (Incorrect) Position



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

3.4 Serial Attached SCSI (SAS) Hard Drive Installation

Install the SAS hard drive as follows:

1. Check that the following accessories are available:
   - — Four M3x0.5 screws, 4mm long with captive external tooth lock washer (included in a plastic bag with every board)
   - — Four M3x0.5 screws, 6 mm long (installed on the board)
   - — HDD mounting bracket (installed on the board)
   - — SAS hard drive (not included with the MPCBL0040 board)

Note: If the plastic bag of screws used to mount the hard drive to the hard drive mounting bracket are misplaced or lost, this is the commercial description of the screws.

"COMMERCIAL DESCRIPTION: MACHINE SCREW, M3.0X0.5 THREADS, 4MM LONG, PAN HEAD, PHILLIPS DRIVE, CAPTIVE EXTERNAL TOOTH LOCKWASHER, STAINLESS STEEL, PASSIVATED. PART SHALL BE RoHS COMPLIANT."

2. Unscrew the top metal cover where the hard drive will be installed. Refer to Figure 5 for the locations of the hard drive cover and screw.
3. Remove the hard drive mounting bracket from the board.
4. Attach the hard drive to the mounting bracket with the 4mm screws and tighten to 4 in-lb (0.45 N-m) using a torque screwdriver. See Figure 7. The hard drive mounting bracket is not symmetrical so ensure the hard drive SAS edge connector will not be obstructed by the mounting bracket during installation.

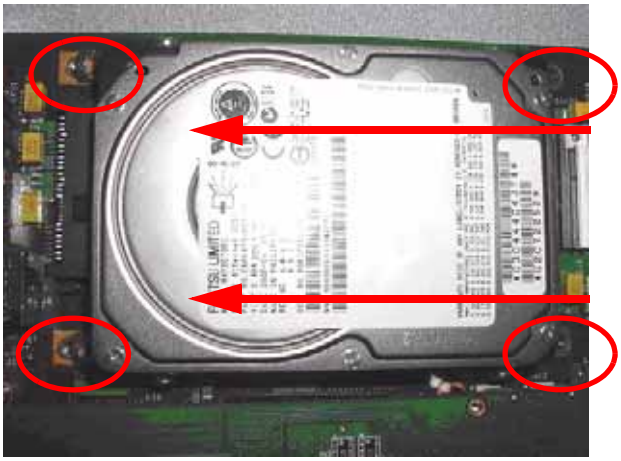
Figure 7. Attaching Hard Drive to HDD Mounting Cage



5. Place the drive/hard drive mounting bracket on the board. Align the hard drive connector with the on-board connector and slide the mounting cage from right to left to secure the connection as shown in Figure 8. Ensure care is taken when installing the drive so that no other components on the board are accidently damaged.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Figure 8. Attaching Hard Drive to On-board Connector



6. Align the screw holes on the mounting cage with the screw holes on the baseboard. Insert the 6 mm screws and tighten to 6 in-lb (0.68 N-m) using a torque screwdriver.
7. Re-attach the hard drive sheet metal cover. Torque top cover screws to 4 in-lb (0.45N-m) using a torque screwdriver.

Note: Hard drives are not included with the MPCBL0040 board and must be purchased separately. Refer to the MPCBL0040 Compatibility Report for a list of devices validated.

3.5 AdvancedMC Module Installation

Install the AdvancedMC module as follows:

1. Remove the AdvancedMC filler panel by pulling on the ejector handle until the module is removed.
2. Insert the AdvancedMC module into the slot and close the ejector handle by pushing it toward the faceplate of the board.

Note: AdvancedMC modules shall only be installed before board payload powers on or after the operating system has fully loaded. If an AdvancedMC module is hot added after the initial BIOS device discovery, but before the operating system is fully loaded, then the AdvancedMC module may not work properly. To correct this, a board payload reset or payload power cycle is required. For details on the amount of BIOS resources allocated for AdvancedMC module hot plug, please refer to Section 6.13, “Pre-Defined Resources for AdvancedMC Modules” on page 141.

Note: AdvancedMC modules are not included with the MPCBL0040 board and must be purchased separately. Refer to the MPCBL0040 Compatibility Report for a list of devices validated.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

3.6 Rear Transition Module (RTM) Installation

Install the Rear Transition module as follows:

1. Ensure the MPCBL0040 board is fully installed in the chassis and the front faceplate screws are tightened so that the board is firmly seated in the chassis.
2. Install the MPRTM0040 Rear Transition Module from the rear of the chassis.
3. Close the RTM ejector handles and tighten the RTM faceplate screws so the board is firmly seated in the chassis.

Note: The MPRTM0040 is not included with the MPCBL0040 board and must be purchased separately. Refer to the MPCBL0040 Compatibility Report for a list of devices validated.

3.7 BIOS Configuration

In most cases, the BIOS defaults provide the correct configuration for board use. However, a user that needs to make changes to the default BIOS settings can refer to Chapter 7.0, “BIOS Setup” for a complete description of the BIOS options.

3.8 Remote Access Configuration

Console redirection to the front panel serial port is enabled by default. This setting redirects the text output of the BIOS and operating system to the RJ-45 serial port on the MPCBL0040 faceplate. The default settings are 9600, N, 8, 1 with no flow control. Use these settings to access the console data.

3.9 Boot Devices

The BIOS Setup program includes a choice of available boot devices, with each boot device having options for removable media (USB CD-ROM, USB flash disk, etc.), SAS hard drive, on-board PATA flash drives, or PXE boot through any of the six GbE adapters.

In every POST, the BIOS detects all available boot devices and displays them on the boot order screen, with the exception of the Intel® Boot Agent (IBA), which displays even if the LAN cable is disconnected.

Refer to Section 7.5.3, “Boot Device Priority Submenu” on page 167 for detailed information on selecting boot devices.

3.9.1 Booting from a SAS Hard Disk

By default, if a SAS disk is installed, it will be the first boot device under the Boot menu priority list. The BIOS attempts to boot any OS image that is installed on the SAS hard disk.

Refer to Section 7.5.3, “Boot Device Priority Submenu” on page 167 for detailed information on selecting boot devices.

3.9.2 Booting from a PATA Flash (On-board)

By default, the PATA Flash are the second and third boot devices respectively in the Boot menu priority list.

Refer to Section 7.5.3, “Boot Device Priority Submenu” on page 167 for detailed information on selecting boot devices.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

3.9.3 Booting from a USB Device

The board can boot from a USB device that is plugged into the MPCBL0040 board or the MPRTM0040 RTM. The most common USB devices used for booting are USB hard drive, USB CD-ROM or USB flash disk.

If a USB device is attached to the board during boot up, the BIOS detects the device and it will appear in the boot device list on the BIOS Setup menu.

If the USB device is non-bootable, the BIOS attempts to boot from the next boot device as configured in the Boot Device Priority list.

Note: For information on how to create a bootable USB flash disk, search the web for “create bootable usb flash”. There are multiple web sites that have information on how to do this.

Refer to Section 7.5.3, “Boot Device Priority Submenu” on page 167 for detailed information on selecting boot devices.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

3.9.4 Booting from a LAN (PXE Boot)

Any of the six on-board Gigabit Ethernet LAN adapters on the base and fabric interfaces can be used for the remote boot process. It is necessary to set up a PXE boot server on which to store the Linux* image. (Details on how to set up a PXE boot server are beyond the scope of this document.) Remember to configure the boot device priority in the BIOS Setup to specify the Gigabit Ethernet LAN adapter(s) as the top priority.

An Ethernet switch must be installed in your AdvancedTCA* chassis in order to boot from LAN.

It is possible to PXE boot from AdvancedMC modules, but the AdvancedMC module installed into the MPCBL0040 must support the PXE boot agent.

Refer to Section 7.5.3, “Boot Device Priority Submenu” on page 167 for detailed information on selecting boot devices.

For a block diagram view, see Figure 3, “Gigabit Ethernet Interface Block Diagram” on page 21.

Table 5. Ethernet Port Mapping

BIOS IBA PXE Boot Port	Identification on MPCBL0040 Faceplate	Operating System Port	MAC Address	PCI Express Port Connection to Memory Controller Hub (MCH)	PICMG 3.0 Port Definition
0200*	Port A	eth4	xxxxxxxxxxN	B1	Base Interface; Port 0, Channel 1
0201*	Port B	eth5	xxxxxxxxxx (N+1)	B1	Base Interface; Port 0, Channel 2
0300*	Port C	eth0	xxxxxxxxxx (N+2)	A0	Fabric Interface; Port 0, Channel 1 (Ports C and D can be jointly selected to connect to the backplane from the on-board Ethernet controller or GbE ports from the AdvancedMC slot)
0301*	Port E	eth2	xxxxxxxxxx (N+4)	A1	Fabric Interface; Port 1, Channel 1 (Ports E and F can be jointly selected to connect to backplane or front panel RJ45.)
0400*	Port D	eth1	xxxxxxxxxx (N+3)	A0	Fabric Interface; Port 0, Channel 2 (Ports C and D can be jointly selected to connect to the backplane from the on-board Ethernet controller or GbE ports from the AdvancedMC slot)
0401*	Port F	eth3	xxxxxxxxxx (N+5)	A1	Fabric Interface; Port 1, Channel 2 (Ports E and F can be jointly selected to connect to backplane or front panel RJ45.)

* Slot xxyy refers to:

- xx = PCI bus number, for example 02 means bus 2.
- yy = Bits 7-3 is the PCI device number; bits 2-0 is the PCI function number. For example, 00 means device 0, function 0; 01 means device 0, function 1 etc.

Note: For the Ethernet operating system port, this is the default unless the default parameters are changed. For example, pci=xxx boot parameter.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

3.10 Digital Ground to Chassis Ground Connectivity

Digital ground is tied to chassis ground through a screw that threads into a standoff in the metal backing plate. The PCB hole for this screw is non-plated, and is surrounded by a large gold plated copper pad on the PCB top side and a copper-free area on the PCB bottom side. The large copper pad is tied to logic ground by several vias around its perimeter. The screw head bears on the copper pad and threads into the backside plate to make the connection. A plastic shoulder washer is used under the screw head to keep the grounds isolated. Boards ship standard with this washer in place. If it is necessary to short the grounds for regulatory reasons, remove the washer and reinstall the screw.

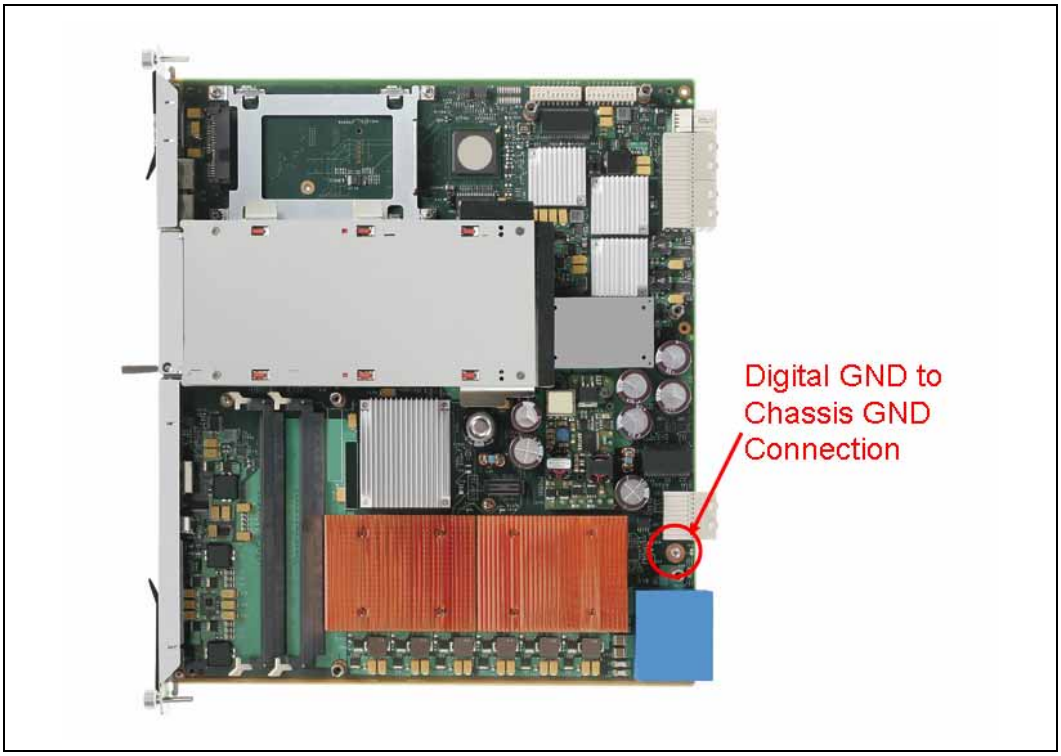
Note: For the MPCBL0040, the default is that digital ground is isolated from chassis ground.

To connect the digital ground to the chassis ground, follow this procedure:

1. Remove the top metal cover from the board. The hard drive and DIMM covers do not need to be removed separately. It is OK to remove the entire top cover with the hard drive and DIMM covers still in place.
2. Remove the screw with the plastic shoulder washer. See Figure 9 for the screw location above the P10 blue connector.
3. Remove the plastic insulating washer to connect digital ground to chassis ground.
4. Store the plastic insulation washer in a safe place. It may be needed to isolate the digital ground from chassis ground in the future.
5. Reinstall the screw and tighten to 4 in-lb (0.45N-m) using a torque screwdriver.
6. Re-install the top metal cover to the board.

Note: Digital ground is also called logic ground. Chassis ground is also known as shelf ground.

Figure 9. Digital Ground to Chassis Ground Screw Location



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

3.11 Identifying MPCBL0040 Ethernet MAC Addresses

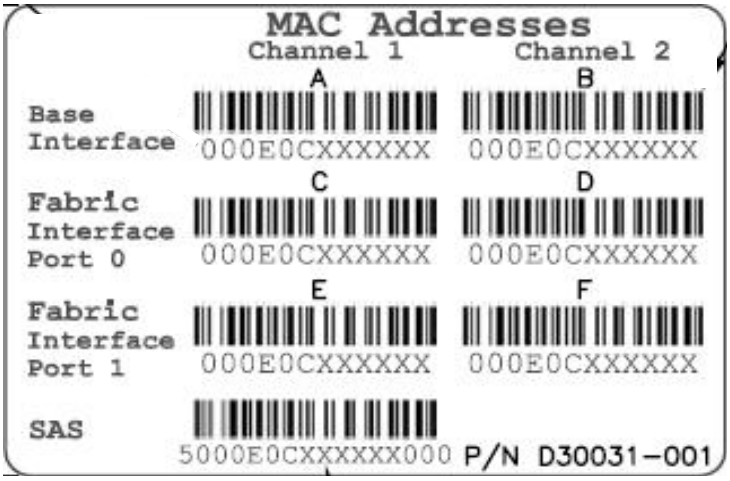
On the backing plate of the MPCBL0040, there is a MAC address label to assist a user in determining the MAC address of each Ethernet port on the SBC. The MAC address may be needed for PXE boot configuration, configuring Serial Over LAN (SOL) and for OS configuration.

Figure 10 shows the location of the MAC address label on the MPCBL0040 backing plate. Table 5, "Ethernet Port Mapping" on page 36 breaks down the mapping of the Ethernet interfaces to the labeling on the MPCBL0040 faceplate and in the operating system.

The first MAC address (Port A) can be retrieved remotely by using IPMI command. From that first MAC address (port A), each port increments by 0x01h.

In the IPMI specification (23.2), parameter #5 (MAC address) of the Get LAN Configuration Parameters Command will be populated automatically with the base interface MAC address. Alternatively, using `ipmitool` from the payload processor, the command is: `ipmitool lan print 1`

Figure 10. MAC Address Label on MPCBL0040 Board



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

3.12 Cable Information

For the front panel ports, here are details on the cables that need to be used with the board:

Table 6. Cable Information

Type	Cable Description	Max Length
SAS Port	4X external SAS cable	7m
Ethernet Port	For intra-building (same building): Unshielded Category 5e cable For inter-building (building to building): Shielded Etherent cable and both ends of the shield must be grounded. Shielded Ethernet cable is required to pass NEBS testing.	100m
Serial Port	Unshielded Category 5e cable with DB-9 to RJ45 converter	8m
USB Port	External USB cable	5m

Note: The SAS cable should be the Molex* 74527-3008 or equivalent.
See http://www.molex.com/cgi-bin/bv/molex/home_init.jsp.

The mating end of the SAS connector should be an SFF-8470 connector (or equivalent).
See http://www.cs-electronics.com/sas-cables.htm.

3.13 Firmware Updates

The major components that need updates are the BIOS and IPMC firmware. See Chapter 10.0, “Firmware Update Utilities” for more information on firmware updates.

3.14 Operating System Install Tips

When installed certain operating systems on the MPCBL0040 board, such as Red Hat*, it is recommended the user disable the 128MB flash memory devices in BIOS before doing the OS install.

If the 128MB flash devices are not disabled, by default the OS installs the bootloader on the flash drives and the kernel on the hard disk drive. Next time, the board boots, the boot loader will hang because it is expecting the kernel to be on the same drive as the bootloader.

To disable the onboard 128MB flash drives:

1. Reboot board, go into BIOS
2. Choose Advanced
3. Choose IDE Configuration
4. Change setting from “P-ATA Only” to “Disabled”.
5. Press Esc
6. Choose Exit
7. Choose Save Changes and Exit

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

4.0 Connectors and LEDs

4.1 Backplane and Front Panel Connectors

Connectors along the rear edge of AdvancedTCA* server blades are divided into three distinct zones, as described in Section 2.3 of the PICMG 3.0 Specification:

- Zone 1 for system management and power distribution. (P10)
- Zone 2 for data fabric (J23)
- Zone 3 for the rear transition module (RTM) (J30, J31, J32)

Figure 11 shows the locations of the backplane and on-board connectors and Table 7 explains the function of each connector.

Figure 11. Backplane and On-board Connector / DIP Switch Locations

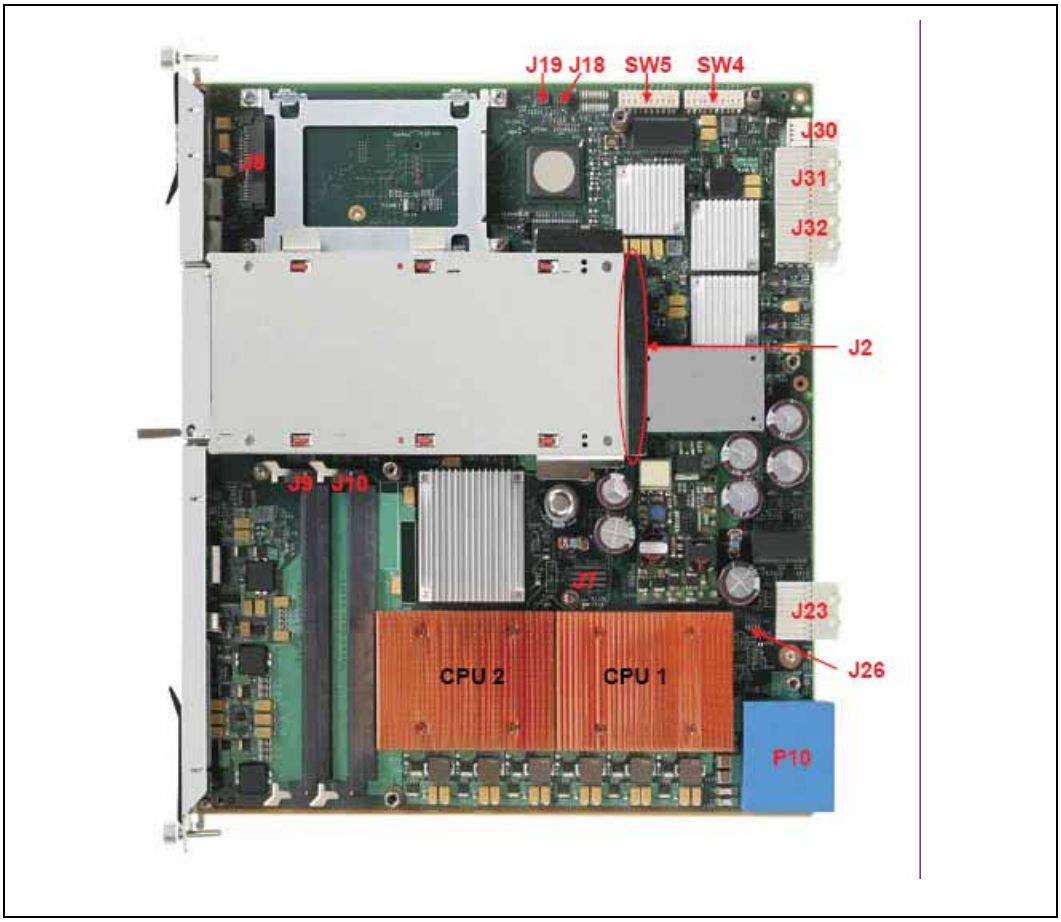


Table 7. Backplane and On-board Connector Assignments

Connector	Description
CPU 1	Processor #1 (CPU 1 is not a connector)
CPU 2	Processor #2 (CPU 2 is not a connector)
J2	AdvancedMC* connector
J7	ITP700 connector
J8	Serial attached SCSI (SAS) hard disk connector
J9	DIMM 2
J10	DIMM 1
J18	JTAG header 2 (for RadiSys manufacturing test purposes only)
J19	JTAG header 1 (for RadiSys manufacturing test purposes only)
J23	AdvancedTCA data transport for Base and Fabric interfaces (Zone 2)
J26	ITP JTAG header
J30	RTM power (Zone 3)
J31	RTM Data and Control connector (Zone 3)
J32	RTM Data and Control connector (Zone 3)
P10	AdvancedTCA power and IPMB
SW4	DIP switches - for manufacturing and debug by RadiSys. Refer to Table 14 for details.
SW5	DIP switches - for customer use. Refer to Table 15 for details.

Figure 12 shows the locations of the front panel connectors on the board and Table 8 describes the function of each front panel connector.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

4.2 Front Panel Connectors

Figure 12. Front Panel Connectors

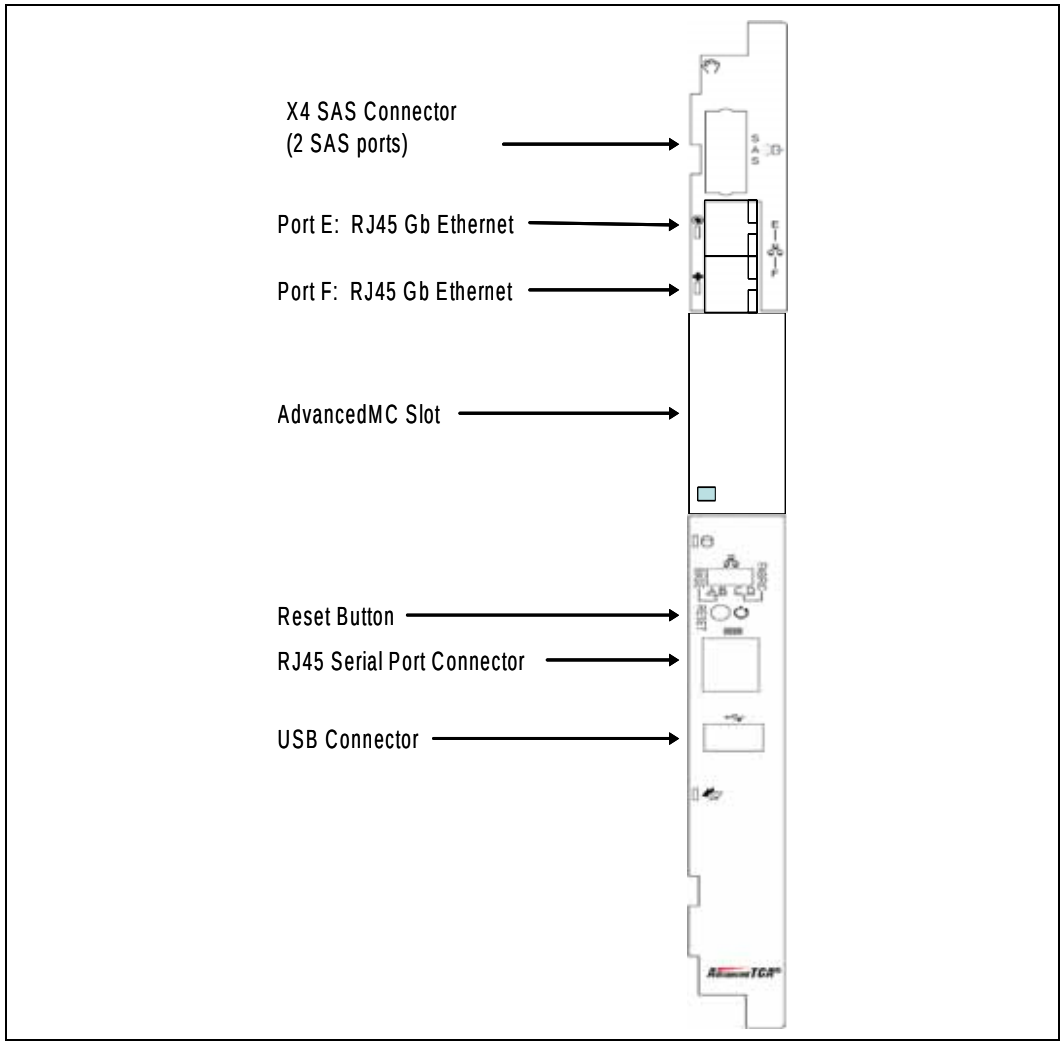


Table 8. Front Panel Connector Assignments

Connector	Description
J3	USB Connector
J4	Serial Port Connector
J34, J36	RJ-45 10/100/1000Mbps Ethernet Connectors
J8	SAS Connector

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

4.2.1 USB Connector (J3)

The MPCBL0040 SBC has one USB connector, J3, that supports USB 2.0 and USB 1.1. This connector is available at the front panel. Figure 13 shows the connector and Table 9 gives the pin assignments.

Figure 13. USB Connector (J3)

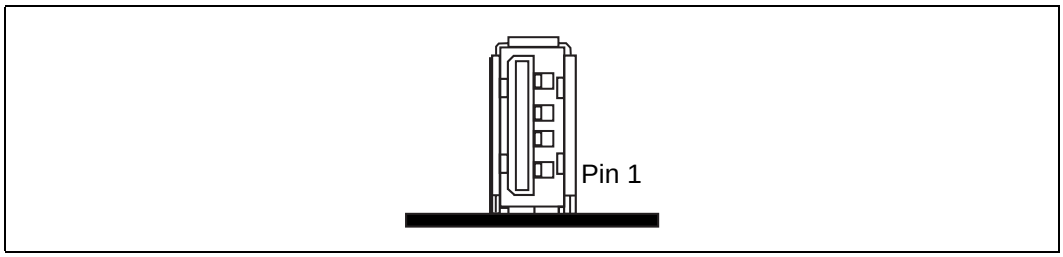


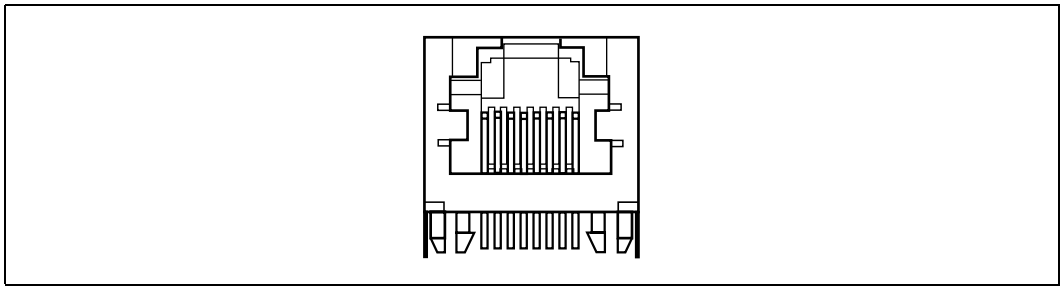
Table 9. USB Connector (J3) Pin Assignments

Pin	Signal
1	+5 V
2	-DATA
3	+DATA
4	GND

4.2.2 Serial Port Connector (J4)

A single serial port interface is provided on the front edge of the card using an RJ-45 style shielded connector. The connector is an 8-pin RJ-45. Figure 14 shows the connector and Table 10 gives the pin assignments. Figure 15 shows the RJ-45 to DB-9 translation.

Figure 14. Serial Port Connector (J4)

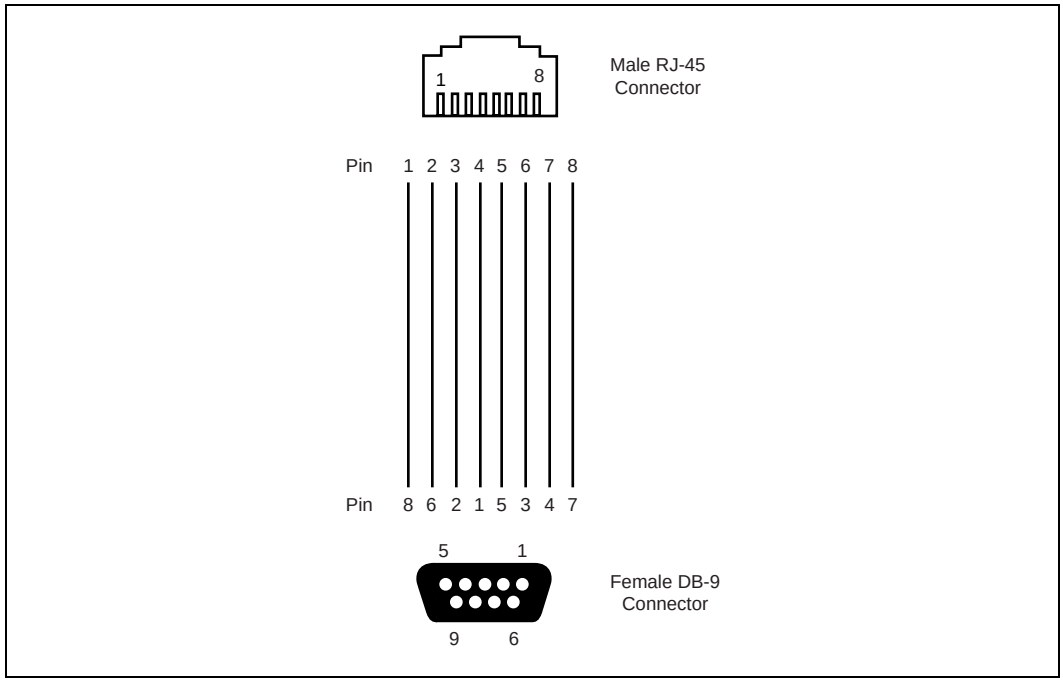


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 10. Serial Port Connector (J4) Pin Assignments

Pin	Signal
1	RTS
2	DTR
3	TXD
4	GND
5	GND
6	RXD
7	DSR
8	CTS

Figure 15. DB-9 to RJ-45 Pin Translation



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

4.2.3 Ethernet 10/100/1000 Connectors (J34, J36)

Two Ethernet ports are provided on the front edge of the board using an RJ-45 style shielded connector (Tyco* RJ714-CL2). Figure 16 shows the connector and Table 11 gives the pin assignments.

Figure 16. Gigabit Ethernet Connector

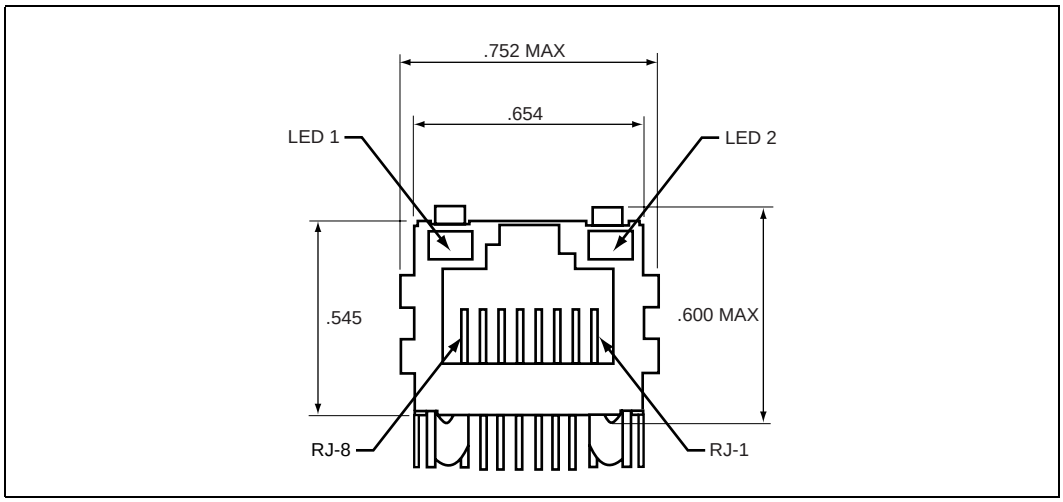


Table 11. Gigabit Ethernet Connector Pin Assignments

Pin	Signal Name	Comments
1	BI_DA+	Bi-directional lane 1, positive polarity
2	BI_DA-	Bi-directional lane 1, negative polarity
3	BI_DB+	Bi-directional lane 2, positive polarity
4	BI_DC+	Bi-directional lane 3, positive polarity
5	BI_DC-	Bi-directional lane 3, negative polarity
6	BI_DB-	Bi-directional lane 2, negative polarity
7	BI_DD+	Bi-directional lane 4, positive polarity
8	BI_DD-	Bi-directional lane 4, negative polarity

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

4.2.4 Front Panel SAS Connector (J8)

Table 12 shows the pinout definition for the front panel SAS connector. There are two SAS ports available from the front panel connector.

Table 12. Front Panel SAS Connector Pin Assignments

Pin	Signal	Pin	Signal
1	GND	14	No Connect
2	SAS_RX2_P	15	No Connect
3	SAS_RX2_N	16	GND
4	GND	17	No Connect
5	SAS_RX3_P	18	No Connect
6	SAS_RX3_N	19	GND
7	GND	20	SAS_TX3_N
8	No Connect	21	SAS_TX3_P
9	No Connect	22	GND
10	GND	23	SAS_TX2_N
11	No Connect	24	SAS_TX2_P
12	No Connect	25	GND
13	GND		

4.2.5 Front Panel Reset Button

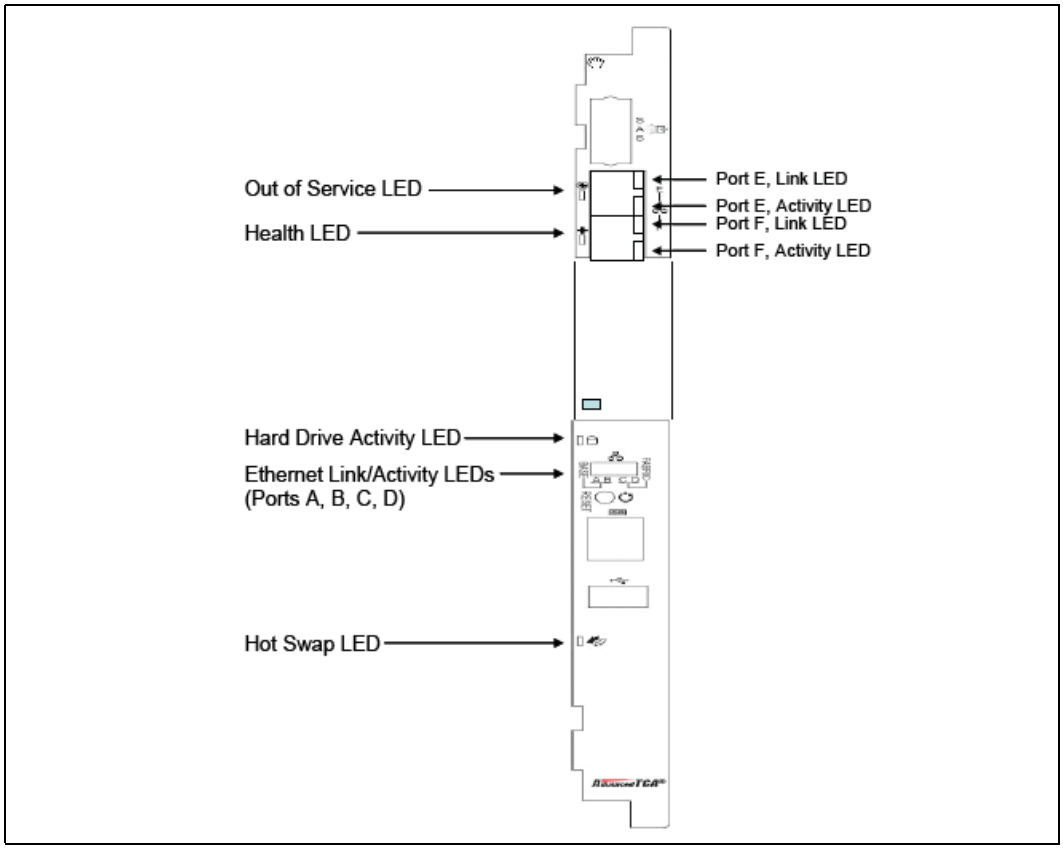
The reset button is located in a small recessed hole below the base and fabric interface LEDs. The reset button is an input to the IPMC to request a payload soft reset. There are IPMI commands to reset the board and change power states through the software. The reset button can only be used when a user is physically present at the chassis to reset the board. The reset button is available at the front panel, as shown in Figure 12 on page 43.

4.2.6 Front Panel LEDs

The MPCBL0040 SBC provides several LEDs to indicate status as shown in Figure 17.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Figure 17. Front Panel LEDs



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

When these LEDs are lit, they indicate a status as defined in the Table 13.

Table 13. Front Panel LED Descriptions (Sheet 1 of 2)

LED	Function
Hot Swap 	**Function:** Hot Swap as defined in the AdvancedTCA 3.0 specification It is also possible for a user to override the default behavior of the LED using AdvancedTCA FRU LED Control commands. **Possible States:** OFF / BLUE / SHORT BLINK / LONG BLINK
Out of Service 	**Function:** Out of Service (AdvancedTCA LED 1) RED: The board is out of service. OFF: The board is running. AMBER-SOLID: The Health LED and Out of Service LED both are solid amber when the IPMC boot block is in update mode. It is possible for a user to override the default IPMC behavior of the LED using AdvancedTCA FRU LED Control commands. **Possible States:** OFF / RED / AMBER
Health 	**Function:** Health (AdvancedTCA LED 2). The SBC health is based on an aggregation of IPMI sensors, like board temperature and voltage. GREEN: The SBC is healthy. RED: The SBC is not healthy. Critical thresholds on voltage rails or temperature have been exceeded or critical event assertion turns LED to red. AMBER-SOLID: The Health LED and Out of Service LED both are solid amber when the IPMC boot block is in update mode. It is possible for the user to override the default IPMC behavior of the LED using AdvancedTCA FRU LED Control commands. **Possible States:** OFF / GREEN / RED / AMBER
Ports A, B, C, D Link/Activity	There is one LED that indicates link and activity for the following ports: • A: Base Interface: Port 0, Channel 1 • B: Base Interface: Port 0, Channel 2 • C: Fabric Interface, Port 0, Channel 1 • D: Fabric Interface, Port 0, Channel 2 **Function:** Gigabit Ethernet Base/Fabric Interface Link and Activity OFF: No Link GREEN: Link GREEN-BLINK: Link and Activity
Ports E & F **Link Speed** 	There is one LED that indicates link speed for the following ports: • E: Fabric Interface: Port 1, Channel 1 • F: Fabric Interface: Port 1, Channel 2 **Function:** Gigabit Ethernet Fabric Interface Link Speed OFF: 10 Mb/s GREEN: 100 Mb/s AMBER: 1000 Mb/s Note: This LED will be active even if Ethernet port is connected to the backplane fabric interface.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

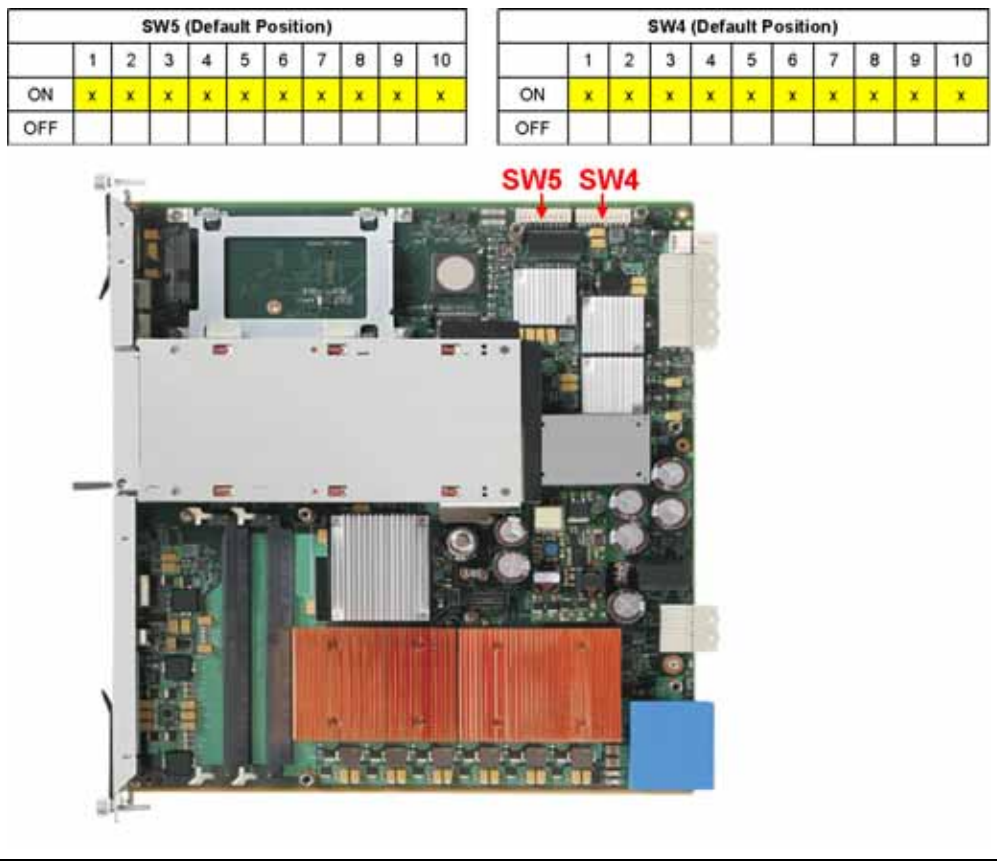
Table 13. Front Panel LED Descriptions (Sheet 2 of 2)

LED	Function
Ports E & F Activity 	There is one LED that indicates activity for the following ports: • E: Fabric Interface: Port 1, Channel 1 • F: Fabric Interface: Port 1, Channel 2 **Function:** Gigabit Ethernet Fabric Interface Link Activity: GREEN-NO BLINKING: No traffic GREEN-BLINKING: Transmit or receive traffic is coming across the link Note: This LED will be active even if Ethernet port is connected to the backplane fabric interface.
Hard Drive Activity 	**Function:** Hard Drive Activity OFF: Normal/No disk access BLINKING GREEN: Disk access (read/write activity)

4.3 DIP Switches

The MPCBL0040 contains a number of DIP switches that allow the user to configure certain options not configurable through the BIOS Setup utility. These DIP switches are used for diagnostic purposes. Users should take precautions when changing these switches. See Figure 18 for the locations of the DIP switches. Table 14 describes the functions of SW4 switches and Table 15 describes the functions of SW5 switches.

Figure 18. DIP Switch Locations



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 14. SW4 IPMI Dip Switches

Switch	Signal Name	Function	Description (Default setting = On)
1	DIAG<2>	BIOS setting (BIOS reads over LPC bus)	Off = Used internally for manufacturing On = Normal operation
2	DIAG<1>	BIOS setting (BIOS reads over LPC bus)	Off = Used internally for manufacturing On = Normal operation
3	DIAG<0>	BIOS setting (BIOS reads over LPC bus)	Off = Used internally for manufacturing On = Normal operation
4	SW_BOOT_N	IPMC Boot Mode	Off = IPMC User Program Mode On = Normal IPMC Boot Mode
5	SW_RST_2166	IPMC reset	Off = Reset the IPMC On = Normal Operation
6	SW_PWRBTN	ICH's power button sleep mode	Off = Force sleep-mode On = Normal Operation
7	SW_FRB_DIS	Fault Resilient Booting	Off = Disable Fault Resilient Booting (BIOS) On = Enable Fault Resilient Booting (BIOS)
8	SW_IPMC_FWE	Write protect IPMC internal flash	Off = Reserved. The setting must not be used. On = Disable write protect of Renesas IPMC internal flash
9	SW_SEL_ICH_IPMC	UART0 (COM1) data routing	Off = IPMC serial port directed to the front-panel serial-port. This is used during IPMC boot block update or IPMC debug. On = Normal operation, ICH serial port directed to front panel serial-port
10	SW_FORCE_PWR_ON	Force power on	Off = Reset IPMC and turn payload power on On = Normal operation

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 15. SW5 IPMI Dip Switches

Switch	Signal Name	Function	Description (Default setting = ON)
1	CLR_PASSWD_N	Clear BIOS password	Off = Clears password to enter BIOS setup menu On = If BIOS password is set, user is required to enter password prior to entering BIOS setup menu
2	CLR_CMOS_N	Clear BIOS CMOS settings	Off = OFF clears all CMOS settings configured by the user. CMOS is reset to factory default settings. On = Normal operation
3	MANF_N	Manufacturing Mode	Off = Manufacturing test mode. BIOS will not boot. Serial port (UART) is set to 115,200. A SEL entry is logged that won't get cleared until board is power cycled On = Normal operation
4	SW_PS_N	Power board without IPMC or shelf manger/ CMM	Off = Power up board without shelf manager interaction On = Normal operation
5	SW_IPMC_WP_N	Write protect IPMC external flash	Off = Disable the IPMC's external flash write-protect On = Provides write-protection of flash memory blocks if IPMC software first "locks down" the desired blocks (by default none of the blocks are locked down after power-on). Note that the IPMC firmware can override this switch setting.
6	SW_FWH_1_IDSEL	BIOS boot device (FWH0 or FWH1) selection	Off = BIOS boots from FWH1 On = Under a normal good scenario, the BIOS boots from FWH0. If BIOS FWH0 is corrupted, it automatically boots from FWH1.
7	RESERVED	RESERVED	Off =Reserved. On = Normal operation.
8	SW_FRC_UPD	Force IPMC into Firmware Update Mode	Off = Force the IPMC into Firmware Update for user image On = Normal operation
9	SW_SSPM_DISB_N	IPMC boot image update mode	Off = Disable IPMC's NMI input, force the IPMC into boot image update mode On = Normal operation
10	SW_BS_ITP_N	Select ITP mode	Off = ITP mode enabled On = Boundary scan mode enabled for ITP chain

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

4.4 On-Board Connectors

4.4.1 AdvancedMC Connector (J2)

Refer to Table 4, “AdvancedMC Connections” on page 23 for a high-level overview of the AdvancedMC port mapping.

- PCI Express Ref clock connects to CLK3

Pin assignments are shown in Table 16. Signals used by the MPCBL0040 board AdvancedMC connector are highlighted in **bold**.

Table 16. AdvancedMC Slot B2 Connector: J2 Pinout (Sheet 1 of 3)

Pin #	Signal Name	Pin #	Signal Name
B85	**GND**	B86	**GND**
B84	**MB_PWR (12V)**	B87	MB_Tx8-
B83	**MB_PS0#**	B88	MB_Tx8+
B82	**GND**	B89	**GND**
B81	**MB_CLK3-**	B90	MB_Rx8-
B80	**MB_CLK3+**	B91	MB_Rx8+
B79	**GND**	B92	**GND**
B78	MB_CLK2-	B93	MB_Tx9-
B77	MB_CLK2+	B94	MB_Tx9+
B76	**GND**	B95	**GND**
B75	MB_CLK1-	B96	MB_Rx9-
B74	MB_CLK1+	B97	MB_Rx9+
B73	**GND**	B98	**GND**
B72	**MB_PWR**	B99	MB_Tx10-
B71	**MB_SDA_L**	B100	MB_Tx10+
B70	**GND**	B101	**GND**
B69	**MB_Tx7-**	B102	MB_Rx10-
B68	**MB_Tx7+**	B103	MB_Rx10+
B67	**GND**	B104	**GND**
B66	**MB_Rx7-**	B105	MB_Tx11-
B65	**MB_Rx7+**	B106	MB_Tx11+
B64	**GND**	B107	**GND**
B63	**MB_Tx6-**	B108	MB_Rx11-
B62	**MB_Tx6+**	B109	MB_Rx11+
B61	**GND**	B110	**GND**
B60	**MB_Rx6-**	B111	**MB_Tx12-**
B59	**MB_Rx6+**	B112	**MB_Tx12+**
B58	**GND**	B113	**GND**
B57	**MB_PWR**	B114	**MB_Rx12-**
B56	**MB_SCL_L**	B115	**MB_Rx12+**
B55	**GND**	B116	**GND**
B54	**MB_Tx5-**	B117	**MB_Tx13-**

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 16. AdvancedMC Slot B2 Connector: J2 Pinout (Sheet 2 of 3)

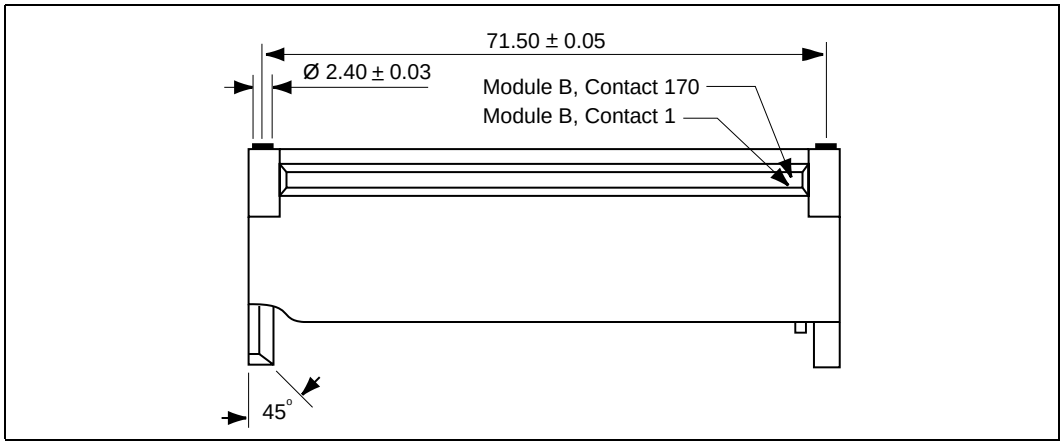
Pin #	Signal Name	Pin #	Signal Name
B53	**MB_Tx5+**	B118	**MB_Tx13+**
B52	**GND**	B119	**GND**
B51	**MB_Rx5-**	B120	**MB_Rx13-**
B50	**MB_Rx5+**	B121	**MB_Rx13+**
B49	**GND**	B122	**GND**
B48	**MB_Tx4-**	B123	**MB_Tx14-**
B47	**MB_Tx4+**	B124	**MB_Tx14+**
B46	**GND**	B125	**GND**
B45	**MB_Rx4-**	B126	**MB_Rx14-**
B44	**MB_Rx4+**	B127	**MB_Rx14+**
B43	**GND**	B128	**GND**
B42	**MB_PWR**	B129	**MB_Tx15-**
B41	**MB_ENABLE#**	B130	**MB_Tx15+**
B40	**GND**	B131	**GND**
B39	MB_Tx3-	B132	**MB_Rx15-**
B38	MB_Tx3+	B133	**MB_Rx15+**
B37	**GND**	B134	**GND**
B36	MB_Rx3-	B135	**MB_Tx16-**
B35	MB_Rx3+	B136	**MB_Tx16+**
B34	**GND**	B137	**GND**
B33	**MB_Tx2-**	B138	**MB_Rx16-**
B32	**MB_Tx2+**	B139	**MB_Rx16+**
B31	**GND**	B140	**GND**
B30	**MB_Rx2-**	B141	**MB_Tx17-**
B29	**MB_Rx2+**	B142	**MB_Tx17+**
B28	**GND**	B143	**GND**
B27	**MB_PWR**	B144	**MB_Rx17-**
B26	**MB_GA2**	B145	**MB_Rx17+**
B25	**GND**	B146	**GND**
B24	**MB_Tx1-**	B147	**MB_Tx18-**
B23	**MB_Tx1+**	B148	**MB_Tx18+**
B22	**GND**	B149	**GND**
B21	**MB_Rx1-**	B150	**MB_Rx18-**
B20	**MB_Rx1+**	B151	**MB_Rx18+**
B19	**GND**	B152	**GND**
B18	**MB_PWR**	B153	**MB_Tx19-**
B17	**MB_GA1**	B154	**MB_Tx19+**
B16	**GND**	B155	**GND**
B15	**MB_Tx0-**	B156	**MB_Rx19-**
B14	**MB_Tx0+**	B157	**MB_Rx19+**

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 16. AdvancedMC Slot B2 Connector: J2 Pinout (Sheet 3 of 3)

Pin #	Signal Name	Pin #	Signal Name
B13	**GND**	B158	**GND**
B12	**MB_Rx0-**	B159	**MB_Tx20-**
B11	**MB_Rx0+**	B160	**MB_Tx20+**
B10	**GND**	B161	**GND**
B9	**MB_PWR**	B162	**MB_Rx20-**
B8	MB_ETH100Tx	B163	**MB_Rx20+**
B7	**GND**	B164	**GND**
B6	MB_ETH100Rx	B165	**MB_TCLK**
B5	**MB_GA0**	B166	**MB_TMS**
B4	**MB_MP (3.3V)**	B167	**MB_TRST#**
B3	**MB_PS1#**	B168	**MB_TDO**
B2	**MB_PWR (12V)**	B169	**MB_TDI**
B1	**GND**	B170	**GND**

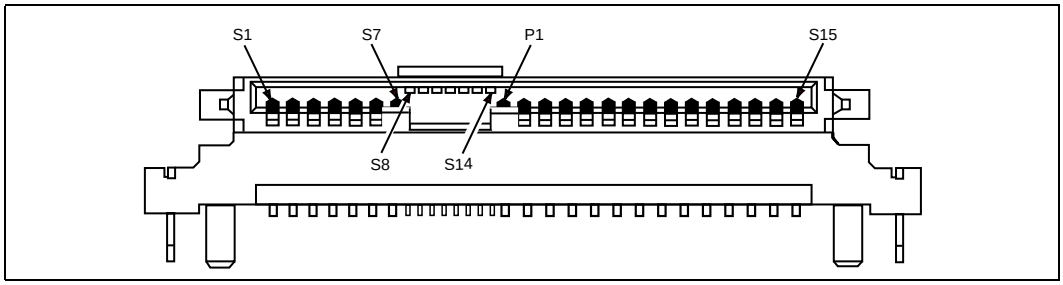
Figure 19. AdvancedMC Connector



4.4.2 Serial Attached SCSI (SAS) Connector (J8)

Figure 20 shows the SAS connector used on the MPCBL0040 board. Table 9 gives pinout information.

Figure 20. On-Board SAS Connector



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 17. On-Board SAS Connector Pinout

Segment	Pin	Name
Primary signal	S1	GROUND
	S2	RP+
	S3	RP-
	S4	GROUND
	S5	TP-
	S6	TP+
	S7	GROUND
Secondary signal [a]	S8	GROUND
	S9	No Connect
	S10	No Connect
	S11	GROUND
	S12	No Connect
	S13	No Connect
	S14	GROUND
Power [b]	P1	V_{33}
	P2	V_{33}
	P3	V_{33}, precharge
	P4	GROUND
	P5	GROUND
	P6	GROUND
	P7	V_5, precharge
	P8	V_5
	P9	V_5
	P10	GROUND
	P11	READY LED
	P12	GROUND
	P13	V_{12}, precharge
	P14	V_{12}
	P15	V_{12}

Notes:

a. S8 through S14 are no-connects on single-port implementations.

b. Behind an SAS plug connector, the precharge pin and each corresponding voltage pin are connected together on the SAS target device (e.g., the V_5, precharge pin, P7, is connected to the two V_5 pins, P8 and P9).

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

4.4.3 Extended ITP700 Debug Port Connector (J7)

The ITP connector allows connection of a tool that helps you observe and control the step-by-step execution of your program for debugging hardware and software. Debugging includes finding a hardware or software error and identifying the location and cause of the error so it can be corrected.

RadiSys continually looks for ways to maximize the development and delivery of mission-critical tools to our internal validation teams and strategic OEM customers. As a result, RadiSys has put together a third-party vendor program team which works with third-party vendors to develop and deliver specific tools formerly supplied by RadiSys to internal and external customers.

RadiSys recommends selecting the vendor of your choice to provide in-circuit emulation hardware and software. One such vendor is listed below:

- American Arium* currently develops in-circuit emulation and run control tools for Intel processors for use by RadiSys BIOS and driver teams, RadiSys manufacturing, and OEM customers.

See http://www.arium.com/ for more information.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

4.5 Backplane Connectors

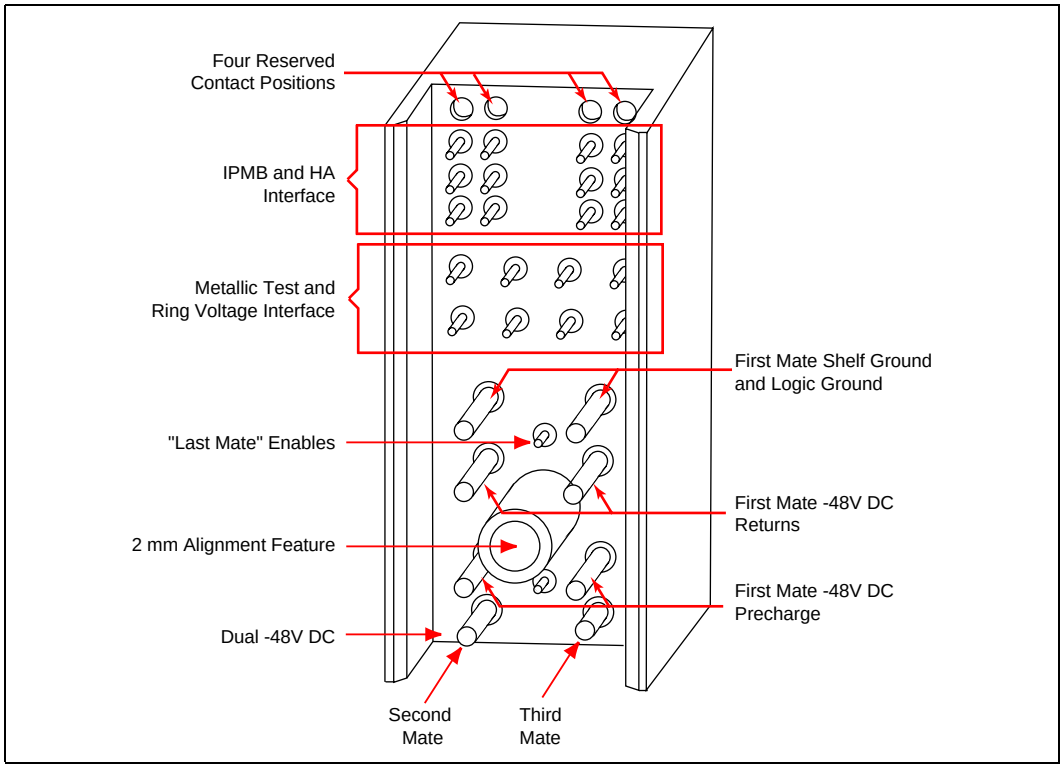
4.5.1 Power Distribution Connector (P10)

Zone 1 consists of P10, a 34-pin Positronic* header connector that provides the following signals:

- Two -48 VDC power feeds (four signals each; eight signals total)
- Two IPMB ports (two signals each, four signals total)
- Geographic address (eight signals)
- Two ground pins
- 12 unused (but physically present) pins

Figure 21 shows the mechanical drawing of the connector. The pin assignments are given in Table 18.

Figure 21. Power Distribution Connector (Zone 1) P10



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 18. Power Distribution Connector (Zone 1) P10 Pin Assignments

Pin	Signal	Description
1	Reserved	No Connect
2	Reserved	No Connect
3	Reserved	No Connect
4	Reserved	No Connect
5	GA0	Geographic Addr Bit 0
6	GA1	Geographic Addr Bit 1
7	GA2	Geographic Addr Bit 2
8	GA3	Geographic Addr Bit 3
9	GA4	Geographic Addr Bit 4
10	GA5	Geographic Addr Bit 5
11	GA6	Geographic Addr Bit 6
12	GA7/P	Geo Adr Bit 7 (Odd Parity)
13	IPMB_CLK_A	IPMB Bus A Clock
14	IPMB_DAT_A	IPMB Bus A Data
15	IPMB_CLK_B	IPMB Bus B Clock
16	IPMB_DAT_B	IPMB Bus B Data
17	Unused	No Connect
18	Unused	No Connect
19	Unused	No Connect
20	Unused	No Connect
21	Unused	No Connect
22	Unused	No Connect
23	Unused	No Connect
24	Unused	No Connect
25	EMI_GND	EMI Chassis Ground
26	LOGIC_GND	Gnd Ref for Card Logic
27	ENABLE_B	Enb DC-DC conv, B Feed
28	VRTN_A	-48 V Return, Feed A
29	VRTN_B	-48 V Return, Feed B
30	-48V_EARLY_A	No Connect
31	-48V_EARLY_B	No Connect
32	ENABLE_A	Enb DC-DC conv, A Feed
33	-48V_A	-48 V Input, Feed A
34	-48V_B	-48 V Input, Feed B

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

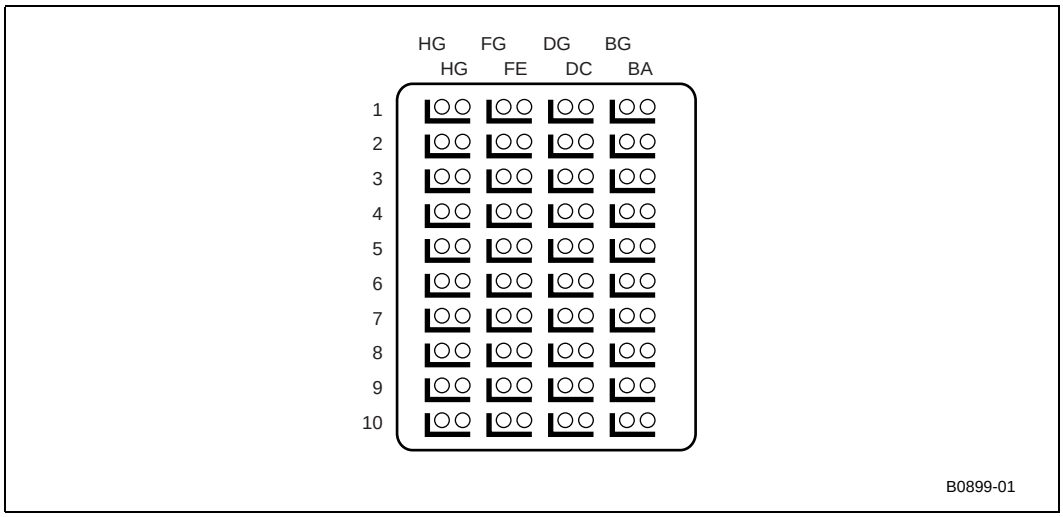
4.5.2 AdvancedTCA Data Transport Connector (J23)

Zone 2 consists of one 120-pin HM-Zd connector, labeled P23, with 40 differential pairs. This data transport connector provides the following signals:

- Two 10/100/1000BASE-T/TX Ethernet base channels (4 differential signal pairs each, 16 signals total)
- Two 1000BASE-BX Ethernet fabric channels (4 differential signal pairs each, 8 signals total)

The connector used is an AMP*/Tyco* part number 1469001-1. Figure 22 shows a face view of the connector.

Figure 22. Data Transport Connector (Zone 2) J23



The BG, DG, FG, and HG (G for Ground) columns contain the ground shields for the four columns of differential pairs. They have been omitted from the pinout tables below for simplification. All pins in the BG, DG, FG, and HG columns are connected to logic ground.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 19. AdvancedTCA Data Transport Connector (Zone 2) J23 Pin Assignments

Pin	A	B	C	D	E	F	G	H
1	No Connect	No Connect	Terminated	Terminated	No Connect	No Connect	Terminated	Terminated
2	F[2]Tx0+	F[2]Tx0-	F[2]Rx0+	F[2]Rx0-	F[2]Tx1+	F[2]Tx1-	F[2]Rx1+	F[2]Rx1-
3	No Connect	No Connect	Terminated	Terminated	No Connect	No Connect	Terminated	Terminated
4	F[1]Tx0+	F[1]Tx0-	F[1]Rx0+	F[1]Rx0-	F[1]Tx1+	F[1]Tx1-	F[1]Rx1+	F[1]Rx1-
5	BI_DA1+ (Tx1+)	BI_DA1- (Tx1-)	BI_DB1+ (Rx1+)	BI_DB1- (Rx1-)	BI_DC1+	BI_DC1-	BI_DD1+	BI_DD1-
6	BI_DA2 + (Tx2+)	BI_DA2- (Tx2-)	BI_DB1+ (Rx2+)	BI_DB1- (Rx2-)	BI_DC2+	BI_DC2-	BI_DD2+	BI_DD2-
7	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
8	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
9	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
10	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect

Fabric interface (Gigabit Ethernet) ports
Base interface (Gigabit Ethernet) ports

Note: All “Terminated” pins are grounded on the baseboard as defined in the PICMG 3.1, Release 1.0 specification.

The following naming convention describes the signals on this connector. Signal direction is defined from the perspective of the MPCBL0040 SBC.

For the Base Interface, the bi-directional 10/100/1000BASE-T data signals have the following conventions:

BI_Dr[c]p

- r = differential pair (A, B, C, or D)
- c = channel (1, 2)
- p = polarity (+, -)

For the Fabric Interface, the 1000BASE-BX data signals have the following conventions:

F[c]dnp

- c = channel (1, 2)
- d = direction (Tx = Transmit, Rx = Receive)
- n = port number (0, 1)
- p = polarity (+, -)

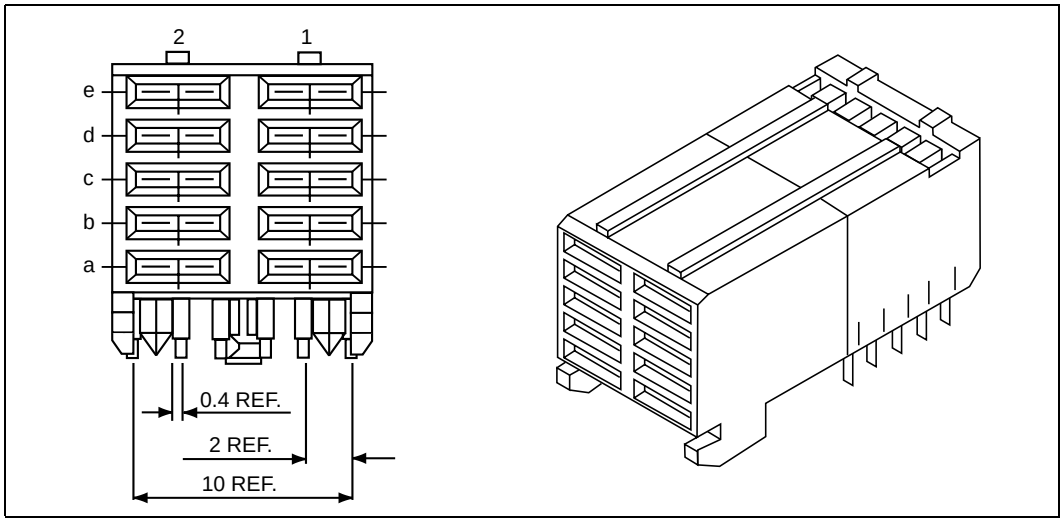
A port is two differential pairs; one Tx and one Rx.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

4.5.3 Zone 3 Rear Transition Module Power Connector (J30)

The J30 connectors are bladed connectors originally developed for FutureBus* applications.

Figure 23. J30 Connector



The signals are arranged as shown in Table 20.

Table 20. J30 Pinout

Pin	Signal	Pin	Signal
E2(S)	ENABLE#	E1(S)	PS1#
D2(S)	12V	D1(S)	12V
C2(M)	IPMI_Sdata	C1(M)	IPMI_Sclk
B2(L)	+3.3V_MP	B1(L)	Logic_GND
A2(L)	Shelf_GND	A1(L)	Logic_GND

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 21. J30 Signal Descriptions

Pin	Signal	Comments
A1	Logic_GND	Logic ground connection (long contact); provides return path for power and signal connections.
A2	Shelf_GND	Shelf ground connection (long contact); provides safety ground contact between SBC and RTM.
B1	Logic_GND	Logic ground connection (long contact); see A1 above.
B2	+3.3V_MP	Management power (long contact); provides up to 100 mA to power management system on RTM. Used exclusively for management power.
C1	IPMI_Sclk	IPMB/I^2C clock signal (medium contact); this provides the clock signal for the two-wire IPMB interface.
C2	IPMI_Sdata	IPMB/ I^2C data signal (medium contact); this provides the data signal for the two-wire IPMB interface.
D1	12V	12V RTM payload power (short contact); provides power to active devices (other than management system) on the RTM. See additional requirements below.
D2	12V	
E1	PS1#	Presence Signal, active low (short contact); the RTM connects this signal to Logic_GND through a 100 Ohm resistor (to facilitate manufacturing test). The SBC reads this signal to understand if an RTM is fully inserted.
E2	ENABLE#	Module enable signal, active low (short contact); the SBC sets this signal high to reset the RMC (RTM Management Controller).

4.5.4 Zone 3 Rear Transition Module Data/Control Connector (J31)

The MPCBL0040 SBC implementation includes an RTM connector (J31) that mates directly to the RTM without connecting through the backplane. The Zone 3 connector J3 consists of one 120-pin HM-Zd connector with 40 differential pairs, which allows high-speed signals to be passed between the boards. The signals that are routed through J31 are the IPMC signals, IEEE 1149.1 JTAG signals, SAS storage ports, USB 2.0 signals, and serial port.

Table 22. AdvancedTCA RTM Connector (Zone 3) J31 Pin

Pin	A	B	C	D	E	F	G	H
1	RMD_INT#	TRTST-	TCLK	TDI	TMS	TDO	Reserved	No Connect
2	SA[0]TX+	SA[0]TX-	SA[0]RX+	SA[0]RX-	SA[1]TX+	SA[1]TX-	SA[1]RX+	SA[1]RX-
3	SA[2]TX+	SA[2]TX-	SA[2]RX+	SA[2]RX-	SA[3]TX+	SA[3]TX-	SA[3]RX+	SA[3]RX-
4	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
5	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
6	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	PCI_RESET
7	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
8	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
9	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
10	USB[0]+	USB[0]-	DSR#	RXD#	RTS	TXD	CTS#	DTR

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 23. J31 Signal Descriptions

Pin	Signal	Comments
A1	RMD_INT#	This signal is driven by the RMD on non-intelligent RTMs to alert the SBC that there is a sensor needing attention. Non-intelligent RTMs are RTMs that don't have its own IPMC controller.
B1	TRST#	Test Reset signal as defined in JTAG (IEEE 1149.1). The SBC's main JTAG chain must connect to this signal.
C1	TCLK	Test Clock signal as defined in JTAG. Required on SBCs and RTMs with JTAG-enabled devices.
D1	TDI	Test Data In signal as defined in JTAG. SBCs must connect this signal into the test data chain (that is, in line with TDO connections from other chips), but must have a means to bypass this connection if an RTM is not installed.
E1	TMS	Test Mode State signal as defined in JTAG. Required on SBCs and RTMs with JTAG-enabled devices.
F1	TDO	Test Data Out signal as defined in JTAG. See TDI comments above. Output of RTM.
G1-H1	RSVD	Reserved.
A2-D3	SA[x]TX+, SA[x]TX-, SA[x]RX+, SA[x]RX-	Storage architecture signals for transmit and receive portions of differential pairs. Three SAS ports are routed to the RTM.
H6	PCI_RESET#	PCI reset signal required on all SBCs supporting PCI Express (pins A3-H4), but optional for RTMs. This signal is used by devices that need to provide a PCI interrupt but cannot always rely on MSI (Message Signaled Interrupt) to be implemented properly.
A10-B10	USB[0]+, USB[0]-	USB data signals. Note that the RTM's 5 V power for the USB connections must be derived from the 12 V rail.
C10	DSR#	Data Set Ready signal for COM1 RS-232 connection.
D10	RXD#	Received Data signal for COM1 RS-232 connection.
E10	RTS#	Ready to Send signal for COM1 RS-232 connection.
F10	TXD#	Transmit Data signal for COM1 RS-232 connection.
G10	CTS#	Clear to Send signal for COM1 RS-232 connection.
H10	DTR#	Data Terminal Ready signal for COM1 RS-232 connection.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

4.5.5 Zone 3 Rear Transition Module Data Connector (J32)

This J32 connector is used to route signals from the AdvancedMC slots to the RTM.

Table 24. AdvancedTCA RTM Connector (Zone 3) J32 Pinouts

Pin	A	B	C	D	E	F	G	H
1	AP1[0]TX+	AP1[0]TX-	AP1[0]RX+	AP1[0]RX-	AP1[1]TX+	AP1[1]TX-	AP1[1]RX+	AP1[1]RX-
2	AP1[2]TX+	AP1[2]TX-	AP1[2]RX+	AP1[2]RX-	AP1[3]TX+	AP1[3]TX-	AP1[3]RX+	AP1[3]RX-
3	AP1[4]TX+	AP1[4]TX-	AP1[4]RX+	AP1[4]RX-	AP1[5]TX+	AP1[5]TX-	AP1[5]RX+	AP1[5]RX-
4	AP1[6]TX+	AP1[6]TX-	AP1[6]RX+	AP1[6]RX-	AP1[7]TX+	AP1[7]TX-	AP1[7]RX+	AP1[7]RX-
5	AP1[8]TX+	AP1[8]TX-	AP1[8]RX+	AP1[8]RX-	No Connect	No Connect	No Connect	No Connect
6	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
7	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
8	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
9	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
10	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect

AP1[x] are signals routed from AdvancedMC to the RTM.

AMC_20 is mapped to AP1[0], AMC_19 to AP1[1], etc. and finally AMC_12 to AP1[8]

Tyco 1-1469373-1 (or equivalent). The Zone 3 alignment block (K2) is assigned a keying value of 73, and uses Tyco 7-1469373-3 (or equivalent).

4.5.6 Alignment Blocks

The MPCBL0040 SBC implements the K1 and K2 alignment blocks at the top of Zone 2 and Zone 3, as required in Section 2.4.4 of the PICMG 3.0 Specification. The Zone 2 alignment block (K1) is assigned a keying value of 11, and uses Tyco 1-1469373-1 (or equivalent). The Zone 3 alignment block (K2) is assigned a keying value of 73, and uses Tyco 7-1469373-3 (or equivalent).

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.0 Hardware Management

The Intelligent Platform Management Controller (IPMC) is based on the Renesas* microcontroller, model HD64F2166. This controller is a 16-bit processor with 40 KBytes of internal RAM and 512 KBytes of internal flash. It supports up to six I^2C buses (master/slave), three serial-ports, a low-pin count (LPC) interface, and an A/D and DAC. This microcontroller is also capable of addressing up to 16 MBytes and has external access to 2 MBytes of flash memory; 512 KBytes of SRAM and a 64 KByte serial EEPROM.

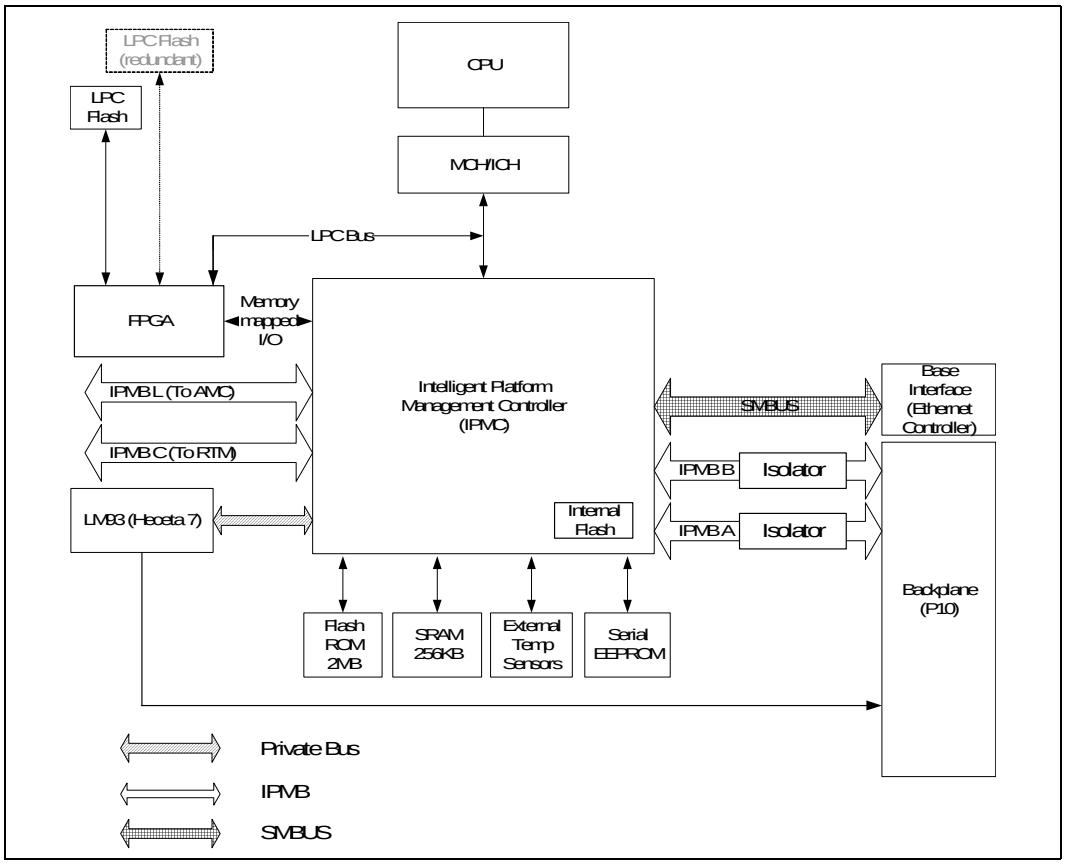
The IPMC implementation on the MPCBL0040 conforms to PICMG 3.0 R1.0 ECN002 specifications. IPMI defines a standardized, abstracted, message-based in-band and out-of-band interfaces between system management software and the platform management hardware. The manageability framework for the MPCBL0040 is developed per the IPMI v2.0 Specification, which includes the following:

- Intelligent Platform Management Controller (IPMC)
- IPMI messaging, commands, and abstractions
- IPMI channels, and sessions
- Sensors
- Sensor Data Records (SDRs) and SDR Repository
- FRU information
- Autonomous event logging
- System Event Log (SEL): holding at least 5,000 entries
- IPMI Hardware Watchdog Timer
- Platform Event Filtering (PEF)
- Serial Over LAN (SOL)— ability to redirect the system serial controller over LAN to a remote console.
- Proprietary management features including:
  - — Fault Resilient Booting
  - — BIOS logging of power-on self-test (POST) progress and POST errors
  - — Snooping of port 80h POST code
  - — Advanced Configuration and Power Interface (ACPI)
  - — Serial port buffering (at least one screen worth of data)
  - — Rear Transition Module (RTM) management support
  - — AdvancedMC* management support

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

The high-level architecture of the baseboard management for the MPCBL0040 is represented in Figure 24.

Figure 24. IPMC Block Diagram



The main processors communicate with the IPMC using the Keyboard Controller Style (KCS) interface. Two KCS interfaces are available for the BIOS to communicate with the IPMC. The BIOS uses the SMS interface for normal communication and the SMM interface when executing code under Systems Management Mode (SMM). The base address of the LPC interface for SMS is 0xCA2/CA3 for the SMS and 0xCA8/CAC for SMM operation. The BIOS is also able to communicate with the IPMC via the KCS interface for POST error logging purposes, fault resilient purposes and critical interrupts.

An external 256 KByte SRAM is used as a storage area for code when flash programming is under execution. The Field Replacement Unit (FRU) inventory information, SEL events, and SDR information is stored in the External Flash memory. Having the SEL and logging functions managed by the IPMC helps ensure that “post-mortem” logging information is available even if the system processor becomes disabled.

IPMB isolators on both IPMB busses are used to switch and isolate a faulty IPMB bus on a board from the backplane IPMB bus connections. Where possible, the IPMC activates the redundant IPMB bus to re-establish system management communication to report the fault.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

The on-board DC voltages are monitored by the LM93 device, manufactured by National Semiconductor*. The IPMC queries the LM93 over a local system management I^2C bus. External CPU thermal diodes and PROCHOT signals are connected to this device to ensure report thermal events.

The FPGA controls the enabling and monitoring of power good signals from all on-board power converters. It also controls power sequencing to ensure that all of the converters power up in the correct order to prevent any latch-up or damage to a device. The FPGA itself is also used to expand the GPIO capabilities of the IPMC management circuitry due to the limited number of GPIO's supported by the IPMC. The LPC interface between the FPGA and ICH is used to monitor the Port 80 codes during power up. In the event of a board failing to power up, a user can query the last five Port 80 codes stored in the FPGA registers using an RadiSys OEM IPMI command.

To increase the reliability of the MPCBL0040 SBC, a watchdog timer is implemented. More details on watchdog timer operation and features is covered in Section 5.14.1, "WDT #1 (IPMI Watchdog Timer)" on page 114.

5.1 Supervision

Table 25 lists the main components that perform hardware monitoring of voltages and timers.

Table 25. Hardware Monitoring Components

Component	Function	Monitors
Intelligent Platform Management Controller	WDT #1	IPMI watchdog timer. If the timer expires (times out), it executes pre-determined action (a hard reset, power down, power cycle or do nothing) and generates an IPMI SEL event is logged.
Intelligent Platform Management Controller	WDT #2	IPMI hardware watchdog timer. This WDT is strobed by IPMC firmware. It has a 1 second timeout with a 500ms strobe. If the WDT expires, it isolates the MPCBL0040 from the backplane IPMB buses, and resets the IPMC.
LM93	Voltage/ Temperature	On-board voltages/temperature, processor thermal diodes, CPU "PROCHOT", and processor VID.
Various Devices	Temperature	Monitor on-board temperature. The board is equipped with seven on-board temperature sensors. See Figure 25, "On-board Temperature Sensor Locations" on page 88.

5.2 Sensor Data Record (SDR)

Sensor Data Records (SDRs) contain information about the type and number of sensors in the baseboard, sensor threshold support, event generation capabilities, and the types of sensor readings handled by system management firmware.

The MPCBL0040 management controller is set up as a satellite management controller (SMC). It supports sensor devices, whose population is static by nature. SDRs can be queried using Device SDR commands to the firmware.

Table 26 lists the sensor identification numbers and information regarding the sensor type, name, supported thresholds, assertion and deassertion information, and a brief description of the sensor purpose. See the Intelligent Platform Management Interface Specification, Version 2.0 and Intelligent Platform Management Interface Specification, Version 2.0 for sensor and event/reading-type table information. The following sections describe the information contained in Table 26.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.2.1 Sensor Type

The sensor type references the values enumerated in the Sensor Type Codes table in the IPMI 2.0 specification. It provides the context in which to interpret the sensor, such as the physical entity or characteristic that is represented by this sensor.

5.2.2 Event/Reading Type

The Event/Reading Type references values from the Event/Reading Type Code Ranges and Generic Event/Reading Type Codes tables in the IPMI 2.0 specification. Note that digital sensors are a specific type of discrete sensors, which have only two states.

5.2.3 Event Thresholds/Triggers

Event Thresholds are supported event generating thresholds for Threshold type sensors.

- [u,l][nr,c,nc]: upper nonrecoverable, upper critical, upper noncritical, lower nonrecoverable, lower critical, lower noncritical
- uc, lc: upper critical, lower critical

Event Triggers are supported event generating offsets for discrete type sensors. The offsets can be found in the Generic Event/Reading Type Codes or Sensor Type Codes tables in the IPMI specification, depending on whether the sensor event/reading type is generic or a sensor specific response

5.2.4 Assertion/De-assertion Enables

Assertions and de-assertion indicators reveals what type of events this sensor can generate.

- As: Assertion
- De: Deassertion

5.2.5 Readable Value/Offsets

Readable value indicates the type of value returned for threshold and other non-discrete type sensors.

Readable offsets indicates the offsets for discrete sensors that are readable via the Get Sensor Reading command. Unless otherwise indicated, all event triggers are readable, In other words, readable offsets consist of the reading type offsets that do not generate events.

5.2.6 Event Data

This is the data that is included in an event message generated by the associated sensor. For threshold-based sensors, the following abbreviations are used:

- R: Reading value
- T: Threshold value

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.2.7 Health LED On/Off

This indicates events that turn on or off the Health LED. The following are used to indicate how the LED is affected.

- +: Event turns on the LED. Payload power cycle is required to turn it off
- C/D: critical event assertion turns LED on. Deassertion turns it off

5.2.8 Rearm Sensors

The “rearm” is a request for the event status for a sensor to be rechecked and updated upon a transition between good and bad states. Rearming the sensors can be done manually or automatically. This column indicates the type supported by the sensor. The following abbreviations are used in the “Rearm” column of Table 26 to describe a sensor:

- A: Auto rearm
- M: Manual rearm

5.2.9 Standby

Some sensors operate on standby power. These sensors may be accessed and/or generate events when the payload power is off, but DC power is present.

5.2.10 Polling Time

The polling time is the interval time in seconds that the IPMC controller reads the sensor to determine the value of the sensor. For example, if the polling time is 5 seconds, the value of that sensor is read every 5 seconds and compared against the Sensor Device Record (SDR) thresholds. If the sensor value exceeds the threshold limits, then a SEL event is generated. Some sensors generate events asynchronously and do not need to be polled. Typically, only analog sensors require polling.

5.2.11 Managing Device

The managing device is the hardware device that a sensor is connected to.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 26. IPMC Hardware Sensor and Events (Sheet 1 of 13)

Sensor No.	Sensor Name	Sensor Type	Event / Reading Type	Event Offset ED1 [3:0]	Event Data		Health Led On	Health Led Off	Event	Assert / De-assert	Readable Value / Offsets	Rearm	Standby	Polling Time, (seconds)	Managing Device
					Byte 2	Byte 3									
01h	Power Unit	Power Unit 09h	Sensor Specific 6Fh	00h	Power Fault Reg #1	Power Fault Reg #2			Power Off	As & De	–	A	X		
				01h					Power Cycle	As					
				05h					Soft Power Control Fault	As & De					
				06h					Power Unit Failure	As & De					
03h	IPMI Watchdog	Watchdog 2 23h	Sensor Specific 6Fh	00h	As per IPMI Spec.	FFh			Timer Expired	As	–	A	X		
				01h					Hard Reset						
				02h					Power Down						
				03h					Power Cycle						
				08h					Timer Interrupt						
04h	Scrty Violation	Platform Security Violation Attempt 06h	Sensor Specific 6Fh	00h	FFh	FFh			Secure Mode Violation attempt	As	–	A	X		
				05h					Out-of-band access password violation						

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 26. IPMC Hardware Sensor and Events (Sheet 2 of 13)

Sensor No.	Sensor Name	Sensor Type	Event / Reading Type	Event Offset ED1 [3:0]	Event Data		Health Led On	Health Led Off	Event	Assert / De-assert	Readable Value / Offsets	Rearm	Standby	Polling Time, (seconds)	Managing Device
					Byte 2	Byte 3									
06h	POST Error	System Firmware Progress (formerly POST error) 0Fh	Sensor Specific 6Fh	00h (POST error)	99h	99h			BIOS Checksum	As	–	A	–		
					FEh	00h			Timer Count Read/Write						
					FEh	01h			CMOS Battery						
					FEh	02h			CMOS Diagnosis Status						
					FEh	03h			CMOS Checksum						
					FEh	04h			CMOS Memory Size						
					FEh	05h	+		RAM Read/Write Test						
					FEh	06h			CMOS Date/Time						
					FEh	07h	+		Clear CMOS Jumper						
					FEh	08h	+		Clear Password Jumper						
					FEh	09h	+		Manufacturing Jumper						
					FEh	0Ah	+		BMC in update						
					FEh	0Bh	+		BMC Response Fail						
					FEh	0Ch	+		Event Log Full						
					FEh	10h	+		Configuration error on DIMM pair 0						
					FEh	11h	+		N/A						
					FEh	12h	+		No system memory is physically installed or fails to access any DIMMs SPD data.						

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 26. IPMC Hardware Sensor and Events (Sheet 3 of 13)

Sensor No.	Sensor Name	Sensor Type	Event / Reading Type	Event Offset ED1 [3:0]	Event Data Byte 2	Event Data Byte 3	Health Led On	Health Led Off	Event	Assert / De-assert	Readable Value / Offsets	Rearm	Standby	Polling Time, (seconds)	Managing Device
07h	Critical Int	Critical Interrupt 13h	Sensor Specific 6Fh	00h	FFh	FFh			Front Panel	As	-	A	-		
				08h			+		Bus error						
08h	Memory	Memory 0Ch	Sensor Specific 6Fh	00h	FFh	FFh			Correctable ECC	As	-	A	-		
				01h			+		Uncorrectable ECC						
09h	Logging Disabled	Event Logging Disabled 10h	Sensor Specific 6Fh	02h	FFh	FFh			Log Area Reset/Cleared	As	-	A	-		
				03h					All logging disable						
				04h					Log Area Full						
				05h		As per IPMI Spec			Log Area Full						
0Ah	Session Audit	Session Audit 2Ah	Sensor Specific 6Fh	00h	FFh As per IPMI Spec.	FFh As per IPMI Spec.			Session Activation	As	-	A	X		
				01h					Session Deactivation						
0Eh	Version Change	TBD 2Bh	Sensor Specific 6Fh												

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 26. IPMC Hardware Sensor and Events (Sheet 4 of 13)

Sensor No.	Sensor Name	Sensor Type	Event / Reading Type	Event Offset ED1 [3:0]	Event Data		Health Led On	Health Led Off	Event	Assert / De-assert	Readable Value / Offsets	Rearm	Standby	Polling Time, (seconds)	Managing Device
					Byte 2	Byte 3									
0Fh	FW Update	OEM C0h	OEM 70h	00h	Major FW Version	Minor FW Version			Roll-Back FW Image Captured	As	–	A	X		
				01h	FFh	FFh			Roll-Back SDR Captured						
				02h	Major FW Version	Minor FW Version			Staged Image Registered						
				03h	FFh	FFh			Staged SDR Registered						
				04h	Major FW Version	Minor FW Version			Roll-Back via Switch						
				05h					Roll-Back via Command						
				06h					FW Roll-Back due to operation check failure						
				07h					Roll-Back Complete						
				08h					Staged FW Update Completed						
				09h					Direct FW Update Completed						
10h	SBC +1.05V Vtt (DDR2 Vtt)	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	LM93
11h	SBC +1.1V (NIC Core)	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	LM93
12h	SBC +1.2V SAS (SAS I/O)	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	LM93

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 26. IPMC Hardware Sensor and Events (Sheet 5 of 13)

Sensor No.	Sensor Name	Sensor Type	Event / Reading Type	Event Offset ED1 [3:0]	Event Data		Health Led On	Health Led Off	Event	Assert / De-assert	Readable Value / Offsets	Rearm	Standby	Polling Time, (seconds)	Managing Device
					Byte 2	Byte 3									
13h	SBC +1.5V (Chipset Core)	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	LM93
14h	SBC +1.5V SUS (Suspend Pwr)	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	X	5	LM93
15h	SBC +1.8V LAN (NIC)	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	LM93
16h	SBC +1.8V MEM (DDR2 Core)	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	LM93
17h	SBC +3.3V	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	IPMC
18h	SBC +3.3V SUS (Suspend Pwr)	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	X	5	LM93
19h	SBC +5.0V	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	LM93
1Ah	SBC +5.0V USB	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	LM93
1Bh	SBC +12.0V	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	LM93
1Ch	AMC +12.0V	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	LM93
1Dh	AMC CurSense	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	LM93
20h	SBC +1.1V SUS (NIC SUS)	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	IPMC
21h	SBC +1.8V (NIC SUS)	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	IPMC

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 26. IPMC Hardware Sensor and Events (Sheet 6 of 13)

Sensor No.	Sensor Name	Sensor Type	Event / Reading Type	Event Offset ED1 [3:0]	Event Data		Health Led On	Health Led Off	Event	Assert / De-assert	Readable Value / Offsets	Rearm	Standby	Polling Time, (seconds)	Managing Device
					Byte 2	Byte 3									
22h	SBC RTC VCC	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	LM93
23h	SBC +5V SUS (Suspend Power)	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	IPMC
30h	SBC Temp 1 (Internal LM93, between CPUs)	Temp 01h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	X	0.5	LM93
31h	SBC Temp 2 (Near MCH)	Temp 01h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	X	0.5	ADT7483
32h	SBC Temp 3 (Near DIMM 1)	Temp 01h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	X	0.5	ADT7483
33h	SBC Temp 4 (Near DIMM 2)	Temp 01h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	X	0.5	ADT7483
34h	SBC Temp 5 (Under HDD)	Temp 01h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	X	0.5	ADT7483
35h	SBC Temp 6 (Near SAS)	Temp 01h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	X	0.5	ADT7483
36h	SBC Temp 7 (Near NIC)	Temp 01h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	X	0.5	ADT7483
54h	BIOS FWH0	OEM C0h	Digital Discrete 03h	01h	FFh	FFh			State Asserted	As	–	A	–		
55h	BIOS FWH1	OEM C0h	Digital Discrete 03h	01h	FFh	FFh			State Asserted	As	–	A	–		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 26. IPMC Hardware Sensor and Events (Sheet 7 of 13)

Sensor No.	Sensor Name	Sensor Type	Event / Reading Type	Event Offset ED1 [3:0]	Event Data Byte 2	Event Data Byte 3	Health Led On	Health Led Off	Event	Assert / De-assert	Readable Value / Offsets	Rearm	Standby	Polling Time, (seconds)	Managing Device
56h	FIT Status	OEM C0h	Digital Discrete 03h	00h	As per RadiSys FIT Spec.				State Deasserted						
				01h					State Asserted						
82h	ACPI State	System ACPI Power State 22h	Sensor Specific 6Fh	00h					S0 / G0	As					
				01h					S1						
				04h					S4						
				05h					S5 / G2						
				07h					G3 Mechanical off						
				0Bh					Legacy On						
				0Ch					Legacy Off						
83h	System Event	System Event 12h	Sensor Specific 6Fh	04h	As per IPMI Spec.	As per IPMI Spec.			PEF Action	As	–	A	–		
84h	Button	Button 14h	Sensor Specific 6Fh	00h	FFh	FFh			Reserved	As	–	A	X		
				01h					Reserved						
				02h					Reserved						
85h	SMI Timeout	SMI Timeout F3h	Digital Discrete 03h	00h	FFh	FFh			State Deasserted	As	–	A	–		
				01h					State Asserted						
87h	NMI State	OEM C0h	Digital Discrete 03h	00h	FFh	FFh			State Deasserted	–	–	–	–		
				01h					State Asserted						

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 26. IPMC Hardware Sensor and Events (Sheet 8 of 13)

Sensor No.	Sensor Name	Sensor Type	Event / Reading Type	Event Offset ED1 [3:0]	Event Data		Health Led On	Health Led Off	Event	Assert / De-assert	Readable Value / Offsets	Rearm	Standby	Polling Time, (seconds)	Managing Device
					Byte 2	Byte 3									
88h	SMI State	OEM C0h	Digital Discrete 03h	00h	FFh	FFh			State Deasserted	–	–	–	–		
				01h			+		State Asserted						
89h	IPMC Watchdog Overflow	OEM C0h	Digital Discrete 03h	01h	FFh	FFh			State Asserted	–	–	–	–		
8Ah	SBC FRU Hot Swap	PICMG Hot Swap Event F0h	Sensor Specific 6Fh	00h					M0 – FRU not installed						
				01h					M1 – FRU inactive						
				02h					M2 – FRU activation request						
				03h					M3 - FRU activation in progress						
				04h					M4 - FRU active						
				05h					M5 – FRU deactivation request						
				06h					M6 - FRU deactivation in Progress						
				07h					M7 - Communication lost						

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 26. IPMC Hardware Sensor and Events (Sheet 9 of 13)

Sensor No.	Sensor Name	Sensor Type	Event / Reading Type	Event Offset ED1 [3:0]	Event Data		Health Led On	Health Led Off	Event	Assert / De-assert	Readable Value / Offsets	Rearm	Standby	Polling Time, (seconds)	Managing Device
					Byte 2	Byte 3									
8Bh	iRTM FRU Hot Swap	PICMG Hot Swap Event F0h	Sensor Specific 6Fh	00h	FFh	FFh			M0 – FRU not installed	As	–	A	X		
				01h					M1 – FRU inactive						
				02h					M2 – FRU activation request						
				03h					M3 - FRU activation in progress						
				04h					M4 - FRU active						
				05h					M5 – FRU deactivation request						
				06h					M6 - FRU deactivation in Progress						
				07h					M7 - Communication lost						
8Ch	AMC FRU Hot Swap	PICMG Hot Swap Event F0h	Sensor Specific 6Fh	00h	FFh	FFh			M0 – FRU not installed	As	–	A	X		
				01h					M1 – FRU inactive						
				02h					M2 – FRU activation request						
				03h					M3 - FRU activation in progress						
				04h					M4 - FRU active						
				05h					M5 – FRU deactivation request						
				06h					M6 - FRU deactivation in Progress						
				07h					M7 - Communication lost						

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 26. IPMC Hardware Sensor and Events (Sheet 10 of 13)

Sensor No.	Sensor Name	Sensor Type	Event / Reading Type	Event Offset ED1 [3:0]	Event Data		Health Led On	Health Led Off	Event	Assert / De-assert	Readable Value / Offsets	Rearm	Standby	Polling Time, (seconds)	Managing Device
					Byte 2	Byte 3									
8Dh	IPMB Link State	PICMG Physical IPMB-0 Link F1h	Sensor Specific 6Fh	00h	FFh	FFh			IPMB A & B disabled	As	–	A	X		
				01h					IPBM A enabled IPMB B disabled						
				02h					IPMB A disabled IPMB B enabled						
				03h					IPMB A & B enabled						
90h	CPU 1 Status	Processor 07h	Sensor Specific 6Fh	00h	FFh	FFh	+		IERR	As	–	M	X	2	IPMC
				01h			+		Thermal Trip	As					
				02h					FRB1	As & De					
				03h					FRB2	As & De					
				04h					FRB3	As & De					
				05h					Config Error	As & De					
				07h				+	Presence	As & De					
				08h					Disabled	As & De					
				0Ah					Automatically throttled (Prochot)	As & De					

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 26. IPMC Hardware Sensor and Events (Sheet 11 of 13)

Sensor No.	Sensor Name	Sensor Type	Event / Reading Type	Event Offset ED1 [3:0]	Event Data		Health Led On	Health Led Off	Event	Assert / De-assert	Readable Value / Offsets	Rearm	Standby	Polling Time, (seconds)	Managing Device
					Byte 2	Byte 3									
91h	CPU 2 Status	Processor 07h	Sensor Specific 6Fh	00h	FFh	FFh	+		IERR	As	–	M	X	2	IPMC
				01h			+		Thermal Trip	As					
				02h					FRB1	As & De					
				03h					FRB2	As & De					
				04h					FRB3	As & De					
				05h					Config Error	As & De					
				07h				+	Presence	As & De					
				08h					Disabled	As & De					
				0Ah					Automatically throttled (Prochot)	As & De					
92h	CPU 1 Temp	Temp 01h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	X	0.5	LM93
93h	CPU 2 Temp	Temp 01h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	X	0.5	LM93
94h	CPU 1 Vcc	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	LM93
95h	CPU 2 Vcc	Voltage 02h	Threshold 01h	R, T	–	–	C	D	[u,l][nr,c,nc]	As & De	Analog	A	–	5	LM93
96h	CPU 1 ThermCtrl	Temp 01h	Discrete 07h	00h					Transitioned to OK	As & De	–	M	–	2	LM93
				01h					Transitioned to Non-Critical from OK						

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 26. IPMC Hardware Sensor and Events (Sheet 12 of 13)

Sensor No.	Sensor Name	Sensor Type	Event / Reading Type	Event Offset ED1 [3:0]	Event Data		Health Led On	Health Led Off	Event	Assert / De-assert	Readable Value / Offsets	Rearm	Standby	Polling Time, (seconds)	Managing Device
					Byte 2	Byte 3									
97h	CPU 2 ThermCtrl	Temp 01h	Discrete 07h	00h					Transitioned to OK	As & De	–	M	–	2	LM93
				01h					Transitioned to Non-Critical from OK						
98h	CPU 1 VRD Hot	Temp 01h	Discrete 07h	00h			D		Transitioned to OK	As & De	Analog	A	–	2	LM93
				01h			+		Transitioned to Non-Critical from OK						
99h	CPU 2 VRD Hot	Temp 01h	Discrete 07h	00h			D		Transitioned to OK	As & De	Analog	A	–	2	LM93
				01h			+		Transitioned to Non-Critical from OK						
9Ah	CPU Config Error	Processor 07h	Generic 03h	01h	FFh	FFh			State Asserted	As & De	Discrete	A	–		
E0h	DIMM 1	Slot Connector 21h	Sensor Specific 6Fh	00h	07h	Slot Number			Fault Status Asserted	As & De	–	A	–		
				02h					Device Installed	As & De					
				08h					Disabled	As					
				09h					Spared	As & De					
E1h	DIMM 2	Slot Connector 21h	Sensor Specific 6Fh	00h	07h	Slot Number			Fault Status Asserted	As & De	–	A	–		
				02h					Device Installed	As & De					
				08h					Disabled	As					
				09h					Spared	As & De					

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 26. IPMC Hardware Sensor and Events (Sheet 13 of 13)

Sensor No.	Sensor Name	Sensor Type	Event / Reading Type	Event Offset ED1 [3:0]	Event Data Byte 2	Event Data Byte 3	Health Led On	Health Led Off	Event	Assert / De-assert	Readable Value / Offsets	Rearm	Standby	Polling Time, (seconds)	Managing Device
E2h	Feed Fail Status	OEM C1h	Digital Discrete 03h	00h	FFh	FFh	D		State Deasserted	-	–	–	X		
				01h		Failure counter (FEED_FAIL)	+		State Asserted	As & De					
E3h	Base Link A Sts	LAN 27h	Sensor Specific 6Fh	00h	FFh	FFh			Heartbeat Lost (Link Down)	As	–	M	X	1	82571EB
				01h					Heartbeat (Link Up)						
E4h	Base Link B Sts	LAN 27h	Sensor Specific 6Fh	00h	FFh	FFh			Heartbeat Lost (Link Down)	As	–	M	X	1	82571EB
				01h					Heartbeat (Link Up)						
E5h	Fabric Lnk C St	LAN 27h	Sensor Specific 6Fh	00h	FFh	FFh			Heartbeat Lost (Link Down)	As	–	M	X	1	82571EB
				01h					Heartbeat (Link Up)						
E6h	Fabric Lnk D St	LAN 27h	Sensor Specific 6Fh	00h	FFh	FFh			Heartbeat Lost (Link Down)	As	–	M	X	1	82571EB
				01h					Heartbeat (Link Up)						
E7h	Fabric Lnk E St	LAN 27h	Sensor Specific 6Fh	00h	FFh	FFh			Heartbeat Lost (Link Down)	As	–	M	X	1	82571EB
				01h					Heartbeat (Link Up)						
E8h	Fabric Lnk F St	LAN 27h	Sensor Specific 6Fh	00h	FFh	FFh			Heartbeat Lost (Link Down)	As	–	M	X	1	82571EB
				01h					Heartbeat (Link Up)						

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.3 System Event Log (SEL)

The System Event Log (SEL) is the collection of events that are generated by the IPMC. Event logs are stored in non-volatile memory (Serial EEPROM). This resides on the board and allows better tracking of error conditions on the baseboard when it is moved from chassis to chassis. Having the SEL and logging functions managed by the IPMC helps ensure that post-mortem logging information is available should a failure occur that disables the system's processor(s). In the MPCBL0040, the 128kB of flash memory dedicated for SEL entries can store 6,552 entries. (128KB / 20 Bytes per SEL = 6553.6 entries less the SEL Cleared Timestamp overhead, brings it down to 6,552 entries)

When a board is installed into a new system, the shelf manager will only log board SEL events that occur after the board is inserted into a chassis. There may be older SEL events stored in the board that may need to be retrieved for debug or troubleshooting purposes. To get all the SEL events stored on the board, issue a *Get SEL Info* IPMI command to find out the number of IPMC SEL entries. Then loop on the *Get SEL Entry* IPMI command for number of SEL entries obtained by the *Get SEL Info* command.

Events are normally forwarded to the shelf manager and logged to SEL on the board. If the on-board SEL is full, new events coming into the IPMC SEL will only be forwarded to the shelf manager. The user needs to ensure on-board SEL log events are backed up (if desired) and SEL log cleared if the log is full.

There are two ways to clear the on-board SEL. One method is to use the Event Log Configuration in the BIOS (see Table 51, "Advanced Menu Options" on page 146). The second method is used to clear the SEL are *Reserve SEL* and *Clear SEL* IPMI commands. Events may be received while the SEL is being cleared. The IPMC implements an event message queue to avoid messages being lost. Messages are not overwritten once they are stored in the queue.

The list of IPMC generated SEL events can be found in Table 26, "IPMC Hardware Sensor and Events" on page 72. Refer to the columns with the titles "Event Offset" and "Event".

A set of IPMI commands (see Appendix A:, "Supported IPMI Commands") allows the SEL to be read and cleared and allows events to be added to the SEL. The IPMI commands used for adding events to the SEL are *Platform Event Message*, *Add SEL* entry, and *Partial Add Entry*.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.3.1 Analog Sensors

Temperature and voltage readings are monitored by the LM93. They are critical parameters that ensure the MPCBL0040 is operating at its predefined threshold limits. The sensors, as defined by PICMG 3.0 are categorized as follows:

- Lower Non-Recoverable
- Lower Non-Critical
- Lower Critical
- Upper Non-Critical
- Upper Critical
- Upper Non-Recoverable

If a lower non-critical or upper non-critical threshold is exceeded, it raises a minor alarm. If a lower critical or upper critical threshold is exceeded, it raises a major alarm. The MPCBL0040 doesn't support any Upper/Lower Non-recoverable thresholds.

The health LED is turned solid red only when critical or non-recoverable thresholds (major alarm) are exceeded. However, for any of the categories above, the IPMC forwards the events to the shelf manager to log in the shelf manager's SEL.

Note: For all the voltages listed in the table below, none of the upper/lower non-critical thresholds are supported. By the time sensor error budgets and hysteresis values are taken into account, it is not always possible to set both non-critical and critical thresholds without the risk of generating substantial quantities of false alarms. To prevent this situation, the non-critical voltage thresholds are not supported.

Table 27. Analog Sensors and Thresholds for SDR v1.12 (Sheet 1 of 3)

Sensor Name	Description	Sensor Number	Normal Value	Thresholds					
				Lower Non-Recoverable	Lower Critical	Lower Non-Critical	Upper Non-Critical	Upper Critical	Upper Non-Recoverable
SBC +1.05V Vtt	1.05 Voltage Rail for DDR2 Vtt	10h	1.05		0.99			1.10	1.21
SBC +1.1V	1.1V for 82571EB	11h	1.1		1.04			1.15	1.27
SBC +1.2V SAS	1.2V for SAS Controller	12h	1.2		1.15			1.27	1.40
SBC +1.5V	1.5V for Chipset Core	13h	1.5		1.42			1.58	1.74
SBC +1.5V SUS	1.5V for Suspend Power	14h	1.5		1.42			1.58	1.74
SBC +1.8V LAN	1.8V for 82571EB	15h	1.8		1.68			1.91	2.09
SBC +1.8V MEM	1.8V for DDR2 Core	16h	1.8		1.69			1.90	2.09
SBC +3.3V	3.3V Voltage Rail	17h	3.3		3.10			3.51	3.87

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 27. Analog Sensors and Thresholds for SDR v1.12 (Sheet 2 of 3)

Sensor Name	Description	Sensor Number	Normal Value	Thresholds					
				Lower Non-Recoverable	Lower Critical	Lower Non-Critical	Upper Non-Critical	Upper Critical	Upper Non-Recoverable
SBC +3.3V SUS	3.3V for Suspend Power	18h	3.3		3.10			3.51	3.87
SBC +5.0V	5V Voltage Rail	19h	5.0		4.73			5.25	5.80
SBC +5.0V USB	5V for USB	1Ah	5.0		4.58			5.36	5.90
SBC +12.0V	12V Voltage Rail	1Bh	12.0		10.90			13.36	14.74
AMC +12.0V	12V for AdvancedMC Slot	1Ch	12.0		10.90			13.36	14.74
AMC CurSense	AdvancedMC Current Sense	1Dh	2.73 Amps					3.8 Amps	4.19 Amps
SBC +1.1V SUS	1.1V for Suspend Power	20h	1.1		1.02			1.17	1.30
SBC +1.8V	1.8V for 82571EB Base Interface Suspend Power	21h	1.8		1.71			1.90	2.10
SBC RTC VCC	Real Time Clock Voltage	22h	3.41		2.00			3.63	4.01
SBC +5V SUS	5V for Suspend Power	23h	5.0		4.60			5.41	5.95
SBC Temp 1	Temp Sensor Between CPUs	30h	38		-5	5	70	80	90
SBC Temp 2	Temp Sensor Near MCH	31h	38		-5	5	65	75	85
SBC Temp 3	Temp Sensor DIMM 1 (J10)	32h	38		-5	5	65	74	85
SBC Temp 4	Temp Sensor DIMM 2 (J9)	33h	38		-5	5	57	66	80
SBC Temp 5	Temp Sensor Under Hard Drive	34h	38		-5	5	75	85	95
SBC Temp 6	Temp Sensor SAS Controller	35h	38		-5	5	65	72	80
SBC Temp 7	Temp Sensor Near 82571EB Fabric Interface 2	36h	38		-5	5	72	82	92

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 27. Analog Sensors and Thresholds for SDR v1.12 (Sheet 3 of 3)

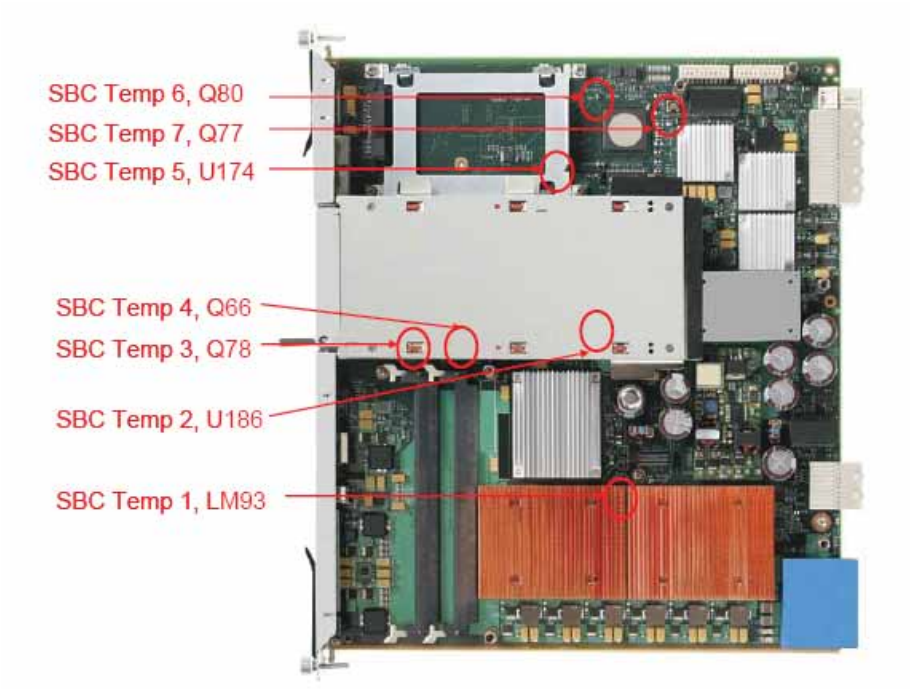
Sensor Name	Description	Sensor Number	Normal Value	Thresholds					
				Lower Non-Recoverable	Lower Critical	Lower Non-Critical	Upper Non-Critical	Upper Critical	Upper Non-Recoverable
CPU 1 Temp	CPU 1 Internal Temp Sensor	92h	38		-5	5	90	100	115
CPU 2 Temp	CPU 2 Internal Temp Sensor	93h	38		-5	5	90	100	115
CPU 1 VCC	CPU 1 Internal VCC	94h	1.27		0.69			1.32	1.40
CPU 2 VCC	CPU 2 Internal VCC	95h	1.27		0.69			1.32	1.40

5.3.2 Temperature Sensor Locations

The SBC is equipped with seven temperature sensors. Refer to Figure 25 for the location of all the on-board temperature sensors.

Note: In Figure 25, the “SBC Temp N” is the name of the on-board temperature sensor followed by the reference designator on the board.

Figure 25. On-board Temperature Sensor Locations



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.3.3 Processor Events

The following processor events are supported:

- **Processor presence** - Indicates if the processor is present in the socket.
- **PROCHOT** - Indicates if the processor has entered automatic thermal throttling mode (50% frequency duty cycle) due to high CPU die temperature.
- **IERR** - The processor asserts IERR as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus.
- **Thermal trip -** A thermal trip error indicates that the processor junction temperature has reached a level where permanent silicon damage may occur. Upon THERMTRIP assertion, the IPMC powers down the boards. PROCHOT is asserted before THERMTRIP asserts.
- **FRB3 Timeout** - The FRB3 algorithm is used to detect whether the boot strap processor is healthy and can run the BIOS. The assumed initial condition is that both processors are enabled. The basic algorithm is followed on each power up or system reset:
  1. At power up/reset, the IPMC starts an internal FRB3 timer. The FRB3 timeout is 2 minutes.
  2. In a good system, the BIOS issues the IPMI Set Watch Dog Timer (WDT #1) command with the “timer use” byte configured for the BIOS. When the IPMC receives this command, the IPMC starts the IPMI Watchdog Timer, and then stops the internal FRB3 timer. At this point, the FRB-2 phase starts.
  3. In a failing system, the BIOS does not issue the IPMI Set WDT command to the IPMC, and the IPMC FRB3 2 minute timer expires.
  4. The IPMC logs an FRB3 failure event against the failing processor sensor, logs a processor disable event against that processor sensor, then causes the payload power to reset.

5.3.4 DIMM Memory Events

The MCH (Memory Controller Hub) has logic built into the hardware to detect and correct correctable errors and detect uncorrectable errors. For either type of error, an SMI is generated to the processor, so that the BIOS can take the appropriate actions. On the MPCBL0040, such action includes detecting the error and sending a memory error event message to the IPMC firmware over the KCS interface.

5.3.4.1 DIMM Configuration Mismatch

Platforms that are based on the Intel® E7520 Chipset require DDR2 DIMMs to be populated in matched pairs. This error can happen due to presence of an inconsistent DIMM configuration. The BIOS detects incompatibility of DIMM configuration and generates an event to IPMC. Sensor type 0Ch; offset 07h; Event Data byte 3 of the event contains the DIMM identification.

5.3.4.2 Correctable Errors

MCH detects and corrects all 4-bit errors (S4EC) and generates an SMI to BIOS. The BIOS detects the cause of the error and sends an event to the IPMC. DIMM pair information is also sent to the IPMC as part of the event.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.3.4.3 Single-Bit ECC Errors

The system detects, corrects, and logs correctable errors as long as these errors occur infrequently (the system should continue to operate without a problem). Occasionally, correctable errors are caused by a persistent failure of a single component. Although these errors are correctable, continual calls to the error logger can affect system performance, preventing further useful work.

For this reason, the system counts certain types of correctable errors and disables reporting if errors occur too frequently. Error correction remains enabled, but calls to the error handler are disabled. This allows the system to continue running, despite a persistent correctable failure.

The BIOS adds an entry to the event log to indicate that logging for that type of error has been disabled. The system BIOS implements this feature for correctable bus errors. If ten errors occur within an hour, the corresponding error handler disables further reporting of that type of error. The BIOS re-enables logging and SMIs the next time the system is rebooted.

5.3.4.4 Uncorrectable Errors

The MCH detects 8-bit errors (D4ED) and generates SMI to the BIOS. If the error is in a data area, the BIOS generates an event to the IPMC. If the error is in a code area, the BIOS itself may be hung and it may not be possible to detect whether an uncorrectable error has occurred.

IPMC provides an additional SMI timeout sensor through which IPMC firmware continually monitors for SMI assertions and sets a 90 second timeout for clearing of SMI assertions. If SMI is not cleared within 90 seconds, the IPMC firmware generates an SMI timeout sensor event. The system manager can set policy for action to take on a SMI timeout, which can be pre-configured with the IPMC firmware to generate a power down, power cycle, cold reset, or warm reset of the blade.

If the OS or application executing on the processor has set up a watchdog timer with IPMC and it times out, a WDT timeout event is sent out and the IPMC takes the action that has been set up in the WDT (hard reset, power down, power cycle or do nothing).

5.3.5 System Firmware Progress (POST Error)

The BIOS performs a power-on self-test (POST) at initialization and logs errors detected to the SEL by generating a System Firmware Progress (sensor type 0Fh) event. The following is a list of POST errors for which events are generated:

- Timer Count Read/Write Error
- CMOS Battery Error
- CMOS Diagnostics Status Error
- CMOS Checksum Error
- CMOS Memory Size Error
- RAM Read/Write Test Error
- CMOS Date/Time Error
- Clear CMOS Jumper
- Clear Password Jumper
- Event Log Full Error
- No physical memory installed or access to the DIMM's SPD data failed

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.3.6 Port 80h POST Codes

As the BIOS goes through its initialization process, it sends progress codes to port 80h. These codes are useful for test debug purposes. For remote management purposes, the IPMC firmware provides the capability to snoop and capture up to five consecutive codes written to port 80h. These codes are captured automatically by the IPMC firmware when the board goes through either cold or warm reset or by an explicit IPMI command received by the IPMC via the available interfaces (IPMB or KCS).

5.3.7 Critical Interrupts

In general, the system BIOS is capable of generating requests on the KCS interface to communicate with the IPMC for error logging, fault resilience, critical interrupts, and reading/writing inventory CPUs and RAM information to the IPMC. Two LPC interfaces are available for the BIOS to communicate with the IPMC: the SMS interface for normal communication with the IPMC, and the SMM interface when executing code under SMM mode.

PCI errors implemented in the MPCBL0040 are handled as follows:

1. The MCH (E7520) sends a parity error/system error (PERR/SERR) message over the hub interface to the ICH, notifying it that an error occurred.
2. The ICH generates an SMI# interrupt when it receives a PERR/SERR message.
3. The SMI handler checks the error status registers of CPU/MCH until it identifies the source and type of the error.
4. The handler sends a message to the IPMC via the KCS interface, causing it to log the error in the IPMC's event log. The IPMC then forwards the event to the shelf manager to log into the SEL.

5.3.8 IPMB Link Sensor

The MPCBL0040 provides two IPMB links to increase communication reliability with the shelf manager and other IPM devices on the IPMB bus. These IPMB links work together for increased throughput where both buses are actively used for communication at any point. A request might be received over IPMB Bus A, and the response is sent over IPMB Bus B. Any requests that time out are retried on the redundant IPMB bus. In the event of any link state changes, the events are written to the SEL. The IPMC monitors the bus for any link failure and isolates itself from the bus if it detects that it is causing errors on the bus. Events are sent to signify the failure of a bus or, conversely, the recovery of a bus.

5.3.9 FRU Hot Swap

The Hot Swap event message conveys the current state of the FRU, the previous state, and a cause of the state change as can be determined by the IPMC. Refer to the PICMG 3.0 specifications for further details on the hot swap state.

5.3.10 Ethernet Link Status

The IPMC firmware monitors the Ethernet link status (present/absent) of all available ports on the SBC. In all, six Ethernet ports are available (two Base interface, four Fabric interface). One sensor is provided for each of the six Ethernet links. Events are generated by IPMC firmware when the sensor detect changes in LAN link status. During normal boot, the link status does change a few times during BIOS POST, when the network controller is enumerated by BIOS and then later when the OS loads the Ethernet Controller driver. Each of these changes will be logged as a SEL event.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.3.11 Power Feeds

Each blade has redundant -48V feeds, from which local on-board voltages are generated. IPMC firmware has ability to detect error in power feed on either of the feeds and generate an event. This is a critical event and health LED will turns to red. Only a feed failure is detected; the feed number is not detected because such detection is assumed to be made at the chassis level.

5.3.12 IPMC Watchdog Timer Reset

As per PICMG 3.0 requirements (section 3.2.4.6.3), the MPCBL0040 provides a watchdog timer that can reset the IPMC if the firmware hangs. After a reset, when IPMC restarts, an event is generated indicating that the IPMC was reset due to watchdog timer expiration.

5.4 Field Replaceable Unit (FRU) Information

The IPMC provides Field Replaceable Unit (FRU) information for the base board it manages and major replaceable modules on the SBC, such as the RTM and AdvancedMC. Table 28 gives the FRU device ID map.

Table 28. FRU Device ID Map

FRU Device ID	FRU Hardare Device
0	MPCBL0040 Single Board Computer
1	AdvancedMC slot on the MPCBL0040 SBC
2	Rear Transition Module (RTM) connected to the MPCBL0040 SBC

FRU information contained in the SBC includes data to describe the SBC as per the PICMG 3.0 Specification. Additional multirecords are provided to enable:

- the BIOS to write CPU information and BIOS version number to FRU data correctly; and
- customers to write their custom inventory information that is not part of any inventory data provided by the MPCBL0040.

Inventory information on the MPCBL0040 is divided into different areas that are written to at manufacturing time. Some information may be written by the BIOS during initialization, which are identified where necessary.

The following sections are definitions for the multirecords implemented by the firmware as part of the FRU data.

5.4.1 Common Header

A common header is mandatory for all FRU Inventory Device implementations. It contains version information for the overall information and offsets to other information areas.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.4.2 Board Area

The board area provides access to the following information, which is written when the board is manufactured:

- Manufacturing date and time
- Board manufacturer name
- Board product name
- Board serial number
- Board part number

5.4.3 Product Area

The product area provides access to following information, which is written when the board is manufactured:

- Manufacturer name (same as board manufacturer name)
- Product name (same as board product name)
- Product part/model number
- Product version
- Product serial number (same as board serial number)
- Asset tag

5.4.4 Multirecord Area

The multirecord area on the MPCBL0040 is further divided into nine different types:

- Board Point-to-Point Connectivity Record for E-Keying
- Carrier Information Table Record
- Carrier Activation and Current Management Record
- Carrier Point-to-Point Connectivity Record for E-Keying (AdvancedMC)
- Carrier Point-to-Point Connectivity Record for E-Keying (Rear Transition Module)
- AdvancedMC Point-to-Point Interface Record for E-Keying
- Rear Transition Module Point-to-Point Interface Record for E-Keying
- Record Type ID with version info for BIOS, Firmware, CPU and RAM Information
- Rear Transition MOdule Utilities Info record
- Power Consumption Information

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.4.4.1 BIOS, Firmware, CPU and RAM Information

An OEM record is provided that allows remote access to additional board-specific information that is not defined in the Platform Management FRU Information Storage Definition v1.0 Specification. Table 29 lists the information that is available on the MPCBL0040 SBC. Note that the table is an illustration. The actual structure that is implemented can be found using the FRU file itself.

Table 29. Additional Board-Specific Information

Information	Size (Bytes)	Data	Type
Manufacturer ID (Intel IANA number)	3	0x000157 (LSB first)	Binary
Record Version	1	1	Binary
Type/Length	1	1	Binary
No. of CPUs	1	x	Binary
Type/Length	1	2	Binary
RAM Information	2	X (in units of 1 MB)	Binary
Type/Length	1	(4 * XXX) + 1	Binary
Type/Length	1	0xFF	Binary
BIOS Version	63 (max)	yyyyyyyy	ASCI
End of Fields	1	0xC1	Binary

5.4.5 MPCBL0040 FRU Record

On the MPCBL0040 SBC, the FRU information pertaining to the board has been structured as below per the Platform Management FRU Information Storage Definition v1 specification.

The “Common”, “Board”, and “Product” fields are used by RadiSys during manufacturing and are used to program all the relevant board information into the FRU.

The “MULTIREC” is an RadiSys multi-record area allocated for use by the BIOS to program the relevant version information to the FRU during power up.

The following FRU record is an illustration of typical FRU information for the MPCBL0040 and is subject to change. Please refer to the MPCBL0040 IPMC release package for the latest FRU file.

```
_LF_NAME       'MPCBL040.fru'// Name for this load file

_LF_VERSION    '0.19'         // Version of this load file

_LF_FMT_VER    '1.50'// Version of the load file format

_IPMI_VERSION  '1.00'// IPMI format version


_FRU (

_FRU_TITLE     'CPU Board' // FRU Title

_START_ADDR    8000        // Start Address
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

```
_DATA_LEN      02D3        // Data Length
_NVS_TYPE      'IMBDEVICE' // Non-volatile Storage Type
_DEV_BUS       FF          // Device Bus
_DEV_ADDRESS   20          // Device Address

_SEE_COMMON
   01                 // Common Header Format Version
   00                // Internal Use Area Starting Offset (in multiples of 8 bytes)
   00                // Chassis Info Area Starting Offset (in multiples of 8 bytes)
   01                 // Board Info Area Starting Offset (in multiples of 8 bytes)
   0C                // Product Info Area Starting Offset (in multiples of 8 bytes)
   16                 // MultiRecord Area Starting Offset (in multiples of 8 bytes)
   00                 // Pad
   DC                 // Common Header Checksum

_SEE_BOARD
   01                 // Board Info Area Format Version Bit Fields
   0B                 // Board Info Area Length (in multiples of 8 bytes)
   00                 // Language Code
   000000             // Mfg. Date/Time
   D1                 // Board Manufacturer
   'Intel Corporation'
   C9                 // Board Product Name
   'MPCBL0040'
   CC                 // Board Serial Number
   '000000000000'
   CA                 // Board Part Number
   '0000000000'
   CC                 // FRU File ID
   'FRU Ver 0.19'
   C1                 // Board Custom Field


_SEE_PRODUCT
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

```
   01                // Product Info Area Format Version Bit Fields
   0a                // Product Info Area Length (in multiples of 8 bytes)
   00                // Language Code
   D1                // Product Manufacturer Name
   'Intel Corporation'
   C9                // Product Name
   'MPCBL0040'
   C9                // Product Part/Model Number
   'MPCBL0040'
   C0                // Product Version
   CC                // Product Serial Number
   '000000000000'
   D4                // Asset Tag
   '00000000000000000000'
   C0                // FRU File ID
   C0                // Product Custom Field
   C1                // Product Custom Field


_SEE_MULTIREC
                     // Board Point-to-Point Connectivity Record for E-Keying
   C0                // Record Type ID
   02                // Version Information
   1E                // Record Length
   AE                // Record Checksum (zero checksum)
   72                // Header Checksum (zero checksum)
   5A3100            // Manufacturer ID (PICMG)
                     // // As per PICMG3.0 v.90 Point-to-point Connectivity Record
   14               // PICMG Record ID For Board Point-to-point Connectivity Record
   00                // Record Format Version
   00                // OEM GUID Count
   01 11 00 00                              // Link Descriptor for Base Ethernet
CH1
   02 11 00 00                              // Link Descriptor for Base Ethernet
CH2
   41 23 00 00                               // Link Descriptor for Fabric Mux 1
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

```
Port 0 & Ethernet 1 Port 1

   41 21 00 00                                  // Link Descriptor for Fabric Mux 1
Port 0

   42 23 00 00                                  // Link Descriptor for Fabric Mux 2
Port 0 & Ethernet 2 Port 1

   42 21 00 00                                  // Link Descriptor for Fabric Mux 2
Port 0

                     // Carrier Information Table Record

   C0                // Record Type ID

   02                // Version Information

   09                // Record Length

   49                // Record Checksum (zero checksum)

   EC                // Header Checksum (zero checksum)

   5A3100            // Manufacturer ID (PICMG)

                     // // As per PICMG3.0 v.90 Carrier Information Table Record

                     1A // PICMG Record ID For Carrier Information Table

   00                // Record Format Version

   01                // AMC.0 Extension

   02                // AMC Site Count

   06                // AMC Site

   09                // RTM Site

                     // Carrier Activation and Current Management Record

   C0                // Record Type ID

   02                // Version Information

   0F                // Record Length

   D2                // Record Checksum (zero checksum)

   5D                // Header Checksum (zero checksum)

   5A3100            // Manufacturer ID (PICMG)

                     // // As per PICMG3.0 v.90

                    17 // PICMG ID For Carrier Activation and Current Management
Record

   00                // Record Format Version

   21 00             // Max Internal Current in 1/10 Amp Increments

   05                // Activation Readiness in Seconds

   02                // Module Descriptor Count

   7C 19 FF          // AMC Activation and Power Descriptors (19h = 2.5A = 30W)
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

```
   C0 11 FF          // RTM Activation and Power Descriptors (11h = 1.7A = 20.4W)
                     // Carrier Point-to-Point Connectivity Record for E-Keying
(AMC)
   C0                // Record Type ID
   02                // Version Information
   37                // Record Length
   43                // Record Checksum (zero checksum)
   C4                // Header Checksum (zero checksum)
   5A3100            // Manufacturer ID (PICMG)
                     // // As per PICMG3.0 v.90
                    18 // PICMG Record ID For Carrier Point-to-Point Connectivity
Record
   00                // Record Format Version
   86                // Resource ID
   10                // Point to Point Port Count
   01 00 00        // Link Descriptor for AMC_P0 to GbE Mux P0
   01 21 00        // Link Descriptor for AMC_P1 to GbE Mux P1
   02 41 00        // Link Descriptor for AMC_P2 to SAS HC P1
   03 90 00        // Link Descriptor for AMC_P4 to MCH PCIe P16
   03 B1 00        // Link Descriptor for AMC_P5 to MCH PCIe P17
   03 D2 00        // Link Descriptor for AMC_P6 to MCH PCIe P18
   03 F3 00        // Link Descriptor for AMC_P7 to MCH PCIe P19
   89 89 01        // Link Descriptor for AMC_P12 to RTM P9
   89 A8 01        // Link Descriptor for AMC_P13 to RTM P8
   89 C7 01        // Link Descriptor for AMC_P14 to RTM P7
   89 E6 01        // Link Descriptor for AMC_P15 to RTM P6
   89 05 02        // Link Descriptor for AMC_P16 to RTM P5
   89 24 02        // Link Descriptor for AMC_P17 to RTM P4
   89 43 02        // Link Descriptor for AMC_P18 to RTM P3
   89 62 02        // Link Descriptor for AMC_P19 to RTM P2
   89 81 02        // Link Descriptor for AMC_P20 to RTM P1
                     // Carrier Point-to-Point Connectivity Record for E-Keying
(RTM)
   C0                // Record Type ID
   02                // Version Information
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

```
   25                // Record Length
   DE                // Record Checksum (zero checksum)
   3B                // Header Checksum (zero checksum)
   5A3100            // Manufacturer ID (PICMG)
                     // // As per PICMG3.0 v.90
                    18 // PICMG Record ID For Carrier Point-to-Point Connectivity
Record
   00                // Record Format Version
   89                // Resource ID
   0A                // Point to Point Port count
   04 00 00        // Link Descriptor for SBC signals to RTM J31 (P0)
   86 2C 01        // Link Descriptor for RTM P9 to AMC_P12
   86 0D 01        // Link Descriptor for RTM P8 to AMC_P13
   86 EE 00        // Link Descriptor for RTM P7 to AMC_P14
   86 CF 00        // Link Descriptor for RTM P6 to AMC_P15
   86 B0 00        // Link Descriptor for RTM P5 to AMC_P16
   86 91 00        // Link Descriptor for RTM P4 to AMC_P17
   86 72 00        // Link Descriptor for RTM P3 to AMC_P18
   86 53 00        // Link Descriptor for RTM P2 to AMC_P19
   86 34 00        // Link Descriptor for RTM P1 to AMC_P20
                     // AMC Point-to-Point Interface Record for E-Keying
   C0                // Record Type ID
   02                // Version Information
   37                // Record Length
   3C                // Record Checksum (zero checksum)
   CB                // Header Checksum (zero checksum)
   5A3100            // Manufacturer ID (PICMG)
                     // // As per PICMG3.0 v.90
                    19 // PICMG Record ID For AMC Point-to-Point Interface Record
   00                // Record Format Version
   00                // GUID Count
   86                                          // [7]=0(Carrier) [5:4]=0h(RSVD)
[3:0]=0x6h(ID B2)
   04                                            // Channel Count
   E0 FF FF                                    // AMC Channel Descriptor 0
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

```
   E1 FF FF                                    // AMC Channel Descriptor 1

   E2 FF FF                                    // AMC Channel Descriptor 2

   A4 98 F3                                    // AMC Channel Descriptor 3

   00 51 00 00 FC                              // AMC Channel 0

   01 51 00 00 FC                              // AMC Channel 1

   02 71 20 00 FC                              // AMC Channel 2

   03 2F 00 00 FC                              // AMC Channel 3 (Lane 0-3, Exact
match)

   03 21 00 00 FC                            // AMC Channel 3 (Lane 0, Exact match)

   03 2F 00 00 FE                             // AMC Channel 3 (Lane 0-3, Matches
with '01b')

   03 21 00 00 FE                              // AMC Channel 3 (Lane 0, Matches
with '01b')

                     // RTM Point-to-Point Interface Record for E-Keying

   C0                // Record Type ID

   02                // Version Information

   74                // Record Length

   59                // Record Checksum (zero checksum)

   71                // Header Checksum (zero checksum)

   5A3100            // Manufacturer ID (PICMG)

                     // // As per PICMG3.0 v.90

                    19 // PICMG Record ID For RTM Point-to-Point Interface Record

   00                // Record Format Version

   05                // OEM GUID Count

   FC FD 47 24 37 08 1A AB 67 4E 23 8E 97 5D FF A8   // GUID 1 (MPCBL0040)

   08 DA 5A 82 B1 FA 1C BA 53 45 55 75 90 74 CC BE   // GUID 2 (MMBRTMIP01A or
MMB480RTMTE01A)

   BA BB 6A 5A 6B E7 DC 87 15 43 DE 1A 3F 17 38 2C   // GUID 3 (RSVD)

   AC 76 75 52 50 0B BC B4 C1 44 FF 7F 64 95 48 A9   // GUID 4 (RSVD)

   66 66 B7 85 54 A7 1E AB 56 49 D2 3D EA 91 6A AA   // GUID 5 (RSVD)

   89                                          // [7]=0(Carrier) [5:4]=0h(RSVD)
[3:0]=0x9h(ID C1)

   01                                            // Channel Count

   E0 FF FF                                    // RTM Channel Descriptor 0

   00 01 0F 00 FC                             // RTM Channel 0

   00 11 0F 00 FC                             // RTM Channel 1
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

```
   00 21 0F 00 FC                          // RTM Channel 2
   00 31 0F 00 FC                          // RTM Channel 3
   00 41 0F 00 FC                          // RTM Channel 3
C0                 // Record Type ID
   02                 // Version Information
   9E                 // Record Length
   DB                 // Record Checksum (zero checksum)
   C5                 // Header Checksum (zero checksum)
   570100             // Manufacturer ID
   01                 // Record Version
   01                 // Type/Length
   02                 // CPU No.s
   02                 // Type/Length
   00 00              // RAM Info
   06                 // Type/Length
   FF FF FF FF FF FF  // Reserved
                      02    // Type/Length
                      00    // FW Boot Major Version
                      00    // FW Boot Minor Version
                      03    // Type/Length
                      00                    // FW Major Version
                      00                    // FW Minor Version
                      00                    // FW Build
                      01                    // Type/Length
                      00                    // FPGA Version Number
                      01                    // Type/Length
                      00                    // Board Version Number
                      01                    // Type/Length
                      00                    // BIOS FWH Selected  0/1
                      FF                    // Type/Length
                      00 00 00 00 00 00 00 00 // BIOS Version
                      00 00 00 00 00 00 00 00
                      00 00 00 00 00 00 00 00
                      00 00 00 00 00 00 00 00
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

```
                        00 00 00 00 00 00 00 00
                        00 00 00 00 00 00 00 00
                        00 00 00 00 00 00 00 00
                        00 00 00 00 00 00 00
                        FF                      // Type/Length
                        00 00 00 00 00 00 00 00 // BIOS Version
                        00 00 00 00 00 00 00 00
                        00 00 00 00 00 00 00 00
                        00 00 00 00 00 00 00 00
                        00 00 00 00 00 00 00 00
                        00 00 00 00 00 00 00 00
                        00 00 00 00 00 00 00
                        C1 // End of Fields

// RTM Utilities Info record
   C0                   // Record Type ID
   02                   // Version Information
   0B                   // Record Length
   55                   // Record Checksum (zero checksum)
   DE                   // Header Checksum (zero checksum)
   570100               // Manufacturer ID (PICMG)
   04             // Intel OEM record subtype
   01                   // Record Format Version
   0C 08                // Product ID
   20                   // Intel IPMI Device ID 20=IPMC, 30=AMC, 40=RTM
   19 00                // FRU file info
   01                   // Flags

// Power Consumtion Information
   C0                   // Record Type ID
   82                   // Version Information
   0B                   // Record Length
   1C                   // Record Checksum (zero checksum)
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

```
97                  // Header Checksum (zero checksum)

570100              // Manufacturer ID

02                  // Intel Record Version / Id

8C                  // Power consumption[ 140 W ]

BE                  // Upper non-recoverable threshold[ 190 W ]

AA                  // Upper critical threshold[ 170 W ]

96                  // Upper non-critical threshold[ 150 W ]

00                  // Lower non-recoverable threshold

00                  // Lower critical threshold

00                  // Lower non-critical threshold
```

5.4.6 FRU Area for Customer-Specific Information

In the SBC FRU, an EEPROM is used to store all the FRU records. Customers can program user-specific information into the customer FRU MRA records. The FRU structure for the MPCBL0040 SBC is defined by the FRU file. Users can utilize the standard IPMI command to write this data.

The physical size available is 1024 bytes with 256 bytes available for user data. There is room for customers to write user data to the FRU after the RadiSys OEM-MRA records at the end of the FRU file. Additional MRA records added by customer shall not exceed this 256 byte limit.

5.4.7 Writing to the Customer FRU MRA

The standard FRU IPMI read/write command is used to write to the customer FRU MRA.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

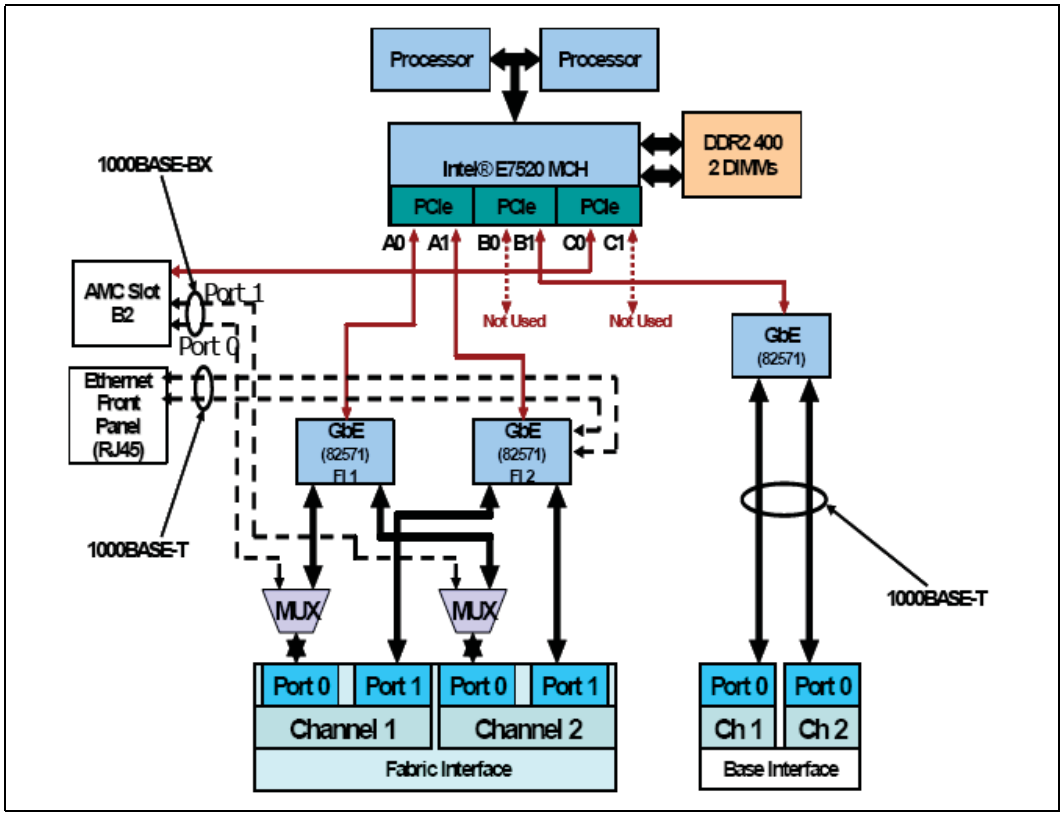
5.5 E-Keying

E-keying has been defined in the PICMG 3.0 Specification to prevent board damage, prevent misoperation, and verify fabric compatibility. The FRU data contains the board point-to-point connectivity record as described in Section 3.7.2.3 of the PICMG 3.0 Specification.

E-Keying is provided for connectivity between the MPCBL0040 board and the RTM and the MPCBL0040 and the AdvancedMC slot as described the in Section 3.9 and 3.7 of the AMC.0 RC.1.1 specification. The Set/Get AdvancedMC Port State IPMI commands defined by the AMC.0 specification are used for either granting or rejecting the E-keys.

Upon management power-on, the firmware sets the Gigabit Ethernet connectivity (fabric interface) to the backplane by default. Refer to Figure 26 for the fabric interface Ethernet routing. In the figure below, bolded lines to the backplane fabric interface show the default board settings.

Figure 26. Fabric Interface Ethernet Routing



The IPMC stores the configuration that determines where the fabric ports are routed; to the front panel or to the backplane. An OEM IPMI command can be sent by the BIOS or external software to get/set the fabric port direction setting.

The user can send this OEM IPMI command when the IPMC is operational, but changes to the routing are not applied on the fly. The user must reset the board to activate the settings. This can be initiated separately via IPMI or AdvancedTCA-defined IPMI commands.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 30 lists connections to the base and fabric interfaces for E-keying purposes, and also lists the link descriptors for the two Gigabit Ethernet channels connected to the base interface and the four Gigabit Ethernet channels on the fabric interface. Table 31 lists AdvancedMC link descriptors.

Table 30. E-Keying Board Point-to-Point Connectivity Link Descriptor List

#	Link Descriptor	Link Grouping ID [31:24]	Link Type Extension [23:20]	Link Type [19:12]	Link Designator			Link Desc Value
					Port 0 - 3 Flags {11:8}	Interface {7:6}	Channel [5:0]	
1	Base Interface Ethernet Ch 1, Port 0	0	0000	00000001	0001	00	000001	0x00001101
2	Base Interface Ethernet Ch 2, Port 0	0	0000	00000001	0001	00	000010	0x00001102
3	Fabric Interface Ethernet Ch 2, Port 0 and Port 1	0	0000	00000010	0011	01	000001	0x00002341
4	Fabric Interface Ethernet Ch 2, Port 0	0	0000	00000010	0001	01	000001	0x00002141
5	Fabric Interface Ethernet Ch 1, Port 0 and Port 1	0	0000	00000010	0011	01	000010	0x00002342
6	Fabric Interface Ethernet Ch 1, Port 0	0	0000	00000010	0001	01	000010	0x00002142

Table 31. AdvancedMC (ID B2) Link Descriptors

#	Link Descriptor	Reserved	Asymmetrical Match	Link Group ID	Link Type Ext.	Link Type	Link Designator	Link Desc Value
		[39:34]	[33:32]	[31:24]	{23:20}	{19:12}	[11:0}	
1	AdvancedMC Channel 0	111111b	00b (Exact)	00h	0h	05h	100h	0xFC00005100
2	AdvancedMC Channel 1	111111b	00b (Exact)	00h	0h	05h	101h	0xFC00005101
3	AdvancedMC Channel 2	111111b	00b (Exact)	00h	2h	07h	102h	0xFC00207102
4	AdvancedMC Channel 3	111111b	00b (Exact)	00h	0h	02h	F03h	0xFC00002F03
5	AdvancedMC Channel 3	111111b	00b (Exact)	00h	0h	02h	103h	0xFC00002103
6	AdvancedMC Channel 3	111111b	10b (matches 01bt)	00h	0h	02h	F03h	0xFE00002F03
7	AdvancedMC Channel 3	111111b	10b (matches 01bt)	00h	0h	02h	103h	0xFE00002103

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.6 IPMC Platform Event Filtering (PEF)

The IPMC supports a maximum of 20 entries. Table 32 describes the factory pre-configured event filters and the unused entries that are software configurable. The only action available is to turn the Health LED to red.

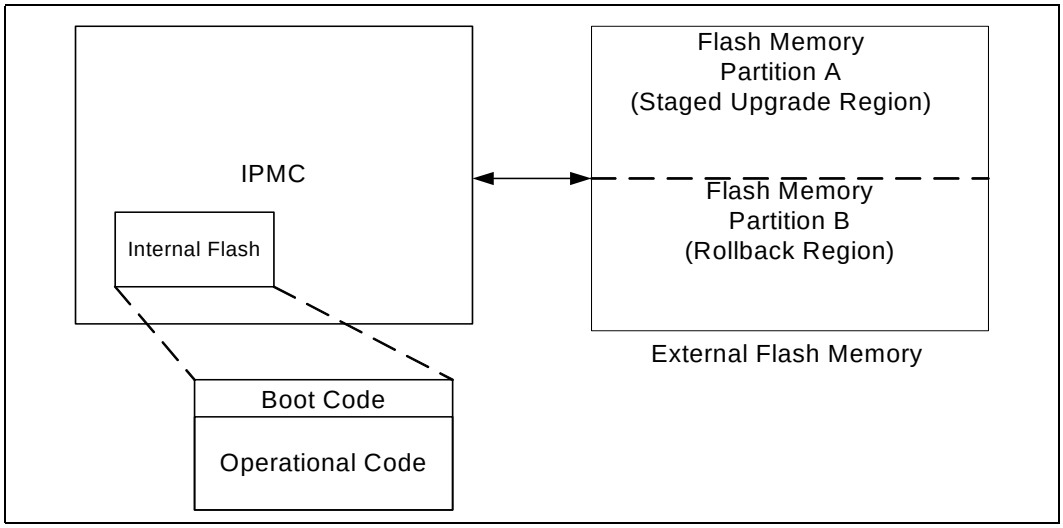
Table 32. Factory Default Event Filters

Event Filter #	Offset Mask	Events
0	PCI PERR and SERR	Critical Interrupt
1	(any)	POST Memory resize
2	Clear CMOS jumper installed	System FW Progress
3	Various other jumpers installed	System FW Progress
4	Memory configuration errors	System FW Progress
5	Memory Read/Write test	System FW Progress
6	Config error, Uncorrectable ECC, or correctable ECC limit	Memory Sensor
7 to 19	Unused	

5.7 IPMC Firmware Code Organization

Figure 27 shows the components of IPMC flash on the MPCBL0040.

Figure 27. High Level Block Diagram of IPMC Flash



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.7.1 Functional Description

The IPMC flash comprises two components:

- **Internal Flash on IPMC** – 512 KB of memory. Used to store the primary firmware image. It consists of boot block and operational code (known as the execution image):
  - **Boot Block** – This area contains the code necessary to update the IPMC main operational code (opcode) when there is no IPMC opcode loaded.
  - **Operational Code** – This area contains the active operational code.
- **External Flash Memory** – External 2 MByte flash memory. The external flash device is partitioned into numerous regions and includes two regions for the Online Firmware Update feature.
  - **Partition A** (Staged Upgrade Region) is used to store the staged firmware image. For every staged firmware update initiated by a user, the staged image is copied to this location (known as the staging image).
  - **Partition B** (Rollback Region) is used to store a backup copy of the original operational code image before a staged update firmware takes place (known as the rollback image).

5.7.2 IPMC Boot Block

The IPMC boot block is a recovery block and will enter direct firmware update mode if there is not a valid operational code image.

Starting with version of IPMC firmware release package 1.10.02, the boot block is now made up of two parts. The bootblock is split into a smaller Bootloader and a section called the XFU (eXternal Firmware Update). The Bootloader is installed using the Renesas utility, same as the Bootblock was in previous versions, but the Bootloader has much less functionality. Once the Bootloader runs, it looks in main flash memory for the XFU which has the rest of the needed boot functionality. The XFU comes as part of the IPMC Operational code.

When the boot block is updated, the operational IPMC firmware is erased. After the boot block update is completed, the next time the board boots, if there is an IPMC operational image in the rollback area, this image will be copied over to the IPMC and will start to execute. If there is no IPMC firmware in the rollback area, the IPMC will automatically enter direct firmware update mode.

The boot block is limited to a single IPMB interface, IPMB0-A. The boot block does not use IPMB0-B. If IPMB0-A is disabled (on the backplane or by the CMM) for any reason and there is no operational image installed, then IPMB communication to the boot block will not be possible. In this case, an operational code firmware update is only possible from the payload processor through KCS.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.8 IPMC Firmware Updates

There are two update modes:

- **Normal Mode** – This upgrade procedure happens when the user updates the IPMC firmware directly to the internal flash on the IPMC. The user will not have the ability to back up the “old” operational image.
- **Staged Update Mode** – The Staged Update feature allows the IPMC operational code to be updated while the system is online (OS is running). After the new image has been staged, it is copied to the internal flash of the IPMC upon completion of the staged upgrade. If the switchover fails, or at the user’s discretion, the firmware may be rolled back to the previous version.

  The advantage of running this mode are is the user can store the old firmware image to a rollback region (for redundancy or backup purposes).

The following section provides an overview of the staged update process. See Section 10.3, “Updating IPMC Firmware” on page 201 for more details and the procedure for updating IPMC firmware.

5.9 Ejector Mechanism

In addition to captive retaining screws, the MPCBL0040 SBC has two ejector mechanisms to provide a positive cam action, which ensures that the blade is properly seated and helps assist during blade extraction. The bottom ejector handle also has a micro switch that is connected to the IPMC to determine if the board has been properly inserted.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.10 Hot Swap LED

The MPCBL0040 SBC supports one blue Hot Swap LED, mounted on the front panel. See Figure 17, “Front Panel LEDs” on page 48 for its location. This LED indicates when it is safe to remove the SBC from the chassis. The on-board IPMC drives this LED to indicate the Hot Swap state. See Table 33.

When the lower ejector handle is disengaged from the faceplate, the Hot Swap switch on the board asserts a signal to the IPMC, and the IPMC moves from the M4 state to the M5 state. At the M5 state, the IPMC asks the CMM (or Shelf Manager) for permission to move to the M6 state. The Hot Swap LED indicates this state by blinking on for about 100 milliseconds, followed by 900 milliseconds in the off state. This occurs as long as the SBC remains in the M5 state. Once permission is received from the CMM or higher level software, the SBC moves to the M6 state.

The CMM or higher level system software may be configured to reject the request to move to the M6 state. If this occurs, the Hot Swap LED returns to a solid off condition, indicating that the SBC has returned to M4 state.

If the SBC reaches the M6 state, either through an extraction request through the lower ejector handle or a direct command from higher-level software, and an a CPI-enabled OS is loaded on the SBC, the IPMC communicates to the OS that the module must discontinue operation in preparation for removal. The Hot Swap LED continues to flash during this preparation time, just like it does in the M5 state. When the main board power is successfully removed from the SBC, the Hot Swap LED remains lit, indicating it is safe to remove the SBC from the chassis.

Warning: Removing the SBC prematurely can lead to corruption of files on the hard drive.

Table 33. Hot Swap LED

LED Status	Meaning
Off	Normal (active) status
Blinking Blue	Preparing for removal/insertion: Long blink indicates activation is in progress, short blink when deactivation is in progress.
Solid Blue	Ready for hot swap

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.11 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with the MPCBL0040 SBC requires an operating system that provides ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration) and APM support (normally contained in the BIOS)
- Power management control of individual devices, add-in boards (some AdvancedMC cards may require an ACPI-aware driver), and hard disk drives
- A soft-off feature that enables the operating system to power off the computer
- Support for an IPMC firmware command switch

The MPCBL0040 board supports the following states: S0, S1, S4 and S5

The AdvancedMC slot on the MPCBL0040 board supports the following state: S0 and S5

For ACPI enabled operating systems, the IPMC is configured such that ACPI mode is enabled via the BIOS ACPI Source Language (ASL) code. When ACPI shut down request is received, the IPMC will pulse the ICH power button for 100ms which will start shutting down the OS. Once OS is shutdown, it will assert the SLP_S5# (sleep S5) signal. If the OS fails to shutdown after 3 minutes (indicated by the fact that the SLP_S5# has not been asserted), the IPMC PICMG State Machine will timeout and force the payload off with a 4-second power button override to the ICH.

For non-ACPI enabled operating systems, the IPMC will perform a 4-second power button override to the ICH.

Note: SLP_S5# is one of the power management signal from ICH. The signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) state.

The IPMC management features are designed to work in conjunction with the ACPI BIOS and hardware features of the baseboard. The following sections illustrate these capabilities.

5.12 Reset Types

The following topics describe the two types of reset requests and the boot relationships among them. The two types of reset requests available on the MPCBL0040 are:

- Hard reset request (always results in a cold boot)
- Soft reset request (can result in either a warm or cold boot)

A hard reset request occurs whenever the processor Reset line is asserted, then deasserted. A soft reset occurs whenever an assertion occurs on the processor Init line. When a soft reset request occurs, the BIOS determines whether to initiate a warm boot while leaving main memory intact or a cold boot that clears memory. Table 34 summarizes hard and soft reset parameters.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 34. Reset Requests

Reset Request	Signal Activated	Type	Description
Hard	Reset	Full reboot	The payload is reset via the SYSRESET* input signal of the I/O Controller Hub (ICH). This reset results in a PCI reset, and thus the entire memory region is tested and the lower 8 MB of RAM is initialized. References to a cold reset imply a hard reset.
Soft	Init	Partial reboot	The payload is reset via the RCIN* input signal to the ICH. The ICH then maps this onto the INIT signal to the FW-Hub and CPUs and is asserted for 16 PCI clocks. A PCI reset is not generated in this scenario and the contents of the lower 8MB of RAM is maintained. References to a warm reset imply a soft reset.

Whenever the BIOS detects that the reset is either a hard reset or a cold boot, it specifically clears the memory location 40h:72h so it does not contain a 1234h. Under warm boot conditions, this memory location contains a 1234h (the developer's application writes this value in this location using /dev/mem when it is started). If a hard reset occurs, it is certain that the 40h:72h location contains a non-1234h value.

5.12.1 Reset Control Sources

Table 35 shows the sources for reset requests and the corresponding type of reset.

Table 35. System Reset Sources and Actions

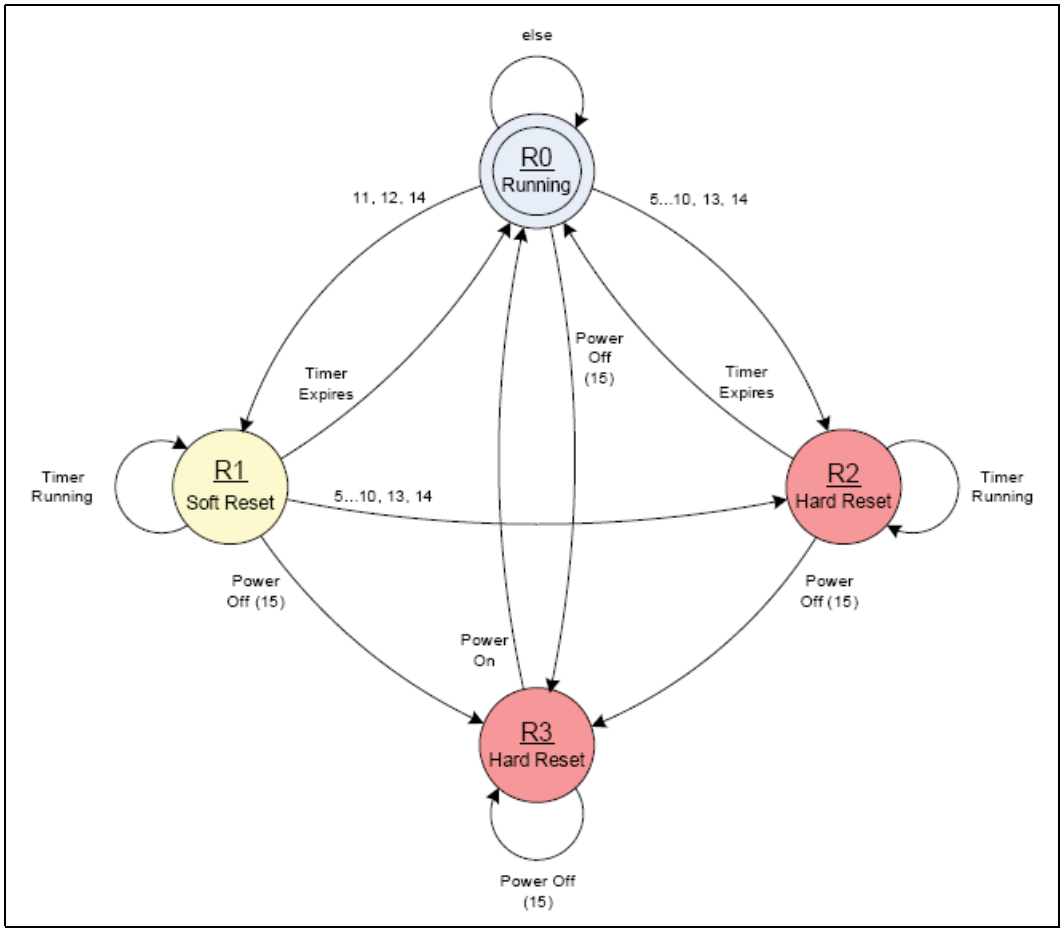
#	Reset Source	Payload Reset		IPMC Reset
		Soft	Hard	
1	Standby Power On Reset (SPOR)	--	--	Yes
2	IPMC Hardware Watch Dog Timer	No	No	Yes
3	IPMC Exit Firmware Update Mode	No	No	Yes
4	IPMI BMC Cold Reset command	No	No	Yes
5	IPMI Chassis Control command (hard reset)	No	Yes	No
6	IPMI Watchdog timer expiration (w/ action configured for payload reset)	No	Yes	No
7	IPMI PEF action	No	Yes	No
8	Fault Resilient Booting (FRB3 failure)	No	Yes	No
9	Set Processor State command (upon disabling a processor)	No	Yes	No
10	Reset BIOS Boot Flash	No	Yes	No
11	Front Panel Reset button	Yes	No	No
12	OS Warm Boot (restart)	Yes	No	No
13	PICMG Payload Activation (M4)	No	Yes	No
14	PICMG FRU Control command	Yes	Yes	No
15	Payload Power Off	--	Yes	No

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.12.2 Payload Reset Diagram

Figure 28 illustrates the reset state of the payload with respect to the possible source of the reset request given in Table 35.

Figure 28. Payload Reset State Diagram



5.12.3 Front Panel Payload Reset

The Reset button is a momentary contact button on the front panel. Its signal is routed through the front panel connector to the IPMC, which monitors and de-bounces it. The signal must be stable for at least 50 ms before a state change is recognized. The Front Panel reset is mapped to generate a soft reset to the payload.

5.12.4 IPMI Commanded Reset

The IPMI Chassis Control command is supported and can be used to generate a hard reset to the payload.

The PICMG FRU Control command can be used to generate either a hard or soft reset to the payload.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.12.5 Watchdog Timer Expiration

The Watchdog Timer can be configured to cause a hard reset to the payload upon its expiration. Timeout and action can be configured in BIOS. For more information, see the *Intelligent Platform Management Interface Specification*, Version 2.0.

5.12.6 FRB3 Failure

Simultaneous with resetting the payload, the IPMC starts an internal FRB3 timer. If the BIOS does not start the IPMI Watchdog Timer with the usage set for BIOS/FRB2, the IPMC resets the system when the internal FRB3 timer expires.

5.13 IPMC Reset Control

Table 36 shows all the sources of IPMC resets and the actions by the system and the IPMC. The payload will not be reset by an IPMC reset except after a combined IPMC boot block and operational code update. In all other cases, the payload is not reset or powered down. The IPMC re-synchronizes itself to the state of the processor and power control signals it finds when it initializes.

Table 36. IPMC Reset Sources and Actions

#	Reset Source	System Reset	IPMC Reset
1	Standby Power On Reset	No (payload not up yet)	Yes
2	IPMC Hardware WDT Expiration	No	Yes
3	IPMC Exit Firmware Update mode	No	Yes
4	IPMI BMC Cold Reset command	No	Yes
5	IPMC boot block update followed by IPMC operational code update	Yes	Yes
6	IPMC operational code update (without updating boot block)	No	Yes

5.13.1 Standby Power On Reset

Upon the SBC being inserted into a chassis, the IPMC is reset via the reset signal to the microcontroller. This is referred to as a Standby Power On Reset (SPOR). The firmware detects this situation programmatically, and initializes all of the GPIOs to a known state. At any time during normal operation, if the microcontroller reset input is asserted, the firmware initializes the GPIOs to a known state as if coming up from a SPOR event. This is only expected to occur if the standby power rail falls well below the regulation parameters of the power unit and the power monitoring hardware has asserted the reset to the microcontroller. If the standby power rail has failed, the payload power rails have also failed. Therefore, the payload has already been impacted, and it is therefore safe for the IPMC to initialize all its GPIOs to a known state.

5.13.2 IPMC Exit Firmware Update Mode

The IPMC firmware can be updated using firmware transfer commands through the LPC or IPMB interface. The IPMC automatically enters Firmware Transfer Mode if it detects that the Force Update signal is asserted during initialization or if the operation code checksum fails. Upon exit from Firmware Transfer Mode, the IPMC resets itself.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

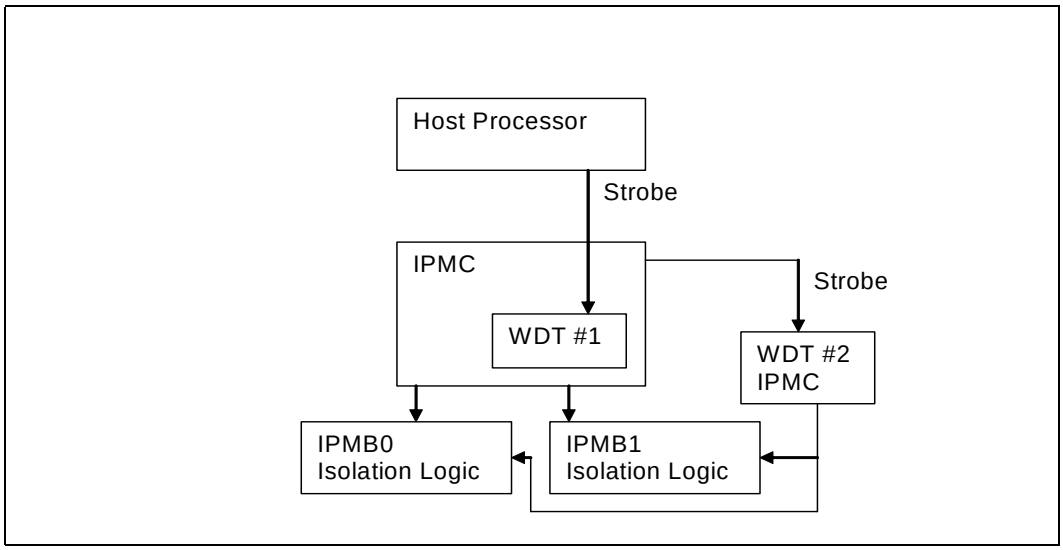
5.13.3 IPMI BMC Cold Reset Command

The IPMC firmware supports the ability to reset the IPMC via the IPMI Cold Reset command. For more information, see the *Intelligent Platform Management Interface Specification*, Version 2.0.

5.14 Watchdog Timers (WDTs)

Figure 29 shows the relationship between the two watchdog timers (WDTs) on the MPCBL0040.

Figure 29. Watchdog Timers



5.14.1 WDT #1 (IPMI Watchdog Timer)

WDT #1 is an IPMI Watchdog Timer. The host processor uses the IPMI “Set Watchdog Timer” message to configure WDT #1 and then the “Reset Watchdog Timer” message to strobe the timer over the KCS interface to the IPMC.

WDT #1 can be set in BIOS. Choose Boot Menu then OS Load Timeout Timer.

WDT #1 can also be configured to take various actions prior to timing out (for example, SMI_N, NMI, nothing) or after timing out (for example, hard reset, power down, power cycle or do nothing). In addition, an event can be logged in the System Event Log whenever the watchdog timer expires. If WDT #1 expires, the IPMC is not impacted (that is, it is not reset).

WDT#1 operates as per the IPMI version 2.0 Specification as IPMI Watchdog Timer.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.14.2 WDT #2 (IPMC Hardware Watch Dog Timer)

WDT #2 is a hardware timer internal to the IPMC and must be strobed by the IPMC firmware. When the IPMC firmware starts, one of the very first actions performed by the firmware is to initialize the internal hardware watchdog timer to expire after one second.

The IPMC firmware must reset the internal timer (programmed to do this every 500ms) before the timer expires. If the firmware fails to reset the hardware timer in 1 second, the IPMC core resets, and the firmware restarts from the reset vector. A failure of this nature is an indication that the firmware has failed in particular manner that it was unable to properly reset the hardware timer.

Any reset of the IPMC is completely transparent to the host processor with the possible exception that system management software attempting to communicate with the IPMC might time-out while the reset is in progress. There is no method for the processor to be explicitly notified that the IPMC is reset, but a SEL event will be logged upon next IPMC initialization cycle.

5.15 FRU Payload Control

The MPCBL0040 implements the FRU Control command as specified in the PICMG 3.0 Specification. Through this command, the payload can be reset, rebooted, or have its diagnostics initiated.

The FRU payload can be controlled by a command line via the CMM. The following RadiSys MPCMM0001/MPCMM0002 CMM commands are supported by the MPCBL0040. Equivalent commands from other shelf managers are available. Refer to the appropriate documentation for third party shelf managers.

Table 37. CMM Commands for FRU Control Options

FRU Control Options	MPCMM0001 / MPCMM0002 command
Cold Reset	cmmset –l bladeN –d frucontrol –v 0 (N is chassis slot number)
Warm Reset	cmmset –l bladeN –d frucontrol –v 1 (N is chassis slot number)
Graceful Reboot	cmmset –l bladeN –d frucontrol –v 2 (N is chassis slot number)
Diagnostic Interrupt	cmmset –l bladeN –d frucontrol –v 3 (N is chassis slot number)

5.15.1 Cold Reset

When this command is initiated, the board performs a hard reset as described in Section 5.12.

5.15.2 Warm Reset

When this command is initiated, the board performs a soft reset as described in Section 5.12.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

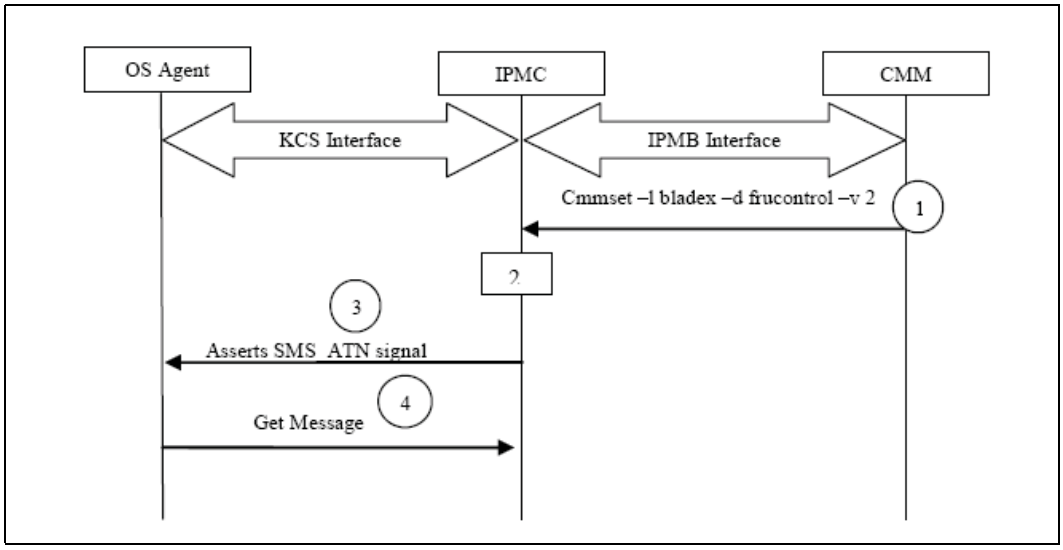
5.15.3 Graceful Reboot

This specific payload control command is implemented using the system interface messaging capability and the SMS_ATN bit of the KCS Status registers.

The Receive Message Queue is used to hold message data for system software until the system software can collect it, while the SMS_ATN bit is used to indicate that the IPMC requires attention from the system software.

The flow diagram shown in Figure 30 will assist users that are developing their system software to interact with this command.

Figure 30. Flow Diagram for Graceful Reboot Command



1. The MM sends a frucontrol=2 command to the IPMC, initiating a graceful reboot.
2. When the IPMC receives frucontrol=2, it formats a message into the send message queue and sets the SMS attention flag (SMS_ATN) on the KCS status register.
3. The OS agent polls for SMS_ATN using the Get Message Flags command.
4. The OS agent sends a Get Message command to the IPMC to retrieve the message from the receive message queue. The Get Message command returns the data in Table 38.

Table 38. Returned Values from the Get Message Command

Byte	Data	Value	Comments
1	Completion Code	00h	
2	Channel	40h	Administrator privilege, Channel 0 (IPMB 0)
3	NetFN/rsLUN	C2h	NetFn=30h, Responder LUN=02h (SMS)
4	Header Checksum	3Eh	2's complement of the previous byte (chk1)
5	IPMC Address	(varies)	Board's IPMB address (depends on slot)
6	Sequence/rqLUN	04h	Sequence=01h, Requestor LUN=00h (IPMB)
7	Command	10h	RadiSys command for shutdown/reboot
8	Data	02h	Reboot action
9	Data Checksum	5F	2's complement of the sum of the previous 4 bytes (chk2)

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

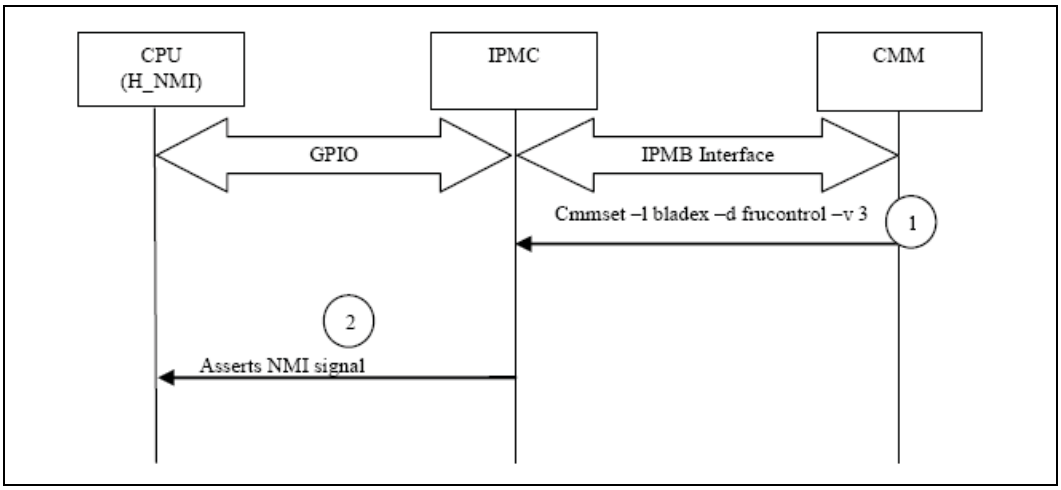
5.15.4 Diagnostic Interrupt

The following command provides the capability for an end user to issue a non-maskable interrupt (NMI) to the payload.

When issued, the NMI signal to the processor is asserted. To fully utilize the support of this command, the user needs to have an NMI handler installed.

The implementation details are shown in Figure 31.

Figure 31. Diagnostic Interrupt Command Implementation



The sequence of actions is as follows:

1. The CMM sends a frucontrol=3 command to the IPMC initiating a diagnostic interrupt.
2. When the IPMC receives frucontrol=3, it asserts the NMI signal to the CPU via the GPIO pins connected to the NMI pin.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.16 OEM IPMI Commands

This section documents the OEM style IPMI commands implemented and supported on the MPCBL0040. The commands are described in the following tables:

- Table 39, “RadiSys OEM Commands (Net Function 0x06h)” on page 118
- Table 40, “RadiSys OEM Commands (Net Function 0x08h)” on page 119
- Table 41, “RadiSys OEM Commands (Net Function 0x30h)” on page 120
- Table 42, “RadiSys OEM Commands (Net Function 0x32h)” on page 130

Table 39. RadiSys OEM Commands (Net Function 0x06h)

Net Function = Application (0x06), LUN = 00			
Code	**Command**	**Request, Response Data**	**Description**
01h	Get Device ID	Per the IPMI 2.0 specification	Platform-specific response fields: Byte 2 (Device ID) – 0x20 Byte 3 (Device revision) – 0x01 Byte 4 (Firmware Revision 1) • bit 7 – Device Available: 0 – Normal operation 1 – Update mode • bits 6:0 – Major Firmware Revision Byte 5 (Firmware Revision 2) Byte 6 (IPMI version) – 0x02 Byte 7 (Additional Device Support) – 0xBF • bit 7: Chassis device • bit 6: Bridge • bit 5: IPMB Event Generator • bit 4: IPMB Event Receiver • bit 3: FRU Inventory Device • bit 2: SEL Device • bit 1: SDR Repository Device • bit 0: Sensor Device Bytes 8:10 (manufacturer ID) – 343 (57h, 01h, 00h) Byte 11: (product ID 1) – 0x0C (MPCBL0040) Byte 12: (product ID 2) – 0x08 (EID/MCPD Block) Byte 13: (Boot Block Revision 1) Byte 14: (Boot Block Revision 2) Byte 15: (Firmware Build Number) Byte 16: (Reserved) – 0x00

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 40. RadiSys OEM Commands (Net Function 0x08h)

Net Function = Firmware Transfer Requests and Response (0x08), LUN = 00			
Code	**Command**	**Request, Response Data**	**Description**
00h	Reserved		
04h	Reserved		
10h	Retry Power On	Request: Byte 1 – 57h (Internet Assigned Numbers Authority [IANA] number for RadiSys, 0x000157) Byte 2 – 01h Byte 3 – 00h Byte 4 – Retry flag setting: • 00h – Disable • 01h – Enable • none – reading the value Response: Byte 1 – Completion Code Byte 2 – 57h (IANA number for RadiSys, 0x000157) Byte 3 – 01h Byte 4 – 00h Byte 5 – optional: read value	This command enables or disables the power on retry flag. Boards with TA (Top Assembly) D24178-007 or below have small percentage chance that they will not power on with an AMC or RTM installed. If this occurs, one workaround is to enable this Retry Power On IPMI command. When the retry flag setting is enabled, the IPMC firmware will monitor the power state of the board and if it fails, it will retry turning on the power up to 10 times. When writing the retry flag setting, the request data has to be 4 bytes size. The response data size is then 4 bytes. When reading the retry flag setting, the size of request has to be 3 bytes. The response data size is then 5 bytes equal, where last (5) byte determines value of flag.
20h	Reserved		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 41. RadiSys OEM Commands (Net Function 0x30h) (Sheet 1 of 10)

Net Function = Promentum General Application (0x30), LUN = 00			
Code	**Command**	**Request, Response Data**	**Description**
01h	Change BIOS Boot Flash	**Request**: Byte 1 – BIOS checksum success/failure indication • 00h – Checksum success (selects main flash) • 01h – Checksum failure (resets and selects other flash image) **Response**: Byte 1 – Completion Code	Changes the BIOS flash image that is loaded.
02h	Set Fabric Interface Requested Selection	**Request**: Byte 1 – 57h (Internet Assigned Numbers Authority [IANA] number for RadiSys, 0x000157) Byte 2 – 01h Byte 3 – 00h Byte 4 – Fabric Ethernet Interface setting: • 00h – Disabled • 01h – Front Panel • 02h – Backplane • FFh – Don't change setting • 03h…FEh – Reserved **Response**: Byte 1 – Completion Code Byte 2 – 57h (IANA number for RadiSys, 0x000157) Byte 3 – 01h Byte 4 – 00h	This command sets the Ethernet port direction for Ports E & F as specified in the request data bytes. Settings made by this command are persistent until explicitly cleared, including board removal from system. The interface selection is independent of the E-Keying status. A board reboot is required for Ethernet port direction change to take effect.
03h	Get Fabric Interface Requested Selection	**Request**: Byte 1 – 57h (IANA number for RadiSys, 0x000157) Byte 2 – 01h Byte 3 – 00h **Response**: Byte 1 – Completion Code Byte 2 – 57h (RadiSys IANA 0x000157) Byte 3 – 01h Byte 4 – 00h Byte 5 – Fabric Ethernet Interface setting • 00h – Disabled • 01h – Front Panel • 02h – Backplane • 03h…FFh – Reserved	This command returns the "requested" Ethernet channel port direction selection for Ports E & F.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 41. RadiSys OEM Commands (Net Function 0x30h) (Sheet 2 of 10)

Net Function = Promentum General Application (0x30), LUN = 00			
Code	**Command**	**Request, Response Data**	**Description**
04h	Get Fabric Interface Actual Selection	**Request**: Byte 1 – 57h (IANA number for RadiSys, 0x000157) Byte 2 – 01h Byte 3 – 00h **Response**: Byte 1 – Completion Code Byte 2 – 57h (IANA number for RadiSys, 0x000157) Byte 3 – 01h Byte 4 – 00h Byte 5 – Fabric Ethernet Interface setting: • 00h – Disabled • 01h – Front panel • 02h – Back plane • 03h...FFh – Reserved	This command returns the Ethernet channel port "routing" selection as actually routed. Due to E-keying selection of the Back Plane, it may not be permissible.
05h	Reserved	N/A	
06h	Reserved	N/A	

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 41. RadiSys OEM Commands (Net Function 0x30h) (Sheet 3 of 10)

Net Function = Promentum General Application (0x30), LUN = 00			
Code	**Command**	**Request, Response Data**	**Description**
07h	Get Version Data	**Request**: Byte 1 – None **Response**: Byte 1 – Completion code Byte 2 – Type/Length • 02h – Two bytes Byte 3 – IPMC Boot Block Revision 1 (Binary) Byte 4 – IPMC Boot Block Revision 2 (BCD) Byte 5 – Type/Length • 03h – Three bytes Byte 6 – IPMC firmware (FW) revision 1 (Binary) Byte 7 – IPMC firmware revision 2 (BCD) Byte 8 – IPMC firmware build (Binary) Byte 9 – Type/Length • 01h – One byte Byte 10 – FPGA version/revision • bits 7:4 – Version bits • bits 3:0 – Revision bits Byte 11 – Type/Length • 01h – One byte Byte 12 – Board version • bit 7 – SBC 0b – MPCBL0020 Board 1b – MPCBL0040 Board • bits 6:4 – Version bits • bits 3:0 – Revision bits Byte 13 – Type/Length • 03h – Three bytes Byte 14 – Staged IPMC FW revision 1 (Binary) Byte 15 – Staged IPMC FW revision 2 (BCD) Byte 16 – Staged IPMC FW build (Binary) Byte 17 – Type/Length • 03h – Three bytes Byte 18 – Rollback IPMC FW revision 1 (binary) Byte 19 – Rollback IPMC FW revision 2 (BCD) Byte 20 – Rollback IPMC FW build (Binary)	This command returns the boot and operational, staged, rollback firmware versions and the FPGA version information in the format required by the FRU OEM MRA definition for this platform. Type/Length Format: Bits Value Meaning 7:6 00 Binary/unspecified 01 BCD 10 6 bit ASCII, packed 11 8 bit ASCII
08h	BoardCPUStartUpPause/AMCStartupPause - Get Status	Described in the next chapter	
09h	BoardCPUStartUpPause/AMCStartupPause - SEt Status	Described in the next chapter	

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 41. RadiSys OEM Commands (Net Function 0x30h) (Sheet 4 of 10)

Net Function = Promentum General Application (0x30), LUN = 00			
Code	**Command**	**Request, Response Data**	**Description**
0Ah	AMC Fabric Interface Selection	**Request**: Byte 1 - Selection Command 00h - Set AMC Fabric Interface Selection 01h - Get AMC Fabric Interface Selection Byte 2 - Fabric Ethernet Interface Selection 00h - Baseboard GbE to Fabric Interface 01h - AMC GbE to Fabric Interface 02h…FFh - reserved. **Response**: Byte 1 - Completion Code Byte 2 - Selection Command 00h - Set AMC Fabric Interface Selection 01h - Get AMC Fabric Interface Selection Byte 3 - Actual Fabric Ethernet Interface Setting 00h - Baseboard GbE to Fabric Interface 01h - AMC GbE to Fabric Interface 02…FFh - reserved.	This command supports setting or retrieving the AdvancedMC Fabric Interface Ethernet® selection to the AdvancedTCA backplane as specified in the request data bytes. Settings made by this command are persistent. The interface selection is independent of the E-Keying status. On sets, the response contains AdvancedMC mux selection after setting the state. If there is a problem encountered in setting the state of the mux, the response will return the actual setting and not the requested setting.
1Ch	Reserved	N/A	
18h - 20h	Reserved	N/A	
21h	Get DIMM State	**Request**: Byte 1 – DIMM Group ID **Response**: Byte 1 – Completion code Byte 2 – DIMM Group Presence • bits 7:1 – Reserved • bit 0 – Presence (1 = group present) Byte 3 – Bitmap of DIMM slot existence Byte 4 – Bitmap of DIMM failure state Byte 5 – Bitmap of DIMM disabled state Byte 6 – Reserved Byte 7 – Bitmap of DIMM presence state	This command allows the *presence, disabled*, *failure*, and *spared* state of a set of DIMMs to be obtained without having to know the IPMC IPMI sensor numbers of the associated DIMM sensors. The state is returned as bitmaps. A bit being set in a bitmap indicates assertion of the state. The DIMM that a bit offset refers to is platform dependent. The DIMM Group Selector value is platform dependent. Platforms with 8 or fewer DIMMs should always use 0 as the Group Selector value. On platforms with memory boards, the Group Selector maps to a board number which is 1 based.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 41. RadiSys OEM Commands (Net Function 0x30h) (Sheet 5 of 10)

Net Function = Promentum General Application (0x30), LUN = 00			
Code	**Command**	**Request, Response Data**	**Description**
22h	Set DIMM State	**Request**: Byte 1 – DIMM Group Selector • bits 7:1 – Group Id • bit 0: – Presence (1 = group present) Byte 2 – Bitmap of DIMM slot existence Byte 3 – Bitmap of DIMM failure state Byte 4 – Bitmap of DIMM disabled state Byte 5 – Reserved Byte 6 – Bitmap of DIMM presence state **Response**: Byte 1 – Completion code	This command allows the failure state of a set of DIMMs to be set. Executing this command causes the associated sensor offsets for affected DIMM sensors. The DIMM Group Id is defined the same as for the Get DIMM State command. The IPMC will accept a variable number of request bytes: as few as 1 bytes of this command (Group selector) up to the fully defined set. Note that the Group/Board Presence flag is ignored on platforms that don't implement removable groups (memory boards). Example of the Slot Existence bitmap: Byte 2 = 0Fh and byte 6 = 0Dh means DIMM 1,3 and 4 are present, the DIMM 2 slot is empty. DIMM slots 5,6,7 and 8 do not exist on this platform.
23h	ReArm DIMMs	**Request**: N/A **Response**: Byte 1 – Completion code	This command causes the DIMM failure and disabled state of all DIMM sensors to be reset.
24h	Reserved	N/A	
25h	SyncSMBus	**Request**: Byte 1 – Action • 0 – Release SMBus ownership • 1 – Acquire SMBus ownership **Response**: Byte 1 – Completion code	This command is used to synchronize IPMC and BIOS access to the SMBus. When the BIOS has SMBus ownership, the IPMC will not access the bus. The BIOS will not access the bus unless it has acquired ownership using this command. The BIOS will need to acquire ownership to access SMBus devices such as DIMM SPD FRUs, and clock chips.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 41. RadiSys OEM Commands (Net Function 0x30h) (Sheet 6 of 10)

Net Function = Promentum General Application (0x30), LUN = 00			
Code	**Command**	**Request, Response Data**	**Description**
28h	Set Processor State	**Request**: Byte 1 – Processor ID Valid values are 0:N-1, where N is the number of processors supported by the platform. Byte 2,3 – Processor state to set This is a bit mask identifying the sensor offsets to set in the associated processor status sensor maintained by the IPMC. The offsets are as defined in the IPMI 1.5 specification. The following offsets are supported: • 0 – IERR • 1 – Thermal Trip • 2 – FRB1/BIST Failure • 3 – FRB2/POST Hang Failure • 4 – FRB3/Processor Startup Failure • 5 – Configuration Error • 6 – SMBIOS Uncorrectable CPU-complex error • 8 – Processor Disabled Byte 4 – Action This byte specifies the action to take after setting the processor status sensor state as requested. It is a bit-mask and multiple actions may be set. • bits 7:1 – Reserved • bit 0 – reset system **Response**: Byte 1 – Completion code	This command allows processor fault state to be asserted and an action to be taken afterwards. Asserting some fault states may cause the IPMC to generate SEL events (depending on the SDR configuration). Processor disabling will not take effect until the next reset.
29h	Get Processor State	**Request**: Byte 1 – Processor ID Valid values are 0:N-1, where N is the number of processors supported by the platform. **Response**: Byte 1 – Completion code Byte 2,3 – Processor state These bytes contain the associated Processor Status sensor's 2-byte event assertion status as defined in the IPMI 1.5 specification.	This command returns the current Processor Status sensor event assertion status for the requested processor. This command allows the caller to get processor state without having to know the IPMI sensor numbers of the Processor Status sensors.
2Ah	ReArm Processors	**Request**: N/A **Response**: Byte 1 – Completion code	This command clears all error and disabled state for all processors. Processor/terminator presence is not affected. Disabled processors are not actually run until the next system reset.
2Bh	Disable FRB2 Action	**Request**: N/A **Response**: Byte 1 – Completion code	This command disables resets associated with the watchdog timer expiring with an FRB2 reason.
30h-32h	Reserved	N/A	
41h	Set System GUID	**Request**: Bytes 1-16 – System GUID **Response**: Byte 1 – Completion code	This command sets the System GUID retrieved per the format of the IPMI 1.5 *Get System GUID* command. This value is stored persistently.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 41. RadiSys OEM Commands (Net Function 0x30h) (Sheet 7 of 10)

Net Function = Promentum General Application (0x30), LUN = 00			
Code	**Command**	**Request, Response Data**	**Description**
42h-43h	Reserved	N/A	
47h	Reserved	N/A	
48h	Internal Platform Event Message	**Request**: Byte 1 – Generator ID Byte 2 – Event Message Revision (04h) Byte 3 – Sensor Type Byte 4 – Sensor Number Byte 5 – Event Dir / Event Type Byte 6 – Event Data 1 Byte 7 – Event Data 2 Byte 8 – Event Data 3 **Response**: Byte 1 – Completion code Byte 2 – Reserved Byte 3:4 – Record ID Byte 5:8 – Timestamp	This command provides a mechanism for the BIOS to log event messages and retrieve the record ID and timestamp of the event. This command can be used to correlate BIOS events with SEL events. The format of the request data is the same as for the Platform Event Message command (Sensor/Event net function, command number 02). See the IPMI 1.5 specification for details on the definition of the request data fields.
50h	Set SM Signal	**Request**: Byte 1 – Signal type: • 0Eh – Health LED • 0Fh – Out Of Service LED • 10h – Hot-Swap LED Byte 2 – Signal instance, zero based Byte 3 – Action: • 0 – Force De-asserted • 1 – Force Asserted • 2 – Revert Byte 4 – Optional value used by multi-value signals **Response**: Byte 1 – Completion code	This command allows the real-time state of certain output signals (for example, LEDs) to be set without losing the IPMC internal state associated with the signals. The command also allows the output signals to revert to their normal behavior. Certain signals take analog values or complex states. The fourth byte of the request is supported for these kinds of signals, for example, Fan Speed Control.
51h	Get SM Signal	**Request**: Byte 1 – Signal type: • 13h – Reset Button • 14h – Hot-Swap Handle Switch Byte 2 – Signal instance, zero based Byte 3 – Action: • 0 – Sample • 1 – Ignore • 2 – Revert **Response**: Byte 1 – Completion code Byte 2 – Signal value: • 0 – De-asserted • 1 – Asserted	This command allows the real-time state of certain input signals to be polled without changes in the signals to be acted on by the IPMC. The command also allows the input signals to revert to their normal behavior. Not all signals are supported by all platforms.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 41. RadiSys OEM Commands (Net Function 0x30h) (Sheet 8 of 10)

Net Function = Promentum General Application (0x30), LUN = 00			
Code	**Command**	**Request, Response Data**	**Description**
52h	Get Self Test History	**Request**: Byte 1 – Action: • 0 – Get First • 1 – Get Next **Response**: Byte 1 – Completion code Byte 2 – First byte of test result • FFh – No more results Byte 3 – Second byte of test result	This command retrieves stored self-test failures. Normal use is to first call with action of "Get First" then use "Get Next" for subsequent calls. If byte 2 of the response is ever 0xFF, all the results have been retrieved.
53h	FakeAMCRemoval	Described in the next subchapter.	
70h	Graceful OS Shutdown	**Request**: Byte 1 • bits 7:3 – Reserved • bits 2:0 – Shutdown Operation: 00h – No change (used to read shutdown command status) 01h – Power off using the OS Agent 02h – Reset using the OS Agent 03h-07h – Reserved **Response**: Byte 1 – Completion code Byte 2 – Only for command status • bits 7:2 – Reserved • bits 1:0 – Shutdown command status 00h – Operation Successful 01h – Operation Failed (no OS agent) 02h – Operation in progress 03h – Reserved	This command performs graceful shutdown using OS agent.
80h-81h	Reserved	N/A	
82h	Get ACPI Configuration Mode	**Request**: N/A **Response**: Byte 1 – Completion code Byte 2 – ACPI Configuration state • bits 7:1 – Reserved • bit 0 – ACPI Mode: 0 = IPMC is in Legacy mode 1 = IPMC is in ACPI mode	
83h	Set ACPI Configuration Mode	**Request**: Byte 1 – ACPI Configuration state • bits 7:1 – Reserved • bit 0 – ACPI Mode 0 = Legacy mode 1 = ACPI mode Byte 2 – ACPI Configuration Mask • bits 7:1 – Reserved • bit 0 – ACPI mode mask 1 = set ACPI mode **Response**: Byte 1 – Completion code	
84h	Reserved	N/A	
86h - 88h	Reserved	N/A	

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 41. RadiSys OEM Commands (Net Function 0x30h) (Sheet 9 of 10)

Net Function = Promentum General Application (0x30), LUN = 00			
Code	**Command**	**Request, Response Data**	**Description**
A0h - A8h	Reserved	N/A	
B0h- B4h	Reserved	N/A	
C2h- C3h	Reserved	N/A	
E6h	Get NMI/ INIT Source	**Request**: N/A **Response**: Byte 1 – Completion code Byte 2 – NMI/INIT Source 1: • bits 7:6 – Reserved • bit 5 – Processor Thermal Trip [1, 2] • bit 4 – Processor IERR [1, 2] • bit 3 – Chassis Control Command • bit 2 – Event (PEF) • bit 1 – Watchdog NMI/Diagnostic Interrupt • bit 0 – Diagnostic Interrupt (FP NMI) Button Byte 3 – NMI/INIT Source 2: • bits 7:4 – Reserved • bit 3 – Chipset NMI [1] • bit 2 – South Bridge NMI [1] • bit 1 – PCI SERR/PERR [1] • bit 0 – Multi-bit Memory Error [1]	This command returns the IPMC's understanding of the source of the latest NMI/INIT assertion. The source information is a composite of IPMC detected sources (Source 1) and externally detected sources (Source2). Although multi-bit memory error is in the external source byte, on some platforms, this may be detected by the IPMC. The source 1 and 2 values are cleared when read and when the system is reset or powered off. [1] Only supported on IA32 systems [2] Support is platform specific

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 41. RadiSys OEM Commands (Net Function 0x30h) (Sheet 10 of 10)

Net Function = Promentum General Application (0x30), LUN = 00			
Code	**Command**	**Request, Response Data**	**Description**
EDh	Set NMI/ INIT Source	**Request**: Byte 1 – • bits 7:4 – Reserved • bit 3 – Chipset NMI [1] • bit 2 – South Bridge NMI [1] • bit 1 – PCI SERR/PERR [1] • bit 0 – Multi-bit Memory Error [1] **Response**: Byte 1 – Completion code	This command merges the given values in with any NMI/INIT sources detected by the IPMC. The values given here will be read by the next *Get NMI/INIT Source* command. This command also causes the IPMC to generate an NMI/ INIT pulse for a supported source. [1] Only supported on IA32 systems
F7h	NMI/INIT Enable / Disable	**Request**: Byte 1 – NMI/INIT enable state • 0 = Disable IPMC NMI/INIT generation • 1 = Enable IPMC NMI/INIT generation **Response**: Byte 1 – Completion code	This command is the master control for the IPMC NMI/INIT generation. The default state for NMI/INIT generation is enabled. The state set by this command is volatile, that is, it is not saved across AC power cycles.
FAh	Get Latest Post Code	**Request**: None **Response**: Byte 1 – Completion Code Byte 2 – Pre-Reset Port80 (byte n-4) Byte 3 – Pre-Reset Port80 (byte n-3) Byte 4 – Pre-Reset Port80 (byte n-2) Byte 5 – Pre-Reset Port80 (byte n-1) Byte 6 – Pre-Reset Port80 (last byte n) Byte 7 – Post-Reset Port80 (byte n-4) Byte 8 – Post-Reset Port80 (byte n-3) Byte 9 – Post-Reset Port80 (byte n-2) Byte 10 – Post-Reset Port80 (byte n-1) Byte 11 – Post-Reset Port80 (last byte n)	Returns two port80 signatures from before the last reset, and afterwards. The first signature contains the last 5 port80 bytes prior to the last payload reset event. The second signature contains the most current port80 bytes after the payload was reset.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 42. RadiSys OEM Commands (Net Function 0x32h)

Net Function = Promentum Platform Specific (0x32), LUN = 00			
Code	**Command**	**Request, Response Data**	**Description**
01h	Get HW Info	**Request:** N/A **Response**: Byte 1: Completion code Byte 2: Board version • bits 1:0 - Reserved • bits 3:2 - Fab revision bits • bits 6:4 - Fab version bits • bit 7 - 1=MPCBL0040, 0=MPCBL0020 Byte 3: FPGA version • bits 3:0 - Revision bits • bits 7:4 - Version bits	Provides version info of the SBC fab and FPGA.
02h	Get Power Unit Status	**Request:** N/A **Response:** Byte 1: Completion code Byte 2: Power State • 00h: Power is ON (ACPI State S0) • 05h: Power is OFF (ACPI State S5) • 20h: Legacy ON • 21h: Legacy OFF • [xx]: All others reserved. Byte 3: Power Status • bit 0: Power Cycle • bit 1: Control Fault • bits 7:2 : reserved Byte 4: Power Fault 1 • bit 0: 1.1 V Standby power fault • bit 1: 1.5 V Standby power fault • bit 2: 1.8 V Standby power fault • bit 3: 3.3 V Standby power fault • bit 4: 5 V Standby power fault • bit 5: 12 V power fault • bit 6: 5 V power fault • bit 7: 3.3 V power fault Byte 5: Power Fault 2 • bit 0: 1.2 V Power fault • bit 1: 1.5 V Power fault • bit 2: 1.8 V Power fault • bit 3: 1.8 V LAN Power fault • bit 4: 1.1 V Power fault • bit 5: 1.05 V Power fault • bit 6: CPU 0 Power fault • bit 7: CPU 1 Power fault	Provides the status of the payload power and corresponding power unit faults from the FPGA.
03h	Reserved	N/A	
55h	Reserved	N/A	
57h	Reserved	N/A	
5Fh	Reserved	N/A	

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.17 Auxiliary OEM IPMI Commands

The sections below describe auxiliary commands for the Intelligent Platform Management Controller (IPMC) code. These commands assist Advanced Mezzanine Card (AMC) and Rear Transition Module (RTM) development.

5.17.1 Pausing Board CPU Startup

Some AMC hardware needs to be initialized before the MPCBL0040 BIOS tries to enumerate the PCI devices. To make sure this happens in the right order, the MPCBL0040 IPMC can be made to wait a defined amount of time between enabling the payload power and starting the BIOS. The following commands provide this control.

Table 43. Net Function = Promentum Platform Specific (0x30), LUN = 00

Net Function = Promentum Platform Specific (0x30), LUN = 00			
Code	**Command**	**Request, Response Data**	**Description**
08h	Get Status	**Request:** Byte 1: Feature ID LSB (0x9) Byte 2: Feature ID MSB (0x0) Byte 3: WaitForMod Cmd • bit 1: get FRU id mask • bit 2: get boot timeout in seconds • bit 3: get boot delay in seconds **Response:** Byte 1: Completion code Byte 2, 3: FRU ID mask, where: • 0x02 coresponds to RTM • 0x04 coresponds to AMC or seconds	Provides the current status of the Wait For Modules facility.
09h	Set Status	**Request:** Byte 1: Feature ID LSB (0x9) Byte 2: Feature ID MSB (0x0) Byte 3: WaitForMod Cmd • bit 1: set FRU id mask • bit 2: set boot timeout in seconds • bit 3: set boot delay in seconds Byte 4: Feature Cmd Data FRU ID mask, where: • 0x02 coresponds to RTM • 0x04 coresponds to AMC or seconds **Response:** Byte 1: Completion code	Use this command to set the mask of FRU IDs to wait on and the number of seconds to wait.

Examples:

To set a wait time for the RTM:

```
cmmset -l bladeN -d ipmicommand -v "0x30 0x09 0x09 0x00 0x01 0x02"
```

To set a wait time for the RTM and AMC:

```
cmmset -l bladeN -d ipmicommand -v "0x30 0x09 0x09 0x00 0x01 0x06"
```

To set the boot timeout to 180 seconds:

```
cmmset -l bladeN -d ipmicommand -v "0x30 0x09 0x09 0x00 0x02 180"
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

To set the boot delay to 60 seconds:

```
cmmset -l bladeN -d ipmicommand -v "0x30 0x09 0x09 0x00 0x03 60"
```

To check the current settings:

```
cmmset -l bladeN -d ipmicommand -v "0x30 0x08 0x09 0x00 0x01"

cmmset -l bladeN -d ipmicommand -v "0x30 0x08 0x09 0x00 0x02"

cmmset -l bladeN -d ipmicommand -v "0x30 0x08 0x09 0x00 0x03"
```

5.17.2 Pausing FRU Startup: AMCStartupPause

A problem in developing the AMC or RTM lies with trying to use the Renesas* hardware debugger. The target hardware must be powered on before the debug environment can be set up. However, when the MPCBL0040 IPMC sees the module and powers it on, it immediately tries to read its FRU and SDR information and get it ready to run. By the time that the hardware debugger is set up and ready to run, the IPMC has timed out. The commands described here allow developers to make the IPMC wait instead of immediately communicating with the module, allowing time for the debugger to become ready.

When AMCStartupPause is enabled, the management power is turned on normally when the AMC or RTM is inserted, but the IPMC does not start requesting FRU or SDR information from the module. Once a trigger message is received, communication proceeds.

The messages are in the RadiSys OEM command set NetFn=0x30, using Cmd=0x08 for querying and Cmd=0x09 for setting and triggering. The command descriptions are as follows.

Table 44. Net Function = Promentum Platform Specific (0x30), LUN = 00

Net Function = Promentum Platform Specific (0x30), LUN = 00			
Code	**Command**	**Request, Response Data**	**Description**
08h	Get Status	**Request:** Byte 1: Feature ID LSB (0xB) Byte 2: Feature ID MSB (0x0) Byte 3: Feature Cmd (0x0) Byte 4: Feature Cmd Data (0x0) **Response:** Byte 1: Completion code Byte 2: • 0 = disabled • 1 = enabled Byte 3: Trigger pending	Provides the the current status of the AMCStartupPauseSBC.
09h	Set Status	**Request:** Byte 1: Feature ID LSB (0xB) Byte 2: Feature ID MSB (0x0) Byte 3: Feature Cmd • 0: disable pause function • 1: enable pause function • 2: trigger FRU to start Byte 4: Feature Cmd Data • FRU ID for Cmd 2, otherwise 0 **Response:** Byte 1: Completion code	Use this command to turn on or off the pause feature, and to trigger the AMC startup sequence when the pause is enabled.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

5.17.3 Fake AMC Removal

To restart the IPMC<->MMC conversations from the beginning, the IPMC needs to see that the module has been removed and re-inserted. The FakeAMCRemoval command has been implemented to simulate this activity for the IPMC.

When the FakeAMCRemoval message is sent, the module "Presence bit" is forced to 0, indicating that the module has been removed. The IPMC shuts down the module's state machine. The next time the periodic AMCTimerCallback() is called, the "Presence bit" is tested again and found to be 1, restarting the connection.

Table 45. Net Function = Promentum Platform Specific (0x30), LUN = 00

Net Function = Promentum Platform Specific (0x30), LUN = 00			
Code	**Command**	**Request, Response Data**	**Description**
53h	Fake Removal	**Request::** Byte 1: FRU ID **Response:** Byte 1: Completion code	Force the SBC into thinking that the given FRU has been removed.

Examples:

To emulate AMC removal:

```
cmmset -l bladeN -d ipmicommand -v "0x30 0x53 0x02"
```

To emulate RTM removal:

```
cmmset -l bladeN -d ipmicommand -v "0x30 0x53 0x01"
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

6.0 BIOS Features

6.1 Introduction

The Promentum™ MPCBL0040 Single Board Computer uses a BIOS developed by RadiSys and AMI*, which is stored in flash memory and can be updated remotely or locally. In addition to the BIOS and BIOS Setup program, the flash memory contains POST and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code.

6.2 BIOS Flash Memory Organization

The MPCBL0040 SBC contains two Firmware Hub (FWH) devices (see Figure 1, “MPCBL0040 SBC Block Diagram” on page 16). The first one is the primary FWH, which holds the BIOS code that executes during POST. The second is the backup FWH, which recovers the system when the primary FWH is corrupted. The SST 49LF008A FWH includes a 1024 KByte symmetrical flash memory device. Internally, the device is grouped into sixteen 64 KByte overlay blocks that are individually erasable, lockable, and unlockable.

6.3 Complementary Metal-Oxide Semiconductor (CMOS) RAM

CMOS RAM is nonvolatile storage that stores data needed by the BIOS. The data consists of certain onboard configurable settings. The settings in the BIOS Setup menu are often called CMOS settings.

Note: The CMOS settings are not affected by the full discharge of the hold up capacitor as all settings are saved to non-volatile memory on the board.

6.4 Redundant BIOS Functionality

The MPCBL0040 SBC hardware has two flash devices for BIOS where redundant copies are stored. Logic to select the active BIOS device is connected to the IPMC. IPMC firmware selects the BIOS device to boot from.

By default, the firmware selects BIOS device FWH0. The BIOS executes code from this flash and performs checksum validation of its operational code. This checksum occurs in the boot block of the BIOS. If the boot block detects a checksum failure in the remainder of the BIOS, it notifies the IPMC of the failure. In the event of failure, the IPMC firmware:

1. Asserts the RESET pin on the processor.
2. Switches the flash device.
3. Deasserts the RESET pin on the processor, allowing BIOS to execute off the second flash device.
4. Logs a SEL event.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

6.5 Language Support

English is the only supported language.

6.6 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from the backup BIOS. Recovery mode is active when the BIOS checksum fails and notifies the IPMC to failover to the backup BIOS.

6.7 Fast Booting Systems

6.7.1 Quick Boot

Use of the following BIOS Setup program settings reduces the POST execution time.

In the Boot Menu:

- Disable Option - ROM(s) if customer configuration does not use IBA(PXE) boot.
- Enable Quick Boot bypasses memory count and the search for a removable drive.

Note: Quick Boot is enabled by default. The boot time may be so fast that some drives might be not be initialized at all. If this occurs, it is possible to introduce a programmable delay ranging from 0 to 35 seconds using the BIOS Setup program, IDE Configuration Submenu, Advanced Menu, IDE Detect Time Out feature.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

6.8 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and booting the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the “Enter” key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt is displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 46 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 46. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Password to Enter Setup	Password During Boot
None	Any user can change all options	Any user can change all options	None	None
Supervisor and User	Can change all options	Based on user access level: • No Access • View Only • Limited • Full Access	Supervisor or user	If the password check option is set to “Setup”, no password is required. Otherwise, a supervisor or a user password is required.
Supervisor Only	Can change all options	Based on user access level: • No Access • View Only • Limited • Full Access	Supervisor (for supervisor mode) or enter only (for user mode)	If the password check option is set to “Setup”, no password is required. Otherwise, a supervisor or a user password is required.
User Only	Can not get into supervisor mode until user password is cleared	Can change all options	User	If the password check option is set to “Setup”, no password is required. Otherwise, a supervisor or a user password is required.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

6.9 Remote Access Configuration

Remote access using serial console redirection allows users to monitor the MPCBL0040 SBC boot process and run the MPCBL0040 BIOS Setup from a remote serial terminal. Connection is made directly through a serial port.

The console redirection feature is useful in cases where it is necessary to communicate with a processor board in an embedded application without video support.

Note: The default settings used for console redirection to the serial port are 9600, n, 8, 1, and no flow control.

Table 47 shows the escape code sequences that may be useful for things like BIOS Setup if function keys cannot be directly sent from a terminal application.

Table 47. Function Key Escape Code Equivalents

Key	Escape Sequence	Notes
F1	ESC OP	
F2	ESC OQ	
F3	ESC OR	
F4	ESC OS	To enter BIOS Setup
F5	ESC OT	
F6	ESC OU	
F7	ESC OV	
F8	ESC OW	
F9	ESC OX	
F10	ESC OY	To save and exit BIOS Setup
F11	ESC OZ	
F12	ESC OI	PXE boot

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

6.10 Boot Device Priority

The default boot order is shown in Section 7.5.3, “Boot Device Priority Submenu” on page 167.

The boot device priority is stored in non volatile RAM (NVRAM), is static across reboots will not change except for in the following conditions:

- The user manually presses F4 during BIOS to enter BIOS Setup Menu, changes the Boot Device Priority and saves BIOS settings.
- After a user performs a BIOS update to the board and the user chooses to load the default BIOS setup. This will erase the current boot order in NVRAM and BIOS will automatically determine a new boot order upon next reboot of the board.
- If there is an error and no valid boot order stored in NVRAM.

As soon as the board boots one time, the boot order will be fixed until changed by the user. A manual save of boot order by user is not needed to fix the boot order.

Above mentioned NVRAM refers to a small portion of the FWH (Firmware Hub). When the NVRAM is empty or does not contain valid boot order information, the BIOS automatically determines a boot order upon next reboot. If a USB device is connected to the board when there is no boot order saved, the USB device will automatically be placed at the top of the boot order.

Once the boot order is static, if a hard drive or any other boot device is added (such as USB boot device), it will be added at the bottom of the boot order list.

If a boot device needs to be added for a single boot, then the user should press F3 during BIOS to bring up a pop up menu to select boot device.

If a boot device needs to be added as a permanent boot device, the user should re-order the boot devices in BIOS Boot Device Priority setup menu.

6.11 Progressive Boot Support

Progressive Boot is a feature added into the system to increase the availability of the system in the event of the primary boot device being corrupted or unbootable.

Taking into account that a user has configured the second/third boot device as a fail safe storage to store a recovery OS or a redundant OS image, the BIOS attempts to boot from the subsequent boot device as configured under the “Boot Device Priority Submenu”. See Section 7.5.3, “Boot Device Priority Submenu” on page 167 for details.

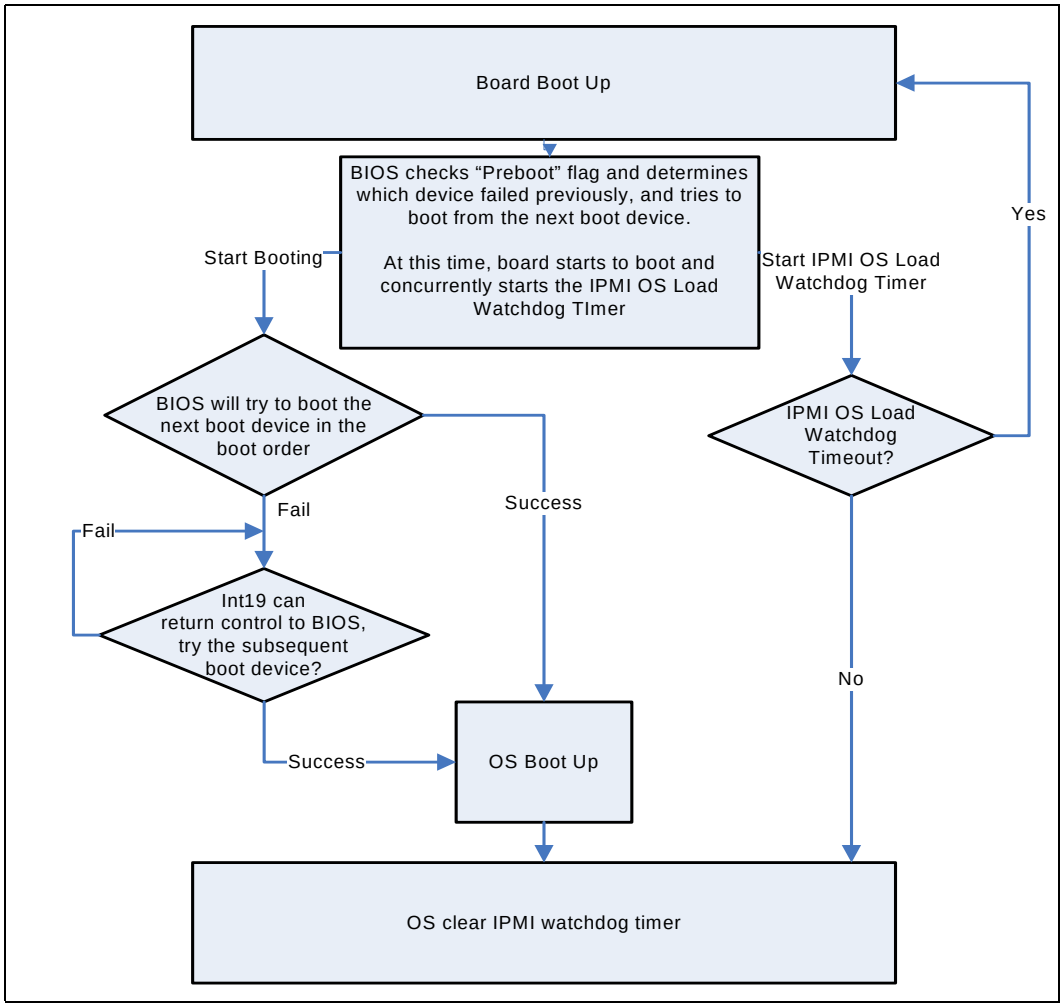
6.11.1 Progressive Boot Mechanism

Prior to OS boot process, the BIOS acquires the IPMI watchdog timer to determine whether the IPMI OS load flag has been expired. If the OS load flag has not been expired, then the IPMI watchdog timer for OS load will be turned on, and the BIOS tries to boot the first boot device in the boot order. If an OS encounters a boot failure and returns to BIOS, then the BIOS can try the next boot device in the boot order. But if an OS encounters a boot failure and does not return to BIOS, the IPMI watchdog timer times out and resets the board. In the next OS boot process, the BIOS checks the IPMI watchdog timer to see whether the OS load flag has expired. If the OS load flag has expired, then the IPMI watchdog timer for OS load is turned on, and the BIOS tries to boot the next boot device from the previous boot device that caused the IPMI watchdog timer to timeout.

Figure 32 shows the boot up sequence.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Figure 32. Boot Up Sequence



6.12 Diagnostics Boot Sequence Configuration

This boot menu is a one time boot menu designed specifically to boot the board to a service operating system diagnostic package to run hardware diagnostics on the board. One time boot menu means that it will boot from the device selected in this menu once and the very next power cycle, it will boot up using the standard boot device selection.

The boot location for the service operating system that has the board diagnostic package can be selected to boot from PXE, local HDD or local flash drive.

Through IPMI, the diagnostic configuration script supplied as part of the diagnostic package is used to configure the SBC BIOS to change the boot sequence. This allows the SBC to boot to the Service OS on the next boot only. The script, after successfully configuring the boot order, also power cycles the SBC.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

6.13 Pre-Defined Resources for AdvancedMC Modules

The AdvancedMC is hot swappable. In order to support AdvancedMC hot add, the MPCBL0040 SBC has to reserve resources that are not being used by a device when the SBC is booted. It is not possible for the SBC to know exactly what resources an AdvancedMC module that is hot added may require before it is inserted. If the resources reserved by the SBC for the AdvancedMC module are adequate, then the AdvancedMC hot add will be successful. If an AdvancedMC module needs more resources (memory, I/O space, etc.) than the SBC has reserved, then the AdvancedMC module will not work properly until the SBC is rebooted with the AdvancedMC module installed. If the hot added AdvancedMC module does not use all of the resources that are reserved by the SBC, then the reserved resources are left unused and cannot be used by another device because they are still reserved.

On the MPCBL0040 board, the BIOS reserves the following resources for the AdvancedMC hot plug slot:

- Bus = 8
- I/O space = 8 KB
- Prefetchable memory = 64 MB
- Non-prefetchable memory = 128 MB

These resources are reserved only if the AdvancedMC slot hot plug capability is enabled in the BIOS Setup menu. If AdvancedMC PCI express selection is set to Disabled (it is Enabled by default), then these resources are not allocated by the BIOS.

If an AdvancedMC module is installed before power up and recognized by the BIOS, then the resources required for that AdvancedMC module is determined and that information is available to the operating system upon boot.

Warning: AdvancedMC modules shall only be installed before board payload powers on or after the operating system has fully loaded. If an AdvancedMC module is hot added after the initial BIOS device discovery, but before the operating system is fully loaded, then the AdvancedMC module may not work properly. To correct this, a board payload reset or payload power cycle is required.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

6.14 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS setup and install an operating system that supports USB. Legacy USB support is enabled by default.

Note: Legacy USB support is for keyboards, mice, hubs and bootable devices like CD-ROM drives and floppy disk drives. Other USB devices are not supported in legacy mode.

Legacy USB support operates as follows:

1. When power is applied to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS, allowing a user to use a USB keyboard.
4. POST completes.
5. The operating system loads. USB keyboards and mice are recognized and may be used to configure the operating system. Keyboards and mice are not recognized during this period if legacy USB support was set to "Disabled" in the BIOS Setup program.
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system. Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that legacy USB support in the BIOS Setup program is set to "Enabled" and follow the operating system's installation instructions.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.0 BIOS Setup

7.1 Introduction

The BIOS Setup program can be used to view and change the BIOS settings for the SBC. The BIOS Setup program is accessed by pressing the F4 key (if connected via serial port) or Delete key (if connected via local USB keyboard) as soon as the BIOS starts booting. Table 48 lists the BIOS Setup program menu bar items.

Table 48. BIOS Setup Program Menu Bar

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit
Allocates resources for hardware components	Configures advanced chipset features	Configures PCI Plug and Play devices	Selects boot options	Sets passwords and security features	Configures chipset	Saves or discards changes to Setup program options

Table 49 lists the function keys available for menu screens.

Table 49. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (moves the cursor left or right)
<↑> or <↓>	Selects an item (moves the cursor up or down)
<Tab>	Selects a field (not implemented)
<Enter>	Executes command or selects the submenu
<F9>	Loads the default configuration values for the current menu
<F10>	Saves the current values and exits the BIOS Setup program
<Esc>	Exits the menu

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.2 Main Menu

To access this menu, select **Main** on the menu bar at the top of the screen. The Main menu options are described in Table 50.

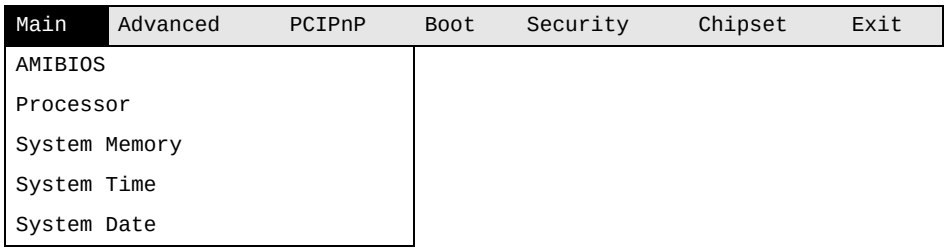


Table 50. Main Menu Options

Feature	Options	Description
BIOS ID	AMIBIOS version Build date ID	Displays the BIOS ID
Processor	Type Speed Count	Displays processor type, speed, and count
System Memory	Size	Displays system memory size of recognized DIMMs
System Time	Hour/minute/second	Specifies the current time
System Date	Day of week Month/day/year	Specifies the current date

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.3 Advanced Menu

To access this menu, select **Advanced** on the menu bar at the top of the screen.

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

- CPU Configuration
- IDE Configuration
- ACPI Configuration
- System Management
- PCI Configuration
- Diagnostics Boot Sequence Configuration
- Event Log Configuration
- PCI Express Configuration
- Ethernet Ports Direction Configuration
- Progressive Boot Configuration
- SMBIOS Configuration
- Remote Access Configuration
- USB Configuration

Under the Advanced menu, the following warning message appears:

> **"WARNING: Setting the wrong values in the sections that follow may cause system to malfunction."**

This is a warning message to users to not modify the settings unless they are familiar with the items. To restore factory defaults, select **Exit** on the menu bar, then select the **Load Optimal Defaults** item (see Table 7.8, "Exit Menu" on page 172).

Table 51 describes the **Advanced** menu, which sets advanced chipset features.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

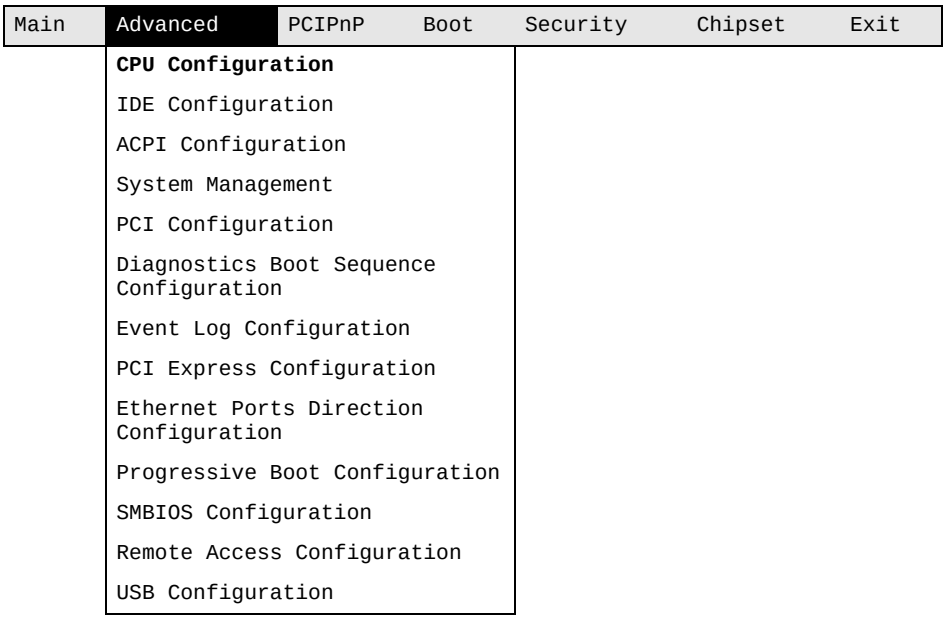
Table 51. Advanced Menu Options

Feature	Options	Description
CPU Configuration	Select to display submenu	Display CPU details, configure Intel SpeedStep® Mode and CPU features
IDE Configuration	Select to display submenu	Display primary IDE master, primary IDE slave drive, and IDE hard drive configuration
ACPI Configuration	Select to display submenu	Enable/disable ACPI support for OS and configure ACPI settings
System Management Configuration	Select to display submenu	Display FRU board and product information, IPMC device, and firmware information
PCI Configuration	Select to display submenu	Configure on-board PCI device settings (SAS controller, Gigabit Ethernet for base and fabric interface, and Fast Ethernet controller)
Diagnostics Boot Sequence Configuration	Select to display submenu	Configures the one time boot location when board diagnostics image is selected (PXE, local HDD or local flash drive)
Event Log Configuration	Select to display submenu	Mark, clear, or view event log Configure error logging supported by BIOS
PCI Express Configuration	Select to display submenu	Configure PCI Express support
Ethernet Ports Direction Configuration	Select to display submenu	Reports current setting of Ethernet Ports E & F; Allows user to change direction of Ethernet ports E & F Reports current setting of Ethernet Ports C & D; Allows user to change direction of Ethernet ports C & D This setting will only take effect after save and exit from BIOS Setup menu.
Progressive Boot Configuration	Select to display submenu	Configure progressive boot configuration
SMBIOS Configuration	Select to display submenu	Configure SMBIOS (SMI Support)
Remote Access Configuration	Select to display submenu	Set remote access type, serial port, serial port settings, and enable/ disable redirection after booting to MS-DOS
USB Configuration	Select to display submenu	Enable/disable USB devices and configure USB2.0 support

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.3.1 CPU Configuration Submenu

To access this submenu, select **Advanced** on the menu bar, then **CPU Configuration**. The CPU configuration options are given in Table 52.



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 52. CPU Configuration Submenu Options

Feature	Options	Description
Manufacturer		Display CPU manufacturer
Brand String		Display CPU brand string
Frequency		Display CPU frequency
FSB Speed		Display front side bus speed
Cache L1		Display L1 cache size
Cache L2		Display L2 cache size
Execute Disable Bit	**Enabled** Disabled	When disabled, force the XD feature flag to always return 0
Core Multi-Processing	**Enabled** Disabled	When disabled, disable one execution core
CPU TM Function	**Enabled** Disabled	Used to enable and disabled thermal monitoring
Virtualization Technology	Enabled **Disabled**	Used to enable and disable Virtualization Technology. After changing this, a board payload power cycle is required for this change to take affect.
DCU Prefetch	**Enabled** Disabled	Enables or disables hardware data cache unit (DCU) for L1 prefetch capabilities
Adjacent Cache-Line Prefetch	**Enabled** Disabled	Enables or disables hardware adjacent cache line for L2 prefetch capabilities
Data Prefetch Logic	**Enabled** Disabled	Enables or disables hardware data prefetch logic (DPL) for L2 prefetch capabilities
Intel SpeedStep® Technology	Maximum Speed Minimum Speed Automatic **Disabled**	Maximum: CPU speed is set to maximum Minimum: CPU speed is set to minimum Automatic: CPU speed controlled by OS Disabled: Default CPU speed
C-State Technology from Intel C1 Enable	**Enabled**/Disabled **Standard**/Enhanced	CPU idle is set to C1 state Enable specific C-state: • Disable = C-state disabled • Standard(Std) = Conventional C-state
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.3.2 IDE Configuration Submenu

To access this submenu, select **Advanced** on the menu bar, then **IDE Configuration**. The IDE configuration options are given in Table 53.

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

- CPU Configuration
- **IDE Configuration**
- ACPI Configuration
- System Management
- PCI Configuration
- Diagnostics Boot Sequence Configuration
- Event Log Configuration
- PCI Express Configuration
- Ethernet Ports Direction Configuration
- Progressive Boot Configuration
- SMBIOS Configuration
- Remote Access Configuration
- USB Configuration

Table 53. IDE Configuration Submenu Options

Feature	Options	Description
IDE Configuration	**P-ATA Only** Disabled	IDE Mode configuration for the 128 MByte Flash memory
Primary IDE Master	**Hard Disk**	Display the primary IDE master drive. While entering Setup, the BIOS auto-detects the presence of IDE devices. This displays the status of the auto detection of IDE devices.
Secondary IDE Master	**Hard Disk**	Display the secondary IDE master drive. While entering Setup, the BIOS auto-detects the presence of IDE devices. This displays the status of the auto-detection of IDE devices.
Hard Disk Write Protect	**Disabled** Enabled	Enable/disable hard disk device write protection. This is effective only if the device is accessed through the BIOS.
IDE Detect Time Out	0 5 10 15 20 25 30 **35**	Select the time out value in seconds for detecting ATA/ATAPI device(s)
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

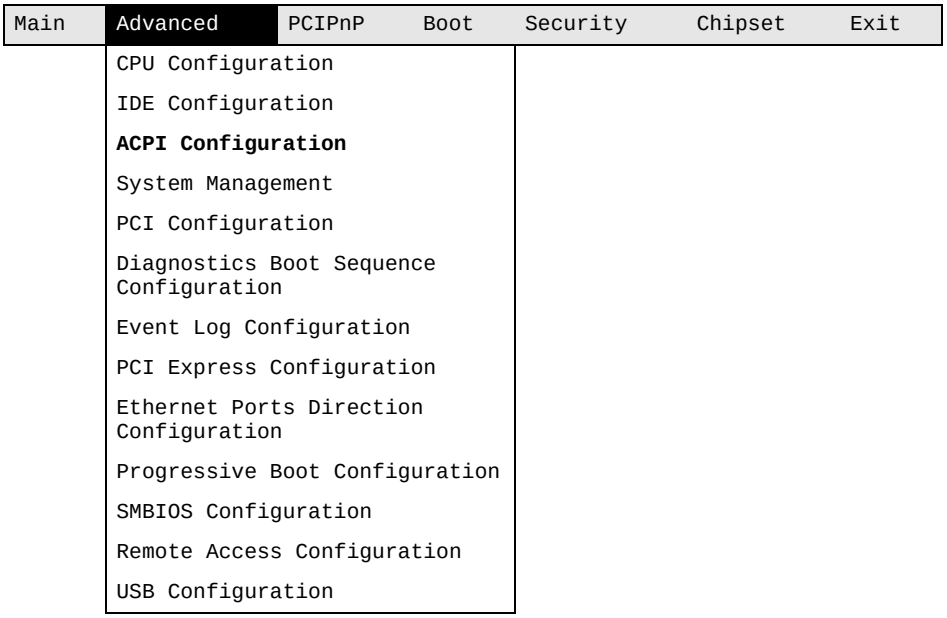
Table 54. Primary/Secondary IDE Master Submenu Options

Feature	Options	Description
Device		Display IDE device
Vendor		Display IDE vendor name
Size		Display IDE device size
LBA Mode		Display IDE LBA Mode status
Block Mode		Display IDE Block Mode status
PIO Mode		Display PIO Mode status
Async DMA		Display Async DMA status
Ultra DMA		Display Ultra DMA-5 status
S.M.A.R.T		Display S.M.A.R.T status
Type	Not installed **Auto** CD/DVD ARMD	Select the type of IDE device connected
LBA/Large Mode	Disabled **Auto**	Disable: Disable LBA ModeAuto Enable the LBA Mode if the device supports it and the device is not already formatted with LBA Mode disable
Block (Multi-Sector Transfer)	Disabled **Auto**	Disable: The data transfer from and to the device occurs one sector at a time. Auto: The data transfer from and to the device occurs multiple sectors at a time if the device supports it.
PIO Mode	**Auto** 0/1/2/3/4	Select PIO Mode
DMA Mode	**Auto** SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2	Select DMA Mode Auto: Auto detected SWDMAn: SingleWordDMAn MWDMAn: MultiWordDMAn
S.M.A.R.T	**Auto** Disabled Enabled	SMART stands for self-monitoring, analysis, and reporting technology Enable/disable S.M.A.R.T. Auto: Enable S.M.A.R.T if the device supports it
32 Data Transfer	**Disabled** Enabled	Enable/disable 32-bit data transfer
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.3.3 ACPI Configuration Submenu

To access this submenu, select **Advanced** on the menu bar, then **ACPI Configuration**.



There are two ACPI configuration submenus:

- **Advanced ACPI Configuration** submenu; see Table 55
- **Chipset ACPI Configuration** submenu; see Table 56

Table 55. Advanced ACPI Configuration Submenu Options

Feature	Options	Description
ACPI Version Features	**ACPI v1.0** ACPI v2.0 ACPI v3.0	Enable RSDP pointers to 64-bit Fixed System Description Tables
ACPI APIC Support	Disabled **Enabled**	Include ACPI APIC table pointer to RSDT pointer list
AMI OEMB Table	Disabled **Enabled**	Include OEMB table pointer to R(x)SDT pointer lists
Headless Mode	**Disabled** Enabled	Enable/disable Headless Operation mode through ACPI
Note: **Bold** text indicates default setting.		

Table 56. Chipset ACPI Configuration Submenu Options

Feature	Options	Description
APIC ACPI SCI IRQ	**Disabled** Enabled	Enable/disable APIC ACPI SCI IRQ
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.3.4 System Management Submenu

To access this submenu, select **Advanced** on the menu bar, then **System Management**. The system management options are given in Table 57.

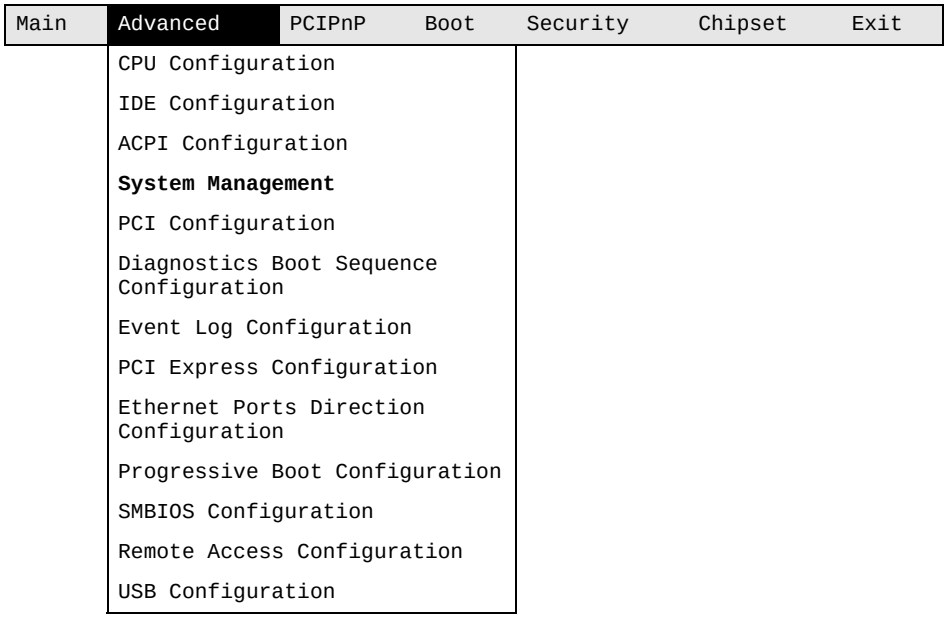


Table 57. System Management Configuration Submenu Options

Feature	Options	Description
FRU Board Information Area		Display FRU board information
Board Product Name		
Board Serial Number		
Board Part Number		
FRU Product Information Area		Display FRU product information
Product Name		
Product Part/Model		
Product Version Number		
Product Serial Number		
BMC Device and Firmware Information		Display BMC device and firmware information
BMC Device ID		
BMC Firmware Revision		
BMC Revision		
SDR Revision		
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.3.5 PCI Configuration Submenu

To access this submenu, select **Advanced** on the menu bar, then **PCI Configuration**. The PCI configuration options are given in Table 58.

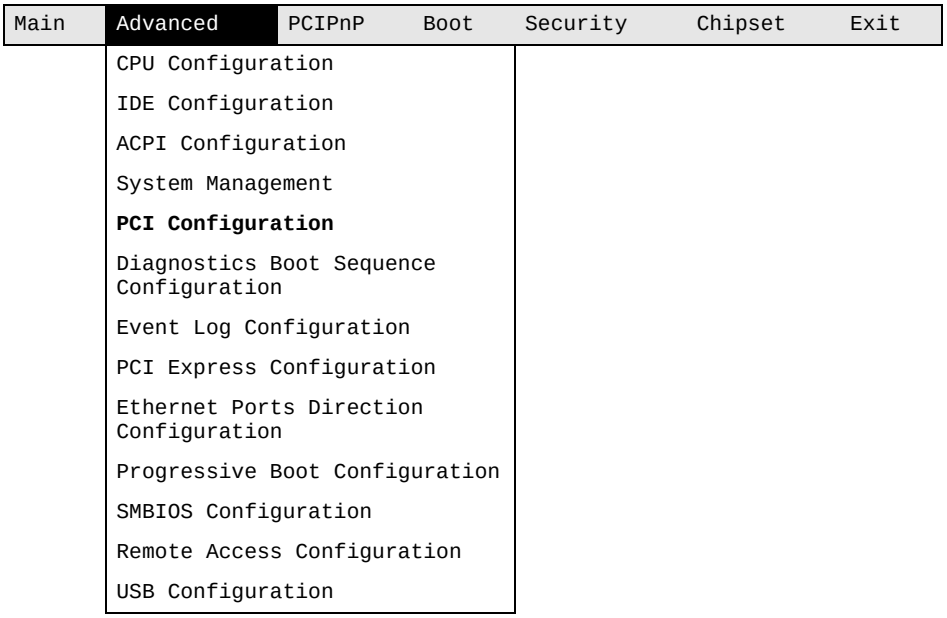


Table 58. On-Board PCI Device Settings

Feature	Options	Description
SAS Controller	Disabled **Enabled**	Enable/disable Option ROM for on-board SAS controller
Ethernet Controller (Ports A&B)	Disabled **Enabled**	Enable/disable Option ROM for Gigabit Ethernet LAN Controller Ports A & B (IBA GE Slot 0200 and 0201)
Ethernet Controller (Ports C&D)	Disabled **Enabled**	Enable/disable Option ROM for Gigabit Ethernet LAN Controller Ports C & D (IBA GE Slot 0300 and 0301)
Ethernet Controller (Ports E&F)	Disabled **Enabled**	Enable/disable Option ROM for Gigabit Ethernet LAN Controller Ports E & F (IBA GE Slot 0400 and 0401)
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 59. AMC & RTM Detection Time Out Setting

Feature	Options	Description
AMC M2 Timeout	2 Sec **5 Sec** 10 Sec No Wait	Selects the time out value for detecting M2 State before detecting M4 State. Selecting No Wait will skip M2 detection.
AMC M4 Timeout	2 Sec 5 Sec 10 Sec **30 Sec**	Selects the time out value for detecting M4 State before starting PCI enumeration.
RTM M2 Timeout	2 Sec **5 Sec** 10 Sec No Wait	Selects the time out value for detecting M2 State before detecting M4 State. Selecting No Wait will skip M2 detection.
RTM M4 Timeout	2 Sec 5 Sec 10 Sec **30 Sec**	Selects the time out value for detecting M4 State before starting PCI enumeration.
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.3.6 Diagnostics Boot Sequence Configuration Submenu

To access this submenu, select **Advanced** on the menu bar, then **Diagnostics Boot Sequence Configuration**. The diagnostics boot sequence configuration options are given in Table 60.

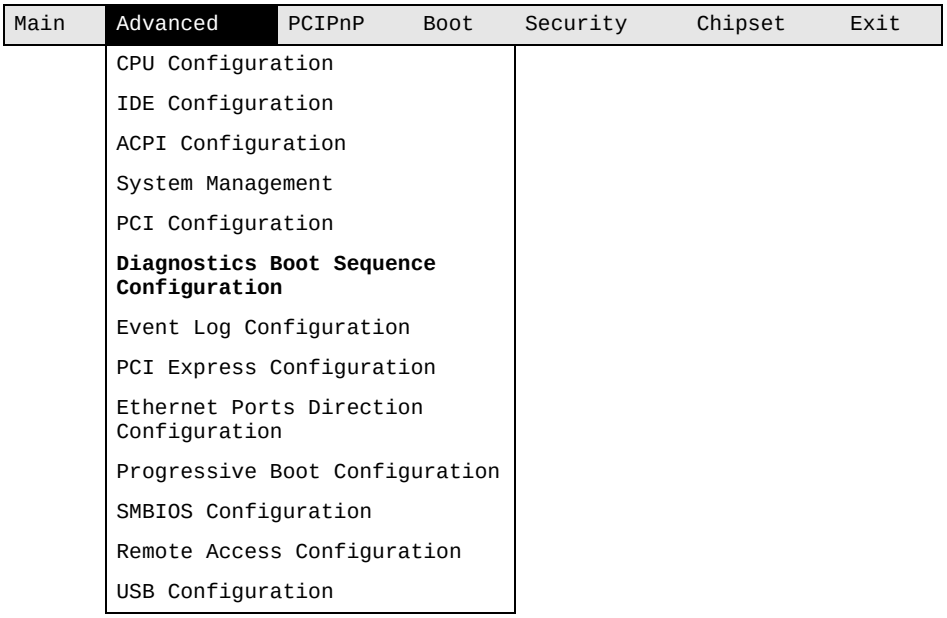


Table 60. Diagnostics Boot Sequence

Feature	Options	Description
Default PXE	Network: IBA GE Slot 0400 v1231 Network: IBA GE Slot 0401 v1231 Network: IBA GE Slot 0300 v1231 Network: IBA GE Slot 0301 v1231 **Network: IBA GE Slot 0200 v1231** Network: IBA GE Slot 0201 v1231 Disabled	Default PXE boot location for board diagnostic tests
Default Hard Drive	**SCSI: #508 ID00 LUN0** HDD: PM-128 MB ATA Flash Disk HDD: SM-128 MB ATA Flash Disk	Default hard drive location for board diagnostic tests The default is shown here with an HDD installed. If no HDD is installed, the default is HDD: PM-128 MB ATA Flash Disk.
Default Removable Drive	**Disabled**	Default removable drive location for board diagnostic tests (for example, USB drive). If the USB drive is installed, it becomes the default.
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.3.7 Event Logging Configuration Submenu

To access this submenu, select **Advanced** on the menu bar, then **Event Log Configuration**. The event logging configuration options are given in Table 61.

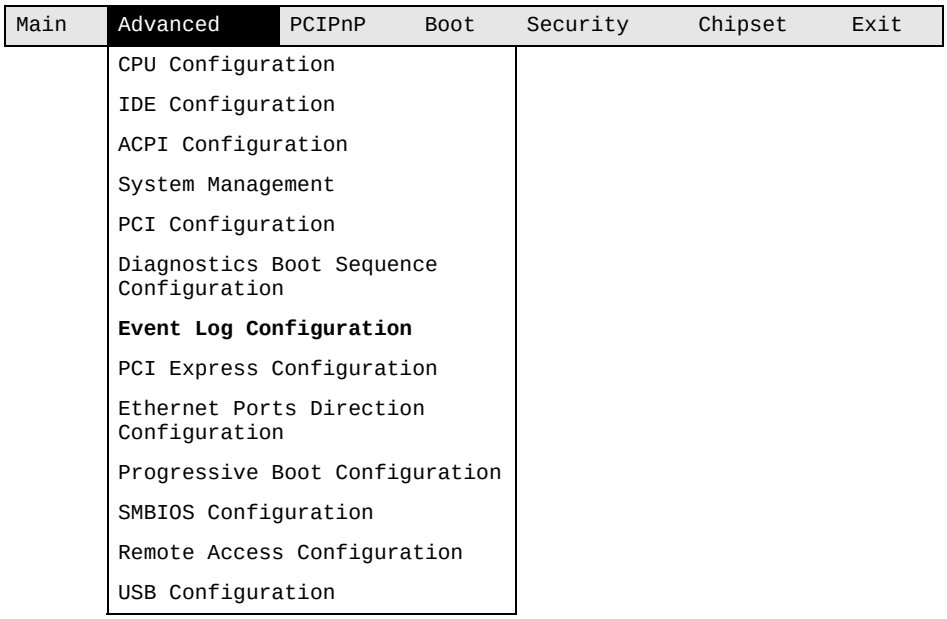


Table 61. Event Logging Configuration Submenu Options

Feature	Options	Description
Assert NMI on Fatal Error	Disabled **Enabled**	Enable/Disable NMI reporting on fatal error events
Clear Event Log		Discard all events in the event log. This event log is the local SEL (System Event Log) for the board.
ECC Event Logging	Disabled **Enabled**	Enable/disable ECC event logging
Hub Interface Event Logging	Disabled **Enabled**	Enable/disable Hub Interface event logging
System Bus Event Logging	Disabled **Enabled**	Enable/disable System Bus error logging
Memory Buffer Event Logging	Disabled **Enabled**	Enable/disable memory buffer event logging
PCI Error logging	Disabled **Enabled**	Enable/disable PCI error logging
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.3.8 PCI Express* Configuration Submenu

To access this submenu, select **Advanced** on the menu bar, then **PCI Express Configuration**. The PCI Express configuration options are given in Table 62.

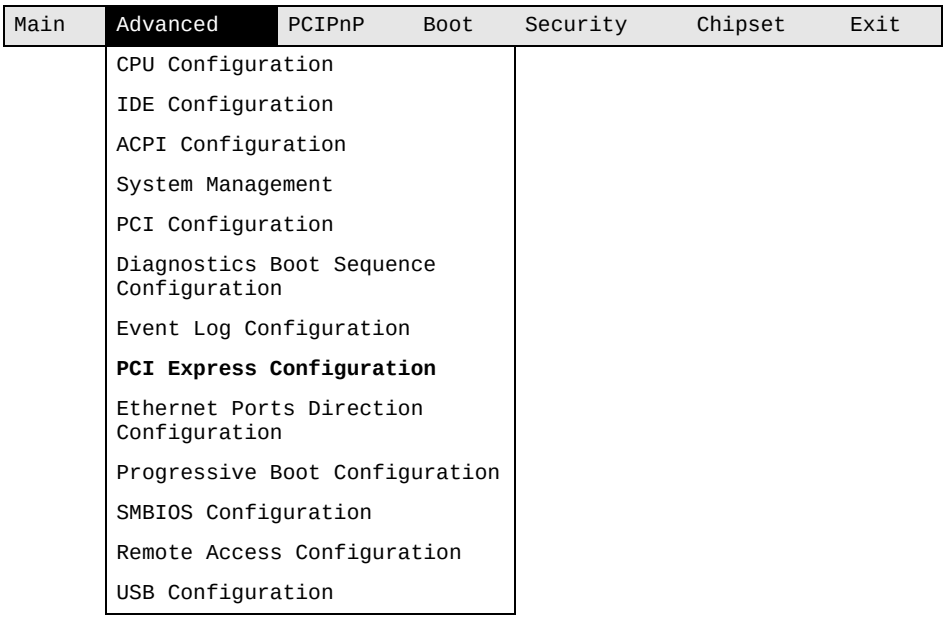


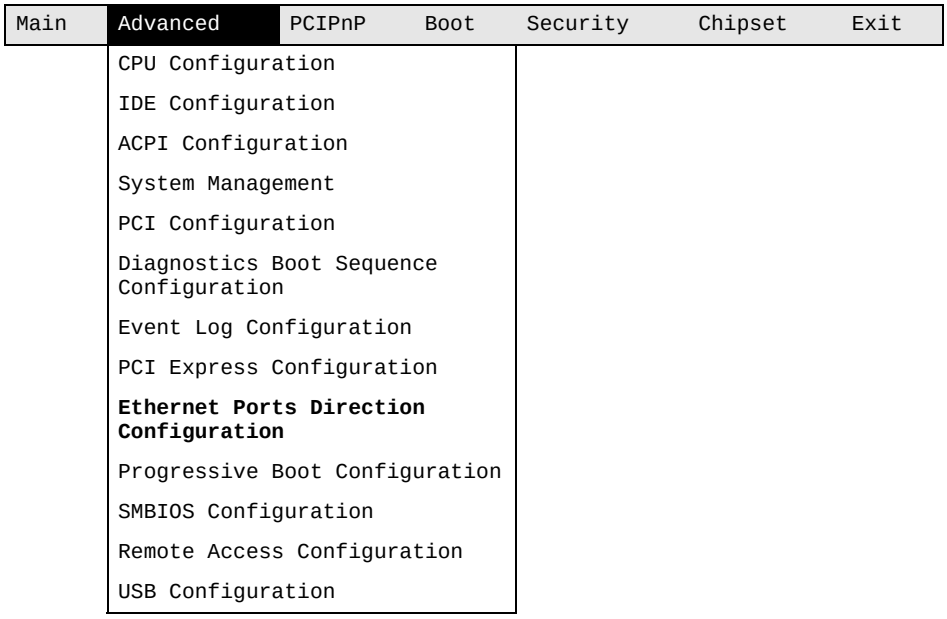
Table 62. PCI Express Configuration Submenu Options

Feature	Options	Description
Active State Power Management	**Disabled** Enabled	Enable/disable PCI Express L0s and L1 link power state
PCI Express Port A0	Auto **Enabled** Disabled	Auto: Visible if card exists Enable: Always visible Disable: Always hide
PCI Express Port A1	Auto **Enabled** Disabled	Auto: Visible if card exists Enable: Always visible Disable: Always hide
PCI Express Port B1	Auto **Enabled** Disabled	Auto: Visible if card exists Enable: Always visible Disable: Always hide
PCI Express Port C0	Auto **Enabled** Disabled	Auto: Visible if card exists Enable: Always visible Disable: Always hide
PCIe Jitter Tolerance	**Enabled** Disabled	Enable/disable PCI Express Jitter tolerance
PCIe Compliance Mode	**Disabled** Enabled	Enable/disable MCH entering PCI Express compliance mode
PIC Express Hot Plug on AdvancedMC	Disabled **Enabled**	Enable/disable PCI Express Hot Plug on AdvancedMC slot (EXPC0 of MCH)
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.3.9 Ethernet Ports Direction Configuration Submenu

To access this submenu, select **Advanced** on the menu bar, then **Ethernet Ports Direction Configuration**. The fabric interface routing configuration options are given in Table 63.



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 63. Change Fabric Interface Submenu Options

Feature	Options	Description
Current Eth Ports E&F Direction	**Front Panel**	Displays the current direction setting of Ethernet Ports E and F. Ethernet Ports E and F can be set to connect to the backplane (Fabric Interface) or Front Panel.
Change Eth Ports E&F Direction	**No** Yes	Change Fabric Interface Direction for Ethernet Ports E and F. Select Yes to switch between “Front Panel connection to Onboard Gb Ethernet Controller” and “Backplane connection to Onboard Gb Ethernet Controller”. The Ethernet port direction change is stored in IPMC non-volatile memory. BIOS will send the OEM IPMI command to the IPMC after choosing Save and Exit from the BIOS Setup Menu. If user discards changes before saving and exiting, IPMI command will not be sent and Ethernet port direction change will not occur.
Current Eth Ports C&D Direction	**Onboard GbE**	Displays the current direction setting of Ethernet Ports C and D. Ethernet Ports C and D can be set to connect to the backplane (Fabric Interface) by choosing Onboard GbE or the ports can be configured to connect from the AdvancedMC connector directly to the fabric interface.
Change Eth Ports C&D Direction	**No** Yes	Change Fabric Interface Direction for Ethernet Ports C and D. Select Yes to switch between “Onboard Gb Ethernet Controller connection to Backplane” and “AdvancedMC connection to Backplane”. The Ethernet port direction change is stored in IPMC non-volatile memory. BIOS will send the OEM IPMI command to the IPMC after choosing Save and Exit from the BIOS Setup Menu. If user discards changes before saving and exiting, IPMI command will not be sent and Ethernet port direction change will not occur. Notel: Once the mux direction has been set to “AdvancedMC connection to Backplane”, to get the AMC module Ethernet connections to communicate to the fabric interface, the AMC module to be deactivated and re-activated so that e-keying for the AMC occurs.
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.3.10 Progressive Boot Configuration

To access this submenu, select **Advanced** on the menu bar, then **Progressive Boot Configuration**. The progressive boot configuration options are given in Table 64.

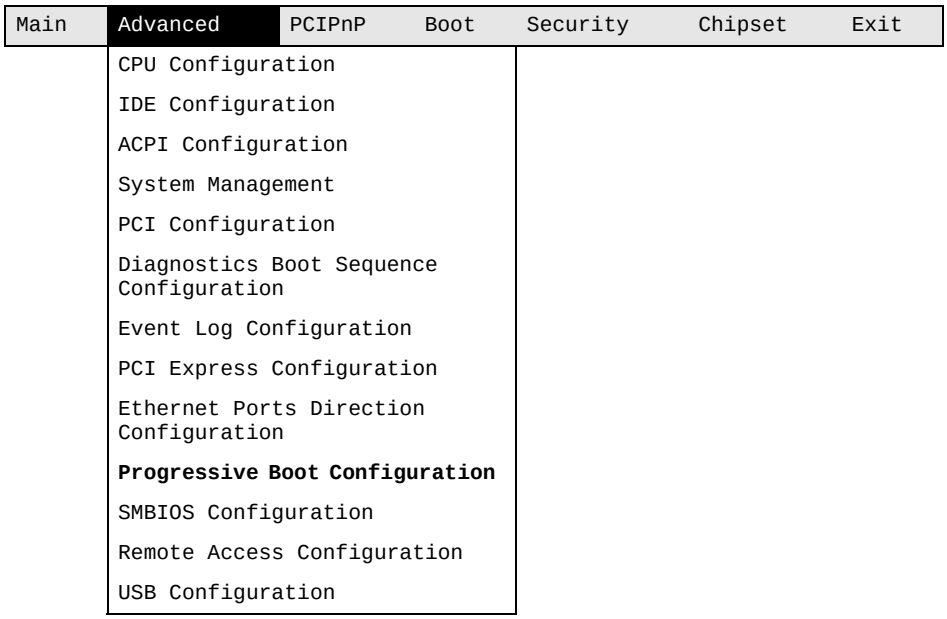


Table 64. Progressive Boot Configuration Submenu Options

Feature	Options	Description
Progressive Boot Support	**Disabled** Enabled	Enable/Disabled Progressive boot support
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.3.11 SMBIOS Configuration Submenu

To access this submenu, select **Advanced** on the menu bar, then **SMBIOS Configuration**. The SMBIOS configuration options are given in Table 65.

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

- CPU Configuration
- IDE Configuration
- ACPI Configuration
- System Management
- PCI Configuration
- Diagnostics Boot Sequence Configuration
- Event Log Configuration
- PCI Express Configuration
- Ethernet Ports Direction Configuration
- Progressive Boot Configuration
- **SMBIOS Configuration**
- Remote Access Configuration
- USB Configuration

Table 65. SMBIOS Configuration Submenu Options

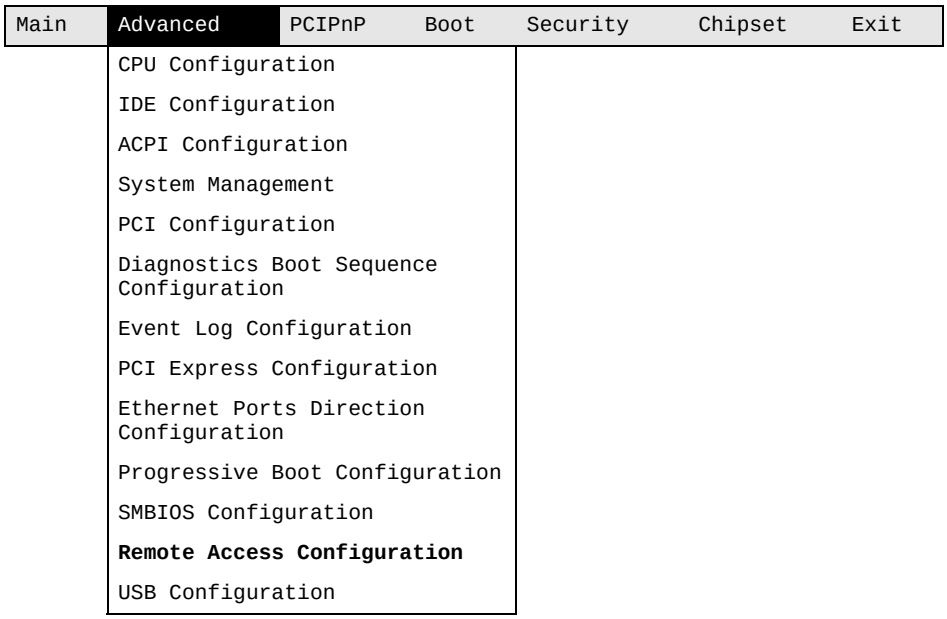
Feature	Options	Description
SMBIOS SMI SUpport	Disabled **Enabled**	SMBIOS SMI Wrapper support for Plug and Play Function 50h-54h

Note: **Bold** text indicates default setting.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.3.12 Remote Access Configuration Submenu

To access this submenu, select **Advanced** on the menu bar, then **Remote Access Configuration**. The remote access configuration options are given in Table 66.



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 66. Remote Access Configuration Submenu Options

Feature	Options	Description
Remote Access	Disabled **Enabled**	Select remote access type
Serial Port Number	**COM1**	Displays serial port number, Base Address and IRQ
Serial Port Mode	115200 8, n,1 57600 8, n,1 38400 8, n,1 19200 8, n,1 **9600 8, n, 1**	Serial port settings. Default is 9600, 8, n, 1
Flow Control	**None** Hardware Software	Select flow control for console redirection
Redirection After BIOS POST	Disabled Boot Loader **Always**	Select the redirection method after the POST boot loader
Terminal Type	**ANSI** VT 100 VT-UTF8	Select the target terminal type
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enable VT-UTF8 Combination Key support for ANSI/VT100 terminals
Sredir Memory Display Delay	**No Delay** Delay 1 sec Delay 2 sec Delay4 sec	Give the delay in seconds to display memory information
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.3.13 USB Configuration Submenu

To access this submenu, select **Advanced** on the menu bar, then **USB Configuration**. The USB configuration options are given in Table 67.

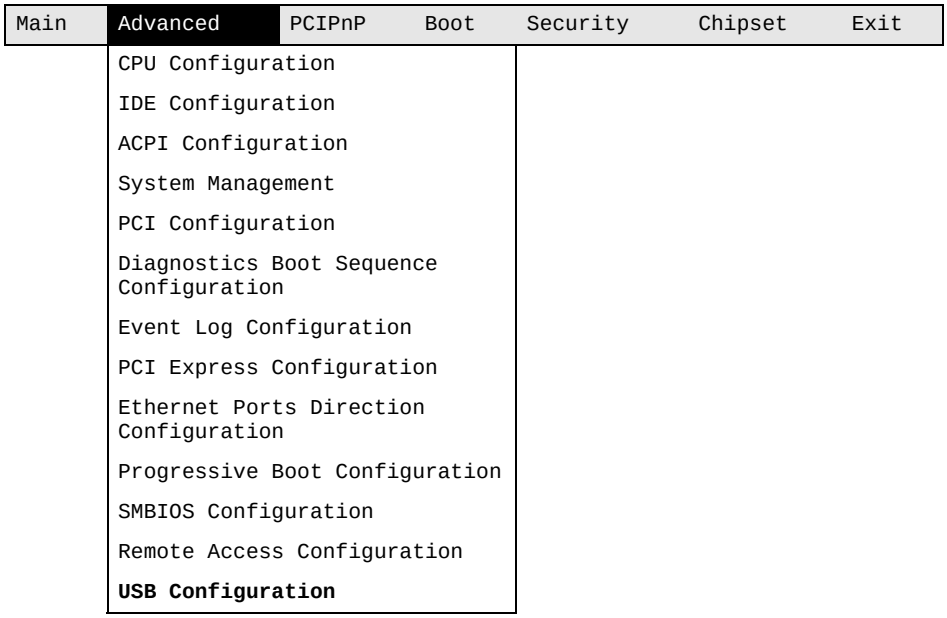


Table 67. USB Configuration Submenu Options

Feature	Options	Description
USB Devices Enabled		Displays the number of USB devices detected by BIOS
USB Function	Disabled **2 USB Ports**	Enable USB host controller
Legacy USB Support	Disabled **Enabled** Auto	Enable support for legacy USB. AUTO option disables legacy support if no USB devices are connected
USB 2.0 Controller	**FullSpeed** HiSpeed	Configures the USB 2.0 controller to FullSpeed (12 Mbps, USB 1.1) or HiSpeed (480 Mbps, USB 2.0)
BIOS EHCI Hand Off	Disabled **Enabled**	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should claim by EHCI driver
USB Mass Storage Device Configuration		This menu is only present if a USB mass storage device (that is, USB flash disk) is present before BIOS starts. If USB mass storage device is not detected, this menu item is not displayed on the screen.
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 68. USB Mass Storage Device Configuration Submenu

Feature	Options	Description
USB Mass Storage Reset Delay	10 Sec **20 Sec** 30 Sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command.
Device		USB mass storage device name will be displayed
Emulation Type	**Auto** Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD (Floppy Disk Drive) option can be used to force a HDD (Hard Disk Drive) formatted to boot as a FDD.

7.4 PCIPnP Menu

To access this menu, select **PCIPnP** from the menu bar at the top of the screen. The PCIPnP options are given in Table 69.

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

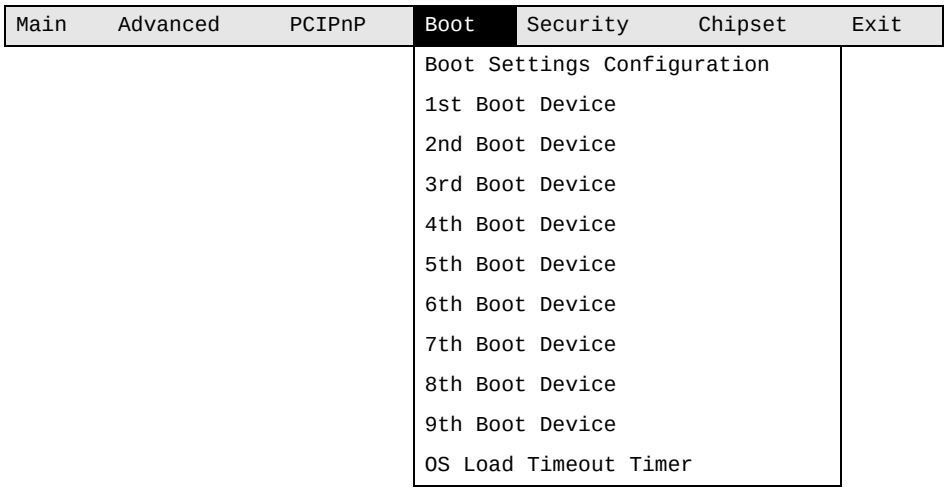
Table 69. PCIPnP Menu Options

Feature	Options	Description
Clear NVRAM	**No** Yes	Clear NVRAM during system boot
Plug & Play OS	**No** Yes	No: BIOS configures all devices in the system Yes: OS configures PnP devices
PCI Latency Timer	**32** 64 96 128 160 192 224 248	Value in units of PCI clocks for PCI device latency timer register
Allocate IRQ to PCI VGA	**Yes** No	YES: Assigns IRQ to PCI VGA card if card requests IRQ NO: Does not assign IRQ to PCI VGA even if card requests an IRQ
PCI IDE BusMaster	**Enabled** Disabled	ENABLED: BIOS uses PCI busmastering for reading/writing to IDE drives
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.5 Boot Menu

To access this menu, select **Boot** from the menu bar at the top of the screen.



7.5.1 Boot Settings Configuration Submenu

To access this submenu, select **Boot** on the menu bar, then **Boot Settings Configuration**. The boot settings configuration options are given in Table 70.

Table 70. Boot Settings Configuration Submenu Options

Feature	Options	Description
Quick Boot	Disabled **Enabled**	Disable/Enable the BIOS to skip certain tests while booting, to decrease the time needed to boot the system.
Quiet Boot	**Disabled** Enabled	Disabled: Display normal POST messaged/OEM logo Enabled: Displays OEM logo instead of POST messages
AddOn ROM Display Mode	**Force BIOS** Keep Current	Set display mode for Option ROM
Bootup Num-Lock	Off **On**	Set power-on state for num-lock
Wait For “F1” If Error	**Disabled** Enabled	Disable/enable waiting for F1 key to be pressed if error occurs
Hit “DEL” Message Display	Disabled **Enabled**	Display “Press DEL to run Setup” in POST
Interrupt 19 Capture	Disabled **Enabled**	Disable/enable the ability for option ROMs to trap interrupt 19
Ethernet Link Boot Control	**Disabled** Boot Ports All Ports	This menu added in version p09-0027 of BIOS. This controls Ethernet port link behavior during PXE boot. When set to ‘Disabled’ all ports have link enabled. When set to ‘Boot Ports’, only the port that is currently being PXE booted will have link enabled and all the other ports will have link disabled. When set to ‘All Ports’, all Ethernet ports have link disabled.
Soft Reset	**Disabled** Enabled	Enable/Disable soft reset feature
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.5.2 OS Load Watchdog Timer Configuration Submenu

To access this submenu, select **Boot** on the menu bar, then **OS Load Timeout Timer**. The options are given in Table 72.

Table 71. OS Load Timeout Timer Configuration Submenu Options

Feature	Options	Description
OS Load Timeout	**Disabled** 60 seconds 120 seconds 150 seconds 240 seconds 480 seconds 600 seconds	Select timeout value for OS load watchdog timer.
OS Load Timeout Action	Stay On **Reset** Power Off Power Cycle	Controls the action upon OS load timeout.
Note: **Bold** text indicates default setting.		

7.5.3 Boot Device Priority Submenu

To access this submenu, select **Boot** on the menu bar, then **<n>th Booth Device Priority**, where "<n>" is the order of priority. The options are given in Table 72.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 72. Boot Device Priority Submenu Options (Sheet 1 of 2)

Feature	Options	Description
1st Boot Device	**HDD: PM- 128 MB ATA Flash Disk** HDD: SM- 128MB ATA Flash Disk Network: IBA GE Slot 0400 v0006 Network: IBA GE Slot 0401 v0006 Network: IBA GE Slot 0300 v0006 Network: IBA GE Slot 0301 v0006 Network: IBA GE Slot 0200 v0006 Network: IBA GE Slot 0201 v0006 USB: USB Disk † SCSI: #xxx IDxx†	Set the first boot device (Primary on-board 128MB flash drive) † If other boot devices are added, they will show up at the bottom of the list and manually will need to be assigned different boot priority if desired.
2nd Boot Device	HDD: PM- 128MB ATA Flash Disk **HDD: SM- 128MB ATA Flash Disk** Network: IBA GE Slot 0400 v0006 Network: IBA GE Slot 0401 v0006 Network: IBA GE Slot 0300 v0006 Network: IBA GE Slot 0301 v0006 Network: IBA GE Slot 0200 v0006 Network: IBA GE Slot 0201 v0006	Set the second boot device (Secondary on-board 128MB flash drive) † If other boot devices are added, they will show up at the bottom of the list and manually will need to be assigned different boot priority if desired.
3rd Boot Device	HDD: PM- 128MB ATA Flash Disk HDD: SM- 128MB ATA Flash Disk **Network: IBA GE Slot 0400 v0006** Network: IBA GE Slot 0401 v0006 Network: IBA GE Slot 0300 v0006 Network: IBA GE Slot 0301 v0006 Network: IBA GE Slot 0200 v0006 Network: IBA GE Slot 0201 v0006	Set the third boot device Default is IBA Slot 0400 (Port E, Fabric Interface Port 1, Channel 1)
4th Boot Device	HDD: PM- 128MB ATA Flash Disk HDD: SM- 128MB ATA Flash Disk Network: IBA GE Slot 0400 v0006 **Network: IBA GE Slot 0401 v0006** Network: IBA GE Slot 0300 v0006 Network: IBA GE Slot 0301 v0006 Network: IBA GE Slot 0200 v0006 Network: IBA GE Slot 0201 v0006	Set the fourth boot device Default is IBA Slot 0401 (Port F, Fabric Interface Port 1, Channel 2)
5th Boot Device	HDD: PM- 128MB ATA Flash Disk HDD: SM- 128MB ATA Flash Disk Network: IBA GE Slot 0400 v0006 Network: IBA GE Slot 0401 v0006 **Network: IBA GE Slot 0300 v0006** Network: IBA GE Slot 0301 v0006 Network: IBA GE Slot 0200 v0006 Network: IBA GE Slot 0201 v0006	Set the fifth boot device Default is IBA slot 0300 (Port C, Fabric Interface Port 0, Channel 1)
Notes: †: A device is only shown as an option if it is installed and detected by the BIOS during boot. **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 72. Boot Device Priority Submenu Options (Sheet 2 of 2)

Feature	Options	Description
6th Boot Device	HDD: PM- 128MB ATA Flash Disk HDD: SM- 128MB ATA Flash Disk Network: IBA GE Slot 0400 v0006 Network: IBA GE Slot 0401 v0006 Network: IBA GE Slot 0300 v0006 **Network: IBA GE Slot 0301 v0006** Network: IBA GE Slot 0200 v0006 Network: IBA GE Slot 0201 v0006	Set the sixth boot device Default is IBA slot 0301 (Port D, Fabric Interface Port 0, Channel 2)
7th Boot Device	HDD: PM- 128MB ATA Flash Disk HDD: SM- 128MB ATA Flash Disk Network: IBA GE Slot 0400 v0006 Network: IBA GE Slot 0401 v0006 Network: IBA GE Slot 0300 v0006 Network: IBA GE Slot 0301 v0006 **Network: IBA GE Slot 0200 v0006** Network: IBA GE Slot 0201 v0006	Set the seventh boot device Default is IBA slot 0200 (Port A, Base Interface Channel 1)
8th Boot Device	HDD: PM- 128MB ATA Flash Disk HDD: SM- 128MB ATA Flash Disk Network: IBA GE Slot 0400 v0006 Network: IBA GE Slot 0401 v0006 Network: IBA GE Slot 0300 v0006 Network: IBA GE Slot 0301 v0006 Network: IBA GE Slot 0200 v0006 **Network: IBA GE Slot 0201 v0006**	Set the eighth boot device Default is IBA slot 0201 (Port B, Base Interface Channel 2)
Notes: †: A device is only shown as an option if it is installed and detected by the BIOS during boot. **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.6 Security Menu

To access this menu, select **Security** from the menu bar at the top of the screen. The options are given in Table 73.

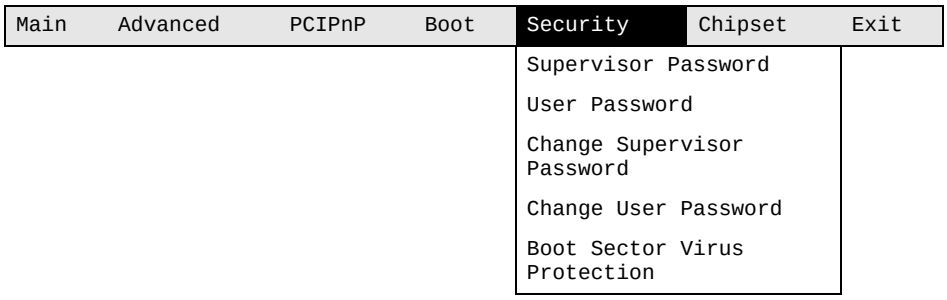


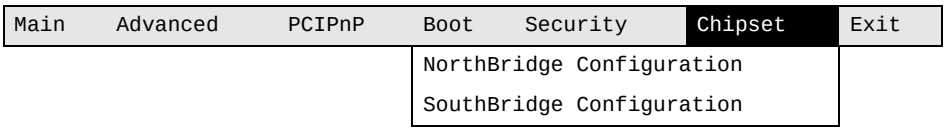
Table 73. Security Menu Options

Feature	Options	Description
Supervisor Password	Not Installed	Display the Supervisor Password status Installed/not Installed
User Password	Not Installed	Display the User Password status Installed/not Installed
Change Supervisor Password		Set the supervisor password
Change User Password		Set the user password
Boot Sector Virus Protection	**Disabled** Enabled	Disable/enable boot sector virus protection
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.7 Chipset Menu

To access this menu, select **Chipset** from the menu bar at the top of the screen.



7.7.1 NorthBridge Configuration Submenu

To access this submenu, select **Chipset** on the menu bar, then **NorthBridge Configuration**. The options are given in Table 74.

Table 74. NorthBridge Configuration Submenu Options

Feature	Options	Description
Memory remap feature	Disabled **Enabled**	Allow remapping of overlapped PCI memory above the total physical memory
Note: **Bold** text indicates default setting.		

7.7.2 SouthBridge Configuration Submenu

To access this submenu, select **Chipset** on the menu bar, then **SouthBridge Configuration**. The options are given in Table 75.

Table 75. SouthBridge Configuration Submenu Options

Feature	Options	Description
ICH SIO Serial Port1 Address	Disabled **3F8/IRQ4** 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Allows BIOS to select ICH serial I/O unit serial port 1 base address
ICH SIO Serial Port2 Address	Disabled 3F8/IRQ4 **2F8/IRQ3** 3E8/IRQ4 2E8/IRQ3	Allows BIOS to select ICH serial I/O unit serial port 2 base address
Note: **Bold** text indicates default setting.		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

7.8 Exit Menu

To access this menu, select **Exit** from the menu bar at the top of the screen. The options are given in Table 76.

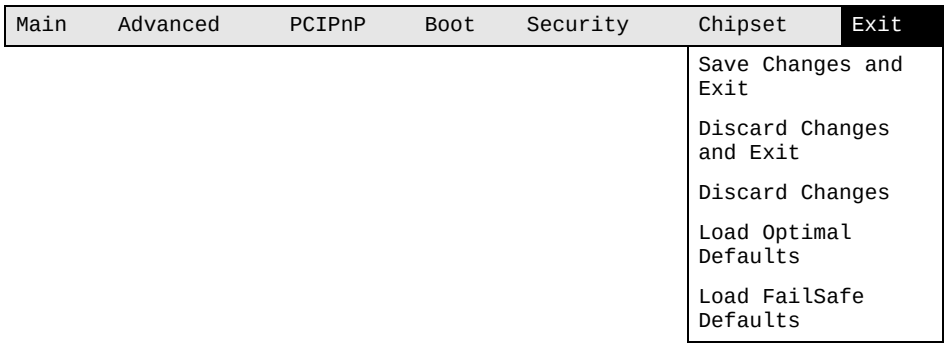


Table 76. Exit Menu Options

Feature	Options	Description
Save Changes and Exit		Exit system Setup after saving changes. Use this to save your configured settings to the CMOS and flash. Similar to pressing F10
Discard Changes and Exit		Exit system Setup without saving changes Similar to pressing ESC
Discard Changes		Discard changes without exiting Similar to pressing F7
Load Optimal Defaults		Load optimal default values Similar to pressing F9
Load FailSafe Defaults		Load failsafe default values Similar to pressing F8

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

8.0 Error Messages and Checkpoints

8.1 BIOS Error Messages

The following table lists the BIOS error messages supported by the MPCBL0040 SBC.

Table 77. BIOS Error Messages

Error Message	Explanation of Error Message
Timer Error	This timer is based on the 8254 that resides in ICH-3. The error message indicates an error while programming the count register of the timer. This may indicate a problem with the timer in ICH-3.
CMOS Battery Low	The BIOS reports this error message when the status bit (RTC_REGD.Bit7) in the ICH3 is low. This bit is hard wired to RTC power, so it is low when the voltage in the hold up capacitor is low.
CMOS Settings Wrong	The BIOS loads default values when it detects CMOS corruption. This error message is triggered if the BIOS fails to load the default value to CMOS.
CMOS Checksum Bad	CMOS contents failed the checksum check. Indicates that the CMOS data has been changed by a program other than the BIOS or the CMOS is not retaining its data due to hardware malfunction.
RAM R/W test failed	Indicates a BIOS fail to read/write to memory content during RAM R/W test. The RAM R/W test is executed during POST.
CMOS Date/ Time Not Set	Indicates that the BIOS has detected an invalid value in the date & time register, for example, invalid date = 50h or invalid month = 13h.
Clear CMOS Jumper installed	Indicates that switch (SW 5-2) is set to OFF.
Clear Password Jumper installed	Indicates that switch (SW 5-1) is set to OFF.
MFG Jumper installed	Indicates that switch (SW 5-3) is set to OFF (for manufacturing test use only)
BMC in Update Mode	Indicates that switch (SW 5-8) is set.
BMC does not respond to BIOS IPMI command	Occurs when the BIOS issues an IPMI command to the IPMC, but the IPMC does not respond to the command and does not return a successful completion code to the BIOS.
System Event Log is Full	Indicates that System Event Log (SEL) storage is full.
Refresh timer test failed	This timer is a counter based on the 82C54 which provides a memory refresh request signal periodically. The memory content needs to be refreshed to compensate for the gradual leakage of charge from the capacitors that store the data.
KBC BAT Test failed	Indicates that the Keyboard controller BAT test has failed.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

8.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST-codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Port 80h POST codes can be retrieved from IPMC with an OEM IPMI command. Refer to Appendix A:, "Supported IPMI Commands". In the case of SBC hang, Port 80h can be retrieved remotely from the chassis management module.

Table 78, Table 79, and Table 80 offer descriptions of the POST codes generated by the BIOS. They define the uncompressed INIT code checkpoints, the boot block recovery code checkpoints, and the runtime code uncompressed in F000 shadow RAM.

Note: Some codes are repeated in the tables because they apply to more than one operation.

Table 78. Boot Block Initialization Code Checkpoints

Checkpoint	Description
Before D0	If the boot block debugger is enabled, CPU cache-as-RAM functionality is enabled at this checkpoint. The stack is enabled at this checkpoint.
D0	Early Boot Strap Processor (BSP) initialization like microcode update, frequency, and other CPU critical initialization. Early chipset initialization is done at this checkpoint.
D1	Early super I/O initialization is done including RTC and keyboard controller. The serial port is enabled at this point if needed for debugging. NMI is disabled. Performs keyboard controller BAT test. Saves power-on CPUID value in scratch CMOS. Goes to flat mode with 4 GByte limit and GA20 enabled.
D2	Verifies the boot block checksum. The system hangs here if the checksum is bad.
D3	Disables CACHE before memory detection. Executes full memory sizing module. If the memory sizing module is not executed, start memory refresh and do memory sizing in boot block code. Does additional chipset initialization. Re-enables CACHE. Verify that flat mode is enabled.
D4	Tests base 512 KBytes memory. Adjusts policies and caches first 8 MBytes. Sets stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. The BIOS now executes from RAM. Copies compressed boot block code to memory in right segments. Copies BIOS from ROM to RAM for faster access. Performs main BIOS checksum and updates recovery status accordingly.
D6	Both key sequence and OEM-specific methods are checked to determine if BIOS recovery is forced. If BIOS recovery is necessary, control flows to checkpoint E0.
D7	Restores the CPUID value back into the register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determines whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Stores the uncompressed pointer for future use in PMM. Copies the main BIOS into memory. Leaves all RAM below 1 MByte read-write including E000 and F000 shadow areas, but closing SMRAM.
DA	Restore the CPUID value back into the register. Give control to BIOS POST (ExecutePOSTKernel). See Table 79 for more information.
DC	System wakes from ACPI S3 state.
E1-E8 EC-EE	OEM memory detection/configuration error. This range is reserved for chipset vendors and system manufacturers. The error associated with this value may be different depending on the platform.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 79. POST Code Checkpoints (Sheet 1 of 2)

Checkpoint	Description
03	Disables NMI, parity, video for EGA, and DMA controllers. Initializes BIOS, POST, runtime data area. Also initializes BIOS modules on POST entry and GPNV area. Initializes CMOS as mentioned in the kernel variable “wCMOSFlags”.
04	Checks CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verifies CMOS checksum manually by reading storage area. If the CMOS checksum is bad, updates the CMOS with power-on default values and clear passwords. Initializes the status register A. Initializes data variables that are based on CMOS Setup questions. Initializes both the 8259-compatible PICs in the system.
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Does a R/W test to CH-2 count register. Initializes CH-0 as the system timer. Installs the POSTINT1Ch handler. Enables IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to “POSTINT1ChHandlerBlock”.
07	Fixes CPU POST interface calling pointer.
08	Initializes the CPU. The BAT test is being done on the KBC. Program the keyboard controller command byte is being done after auto detection of the KB/MS using AMI KB-5.
C0	Early CPU Init Start. Disable Cache. Init Local APIC.
C1	Sets up bootstrap processor information.
C2	Sets up bootstrap processor for POST.
C5	Enumerates and sets up application predecessors.
C6	Re-enables cache for bootstrap processor.
C7	Early CPU Init Exit.
0A	Initializes the 8042-compatible keyboard controller.
0B	Detects the presence of a PS/2 mouse.
0C	Detects the presence of a keyboard in the KBC port.
0E	Tests and initializes different input devices. Also, updates the kernel variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompresses all available language, BIOS logo, and silent logo modules.
13	Early POST initialization of chipset registers.
20	Relocates the system management interrupt vector for all CPUs in the system.
24	Uncompresses and initializes any platform-specific BIOS modules. GPNV is initialized at this checkpoint.
2A	Initializes different devices through DIM. See Table 80, “Device Initialization Manager (DIM) Code Checkpoints” on page 177 for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that has optional ROMs.
2E	Initializes all the output devices.
31	Allocates memory for ADM module and uncompresses it. Gives control to the ADM module for initialization. Initializes language and font modules for ADM. Activates the ADM module.
33	Initializes the silent boot module. Sets the window for displaying text information.
37	Displays the sign-on message, CPU information, setup key message, and any OEM-specific information.
38	Initializes different devices through DIM. See the DIM Code Checkpoints section of the document for more information. USB controllers are initialized at this point.
39	Initializes DMAC-1 and DMAC-2.
3A	Initializes RTC date/time.
3B	Tests for total memory installed in the system. Also, checks for DEL or ESC keys to limit memory test. Displays total memory in the system.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 79. POST Code Checkpoints (Sheet 2 of 2)

Checkpoint	Description
3C	Mid-POST initialization of chipset registers.
40	Detects different devices successfully installed in the system (for example, parallel ports, serial ports, and coprocessor in the CPU) and updates the BDA, EBDA, etc.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for the Extended BIOS Data Area from base memory. Programs the memory hole or any kind of implementation that needs an adjustment in system RAM size.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initializes Int-13 and prepares for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7C	Generates and writes content of ESCD in NVRam.
84	Logs errors encountered during POST.
85	Displays errors to the user and gets the user response to error.
87	Executes BIOS Setup if needed/requested. Checks boot password if installed.
8C	Late POST initialization of chipset registers.
8D	Builds ACPI tables (if ACPI is supported).
8E	Programs the peripheral parameters. Enable/Disable NMI as selected.
90	Initializes system management interrupt by invoking all handlers. **NOTE:** This checkpoint comes immediately after checkpoint 20h.
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fills the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initializes runtime language module. Displays the boot option popup menu.
A7	Displays the system configuration screen if enabled. Initializes the CPUs before boot, which includes the programming of the MTRRs.
A9	Waits for user input at configuration display if needed.
AA	Uninstalls the POST INT1Ch vector and the INT09h vector.
AB	Prepares the BBS for Int 19 boot. Initializes MP tables.
AC	End of POST initialization of chipset registers. De-initializes the ADM module.
B1	Saves the system context for ACPI. Prepares the CPU for OS boot including final MTRR values.
00	Passes control to the OS loader (typically INT19h).

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 80. Device Initialization Manager (DIM) Code Checkpoints

Checkpoint	Description
2A	Initializes different buses and performs the following functions: • **Function 0: Reset, Detect, and Disable** - Disables all device nodes, PCI devices, and PnP ISA cards. Assigns PCI bus numbers. • **Function 1: Static Device Initialization** - Initializes all static devices that include manual configured on-board peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Reserves static resources. • **Function 2: Boot Output Device Initialization** - Searches for and initializes any PnP, PCI, or AGP video devices.
38	Initializes different buses and performs the following functions: • **Function 3: Boot Input Device Initialization** - Searches for and configures PCI input devices and detects if system has a standard keyboard controller. • **Function 4: IPL Device Initialization** - Searches for and configures all PnP and PCI boot devices. • **Function 5: General Device Initialization** - Configures all on-board peripherals that are set to automatic configuration and configures all remaining PnP and PCI devices.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

9.0 Serial Over LAN

Serial over LAN (SOL) is a packet format and protocol defined in the IPMI v2.0 specification for transmitting serial port data over Ethernet using IPMI over LAN (RMCP+) messages. This two-way redirection of a blade's serial port data over Ethernet is independent of the operating system or any applications executing on it. The BIOS also supports redirection of its console over a serial port, which can be redirected over the network for remote access.

The SOL mechanism, coupled with an SOL client utility executing on a remote node, allows the viewing of serial port data from any IPMI v2.0 based, SOL-enabled blade, thus providing a virtual remote terminal server for accessing the blade's serial port character stream.

9.1 References

- *Intelligent Platform Management Interface Specification v2.0*, dated June 1, 2004
- *AES - Advanced Encryption Standard,* http://csrc.nist.gov/publications/fips/fips197/fips-197.pdf

9.2 SOL Architecture

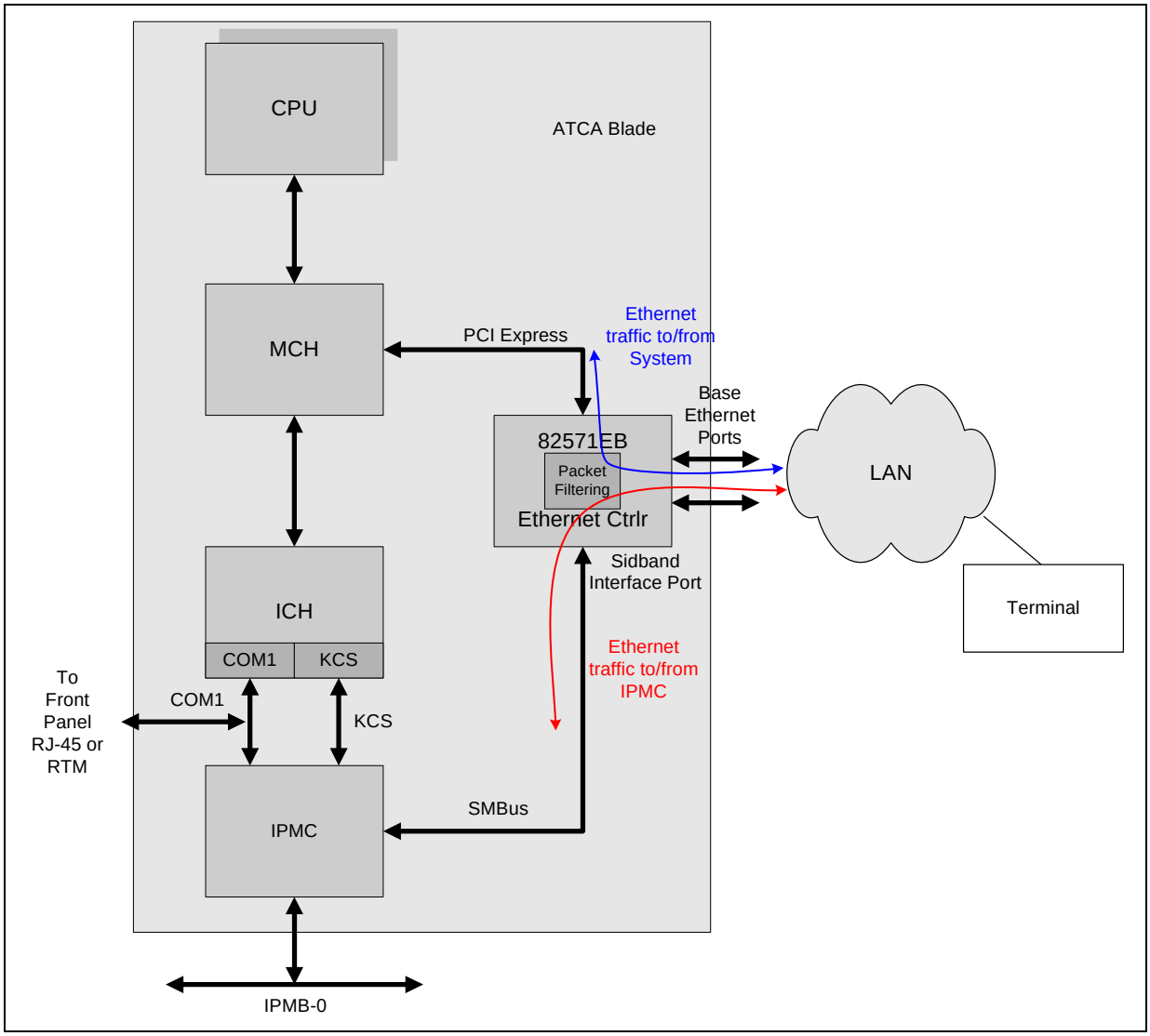
The SOL implementation on the Promentum™ MPCBL0040 blade is based on the definition in Section 15 of the IPMI v2.0 specification.

Serial over LAN (SOL) enables suitably designed blades and servers to transparently redirect a serial character stream of a baseboard UART to/from a remote client via LAN over RMCP+ sessions. This enables users at remote consoles to access the serial port of a blade/server and interact with a text-based BIOS console, operating system, command line interfaces, and serial text-based applications.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Figure 33 is a block diagram of the SOL implementation on the blade.

Figure 33. SOL Block Diagram



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

This architecture requires the following components to perform Serial over LAN operations:

- SOL-capable firmware executing on the Intelligent Platform Management Controller (IPMC). The IPMC also provides a dedicated SMBus connection to the base interface Ethernet controller. This connectivity is not shared with IPMB-0 or any other I^2C/ SMBus/IPMB connections that the IPMC may provide on the blade for hardware management.
- The base interface Ethernet controller, which provides a sideband interface port to the IPMC over which SOL traffic is redirected. The Ethernet controller also filters packets based on MAC address, RMCP port number, or IP address, and forwards the packets to the IPMC over the sideband interface.
- Client software running on any remote node that has LAN access to the blade whose serial port data is to be accessed. The IPMC is responsible for controlling the serial hardware MUX, the transformation of serial data to and from network packets, and the transmission and reception of SOL network packets through the Ethernet controller sideband interface port.

9.2.1 Architectural Components

9.2.1.1 IPMC

As shown in the block diagram in Figure 33, the IPMI controller on the blade provides a UART interface to the blade's serial port (COM1). This interface is used by the IPMC firmware to write data to the blade's serial port or to receive the blade's serial port data written by the BIOS or the operating system. The serial port may be connected to either to the IPMI controller or to RJ-45 connector(s) on the front panel and the RTM (if available). The switching of the serial port between front-panel/RTM and the IPMC's UART port is controlled by the IPMC firmware.

The IPMC also provides a dedicated SMBus connection to the Ethernet controller, whose ports are connected to the base Ethernet interface.

The KCS interface is used for interaction between the IPMC firmware and software executing on the OS (for example, OpenIPMI or OpenHPI) by sending/receiving IPMI messages, and does not play a role during SOL communication. The KCS interface however, may be used for SOL-related IPMC configuration, as described below.

9.2.1.2 Ethernet Controller

The Ethernet controller provides an advanced pass-through mode of operation where the controller allows the on-board IPMC to communicate over the Ethernet ports using a sideband interface port.

The Ethernet controller is available with standby (management) power, so that it is possible to view the initial serial port data written by the BIOS or the OS.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

9.3 Theory of Operation

9.3.1 Front Panel Serial Port or RTM

By default, the serial console is connected to the serial port connector(s) on the front panel and RTM (if available).

If serial cables are connected to both the front panel and RTM connectors, both connections will be active. However, only one user is allowed to use the serial session.

9.3.2 Serial Over LAN

IPMC firmware is pre-configured at manufacturing time with default serial port settings (baud rate, parity bits, data bits, stop bits, flow control), user name and password for RMCP+ sessions. The SOL feature, however, is disabled by default.

The IP address to be used by IPMC can be configured during initial setup of the blade in the system.

The IP address, once configured by the reference script provided, is stored in a non-volatile memory and is persistent across IPMC update and payload resets. The IP addresses are assigned to the IPMC independently of the host (OS) IP addresses and they need not match. The IP addresses used by the OS are not visible to the IPMC.

To start SOL communication, the user invokes the SOL client utility with the IP address of the blade and a series of authentication parameters (username, password, privilege level, cipher suite, etc.). The IPMI v2.0 specification allows for AES encryption algorithms for encryption of payload data sent over the network, including AES-128, which uses 128-bit cipher keys.

The SOL client utility initializes an RMCP+ session with the blade and activates SOL. When authentication is successfully completed, the IPMC firmware collects serial port data from the blade's serial port, formats it into network packets and forwards it to the SOL client utility over the SOL session. The SMBus sideband interface port between the IPMC and base interface Ethernet controller is used for this purpose. The SOL client utility receives the packets, extracts the serial port data, and displays it on the screen. The IPMC extracts the serial port data received from the SOL client utility and writes it to the serial port of the blade. This allows network redirection of blade's serial port data stream that is independent of the host OS or BIOS. The Ethernet controller plays a critical role in redirecting the packets meant for the IPMC, based on receive filters.

The maximum baud rate supported by the IPMC for SOL is 38.4 kbps. The default SOL baud rate is 9.6 kbps.

Note: The BIOS default baud rate is 9.6 kbps. If SOL is configured for a different baud rate, the BIOS output is not seen using the SOL client until the BIOS baud rate is set to match the SOL client baud rate.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

9.4 Serial Over LAN Client

The SOL client establishes an IPMI-over-LAN connection with the IPMC on the blade. It then activates SOL, which effectively switches the board hardware to redirect serial traffic to the IPMC instead of the serial port. Any outbound characters from the UART are now packetized by the IPMC and sent over the network to the SOL client via the sideband interface port. Conversely, any input on the SOL client is packetized by the client and sent over the network to the IPMC, which is responsible for conveying it to the UART.

SOL data is carried over the network in UDP datagrams. IPMI 2.0 defines the specification of packet formats and protocols for SOL. As per the IPMI 2.0 specification, RMCP+ is the packet format with the Payload Type set to “SOL”. Authentication, integrity, and encryption for SOL are part of the RMCP+ specification.

The ipmitool client (version 1.8.7 or higher) is required. The ipmitool software is open source. For more information, see Section 9.8.2.2, “Installing ipmitool” on page 194.

This client needs to be downloaded and compiled on the Linux* operating system of your choice.

9.5 Reference Configuration Script

RadiSys provides an SOL reference script (reference_cfg) that sets up the various parameters required for SOL operation.

The SOL configuration reference script (reference_cfg) sends a sequence of IPMI commands to configure an SBC to enable the SOL feature. This script can be executed on a payload CPU for local configuration, or on a node that has network connectivity to the target SBC. Without this IPMC configuration, the SOL client utility is not able to communicate with the SBC. This script is provided to customers as an example of a semi-automated method of configuring systems and is not meant for use in production environments.

The ipmitool utility enables a user to establish an RMCP+ session with an SBC's management controller and activate two-way SOL packet communication.

It is important to note that while the ipmitool is a supported utility, reference_cfg is provided as an unsupported reference to be modified by customers to suit their specific environments and integration needs.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

9.6 Supported Usage Model

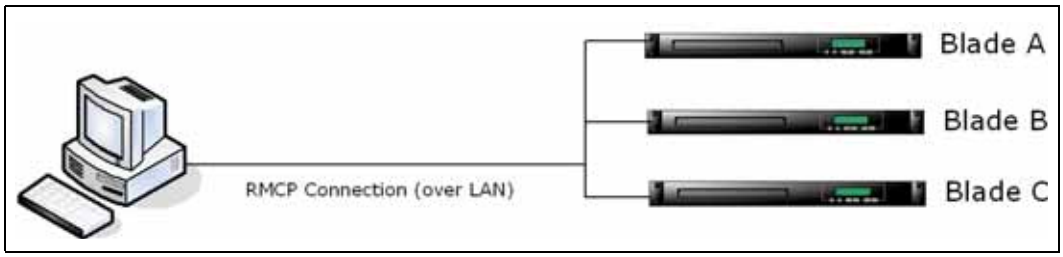
Customers are expected to use SOL to accomplish the following:

- BIOS console redirection
- Remote terminal access for OS setup and viewing text console output

The ipmitool utility runs on a remote network node and communicates over the LAN interface. The remote node and the target SBC may be on the same subnet or on different subnets.

The reference script can be run on the remote node.

Figure 34. Reference Script Running on Remote Node, Communicating over LAN



Note: The machine or “remote node” running ipmitool may also be an MPCBL0040 SBC within the same chassis.

9.6.1 Configuring the Blade for SOL

To configure a blade for SOL, the machine on which the configurator is installed (typically the remote node) needs to establish an RMCP connection with the SBC. The configurator sends commands and configuration settings to the SBC to configure and enable SOL operation. To configure a blade for SOL, reference_cfg needs to run either on the same blade as the IPMC and communicate via the KCS interface, or on a remote node. In the latter case, the script sends IPMI messages over the LAN to the SBC’s shelf manager, which in turn bridges data to the IPMC’s IPMB-0 interface.

The minimal per-blade configuration that must be set up includes the following:

- An IP/MAC address, subnet mask and default gateway
- ARP configuration
- User ID and password to authenticate access
- Channel, user, payload, and SOL privilege levels

The configuration utility is referring to the reference_cfg script described above.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

9.7 Reference Script (reference_cfg)

9.7.1 SOL Configuration Reference Script (reference_cfg)

The reference script can run with no special setup. The script uses built-in bash commands as well as grep and awk. The environment in which the script runs must have bash installed at /bin/bash (or a symbolic link at that location), and must include grep and awk in the path.

The reference script is implemented as two separate bash files: reference_cfg, which contains the necessary IPMI commands, and reference_func, a library of supporting functions. When reference_cfg runs, it looks for the library in the following paths in the order listed:

1. the current working directory
2. /usr/lib/sbcutils
3. /home/scripts

If reference_cfg cannot find the library in any of these locations, it terminates with an error message.

When running the reference script on a remote node over RMCP via a shelf manager, RMCP to IPMB bridging must be enabled on the shelf manager. In the case of the Promentum™ MPCMM0001/0002 Chassis Management Module, the following command enables RMCP:

```
# cmmset -d rmcpenable -v 1
```

RMCP and KCS communication requires the OpenIPMI application library, version 1.4 or later. KCS communication further requires the OpenIPMI driver.

9.7.2 Default Behavior

To configure a blade for SOL communications, many items need configuration (for example, user information, channel parameters, LAN parameters and SOL parameters). Most of the values used for configuration appear as hard-coded default values.

9.7.3 SOL User Information

SBCs from RadiSys implement four different users, User1 through User4. User1 has a null username which is not editable. The script configures User2 as specifically enabled for SOL payloads.

The user name is “solusername”, zero-padded to a length of 16 bytes as per the IPMI 2.0 specification. The password is “soluserpassword”, zero-padded to 20 bytes as per the IPMI 2.0 extension.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

9.7.4 LAN Parameters

The reference script configures IPMI channel one. The IPMI channel number used by reference_cfg can be changed to any IPMI LAN channel supported by the target SBC.

The configured channel must be a base interface, not a fabric interface. On the MPCBL0040 SBC, IPMC channel 1 corresponds to the Ethernet interface eth4.

Since reference_cfg uses IPMI channel one, this means that, for any SBC, eth0 is routed to a switch in slot seven (this may vary on different chassis implementations).

IP and MAC addresses supplied to the IPMC are specified on the command-line as per Table 81, “SOL Configuration Reference Script Command-line Options” on page 187. The IP source is set to “static” and the subnet mask is set for a class C subnet. The gateway IP and MAC addresses should be specified with the command to enable RMCP communication across subnets. If the IP or MAC address options are missing from the command line, those parameters are not changed on the IPMC.

Note: The IP, MAC, gateway, and gateway MAC parameters are optional. If these settings have been previously configured and have not changed, it is not necessary to supply them on the command line every time the scripts is executed.

The IP and MAC address for an IPMC can be obtained from the operating system running on the SBC with the `ifconfig` command. In the output from this command, the `inet addr` field contains the IP address; the `HWaddr` field contains the MAC address.

The IP and MAC address of the subnet’s gateway can be obtained from the operating system running on the SBC by executing the `route` command to obtain the host name of the gateway, then by executing the `arp -a gateway_hostname` command to obtain the gateway’s IP address and MAC address. (If needed, execute the `ping gateway_hostname` command, then re-execute the `arp` command to obtain the IP and MAC addresses.)

Gratuitous ARPs generated by the BMC are enabled and sent every three seconds.

The `md5` authentication type is enabled for all privilege levels.

9.7.5 SOL Parameters

The SOL payload type is enabled with a privilege level of operator. Neither payload encryption nor payload authentication is forced. Serial characters are accumulated for as long as 40 milliseconds or as many as 50 characters. SOL packets are retried every 100 milliseconds, up to seven times. The default SOL baud rate is 9600 bps.

9.7.6 Channel Parameters

Channel 1 is configured as “always available”, meaning that all RMCP traffic to the SBC LAN adaptor is routed exclusively to the IPMC and not to system software.

For channel 1, User2 is enabled for general IPMI messaging (as opposed to SOL only messaging). User2 has a privilege level of operator on channel 1.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

9.7.7 Command Line Options

The available command-line options for the reference script are given in Table 81.

Table 81. SOL Configuration Reference Script Command-line Options

Option	Meaning
-h	"help" - Display usage, version number and a list of options. When this option is specified, all other options are ignored.
-l	"location" - Specifies which blade to configure. When running on the MPCMM0001, this value should be one of ["blade1" to "blade14"]. When running on a remote node, this value should be the IPMB address. When running on the local processor, this option is ignored.
-i	"IP" - Specifies which IP address should be used to configure the blade. The IP address should be given in the form ###.###.###.### where "###" is a decimal number from 0 to 255.
-j	Specifies the IP address of the subnet's gateway.
-n	Specifies the MAC address of the subnet's gateway.
-g	"Gratuitous ARPs" - Turns on gratuitous ARPs. If this switch is not supplied, then generated ARP responses are enabled instead.
-V	"Version" - Displays the version and quits.
-I	"Interface" - Specifies the interface used to communicate to the IPMC. Must be one of: kcs, lan or ipmb.
-m	"MAC" - Specifies which MAC address should be used to configure the blade. MAC address is given in the form of ##:##:##:##:##:##
-H	RMCP-IP - IP address or host name of the shelf manager used to bridge RMCP messages to IPMB.
-U	"User" - Specifies the username for establishing the RMCP sessions. If not specified, the default value root is used.
-P	"Password" - Password for establishing RMCP sessions. If not specified, the default value cmmrootpass is used.
-A	"Authorization" - Authorization type for establishing the RMCP sessions. One of {none|straight|md2|md5}.
-?	Print the message and quit.

9.8 Setting up a Serial Over LAN Session

9.8.1 Target Blade Setup

The target blade is the SOL blade that sends the serial data to the client.

Ensure that the MPCBL0040 SBC has the following firmware/OS versions loaded:

- IPMC Firmware 1.03.01 or later
- BIOS P02-00014 or later
- sbcutilities 1.2.0.10 or later
- MontaVista* 4.0 LSP, Red Hat* RHEL 4.0 U3, or Wind River* PNE LE 1.2 LSP

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

9.8.1.1 BIOS Configuration

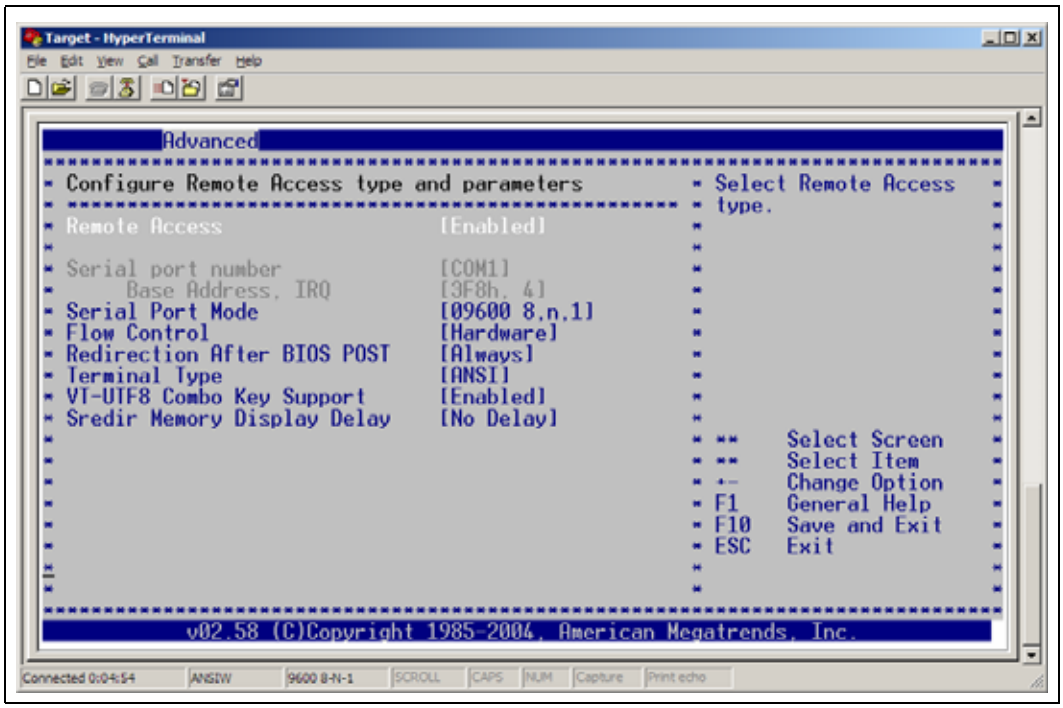
Configure the target blade BIOS baud rate so that it is set to 9600. The SOL target blade can operate at baud rates of 9600, 19200, and 38400 only. All examples in this document reflect a baud rate of 9600.

Configure the BIOS on the SOL Target Blade as follows (refer also to Figure 35):

1. When the blade starts booting, press F4 from HyperTerminal (or equivalent terminal program) to enter BIOS setup menu.
2. Choose the **Advanced** menu.
3. Choose the **Configure Remote Access** menu.
   Change the **Flow Control** parameter to “Hardware”.
4. Change **Serial Port Mode** to the 9600 baud rate if it is not already set to that speed.
5. Press **Esc**.
6. Choose **Save and Exit**.

Note: If the default BIOS baud rate is changed to a baud rate other than 9600, then the reference_cfg script will need to be changed to match the same baud rate.

Figure 35. BIOS Configuration of SOL Target Blade



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

9.8.1.2 Operating System Configuration

Configure the operating system baud rate to match the BIOS baud rate:

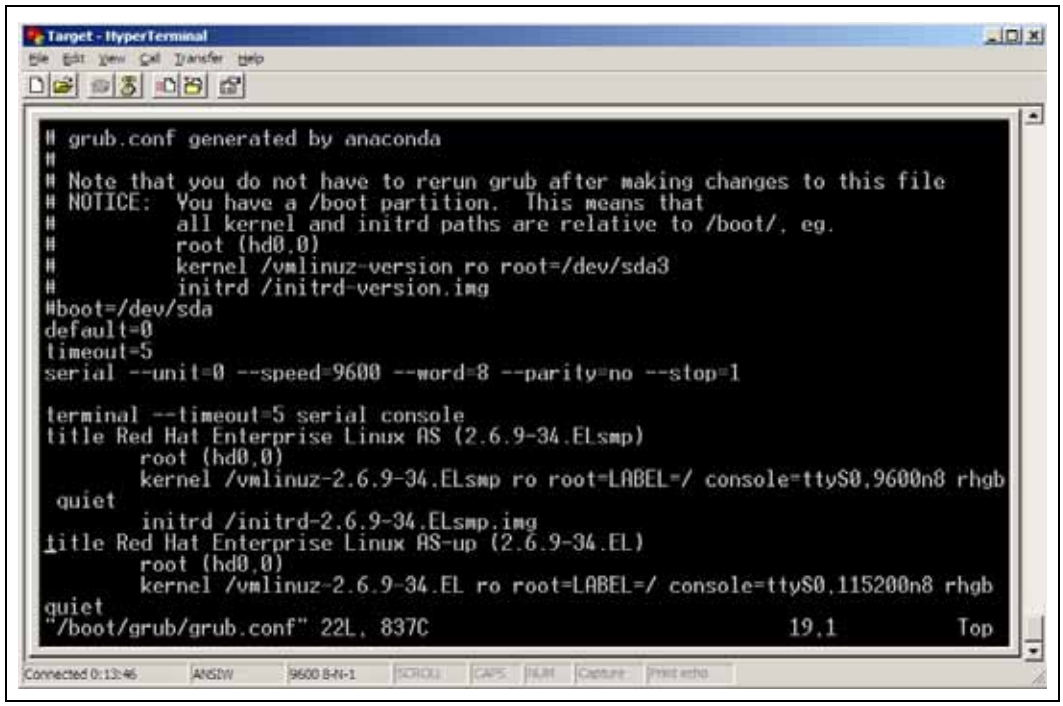
1. When using MontaVista:
   a. Edit the /etc/lilo.conf file
   b. Type `vi /etc/lilo.conf`
   c. Set the bootloader baud rate by adding or modifying a line as follows:
      `serial=0,9600n8r`
   d. Change the append line to read as follows:
      `append="ip=off console=ttyS0,9600n8r panic=5"`

Note: Hardware flow control is required (hence the `r` option)

   e. Once completed, save the lilo.conf file using the `wq!` command
   f. On the serial console, type `lilo`

   When using Red Hat RHEL 4 U3:
   a. Edit the /boot/grub/grub.conf file
   b. Type `vi /boot/grub/grub.conf` (see Figure 36).
   c. Change the serial line to read:
      `serial --unit=0 --speed=9600 --word=8 --parity=no --stop=1`
   d. Change the kernel line to read:
      kernel /vmlinuz-2.6.9-34.ELsmp ro root=LABEL=/ console=ttyS0, 9600n8 rhgb quiet
      Here you are adding `console=ttyS0,9600n8 rhgb quiet` to the end of the kernel line, if it does not already exist.
   e. Type `:wq!` to save the changes.

Figure 36. Configuration for RHEL



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

2. Ensure that at least one `agetty` process is running on the serial port. To do this, modify the /etc/inittab file. Issue the `vi /etc/inittab` command and change the system console by adding or modifying the “co” service as follows:

   a. For MontaVista:
   ```
   co:2345:respawn:/sbin/agetty ttyS0 CON9600 vt102
   ```

   b. For Red Hat RHEL:
   ```
   co:2345:respawn:/sbin/agetty ttyS0 9600 vt100-nav
   ```

3. Reboot the blade.
4. Change HyperTerminal to 9600, 8, n, 1, n to make sure the BIOS, bootloader and OS come up at 9600 baud.
5. Optionally, if needed, configure the host OS IP address. This IP address can be the same or different as the IP address that will be assigned to the IPMC controller on the blade. The IP address of the host OS and IPMC should be on the same subnet. For the MPCBL0040 blade, use Eth4 for base interface port A.

   — For MontaVista:
   ```
   # vi /etc/network/interfaces
   ```

   — For Red Hat RHEL:
   ```
   # vi /etc/sysconfig/network-scripts/ifcfg-eth
   ```

9.8.1.3 sbcutils RPM Installation

The sbcutils RPM is installed via the following procedure. For complete details on sbcutils installation, refer to the sbcutilities RPM install procedure on the MPCBL0040 product page at http://www.radisys.com/service_support/tech_solutions/techsupportlib_detail.cfm?ProductID=1466.

1. Copy the RPM to the target blade. Ensure that the RPM copied is for the particular OS installed on the target blade.
2. Check the version of `sbcutils` installed: `rpm -q sbcutils`
3. If a previous version of the `sbcutils` RPM is installed, remove it by using this command: `rpm -e sbcutils`
4. Install a new version of `sbcutils` as follows:

   — For MontaVista 3.1:
   ```
   rpm -ivh sbcutils-1.3.0-3.i386-mv31.rpm
   ```

   — For MontaVista 4.0:
   ```
   rpm -ivh sbcutils-1.3.0-3.i386-mv40.rpm
   ```

   — For Wind River PNE 1.2:
   ```
   rpm -ivh sbcutils-1.3.0-3.i386-wr12.rpm
   ```

   — For Red Hat RHEL U3:
   ```
   rpm -ivh sbcutils-1.3.0-3.i386-rhel4.rpm
   ```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

9.8.1.4 Execute the reference_cfg Script

1. For Red Hat RHEL only: Before using the reference_cfg script, start the IPMI drivers. For MontaVista, the IPMI drivers start automatically.

   Start IPMI driver by issuing the following commands:

   — `# /etc/init.d/ipmi start` (this starts ipmi drivers for this particular session only)

   — `# chkconfig ipmi on` (this starts ipmi drivers by default on the next reboot)

Note: The following apply to commands in the three procedures in step 2, below:

— When the SOL client and SOL target are behind the same gateway, the "<Gateway MAC Addr>" and "<Gateway IP Addr>" parameters can be omitted.

— The "-l <SOL Target IPMB Addr>" parameter needs to be entered as "-l 0xNN", where NN is the IPMB address of the target blade. The IPMB address depends upon the location of the target blade in the chassis. Refer to Table 90, "Mapping of Physical Slot to IPMB Address in Promentum™ MPCHC0001 14U Shelf" on page 254 for the IPMB address for each physical slot in an MPCHC0001 chassis. Other chassis may have different IPMB addresses.

2. Choose one of the three interfaces below to execute the reference_cfg script. It does not matter which interface is chosen. The reference_cfg script can be executed through any of these interfaces.

   — **Script executed on the local SOL target blade payload**. Communication is from host processor to local IPMC through the KCS interface.

   Execute this command to configure SOL on the target blade:

   ```
   reference_cfg -I kcs -g -i <SOL Target IP Addr>
   ```

   — **Script executed on the RadiSys CMM**. Communication is from CMM to target blade through IPMB. This requires the MPCMM0001 or MPCMM0002 CMM and firmware version 6.1.0.2779 or later.

   a. FTP the /usr/bin/reference_cfg and /usr/lib/sbcutils/reference_funcs files to the CMM /home/scripts directory. The CMM default IP address is 10.90.90.91. If you cannot FTP to the CMM, at the CMM prompt, type `vi /etc/ftpusers` and comment out the root (# root). Then type `:wq!` to save the file.

   b. Execute the following command to the change the reference_cfg file attributes: `chmod 777 reference_cfg`

   c. Execute the following command to configure SOL on the target blade:

   ```
   reference_cfg -I ipmb -g -i <SOL Target IP Addr>
       -j <Gateway IP Addr> -n <Gateway MAC Addr>
       -l <SOL Target IPMB Addr>
   ```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

— **Script executed on a remote computer**. Communication is from the remote computer to the CMM through a LAN interface (RMPC), which is then bridged to the target blade's IPMC through the IPMB.

a. Transfer the /usr/bin/reference_cfg and /usr/lib/sbcutils/reference_funcs files to the remote computer using FTP.

b. Transfer the /usr/share/doc/sbcutils/cmdPrivilege.ini file to both the active and standby CMMs. Place the cmdPrivelege.ini file in the /etc/ directory. This file is needed to set up RMCP.

c. Reboot both CMMs.

d. Once the CMMs have booted, from the remote computer execute the following command:

```
reference_cfg -I lan  -g -i <SOL Target IP Addr>
    -j <Gateway IP Addr> -n <Gateway MAC Addr>
    -l <SOL Target IPMB Addr> -H <CMM IP Addr>
    -U root -P cmmrootpass -A md5
```

3. If the configuration script is successful, an output similar to the following is displayed on the console. Once the configuration has been successfully written to the SOL target blade, it is ready for a user to activate the SOL session from the client blade.

```
cmmget -l blade14 -t raw -d "0x06 0x41 1 0x80"
reference_cfg: Data response "0x2A 0x03"
reference_cfg: Success

cmmget -l blade14 -t raw -d "0x0C 0x21 1 0x01 0x01"
reference_cfg: Success

cmmget -l blade14 -t raw -d "0x0C 0x21 1 0x02 0x03"
reference_cfg: Success

cmmget -l blade14 -t raw -d "0x0C 0x21 1 0x03 0x07 0x2A"
reference_cfg: Success

cmmget -l blade14 -t raw -d "0x0C 0x21 1 0x04 0x03 0x0A"
reference_cfg: Success

cmmget -l blade14 -t raw -d "0x0C 0x21 1 0x05 0x06"
reference_cfg: Success

cmmget -l blade14 -t raw -d "0x0C 0x21 1 0x06 0x06"
reference_cfg: Success
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

9.8.2 Client Blade Setup

The client blade is the SOL blade that will activate SOL on the target and receive serial output from the target. The output is displayed on the client console.

Ensure that the MPCBL0040 SBC has the following firmware/OS versions loaded:

- IPMC Firmware 1.03.01 or later
- BIOS P02-00014 or later
- System must be running a Linux* OS
- ipmitool 1.8.7 or later running on the client blade

Note: ipmitool needs to be installed on a Linux* computer and that computer can be located anywhere in the network. In the example described in this section, ipmitool is running on another blade in the same chassis.

9.8.2.1 Configure Ethernet Port

For MontaVista 4.0:

1. Configure the IP address of the Ethernet port using:
   `vi /etc network interfaces`

```
auto lo ethN
iface lo inet loopback
auto ethN
iface ethN inet static
    address 192.168.0.42
    network 192.168.0.0
    netmask 255.255.255.0
    broadcast 192.168.0.255
    gateway 192.168.0.1
```

2. Restart the network using the command:
   `/etc/init.d/networking restart`

For Red Hat RHEL:

1. Configure IP address of Ethernet port using:
   `vi /etc/sysconfig/network-scripts/ifcfg-ethN`

```
ifcfg-eth4
BOOTPROTO=static
IPADDR=10.90.90.113
NETMASK=255.0.0.0
ONBOOT=yes
TYPE=Ethernet
DHCP_HOSTNAME=rhel4u3
```

2. Execute this command to restart the network: `service network restart`

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

9.8.2.2 Installing ipmitool

1. Download ipmitool version 1.8.7 or later from http://ipmitool.sourceforge.net/
2. Install the ipmitool on the client blade. The ipmitool provides the SOL client interface.
3. Type: `tar zxvf  ipmitool-1.8.7.tar.gz`
4. Change directory to the ipmitool directory created after tar:
   `cd ipmitool-1.8.7`
5. Type: `./configure`
6. Type: `make install`
7. For Red Hat RHEL only: Before using ipmitool, start the ipmi drivers. In MontaVista, the IPMI drivers start automatically.
   — Start the IPMI driver by issuing the following commands:
   `# /etc/init.d/ipmi start`
   (this command starts the ipmi drivers for this particular session only)

   `# chkconfig ipmi on`
   (this command starts the ipmi drivers by default on the next reboot)
8. If the computer that ipmitool was just installed on has a local IPMC, the ipmitool installation can be tested by typing: `ipmitool raw 6 1`. If ipmitool is running correctly, the response should be in a format similar to:

```
20 81 01 03 02 3f 57 01 00 0c 08 01 05 01 00
```

9.8.2.3 Starting an SOL Session

Before starting an SOL session, first make sure you can `ping` the target blade.

On the client blade, execute this command:

```
# ipmitool -I lanplus -L operator -H <SOL Target IP addr>
    -U solusername -P  soluserpassword sol activate
```

If the SOL session is activated successfully, the following message is displayed:

```
[SOL Session operational.  Use ~? for help]
```

Press enter and you should see the target output on the console.

If the SOL session does not activate, run this command to see how ipmitool is configured:

```
# ipmitool -I lanplus -L operator -H <SOL Target IP Addr>
    -U solusername -P  soluserpassword sol info
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

9.8.2.4 Checking SOL Configuration

To check the SOL configuration, the following command can be issued.

Note: This requires ipmitool to be installed on the SOL target blade also.

Use `ipmitool lan print 1` to display configuration for the 1st eth channel (this Ethernet port is connected to Ethernet switch located in Slot #7 on the MPCH0001 chassis) and `ipmitool lan print 2` to display configuration for the 2nd eth channel (Ethernet switch located in Slot #8).

```
root@DRBlade14:/usr/bin# ipmitool lan print 1
Set in Progress         : Set Complete
Auth Type Support       : NONE MD2 MD5 PASSWORD
Auth Type Enable        : Callback :
                        : User     :
                        : Operator :
                        : Admin    :
                        : OEM      :
IP Address Source       : Unspecified
IP Address              : 10.90.90.14
Subnet Mask             : 255.255.255.0
MAC Address             : 00:0e:0c:98:55:6e
SNMP Community String   :
IP Header               : TTL=0x40 Flags=0x40 Precedence=0x00 TOS=0x10
BMC ARP Control         : ARP Responses Disabled, Gratuitous ARP Disabled
Gratituous ARP Intrvl   : 2.0 seconds
Default Gateway IP      : 0.0.0.0
Default Gateway MAC     : 00:00:00:00:00:00
Backup Gateway IP       : 0.0.0.0
Backup Gateway MAC      : 00:00:00:00:00:00
RMCP+ Cipher Suites     : None
Cipher Suite Priv Max   : XXXXXXXXXXXXXXX
                        :     X=Cipher Suite Unused
                        :     c=CALLBACK
                        :     u=USER
                        :     o=OPERATOR
                        :     a=ADMIN
```

9.8.2.5 Ending an SOL Session

To use the front panel serial console port on the target blade, end the SOL session.

To end the SOL session:

1. Type: **~**. (Note: After pressing ~ just once, this symbol does not appear on the console screen. This is done at the login prompt.)
2. After typing **~** the SOL session deactivates on the SOL target blade. To make sure the target blade SOL session is deactivated, type the following command:

```
# ipmitool -I lanplus -L operator -H <SOL Target IP Addr>
    -U solusername -P soluserpassword sol deactivate
```

SOL is stopped completely and the serial console port is now redirected to the front panel of the SOL target blade.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

9.8.2.6 Recovering SOL Session if ipmitool Segfaults

If ipmitool segfaults while in a SOL session and another SOL session is immediately activated, ipmitool will not be able to establish a new session because no SOL close session occurred. Ipmitool is still receiving encrypted packets from the previous SOL session and is expecting to receive encrypted packets that are responses to the new SOL session establishment commands.

There are two ways to recover:

- Wait for 60 seconds + 3 seconds (approximately) before establishing new SOL session. The IPMC firmware takes 60 seconds (session timeout) to clear the session.
- Using ipmitool, do an explicit Deactivate and then Activate a new SOL session:

Deactivate the SOL session:

```
# ipmitool -I lanplus -L operator -H <SOL Target IP Addr>
    -U solusername -P soluserpassword sol deactivate
```

Reactivate the SOL session:

```
# ipmitool -I lanplus -L operator -H <SOL Target IP Addr>
    -U solusername -P soluserpassword sol activate
```

9.9 Operating Systems for SOL Client (ipmitool)

The SOL client utility (ipmitool) can be compiled to work with any Linux* OS.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.0 Firmware Update Utilities

10.1 Firmware and BIOS Locations

For the latest firmware and BIOS, go to the MPCBL0040 download page at:

http://www.radisys.com/service_support/tech_solutions/techsupportlib_detail.cfm?ProductID=1466

10.2 BIOS Image Updates

At times, new BIOS images will be released to add features or fix issues.

- The BIOS image needs to be executed locally on-board.
- The BIOS image update utilities will only work under MS-DOS* and Linux*.
- If doing updates remotely, FTP the update utility and the P-xxxx.rom file to the board and use telnet to login to execute the BIOS updates.

Note: Ensure that binary mode is used when transferring the P-xxxx.rom file using FTP.

10.2.1 Updating BIOS under MS-DOS

The following is a step-by-step procedure to update the BIOS under MS-DOS.

1. Copy the flash utility (Flashdos.exe) and the P-xxxx.rom file to an MS-DOS bootable floppy disk.
2. Boot the board from a USB floppy disk/USB flash drive (connected to the USB port) to an MS-DOS prompt.
3. Copy the flash utility and BIOS ROM image to RAM disk, which is automatically generated (C: drive).
4. Issue the command `flashdos /b P-xxxx.ROM` command.
5. Type Y to overwrite the BIOS on the board.
6. Type Y to clear the current CMOS settings on the board (if desired).
7. Type Y to reboot the system after the BIOS has been upgraded successfully.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.2.2 Updating BIOS under Linux (Interactive mode)

This method requires operator/human intervention. The following is a step-by-step procedure to update the BIOS under Linux.

1. Copy the flash utility (flashlnx) and the P-xxxx.rom file to the SBC (via FTP/etc.). Ensure both the flash utility and the P-xxxx.rom file are in the same directory.
2. Issue the `./flashlnx -b P-xxxx.ROM` command.
3. Type Y to overwrite the BIOS on the board.
4. Type Y to clear the current CMOS settings on the board (if desired).
5. Type Y to reboot the system after the BIOS has been upgraded successfully.

10.2.3 Updating BIOS under Linux (Quiet Mode)

The BIOS update utility supports quiet mode, where messages are not sent to the screen. This mode can be used for automatic (programmatic) invocations of the update utility.

To update the BIOS automatically without human intervention or responses to prompts, execute the `./flashlnx -q -b P-xxxx.ROM` command.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.2.4 Synchronizing BIOS Image and Settings from FWH0 (Main) to FWH1 (Backup)

Prior to upgrading the main BIOS (FWH0), a user can create a mirror image where it will copy all the operational codes and CMOS settings to redundant BIOS Flash device. It is suggested the user preserves a copy of the old BIOS image prior to updating the main BIOS in case FWH0 update fails.

The syntax `./flashlnx -m` can be used to initiate this transfer. Refer the suggested method in Table 82.

Table 82. Suggested Method of BIOS Image Synchronization prior to BIOS Upgrade

BIOS Image	Command	Behavior
FWH0 Image N FWH1 Image N-1		• This is the original FWH images before an upgrade. • FWH0 has Image N installed, which is a newer image than what is installed in FWH1, which is Image N-1.
FWH0 Image N FWH1 Image N	./flashlnx –m	• The user can initiate a BIOS update while the OS is running. • When this command is executed, the Image N in FWH0 (BIOS codes + CMOS settings) is synchronized to FWH1. Image N has now been copied to the backup FWH1 BIOS image. • No reboot is needed for this operation.
FWH0 Image N+1 FWH1 Image N	./flashlnx –b Pxx-xxxx	• When this command is initiated, the FWH0 image will be updated to the latest version (Image N+1). • The latest version of the BIOS will take effect after the user initiates a reset. • If a checksum error is detected on FWH0 after a reboot, it will automatically switch to FWH1 and regain normal operation.
Note: N = BIOS version		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.2.5 Copying and Saving BIOS (Including CMOS Settings)

The CMOS settings, together with the BIOS binary image, can be copied to a file with a file name specified by the user. This feature is useful if you wish to use one standard CMOS configuration or BIOS settings across multiple MPCBL0040 boards.

10.2.5.1 Copying BIOS.bin from the SBC

1. Copy the flashlnx utility to the SBC. This SBC is the one with custom CMOS settings that will be used to update other SBCs.
2. Issue the `./flashlnx -r -afff00000 -s1048576 BIOS.bin` command to copy the BIOS with the customized CMOS settings to the same directory from which the flashlnx utility is executed. All user preferred settings (including the BIOS image) are saved in the file named BIOS.bin.

Note: BIOS.bin is a generic file name used here to illustrate the command line used to perform the operation. You may wish to use a filename that reflects the BIOS version (for example, P0x-00yy.bin) instead of BIOS.bin.

10.2.5.2 Saving BIOS.bin to the SBC

1. Copy the flashlnx utility and BIOS.bin to the SBC running MontaVista* Carrier Grade Linux.
2. Execute `chmod +x flashlnx` to change the file attribute to an executable form.
3. Execute `./flashlnx -b -zc BIOS.bin` to copy the BIOS.bin file to the FWH and CMOS.
4. Upon completion, perform a reset to ensure that the new CMOS settings and BIOS are loaded.

Caution: To ensure that the BIOS.bin file is not corrupted, RadiSys strongly suggests performing these steps before major deployment of any SBCs running in a live network environment.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.2.6 BIOS Utility Command Line Options

Table 83 lists the command line parameter switches and features supported by the BIOS flash utility.

Table 83. Flashdos Utility Command Line Options

Command Line Parameter	Description
/b [option] bios_image where possible [option] values are: • /z - do not clear the CMOS • /zc - update the CMOS from image	Program a BIOS image to primary fimware hub (FWH0)
/i [bios_image]	Display BIOS system information
/r [options] bin_image where possible [option] values are: • /aAddress - physical address in hex • pPage - page number in decimal • /sSize - image size in decimal	Read the flash image and store to a file
/m	Mirror image where all the operational codes and CMOS settings are copied from FWH0 to FHW1 (redundant BIOS flash device)
/b cmos_image	Backup current CMOS settings to a file
/r cmos_image	Restore CMOS settings from a file
/q	Force non-interactive mode (assumes “yes” for all prompts)
Note: The command line parameters shown reflect flashdos usage, where command line options use the “/” symbol. When using flashlnx, replace “/” with “-”.	

10.3 Updating IPMC Firmware

The following subsections describe step-by-step procedures for updating the IPMC boot block and IPMC operational code.

IPMC firmware updates are divided into two phases:

- Boot block update - not typically needed
- Operational code update - most common form of update

The procedure for updating the boot block is in the following section, “Updating IPMC Boot Block”.

The procedures for updating the operational code are located in Section 10.6.7, “Direct Firmware Update” on page 219 and Section 10.6.8, “Staged Firmware Update” on page 223.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.3.1 Updating IPMC Boot Block

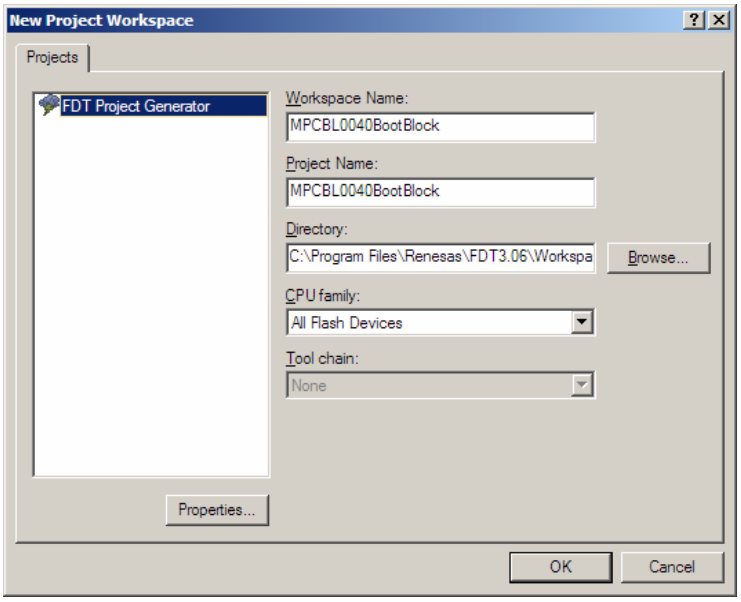
It is recommneded that the IPMC Boot Block update is done on a computer using a COM port. It is possible to update the boot block from a computer with a USB to serial adapter, but some USB to serial adapters have found to be less reliable and using this USB to serial adapter may cause some intermittent communication or timeout errors when doing the update.

1. Update the IPMC firmware using the staged firmware update mode. Refer to Section 10.6.8, “Staged Firmware Update” on page 223. This step is performed first to ensure a valid IPMC operational code is saved into the into the rollback area. Once the boot block is updated, the IPMC operational code is erased and the next time the board boots, the IPMC operational code that is in the rollback area will be automatically copied to the IPMC and the board will boot.
2. One the MPCBL0040 board, change the DIP switch positions as follows:
   a. Set SW4.9 to OFF (COM port to IPMC)
   b. Set SW5.9 to OFF (enable IPMC serial update mode)

Note: All other DIP switches should be in the ON state.

3. Reinsert the blade into the chassis.
4. Connect a serial cable to the front panel serial port.
5. Start the Renesas* Flash Development Toolkit. The program to download is the latest version of the “[Evaluation Software] Flash Development Toolkit V.X.XX”. This Renesas toolkit can be downloaded from: http://www.renesas.com/fmwk.jsp?cnt=/download_search_results.jsp&fp=/support/downloads/download_results&layerId=1050
6. Create a new project workspace named “MPCBL0040BootBlock”. See Figure 37.

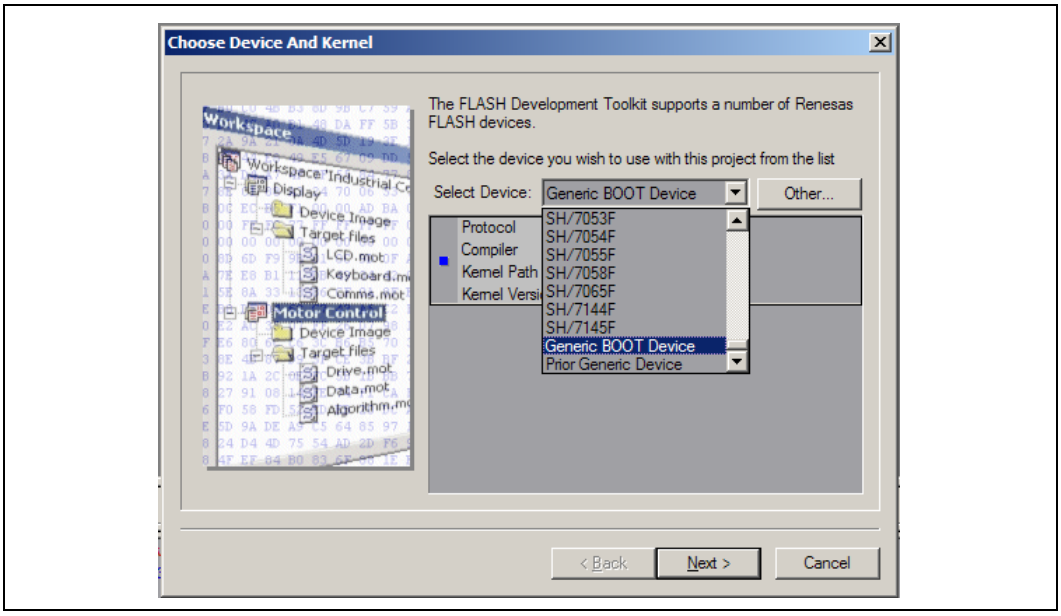
Figure 37. Creating a New Project Workspace



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

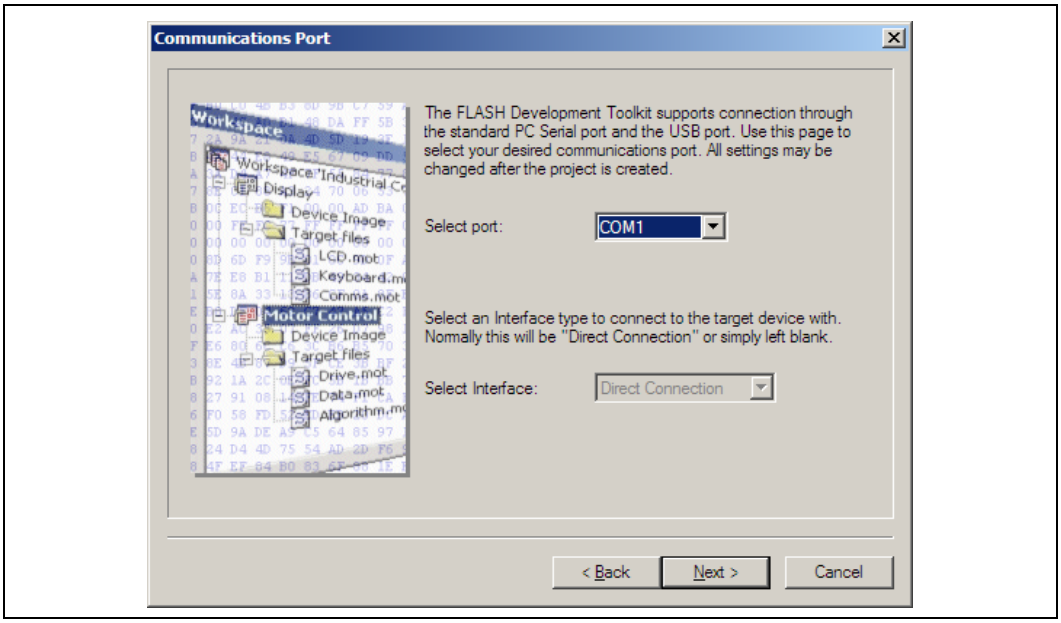
a. Select “Generic Boot Device” at the bottom of the pull-down menu. See Figure 38.

Figure 38. Selecting a Boot Device



b. On the next screen, select the **COM** port connected to the board. See Figure 39.

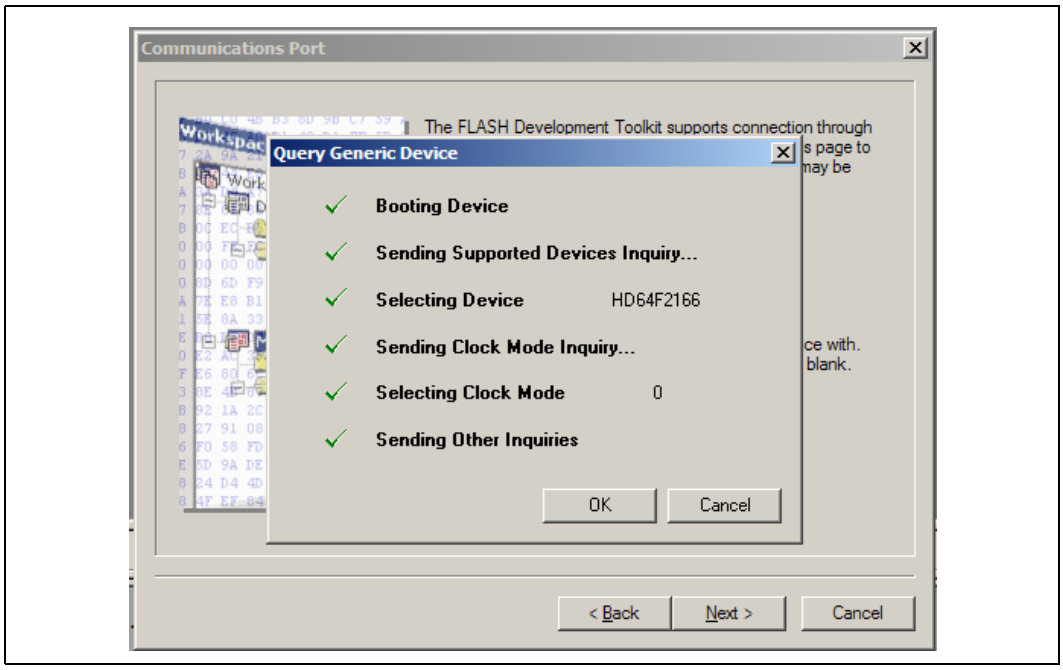
Figure 39. Selecting a COM Port



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

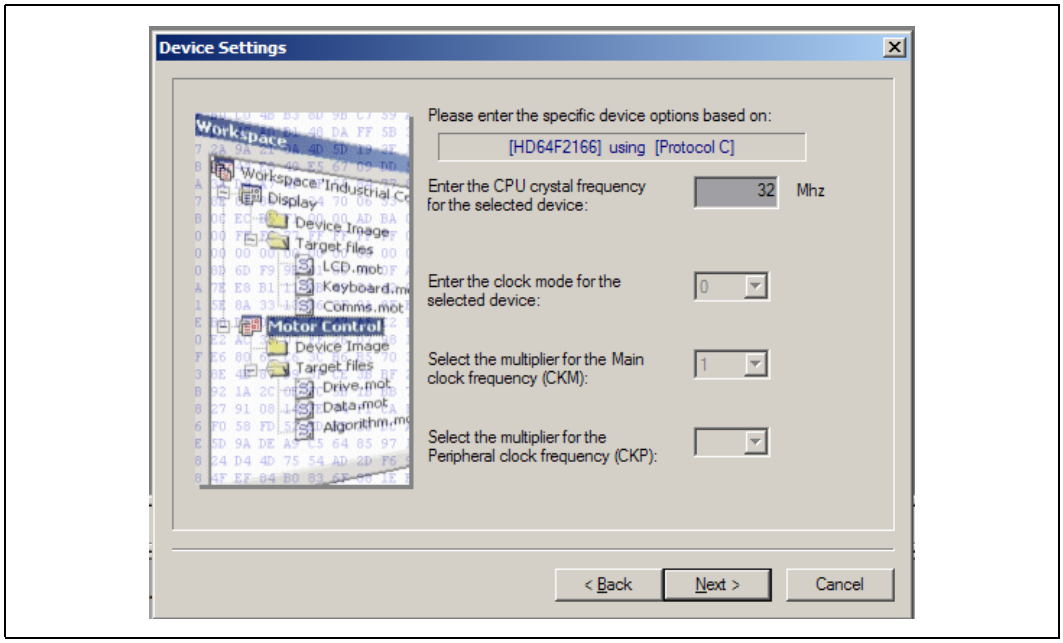
c. After selecting a COM port, Renesas* attempts to query the device. The following dialog is displayed. See Figure 40.

Figure 40. Query Device



d. In the **Device Settings** window, change the CPU crystal frequency to 32 MHz. See Figure 41.

Figure 41. Changing CPU Crystal Frequency



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

e. Use the defaults for the remaining device settings.

f. Click **Next>** until you reach the end of the section.

7. Under the **Project** menu, right-click the project name and choose **Add Files**.
8. Add the file MPCBL0040_BL_XXX.mot (IPMC bootloader)
9. Right-click the MPCBL0040_BL_XXX.mot filename and choose **User Boot Flash**.
10. Right-click the MPCBL0040_BL_XXX.mot filename again and choose **Download File to [User Boot Flash]**.
    The following text (or similar) should appear at the bottom of the screen after successful completion of the update procedure:

```
Loaded the Write operation module
Writing image to device... [0x00000000 - 0x000009FF]
Writing image to device... [0x00001F80 - 0x00001FFF]
Data programmed at the following positions:
 0x00000000 - 0x000009FF      Length : 0x00000A00
 0x00001F80 - 0x00001FFF      Length : 0x00000080
2.73 K programmed in 1 seconds
Image successfully written to device
```

11. After the boot block updates successfully, confirm matching checksums by right clicking on the filename “MPCBL0040_BL_101.mot”, then “Compare File-> Device Checksum”. Verify the checksum of the file matches the checksum of the device.
12. Exit the program.
13. Eject blade or power down (including standby power) the SBC.
14. Change the SW4 and SW5 switches to their default positions (all switches set to ON):
    — Set SW4.9 to ON (COM port to SBC).
    — Set SW5.9 to ON (disable IPMC serial update mode).
15. Reinsert the blade into the chassis.
16. If there is a IPMC operational code in the rollback area, this will be copied automatically to the IPMC and the board will boot. Once the board boots, then update the IPMC firmware using the staged firmware update mode. Refer to Section 10.6.8, “Staged Firmware Update” on page 223. The rest of the steps in this procedure do not need to be followed.
17. If the board doesn’t boot, there was not valid IPMC operational code image in the rollback area. If this happens, press and release the front panel reset button. This will force the board payload power to turn on. Then follow the remaining steps in this section.

Note: The board does not boot up until the front panel reset button is pressed and released.

18. Once the board boots, the IPMC operational code must be updated using the direct firmware update mode. Staged firmware update mode does not work the first time after updating the boot block. Refer to Section 10.6.7, “Direct Firmware Update” on page 219.
19. After the direct IPMC firmware update, the board payload power will be cycled and the board will automatically reboot. This reboot only occurs after the boot block is updated followed by an IPMC operational code update. All subsequent IPMC firmware updates do not impact payload power.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.3.2 Updating RTM Boot Block

1. Change the RTM DIP switch positions as follows:
   — Set SW1.9 to OFF.
   — Set SW1.10 to OFF.
2. Connect a serial cable to RTM connector P8. This requires a custom cable with the pinout shown in Table 84.

Table 84. RTM Boot Block Serial Port Pinout

Signal Name	Connector P8 on the RTM	Serial Port Cable DB-9 Connection
Tx (Transmit)	Pin 1	Pin 2
Rx (Receive)	Pin 2	Pin 3
No Connect	Pin 3	No connect
Ground	Pin 4	Pin 5

3. Follow steps 3 through 8 in Section 10.3.1, “Updating IPMC Boot Block” on page 202. At step 4, name your workspace “MPRTM0040BootBlock”. The name of the RTM file for step 5 is “BB-RT10x.mot” (where, x is the version number).
4. After the boot block code has been programmed, change the DIP switch positions as follows:
   — Set SW1.7 to OFF.
   — Toggle SW1.8 OFF then ON.

Note: The DIP switches can be toggled with the RTM still powered and plugged in or you can pull out the RTM to toggle the switches.

5. After the boot block is updated, the RTM firmware must also be updated. The firmware update requires the -force-fw-update option. Refer to Section 10.6.7, “Direct Firmware Update” on page 219.

10.4 SBC Utilities Installation Procedure

The SBC utilities and the supporting libraries are packaged together and released as a single RPM package manager archive (RPM). This rpm file is included as part of the MPCBL0040 IPMC Update Utilities package. The filename is “MPCBL0040-sbcutils-w.x.y-z.i386-mv40.rpm”, where MPCBL0040 refers to the Single Board Computer. This utility is specifically created for this board only.

- *x* refers to the software generation number.
- *y* refers to the Interim Product Release number. This is typically changed when the release includes bug fixes.
- *z* refers to the build number of the software.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.4.1 Contents of SBC Utilities RPM Package

The SBC utilities rpm includes the following:

- sbcupdate - a binary tool that is used to perform an IPMC firmware upgrade. It also updates FRU and SDR information on the SBC and the RTM.
- reference_cfg - a reference configuration script that contains all the necessary IPMI commands to enable and configure the SBC for SOL functionality on the MPCBL0040SBC.
- reference_funcs - a support file that contains functions used by the reference_cfg script.

Note: ipmitool is the SOL client for the SBC. This tool is not part of the SBC utilities RPM package, but is discussed in this chapter.

10.4.2 Remove Existing Packages

Before installing the RPM on a host system (Single Board Computer), verify that a different version of the sbcutils RPM is not currently installed.

To check if a package has been installed on the system before, execute this command:

```
# rpm -q sbcutils
```

Either the rpm tool returns the version of the installed package or it reports that no package is installed.

If a version of the sbcutils package is already installed, the user must remove it before attempting to install the latest version. If the user attempts to install the latest version of the sbcutils package before resolving this conflict, the rpm tool will fail with the error message similar to:

```
Error: Failed Dependencies

sbcutils conflicts with sbcutils-1.1.0.1
```

To remove the existing installation, execute the following command:

```
# rpm -e sbcutils
```

10.4.3 Installing the sbcutils Package

Once older packages have been removed from the host system, execute the following command to install the sbcutils package:

```
# rpm -ivh sbcutils-1.1.0-1.i386-mv31.rpm


Preparing...        ########################################### [100%]
   1:sbcutils       ########################################### [100%]
```

- -i specifies an installation operation.
- -v requests verbose output.
- -h causes hash characters to be displayed to indicate the progress of the installation.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.5 System Configuration

10.5.1 Introduction

If the sbcupdate utility is to be used with RMCP, it is essential that communication between the target IPMC and a remote network node via a shelf manager can be established.

The shelf manager must bridge IPMI messages between the LAN and IPMB bus. If this feature can be disabled, make sure that bridging is in the enabled state before attempting RMCP bridge communication. Furthermore, if the shelf manager supports filtering and privilege settings for individual IPMI commands, make sure that the IPMI commands listed in Table 85 are not filtered and are set to the indicated privilege levels. Table 85 is the list of commands that must be FORWARDED from the LAN to the IPMB.

Table 85. Required IPMI Command Privileges for RMCP Bridging

IPMI Command	Net Function	Command	Privilege Required
Get Device ID	06h	01h	User
Cold Reset	06h	02h	Admin
Set Channel Access	06h	40h	Admin
Get Channel Access	06h	41h	User
Set User Name	06h	45h	Admin
Set User Access	06h	43h	Admin
Set User Password	06h	47h	Admin
Set User Payload Access	06h	4Ch	Admin
Enter Firmware Transfer Mode	08h	00h	Admin
Firmware Program	08h	01h	Admin
Firmware Read	08h	02h	Admin
Exit Firmware Transfer Mode	08h	04h	Admin
Set Program Segment	08h	05h	Admin
Get FRU Inventory Information	0Ah	10h	User
Read FRU Data	0Ah	11h	User
Write FRU Data	0Ah	12h	Operator
Get SDR Repository Info	0Ah	20h	User
Reserve SDR Repository	0Ah	22h	User
Get SDR	0Ah	23h	User
Partial Add SDR	0Ah	25h	Operator
Clear SDR Repository	0Ah	27h	Operator
Set LAN Configuration Parameters	0Ch	01h	Admin
Set Serial/Modem configuration	0Ch	10h	Admin
Set SOL Configuration Parameters	0Ch	21h	Admin
Get PICMG Properties	2Ch	00h	User
Get Address Info	2Ch	01h	User
Get Serial Buffer [1]	30h	30h	User
Set Serial Buffer Configuration [2]	30h	32h	User
Online Update Prepare For Update	30h	A0h	Admin

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 85. Required IPMI Command Privileges for RMCP Bridging (Continued)

IPMI Command	Net Function	Command	Privilege Required
Online Update Open Area	30h	A1h	Admin
Online Update Write Area	30h	A2h	Admin
Online Update Close Area	30h	A3h	Admin
Online Update Register Update	30h	A4h	Admin
Online Update Capture Rollback Image	30h	A5h	Admin
Online Update Get Status	30h	A6h	Admin
Online Update Get Capabilities	30h	A7h	Admin

Notes:
1. This command is needed only when using the reference_sbr script. Not all SBCs support this feature.
2. This command is needed only if Serial Buffer Reading configuration is enabled in the reference_cfg script. Not all SBCs support this feature.

10.5.2 Configuring the Promentum™ MPCMM0001/0002 CMM

This section describes the procedure to configure the Promentum™ MPCMM0001/0002 Chassis Management Module (CMM) to support RMCP bridging.

The CMM filters individual IPMI commands for bridging based on the /etc/cmdPrivillege.ini CMM configuration file. (Note that the double “l” in the filename is spelled this way on purpose.) Each combination of net function and command number can be given a custom privilege level. Each combination can also be disabled, in which case the command is not bridged between the LAN and IPMB. This is an example cmdPrivillege.ini file, which can be modified if needed. Even without modifications, the file is working and can be used as is.

Copy cmdPrivillege.ini File

1. After the sbcutils installation, copy the cmdPrivillege.ini file from the sbcutils installation path (/usr/share/doc/sbcutils) directory to the CMM’s /etc path. Copy the cmdPrivillege.ini file to both the active and standby CMMs.
2. After any change to this configuration file, both CMM RMCP server’s must be restarted to enable the changes to take effect. To stop and then start the RMCP server, execute the following commands in sequence. Note, this must be done on both CMMs at the same time (within 10 to 15 seconds of each other):

```
# cmmset -d rmcpenable -v 0
Success
# cmmset -d rmcpenable -v 1
Success
```

Note: On some versions of the CMM firmware, enabling the RMCP server results in an error for the first 10 to 15 attempts before the server is successfully restarted.

```
# cmmset -d rmcpenable -v 1
IMB ERROR Completion Code Error.
# cmmset -d rmcpenable -v 1
IMB ERROR Completion Code Error.
# cmmset -d rmcpenable -v 1
IMB ERROR Completion Code Error.
# cmmset -d rmcpenable -v 1
IMB ERROR Completion Code Error.
# cmmset -d rmcpenable -v 1
IMB ERROR Completion Code Error.
# cmmset -d rmcpenable -v 1
IMB ERROR Completion Code Error.
# cmmset -d rmcpenable -v 1
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

```
IMB ERROR Completion Code Error.
# cmmset -d rmcpenable -v 1
Success
```

3. To verify the RMCP enable state, use the following command. A “0” indicates disabled and “1” indicates enabled.

```
# cmmget -d rmcpenable
1
```

Details of cmdPrivillege.ini File

The first section in the cmdPrivillege.ini file lists the net functions to be configured and gives each net function value a mnemonic string equivalent.
For example:

```
[IPMI]
NumNetFunc=25
NetFunc00=Chassis
NetFunc02=Bridge
NetFunc04=S_E
NetFunc06=App
NetFunc08=Firmware
NetFunc0A=Storage
NetFunc0C=Transport
NetFunc2C=PICMG
NetFunc30=Platform
```

The “NumNetFunc” field should be set to the value of the largest net function (30h hexadecimal or 48 decimal in the above example), divided by two, plus 1. This field must be set with a decimal number.

Each subsequent section of this file starts with a net function string equivalent, followed by the number of commands in the section, followed by an ordered, zero-based list of command numbers and privilege levels. For example, the section that configures commands of net function 0Ch starts this way:

```
[Transport]
NumCMD=35
00=D
01=A
02=O
03=D
04=D
```

The “NumCMD” field should be set to the highest command number of the section plus one and written in decimal format. Each command number is assigned a one character code to indicate the desired privilege level and enabled state. Any command number that is not a defined command should be disabled.

The character codes used in the cmdPrivillege.ini file are as follows:

- D - Disabled
- U - Enabled with user privilege
- O - Enabled with operator privilege
- A - Enabled with administrator privilege

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6 SBC Update Utility

This section is an overview of the SBC Update tool used to update the IPMC firmware on Single Board Computer. This tool also can update FRU and SDR information on the SBC and the RTM.

10.6.1 Communication Interfaces

Graphical examples of the communication interfaces used for firmware updates are provided in this section.

The term “payload” is used in following graphics and refers to the CPU(s) of a SBC that perform user-specific computational tasks.

Figure 42. KCS - Local Communication from CPU to Local IPMC

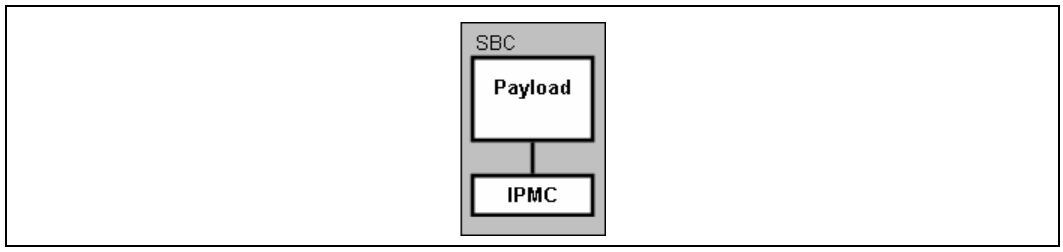


Figure 43. KCS Bridge - Local Communication from CPU to LOCAL IPMC Bridged to RTM

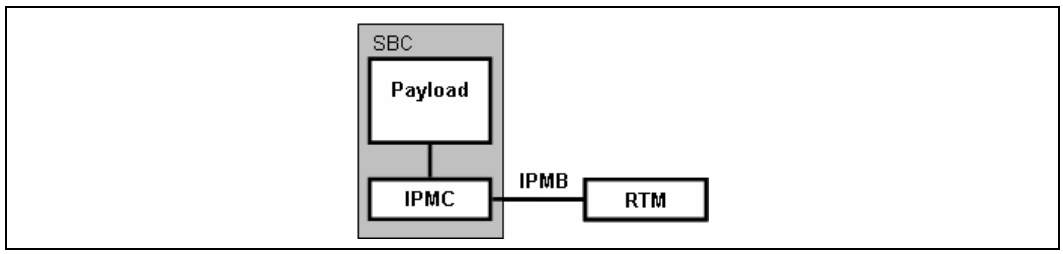


Figure 44. RMCP Bridge - Remote Communication to Shelf Manager Bridged to IPMC

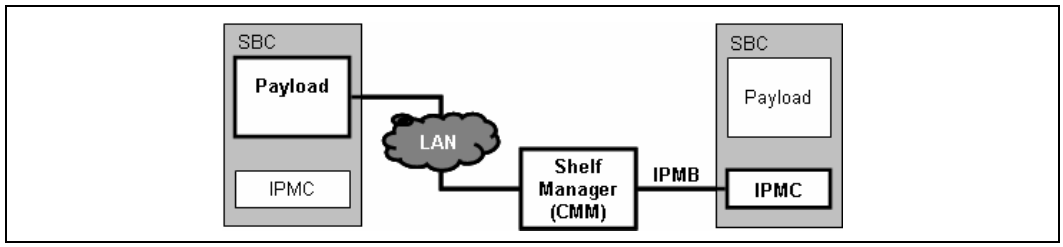
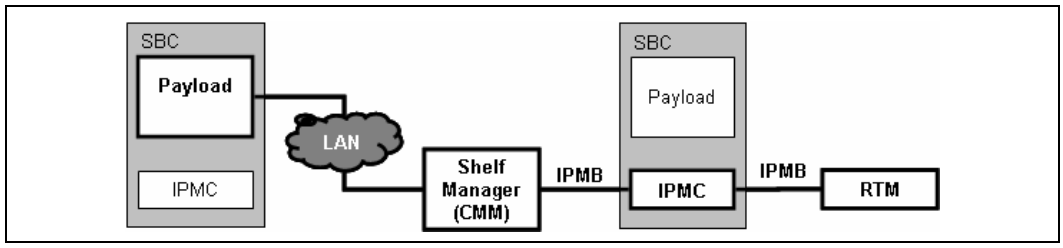


Figure 45. RMCP Double Bridge - Remote Communication to Shelf Manager Bridged to IPMC then Bridged to the RTM



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Figure 46. IPMB - Remote Communication from Shelf Manager to IPMC

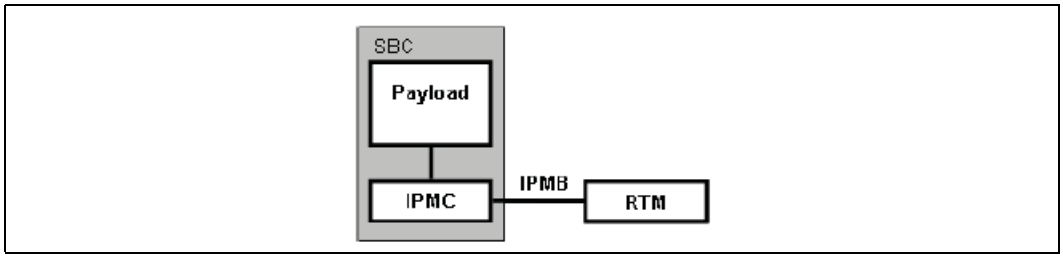
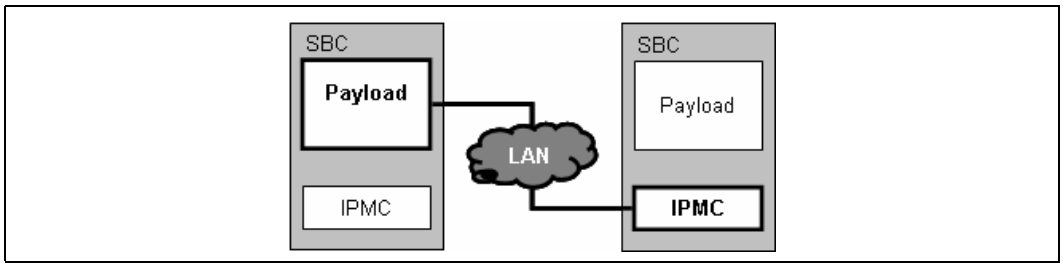


Figure 47. RPMC + Direct - Remote Communication to IPMC Directly through LAN Interface



10.6.2 IPMC Operational Code Firmware Update Modes

There are two update modes:

- **Direct Update Mode** - This upgrade procedure happens when the user updates the IPMC firmware directly to the internal flash on the IPMC. The user does not have the ability to back up the “old” operational image.
- **Staged Update Mode** - The Staged Update feature allows the IPMC operational code to be updated while the system is online (OS is running). After the new image has been staged, it is copied to the internal flash of the IPMC upon completion of the staged upgrade. If the switchover fails, or at the user's discretion, the firmware may be rolled back to the previous version.

  The advantage of running this mode is that the user can store the old firmware image to a rollback region (for redundancy purposes). A pending firmware update may also be created allowing the user to continue to use the current firmware before the actual update.

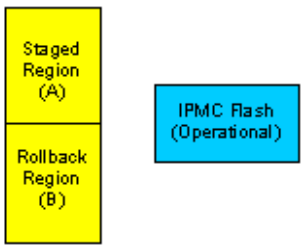
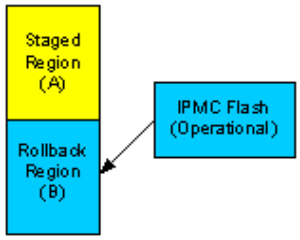
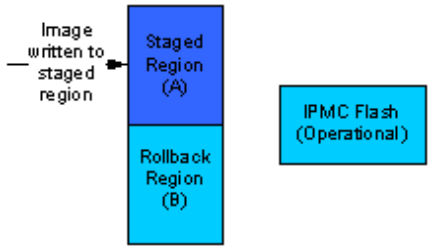
The following section provides an overview of the staged update process. See Section 10.3, “Updating IPMC Firmware” on page 201 for more details and the procedure for updating IPMC firmware.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.3 Staged Update Process

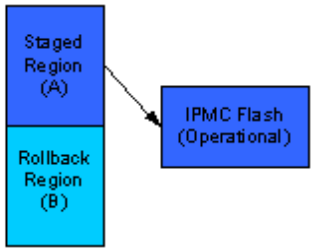
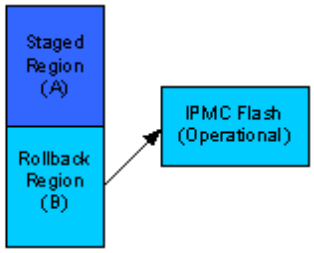
Table 86 explains the process of an online staged update. The diagrams in the table are color-coded to show old, new, or no firmware images, as indicted.

Table 86. Staged Update Process

Scenario	Behavior	Actions
Fresh from production/ factory		This is the original firmware composition when a board is shipped from a factory. Both external flash partitions are empty.
Initiating online staged update (step 1)		When a staged firmware update is initiated, depending upon user specified command options, the sbcupdate utility first copies the current operational image into the rollback region(B).
Copying new image to the staged region (step 2)		The new firmware image is written to Staged Region (A) of the external flash. Note that the IPMC continues to operate with the original operational firmware image, even after the online update has been successfully staged. The IPMC needs to be reset for the new firmware image to be transferred to the IPMC from Staged Region (A).
Legend: 		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 86. Staged Update Process

Scenario	Behavior	Actions
Activating the staged image (step 3)		Upon completion of the staged update, the new firmware image from staged region is written to operational image (internal flash of IPMC).
Initiating a rollback (optional)		User can initiate a rollback by invoking the rollback option with SBC update utility. Upon IPMC reset, an automatic rollback recovery can occur if the IPMC boot block detects incomplete update or checksum error with the IPMC firmware image. User can initiate a rollback by invoking the rollback option with SBC update utility. If the force rollback option is used and there isn't a valid rollback image, the IPMC will enter direct firmware update mode.
Legend: 		

10.6.4 Firmware Naming Scheme

Firmware for both the IPMC of the MPCBL0040 SBC and the RTM has a standard naming scheme. The letter “N” is given with the file name which refers to the version of the update. In all instances, replace the sequence of “N”s with the number of your update file.

IPMC naming:

- MPCBL0040_FW_NNNN.hex - IPMC firmware update
- MPCBL0040_NNN.sdr - SDR update
- MPCBL0040_NNN.fru - FRU update

RTM naming:

- MPRTM0040_FW_NNNN.hex - RTM firmware update
- MPRTM0040_NNN.sdr - RTM SDR update
- MPRTM0040_NNN.fru - RTM FRU update

For example, here is the IPMC firmware update for version 1.07.01:

- MPCBL0040_1071.hex

Here is an example IPMC FRU update for version 0.15:

- MPCBL0040_015.fru

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.5 Utility Invocation

Note: The section refers to sbcupdate version 1.3.3-1

The general format for utility invocation is:
`sbcupdate [<options>] [<input-files>]`

Each option has a long-form name that consists of two dashes followed by a multi-character string of letters, numbers, and dashes. For long-form options that take arguments, the argument values are separated from the option name by one or more spaces or the '=' operator.

For example, this command uses the long form of an option with no arguments:

```
# sbcupdate --mode
```

The following command uses the long form of an option that takes an argument:

```
# sbcupdate --mode staged
```

or

```
# sbcupdate --mode=staged
```

Many options also have an alternate short-form name that follows the POSIX conventions for command-line options, namely, a single dash followed by a single letter. For short-form options that take arguments, the argument values are either concatenated to the end of the option name or separated by one or more spaces.

For example, this command uses the short form of an option with no arguments:

```
# sbcupdate -M
```

This command uses the short form of an option that takes an argument:

```
# sbcupdate -M staged
```

This command uses the short form without a space separating the option and the argument:

```
# sbcupdate -Mstaged
```

Throughout the chapter, the short-form syntax is used. Any short-form option may be substituted with the long form. If the long form is preferred, see Table 87, "Common Command Line Options and Arguments" on page 216.

After any options and option arguments are supplied on the command line, any remaining strings are interpreted as input files. Tools that accept multiple file formats as input determine the format of each file based on the file extension used in the file name. The file extensions recognized are:

- .fru—ASCII FRU file
- .bfru—binary FRU file
- .sdr—ASCII SDR file
- .bsdr—binary SDR file
- .hex—IPMC firmware file
- .cfg—configuration metadata file
- .thr - threshold configuration file

sbcupdate 1.3.3-1 options and arguments are described in Table 87.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Note: All commands and options are case sensitive.

Table 87. Common Command Line Options and Arguments (Sheet 1 of 3)

Short Form Name	Long Form Name	Possible Argument	Description
General options			
-?	--help	*none*	Output a text description of each option.
none	--usage	*none*	A usage message displaying options by their short and long names.
-V	--version	*none*	Output the version number.
-v	--verbose	1 | 2 | 3	Verbose output level.
Communication options			
-I	--interface	kcs | lan | lanplus	Interface type. • *kcs* denotes the local KCS interface on the SBC. Use this interface only if the executable is being run on the SBC and targets the IPMC on the same SBC. • *lan* denotes IPMI over LAN using RMCP. Use this interface only if the executable is being run on a remote node with a LAN connection to a shelf manager that is configured with an RMCP bridge. • *lanplus* denotes IPMI over LAN using RMCP+. Use this interface only if the executable is being run on a remote node with a direct LAN connection. If omitted, kcs is assumed.
-H	--host	<*ip-address*> | <*hostname*>	IP address or name of the host to update over RMCP.
-U	--user	<*string*>	User name. May be up to 16 characters. Valid only with lan interface.
-P	--password	<*string*>	User password. May be up to 20 characters. Valid only with lan interface.
-A	--auth	none | md2 | md5 | password	Authorization algorithm type. Valid only with lan interface.
-L	--privilege	user | operator | admin	Privilege level. Valid only with lan interface.
-t	--target	**KCS interface** 0x20 | rtm | 0x20:rtm **LAN interface** 0xNN[:rtm] | bladeN[:rtm]	**KCS interface** 0x20 denotes the local SBC and targets the local IPMC. rtm or 0x20:rtm denotes the RTM on the local SBC. Omitting the –t option is equivalent to specifying –t 0x20. **LAN interface** The value of NN in 0xNN is the hexadecimal IPMB address of the SBC. The IPMC on that SBC is targeted. The value of N in bladeN can range from 1–14, inclusive determining which SBC to use in the chassis. The IPMB to physical slot mapping used in the Promentum™ MPCHC0001 chassis is assumed. See Table 90 on page 254. The IPMC on the specified SBC is targeted. If :rtm is appended to either target, the RTM on the specified SBC is targeted.
General Update options			

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 87. Common Command Line Options and Arguments (Sheet 2 of 3)

Short Form Name	Long Form Name	Possible Argument	Description
-M	--mode	auto | staged | direct | cancel | rollback | get | info | get | get <file> | threshold	• auto (default) means that staged is attempted first, and direct is used as a fall back. • staged starts a staged update and does not fall back to a direct update. • direct bypasses the initial check for staged capability and starts immediate update. • cancel stops any pending staged firmware update. • rollback forces a rollback on the next reset. • info requests various pieces of information regarding the version of the SDR and FRU packages, and sends the information to the standard output. • get used with no arguments puts the utility into the mode to retrieve the FRU and SDRs from the targeted device. • get used with a <file> argument displays the contents of the file to the standard output. The file extension must be .fru, .bfru, .sdr, or .bsdr and must contain ASCII FRU data, binary FRU data, ASCII SDR data, or binary SDR data, respectively. • get can be used with the –o option to save FRU or SDR data to a file in binary or ASCII format. See the –o option in this table for more information.
none	--reset	*none*	Reset the target after an update. This is the default behavior.
none	--no-reset	*none*	Applies only to staged firmware updates. This option stops a reset of the target IPMC from being performed after performing a staged firmware update. This should not affect payload operation.
none	--force-id	*none*	Forces the firmware update to occur. This is needed to override product ID or manufacturer ID mismatches. (This will happen if the SBC is in failsafe mode.)
Firmware Update options			
none	--capture-rb	*none*	Capture a rollback image during staged update. This is the default behavior.
none	--no-capture-rb	*none*	Applies only to staged firmware updates. This option does not capture a rollback image, thus preserving the contents of the rollback area.
none	--force-fw-update	*none*	This option is needed to downgrade the firmware version or if the target is in firmware transfer state so version information is not available. This forces the firmware update in these cases.
none	--force-fpga-update	*none*	Does not apply.
FRU/SDR Update options			
-b	--byte	*INT*	Number of FRU bytes to get from the target. Only valid in get mode when saving to a binary FRU file (default: unlimited).
none	--force-sdr-update	*none*	This option is needed to downgrade the SDR version, if SDR information is missing either from the system or from the input file, or if the target has a pending staged firmware update. This option forces the SDR update in these cases.
none	--force-fru-update	*none*	This option is needed to downgrade the FRU version, if the FRU version information is missing from the system or from the input file, or also performing a full FRU update. The option forces the FRU update in these cases.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 87. Common Command Line Options and Arguments (Sheet 3 of 3)

Short Form Name	Long Form Name	Possible Argument	Description
-o	--output	<*file*>	Use with –M get to save the contents of the FRU or the SDR to a file. The name of the file is specified as the argument to -o. The file extension given at the end of the file name determines whether FRU or SDR data is saved and whether the data is stored in ASCII or binary form as follows: <*file*>.fru – Save FRU data in ASCII <*file*>.bfru – Save FRU data in binary <*file*>.sdr – Save SDR data in ASCII <*file*>.bsdr – Save SDR data in binary
Threshold Management options			
none	--get-thr	*none*	Allows reading all thresholds settings for sensor.
none	--get-thr-factory	*none*	Allows reading factory default thresholds settings for sensor.
none	--get-thr-active	*none*	Allows reading active thresholds settings for sensor.
none	--get-thr-sdr	*none*	Allows reading sensors thresholds settings from sdr repository.
none	--restore-thr	*none*	Allows restoring factory default settings for sensors all thresholds.
none	--restore-thr-active	*none*	Allows restoring factory default settings for sensors active thresholds.
none	--restore-thr-sdr	*none*	Allows restoring factory default settings for sensors thresholds in SDR repository.
-s	--sensor	INT	Sensor number (0xff for all sensors).

10.6.6 Automatic Firmware Update

While performing a firmware update via the KCS interface or an RMCP bridge, invoking auto mode will automatically negotiate between a direct or staged firmware update. A staged firmware update will be attempted first, while the direct firmware update is used as a fall back. If the target supports staged updates and it is in a state that allows staged updates, a staged update will be performed. If staged updates are not possible, a direct firmware update will be attempted. Note that auto mode is the default mode, by omitting the mode option (-M), auto is assumed.

10.6.6.1 Automatic Firmware Update using KCS Interface

To perform an auto firmware update over the KCS interface, you must be logged into the target SBC as root.

The syntax of the command is:

```
# sbcupdate -I kcs -M auto <path to firmware image/filename>
```

The following is an example of an auto firmware update via the KCS interface:

```
# sbcupdate -I kcs -M auto MPCBL0040_FW_NNNN.hex
```

The above command line can be abbreviated since the KCS interface and the auto mode are both default options. The command can be abbreviated as follows:

```
# sbcupdate MPCBL0040_FW_NNNN.hex
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.6.2 Automatic Firmware Update via RMCP Bridging

In order for RMCP bridging to work correctly, the Shelf Manager must be connected to the network in order to transmit TCP/IP traffic to and from your client. You must also specify the interface option to be lan for RMCP bridging. Auto mode is default so by omitting the -M option, auto is assumed.

When using the sbcupdate utility over RMCP bridge with Promentum MPCMM0001/0002 Chassis Management Module:

- Check that the CMM firmware version is 6.1.1.x or higher.
- Transfer the /usr/share/doc/sbcutils/cmdPrivilege.ini file to both the active and standby CMMs. Place cmdPrivelege.ini in the /etc/ directory on the CMMs. Then, restart the RMCP servers. More details on this can be found in Section 10.5.2, “Configuring the Promentum™ MPCMM0001/0002 CMM” on page 209.

When using the sbcupdate utility over an RMCP bridge with a 3rd party Shelf Manager, it is essential that communication between the target IPMC and a remote network node via a shelf manager can be established. Refer to Table 85, “Required IPMI Command Privileges for RMCP Bridging” on page 208 for more information on the required RMCP commands that must be forwarded to IPMB by the Shelf Manager.

The syntax of the command is:

```
# sbcupdate -I lan -M auto -H <shelf_manager_ip_address>
    -U <RMCP_username> -P <RMCP_password> -t <target>
    <path to firmware image/filename>
```

An example of auto firmware update via RMCP bridging is:

```
# sbcupdate -I lan -M auto -H 10.90.90.91 -U root
    -P cmmrootpass -t 0x8e MPCBL0040_FW_NNNN.hex
```

10.6.7 Direct Firmware Update

Note: The user must not initiate a direct firmware update while a direct firmware update is in progress. Doing so results in the sbcupdate utility exiting because of write/verify failures. If this does happen, exit all invocations of sbcupdate, then the sbcupdate utility can be run again to update the firmware.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.7.1 Direct Firmware Update Using the KCS Interface

To perform a direct firmware update over the KCS interface, you must be logged into the target SBC as root. Note that the KCS is the default interface if the -I option is omitted, so the command line can be abbreviated.

The syntax of the command using the short form for the options is:

```
# sbcupdate -I kcs -M direct <path to firmware image/filename>
```

The syntax of the command using the long form for the options is:

```
# sbcupdate --interface kcs --mode direct
    <path to firmware image/filename>
```

The output from this command should be similar to the following:

```
Entering Direct Firmware Update mode.
Entered Direct Firmware Update mode.
Erasing the current firmware area.
The firmware area has been erased.
Updating firmware.
0% completed
10% completed
20% completed
30% completed
40% completed
50% completed
60% completed
70% completed
80% completed
90% completed
100% completed
Exiting direct firmware update mode.
Firmware successfully updated.
Program exiting!
```

10.6.7.2 Direct Firmware Update to RTM via KCS

To perform a direct firmware update to an RTM, you must specify the target, -t option, to be the RTM. By omitting the -I option, the interface defaults to KCS.

For target information, refer to Table 87, “Common Command Line Options and Arguments” on page 216.

The following is an example of an RTM direct firmware update with the -I option omitted:

```
# sbcupdate -M direct -t rtm MPRTM0040_NNN.hex
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.7.3 Direct Firmware Update via RMCP Bridging

For RMCP bridging to work correctly, the Shelf Manager must be connected to the network so that it can transmit TCP/IP traffic to and from the client. The interface option must also be set to lan for RMCP bridging.

When using the sbcupdate utility over an RMCP bridge with the Promentum™ MPCMM0001/0002 Chassis Management Module:

- Check for a CMM firmware version of 6.1.1.x or higher.
- Transfer the /usr/share/doc/sbcutils/cmdPrivilege.ini file to both the active and standby CMMs. Place cmdPrivelege.ini in the /etc/ directory on the CMMs. Then, restart the RMCP servers. More details on this can be found in Section 10.5.2, “Configuring the Promentum™ MPCMM0001/0002 CMM” on page 209.

When using the sbcupdate utility over an RMCP bridge with a 3rd party Shelf Manager, it is essential that communication between the target IPMC and a remote network node via a shelf manager can be established. Refer to Table 85, “Required IPMI Command Privileges for RMCP Bridging” on page 208 for more information on the required RMCP commands that must be forwarded to IPMB by the Shelf Manager.

The syntax of the command is:

```
# sbcupdate -I lan -M direct -H <shelf_manager_ip_address>
    -U <RMCP_username> -P <RMCP_password> -t <target>
    <path to firmware image/filename>
```

An example command for direct firmware update via RMCP bridging is:

```
# sbcupdate -I lan -M direct -H 10.90.90.91 -U root
    -P cmmrootpass -t 0x8e MPCBL0040_FW_NNNN.hex
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.7.4 Direct Firmware Update to RTM via RMCP Bridging

To perform a direct firmware update to an RTM via RMCP bridging, you must add the RTM to your target along with the target blade.

For RMCP bridging to work correctly, the Shelf Manager must be connected to the network so that it can transmit TCP/IP traffic to and from the client. The interface option must also be set to lan for RMCP bridging.

When using the sbcupdate utility over an RMCP bridge with the Promentum™ MPCMM0001/0002 Chassis Management Module:

- Check for a CMM firmware version of 6.1.1.x or higher.
- Transfer the /usr/share/doc/sbcutils/cmdPrivilege.ini file to both the active and standby CMMs. Place cmdPrivelege.ini in the /etc/ directory on the CMMs. Then, restart the RMCP servers. More details on this can be found in Section 10.5.2, “Configuring the Promentum™ MPCMM0001/0002 CMM” on page 209.

When using the sbcupdate utility over an RMCP bridge with a 3rd party Shelf Manager, it is essential that communication between the target IPMC and a remote network node via a shelf manager can be established. Refer to Table 85, “Required IPMI Command Privileges for RMCP Bridging” on page 208 for more information on the required RMCP commands that must be forwarded to IPMB by the Shelf Manager.

The syntax of the command is:

```
# sbcupdate -I lan -M direct -H <shelf_manager_ip_address>
   -U <RMCP_username> -P <RMCP_password>
   -t <target_blade>:rtm <path to RTM firmware image/filename>
```

An example of a command for direct firmware update to RTM via RMCP bridging is:

```
# sbcupdate -I lan -M direct -H 10.90.90.91 -U root
    -P cmmrootpass -t 0x8e:rtm MPRTM0040_NNN.hex
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.8 Staged Firmware Update

10.6.8.1 Staged Firmware Update Using KCS Interface

The staged firmware update mode allows the option of creating a backup copy of the current operational image into a rollback partition area of flash memory, and then writes the new operational firmware image to a staging area of flash memory. This process happens while the IPMC is running normally. After completion of a staged update, the IPMC resets automatically and the new firmware is loaded to the IPMC (unless the -noreset-mmc option is used).

To perform a staged firmware update over the KCS interface, you must be logged into the target SBC as root.

The syntax of the command is:

```
# sbcupdate -I kcs -M staged <path to firmware image/filename>
```

An example of a staged mode update is:

```
# sbcupdate -I kcs -M staged MPCBL0040_FW_NNNN.hex
```

The output from this command should be similar to the following:

```
Entering Staged Firmware Update mode.
Preparing the staging flash area.
Staging flash area preparation complete.
Capturing the rollback image.
Rollback image captured successfully.
Uploading the new stage firmware image to the staging area.
0% completed
10% completed
20% completed
30% completed
40% completed
50% completed
60% completed
70% completed
80% completed
90% completed
100% completed
New staged image successfully uploaded.
Registering the staged firmware update in flash.
Staged firmware update successfully registered in flash.
The target management controller is being reset.
sbcupdate (W606) Please ignore any select timeout warnings.  They are issued by the
linux diver due to the target reset, and may be ignored.
IPMI message handler: BMC returned incorrect response, expected netfn 7 cmd 2, got
netfn31 cmd a2

The target management controller has been reset.
Staged Firmware Update complete!
Program exiting!
```

Note: The “IPMI message handler: BMC returned incorrect response.” error message is to be expected and may be ignored. This is a timeout error in response to warning (W606) as seen in the output above.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.8.2 Creating a Pending Staged Firmware Update

To create a pending staged firmware update, the update command needs to be invoked with the --no-reset option, otherwise the target resets by default. This allows further operation with the current firmware with an update pending whenever a reset is initiated. The target can be reset with the --reset option.

The following is an example of creating a pending staged firmware update:

```
# sbcupdate -I kcs -M staged --no-reset MPCBL0040_FW_NNNN.hex
```

The following command resets the target initiating the firmware update:

```
# sbcupdate --reset
```

Under no circumstances will the operating system and applications reset as a result of resetting a management controller.

10.6.8.3 Staged Firmware Update via RMCP Bridging

For RMCP bridging to work correctly, the Shelf Manager must be connected to the network in order to transmit TCP/IP traffic to and from the client. The interface option must also be set to lan for RMCP bridging.

When using the sbcupdate utility over an RMCP bridge with the Promentum™ MPCMM0001/0002 Chassis Management Module:

- Check for a CMM firmware version of 6.1.1.x or higher.
- Transfer the /usr/share/doc/sbcutils/cmdPrivilege.ini file to both the active and standby CMMs. Place cmdPrivelege.ini in the /etc/ directory on the CMMs. Then, restart the RMCP servers. More details on this can be found in Section 10.5.2, “Configuring the Promentum™ MPCMM0001/0002 CMM” on page 209.

When using the sbcupdate utility over an RMCP bridge with a 3rd party Shelf Manager, it is essential that communication between the target IPMC and a remote network node via a shelf manager can be established. Refer to Table 85, “Required IPMI Command Privileges for RMCP Bridging” on page 208 for more information on the required RMCP commands that must be forwarded to IPMB by the Shelf Manager.

After completion of a staged update, the IPMC resets automatically and the new firmware is loaded to the IPMC.

The syntax of the command is:

```
# sbcupdate -I lan -M staged -H <shelf_manager_ip_address
    or DNS_host_name> -U <username> -P <password>
    -t <target> <path_to_firmware_image/filename>
```

An example of staged firmware update via RMCP is:

```
# sbcupdate -I lan -M staged -H 10.90.90.91 -U root
    -P cmmrootpass -t 0x8e /tmp/MPCBL0040_FW_NNNN.hex
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.9 Canceling Staged Firmware Update

10.6.9.1 Cancel Staged Firmware Update via KCS Interface

To cancel a staged firmware update, a valid staged firmware update must already be pending.

To check if there is a pending staged firmware update, execute the -M info option.

The following is an example of how to check for pending updates:

```
# sbcupdate -M info

Current firmware version: 1.07.01
Current bootblock version: 1.07
Current staged firmware version: 1.07.01 (pending)
Current rollback firmware version: 1.07.01
```

Note: This example output is only the beginning of the actual output. Notice that the “Current staged firmware version” is pending.

Execute the following command to cancel any pending staged firmware updates:

```
# sbcupdate -M cancel
```

The output of this command is:

```
Canceling any pending staged firmware updates.
All pending staged firmware updates have been canceled.
Program exiting!
```

Execute the -M info option again to see that the staged firmware updated has canceled:

```
# sbcupdate -M info

Current firmware version: 1.07.01
Current bootblock version: 1.07
Current staged firmware version: <None>
Current rollback firmware version: 1.07.01
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.9.2 Cancel Staged Firmware Update via RMCP Bridging

To cancel a staged firmware update, a valid staged firmware update must already be pending.

For RMCP bridging to work correctly, the Shelf Manager must be connected to the network so that it can transmit TCP/IP traffic to and from the client. The interface option must also be set to lan for RMCP bridging.

When using the sbcupdate utility over an RMCP bridge with the Promentum™ MPCMM0001/0002 Chassis Management Module:

- Check for a CMM firmware version of 6.1.1.x or higher.
- Transfer the /usr/share/doc/sbcutils/cmdPrivilege.ini file to both the active and standby CMMs. Place cmdPrivelege.ini in the /etc/ directory on the CMMs. Then, restart the RMCP servers. More details on this can be found in Section 10.5.2, “Configuring the Promentum™ MPCMM0001/0002 CMM” on page 209.

When using the sbcupdate utility over an RMCP bridge with a 3rd party Shelf Manager, it is essential that communication between the target IPMC and a remote network node via a shelf manager can be established. Refer to Table 85, “Required IPMI Command Privileges for RMCP Bridging” on page 208 for more information on the required RMCP commands that must be forwarded to IPMB by the Shelf Manager.

The syntax of the command is:

```
# sbcupdate -I lan -M cancel -H <shelf_manager_ip_address>
    -U <username> -P <password> -t <target>
```

For example:

```
# sbcupdate -I lan -M cancel -H 10.90.90.91 -U root
    -P rootpass -t 0x8e
```

10.6.10 Setting Manual Rollback of the Firmware

10.6.10.1 Manual Rollback via KCS Interface

To force a manual rollback of the firmware, a valid rollback image must already be present on the target management controller. If there is no firmware image in the rollback area, the IPMC will go into direct update mode.

To run the command over the KCS interface, execute the following command:

```
# sbcupdate -I kcs -M rollback
```

Note: If no interface is specified, KCS is assumed.

The output from this command should be similar to the following:

```
Registering a manual rollback of the firmware on the next IPMC reset.
The target management controller is being reset.
sbcupdate (W606) Please ignore any select timeout warnings. They are issued by
the Linux driver due to target reset and may be ignored.
IPMI message handler: BMC returned incorrect response. expected netfn 7 cmd 2.
got netfn 31 cmd a4
The target management controller has been reset.
Manual rollback of the firmware for the next IMPC reset has been registered.
Program exiting!
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Note: The “IPMI message handler: BMC returned incorrect response.” error message is to be expected and may be ignored. This is a timeout error in response to warning (W606) as seen in the output above.

10.6.10.2 Manual Rollback via RMCP Bridging

To force a manual rollback of the firmware, a valid rollback image must already be present on the target management controller. If there is no firmware image in the rollback area, the IPMC will go into direct update mode.

For RMCP bridging to work correctly, the Shelf Manager must be connected to the network so that it can transmit TCP/IP traffic to and from the client. The interface option must also be set to lan for RMCP bridging.

When using the sbcupdate utility over RMCP bridge with Promentum MPCMM0001/0002 Chassis Management Module:

- Check for a CMM firmware version of 6.1.1.x or higher.
- Transfer the /usr/share/doc/sbcutils/cmdPrivilege.ini file to both the active and standby CMMs. Place cmdPrivelege.ini in the /etc/ directory on the CMMs. Then, restart the RMCP servers. More details on this can be found in Section 10.5.2, “Configuring the Promentum™ MPCMM0001/0002 CMM” on page 209.

When using the sbcupdate utility over an RMCP bridge with a 3rd party Shelf Manager, it is essential that communication between the target IPMC and a remote network node via a shelf manager can be established. Refer to Table 85, “Required IPMI Command Privileges for RMCP Bridging” on page 208 for more information on the required RMCP commands that must be forwarded to IPMB by the Shelf Manager.

The syntax of the command is:

```
# sbcupdate -I lan -M rollback
    -H <ip address of shelf manager> -U <RMCP_username>
    -P <RMCP_password> -t <target>
```

For example:

```
# sbcupdate -I lan -M rollback -H 10.90.90.91 -U root
    -P cmmrootpass -t 0x8e
```

10.6.11 Retrieving FRU and SDR Data

Both FRU data and SDR data can be retrieved from a device using the get mode. More details and some examples using this option are provided in the remainder of this section.

10.6.11.1 Retrieving FRU and SDR via KCS Interface

In order to retrieve FRU and SDR data from a device via KCS, specify the get mode (-M get).

To run the command over the KCS interface, execute the following command:

```
# sbcupdate -I kcs -M get
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.11.2 Retrieving FRU and SDR Information Using the -o Option

Both FRU and SDR information can be retrieved separately and stored in either binary or ASCII files. The -o option in conjunction with the -M get option saves FRU and SDR information to a specified file.

The syntax for using the -o option is:

```
# sbcupdate -M get -o <filename.ext>
```

The .ext represents the extension of the filename. The filename can be one of the following:

- Binary FRU: <filename>.bfru
- Binary SDR: <filename>.bsdr
- ASCII FRU: <filename>.fru
- ASCII SDR: <filename>.sdr

An example of the command line for ASCII FRU information retrieval is as follows:

```
# sbcupdate -M get -o getfru.fru
```

The output of this command should be similar to the following:

```
Successful retrieval of data from the target.
Program exiting!
```

The FRU data has been written to the getfru.fru file.

10.6.11.3 Retrieving FRU and SDR via RMCP Bridging

To retrieve the FRU and SDR contents of a management controller via an RMCP bridge, specify the get mode (-M get).

For RMCP bridging to work correctly, the Shelf Manager must be connected to the network so that it can transmit TCP/IP traffic to and from the client. The interface option must also be set to lan for RMCP bridging.

When using the sbcupdate utility over an RMCP bridge with the Promentum™ MPCMM0001/0002 Chassis Management Module:

- Check for a CMM firmware version of 6.1.1.x or higher.
- Transfer the /usr/share/doc/sbcutils/cmdPrivilege.ini file to both the active and standby CMMs. Place cmdPrivelege.ini in the /etc/ directory on the CMMs. Then, restart the RMCP servers. More details on this can be found in Section 10.5.2, “Configuring the Promentum™ MPCMM0001/0002 CMM” on page 209.

When using the sbcupdate utility over an RMCP bridge with a 3rd party Shelf Manager, it is essential that communication between the target IPMC and a remote network node via a shelf manager can be established. Refer to Table 85, “Required IPMI Command Privileges for RMCP Bridging” on page 208 for more information on the required RMCP commands that must be forwarded to IPMB by the Shelf Manager.

The syntax of the command is:

```
# sbcupdate -I lan -M get -H <shelf_manager_ip_address>
    -U <RMCP_username> -P <RMCP_password>  -t <target>
```

For example, you might execute the following command:

```
# sbcupdate -I lan -M get -H 10.90.90.91 -U root
    -P cmmrootpass -t 0x8e
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.12 Updating FRU Data

To update FRU data on either the IPMC or the RTM, sbcupdate needs to know about the fields that exist in the FRU as well as the actual data to be written to the FRU.

Information about the fields in the FRU is contained in the /usr/share/doc/sbcutils/master.cfg file. This file applies to FRU information on both IPMCs and RTMs.

Information about the actual data to be written to the FRU is contained in a .fru file that is specific both to the SBC and to the FRU (either IPMC or RTM).

There are two possible FRU updates, full and incremental FRU updates. It is recommended to use the incremental FRU update method only.

- **Full FRU update** - All system FRU information is removed from the system and replaced with FRU data from a file. Any modifications or additions performed by users, such as product number/name change, asset tag change or customer MRA record additions, are overwritten (lost).
- **Incremental FRU update** - The sbcutils package comes with a configuration file called /usr/share/doc/sbcutils/master.cfg that controls what system data to preserve. The supplied configuration file also directs sbcupdate to replace all PICMG and RadiSys records on the system with the input file PICMG and RadiSys records. Any other MRA record (i.e. customer created records) will not be altered during incremental FRU updates.

To perform FRU updates in certain circumstances, the --force-fru-update option may be necessary in the syntax. The following are examples of when to invoke this option:

- Downgrading an FRU version.
- The FRU version information is missing either from the system or from the input file.
- Performing a full FRU update.

Note: Using the --force-fru-update option will all FRU data and will not maintain any variable data in the FRU

The --force-id option may also be a necessary option in the following circumstances:

- The Product ID in the input file does not match the product ID of the system.
- The FRU version information is missing either from the system or from the input file.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.13 Writing Data to the FRU on the SBC or RTM

10.6.13.1 Incremental FRU Update via KCS

To perform an incremental FRU update, use the supplied FRU file from the release package for your target IPMC along with the supplied /usr/share/doc/sbcutils/master.cfg file provided with the SBC utilities package. Staged FRU updates are not supported, therefore it is not necessary to specify direct mode (-M direct).

10.6.13.2 Incremental FRU Update via RMCP Bridging

To perform an incremental FRU update, use the supplied FRU file from the release package for your target IPMC along with the supplied /usr/share/doc/sbcutils/master.cfg file provided with the sbc utilities package. Staged FRU updates are not supported, therefore it is not necessary to specify direct mode (-M direct).

For RMCP bridging to work correctly, the Shelf Manager must be connected to the network so that it can transmit TCP/IP traffic to and from the client. The interface option must also be set to lan for RMCP bridging.

When using the sbcupdate utility over an RMCP bridge with the Promentum™ MPCMM0001/0002 Chassis Management Module:

- Check for a CMM firmware version of 6.1.1.x or higher.
- Transfer the /usr/share/doc/sbcutils/cmdPrivilege.ini file to both the active and standby CMMs. Place cmdPrivelege.ini in the /etc/ directory on the CMMs. Then, restart the RMCP servers. More details on this can be found in Section 10.5.2, “Configuring the Promentum™ MPCMM0001/0002 CMM” on page 209.

When using the sbcupdate utility over an RMCP bridge with a 3rd party Shelf Manager, it is essential that communication between the target IPMC and a remote network node via a shelf manager can be established. Refer to Table 85, “Required IPMI Command Privileges for RMCP Bridging” on page 208 for more information on the required RMCP commands that must be forwarded to IPMB by the Shelf Manager.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.14 Full FRU Update via KCS

To perform a full FRU update, use the supplied FRU file for your target IPMC. Staged FRU updates are not supported, therefore it is not necessary to specify direct mode (-M direct). To invoke full FRU update requires the --force-fru-update command.

Caution: Full FRU updates remove all system FRU information and replaces it with FRU data from a file. All variable data and modifications/additions performed by users, such as product number or name change, asset tag change or customer MRA record additions are overwritten.

Here is an example of a full FRU update:

```
# sbcupdate -I kcs --force-fru-update MPCBL0040_NNN.fru
```

The output from this command should be similar to the following:

```
Beginning update of the FRU.
Writing FRU - Addr(0x20) ID(0) Bus(255)
Writing FRU Board Info Area
Writing FRU Product Info Area
Writing FRU Multi Record Area
Verifying contents of FRU
The FRU has been successfully updated.
Program exiting!
```

The following is an example of when the FRU version information is missing from the system; the --force-id option must now be invoked:

```
# sbcupdate -I kcs --force-fru-update --force-id
    MPCBL0040_NNN.fru
```

To update the RTM FRU over the KCS interface on the MPCBL0040 SBC, execute the following command:

```
# sbcupdate -I kcs -t rtm --force-fru-update MPRTM0040_NNN.fru
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.15 Full FRU Update via RMCP Bridging

To perform a full FRU update, use the supplied FRU file for your target IPMC. Staged FRU updates are not supported, therefore it is not necessary to specify direct mode (-M direct). To invoke full FRU update requires the --force-fru-update command.

Caution: Full FRU updates remove all system FRU information and replace it with FRU data from a file. All variable data and modifications/additions performed by users, such as product number or name change, asset tag change or customer MRA record additions are overwritten.

For RMCP bridging to work correctly, the Shelf Manager must be connected to the network so that it can transmit TCP/IP traffic to and from the client. The interface option must also be set to lan for RMCP bridging.

When using the sbcupdate utility over an RMCP bridge with the Promentum™ MPCMM0001/0002 Chassis Management Module:

- Check for a CMM firmware version of 6.1.1.x or higher.
- Transfer the /usr/share/doc/sbcutils/cmdPrivilege.ini file to both the active and standby CMMs. Place cmdPrivelege.ini in the /etc/ directory on the CMMs. Then, restart the RMCP servers. More details on this can be found in Section 10.5.2, “Configuring the Promentum™ MPCMM0001/0002 CMM” on page 209.

When using the sbcupdate utility over an RMCP bridge with a 3rd party Shelf Manager, it is essential that communication between the target IPMC and a remote network node via a shelf manager can be established. Refer to Table 85, “Required IPMI Command Privileges for RMCP Bridging” on page 208 for more information on the required RMCP commands that must be forwarded to IPMB by the Shelf Manager.

The command to update the IPMC FRU on the MPCBL0040 has the following syntax:

```
# sbcupdate -I lan -H <shelf_manager_ip_address>
    -U <RMCP_username> -P <RMCP_password> -t <target>
    --force-fru-update MPCBL0040_NNN.fru
```

The command to update the RTM FRU on the MPCBL0040 has the following syntax:

```
# sbcupdate -I lan -H <shelf_manager_ip_address>
    -U <RMCP_username> -P <RMCP_password>
    -t <target>:rtm --force-fru-update MPRTM0040_NNN.fru
```

An example of updating the IPMC FRU:

```
# sbcupdate -I lan -H 10.90.90.91 -U root -P cmmrootpass
    -t 0x8e --force-fru-update MPCBL0040_NNN.fru
```

The following is an example of updating the RTM FRU:

```
# sbcupdate -I lan -H 10.90.90.91 -U root -P cmmrootpass
    -t 0x8e:rtm --force-fru-update MPRTM0040_NNN.fru
```

The output from this command should be similar to the following:

```
Beginning update of the FRU.
Writing FRU - Addr(0x20) ID(0) Bus(255)
Writing FRU Internal Use Area
Writing FRU Board Info Area
Writing FRU Product Info Area
Writing FRU Multi Record Area
Verifying contents of FRU
The FRU has been successfully updated.
Program exiting!
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.16 Writing SDR Data

10.6.16.1 SDR Update via KCS

To perform an SDR update via KCS, use the supplied SDR file from the release package for your target IPMC. Staged SDR updates are not supported, therefore it is not necessary to specify direct mode (-M direct).

Note: If no interface is specified, KCS is assumed.

The output of this command should be similar to the following:

```
Beginning update of the SDRs.
Upgrading the SDR from version unkown to version 0.1.
The SDRs have been successfully updated.
The proxied target management controller is being reset.
The porxied target management controller has been reset.
The target management controller is being reset.
sbcupdate (W606) Please ignore any select timeout warnings. They are issued by
the Linux driver due to target reset and may be ignored.
IPMI message handler: BMC returned incorrect response. Expected netfn 7 cmd 2.
got netfn 7 cmd 33
The target  management controller has been reset.
Program exiting.
```

Note: The “IPMI message handler: BMC returned incorrect response.” error message is to be expected and may be ignored. This is a timeout error in response to warning (W606) as seen in the output above. This exact error message may not appear and it may not always be the same error message.

When performing an SDR update, in certain circumstances it may be necessary to invoke the --force-sdr-update option. The following are instances of when to invoke this option:

- Downgrading an SDR version.
- The SDR version information is missing either from the system or from the input file.
- The target has a pending staged firmware update or with RTM/AMC targets, the carrier board has a pending update.

An example of the use of the --force-sdr-update option is:

```
# sbcupdate -I kcs --force-sdr-update MPCBL0040_NNN.sdr
```

10.6.16.2 RTM SDR Update via KCS

To perform an RTM SDR update, you must specify the target (-t option) to be the RTM. You will use the supplied SDR file from the release package for your target RTM.

The following is an example of updating an RTM SDR:

```
# sbcupdate -I kcs -t rtm MPRTM0040_NNN.sdr
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.16.3 SDR Update via RMCP Bridge

To perform an SDR update via an RMCP bridge, use the supplied SDR file from the release package for your target ICMP. To run the command over an RMCP bridge, you must have a shelf manager (an Promentum™ MPCMM0001/0002 Chassis Management Module) that bridges IPMB traffic. The shelf manager must be connected to the network so that it can transmit TCP/IP traffic to and from the client. The interface selected must be lan, since the KCS interface is assumed otherwise.

The syntax of the command used to execute an MPCBL0040 SDR update is as follows:

```
# sbcupdate -I lan -H <shelf_manager_ip_address>
    -U <RMCP_username> -P <RMCP_password> -t <target>
    MPCBL0040_NNN.sdr
```

For example:

```
# sbcupdate -I lan -H 10.90.90.91 -U root -P cmmrootpass
    -t 0x8e MPCBL0040_NNN.sdr
```

10.6.17 RTM SDR Update via RMCP Bridge

To perform an RTM SDR update via RMCP bridge, you must specify the target blade as well as the RTM.

The syntax of RTM SDR update via RMCP bridge command is as follows:

```
# sbcupdate -I lan -H <shelf_manager_IP_address>
    -U <RMCP_username> -P <RMCP_password>
    -t <target blade>:rtm MPRTM0040_NNN.sdr
```

For example:

```
# sbcupdate -I lan -H 10.90.90.91 -U root -P cmmrootpass
    -t 0x8e:rtm MPRTM0040_NNN.sdr
```

10.6.18 Writing Asset Tag Information

To write asset tag information, execute the following command:

```
sbcupdate [-i <interface>] [-t <target>]
    /usr/share/doc/sbcutils/asset.cfg
```

You are prompted for an asset number, which consists of one to 20 alphanumeric characters. This string is written to the device targeted in the command (IPMC or RTM) over the specified interface (or over KCS if no interface is specified).

The following is an example of writing asset tag information:

```
# sbcupdate -I kcs /usr/share/doc/sbcutils/asset.cfg
```

The output from the command should be similar to the following:

```
Enter value for PRODUCT Asset Tag (Maximum length allowed is 20 characters):
-Your data entered-
Writing FRU - ADDR(0x20) ID(0) Bus(0)
Writing FRU Product Info Area
Verifying contents of FRU
Program exiting!
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.6.19 Output from the –M info Option

The following is example output from the -M info option. See Table 87, “Common Command Line Options and Arguments” on page 216 for more information about using the -M info option. The version in the staged area and the version in the rollback area are both included the output.

For example:

```
# sbcupdate -I kcs -M info
```

The output from this command should be similar to the following:

```
root@demo:~/utils# sbcupdate -M info
sbcupdate - RadiSys SBC Utilities 1.3.2.2
Running with the invocation: -M info
Current firmware version: 1.11.12
Current bootblock version: 1.05
Current staged firmware version: <None>
Current rollback firmware version: <None>

Manufacturer ID: 343 (0x00000157)
Product ID: 2060 (0x080c)
Device type: IPMC
FPGA revision: 1.0A
Board revision: 0xA0

FRU device ID: 0
FRU version: 0.16
FRU Asset Tag: 00000000000000000000
BIOS Primary Version: DC752HRA.86E.0027.P09.0703091351

SDR version: SDR File 1.07
SDR Package version: SDR Package E

Successful retrieval of data from the target.
Program exiting!
```

An example of the -M info option for the RTM is as follows:

```
# sbcupdate -M info -t rtm
```

The output from this command should be similar to the following:

```
Current firmware version: 1.05.01
Current bootblock version: 1.07

Manufacturer ID: 343 (0x00000157)
Product ID: 2224 (0x08b0)
Device type: RTM
FPGA revision: <Not Available>
Board revision: <Not Available>

FRU device ID: 1
FRU version: 0.06
FRU Asset Tag: <Blank>

SDR version: SDR File 0.1
SDR Package version: SDR Package 0.0.1

Successful retrieval of data from the target.
Program exiting!
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.7 Sensor Device Record (SDR) Threshold Management

The SBC update tool can be use to manage the SDR thresholds setting of all sensors. The SDR threshold change feature is for customers that want to change the default values of RadiSys defined SDR thresholds. The primary use of this is to change upper non-critical temperature thresholds so that the blade temperature thresholds can be set for different temperature environments. The types of thresholds that can be managed are follows:

- The ACTIVE thresholds, which are the current thresholds value of the operational FRU
- The SDR thresholds, which store sensor threshold values that are used to set the active sensor thresholds when the FRU transitions from the M0 state to the M1 state
- The factory default thresholds. The ACTIVE and SDR thresholds can be restored to these values without an external configuration file. The ACTIVE and SDR thresholds values are not allowed to be set outside of the range defined by non-recoverable thresholds in the factory default setting.

The following subsections describe step-by-step procedure to read, change and restore the SDR thresholds setting.

Caution: Changes to voltage and current thresholds can lead to device corruption or failure.

Note: RadiSys is not responsible for customer changes of thresholds that fall outside the RadiSys- defined factory default settings.

10.7.1 Reading Thresholds Using KCS Interface

To read the threshold from a device via KCS, specify the threshold mode using `-M threshold` and add options to specify types of threshold to be read.

The syntax of the command is:

```
# sbcupdate -I kcs -M threshold [--get-thr-factory]
      [--get-thr-active] [--get-thr-sdr] [--get-thr] -s 0xYZ
```

where:

- `--get-thr-factory` reads FACTORY settings of thresholds
- `--get-thr-active` reads ACTIVE settings of thresholds
- `--get-thr-sdr` reads thresholds settings from SDR repository
- `--get-thr` reads all of the above
- `0xYZ` specifies the sensor number and accepts the following value:
  - `0x00` to `0xFE` to read thresholds settings of single sensor
  - `0xFF` to read threshold settings of all sensors

The following is an example to read the threshold of a sensor threshold:

```
# sbcupdate -I kcs -M threshold --get-thr-factory --get-thr-active
--get-thr-sdr --get-thr -s 0x93
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

The output from this command should be similar to the following:

```
Reading thresholds settings.
SENSOR_NUMBER                              : 93
_ACTIVE_LOWER_NON_CRITICAL_THRESHOLD       : B0
_ACTIVE_LOWER_CRITICAL_THRESHOLD           : AB
_ACTIVE_LOWER_NON_RECOVERABLE_THRESHOLD    : A1
_ACTIVE_UPPER_NON_CRITICAL_THRESHOLD       : EC
_ACTIVE_UPPER_CRITICAL_THRESHOLD           : F9
_ACTIVE_UPPER_NON_RECOVERABLE_THRESHOLD    : FE
_ACTIVE_POSITIVE_GOING_HYSTERESIS          :  2
_ACTIVE_NEGATIVE_GOING_HYSTERESIS          :  2
_SDR_LOWER_NON_CRITICAL_THRESHOLD          : B0
_SDR_LOWER_CRITICAL_THRESHOLD              : AB
_SDR_LOWER_NON_RECOVERABLE_THRESHOLD       : A1
_SDR_UPPER_NON_CRITICAL_THRESHOLD          : EC
_SDR_UPPER_CRITICAL_THRESHOLD              : F9
_SDR_UPPER_NON_RECOVERABLE_THRESHOLD       : FE
_SDR_POSITIVE_GOING_HYSTERESIS             :  2
_SDR_NEGATIVE_GOING_HYSTERESIS             :  2
_FACTORY_LOWER_NON_CRITICAL_THRESHOLD      : B0
_FACTORY_LOWER_CRITICAL_THRESHOLD          : AB
_FACTORY_LOWER_NON_RECOVERABLE_THRESHOLD   : A1
_FACTORY_UPPER_NON_CRITICAL_THRESHOLD      : EC
_FACTORY_UPPER_CRITICAL_THRESHOLD          : F9
_FACTORY_UPPER_NON_RECOVERABLE_THRESHOLD   : FE
_FACTORY_POSITIVE_GOING_HYSTERESIS         :  2
_FACTORY_NEGATIVE_GOING_HYSTERESIS         :  2
Program exiting!
```

Note: Only specified sensor threshold values will appear in the output. The output will be displayed on the console or redirected to the output file specified by <-o `filename.thr`> in the command line.

The syntax of the command to redirect output to a .thr file:

```
# sbcupdate [-I kcs] -M threshold [--get-thr-factory]
      [--get-thr-active] [--get-thr-sdr] [--get-thr]
      -s 0xYZ [-o filename.thr]
```

Below is the example of the content of the filename.thr:

```
SENSOR_NUMBER                              : 93
_ACTIVE_LOWER_NON_CRITICAL_THRESHOLD       : B0
_ACTIVE_LOWER_CRITICAL_THRESHOLD           : AB
_ACTIVE_LOWER_NON_RECOVERABLE_THRESHOLD    : A1
_ACTIVE_UPPER_NON_CRITICAL_THRESHOLD       : EC
_ACTIVE_UPPER_CRITICAL_THRESHOLD           : F9
_ACTIVE_UPPER_NON_RECOVERABLE_THRESHOLD    : FE
_ACTIVE_POSITIVE_GOING_HYSTERESIS          :  2
_ACTIVE_NEGATIVE_GOING_HYSTERESIS          :  2
_SDR_LOWER_NON_CRITICAL_THRESHOLD          : B0
_SDR_LOWER_CRITICAL_THRESHOLD              : AB
_SDR_LOWER_NON_RECOVERABLE_THRESHOLD       : A1
_SDR_UPPER_NON_CRITICAL_THRESHOLD          : EC
_SDR_UPPER_CRITICAL_THRESHOLD              : F9
_SDR_UPPER_NON_RECOVERABLE_THRESHOLD       : FE
_SDR_POSITIVE_GOING_HYSTERESIS             :  2
_SDR_NEGATIVE_GOING_HYSTERESIS             :  2
_FACTORY_LOWER_NON_CRITICAL_THRESHOLD      : B0
_FACTORY_LOWER_CRITICAL_THRESHOLD          : AB
_FACTORY_LOWER_NON_RECOVERABLE_THRESHOLD   : A1
_FACTORY_UPPER_NON_CRITICAL_THRESHOLD      : EC
_FACTORY_UPPER_CRITICAL_THRESHOLD          : F9
_FACTORY_UPPER_NON_RECOVERABLE_THRESHOLD   : FE
_FACTORY_POSITIVE_GOING_HYSTERESIS         :  2
_FACTORY_NEGATIVE_GOING_HYSTERESIS         :  2
```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.7.2 Reading Thresholds via RMCP Bridging

In order for RMCP bridging to work correctly, the shelf manager must be connected to the network in order to transmit TCP/IP traffic to and from the client. The user must also specify the `-I lan` interface option for RMCP bridging.

To read the threshold from a device via RMCP bridge, specify the threshold mode (`-M threshold`) and add options to specify types of threshold to be read.

The syntax of the command is:

```
# sbcupdate -I lan -H <ip address of shelf manager> -U <username>
      -P <password> -t <IPMB address> -M threshold
      [--get-thr-factory] [--get-thr-active] [--get-thr-sdr]
      [--get-thr] -s 0xYZ
```

For example, users would execute the following command:

```
# sbcupdate -I lan -H 10.90.90.91 -U root -P cmmrootpass -t 0x8e
      -M threshold --get-thr-factory --get-thr-active
      --get-thr-sdr --get-thr -s 0x93
```

10.7.3 Changing Thresholds Values Using KCS Interface

To change the threshold values using the KCS interface, regular ".thr" file needs to be specified in the command line.

The syntax of the command is:

```
# sbcupdate -I kcs <path to change threshold file/filename>
```

The following is the example to change only selected thresholds using the change.thr file:

```
# sbcupdate -I kcs change.thr
```

The output from this command should be similar to the following:

```
Changing thresholds settings.
Program exiting!
```

Note: The change.thr file is a file of the same format as the regular .thr file created by the sbcupdate tool when reading thresholds to a file. Each record in the .thr file should begin with _SENSOR_NUMBER line followed by predefined THRESHOLDS lines. Only thresholds listed in records are affected in SBC.

An example to change SBC Temp 1 Upper Non-critical thresholds is as follow:

1. Create a change.thr file with content as below:
   ```
   _SENSOR_NUMBER                          : 30
   _ACTIVE_UPPER_NON_CRITICAL_THRESHOLD    : 45
   ```
2. Run the change threshold command.
   ```
   # sbcupdate -I kcs change.thr
   ```
3. Read the sensor threshold using a command as in Section 10.7.1, "Reading Thresholds Using KCS Interface" or the cmmget command to make sure the SBC Temp 1 Upper Non-critical thresholds is changed to the value stated in the change.thr file.
   ```
   # sbcupdate -I kcs -M threshold --get-thr-factory
   --get-thr-active --get-thr-sdr --get-thr -s 0x30
      or
   # cmmget -l blade12 -t "SBC Temp 1" -d thresholdsall
   ```


Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.7.4 Changing Thresholds Values via RMCP Bridging

For RMCP bridging to work correctly, the shelf manager must be connected to the network in order to transmit TCP/IP traffic to and from the client. The user must also specify the interface option to be “lan” for RMCP bridging.

To change the threshold values, the regular .thr file needs to be specified in the command line.

The syntax of the command is:

```
# sbcupdate -I lan -H <ip address of shelf manager>
      -U <username> -P <password> -t <IPMB address>
      <path to restore threshold file/filename>
```

For example, user would execute the following command:

```
# sbcupdate -I lan -H 10.90.90.91 -U root -P cmmrootpass
      -t 0x8e change.thr
```

10.7.5 Restoring Factory Default Thresholds Values Using KCS Interface

To restore the factory default values of ACTIVE and SDR threshold types using the KCS interface, specify the threshold type to be restored.

The syntax of the command is:

```
# sbcupdate -I kcs [--restore-thr-active] [--restore-thr-sdr]
      [--restore-thr] -s 0xYZ
```

where:

- `--restore-thr-active` restores ACTIVE settings of thresholds
- `--restore-thr-sdr` restores thresholds settings from SDR repository
- `--restore-thr` restores all of the above
- `0xYZ` specifies the sensor number and accepts the following value:
  - 0x00 to 0xFE to read thresholds settings of single sensor
  - 0xFF to read threshold settings of all sensors

The sbcudate utility also supports restoring only selected thresholds values using the KCS interface by providing a special restore.thr file in command line.

The syntax of the command is:

```
# sbcupdate -I kcs <path to restore threshold file/filename>
```

The following example shows how to restore only selected thresholds using the restore.thr file:

```
# sbcupdate -I kcs restore.thr
```

The output from this command should be similar to the following:

```
Restoring factory default thresholds settings.
Program exiting!
```

Note: The restore.thr file is a file of the same format as the regular .thr file created by the sbcupdate tool when reading thresholds to a file. Because factory default settings can not be restored, any _FACTORY_ lines that appear in restore.thr will be ignored and a warning will be displayed on console.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

10.7.6 Restoring Factory Default Thresholds Values via RMCP Bridging

For RMCP bridging to work correctly, the shelf manager must be connected to the network in order to transmit TCP/IP traffic to and from the client. The user must also specify the interface option to be lan for RMCP bridging.

To restore the factory default values of ACTIVE and SDR threshold types via RMCP bridge, specify the threshold type to be restored.

The syntax of the command is:

```
# sbcupdate -I lan -H <ip address of shelf manager>
      -U <username> -P <password> -t <IPMB address>
      [--restore-thr-active] [--restore-thr-sdr]
      [--restore-thr] -s 0xYZ
```

The sbcudate utility also supports restoring only selected thresholds values using RMCP bridge by providing a special restore.thr file in command line.

The syntax of the command is:

```
# sbcupdate -I lan -H <ip address of shelf manager>
      -U <username> -P <password> -t <IPMB address>
      <path to restore threshold file/filename>
```

For example, user would execute the following command:

```
# sbcupdate -I lan -H 10.90.90.91 -U root -P cmmrootpass -t
      0x8e restore.thr
```

10.8 Displayed Messages

Warning and error messages are formatted with the name of the utility generating the message, the message number and the message text. For example, if sbcupdate is given a firmware file intended for a product that is not the same as the target MMC, the following message is displayed:

```
sbcupdate (E525) Product ID mismatch!  The supplied input file is not intended for
this target.
```

Table 88, “Informational Messages” on page 240 lists possible informational messages and Table 89, “Warning and Error Messages” on page 243 lists the possible warnings and errors.

Table 88. Informational Messages

Message	Description
%1 - RadiSys SBC Utilities %2	Version information displayed with the ¬¬ version option. %1 is the name of the utility and %2 is the version of the SBC Utilities package.
Entering Staged Firmware Update mode.	This informational message is displayed when the utility begins a Staged Firmware Update.
Preparing the staging flash area.	This informational message is displayed when the staging area in flash memory is being erased, making room for the new image to be uploaded. This operation can take a number of seconds to complete, depending on system activity.
Staging flash area preparation complete.	This informational message is displayed once the staging area has been erased.
Capturing the rollback image.	This informational message is displayed when the rollback image is being copied. This operation includes erasing the rollback area prior to capturing a new rollback image. This operation can take a number of seconds to complete, depending on system activity.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 88. Informational Messages (Continued)

Message	Description
Rollback image captured successfully.	This informational message is displayed when the rollback image has been successfully captured.
No rollback is being captured.	This informational message is only displayed when the no capture rb command-line option is included with the update. Messages I503 and I504 are not displayed if this message is displayed.
Uploading the new staged firmware image to the staging area.	This informational message is displayed once the new staging image supplied in the RadiSys HEX file is being written to flash memory.
New staged firmware image successfully uploaded.	This informational message is displayed once the image has finished being written to flash memory. This does not imply the update is complete.
Forced firmware update in progress, ignoring product and manufacturer IDs.	This informational message is displayed when the force id command-line option is included in the update. This overrides comparisons between product and manufacturer IDs between the supplied HEX file from RadiSys and what is on the SBC. This would be used in the event the firmware is corrupt and is reporting false information about the SBC; use this only when directed.
Registering the staged firmware update in flash.	This informational message is displayed at the conclusion of the staged update. It indicates that the staged image was successfully written and verified. A bit is set in flash memory telling the IPMC to write the new staged image to the operational area on the next IPMC reset. This operation may take a few seconds, depending on system activity.
Staged firmware update successfully registered in flash.	This informational message is displayed when the registration of the valid staging image has been completed.
Staged Firmware Update complete!	This informational message is displayed when all staged update operations have completed successfully. This indicates the update has been completed.
Entering Direct Firmware Update mode.	This informational message is displayed when a direct firmware update is being initiated. This indicates the operational code in the IPMC is being halted, and all commands will be serviced by the boot block. This operation may take a few seconds, depending on the number of outstanding transactions being processed by the IPMC.
Entered Direct Firmware Update mode.	This informational message is displayed after the transition from operational firmware to boot block has been completed. This is only displayed once a GetDeviceID shows the lowest bit of byte 4 on, per the IPMI spec (Is Device Busy).
Updating firmware.	This informational message is displayed before the writing of the firmware is initiated.
Firmware successfully updated.	This informational message is displayed after the new firmware has been written and verified.
Exiting direct firmware update mode.	This informational message is displayed when the transition from the boot block back to the new operational code is initiated. This message implies that the IPMC is being reset.
Program exiting!	This informational message is displayed when the utility has completed all operations and is completing execution.
Mismatch at offset %1 (length %2 bytes).	This informational message is displayed if the write verification during a direct firmware update finds a mismatch. %1 is replaced with the byte offset that the difference was located at and %2 is replaced with the number of bytes found to be different.
Got: %1 Expected: %2	This informational message is displayed if the write verification during a direct firmware update finds a mismatch. %1 is replaced with the data byte read from flash memory, and %2 is replaced with the data byte that should have been in flash memory.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 88. Informational Messages (Continued)

Message	Description
%1%% completed	This informational message is displayed during a direct firmware update for every 10% of the firmware image written. %1 is replaced with the percentage completed. It ranges from 0% to 100%.
The %1 target management controller is being reset.	This informational message is displayed after the utility is about to sent a cold reset command to the target MMC.
The target management controller has been reset	This informational message is displayed after the utility has sent a cold reset command to the target MMC and no error completion codes have been received.
Running with the invocation: %1	Displays a copy of all arguments, given exactly as they were supplied on the command line.
%1 in progress.	This verbose message is a level 1 verbose message, and is displayed during CaptureRollback or EraseStagingArea operations. It can be viewed by passing -v 1 or --verbose 1 on the command-line. Note that higher levels of verbosity still activate this message. %1 is replaced with the current function being executed. This message is only available in staged updates.
Canceling any pending staged firmware updates.	This informational message is displayed when the 'cancel' mode is invoked. It indicates the start of the process to cancel a pending staged firmware update.
All pending staged firmware updates have been canceled.	This informational message is displayed when the cancel mode has been completed successfully.
Registering a manual rollback of the firmware on the next IPMC reset.	This informational message is displayed when the 'rollback' mode is invoked. It indicates the start of the process to force a rollback to happen on the next IPMC reset.
Manual rollback of the firmware for the next IPMC reset has been registered.	This informational message is displayed when the manual rollback registration has been completed.
Successful retrieval of the FRU.	This informational message is displayed when the FRU get operation has completed successfully.
The FRU has been successfully updated.	This informational message is displayed when the FRU has been successfully written to the target FRU device.
Successful retrieval of data from the target.	A read operation from the system has completed with no errors.
The SDRs have been successfully updated.	This informational message is displayed when the SDR has been successfully written to the target device.
Beginning update of the FRU.	This information message is displayed to indicate the start of the FRU update.
Beginning update of the SDRs.	This information message is displayed to indicate the start of the SDR update.
No firmware version to report.	This message is displayed when using the info mode to obtain version information of a board that is not provided by RadiSys in firmware transfer mode. Once the board (not provided by RadiSys) exits firmware transfer mode, the firmware version can be read.
Upgrading the FRU from version %1 to version %2.	This information message is displayed to indicate the direction of FRU update, as an upgrade from one version to another. %1 is replaced with the existing system FRU version. %2 is replaced with the newer version that is being used for the update.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 88. Informational Messages (Continued)

Message	Description
Upgrading the SDR from version %1 to version %2.	This information message is displayed to indicate the direction of SDR update, as an upgrade from one version to another. %1 is replaced with the existing system SDR version. %2 is replaced with the newer version that is being used for the update.
Erasing the current firmware area.	In versions of the boot block that support one shot full-firmware erasures, this message is displayed to signal the start of erasure.
The firmware area has been erased.	This message is displayed to signal the end of firmware erasure. It is only displayed if the target boot block supports one shot full-firmware erasure.

Table 89. Warning and Error Messages

Number	Message	Description
E102	Unsupported interface “%1”. Must be one of {kcs | lan}.	The user has supplied the interface option with an argument other than “kcs” or “lan”. %1 is replaced with the offending interface name.
E103	Unsupported authorization type “%1”. Must be one of {none | md2 | md5 | password}.	The user has supplied the authtype option with an argument other than “none”, “md2”, “md5”, or “password”. %1 is replaced with the offending authorization type.
E104	Unsupported privilege level “%1”. Must be one of {callback | user | operator | admin}.	The user has supplied the privilege option with an argument other than “callback”, “user”, “operator” or “admin”. %1 is replaced with the offending privilege level.
E105	Illegal IPMB address: 0x%1.	The user has supplied an out-of-range IPMB address. The range enforced by sbcupdate is [0x02, 0xFE], but the chassis in use is likely to require a subset of this range.
E106	Parse error: %1.	This message is displayed as a result of a number of different errors in invocation syntax such as, unknown option, missing option argument, string supplied for a numerical option argument, etc. %1 is replaced with further detail on the parse problem.
E107	AMC site number %1 is out-of-range (must be between %2 and %3).	From the AMC specification, the AMC site numbers must be between 1 and 8, inclusive.
E108	IPMC site number %1 is out-of-range (must be between %2 and %3).	The user has supplied an out-of-range IPMC site number. The range enforced by sbcupdate is [0x01, 0xFF], but the chassis in use is likely to require a subset of this range.
E109	Syntax error in target argument: “%1”	The argument to the target option is malformed.
E110	When communicating locally, it is not possible to specify a target blade other than 0x20.	For “direct to the blade” operation (that is, KCS or RMCP+ direct), if the target argument includes an IPMB address, it must be 0x20 (for example: --target 0x20:rtm or --target rtm). SBCs and CMMs from RadiSys do not support bridging from one SBC to another to from the SBC to the ShMC.
E150	IPMI communication problem while reading FRU address info.	During a FRU operation, this message is displayed if there is a problem sending messages to the carrier SBC, for example, a timeout or error completion code. The three commands send to the carrier are Get Device ID, Get PICMG Properties and Get Address Info.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 89. Warning and Error Messages (Continued)

Number	Message	Description
E151	The specified system does not support FRUs of type "%1".	The user specified an FRU operation to a target that is not supported by the SBC. For example, this message is displayed if the target argument is “amc” and the SBC in use does not have an AdvancedMC* module.
E152	The specified target is ambiguous. There is more than one possible FRU of type "%1".	If the target’s carrier board supports more than one sub-FRU of the given type, then the sub-FRU’s site number must be supplied on the command line. For example, on an MPCBL0040 SBC, it is fine to use “--target amc” because only a single amc is supported. Using the same target argument for a multi-AMC SBC is ambiguous. In that case, it is required to use something like “--target amc6”.
E153	There is no response from any %1 at the specified location.	A sub-FRU was specified but is not currently present in the system.
E154	IPMI communication error while checking for the target presence.	While attempting to check for the presence of a sub-FRU, there was an IPMI communication error, such as a timeout. No completion code was returned, successful or otherwise, in response to the query.
E155	IPMI communication problem while determining the IPMB-0 address of IPMC site %1.	While attempting to find the IPMB address of the target (such as the Get Address Info command) there was an IPMI communication error, such as a timeout. No completion code was returned, successful or otherwise, in response to the query.
E156	The specified system does not support IPMCs at site %1.	The target site specified is supported by the chassis, but not for an AdvancedTCA board. For example, slots 15 and 16 of an MPCHC0001 contain PEM and fan trays, but not SBCs.
E157	Cannot bridge to the target from a %1. Did you mean to use the --target/-t option?	Cannot communicate to a second SBC while running locally on a different SBC (for example, the KCS interface).
E158	Cannot contact the %1 while its carrier board is in firmware transfer mode.	It is not possible to communicate with a sub-FRU (for example, an RTM or AMC) while the carrier board (for example, SBC) is in firmware transfer mode. Try again later when the carrier is no longer in transfer mode, or bring the carrier out of transfer mode with the RadiSys OEM Exit FW Transfer mode command.
E204	RMCP connection to "%1" failed	An RMCP/RMCP+ session could not be activated with the target because of an earlier problem such as a bad username or password.
E206	Invalid Username	An RMCP/RMCP+ session can not be established because the supplied username was not accepted by the target.
E207	Invalid Password	An RMCP/RMCP+ session can not be established because the supplied password was not accepted by the target.
E213	The authentication type: %1 is unavailable for the selected privilege level	An RMCP/RMCP+ session can not be established because the desired authentication algorithm (for example, MD2, MD5, etc.) was refused by the target for the supplied privilege level. If no privilege is specified, the default privilege is administrator. If no privilege is specified, it is the same as typing –L administrator.
E214	No valid authentication type available	For the given user and channel, the target does not support MD5, MD2, straight password or none. This could mean the target is misconfigured, or that the target only supports an OEM authentication algorithm.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 89. Warning and Error Messages (Continued)

Number	Message	Description
E218	Unable to find suitable KCS Driver	No IPMI request can be made using any known IPMI device driver. For operating systems that have a compiled-in IPMI driver, this indicates that the KCS interface is in a bad state and may require a power cycle of the SBC and/or any attached sub-FRUs. For OSs that have loadable IPMI driver modules, the KCS interface could be broken as above, or else the IPMI driver service needs to be started with the /etc/init.d/ipmi start command.
E222	No slot available to establish session	For direct LAN communication to an SBC (for example, RMCP+ direct), the SBC already has its maximum number of RMCP+ sessions active and cannot accept a new session. For an RMCP bridge, it is the ShMC that cannot accept an additional RMCP/RMCP+ session.
E226	A LAN failure occurred	A LAN (that is RMCP/RMCP+) error occurred that is not described by an other situation in this table.
E546	Requested information not supported on the target	This message should only be displayed if there is an internal code error in which a FRU library operation is called without a specification of what operation is to be performed.
E700	Unsupported firmware update mode "%1". It must be one of %2	This error message is displayed when an unsupported mode is supplied on the command line. The command-line option is -M or --mode. %1 is replaced with what was supplied, and %2 is replaced with the mode types that are supported.
E701	You must supply exactly one input filename	This error message is displayed when a HEX file provided by RadiSys was not supplied on the command line, or if there is more than one file or option specified at the end of the command line.
E702	Manufacturer ID mismatch! The supplied input file is not intended for this target.	This error message is displayed when the supplied HEX file provided by RadiSys has a different manufacturer ID for the target SBC. This can be displayed whether performing a direct or staged firmware update.
E703	Product ID mismatch! The supplied input file is not intended for this target.	This error message is displayed when the supplied HEX file supplied by RadiSys has a different product ID for the target SBC. This can be displayed whether performing a direct or staged firmware update.
E704	Staged firmware updates are not available at this time. Either the target does not have that capability, or the target is in direct firmware transfer mode. Use -M direct or --mode direct to perform a firmware upgrade.	This error message is displayed when a staged firmware update was requested, but the target IPMC does not support them. This can only be displayed when specifically requesting a staged update with mode staged or -M staged.
E705	Firmware rollback updates are not supported for the specified target.	This error message is displayed if the IPMC does not support capturing a rollback image. This is more of a safety measure, and can be overridden with nocapturerb. This is only displayed if attempting a staged firmware update.
E706	Preparation of the staging flash area failed!	This error message is displayed if an error occurred while erasing the flash memory where the staging image is to be written. Failure cases can be a flash error, no permission, or a refused operation due to another operation being performed on the same area. The underlying library should supply a more descriptive message indicating what specifically failed. This is only displayed if attempting a staged firmware update.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 89. Warning and Error Messages (Continued)

Number	Message	Description
E707	Capture of the rollback image failed!	This error message is displayed if an error occurred while capturing the rollback image. Failure cases can be a flash error, no permission, or a refused operation due to another operation being performed on the same area. The underlying library should supply a more descriptive message indicating what specifically failed. This is only displayed if attempting a staged firmware update.
E708	Upload of the new staged image failed!	This error message is displayed if an error occurred while writing the new staging image to the staging area of flash memory. Failure cases can be a flash error, no permission, or a refused operation due to another operation being performed on the same area. The underlying library should supply a more descriptive message indicating what specifically failed. This is only displayed if attempting a staged firmware update.
E709	Registration of staged firmware update in flash failed!	This error message is displayed if an error occurred while writing to flash memory indicating the IPMC needs to perform a staged update on reset. Failure cases can be a flash error, no permission, or a refused operation due to another operation being performed on the same area. The underlying library should supply a more descriptive message indicating what specifically failed. This is only displayed if attempting a staged firmware update.
E710	Error updating the firmware!	This error message is displayed if any error occurred during a direct firmware update. Possible causes are communication failures during RMCP-related updates, flash errors, and no permission.
E711	Cannot cancel pending staged firmware updates because the target is in firmware transfer mode.	This error message is displayed if the cancel mode is requested, but the blade is in firmware transfer mode.
E712	Cannot register a manual rollback of the firmware because the target is in firmware transfer mode.	This error message is displayed if the rollback mode is requested, but the blade is in firmware transfer mode.
E713	Cannot cancel pending staged firmware updates because staged firmware updates are not supported by this target.	This error message is displayed if the cancel mode is requested, but staged firmware updates are not supported by the currently running firmware.
E714	Cannot register a manual rollback of the firmware because staged firmware updates are not supported by this target.	This error message is displayed if the rollback mode is requested, but staged firmware updates are not supported by the currently running firmware.
E720	Exit direct firmware update mode operation refused by target.	This error message is displayed if the Exit Firmware Transfer mode IPMI command is refused by the IPMC. This can happen if the IPMC is busy and is unable to switch states. This only happens during direct firmware updates.
E721	Write direct firmware update area operation refused by target.	This error message is displayed if a write command is refused by the IPMC. This can happen if the flash area is busy and cannot be accessed. This only happens during direct firmware updates.
E722	Verify direct firmware update area operation refused by target.	This error message is displayed if a read command is refused by the IPMC during write verification. This can happen if the flash area is busy and cannot be accessed. This only happens during direct firmware updates.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 89. Warning and Error Messages (Continued)

Number	Message	Description
E723	Flash error occurred during an exit direct firmware update mode operation.	This error message is displayed if a flash memory error is detected after attempting to exit Firmware Transfer Mode. This only happens during direct firmware updates.
E724	Flash error occurred during a write direct firmware update area operation.	This error message is displayed if a flash memory error is detected during a write operation. This only happens during direct firmware updates.
E725	Flash error occurred during a verify direct firmware update area operation.	This error message is displayed if a flash memory error is detected during a read operation while verification of the previous write. This only happens during direct firmware updates.
E726	Communication error while attempting to exit direct firmware update mode.	This error message is displayed if an IPMI communication failure occurs while sending the Exit Firmware Transfer Mode request. Communication failures can be caused by lossy networks if using RMCP or an RMCP bridge, excessive IPMB traffic within a chassis, or an overrun shelf manager (RMCP bridge only). This only happens during direct firmware updates.
E727	Communication error while attempting to verify direct firmware update area.	This error message is displayed if an IPMI communication failure occurs when sending a read request during verification. Communication failures can be caused by lossy networks if using RMCP or an RMCP bridge, excessive IPMB traffic within a chassis, or an overrun shelf manager (RMCP bridge only). This only happens during direct firmware updates.
E728	Communication error while attempting to set the write segment.	This error message is displayed if an IPMI communication failure occurs when attempting to set the current write segment. Communication failures can be caused by lossy networks if using RMCP or an RMCP bridge, excessive IPMB traffic within a chassis, or an overrun shelf manager (RMCP bridge only). This only happens during direct firmware updates.
E729	The target reports a previous staged firmware update failure.	This warning message is currently not displayed during a staged update. It is part of the GetStatus command. It would be displayed if a non-successful IPMI completion code was returned from the GetStatus command.
E730	IPMI error while attempting to register staged firmware update (completion code 0x%1).	This error message is displayed when an unknown, non-successful IPMI completion code is returned when registering the staged update in flash. This can only be displayed during a staged update. %1 is replaced with the IPMI completion code, displayed in hexadecimal format.
E731	IPMI error while attempting to close staging area (completion code 0x%1).	This error message is displayed when an unknown, non-successful IPMI completion code is returned when closing the staging area after an update has been performed. This can only be displayed during a staged update. %1 is replaced with the IPMI completion code, displayed in hexadecimal format.
E732	IPMI error while attempting to erase staging area (completion code 0x%1).	This error message is displayed when an unknown, non-successful IPMI completion code is returned when erasing the staging area prior to an update being performed. This can only be displayed during a staged update. %1 is replaced with the IPMI completion code, displayed in hexadecimal format.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 89. Warning and Error Messages (Continued)

Number	Message	Description
E733	IPMI error while attempting to capture rollback (completion code 0x%1).	This error message is displayed when an unknown, non-successful IPMI completion code is returned when capturing a rollback image. This can only be displayed during a staged update. %1 is replaced with the IPMI completion code, displayed in hexadecimal format.
E734	IPMI error while attempting to get staged update status (completion code 0x%1).	This error message is displayed when an unknown, non-successful IPMI completion code is returned when getting the status of an update. This is currently not being used. This can only be displayed during a staged update. %1 is replaced with the IPMI completion code, displayed in hexadecimal format.
E735	Register staged firmware update operation refused by target.	This error message is displayed when a register update operation is refused by the IPMC. This can happen if the firmware currently has that part of flash in use. This can only be displayed during staged updates.
E736	Close staging area operation refused by target.	This error message is displayed if the staged area is attempted to be closed and is refused by the IPMC. This can happen if the firmware currently has that part of flash in use. This can only be displayed during staged updates.
E737	Write staging area operation refused by target.	This error message is displayed if a write operation is refused by the IPMC during a staged update. This can happen if the firmware currently has that part of flash in use. This can only be displayed during staged updates.
E738	Erase staging area operation refused by target.	This error message is displayed if erasing the staging area is refused by the IPMC. This can happen if the firmware currently has that part of flash in use. This can only be displayed during staged updates.
E739	Capture rollback operation refused by target.	This error message is displayed if capturing the rollback image is refused by the IPMC. This can happen if the firmware currently has that part of flash in use. This can only be displayed during staged updates.
E740	Flash error occurred during a register staged firmware update operation.	This error message is displayed if a flash error occurs while registering the staged update in flash memory. This can only be displayed during staged updates.
E741	Flash error occurred during a close staging area operation.	This error message is displayed if a flash error occurs when closing the staging area. This can only be displayed during staged updates.
E742	Flash error occurred during an erase staging area operation.	This error message is displayed if a flash error occurs while the staging area of flash memory is being erased. This can only be displayed during staged updates.
E743	Communication error while attempting to write to the staging firmware area.	This error message is displayed if an IPMI communication failure occurs while writing a staged update. Communication failures can be caused by lossy networks if using RMCP or an RMCP bridge, excessive IPMB traffic within a chassis, or an overrun shelf manager (RMCP bridge only). This can only be displayed during staged updates.
E744	Capture rollback operation timed out, aborting staged firmware update.	This error message is displayed if the capture rollback operation does not abort with an error, but takes too long to complete. This can be caused by excessive load on the IPMC, or heavy flash memory access on the IPMC. This can only be displayed during staged updates.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 89. Warning and Error Messages (Continued)

Number	Message	Description
E745	The target reports that the staging area image is corrupt.	This error message is displayed if the Get Status command finds that the staging image is corrupt. Possible causes are undetected write errors or failing flash memory. This message is not displayed in the current version, since checks are performed during an update that satisfy this function.
E746	The target reports that the rollback area image is corrupt.	This error message is displayed if the Get Status command finds that the rollback image is corrupt. Possible causes are undetected write errors or failing flash memory. This message is not displayed in the current version, since checks are performed during an update that satisfy this function.
E749	File %1 cannot be opened: %2.	This error message is displayed if the provided filename cannot be opened. Examples are the file is missing or permissions are insufficient. %1 is replaced with the supplied filename, and %2 is replaced with the error.
E751	Unknown hex record type encountered at line %1.	This error message is displayed if the supplied file contains a record not conforming to the HEX record standard for RadiSys. This could indicate that the supplied file is corrupt. %1 is replaced by the line number in the file where the bad record was found.
E752	Hex record checksum incorrect at line %1.	This error message is displayed if the two's complement checksum of the hex record line does not match the line's checksum. This format is defined by the HEX record standard for RadiSys. This could indicate the supplied file is corrupt. %1 is replaced by the line number in the file where the bad record was found.
E753	Unable to allocate memory while parsing file.	This error message is displayed when the supplied filename is being read into memory, and the operating system runs out of available memory. This indicates that the client machine is running a large program, or may be running a program with a memory leak.
E754	No EOF hex record found. Supplied file appears to be corrupt.	This error message is displayed when the supplied file has no HEX EOF (end-of-file) record. This is defined by the HEX record standard for RadiSys. This could indicate the supplied file is corrupt.
E755	Unknown open failure for file %1.	This error message is displayed when an unknown error occurs while attempting to open the supplied file. This message is the last catch-all message to detect unknown failures. %1 is replaced with the supplied filename.
E756	The supplied file has an unsupported opcode header version (%1).	This error message is displayed if the supplied filename contains a data format for the operational code that is not supported. The data format could differ when major enhancements are made to the operational image. %1 is replaced with the opcode header version that was found in the supplied file.
E757	The supplied file does not contain a valid operational code header.	This error message is displayed if the header portion of the operational code image cannot be found. This could indicate the supplied file is corrupt.
E758	Invalid record length encountered at line %1.	This error message is displayed if the HEX record specifies a certain length for a record, but the data does not match that length. This could indicate the supplied file is corrupt.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 89. Warning and Error Messages (Continued)

Number	Message	Description
E759	Errors occurred while running prechecks. Aborting.	This error message is displayed if all other known checks and messages cannot catch the error. This message should not be seen in practical operation.
E760	The specified file %1 is an unknown file type.	This error message is displayed if a file is specified that has an unknown file extension. Valid file extensions are: .hex, .cfg, .fru, .bsdr, and.bfru.
E761	Staged FRU updates are not supported.	This error message is displayed if an FRU update is being performed, and the mode is staged.
E762	Cannot downgrade the firmware from version %1 to version %2 without the --force-fw-update flag.	This flag is required to show the user's intention to downgrade the firmware. If this is really the intended operation, supply the switch and this error no longer appears.
E764	Cannot perform an SDR update with a pending staged firmware image. Please cancel the staged update, or use --force-sdr-update or --no-reset.	If there is a pending staged firmware update, it is not possible to perform an SDR update that would reset the target. If the target were to reset after the SDR update (which is the default behavior), then the FW version would change also. To do the SDR update, either commit the pending firmware update by resetting the target, or prevent target reset after the SDR update with the --no-reset flag, or else give the --force-sdr-update flag to show that the pending firmware update should be committed at the same time.
E765	IPMI error when trying to contact the carrier board for the proxied target.	Before communicating with a sub-FRU such as an RTM or AMC, the carrier board (for example, an SBC) must be queried to see if it is in a mode that would prevent sub-FRU communication. This message is displayed if there is a timeout to this query.
E766	Cannot perform requested operations against the requested target. The target's carrier board is in firmware transfer mode, and cannot forward requests.	If a carrier board is in firmware transfer mode, then none of its sub-FRUs are contactable. It is not possible, for example, to update RTM firmware while its carrier is busy in firmware transfer mode.
E767	A timeout occurred waiting for the target management controller to reset.	After sbcupdate resets a target, it waits until the target is able to respond to a get device ID and the response indicates the target is no longer in firmware transfer mode.
E768	Error performing the requested operation	An operation failed with an unknown error. This is a generic catch-all and should not be displayed in practice.
E769	Requested operation not supported on the target.	A user attempted to get a type of information (for example, FRU, SDR, etc.) from a target that does not support that type.
E770	IPMI error during a Get Device Id transfer.	A non-successful completion code was returned for a Get Device ID command request.
E772	IPMI error during a Staged Get Capabilities transfer.	A non-successful completion code was returned for a Staged Get Capabilities command request.
E773	IPMI error during a Staged Get Version Data transfer.	A non-successful completion code was returned for a Staged Get Version command request.
E774	No valid staging or rollback images were found to register. Aborting.	A user attempted to use the rollback mode when there was no valid staged or rollback firmware image available.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 89. Warning and Error Messages (Continued)

Number	Message	Description
E775	Cannot perform a full FRU upgrade without specifying --force-fru-update. Performing a full FRU update will overwrite all data stored in the FRU such as serial numbers, part numbers, manufacture date, etc. Please supply a .cfg file name to perform an incremental FRU update.	This error message is displayed when a full FRU update is attempted without specifying the force flag on the command line. It also briefly states the impact of a full FRU update.
E776	Cannot downgrade the FRU from version %1 to version %2 without the --force-fru-update flag.	This error message is displayed on a FRU downgrade attempt without the force flag. The FRU downgrade attempt explicitly requires the –-force-fru-update flag.
E777	Cannot compare FRU Product ID. System FRU Product ID is missing. Use --force-id flag to update	This error message is displayed when the Product ID information in the existing system FRU is missing. Due to this, the Product ID in the supplied input FRU file and system FRU cannot be compared.
E778	Cannot downgrade the SDR from version %1 to version %2 without the --force-sdr-update flag.	This error message is displayed on an SDR downgrade attempt without the force flag. The SDR downgrade attempt explicitly requires the –force-sdr-update flag.
E779	Cannot compare SDR versions. Both System and File information is missing. Use --force-sdr-update flag to update	This error message is displayed when the SDR version information is missing from both the system SDR and the supplied input SDR file. Hence SDR version information cannot be compared.
E780	Cannot retrieve FRU/SDR data since the target is in firmware transfer mode.	This error message is displayed when FRU or SDR data is queried but the target is already in the firmware transfer mode.
E781	Cannot perform FRU update since the target is in firmware transfer mode.	This error message is displayed when a FRU update is attempted, but the target is already in the firmware transfer mode.
E782	Cannot perform SDR update since the target is in firmware transfer mode.	This error message is displayed when a SDR update is attempted but the target is already in the firmware transfer mode.
E784	Cannot compare both FRU Product ID and version. System information is missing. Use --force-id and --force-fru-update flag to update	This error message is displayed when both FRU product ID and version data from the system FRU is missing. In such a case, the user is directed to use the appropriate force flags to be able to perform the operation.
E785	Cannot compare both FRU Product ID and version. File information is missing. Use --force-id and --force-fru-update flag to update	This error message is displayed when both FRU product ID and version data from the supplied input FRU file is missing. In such a case, the user is directed to use the appropriate force flags to be able to perform the operation.
E786	Cannot compare FRU versions. System FRU version information is missing. Use --force-fru-update flag to update	This error message is displayed when the system FRU version information is missing and hence the FRU version data cannot be compared with the corresponding value in the supplied input FRU file. User is directed to use the appropriate force flag to be able to perform the operation.
E787	Cannot compare FRU versions. File FRU version information is missing. Use --force-fru-update flag to update	This error message is displayed when the FRU version information in the supplied input FRU file is missing and therefore the FRU version data cannot be compared with the corresponding value in the system FRU. The user is directed to use the appropriate force flag in order to perform the operation.
E788	Cannot compare FRU Product ID. File FRU Product ID is missing. Use --force-id flag to update	This error message is displayed when the FRU Product ID information in the supplied input FRU file is missing and therefore this data cannot be compared with the corresponding value in the system FRU. The user is directed to use the appropriate force flag in order to perform the operation.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 89. Warning and Error Messages (Continued)

Number	Message	Description
E789	Cannot compare FRU versions. Both File and System FRU version information is missing. Use --force-fru-update flag to update	This error message is displayed when the FRU version information is missing in both the supplied input FRU file and the system FRU. The user is directed to use the appropriate force flag in order to perform the operation.
E790	Cannot compare FRU Product ID. Both File and System FRU Product ID is missing. Use --force-id flag to update	This error message is displayed when the FRU Product ID information is missing in both the supplied input FRU file and the system FRU. The user is directed to use the appropriate force flag in order to perform the operation.
E791	Cannot compare both FRU Product ID and version. Both System and File information is missing. Use --force-id and --force-fru-update flag to update	This error message is displayed when both the FRU product ID and version data is missing from both the supplied input FRU file and the system FRU. The user is directed to use the appropriate force flags in order to perform the operation.
E792	Cannot compare SDR versions. File information is missing. Use --force-sdr-update flag to update	This error message is displayed when the SDR version information is missing from the supplied input SDR file. Therefore, this data cannot be compared with the system SDR version information. The user is directed to use the appropriate force flags in order to perform the operation.
E793	Cannot compare SDR versions. System information is missing. Use --force-sdr-update flag to update	This error message is displayed when the SDR version information is missing from the system SDR. Therefore, this data cannot be compared with the version information in the supplied input SDR file. The user is directed to use the appropriate force flags in order to perform the operation.
E800	Target is in firmware transfer mode. You must force the firmware update with --force-fw-update since another firmware update may be running right now.	When a target is in firmware transfer mode, it either means that a second user is actively updating the firmware, or that the target is in firmware transfer mode with no active update in progress. In the latter case, use the --force-fw-update flag to initiate an update.
W201	Bad hostname or IPv4 address "%1"	The argument to the --H/--host option contains an illegal character such as "~".
W202	Socket connection has been dropped	The socket connection is no longer open due either to network problems or the remote RMCP node (usually the ShMC) not responding.
W203	The selected user does not have %1 privilege level access	This message is displayed if, during RMCP/RMCP+ communication, the user given on the command line does not have administrative privilege, or does not have the privilege specified with the "-L" option. Either use a different user or configure the target so that the desired user has the required privilege.
W221	KCS Driver Failure	The IPMI driver is responding with an error such as a timeout.
W225	Non-standard RMCP bridging detected.	If, during an RMCP bridge, the ShMC responds to a send message request with data from the embedded send message request, this message is displayed. This type of send message response does not conform to the IPMI 2.0 specification. This is only a warning and not an error because sbcupdate is designed to work this way with a shelf manager that does not implement RMCP bridging per the specification.
W600	Upgrading with the same version of the firmware, version %1.	This warning message is displayed when the major, minor, and build version numbers of the firmware are the same between the SBC and supplied firmware image. This message can be displayed on both staged and direct firmware updates.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 89. Warning and Error Messages (Continued)

Number	Message	Description
W601	Retrying direct firmware update.	This warning message is displayed when any failure is detected during a direct firmware update, and the update is being retried. The retry is only attempted once, and implies that the whole image will be rewritten. For example, if the update is 90% complete and an error occurs, the retry begins at 0%.
W602	Target management controller currently in direct firmware update mode, cannot compare firmware versions.	This warning message is displayed when the target IPMC is in firmware transfer mode. When in this mode, the version of the current firmware is meaningless; therefore a comparison cannot be done between the supplied file and the target management controller. This message can be displayed on both staged and direct firmware updates.
W603	Downgrading the firmware from version %1 to version %2.	This warning message is displayed when the firmware is being downgraded. %1 is the current version, %2 is the version attempting to be programmed to the target IPMC.
W605	The target management controller needs to be manually reset for the SDR update to take effect.	This warning message is displayed when an SDR update is attempted specifying a -–no-reset flag (no reset) and there is a pending staged firmware image. For the SDR update to take effect, the target controller needs to be manually reset.
W606	Please ignore any select timeout warnings. They are issued by the Linux driver due to the target reset, and may be ignored.	When a target resets, for example after a firmware or SDR update, it may not be able to respond to the Linux IPMI driver's presence pings. If the driver does not receive a ping in time, the driver issues warning messages. These can safely be ignored.
W607	Downgrading the FRU from version %1 to version %2.	This warning message is displayed to indicate the direction of FRU update, as a downgrade from one version to another. %1 is replaced with the existing system FRU version. %2 is replaced with the older version that is being used as input for the update.
W608	Upgrading with the same version of the FRU, version %1.	This warning message is displayed to indicate the direction of FRU update, as a upgrade, but with the same version as exists on the system. %1 is replaced with the existing FRU version.
W609	Downgrading the SDR from version %1 to version %2.	This warning message is displayed to indicate the direction of SDR update, as a downgrade from one version to another. %1 is replaced with the existing system SDR version. %2 is replaced with the older version that is being used as input for the update.
W610	Upgrading with the same version of the SDR, version %1.	This warning message is displayed to indicate the direction of SDR update, as a upgrade but with the same version as exists on the system. %1 is replaced with the existing FRU version.
W611	Target is in firmware transfer mode, hence cannot display all information	This warning message is displayed to indicate that on the "Info" query, not all information can be displayed since the target is in firmware transfer mode.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 90. Mapping of Physical Slot to IPMB Address in Promentum™ MPCHC0001 14U Shelf

Physical Slot	Logical Slot	Hardware Address	IPMB Address
1	13	4Dh	9Ah
2	11	4Bh	96h
3	9	49h	92h
4	7	47h	8Eh
5	5	45h	8Ah
6	3	43h	86h
7	1	41h	82h
8	2	42h	84h
9	4	44h	88h
10	6	46h	8Ch
11	8	48h	90h
12	10	4Ah	94h
13	12	4Ch	98h
14	14	4Eh	9Ch

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

11.0 Specifications

This chapter provides the MPCBL0040 mechanical, environmental, and reliability specifications.

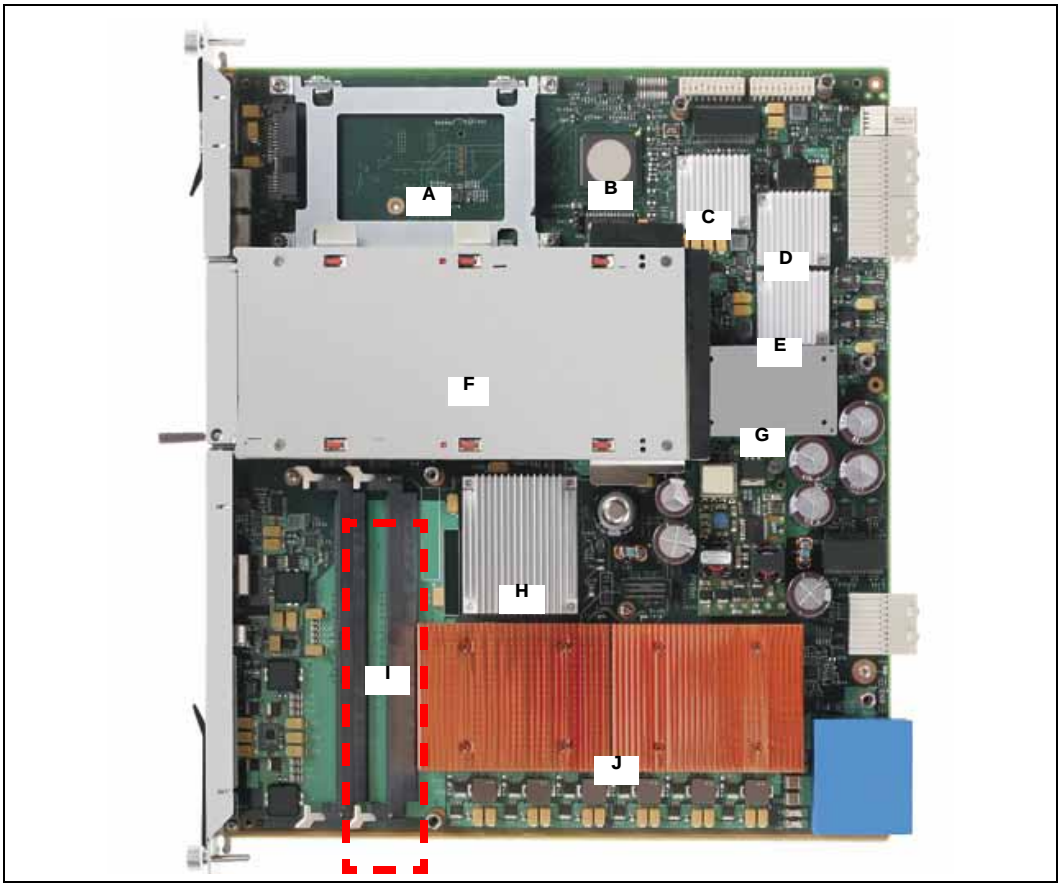
11.1 Mechanical Specifications

11.1.1 Board Outline

The MPCBL0040 form factor is mechanically compliant with the PICMG 3.0 Specification which stipulates dimensions of 322.25 mm x 280.00 mm (12.687" x 11.024"). The board pitch is 6HP, and the PCB thickness is 97 mm (±0.7 mm).

Figure 48 shows the locations of major components of the MPCBL0040 SBC. Table 91 lists the components shown in the figure.

Figure 48. Component Layout



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 91. Board Components

Label (Figure 48)	Component/Function
A	SAS Hard Disk Bay
B	LSI* 1068 SAS Controller
C	Intel® 82571EB Gigabit Ethernet Controller (Fabric Interface)
D	Intel® 82571EB Gigabit Ethernet Controller (Fabric Interface)
E	Intel® 82571EB Gigabit Ethernet Controller (Base Interface)
F	Advanced Mezzanine Card
G	Tyco* QBW -48V to 12V converter
H	Intel ® E7520 Memory Controller Hub (MCH)
I	DDR2 Memory Bank
J	Dual-Core Intel® Xeon® processor LV 2.0 GHz Processors

11.1.2 Backing Plate and Primary Side Top Cover

The MPCBL0040 SBC has a rugged metal backing plate that forms a single-piece faceplate. This backing plate is made of zinc-plated commercial-quality cold-rolled steel. The backing plate and integral faceplate are nominally 1.2 mm thick. The top cover is made of zinc-plated commercial-quality cold-rolled steel and is nominally 0.80 mm thick.

There are two removable cutouts on the top cover for easy access to memory modules and hard drive. The solid backing plate and top cover provide PCB stiffening, enhanced EMI protection from adjacent boards, and protection during flame tests.

Caution: Removing the backing plate can damage the components on the board and may void the warranty if any hardware is damaged during the removal/reattachment of the backing plate. No user-serviceable parts are available under the PCB. Do not remove the faceplate or backing plate.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

11.2 Environmental Specifications

The test methodology is a combination of RadiSys and NEBS test requirements with the intent that the product will pass pure system-level NEBS testing. The MPCBL0040 has passed board level tests that are applicable to NEBS.

Table 92 summarizes environmental limits, both operating and nonoperating.

Table 92. Environmental Specifications

Parameter	Conditions	Detailed Specification
Temperature (Ambient)	Operating	-5 to 55° C
	Storage	-40 to 70° C
Airflow	Operating	30 cubic feet per minute (CFM) minimum
Humidity	Operating	15%-90% (non-condensing) at 55° C
	Storage	5%-95% (non-condensing) at 40° C
Altitude	Operating	4,000 m (13,123 ft.) Note: May require additional cooling above 1800 m (5,905 ft.).
	Storage	15,000 m (49,212 ft.)
Unpackaged Vibration	Operating	Sine sweep: • 5 to 100 Hz: 0.1G @ 0.1 Octave/minute Random profile: • 5 Hz @ 0.01 g2 /Hz to 20 Hz @ 0.02 g2 /Hz (slope up) • 20 Hz to 500 Hz @ 0.02 g2 /Hz (flat) • 3.13 g RMS, 10 minutes per axis for all three axes
	Storage	5 to 50 Hz: 0.5G @ 0.1 Octave/minute 50 to 500 Hz: 3G @ 0.25 Octave/minute
Shock	Storage	50G, 170 inches/second trapezoidal

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

11.3 Reliability Specifications

11.3.1 Mean Time Between Failure (MTBF) Specifications

Calculation Type: MTBF/FIT Rate

Standard: Telcordia* Standard SR-332 Issue 1

Methods: Method I, Case I, Quality Level II

The calculation results were generated using the references and assumptions listed. This report and its associated calculations supersede all other released Mean Time Between Failures (MTBF) and Failure in Time (FIT) calculations of earlier report dates. The reported failure rates do not represent catastrophic failure. Catastrophic failure rates will vary based on application environment and features critical to the intended function.

Table 93. Reliability Estimate Data

Failure Rate (FIT)	11,472 failures in 10^9 hours
MTBF	87,166 hours

Note: The MTBF data is calculated without the hard disk, AdvancedMC and DIMMs installed.

11.3.1.1 Environmental Assumptions

- Failure rates are based on a 40° C ambient temperature.
- Applied component stress levels are 50% (voltage, current, and/or power).
- Ground, fixed, controlled environment with an environmental adjustment factor equal to 1.0.

11.3.1.2 General Assumptions

- Component failure rates are constant.
- Board-to-system interconnects included within estimates.
- Non-electrical components (screws, mechanical latches, labels, covers, etc.) are not included within estimations.
- Printed circuit board is considered to have a 0 FIT rate.

11.3.1.3 General Notes

- Method I, Case I = Based on parts count. Equipment failure is estimated by totaling device failures rates and quantities used.
- Quality Level II = Devices purchased to specifications, qualified devices, vendor lot-to-lot controls for AQLs and DPMs.

Where available, direct component supplier predictions or actual FIT rates have been used.

The SBC MTBF does not include addition of the AMCs, hard drives or memory. Please contact the manufacturer for specific component and relevant operational MTBF information.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

11.4 Power Consumption

The power consumed by the MPCBL0040 SBC is dependent on the configuration and workload. Table 94 shows operating voltage ranges and Table 95 gives total measured power values for selected board configurations.

Table 94. Operating Voltage Ranges

Operating Modes	Voltage
Normal	-38 VDC to -72 VDC
Non-Operating	0 VDC to < -38 VDC, -72 VDC to -75 VDC

Note: These voltages assume a 1 V round trip drop on power signals between shelf power input terminals and board/module slots.

Table 95. Total Measured Power

Configuration	Max Power
Two 4 GByte DIMMs 1 Local SAS HDD No AdvancedMC No RTM	140 W
Two 4Gbye DIMMs 1 Local SAS HDD AdvancedMC (25 W max.) No RTM	165 W
Two 4 GByte DIMMs 1 Local SAS HDD AdvancedMC (25 W max.) RTM: MPRTM0040 (9 W max. without RTM hard drive)	174W
Two 4 GByte DIMMs 1 Local SAS HDD AdvancedMC (25 W max.) RTM: MPRTM0040 (20 W max. with RTM hard drive)	185 W

The board requests 140W during power negotiations with the ShMM.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

11.5 Board Layer Specifications

- Material: TG180 FR4
- Layers: 16
- Copper:
  - Outer layers 1 and 16 are 0.5 oz. copper plated.
  - Middle planes 3, 5, 7, 10, 12, and 14 are 0.5 oz. copper.
  - All others are 1 oz. copper.

11.6 Cooling Requirements

The MPCBL0040 SBC should be installed vertically in a chassis, with bottom-to-top airflow. Airflow is expected to be distributed across the bottom edge of the installed MPCBL0040 blade and to maintain at least 30 cubic feet per minute (CFM) airflow.

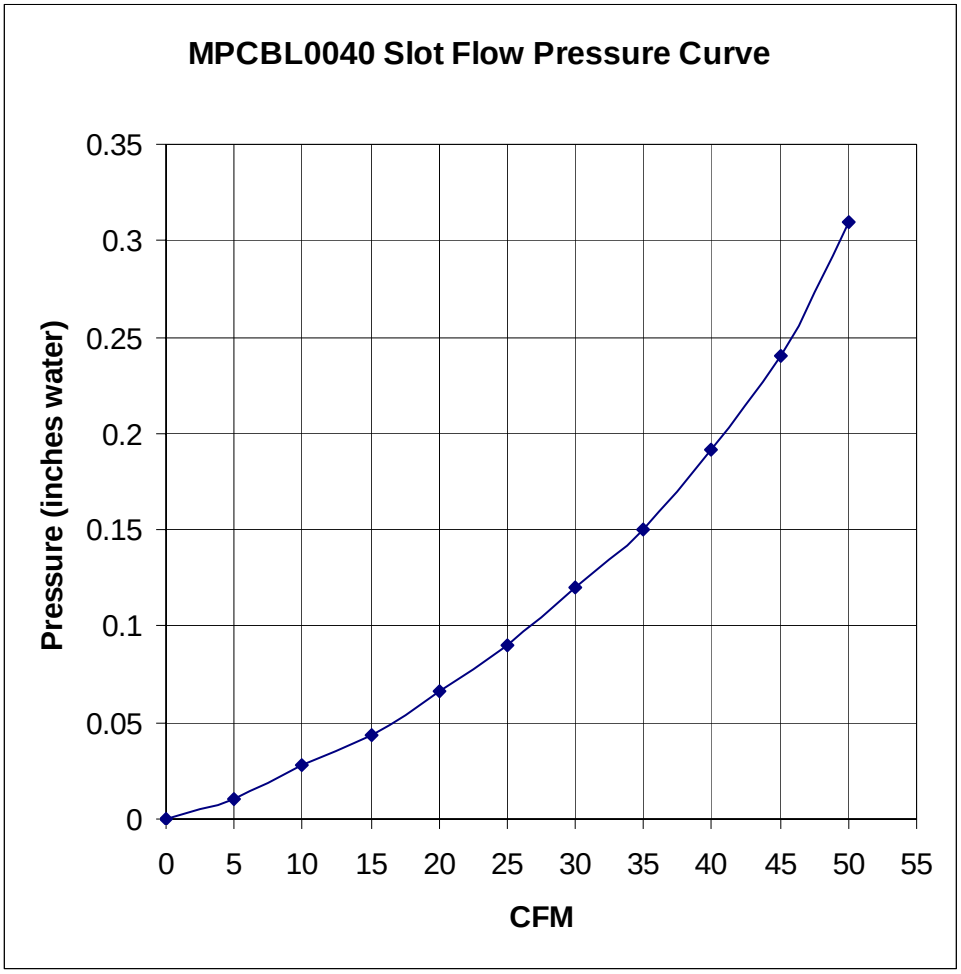
- Most components on the MPCBL0040 blade are specified to operate with a localized ambient temperature up to 70° C and do not require heat sinks.
- The MPCBL0040 blade uses custom heat sinks designed by RadiSys. The following are the on-board components that have heat sinks installed:
  - Processors
  - GbE Controllers (Intel® 82571EB Gigabit Ethernet Controller)
  - Memory Controller Hub (Intel® E7520 Memory Controller Hub Chipset)
- The rate of airflow specified above is critical to ensuring that the blade operates as designed.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

11.7 Thermals

The curve of the pressure drop versus the flow rate in Figure 49 represents the flow impedance of the slot. This information is provided in accordance with Section 5 of the PICMG 3.0 Specification to aid system integrators in using the Promentum™ MPCBL0040 Single Board Computer in various AdvancedTCA* shelves.

Figure 49. Pressure vs. Flow Rate



Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

11.8 Weight

The weight of the baseboard is 3.31 kg (7.3 lbs) with no DIMMs, no hard drive, no packaging materials and one AdvancedMC filler panel installed.

The SAS hard drive adds approximately 0.21 kg (0.5 lbs). For the most accurate hard drive weight, please check with the manufacturer for the particular make/model of interest.

Each DIMM adds up to approximately 0.045 kg (0.10 lbs). For the most accurate memory weight, please check with the manufacturer for the particular make/model of interest.

The packaged weight of the MPCBL0040 is 4.08 kg (9 lbs). Packaged weight includes baseboard, packaging materials and one AdvancedMC filler panel. DIMMs and hard drive do not ship with the board are not included in the package weight.

11.9 Compliance

The MPCBL0040 product conforms to the following specifications:

- AdvancedTCA 3.0 R1.0 and ECN001 (AdvancedTCA base specification)
- AdvancedTCA 3.1 R1.0 (Ethernet/Fibre Channel over AdvancedTCA)
- AdvancedMC AMC.0 R1.0 (AdvancedMC base specification)
- AdvancedMC AMC.1 R1.0 (PCI Express and Advanced Switching)
- AdvancedMC AMC.2 R1.0 (Gb Ethernet)

IPMI 2.0 (Intelligent Platform Management Interface)

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

12.0 Agency Information

12.1 North America (FCC Class A)

Federal Communications Commission (FCC) Part 15 Rules

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

12.2 Canada – Industry Canada (ICES-003 Class A)

Industry Canada ICES-003 Issue 3

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe A respecte toutes les exigences du Règlement sur le matérial brouilleur du Canada.

12.3 European Union

The products covered by this notice meet the following European Directives:

- 73/23/EEC Low Voltage Directive
- 89/336/EEC EMC Directive

To achieve CE compliance, be sure to select a host that already meets the EMC and Low Voltage Directives before the addition of any optional board. Remember that the use of option boards declared compliant with the Directives by their manufacturer only gives “presumption of compliance” for the whole system. It is the responsibility of the system supplier to verify that the requirements of the listed Directives are still met by the final system, as supplied to the end-user. System integrators should take notice of further conditions expressed in the sections below and the Safety Information sheet supplied with each board.

Warning: This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

13.0 Certifications

Safety:

- IEC60950-1
- EN60950
- UL/CSA 60950-1

Hazardous substances:

- The Promentum™ MPCBL0040N01Q has been verified to be compliant with the European Directive 2002/95/EC, officially titled “The Restriction on the Use of Hazardous Substances (RoHS) in Electrical and Electronic Equipment” or RoHS. Specifically, this product uses only RoHS compliant parts and Pb-free solder and may take advantage of certain exemptions referenced within the Directive.
- The Material Declaration Datasheets (MDDS) is available on request.

Electromagnetic Compatibility (EMC) emissions:

- CISPR22/EN55022 Class A
- EN300386
- FCC Rules CFR 47 Part 15B Class A
- ICES-003 Class A

Electromagnetic Compatibility (EMC) immunity:

- CISPR24/EN55024
- EN300386

Network Equipment Building System (NEBS) compliance:

- The test methodology is a combination of RadiSys and NEBS test requirements with the intent that the product will pass pure system-level NEBS testing.
- RadiSys has performed NEBS testing from GR-1089-CORE and GR-63-CORE that is applicable at the board level.
- The Ethernet ports on the front panel of the MPCBL0040 SBC must used shielded Ethernet cable and both ends of the shield must be grounded.
- RadiSys has performed testing from ETSI 300 019 that is applicable at the board level.

United States Export Classification:

- 5D002 Unrestricted

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

14.0 Safety Warnings

14.1 Safety Precautions

Review the following precautions to avoid personal injury and prevent damage to this product or products to which it is connected. To avoid potential hazards, use the product only as specified.

Read all safety information and understand the precautions associated with safety symbols, written warnings, and cautions before accessing parts or locations within the unit.

SYSTEM FOR RESTRICTED ACCESS USE ONLY!

Warning: To avoid the risk of electrical shock hazard, special measures and precautions must be taken when using these products:
- Access to this equipment must be restricted by locating this equipment where access can only be gained by SERVICE PERSONNEL who have been informed about the reasons for the restrictions applied to the location and about any precautions that shall be taken. Access is through the use of a TOOL, lock and key, or other means of security and is controlled by the authority responsible for the location.
- This product should only be used by SERVICE PERSONNEL who have the knowledge and training required to work with products of this type.
- To avoid shock, ensure that the chassis power cables are connected to a properly wired and grounded receptacle.
- The system containing these boards should not be operated with the faceplates, blank panels, or covers removed. Some voltages, that are on the board and inside the chassis, present an electrical shock and/or energy hazard to the user. Keep hands out of the chassis when power is applied or when performing hot swap of the boards.

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Appendix A: Supported IPMI Commands

Table 96 shows the IPMI commands supported by the MPCBL0040 SBC.

Table 96. Supported IPMI Commands (Sheet 1 of 6)

Command	NetFn	Cmd
IPM Device "Global" Commands		
Get Device ID	App	01h
Cold Reset	App	02h
Get Self Test Results	App	04h
Set ACPI Power State	App	06h
Get ACPI Power State	App	07h
BMC Watchdog Timer Commands		
Reset Watchdog Timer	App	22h
Set Watchdog Timer	App	24h
Get Watchdog Timer	App	25h
BMC Device and Messaging Commands		
Set BMC Global Enables	App	2Eh
Get BMC Global Enables	App	2Fh
Clear Message Flags	App	30h
Get Message Flags	App	31h
Get Message	App	33h
Send Message	App	34h
Read Event Message Buffer	App	35h
Get System GUID	App	37h
Get Channel Authentication Capabilities	App	38h
Get Session Challenge (through LAN interface only)	App	39h
Activate Session (through LAN interface only)	App	3Ah
Set Session Privilege Level (through LAN interface only)	App	3Bh
Close Session (through LAN interface only)	App	3Ch
Get Session Info (through LAN interface only)	App	3Dh
Get AuthCode	App	3Fh
Set Channel Access	App	40h

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 96. Supported IPMI Commands (Sheet 2 of 6)

Command	NetFn	Cmd
Get Channel Access	App	41h
Get Channel Info	App	42h
Set User Access	App	43h
Get User Access	App	44h
Set User Name	App	45h
Get User Name	App	46h
Set User Password	App	47h
Activate Payload	App	48h
Deactivate Payload	App	49h
Get Payload Activation Status	App	4Ah
Get Payload Instance Info	App	4Bh
Set User Payload Access	App	4Ch
Get User Payload Access	App	4Dh
Get Chan Payload Support	App	4Eh
Get Chan Payload Version	App	4Fh
Get Chan OEM Payload Info	App	50h
Master Write Read I2C	App	52h
Get Chan Cipher Suites	App	54h
Suspend Payload Encryption	App	55h
Set Channel Security Keys	App	56h
Reserved	App	E0h
Chassis Device Commands – 00h		
Get Chassis Status	Chassis	01h
Chassis Control	Chassis	02h
Get System Restart Cause	Chassis	07h
Set System Boot Options	Chassis	08h
Get System Boot Options	Chassis	09h
Event Commands – 04h		
Set Event Receiver	S/E	00h
Get Event Receiver	S/E	01h
Platform Event (a.k.a. “Event Message”)	S/E	02h
PEF and Alerting Commands – 04h		
Get PEF Capabilities	S/E	10h
Arm PEF Postpone Timer	S/E	11h
Set PEF Configuration Parameters	S/E	12h
Get PEF Configuration Parameters	S/E	13h
Set Last Processed Event ID	S/E	14h
Get Last Processed Event ID	S/E	15h
Sensor Device Commands – 04h		

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 96. Supported IPMI Commands (Sheet 3 of 6)

Command	NetFn	Cmd
Get Device SDR Info	S/E	20h
Get Device SDR	S/E	21h
Reserve Device SDR Repository	S/E	22h
Set Sensor Hysteresis	S/E	24h
Get Sensor Hysteresis	S/E	25h
Set Sensor Threshold	S/E	26h
Get Sensor Threshold	S/E	27h
Set Sensor Event Enable	S/E	28h
Get Sensor Event Enable	S/E	29h
Re-arm Sensor Events	S/E	2Ah
Get Sensor Event Status	S/E	2Bh
Get Sensor Reading	S/E	2Dh
RadiSys OEM Commands (RadiSys = 08h)		
Reserved	FWTR	00h - 07h
Retry Power On	FWRT	10h
Reserved	FWRT	20h
FRU Device Commands – 0Ah		
Get FRU Inventory Area Info	Storage	10h
Read FRU Data	Storage	11h
Write FRU Data	Storage	12h
SDR Repository Commands – 0Ah		
Get SDR Repository Info	Storage	20h
Get SDR Repository Allocation Info	Storage	21h
Reserve SDR Repository	Storage	22h
Get SDR	Storage	23h
Add SDR	Storage	24h
Partial Add SDR	Storage	25h
Delete SDR	Storage	26h
Clear SDR Repository	Storage	27h
Get SDR Repository Time	Storage	28h
Set SDR Repository Time	Storage	29h
Enter SDR Repository Update Mode	Storage	2Ah
Exit SDR Repository Update Mode	Storage	2Bh
Run Initialization Agent	Storage	2Ch
SEL Device Commands – 0Ah		
Get SEL Info	Storage	40h
Get SEL Allocation Info	Storage	41h
Reserve SEL	Storage	42h
Get SEL Entry	Storage	43h
Add SEL Entry	Storage	44h

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 96. Supported IPMI Commands (Sheet 4 of 6)

Command	NetFn	Cmd
Partial Add SEL Entry	Storage	45h
Delete SEL Entry	Storage	46h
Clear SEL	Storage	47h
Get SEL Time	Storage	48h
Set SEL Time	Storage	49h
LAN Device Commands – 0Ch		
Set LAN Configuration Parameters	Transport	01h
Get LAN Configuration Parameters	Transport	02h
Suspend BMC ARPs	Transport	03h
Get IP/UDP/RMCP Statistics	Transport	04h
Serial/Modem Device Commands – 0Ch		
Set Serial/Modem Configuration	Transport	10h
Get Serial/Modem Configuration	Transport	11h
Set Serial/Modem Mux	Transport	12h
Serial/Modem Connection Active	Transport	18h
Callback	Transport	19h
Set SOL 2.0 Configuration	Transport	21h
Get SOL 2.0 Configuration	Transport	22h
AdvancedTCA™ - 2Ch		
Get PICMG Properties	PICMG*	00h
Get Address Info	PICMG	01h
FRU Control	PICMG	04h
Get FRU LED Properties	PICMG	05h
Get LED Color Capabilities	PICMG	06h
Set FRU LED State	PICMG	07h
Get FRU LED State	PICMG	08h
Set IPMB State	PICMG	09h
Set FRU Activation Policy	PICMG	0Ah
Get FRU Activation Policy	PICMG	0Bh
Set FRU Activation	PICMG	0Ch
Get Device Locator Record ID	PICMG	0Dh
Set Port State	PICMG	0Eh
Get Port State	PICMG	0Fh
Compute Power Properties	PICMG	10h
Set Power Level	PICMG	11h
Get Power Level	PICMG	12h
Get Fan Speed Properties	PICMG	14h
Get IPMB Link Info	PICMG	18h
Set AMC Port State (AMC.0)	PICMG	19h
Get AMC Port State (AMC.0)	PICMG	1Ah

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 96. Supported IPMI Commands (Sheet 5 of 6)

Command	NetFn	Cmd
FRU Control Capabilities	PICMG	1Eh
RadiSys OEM Commands (RadiSys = 30h)		
Change BIOS Boot Flash	INTEL	01h
Set Fabric Interface Selection	INTEL	02h
Get Fabric Interface Selection	INTEL	03h
Get Fabric Interface Actual Selection	INTEL	04h
Reserved	INTEL	05h - 06h
Get Version Data	INTEL	07h
Reserved	INTEL	08h - 09h
AMC Fabric Interface Selection	INTEL	0Ah
Reserved	INTEL	0Bh - 0Fh
Reserved	INTEL	18h - 20h
Get DIMM State	INTEL	21h
Set DIMM State	INTEL	22h
ReArm DIMMs	INTEL	23h
Reserved	INTEL	24h
Sync SMBus Arbitration	INTEL	25h
Set Processor Status	INTEL	28h
Get Processor Status	INTEL	29h
ReArm Processors	INTEL	2Ah
Disable FRB Action	INTEL	2Bh
Reserved	INTEL	30h - 32h
Set System GUID	INTEL	41h
SetAuxChannelInfo	INTEL	42h
SetGetSDRTransChans	INTEL	43h
Log Post Code	INTEL	47h
SEL Internal Platform Event	INTEL	48h
Set SM Signal	INTEL	50h
Get SM Signal	INTEL	51h
Get Self Test History	INTEL	52h
Reserved	INTEL	53h
Manufacturing Test Mode	INTEL	54h
Graceful OS Shutdown	INTEL	70h
Init Agent Started	INTEL	80h
Init Agent End	INTEL	81h
Get ACPI Configuration	INTEL	82h
Set ACPI Configuration	INTEL	83h
Reserved	INTEL	84h
Reserved	INTEL	86h - 8Ch
Reserved	INTEL	A0h - A8h

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Table 96. Supported IPMI Commands (Sheet 6 of 6)

Command	NetFn	Cmd
Reserved	INTEL	B0h - B4h
Reserved	INTEL	C2h - C3h
Get NMI Source	INTEL	E6h
Set NMI Source	INTEL	EDh
NMI Enable Disable	INTEL	F7h
Get Latest Port80 Codes	INTEL	FAh
Other RadiSys OEM Commands: PLAT=32h		
Get HW Info	PLAT	01h
Get Power Unit Status	PLAT	02h
Reserved	PLAT	03h
Reserved	PLAT	55h
Reserved	PLAT	57h
Reserved	PLAT	5Fh

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Appendix B: Reference Documents

The following documents should be available when using this specification.

- PICMG AdvancedTCA Specification (http://www.advancedtca.org)
- PICMG Advanced Mezzanine Card Specification (http://www.picmg.org)
- Renesas H8S/2168 Group Product Specification (http://www.renesas.com/fmwk.jsp?cnt=h8s2168_root.jsp&fp=/products/mpumcu/h8s_family/h8s2100_series/h8s2168_group/)

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Artisan Scientific - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisan-scientific.com

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP