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SF810 Endura Micro NLX Motherboard Product Manual

Revision 1.1
July 2000

Revision History

Revision	Revision History	Date
1.0	First Release	June 2000
1.1	Revised video memory allocation description for Intel PV 4.x drivers.	July 2000

Notational Conventions

This manual uses the following conventions:

- Screen text and syntax strings appear in this font.
- All numbers are decimal unless otherwise stated ('h' indicates a hexadecimal number).
- Bit 0 is the least-significant bit. If a bit is set to 1, the associated description is true unless otherwise stated.



Warnings indicate situations that may result in physical harm to you or the hardware.



Cautions indicate situations that may result in damage to data or the hardware.



Notes indicate important information about the product.



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When removing or replacing the lithium cell, do not use a conductive instrument as a short-circuit may cause the cell to explode. Always replace the cell with one of the same type. This product uses a CR2032 cell. Dispose of a spent cell promptly – do not recharge, disassemble or incinerate. Keep cells away from children.

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This product contains static-sensitive components and should be handled with care. It is recommended that the product be handled in a Special Handling Area (SHA) as defined in EN100015-1:1992. Such an area has working surfaces, floor coverings and chairs connected to a common earth reference point. An earthed wrist strap should be worn whilst handling. Other examples of static-sensitive devices are the memory modules and the processor. Failure to employ adequate anti-static measures can cause irreparable damage to components on the motherboard.

Safety

This product complies with the American Safety Standard UL1950.

Electromagnetic Compatibility

This product complies with the following EMC standards.

FCC Class B (Title 47 of Code of Federal Regulations, parts 2 & 15, subpart B)
EN55022:1998 Class B
EN55024:1998

FCC Compliance Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures.

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and the receiver

- Connect the equipment into an outlet on a different circuit to that of the receiver
- Consult the dealer or an experienced radio/TV technician for help.

Any change or modification to this product not expressly approved by RadiSys could void the approvals held by this product.

Legal Directives

This product complies with the relevant clauses of the following European Directives.

Low Voltage Directive	73/23/EEC
EMC Directive	89/336/EEC
CE Marking Directive	93/68/EEC

This product, when supplied, complies with the CE Marking Directive and its strict legal requirements. Use only parts tested and approved by RadiSys.

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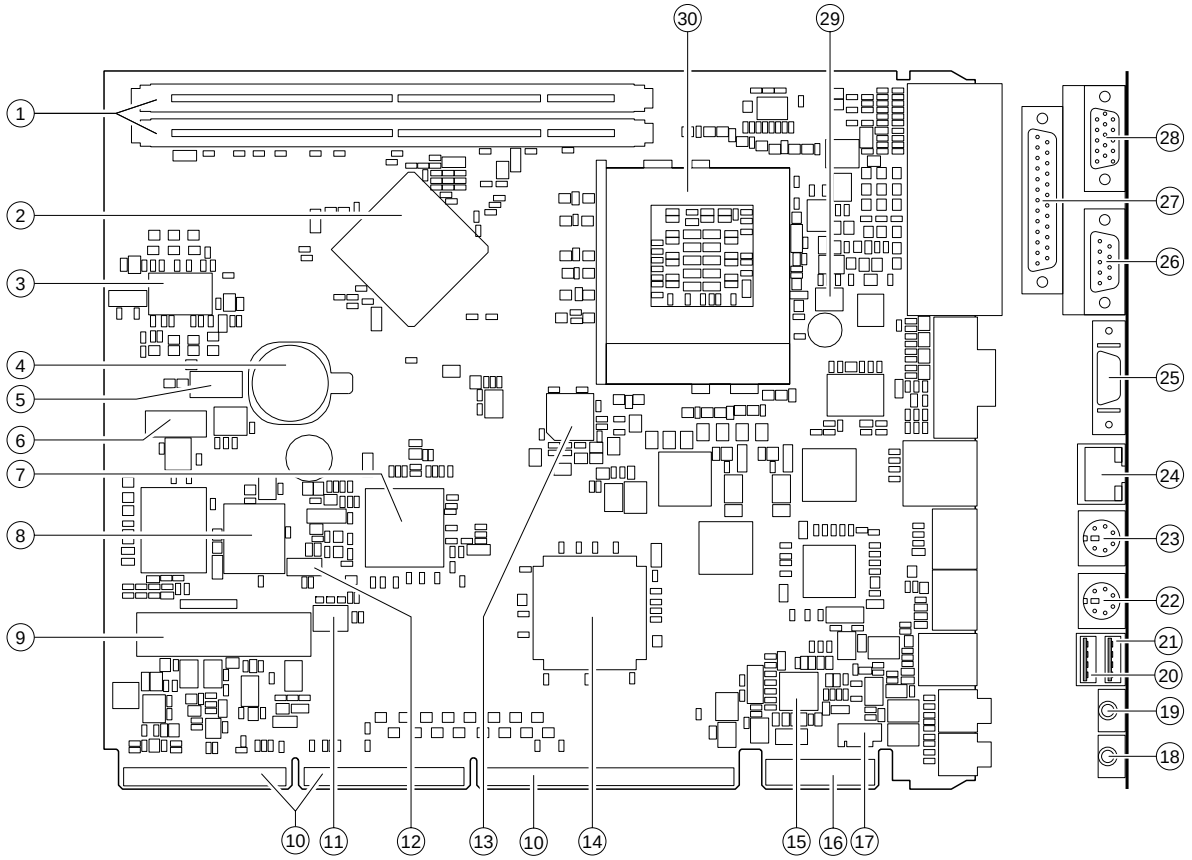
1 Overview

The SF810 “Springfield” is a Micro NLX form factor motherboard based around an Intel Celeron or Pentium III processor and an Intel 810 family chipset. It integrates video, audio, system monitoring and Ethernet on a 10.0 x 8.25-inch board and is targeted at the embedded PC technology market.

Form Factor	Micro NLX, 10.0 x 8.25 inches
Processor	370 pin PGA socket for Intel Celeron and Pentium III processors 66 or 100 MHz bus speed
Chipset	Intel 810 PCI / ISA bridge
Flat Panel	On-board PanelLink flat panel controller Support for DDWG DVI & VESA DFP
Memory	Two DIMM sockets for PC100 SDRAM modules without ECC or parity Min 16MB Max 512MB memory
Video	3D graphics controller integrated within chipset
Audio	AC97 v2.1 CODEC Digital audio controller integrated within chipset MIC and Line-out jacks on rear panel CD input on motherboard CD input, telephony and Line-out via riser supplemental connector
Power Management	APM, ACPI, PCI PME
System Management	Voltage, temperature and fan monitoring Fan control
BIOS	Based on Phoenix 4.0 release 6 4Mbit device Includes POST, Setup, SMBIOS, ACPI, APM, PnP, video BIOS Customizable startup logo
I/O	Dual rear USB 1.1 (or single rear plus single riser) Two serial ports (one on header) Bi-directional/EPP/ECP parallel port PS/2 keyboard and mouse IrDA General Purpose I/O Lines (8)
Network	Intel 82559ER-based 10/100Mbps Ethernet
Disks	Dual UltraDMA/66 interfaces with ATAPI CD, LS120 and ZIP drive support 3-mode floppy interface with on-board connector
Expansion	Supports up to 5 PCI and 5 ISA slots via riser

1.1 Motherboard Layout

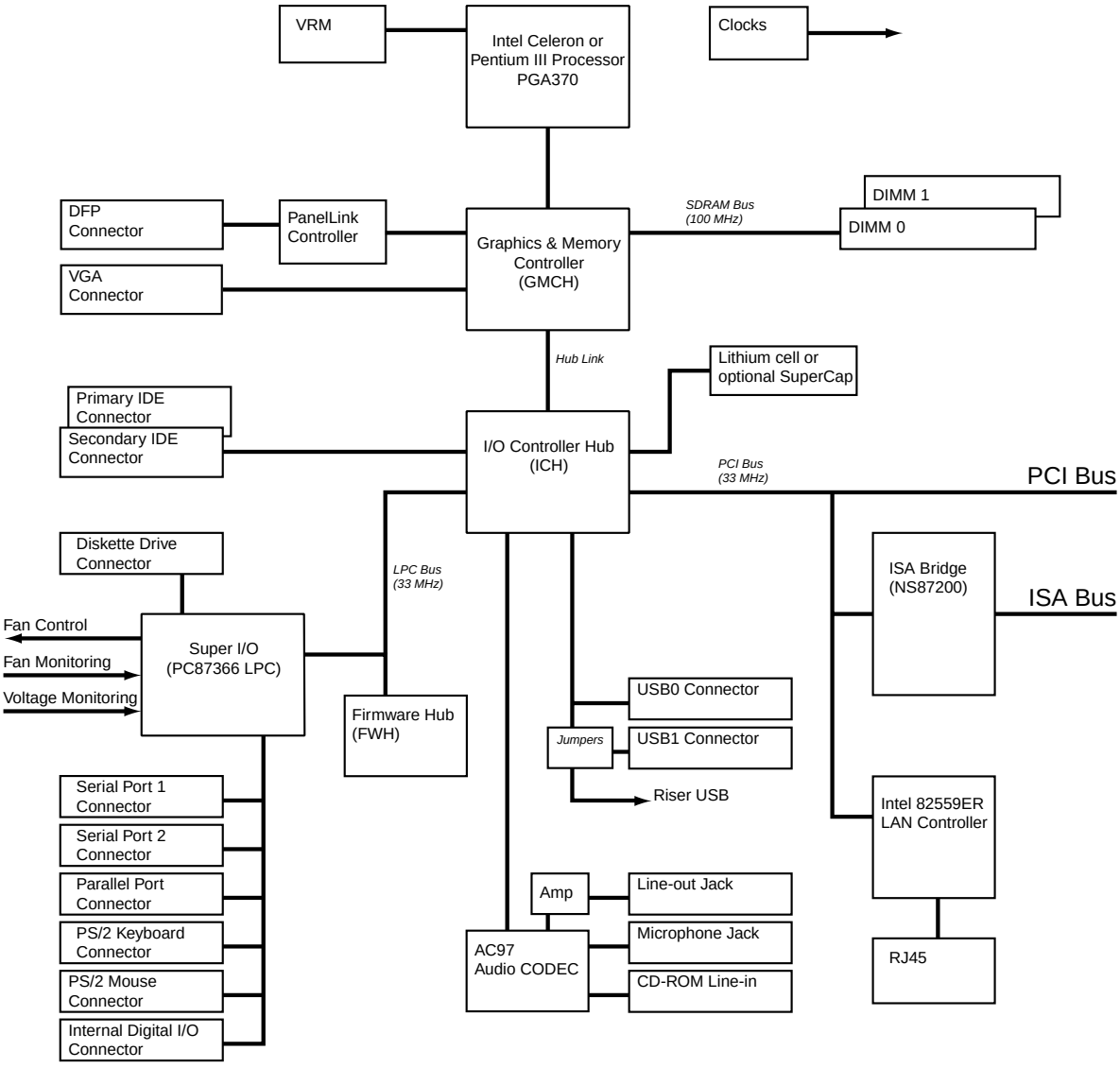
The figure below shows the layout of the SF810 motherboard with the major components identified.



1	PC100 DIMM sockets	**16**	NLX supplementary edge connector
2	Graphics & memory controller (GMCH)	**17**	ATAPI CD-ROM audio header
3	Clock generator	**18**	Mono microphone input
4	3V Lithium cell – use CR2032	**19**	Stereo audio line output
5	Serial port 2 header	**20**	USB 1.1 channel 1
6	GPIO header	**21**	USB 1.1 channel 0
7	I/O controller hub (ICH)	**22**	PS/2 mouse
8	Firmware hub (FWH)	**23**	PS/2 keyboard
9	Diskette header (optional)	**24**	10/100 Ethernet RJ45
10	NLX edge connectors	**25**	Digital Flat Panel (DFP) monitor
11	USB port 1 configuration jumpers	**26**	Serial port 1
12	Operating mode jumper	**27**	Parallel port
13	Digital flat panel converter	**28**	VGA monitor
14	ISA bridge (NS87200)	**29**	Processor fan power connector
15	AC97 audio CODEC	**30**	PGA370 socket for processor

1.2 Block Diagram

The figure below shows a block diagram of the SF810 motherboard.



1.3 Product Options

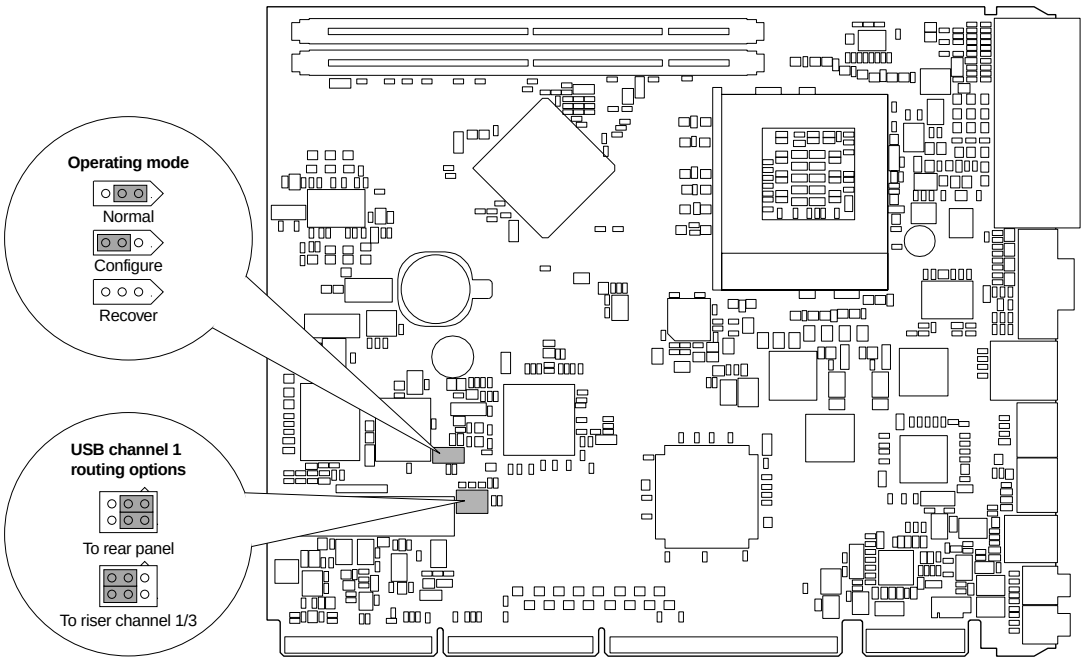
The table below lists the product options available.

Functions	SF810-V	SF810-L	SF810-FPL
ISA support	Yes	Yes	Yes
Flat panel interface	No	No	Yes
LAN	No	82559ER	82559ER
SuperCap	No	No	No

Each of the products is available with a choice of CPU speed. Consult the latest price list for the available options. Other product options are available to special order for high volume customers.

1.4 Configuration

The majority of the configuration of the motherboard is done through the Setup utility built into the BIOS – discussed later in this document. There are, however, three jumpers that also control the operation of the motherboard and these are described below.



1.4.1 Operation Mode Selection

This jumper selects one of three operating modes for the motherboard – Normal, Configure and Recovery modes. The factory default position for this jumper selects 'Normal' mode.

Normal Mode
This is the position the jumper should be in for normal operation of the motherboard. If the motherboard detects corruption in the BIOS ROM, then recovery mode will be entered regardless of the state of the jumper.

Recovery Mode
If the jumper is in the recovery mode position or if the motherboard detects a corrupted BIOS ROM then recovery mode is entered. The motherboard will not boot and will wait until a valid recovery diskette is detected and will then copy a new BIOS into the ROM. The motherboard must be powered down and then re-powered with the jumper in the normal position before normal operation can resume.

Configure Mode
With the jumper in this position the motherboard will automatically run the BIOS Setup utility regardless of the state of the Setup disable flag that can be set in the BIOS defaults. Additional BIOS settings are also available within Setup in this mode.

1.4.2 USB Channel 1 Routing

The USB routing jumpers allow the motherboard to be configured to route channel 1 to the rear connector (top socket of the dual USB connector) or to the riser (on riser channel 1/3). The factory default jumper position routes the USB to the rear panel.

2 Motherboard Description

2.1 Processor

The SF810 motherboard supports Intel Celeron and Pentium III processors in a PGA370 package (either PPGA or FC-PGA). The table below lists the supported processors. An on-board voltage regulator generates the voltage for the CPU. Both the processor voltage and the operating frequency are automatically adjusted by the motherboard to suit the installed processor.

Processor Type	Processor Speed	CPU bus speed	Cache size	Package
Intel Celeron	300 MHz	66 MHz	128kB	PPGA
Intel Celeron	366 MHz	66 MHz	128kB	PPGA
Intel Celeron	433 MHz	66 MHz	128kB	PPGA
Intel Celeron	566 MHz	66 MHz	128kB	FC-PGA
Intel Pentium III	600 MHz	100 MHz	256kB	FC-PGA
Intel Pentium III	700 MHz	100 MHz	256kB	FC-PGA
Intel Pentium III	850 MHz	100 MHz	256kB	FC-PGA

2.2 System Memory

The SF810 motherboard has two DIMM sockets to accept PC100 modules. The sockets may be populated in any order and each can accept either single or double-sided modules. The minimum total memory size is 16MB and the maximum is 512MB. The BIOS automatically configures the motherboard for the correct size, speed and type. See the RadiSys web site at www.radisys.com for a list of memory modules that have been tested with this product.



When using the on-board video controller, the frame buffer is held within system memory and thus less memory is available to the operating system.

Each memory module should meet the following requirements

- Compliance with the Intel PC100 specification
- Inclusion of a serial presence detect (SPD) ROM
- The module type is 3.3V 168-pin unbuffered synchronous DRAM (SDRAM)
- Based on 16Mb, 64Mb or 128Mb devices
- Capacity of between 16MB and 256MB
- 64 bits wide. ECC or parity is not supported

2.3 Chipset

The SF810 motherboard is based around an Intel 810 chipset comprising two parts -

- Graphics and memory controller hub (GMCH). This includes the processor interface, a high-performance 3D graphics controller and the system memory controller.
- I/O controller hub (ICH). This provides all the PCAT-compatible devices and the PCI bus interface. In addition, it integrates USB and SMBus controllers, a dual UltraATA/66 disk controller, an AC97 digital audio controller and power management functions.

In addition, a National Semiconductor NS87200 ISA bridge is used to support ISA devices via the riser and a firmware hub flash ROM contains the system BIOS, setup utility and video BIOS.

2.4 Video

The video controller is integrated within the 810 chipset GMCH and provides the features listed below.

- 2D graphics with full 2D acceleration
- 3D graphics with extensive rendering capabilities
- Hardware motion compensation for software MPEG2 decode
- System memory is used as frame buffer storage
- 15-way D-type for analog RGB output with VESA DDC2B capability
- Optional on-board Silicon Image SII164 PanelLink flat panel video controller
- Optional Vesa DFP connector on rear panel (DDWG DVI is supported via adapter)

The motherboard has two output connectors – a standard analog VGA connector and an optional digital flat panel connector meeting the Vesa DFP specification. Whilst it is possible to connect a monitor to both these connectors at the same time, the displays will be identical since there is only one video controller. The BIOS supports multiple independent displays via PCI (or ISA) video cards.

The Intel 810 chipset supports a wide variety of video modes. The drivers for specific operating systems support a subset of these modes. The table below lists the video modes supported by the Windows and Linux drivers.

Resolution	Color Depth (bpp) **	Windows 2D Refresh Rates (Hz)	Windows 3D Refresh Rates (Hz)	Linux 2D Refresh Rates (Hz)	Flat Panel Refresh Rates (Hz)
640 x 480	8, 24	60, 70, 72, 75, 85		60, 75, 85	60 *
	16	60, 70, 72, 75, 85	60, 70, 72, 75, 85	60, 75, 85	60 *
720 x 480	8, 24	75, 85			60 *
	16	75, 85	75, 85		60 *
720 x 576	8, 24	60, 75, 85			60 *
	16	60, 75, 85	75, 85		60 *
800 x 600	8, 24	60, 70, 72, 75, 85		60, 75, 85	60 *
	16	60, 70, 72, 75, 85	60, 70, 72, 75, 85	60, 75, 85	60 *
1024 x 768	8, 24	60, 70, 72, 75, 85		60, 75, 85	60
	16	60, 70, 72, 75, 85	60, 70, 75, 85	60, 75, 85	60
1152 x 864	8, 16, 24	60, 70, 72, 75, 85		60, 75, 85	
1280 x 960	8, 16	60, 75, 85			
1280 x 1024	8, 16	60, 70, 72, 75, 85		60, 75, 85	
	24	60, 70, 75, 85		60, 75, 85	
1600 x 1200	8	60, 70, 72, 75, 85		60, 75, 85	
	16			60, 75, 85	

* These resolutions are supported via centering
** Bits per pixel. 8bpp=256 colors, 16bpp=64k colors, 24bpp=16M colors

2.4.1 System Memory Allocation

The video controller does not have its own memory and makes use of system memory for all its needs. This must be taken into account when the amount of system memory is chosen. When the on-board video controller is not used, it should be disabled completely via BIOS Setup to prevent system memory being allocated to the controller.

The motherboard BIOS allocates 1MB of system memory to the video controller to support legacy VGA graphics. The amount of system memory reported by the BIOS will reflect this reduction when the on-board video controller is enabled. Once the operating system loads, the video drivers allocate further system memory dependant on availability as described in the table below for Intel PV 4.x video drivers. Systems using Windows NT 4.0, Windows 2000 or those that require 16M colors at a resolution greater than 1024 x 768 must have at least 64MB of system memory.

Total Allocation of System Memory for On-board Video (including 1MB legacy support)			
	Total System Memory Size		
Operating System	**32MB**	**64MB**	**128MB or greater**
Windows 98	7MB	11MB	11MB
Windows NT 4.0	Not valid	10MB	10MB
Windows 2000	Not valid	10MB	11MB

2.5 Audio

The chipset ICH contains a digital audio controller that is supported on the motherboard by an Analog Devices AD1881A audio CODEC. The motherboard has an on-board ATAPI CD-ROM audio line-input connector and also supports the NLX supplemental connector audio interface. The rear panel has two 3.5mm audio jacks for stereo Line output (driven by an amplifier and suitable for driving headphones) and a monaural microphone input with phantom power suitable for electret microphones.

2.6 Network

The SF810 supports an optional 10/100 Ethernet controller based around the Intel GD82559ER. An RJ45 connector located on the rear panel integrates two LED indicators to provide link status information. The list below describes the features provided.

- IEEE 802.3 10Base-T and 100Base-TX compatible
- 32-bit bus-mastering PCI device
- Jumper-less configuration
- RJ45 with two integral LEDs showing line activity, link integrity and line speed

The operation of the two indicators is described in the table below.

LED color	**LED state**	**Indicates**
Green	Off	10Mbps link speed
	On	100Mbps link speed
Yellow	Off	No link is established
	Steady on	Link is established but there is no communication activity
	Blinking	Link is established and communication activity is detected

2.7 IDE Drives

Two independent bus-mastering IDE interfaces are provided via connectors on the riser, each supporting ATA modes up to UltraATA/66. The following drive types are supported.

- ATA hard disks up to UltraATA/66 speeds
- ATAPI devices such as CD-ROMs
- LS120 drives

The BIOS supports logical block addressing (LBA) and extended CHS translation modes for hard disks. When booting from LS120 drives, the correct mode (floppy or hard disk) must be chosen in Setup. The BIOS supports both automatic and manual determination of ATA cable type (80 - or 40-pin) to support UltraATA/66 drives.

2.8 Diskette Drives

Two floppy drives are supported via connectors on the riser. The drives should be 2- or 3-mode 3.5-inch devices supporting 720kB, 1.2MB or 1.44MB formats. The controller is located at I/O addresses 3F0-3F7h and uses IRQ6.

2.9 Standard PC I/O

The standard PC I/O functions serial ports, parallel ports, keyboard and mouse ports and diskette drive controller are provided via a National Semiconductor NS87366 Super I/O device attached to the low pin count (LPC) bus from the chipset ICH. In addition, this device provides system monitoring and fan control functions and general-purpose I/O lines.

2.9.1 Serial Ports

The SF810 motherboard supports two 16C550-compatible serial ports that can operate at speeds of up to 115.2kbps. Serial port 1 is located on the rear panel whilst serial port 2 is via a header. Each port can be assigned as COM1 through COM4 via the BIOS Setup utility:-

- I/O address 3F8-3FFh, IRQ4
- I/O address 2F8-2FFh, IRQ3
- I/O address 3E8-3EFh, IRQ4
- I/O address 2E8-2EFh, IRQ3

2.9.2 Parallel Port

The SF810 has a 25 way female D-sub parallel port connector located on the rear panel. It supports the following operating modes, configured via the BIOS Setup utility.

- Standard PC-compatible parallel port
- Bi-directional parallel port
- EPP mode
- ECP mode

The I/O locations can be assigned as follows.

- I/O address 3BC-3BEh & 7BC-7BEh, IRQ7
- I/O address 378-37Fh & 778-77Fh, IRQ5 or IRQ7
- I/O address 278-27Fh & 678-67Fh, IRQ5 or IRQ7

2.9.3 Infra-red Support

The SF810 motherboard supports an IrDA compliant infra-red interface via the riser. An IR transceiver must be added such as the Hewlett Packard HSDL-3201 or the HSDL-3610 device. The IR port shares the serial port 2 channel and thus the two ports cannot be used simultaneously. A transfer rate of up to 115kbps is supported.

2.9.4 Keyboard and Mouse Ports

Two PS/2 style keyboard and mouse ports are provided on the rear panel. The two ports are interchangeable with the motherboard automatically detecting which peripheral is attached to which port. Both ports provide a resettable fuse protected +5V supply to the peripheral.

The keyboard controller is functionally equivalent to the 8042 standard and is located at I/O addresses 60-64h and uses IRQ1. The mouse shares the same controller and uses IRQ12.

2.10 USB Ports

Two USB 1.1 compliant ports are provided. Normally, both are routed to the stacked USB connector on the rear panel but channel 1 can be re-routed to the riser channel 1/3 via the jumpers (see the configuration section of this document). Both ports provide a resettable fuse protected +5V supply to the peripheral.

The BIOS supports the use of a USB keyboard and/or mouse in lieu of a PS/2 device via the BIOS customization tools (the feature is disabled by default). This USB legacy support provides emulation of standard keyboards and/or mice and since it causes performance degradation should be enabled only when the operating system being used also supports USB (the emulation is automatically disabled once the operating system is running).

2.11 General Purpose I/O Lines

In order to support products that require a small number of internal input or output lines (such as switches or LED indicators), the SF810 provides access to 8 general-purpose lines via a 12-pin header. Each line can be programmed independently as an input or an output. The signals are provided by the National Semiconductor NS87366 Super I/O device. It is the responsibility of the customer to provide suitable software to control these lines.

2.12 CMOS RAM & RTC

The chipset integrates a Motorola MC146818A compatible real-time clock (RTC) and 256 bytes of CMOS RAM that is used by the BIOS to store configuration information. A replaceable primary lithium coin cell or, optionally, a Super Cap backs up both the RTC and the CMOS RAM. The former provides for approximately 5 years of unpowered backup. The SuperCap provides for greater than 1-hour life and eliminates cell replacement as a reason for scheduled maintenance.

The lithium coin cell is a CR2032 device.

The RTC includes a century byte and is supported by the BIOS to provide year 2000 compliance.

When the +5V standby power is applied to the motherboard, the RTC and the CMOS RAM are powered from that rather than the lithium cell or the optional SuperCap.

2.13 Expansion Cards

Expansion cards are supported via the NLX riser.

PCI Slots
A maximum of 5 bus-master PCI 2.2 compliant slots are supported although risers with a high PCI slot count must be carefully validated to ensure signal compliance with the PCI specification. In order to fully meet the PCI 2.2 specification, the 3VAux-power supply rail must be provided by the riser.

ISA Slots
The motherboard supports ISA slots on the riser via the NS87200 ISA bridge. A maximum of 5 slots is typical although additional slots can be supported with suitable buffering on the riser. Suitable signal termination may be required on risers with slots positioned far from the NLX connector.



Support for ISA card option ROMs is possible only if certain BIOS features are disabled – see the BIOS section for details.

AMR Support
The NLX 1.8 specification supports up to 4 audio CODECs. The SF810 motherboard supports two channels, one of which (the primary channel) is used by the on-board AC97 CODEC.

2.14 System management

The SF810 motherboard includes hardware system management functions. They monitor system voltages, motherboard and CPU temperatures, fan speed and control system fans. The following sections describe this in more detail. The BIOS Setup utility can be used to display the status of the system monitors.

2.14.1 Voltage Monitoring

The table below details the motherboard voltage rails monitored and their usage.

Voltage Rail	Usage on Motherboard
+12V	Serial ports, processor voltage generation, audio headphone amplifier, fans.
+5.0V	Processor voltage generation, internal logic, keyboard, mouse, USB and video ports.
+3.3V	Chipset ICH, firmware hub, ISA bridge, audio CODEC, SIO, clock generator, flat panel controller.
+2.5V	Processor signaling.
+1.8V	Chipset GMCH, chipset ICH.
+1.5V	Processor bus termination.
-12V	Serial ports.
VCPU	Processor core voltage.
+3.3V Standby	Primary standby voltage to systems that control motherboard wake-up, System memory DIMMs, Ethernet controller.
VBAT*	This rail is used to power the RTC and the CMOS RAM.

* The VBAT supply is generated from the +3.3V standby supply when available in order to preserve the life of the lithium cell. This means, however, that the voltage read via the monitor is that of the standby rail and not of the lithium cell itself.

A regulator on the motherboard generates the processor operating voltage with each processor selecting the correct voltage automatically. The table below indicates the correct operating voltage for the different processors.

Processor Type	Processor Speed	Operating Voltage
Intel Celeron	300 MHz	2.00V
Intel Celeron	366 MHz	2.00V
Intel Celeron	433 MHz	2.00V
Intel Celeron	566 MHz	1.50V
Intel Pentium III	600 MHz	1.65V
Intel Pentium III	700 MHz	1.65V
Intel Pentium III	850 MHz	1.65V

2.14.2 Temperature Monitoring

There are two temperature sensors on the motherboard. The first measures the motherboard temperature. Since the sensor is contained within the SIO, this will be a localized reading dominated by the motherboard surface temperature around the SIO component.

The second temperature sensor is located on the processor die and thus accurately measures the local die temperature. Since the local die temperature fluctuates rapidly with activity, the controller within the SIO filters the signal to produce an average temperature.

2.14.3 Fan Monitoring

The motherboard includes three fan monitors that check for the fan tachometer signal to determine that rotation speed. Fan speed limits can be set to cause an alarm in the event that the fan rotates more slowly than the limit. Using this method, early warning of a failing fan can be generated.

Note that when a fan is temperature controlled, the fan monitoring alarms for that fan should not be used since the speed is determined by the temperature control mechanism and the fan will sometimes be intentionally slowed or stopped.

The three NLX fan tachometer signals are assigned to fans as follows.

	Usage by motherboard	Typical usage on NLX riser
FAN_TACH1		System Fan
FAN_TACH2		PSU Fan*
FAN_TACH3	CPU Fansink	

* This signal is carried on the extension power connector and is often omitted.

2.14.4 Fan Control

The motherboard supports two controllable fans – the CPU fansink and the system fan. The logic for the CPU fansink implements variable speed control whereas the system fan is either on or off.

2.14.5 Tamper Detection

The motherboard supports tamper detection security that operates via the chassis tamper switch connected to the riser (TAMP_DET# signal). When the motherboard detects this signal low the BIOS can be configured to display a warning message or to require a password at the next boot.

Since the logic is powered by the lithium cell, the tamper detection continues to operate even if the board is unpowered.

2.15 Power management

The SF810 motherboard implements a number of power management features with software support for APM and ACPI. Where an operating system does not support ACPI, the motherboard defaults to using APM. An APM driver is required by the operating system in order to take advantage of the APM power management features.

2.15.1 ACPI Power States

An ACPI-aware operating system directs the power management of the motherboard – causing the various devices within the system to change power state as appropriate. The table below describes the ACPI power states available using the SF810 motherboard.

Global State	Sleep State	Device State	Description
G0	S0	C0, D0	Fully operational, all devices powered.
G1 Sleeping	S1 CPU stopped	C1, D1, D2, D3	Sleep state. CPU is stopped but all devices are powered.
G1 Sleeping	S4 Suspend to disk	D3	All devices are unpowered except wake-up logic. Memory and system context saved to disk.
G2/S5	S5 Soft Off	D3	All devices are unpowered. Memory contents and context are lost. No wake-up possible.
G3 Mechanical Off	No power	No power	System is unpowered with no standby rails. No wake-up is possible

2.15.2 ACPI Wake-up Support

The table below indicates which events can cause an ACPI wake-up and from which sleep states.

Event	Sleep State	Comment
Power switch	S1, S4, S5	
RTC alarm	S1, S4	
PS/2 keyboard or mouse	S1	Ports are unpowered in S4, S5
USB device (any port)	S1	Ports are unpowered in S4, S5
On-board LAN (82559ER)	S1, S4	Restricted wake-up support. Magic Packet is NOT supported.
IR device	S1	
PCI PME signal	S1, S4	

2.16 Indicators

The NLX riser supports two LED indicators – power and message. The SF810 motherboard drives these as described in the table below. The table assumes that the riser is compatible with the NLX reference riser and that if a dual color LED is used it is green/yellow. Some NLX risers implement the message waiting indication by blinking the power LED. If not, the BIOS can be configured to blink the message LED directly, via the customization process.

LED	LED state	Indicates
Power (single color)	Off	The motherboard is powered down or in one of the ACPI sleep states (including S1).
	On	The motherboard is fully powered up (S0).
Power (dual color)	Off	The motherboard is powered down or in ACPI sleep states S4 or S5 (no +5V supply available).
	Green	The motherboard is fully powered up (S0).
	Yellow	The motherboard is in sleep state S1.
Message	Off	No message waiting (as determined by ACPI TAPI)
	On	Message waiting (as determined by ACPI TAPI)

2.17 BIOS

The system BIOS is held within a flash ROM device called the firmware hub (FWH). The device is a 4Mbit part that contains the following code.

- System BIOS, POST and configuration (Setup) utility
- Video BIOS
- System management data for DMI/SMBIOS
- Product configuration information including boot logo and CMOS defaults
- Processor microcode updates
- Customizations

The code is built from a number of software and data modules that can be customized and assembled with a software tool that can be provided by RadiSys. Software to support BIOS updates and crisis recovery is also available - see the OEM products Download Library on www.radisys.com for BIOS updates and support software.

The configuration of the motherboard is generally automatic with intervention possible via the built-in BIOS Setup utility. The operation and feature set are described in the BIOS chapter of this document.

2.18 Operating Systems Support

The following operating systems are validated by RadiSys with the SF810 motherboard. Contact RadiSys for information on the support of other operating systems. See the OEM products Download Library on www.radisys.com for device drivers.

- Microsoft MS-DOS 6.2
- Microsoft Windows 95, 98, NT 4.0, 2000

3 Specifications

3.1 Regulatory EMC Compliance

The table below lists the EMC regulations the SF810 motherboard complies with when correctly installed.

Regulation
FCC Class B (Title 47 of Code of Federal Regulations, parts 2 & 15, subpart B)
EN55022:1998 Class B
EN55024:1998

3.2 Regulatory Safety Compliance

The table below lists the safety regulations the SF810 motherboard complies with when correctly installed.

Regulation
UL1950/CSA950 3rd edition
IEC 950 2nd edition, 1991 with amendments 1, 2, 3, 4
EN60950 2nd edition, 1992 with amendments 1, 2, 3, 4

3.3 Environmental

Parameter	State	Specification
Temperature*	Operating	0°C to 55°C
(ambient)	Storage	–40 to 85 °C
Humidity		5% to 95% non-condensing
Shock	Packaged	0 to 20lbs: 36 inches free fall, 167 inches/s velocity change
		21 to 40lbs: 30 inches free fall, 152 inches/s velocity change
		41 to 80lbs: 24 inches free fall, 136 inches/s velocity change
		81 to100lbs: 18 inches free fall, 118 inches/s velocity change
	Unpackaged	30 g trapezoidal waveform,170 inches/s velocity change
Vibration	Packaged	10Hz to 40Hz: 0.015g^2Hz
		40Hz to 500Hz: 0.015g^2Hz sloping down to 0.00015g^2Hz
	Unpackaged	5Hz to 20Hz: 0.01g^2Hz sloping up to 0.02g^2Hz
		20Hz to 500Hz: 0.02g^2Hz
Altitude	Operating	To 15000 ft. (4500m)
	Storage	To 40000 ft. (12000m)
ESD	Operating	4kV direct contact, 8kV air



** This is the motherboard specification. Intel Celeron processors have a minimum operating temperature of 5°C. Refer to the relevant Intel processor datasheet for the maximum operating temperature. The user must ensure that the system enclosure provides adequate airflow to ensure the processor temperature is within its operating limits.*

3.4 Industry Compliance

The SF810 motherboard implements the following industry specifications.

Specification	Description	Revision
ACPI	Advanced Configuration and Power Interface Specification	1.0b
APM	Advanced Power Management BIOS Specification	1.2
AC'97	Audio CODEC '97 Component Specification	2.1
ATAPI	ATA Packet Interface for CD-ROMs	2.5
NLX	NLX Motherboard Form Factor Specification	1.8
PCI	Peripheral Component Interconnect Local Bus Specification	2.2
	PCI Power Management Interface Specification	1.1
USB	Universal Serial Bus Specification	1.1

3.5 Miscellaneous

Parameter	Conditions	Specification
RTC Clock accuracy	25°C, 3.3V	+/- 25 ppm max.
Audio LINE (headphones) continuous average output power	8Ω load, +5V supply at 5.0V	200mW max
Audio full scale LINE input level	Input impedance 20kΩ typ.	1.0V rms.
Audio full scale MIC input level	Gain set to 0dB	1.0V rms.
	Gain set to 20dB	100mV rms.

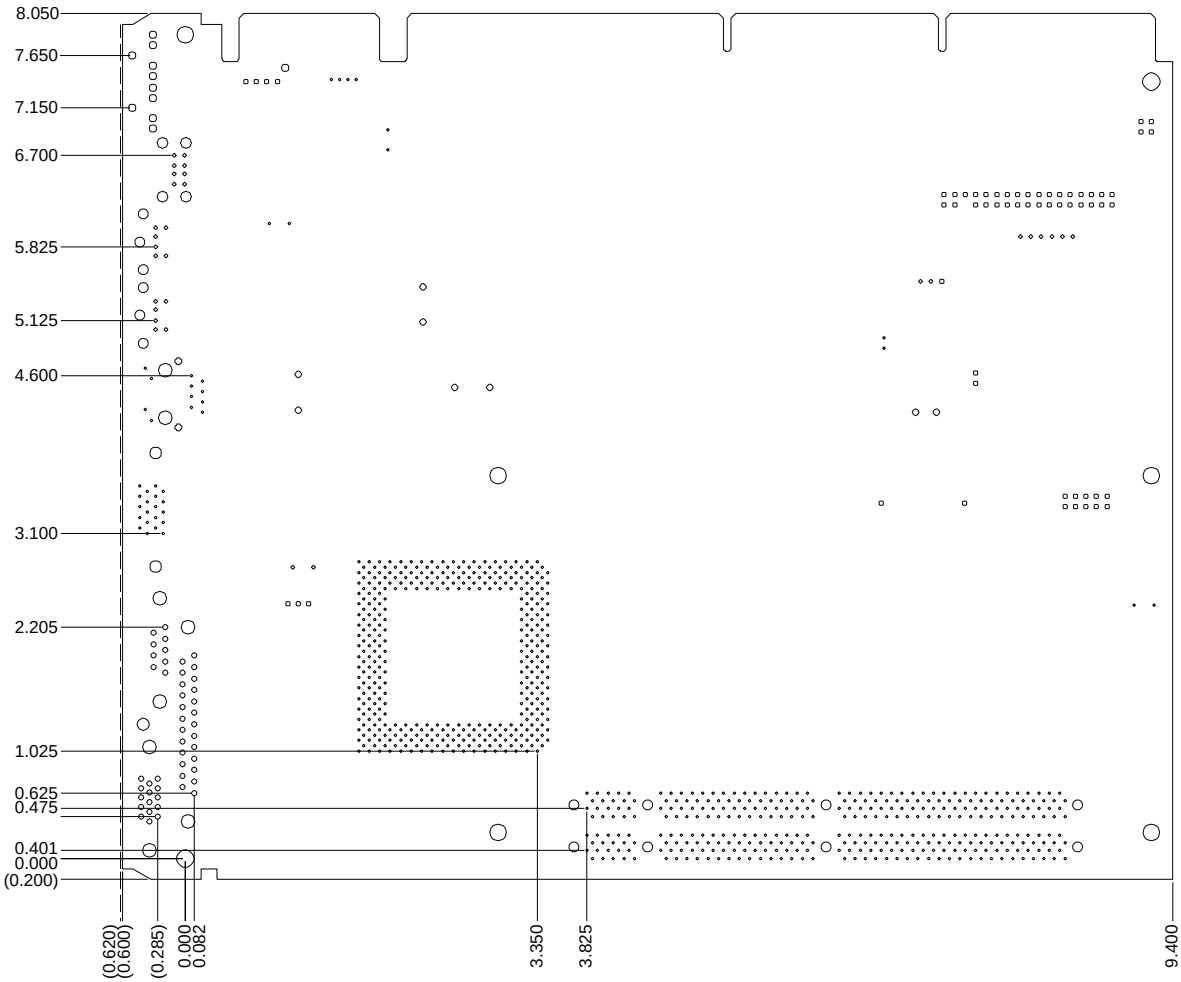
3.6 Mechanical

3.6.1 Motherboard

The SF810 is an NLX 1.8 compliant motherboard measuring 10.0 x 8.25 inches. It is manufactured using a 4-layer PCB with components on the topside only. The screen-printing includes the following.

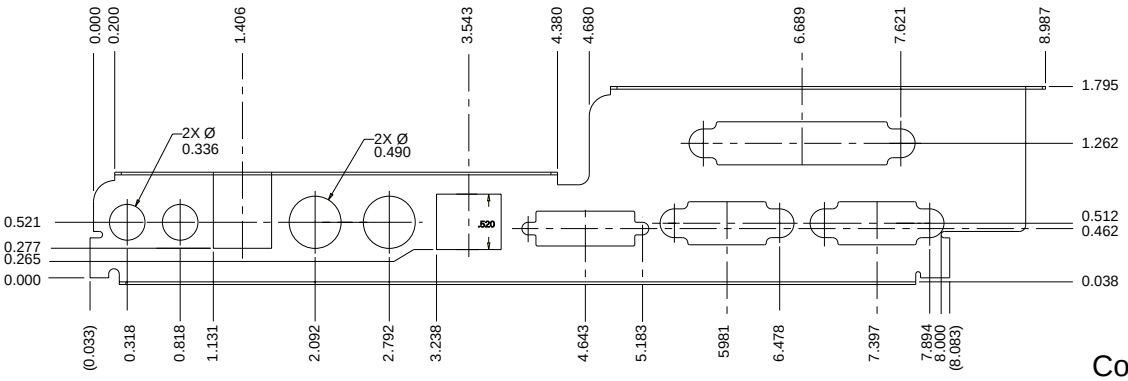
- Product Name, RadiSys part number and RadiSys branding.
- Location for serial number label
- Selected component reference designators

The figure below shows the dimensions of the motherboard and the location of the rear panel connectors (referenced via pin 1) and the location of the processor and memory sockets.

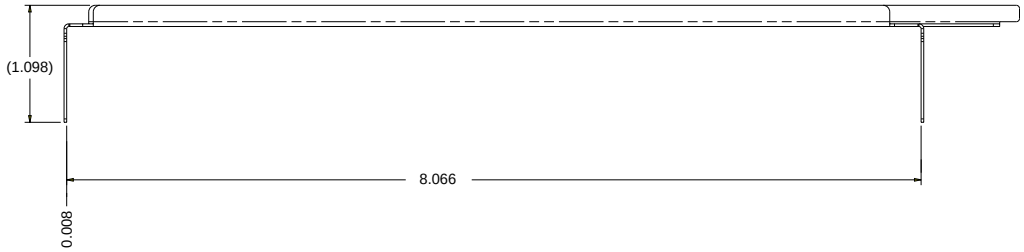


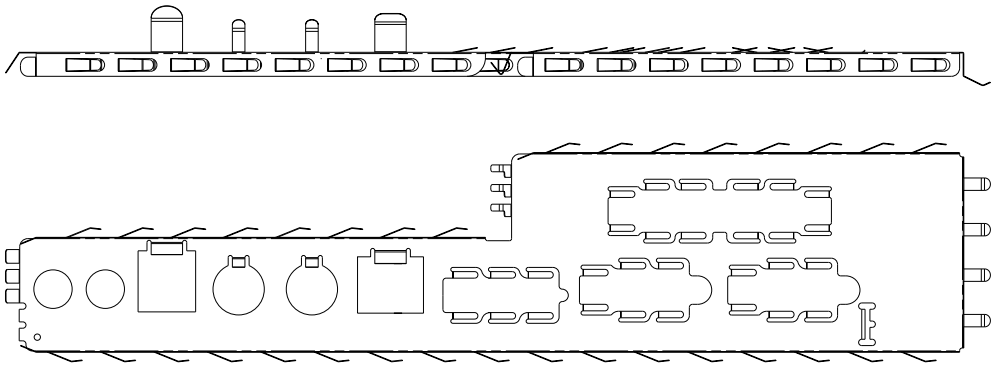
3.6.2 I/O Shield and Cover

An I/O shield for the SF810 when used in a standard NLX chassis with a 9.0-inch aperture is available and is illustrated below. The shield is in two parts – the shield itself, which is manufactured to provide flexible fingers that contact the chassis and a cover that fits inside the shield envelope and provides the stiffness. Each motherboard variant has a unique cover but all use an identical shield.



Cover

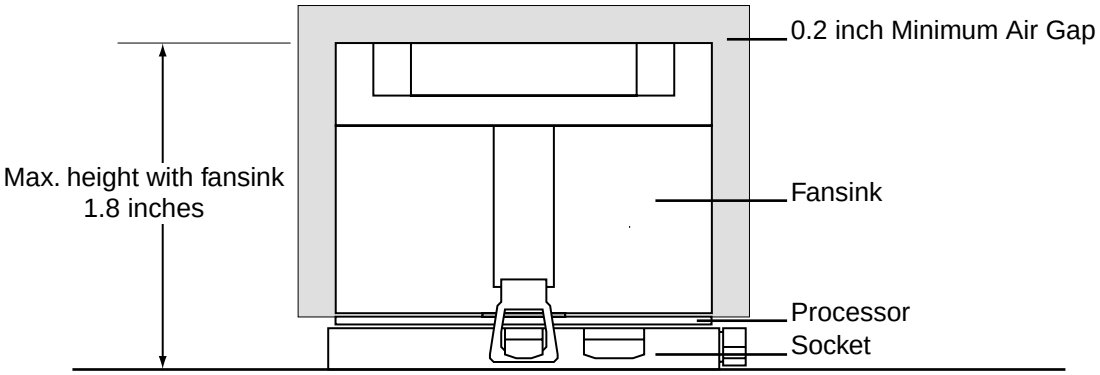




Shield

3.6.3 Fansink

The motherboard can be optionally shipped with a processor fansink, which must have a minimum air space of 0.2 inches around it to function correctly. This is shown in the drawing below.



3.7 Electrical

3.7.1 Motherboard Power Consumption

The motherboard power consumption is highly dependent on the processors, memory and devices attached and also on the software that is running and the power state that the board is in. The figures given in the table below are designed to give the user a guide to the power requirements that should be expected under selected conditions. They should not be interpreted as maximum requirements.

The figures are based on measurements of a real system configured in the following manner.

Processor	Intel Celeron at 433 MHz
Memory	128MB
Drives	Quantum LCT08, CD-ROM, floppy drive (all powered independently)
Video	On-board

	Motherboard Current				
Mode	**+3.3V**	**+5V**	**+12V**	**-12V**	**+5Vsby**
MS-DOS Prompt without power management	1.9A	2.9A	0.32A	60mA	50mA
Windows 2000 desktop idle	1.6A	3.2A	0.35A	60mA	50mA
Windows 2000 standby	1.5A	0.7A	0.25A	60mA	50mA
Off with AC connected and LAN	0	0	0	0	160mA
Stress test maximums*	2.1A	4.7A	0.36A	60mA	50mA

* These results are from a suite of stress tests designed to maximize the power dissipation of the above configuration. Each figure is the worst case seen from any test – they are not maximums that can be measured together.



It is very important that the power supply used can support the required load current on all rails – failure to meet this can cause damage to the power supply or the motherboard. Pay particular attention to the 5V Standby power requirement – the LAN controller (when fitted) is powered from this rail.

3.7.2 General Purpose I/O Lines

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{3.3V}$		10	µA
		$V_{IN} = V_{GND}$		10	µA
V_H	Input Hysteresis		250		mV
V_{OH}	Output High Voltage	I_{OH} = -3mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 6mA		0.4	V

4 Motherboard BIOS

4.1 Configuration

The motherboard BIOS includes a setup utility that can be used to both view and modify the board's configuration. The settings are stored in CMOS RAM with the default settings held in the flash ROM. To start the utility, press the F2 key when prompted. If 'silent-boot' is on (logo displayed) then press the ESC key to show the start-up messages.

The display is divided into four areas.

- The top bar shows the six main menus
- The large left area shows the options
- The large right area displays help text specific to the highlighted option or menu
- The bottom bar shows the action of the active keys

The primary menus are briefly described in the table below. The help text describes each option more fully. Many options have sub-menus.

Menu	Options
Main	Product description including processor and memory fitted.
	Date and time.
	IDE disks found and sub-menus for extra configuration.
Advanced	Start-up display mode (silent-boot etc.).
	Operating system type (ACPI etc.).
	Advanced chipset configuration.
	Processor cache control.
	PCI space configuration.
	I/O devices configuration.
	Advanced hard disk drive options.
Security	Passwords and permissions.
Power	Behavior after AC-reconnect.
	Power savings modes and timers.
Boot	Selects device boot order.
Exit	Save with or without changes.
	Load default settings (from flash ROM).

4.2 Update and Recovery

This section describes how to update the code and data held in the BIOS ROM. The process should be undertaken with care and must not be interrupted. A recovery mechanism is also described that enables a corrupted BIOS ROM (as a result of an interrupted update, for example) to be repaired.

Updates are available online from the RadiSys site in the form of a compressed image (ZIP) of a number of files. Using the software contained in the ZIP file, you must first create a flash diskette that is then used for the update or recovery process. Included in the ZIP file is a 'Readme.txt' file that contains information on the update and instructions on how to use it. Always read this document before proceeding as it may contain updates to the descriptions below.

The update process assumes you have a PC that can be used to create an update diskette and that the system to be updated or recovered has a diskette drive attached.



Updating the BIOS is a process that should be undertaken with caution. Always complete the process before powering-down or restarting the motherboard – failure to do this may result in a corrupted BIOS that will require recovery.

4.2.1 Creating a BIOS Update Diskette

Follow the steps below. You need a PC with Microsoft MS-DOS, Windows 95 or Windows 98 and a blank diskette.

1. Obtain the file update ZIP file from the Download Library on the RadiSys web site, www.radisys.com.
2. Unzip the contents to a directory on your hard drive.
3. To create the update diskette, run CRISDISK from the directory created in step 2.
4. Insert a blank diskette into the floppy drive.
5. Follow the steps as directed, using the option to create a disk with full DOS. A copy of MS-DOS 'Format.com' must be available or the diskette must be pre-formatted.

4.2.2 Updating the System BIOS

The system BIOS can be updated from MS-DOS without changing jumpers as described below. It is recommended that you create a recovery diskette (described later) before updating the BIOS. This operation does not affect the customization area in the BIOS.

1. Create an update diskette as described above.
2. Boot the system to be updated into MS-DOS without memory managers or boot from the update diskette.
3. If you did not boot from the update diskette, do the following.
   A. Insert the flash diskette into the floppy drive.
   B. Change the MS-DOS directory to match the floppy drive's directory.
   C. Type UPDATE and press Enter.
4. Choose the 'Update System BIOS Only' option and press Enter. This initiates the update. When it is finished, the following message appears:

   Flash memory has been successfully programmed
   PRESS ANY KEY TO RESTART THE SYSTEM
   If the system does not restart
   TURN THE POWER OFF, THEN ON

5. Turn off the system power and re-boot.

If the update operation fails for any reason (if it was interrupted, for example), and the motherboard will no longer operate, then the BIOS must be recovered.

4.2.3 Creating a BIOS Recovery Diskette

Follow the steps below. You need a PC with Microsoft MS-DOS, Windows 95, Windows 98 or Windows NT and a blank diskette.

1. Obtain the file update ZIP file from the Download Library on the RadiSys web site, www.radisys.com.
2. Unzip the contents to a directory on your hard drive.
3. To create the update diskette, run CRISDISK from the directory created in step 2.
4. Insert a blank diskette into the floppy drive.
5. Follow the steps as directed, using the option to create a disk with MiniDOS.

4.2.4 Recovering the System BIOS

The recovery diskette should be used to recover system BIOS when the motherboard no longer operates. Normally, the motherboard will recognize a corrupted BIOS and will automatically initiate the recovery operation. The process is described below.

1. If the motherboard has recognized a corrupted BIOS it will wait for the recovery diskette to be inserted into the drive. If it has not, remove the operating mode selection jumper to place the board into the recover mode (see Configuration section of this document).
   A. Turn off the power.
   B. Remove any covers to gain access to the jumper.
   C. Remove the jumper from the operating mode selection block
2. Insert the recovery diskette into the floppy drive.
3. Power up the motherboard. You will hear the following audio signals if you have a speaker connected. If you do not have a speaker, wait for approximately 1 minute after all activity has stopped to ensure the operation has completed.

Beep code	Definition
One short beep	BIOS update begins.
One long beep	BIOS update is finished.
Three beeps	This indicates an error.

4. Power down the motherboard.
5. If you removed the operating mode jumper,
   A. Refit the jumper into the normal operating position.
   B. Replace the system cover(s).
6. Power up the motherboard. The recovery process is now complete and the product should boot normally.

4.2.5 Updating the BIOS Customization Area

The BIOS customization area can be updated with the system BIOS by following the system BIOS update process described above but choosing the 'Update System BIOS and Customization Data' option from the menu when running UPDATE. If you do this using the standard update files contained in the downloaded ZIP, the customizations will be set to RadiSys standard defaults. To update with customer-specific data you must first customize the update disk as described in the BIOS Customization section of this document.

4.2.6 Updating the Flash Bootblock

There is an area of the BIOS ROM, the bootblock, which is normally not updated. It contains code to perform the recovery process and data that identifies the motherboard. It is possible to update this area using an enhanced version of the BIOS update files and software contained in a ZIP file that is available on special request. The update procedure is documented on the 'Readme.txt' file contained within the ZIP file.



Updating the flash bootblock should not normally be attempted. If this process is interrupted, the motherboard cannot be recovered and must be returned to RadiSys for repair.

4.3 Customization

There are a number of features of the BIOS that can be customized and the software to accomplish this is contained within the BIOS update ZIP file that can be obtained from the Download Library on the RadiSys web site, www.radisys.com. The 'Readme.txt' file also contained in this ZIP provides updated customization information and should be read before proceeding.

The process involves updating various files on the update disk created as described in the 'Creating a BIOS Update Diskette' section of this document. Once updated, this diskette can be used as described in the 'Updating the BIOS Customization Area' section of this document.

To customize the Quietboot logo, simply replace the 'Logo.bmp' file on the update diskette with a new image with BMP format. The logo should be 16-color and the palette can be chosen at will. Note, however, that the BIOS start-up progress indicator uses two colors, which should be visible against the background.

To customize the processor microcode update selections, replace the 'P6upd.bin' file on the update diskette with a new one. This is formed by concatenating four microcode updates in binary form. They can be obtained from Intel.

The update process will destroy any default CMOS settings that have been saved to the flash ROM using the BIOS Setup utility. If you are updating multiple motherboards and wish each to customize the default CMOS area, use the following process. You must redo this process for each new release of BIOS.

1. Generate all the customizations required.
2. Update the BIOS on one motherboard that will then act as the 'gold' board.
3. Change the CMOS settings on the 'gold' board as required using the BIOS Setup utility.
4. Save the CMOS settings to the flash ROM using the BIOS Setup utility.
5. Run the GETCSR utility contained within the update ZIP file. This generates a file called 'Csr.bin' that you must use to replace the one on the update diskette. Do not use this file with any other BIOS revision.
6. All subsequent motherboards updated with this diskette will have the saved default CMOS settings.

4.4 BIOS Error Indications

Once the motherboard powers-up the BIOS code runs Power-On-Self-Test software to check that the motherboard is operating correctly. During this process, the code writes an 8-bit value to an error port at various code checkpoints. If a fatal error is determined, then the error code indicates the last successful checkpoint reached. The BIOS will attempt to write this code to the display. The error port (I/O location 80h) can be read via “off-the-shelf” Debug cards. The table below lists the checkpoint codes.

There are a number of checkpoints that also generate an audible ‘beep’ code on failure using the standard PC speaker (also routed though the motherboard audio system). The beep codes are made up of up to 4 groups of short beeps and are also listed below.

Once the video is enabled further errors generated during and after POST are sent to the video display as text messages. These messages are always displayed unless the motherboard is configured for silent boot or headless (no keyboard, mouse or display) operation.

BIOS POST Checkpoint Codes			
02h	Verify Real Mode	6Ch	Display shadow message
03h	Disable NMI	6Eh	Display non-disposable segments
04h	Get CPU type	70h	Display error messages
06h	Initialize system hardware	72h	Check for configuration errors
08h	Initialize chipset registers with initial POST values	74h	Test real-time clock
09h	Set in POST flag	76h	Check for keyboard errors
0Ah	Initialize CPU registers	7Ah	Test for key lock on
0Bh	Enable CPU cache	7Ch	Set up hardware interrupts vectors
0Ch	Initialize cache to initial POST values	7Eh	Test coprocessor if present
0Eh	Initialize I/O	80h	Disable onboard I/O ports
0Fh	Initialize local bus IDE	81h	Late device initialization
10h	Initialize Power Management	82h	Detect and install external RS232 ports
11h	Load alternate registers with initial POST values	83h	Configure IDE controller
12h	Restore CR0	84h	Detect and install external parallel ports
13h	Reset PCI BM	85h	Initialize PCI PCC devices
14h	Initialize keyboard controller	86h	Re-initialize onboard I/O ports
16h	BIOS ROM checksum	87h	Configure MCD devices
17h	Pre-size DRAM	88h	Initialize BIOS Data Area
18h	8254 timer initialization	89h	Enable NMI
1Ah	8237 DMA controller initialization	8Ah	Initialize Extended BIOS Data Area
1Ch	Reset Programmable Interrupt Controller	8Bh	Initialize mouse
20h	Test DRAM refresh	8Ch	Initialize floppy controller
22h	Test 8742 Keyboard Controller	8Eh	Execute auto-typing
24h	Set ES segment to register to 4GB	8Fh	Hard disk controller fast pre-initialization

BIOS POST Checkpoint Codes			
26h	Enable A20	90h	Initialize hard disk controller
28h	Autosize DRAM	91h	Initialize local bus hard disk controller
29h	Initialize PMM	92h	Jump to UserPatch2
2Ah	Clear 512KB base RAM	93h	Build MPTABLE for multiprocessor boards
2Ch	Test 512KB base address lines	95h	Install CDROM for boot
2Eh	Test low byte of 512KB base memory	96h	Clear huge ES segment register
2Fh	Pre-System Shadow	97h	Fix up MP table
30h	Test high byte of 512KB base memory	98h	Search for option ROMs (beep for bad checksum)
32h	Test CPU bus-clock frequency	99h	Check for SMART HDD
33h	Initialize PDM	9Ah	Shadow option ROMs
34h	Test CMOS RAM	9Ch	Set up Power Management
35h	Initialize alternate chipset registers	9Dh	Initialize security
36h	Warm start shutdown entry point	9Eh	Enable hardware interrupts
37h	Reinitialize the chipset	9Fh	(Second) HDD fast initialization
38h	Shadow system BIOS ROM	A0h	Set time of day
39h	Reinitialize the cache	A2h	Check keylock
3Ah	Auto-size cache	A4h	Initialize typematic rate
3Ch	Configure advanced chipset registers	A8h	Erase F2 prompt
3Dh	Load alternate registers with CMOS values	AAh	Scan for F2 keystroke
3Eh	Read HW	ACh	Enter SETUP
40h	Set Initial CPU speed	AEh	Clear in-POST flag
42h	Initialize interrupt vectors	B0h	Check for errors
44h	Initialize BIOS interrupts	B2h	POST done--prepare to boot operating system
45h	Core Device Init	B4h	One beep before boot
46h	Check ROM copyright notice	B5h	Quiet boot end/Display MultiBoot menu
48h	Check video configuration against CMOS	B6h	Check password (optional)
49h	Initialize PCI bus and devices	B8h	Clear global descriptor table
4Ah	Initialize all video adapters in system	B9h	Prepare to boot
4Bh	Display QuietBoot™ screen	BAh	DMI
4Ch	Shadow video BIOS ROM	BBh	Initialize BCVS
4Eh	Display copyright notice	BCh	Clear parity checkers
50h	Display CPU type and speed	BDh	Boot Menu
51h	Initialize EISA board	BEh	Clear screen (optional)
52h	Test keyboard	BFh	Check virus and backup reminders
54h	Set key click if enabled	C0h	Try to boot with INT19

BIOS POST Checkpoint Codes			
56h	Enable keyboard	C1h	Initialize PEM
58h	Test for unexpected interrupts	C2h	PEM log
59h	Initialize PDS	C3h	PEM Display
5Ah	Display prompt "Press F2 to enter SETUP"	C4h	PEM sys error initialization
5Bh	CPU cache off	C5h	Dual CMOS
5Ch	Test RAM between 512KB and 640KB	C6h	Docking initialization
5Eh	Base Address	C7h	Late docking initialization
60h	Test extended memory	D0h	Interrupt handler error
62h	Test extended memory address lines	D2h	Unknown interrupt error
64h	Jump to UserPatch1	D4h	Pending interrupt error
66h	Configure advanced cache registers	D6h	Initialize option ROM error
68h	Enable external and CPU caches	D8h	Shutdown error
69h	PM set up SMM	DAh	Extended Block Move
6Ah	Display external cache size	DCh	Shutdown 10 error
6Bh	Load custom defaults		

Checkpoint Code		Beep Code
16h	BIOS ROM checksum	1-2-2-3
20h	Test DRAM refresh	1-3-1-1
22h	Test 8742 Keyboard Controller	1-3-1-3
2Ch	Test 512KB base address lines	1-3-4-1
2Eh	Test low byte of 512KB base memory	1-3-4-3
46h	Check ROM copyright notice	2-1-2-3
58h	Test for unexpected interrupts	2-2-3-1
98h	Search for option ROMs (beep for bad checksum)	1-2
B4h	One beep before boot	1

4.5 ISA Option ROMs

When the motherboard is used in conjunction with an ISA card that includes an option ROM, the USB legacy support must be disabled in order for the ROM to be accessible.

5 Customer Support

RadiSys Online Support at www.radisys.com and includes device drivers, BIOS updates, support software and documentation. See the OEM products Download Library.

RadiSys hotline numbers for the US and Canada are

Support: (800) 438-4769
Service: (800) 256-5917



Online specifications and reference material:

Specification	Description	Location
AC97	Audio CODEC specification	http://developer.intel.com/pc-supp/platform/ac97
ACPI	Advanced Configuration and Power Interface specification	www.teleport.com/~acpi
APM	Advanced Power Management specification	www.microsoft.com/hwdev/busbios/amp_12.htm
DDWG	Digital Display Working Group	www.ddwg.org
Intel 810 Chipset	Intel 810 chipset datasheet	http://developer.intel.com/design/chipsets/810/index.htm
Intel Celeron processor	Intel Celeron processor datasheet	http://developer.intel.com/design/celeron
Intel Pentium III processor	Intel Pentium III processor datasheet	http://developer.intel.com/design/pentiumiii
NLX	NLX form factor specification	www.teleport.com/~ffsupprt/spec/index.htm
PCI	PCI local bus specification	www.pcisig.com
SDRAM DIMMs	PC SDRAM module specification	http://developer.intel.com/design/chipsets/memory
SMBus	System management bus	www.sbs-forum.org/index.htm
USB	Universal Serial Bus specification	www.usb.org/developers
VESA	Video Electronics Standards Association	www.vesa.org

Appendix A Technical Reference

A.1. I/O Map

Address (hex)*	Description
0000 – 000F	DMA controller 1
0020 – 0021	Interrupt controller 1
0040 – 0043	Timer counter
0060 – 0064	Keyboard and mouse controller
0070 – 0071	RTC and CMOS RAM
0080 – 008F	DMA controller page registers (for channels 1 and 2)
0092	PC compatible Port 92 (fast A20 and PIC)
x094	VGA controller POS102 access control
00A0 – 00A1	Interrupt controller 2
00B2 – 00B3	Advanced power management (APM) control registers
00C0 – 00DF	DMA controller 2
00F0	Floating point error control
x102	VGA controller POS102 register
015C – 015D	SIO control registers
0170 – 0177	Secondary IDE controller
01F0 – 01F7	Primary IDE controller
0228 –022F	Parallel port, LPT3
0278 –027F	Parallel port, LPT2
02E8 – 02EF	COM4 serial port
02F8 – 02FF	COM2 serial port
0374 – 0376	Secondary IDE controller
0378 –037F	Parallel port, LPT1
x3B0 – x3BB	VGA controller
x3C0 – x3CF	EGA controller registers
x3D4 – x3DA	CGA controller registers
03F0 – 03F5	Flexible diskette controller
03F6 – 03F7	Primary IDE controller
03E8 – 03EF	COM3 serial port
03F8 – 03FF	COM1 serial port
04D0 – 04D1	Interrupt controller
0778 – 077A	ECP registers (for parallel port)
0CF8 – 0CFF	PCI configuration address and data registers
1000 – 105F	ACPI registers
1060 – 107F	TCO controller

Address (hex)*	Description
1600 – 165F	SIO system management controller and GPIO
FFA0 – FFA7	Primary IDE bus master registers
FFA8 – FFAF	Secondary IDE bus master registers
Dynamically assigned	USB controller (32 locations on 32-byte boundary)
Dynamically assigned	SMBus controller (16 locations on 16-byte boundary)
Dynamically assigned	PCI bridge (4096 locations on a 4096-byte boundary)
Dynamically assigned	LAN controller (32 locations on a 32-byte boundary)

* An ‘x’ prefix for the address indicates that only the low-order 10 address bits are decoded.

A.2. PCI Interrupt Allocation

In order to share PCI interrupts efficiently, the routing of the PCI interrupts INTA - INTD to the motherboard interrupts PCIINT0 – PCIINT3 are rotated for each slot. Thus the PCI card INTA signal for PCI slots 1 to 5 are spread across the four motherboard inputs.



The riser defines the interrupt routing for NLX. The table below describes the default assumptions of the BIOS and follows the recommendations in the NLX 1.8 specification. It is possible to reconfigure these assignments with the BIOS customisation software to tie interrupt rotation to IDSEL.

Device	PCIINT0	PCIINT1	PCIINT2	PCIINT3
PCI Slot 1 (on riser)	INTA	INTB	INTC	INTD
PCI Slot 2 (on riser)	INTD	INTA	INTB	INTC
PCI Slot 3 (on riser)	INTC	INTD	INTA	INTB
PCI Slot 4 (on riser)	INTB	INTC	INTD	INTA
PCI Slot 5 (on riser)	INTA	INTB	INTC	INTD
Ethernet controller	-	-	-	INTA
USB controller	-	-	-	INTD
SMBus controller	-	INTB	-	-
AC97 audio controller	-	INTB	-	-

Example. From the table above, the INTA interrupt from a card plugged into PCI slot 3 of the NLX riser would be routed to the motherboard PCIINT2.

A.3. PCI Device Assignments

Device	IDSEL	Bus Number	Device Number	Function Number
Chipset host bridge		0	0	0
Graphics controller		0	1	0
PCI bridge		0	30	0
LPC bridge		0	31	0
(Includes DMA, timers, PIC, APIC, RTC,				

Device	IDSEL	Bus Number	Device Number	Function Number
power & system management, GPIO)				
IDE controller		0	31	1
USB controller		0	31	2
SMBus controller		0	31	3
AC97 audio controller		0	31	5
AC97 MODEM controller		0	31	6
PCI Slot 1 (on riser)	AD31	1	15	
PCI Slot 2 (on riser)	AD29	1	13	
PCI Slot 3 (on riser)	AD27	1	11	
PCI Slot 4 (on riser)	AD25	1	9	
PCI Slot 5 (on riser)	AD23	1	7	
ISA bridge	AD22	1	6	0
Ethernet controller	AD20	1	4	0

Note that the PCI slots, the ISA bridge and the Ethernet controller are behind a virtual bridge implemented by the chipset ICH. Each device therefore resides on PCI bus 1.

A.4. ISA Interrupt Allocation

Interrupt	Description
IRQ0	System Timer
IRQ1	Keyboard Controller
IRQ2	Cascade interrupt
IRQ3	COM2, COM1 or unassigned
IRQ4	COM1, COM2 or unassigned
IRQ5	Parallel port or unassigned
IRQ6	Floppy
IRQ7	Printer port or unassigned
IRQ8	Real time clock/CMOS RAM
IRQ9	Unassigned
IRQ10	Unassigned
IRQ11	Unassigned
IRQ12	PS/2 mouse or unassigned
IRQ13	Floating point unit
IRQ14	Primary IDE or unassigned
IRQ15	Secondary IDE or unassigned
NMI	ISA IOCHCHK and PCI PERR and SERR signals

A.5. ISA DMA Channel Allocation

DMA Channel	Description
Channel 0	Unassigned 8-bit channel
Channel 1	Unassigned 8-bit channel
Channel 2	Floppy controller or unassigned 8-bit channel
Channel 3	ECP parallel port or unassigned 8-bit channel
Channel 4	Cascade channel
Channel 5	Unassigned 16-bit channel
Channel 6	Unassigned 16-bit channel
Channel 7	Unassigned 16-bit channel

A.6. SMBus Resource Allocation

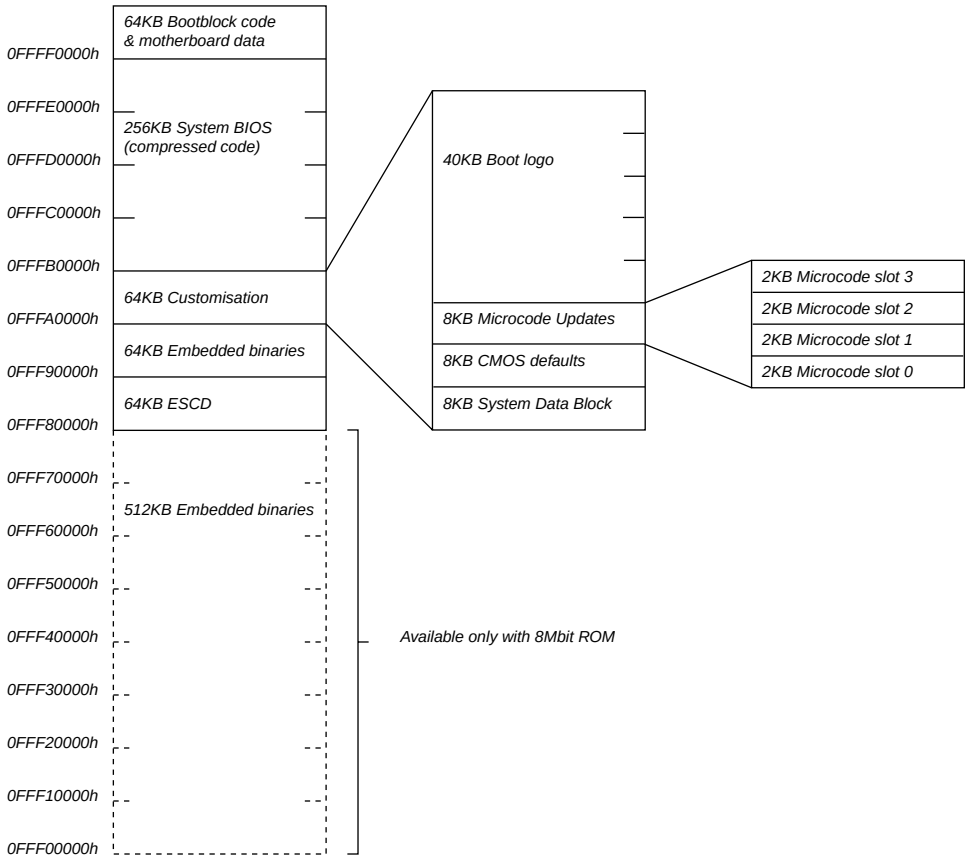
Address	Description
1010 000X	Memory module 1
1010 001X	Memory module 2
1101 001X	Clock synthesizer



The SMBus is routed to the NLX riser and therefore devices attached to this bus via the riser will also appear in the SMBus space.

A.7. BIOS Organization

The BIOS ROM is a 4Mbit device containing eight symmetrical 64KB blocks. The diagram below shows how the ROM is used to store code and control information. The addresses shown refer to the ROM image at the top of the 4GB-address space. Note that the system BIOS segment is compressed in this image. When the BIOS runs, the code is uncompressed in real-time and the resulting code and data image is found at physical address 0E0000h through 0FFFFFh. The diagram includes the map for products that contain an 8Mbit ROM where fitted although this is not fitted as standard.



Appendix B Connector Descriptions

B.1. Connector Part Numbers

The various motherboard connectors are listed in the table below along with the part number of one of the approved vendors. The list is intended to assist in the selection of mating connectors.

Connector	Part Number	Type
Rear audio jacks	Foxconn JA1333L-102	3.5mm stereo jack
Dual rear USB	Foxconn UB1112C-81	
Rear PS/2 keyboard and mouse	Foxconn MH11063-H1	Stacked 6-way mini-DIN
Rear Ethernet	Pulse Engineering J0026/D01B	RJ45 with LEDs and transformer
Rear DFP monitor	Foxconn QB11103-B3	20-way MDR
Rear VGA monitor, parallel port and serial port (1) stack	Foxconn DM11353-BV5	Combination 15-way high-density female, 25-way female and 15-way male D-type
Serial port 2 header	Foxconn HL09051-P5	2 by 10-way shrouded header
CPU Fan	Foxconn HF06031	3-way with locking ramp
GPIO header	Foxconn HL09061-P9	2 by 6-way shrouded header
DIMM sockets	Foxconn AT08413-K8	168-pin, 3V SDRAM
ATAPI CD-ROM LINE input	Foxconn HF11040-P1	
Processor socket	Foxconn PZ37047-S01-S	370-pin ZIF PGA

B.2. NLX Connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	-12V	B1	Not Used	A86	IRQ10	B86	LA21
A2	REQ4#	B2	+12V	A87	IRQ15	B87	LA20
A3	+12V	B3	PCSPKR_L	A88	IRQ12	B88	LA19
A4	GNT4#	B4	+12V	A89	GND	B89	LA18
A5	+3.3V	B5	CLK0	A90	IRQ14	B90	LA17
A6	INTD#	B6	GND	A91	DRQ0	B91	DACK0#
A7	+3.3V	B7	CLK1	A92	MEMR#	B92	DACK5#
A8	INTA#	B8	SERIRQ	A93	MEMW#	B93	SD8
A9	INTB#	B9	INTC#	A94	SD9	B94	DACK6#
A10	CLK2	B10	+3.3V	A95	DRQ5	B95	SD10
A11	+3.3V	B11	CLK3	A96	DRQ6	B96	+5V
A12	RST#	B12	GND	A97	+5V	B97	SD11
A13	GNT0#	B13	GNT3#	A98	SD12	B98	DRQ7
A14	CLK4	B14	+3.3V	A99	DACK7#	B99	SD13

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A15	GND	B15	GNT2#	A100	SD14	B100	SD15
A16	GNT1#	B16	AD31	A101	MASTER#	B101	GND
A17	+3.3V	B17	REQ0#	A102	IDEA_DD8	B102	GND
A18	REQ2#	B18	GND	A103	IDEA_RST#	B103	IDEA_DD7
A19	REQ3#	B19	AD29	A104	IDEA_DD9	B104	IDEA_DD6
A20	AD30	B20	AD28	A105	+5V	B105	IDEA_DD5
A21	GND	B21	AD26	A106	IDEA_DD4	B106	IDEA_DD11
A22	AD25	B22	+3.3V	A107	IDEA_DD10	B107	IDEA_DD12
A23	REQ1#	B23	AD24	A108	IDEA_DD3	B108	GND
A24	AD27	B24	C/BE3#	A109	IDEA_DD13	B109	IDEA_DD14
A25	+3.3V	B25	AD22	A110	IDEA_DD1	B110	IDEA_DD2
A26	AD23	B26	GND	A111	GND	B111	IDEA_DD0
A27	AD20	B27	AD21	A112	IDEA_IOW#	B112	IDEA_DD15
A28	AD18	B28	AD19	A113	IDEA_DRQ	B113	IDEA_IOR#
A29	GND	B29	AD16	A114	IDEA_IORDY	B114	IDEA_CSEL
A30	AD17	B30	+3.3V	A115	IDEA_DAK#	B115	IDEA_IRQ
A31	IRDY#	B31	C/BE2#	A116	Not Used	B116	+5V
A32	DEVSEL#	B32	FRAME#	A117	IDEA_DA2	B117	IDEA_DA1
A33	+3.3V	B33	TRDY#	A118	IDEA_CS0#	B118	IDEA_DA0
A34	STOP#	B34	GND	A119	+5V	B119	IDEA_CS1#
A35	PERR#	B35	Not Used	A120	Not Used	B120	IDEB_DD8
A36	SERR#	B36	LOCK#	A121	IDEB_RST#	B121	IDEB_DD7
A37	GND	B37	Not Used	A122	IDEB_DD9	B122	GND
A38	C/BE1#	B38	+3.3V	A123	IDEB_DD6	B123	IDEB_DD10
A39	AD13	B39	AD15	A124	IDEB_DD5	B124	+5V
A40	AD10	B40	PAR	A125	IDEB_DD11	B125	IDEB_DD4
A41	GND	B41	AD14	A126	IDEB_DD12	B126	IDEB_DD3
A42	C/BE0#	B42	GND	A127	GND	B127	IDEB_DD13
A43	AD0	B43	AD11	A128	IDEB_DD2	B128	IDEB_DD14
A44	AD6	B44	AD12	A129	IDEB_DD15	B129	IDEB_DD1
A45	+3.3V	B45	AD9	A130	IDEB_IOW#	B130	IDEB_DD0
A46	AD5	B46	+3.3V	A131	IDEB_DRQ	B131	IDEB_IOR#
A47	AD1	B47	AD8	A132	IDEB_IORDY	B132	IDEB_CSEL
A48	AD3	B48	AD7	A133	GND	B133	IDEB_IRQ
A49	GND	B49	AD4	A134	IDEB_DAK#	B134	IDEB_DA1
A50	AD2	B50	GND	A135	+3.3VSBY	B135	IDEB_DA2
A51	+5V	B51	PME#	A136	IDEB_DA0	B136	IDEB_CS1#
A52	RSTDRV	B52	+5V	A137	IDEB_CS0#	B137	Not Used
A53	IOCHK#	B53	IRQ9	A138	Not Used	B138	GND

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A54	SD6	B54	DRQ2	A139	+5V	B139	DRATE0
A55	SD7	B55	SD3	A140	Not Used	B140	DS1#
A56	SD4	B56	ZWS#	A141	DENSEL	B141	DS0#
A57	+5V	B57	SD1	A142	MTR0#	B142	DIR#
A58	SD2	B58	AEN	A143	INDEX#	B143	Not Used
A59	SD5	B59	IOCHRDY	A144	MTR1#	B144	GND
A60	SD0	B60	SA18	A145	GND	B145	WDATA#
A61	SMEMW#	B61	SMEMR#	A146	WGATE#	B146	TRK0#
A62	SA19	B62	SA16	A147	STEP#	B147	Not Used
A63	IOW#	B63	IOR#	A148	WP#	B148	RDATA#
A64	SA17	B64	DRQ3	A149	HDSEL#	B149	DSKCHG#
A65	GND	B65	SA15	A150	SDA	B150	GND
A66	DACK3#	B66	GND	A151	SCL	B151	Not Used
A67	SA14	B67	SA13	A152	FANTACH1	B152	Not Used
A68	DACK1#	B68	+5V	A153	FANTACH2	B153	Not Used
A69	DRQ1	B69	REFRESH#	A154	FANTACH3	B154	IRTX
A70	SA12	B70	SA11	A155	FANCTL	B155	IRRX
A71	SYSCLK	B71	SA10	A156	+5V	B156	Not Used
A72	SA9	B72	IRQ7	A157	USB1N	B157	FP_RST#
A73	+5V	B73	IRQ6	A158	USB1P	B158	GND
A74	IRQ5	B74	SA8	A159	USB1_OC#	B159	PWRLED#
A75	SA7	B75	SA6	A160	Not Used	B160	PWROK
A76	IRQ3	B76	DACK2#	A161	Not Used	B161	SOFTON
A77	IRQ4	B77	SA4	A162	Not Used	B162	PS_ON#
A78	SA5	B78	GND	A163	GND	B163	Not Used
A79	TC	B79	SA3	A164	VBAT	B164	Not Used
A80	BALE	B80	SA2	A165	TAMPER#	B165	Not Used
A81	GND	B81	SA1	A166	MSGLED#	B166	Not Used
A82	OSC	B82	SA0	A167	Not Used	B167	Not Used
A83	IOCS16#	B83	SBHE#	A168	Not Used	B168	Not Used
A84	MEMCS16#	B84	LA23	A169	+5VSBY	B169	Not Used
A85	IRQ11	B85	LA22	A170	+3.3VSENSE	B170	Not Used

B.3. NLX Supplemental Connector

Pin	Signal	Pin	Signal
X1	CDIN_LEFT	Y1	CDIN_RIGHT
X2	GND	Y2	CDIN_GND
X3	MIC_IN	Y3	+5VA
X4	LINEO_LEFT	Y4	LINEO_RIGHT
X5	FPSPKR_EN	Y5	Not Used
X6	Not Used	Y6	Not Used
X7	GND	Y7	AC97_RST#
X8	Not Used	Y8	AC97_SDIN0
X9	AC97_SDIN1	Y9	GND
X10	Not Used	Y10	AC97_SDOUT
X11	Not Used	Y11	AC97_SYNC
X12	GND	Y12	AC97_BITCLK
X13	MODEM_MIC	Y13	MODEM_SPKR

B.4. DFP Monitor

Pin	Signal	Pin	Signal
1	TX1+	11	TX2+
2	TX1-	12	TX2-
3	SHLD1	13	SHLD2
4	SHLDC	14	SHLD0
5	TXC+	15	TX0+
6	TXC-	16	TX0-
7	GND	17	Not Used
8	+5V	18	HPD
9	Not Used	19	DDC_DAT
10	Not Used	20	DDC_CLK

B.5. Serial Port 1

Pin	Signal	Pin	Signal
1	DCD	6	DSR
2	RxD	7	RTS
3	TxD	8	CTS
4	DTR	9	RING
5	GND		

B.6. VGA Monitor

Pin	Signal	Pin	Signal
1	RED	9	+5V
2	GREEN	10	GND
3	BLUE	11	RESERVED
4	RESERVED	12	SDA
5	GND	13	HSYNC
6	RED RTN	14	VSYNC
7	GREEN RTN	15	SCL
8	BLUE RTN		

B.7. Serial Port 2

Pin	Signal	Pin	Signal
1	DCD	2	DSR
3	RxD	4	RTS
5	TxD	6	CTS
7	DTR	8	RING
9	GND	10	KEY

B.8. Parallel Port

Pin	Signal	Pin	Signal
1	STB#	14	AFD#
2	DB0	15	ERR#
3	DB1	16	INIT#
4	DB2	17	SLIN#
5	DB3	18	GND
6	DB4	19	GND
7	DB5	20	GND
8	DB6	21	GND
9	DB7	22	GND
10	ACK#	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT		

B.9. General Purpose I/O

Pin	Signal	Pin	Signal
1	GPIO20	2	GPIO21
3	GPIO22	4	GPIO23
5	GPIO24	6	GPIO25
7	GPIO26	8	GPIO27
9	KEY	10	GND
11	+5V	12	+3.3V

B.10. USB Ports

Pin	Signal
1	+5V
2	DATA-
3	DATA+
4	GND

B.11. PS/2 Keyboard

Pin	Signal	Pin	Signal
1	DATA	4	+5V
2	Not Used	5	CLOCK
3	GND	6	Not Used

B.12. PS/2 Mouse

Pin	Signal	Pin	Signal
1	DATA	4	+5V
2	Not Used	5	CLOCK
3	GND	6	Not Used

B.13. ATAPI CD-ROM

Pin	Signal
1	LEFT
2	GND
3	GND
4	RIGHT

B.14. Processor Fan

Pin	Signal
1	GND
2	POWER
3	TACH#

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