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SPIRIT™-6040 Quad Reference Guide

www.radisys.com

World Headquarters
5445 NE Dawson Creek Drive • Hillsboro, OR 97124 USA
Phone: 503-615-1100 • Fax: 503-615-1121
Toll-Free: 800-950-0044

International Headquarters
Gebouw Flevopoort • Televisieweg 1A
NL-1322 AC • Almere, The Netherlands
Phone: 31 36 5365595 • Fax: 31 36 5365620

07-1036-01
May 2000

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Before you begin

This guide describes SP6040 (SPIRIT™-6040 Quad) module, a highly integrated, intelligent I/O subsystem designed for use in 32-bit CompactPCI telecom applications.

This document assumes that you have some familiarity with CompactPCI and H.110 Time Division Multiplex bus architectures. It is also assumes that you are familiar with the *CompactPCI Hot Swap Specification* and *CompactPCI Computer Telephony Specification*.

About this guide

Guide contents

Chapter		Description
1	Overview	Provides an introduction to the SP6040 module, a brief description of the features provided, and tables of specifications.
2	Installation	Explains how to install the SP6040 in a CompactPCI chassis and installing a Windows† NT driver.
3	Theory of operation	Describes how the components of the SP6040 module operates to provide an Intelligent I/O subsystem for Telecom applications.

Appendix		Description
A	Device initialization and memory maps	Maps the addresses used by the i960†RD (IOP) for I/O on its Local and Primary PCI bus.
B	Connectors, headers, and jumpers	Details the location, function, and pin-outs of the connectors and configuration jumpers used on the SP6040.
C	Diagnostics and monitors	Describes the POST and Extended Diagnostics available and the utilities supplied for integrating application code into the SP6040.
D	PMC modules	Describes how to install and disconnect an optional PMC module.
E	Board support package	Describes how to install and operate components in the Board Support Package.

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Notational conventions

This manual uses the following conventions:

- `Screen text and syntax strings appear in this font.`
- All numbers are decimal unless otherwise stated.
- Bit 0 is the low-order bit. If a bit is set to 1, the associated description is true unless otherwise stated.


Notes indicate important information about the product.


Tips indicate alternate techniques or procedures that you can use to save time or better understand the product.


The globe indicates a World Wide Web address.


Cautions indicate situations that may result in damage to data or the hardware.

This includes situations that *may* cause damage to hardware via electro-static discharge (ESD).


Warnings indicate situations that may result in physical harm to you or the hardware.

Where to get more information

About the SP6040

You can find out more about SP6040 from these sources:

- **Readme files**: Lists features and issues that arose too late to include in other documentation.
- **World Wide Web**: RadiSys maintains an active site on the World Wide Web. The site contains current information about the company and locations of sales offices, new and existing products, contacts for sales, service, and technical support information. You can also send e-mail to RadiSys using the web site.

  
  When sending e-mail for technical support, please include information about both the hardware and software, plus a detailed description of the problem, including how to reproduce it.

  
  To access the RadiSys web site, enter this URL in your web browser:
  `http://www.radisys.com`

  Requests for sales, service, and technical support information receive prompt response.
- **Other**: If you purchased your RadiSys product from a third-party vendor, you can contact that vendor for service and support.

About related products

TASK-6000

TASK-6000 software is a tool set that provides a framework for composing, executing and dynamically configuring optimized real-time TMS320C62x DSP applications. The Voice

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Gateway Platform (VGP), available from RadiSys, has been used as the reference hardware platform.

For detailed information about TASK-6000 products, see the following publications:

TASK-6000 User's Manual, (07-0992-xx)

TASK-6000 Installation Guide, (07-1000-xx)

Other references

Enterprise Computer Telephony Forum

ECTF H.110, Revision 1.0, Hardware Compatibility Specification: CT Bus, January 26, 1998.

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1 Overview

The SPIRIT™-6040 Quad (SP6040) is a highly integrated, single-slot, intelligent I/O subsystem designed for use in 32-bit CompactPCI (cPCI) telecom applications.

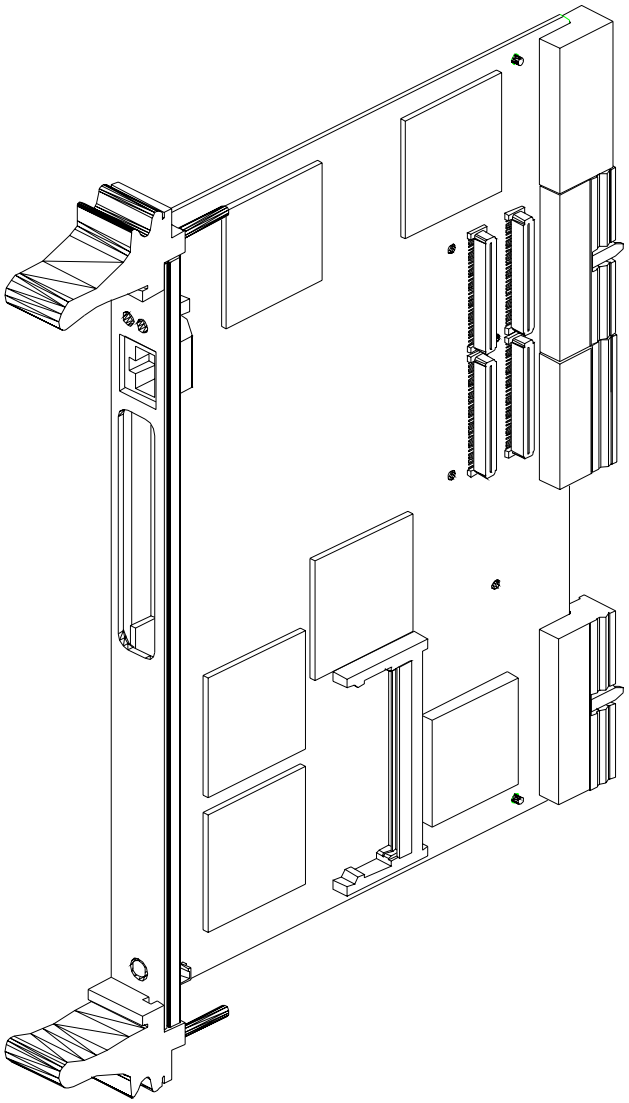


Figure 1-1. The SPIRIT™-6040 Quad (SP6040)

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A member of the SPIRIT-6000 family, the SP6040 includes the following features:

- Four TMS320C6201 Digital Signal Processors (C6201), that provide up to 1600 MIPS.
- A hot-swappable, 32-bit CompactPCI interface on the J1 CompactPCI connector[1].
- A DEC/Intel 21554 PCI-PCI bridge. The 21554 PCI-PCI Bridge serves as the SP6040's CompactPCI interface and provides address translation between the CompactPCI host and on-board PCI devices.
- An Intel i960RD that serves as I/O processor (IOP). The i960RD (66 MHz core) serves as the IOP, with 33MHz local and PCI bus interfaces.
- A hot-swappable, ECTF H.110 compliant, TDM bus interface on the J4 CompactPCI connector[2].
- H.110 TDM Bus Interface and Time Slot Interchanger (Lucent T8105 TDM Switch). This device provides high-performance routing of telecom data between the DSP, the option module connector, and the H.110 TDM bus.
- An audio monitor, accessible via an on-board header. You can configure this resource to connect either directly to a C6201 serial port or to the H.110 TDM Switch, to allow drop/insert capability for any selected TDM slot.
- A PMC socket[3], with additional pin-outs (via PMC J13/J14) that support optional RadiSys Dual/Quad E1/T1/LAN-HDLC or PMC-4(2)T1/E1 LAN option modules.

The SP6040 is available in these configurations:

Table 1-1. SP6040 product configurations

Product code	Options	Description
SPIRIT-6040	Default configuration	Standard product for the telecom market
SP-6040-CPCI-CB	Default configuration without the CompactPCI J3 connector	CompactPCI J3 connector removed to avoid conflict with backplane signalling

Mechanical information

The SP6040 occupies a single 6U CompactPCI slot. 6U boards are 233.35 mm (6U) x 160.0 mm (9.19" x 6.29"). The sum of the component height and warpage is less than or equal to 13.71 mm (0.54") from the component side of an ideal (no warpage) board, and 1.52 mm (0.060") from the solder side. The SP6040 occupies a single CompactPCI option slot with or without a compliant PCI Mezzanine card mounted on the module. The exact mechanical requirements are specified in the *CompactPCI Specification*.

1. *CompactPCI Specification*
2. *ECTF H.110, Revision 1.0*
3. *IEEE P1386.1/Draft 2.0 Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC*, *IEEE P1386/Draft 2.0, Draft Standards for a Common Mezzanine Card Family: CMC*

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Specifications

The SP6040 has been tested to meet the specifications listed in Table 1-2 and Table 1-3. Contact RadiSys for associated agency compliance Listings, Declarations and/or Test reports.

Table 1-2. SP6040 environmental specifications

Characteristic	State	Value
Temperature	Operating	Required airflow across the module is shown for a range of inlet air temperatures, as indicated in Figure 1-2, at point of entry of forced air. These values are derated 2°C per 1000 ft (300 m) over 6600 ft (2000m). 2°C per hour maximum excursion gradient.
	Storage	–40°C to 85°C 5°C per hour maximum excursion gradient.
Humidity	Operating/storage	5% to 95% noncondensing.
Altitude	Operating	0 to 10,000 feet (3000 m).
	Storage	0 to 40,000 feet (12.000 m).
Airflow	Operating	See Figure 1-2.
Vibration	Operating	2.5 g acceleration over 5–300 Hz sine wave, 1 oct/min. sine sweep.
	Storage	5 g acceleration over 5–2,000 Hz sine wave, 1 oct/min. sine sweep.
Shock	Operating	30 g, 11 ms duration, half-sine shock pulse.
	Storage	50 g, 11 ms duration, half-sine shock pulse.

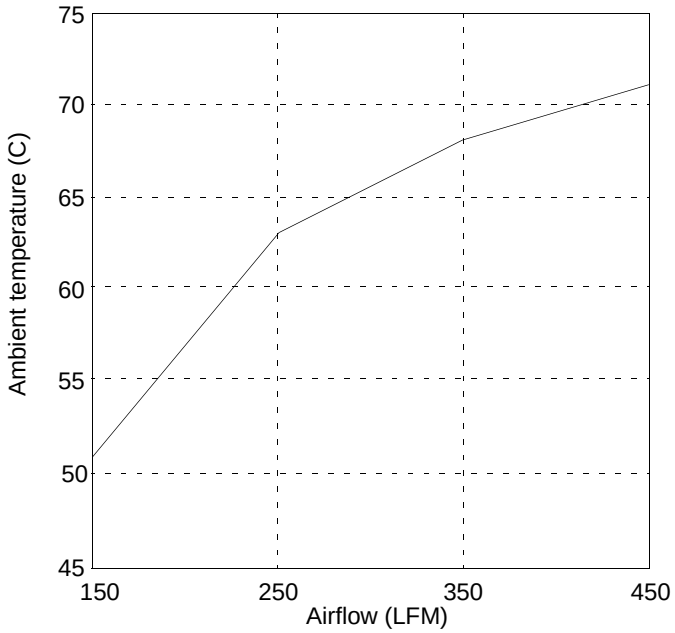


Figure 1-2. SP6040 airflow requirements

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Table 1-3. Additional SP6040 specifications

Characteristic	Value	
Current	+5V (+5/–3%)	0.4A typical; 0.52A maximum
	+3.3V (+5/–3%)	4.0 to 5.2A typical (depending on C6201 activity); 7A maximum
	+12V (+/–5%)	0.02A typical; 0.0026A maximum
	–12V (+/–5%)	0.002A typical; 0.0026A maximum
Mechanical	Weight	0.6 lb. (0.29 kg)
	Dimensions	233.35mm (6U) x 160 mm
NEBS	Designed to be part of a system that meets NEBS Level 3, as defined in bellcore SR3580, Issue 1. (With the exception of the contaminants testing, which is only tested to indoor levels.)	
Safety	US and Canada	The SP6040 is listed to UL-1950 and CSA 22.2 Nr. 950 as an SELV computer accessory board.
	Europe	EN 60950:1992 + A1:1993 + A2:1993 + A3:1995 + A4:1997 + A11:1998.
	CE mark	Low-voltage directive 93/68/EEC.
EMC	FCC	Tested to FCC part 15, class A emissions limits.
	CE mark	EMC directive 89/336/EEC.
	Emissions	EN 55022:1998, class A levels.
	Immunity	EN 55024:1998
MTBF	MTBF (Mean Time Between Failure) is predicted for the module using Bellcore Technical Requirement TR-332, Issue 6. The calculations were performed using a Ground Benign, controlled environment at 40°C with a 50% electrical stress factor. The MTBF predicted for the module is 186,576 hours.	

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2 Installation

This chapter explains how to install a SP6040 in a CompactPCI (cPCI) telecom chassis.



For information about setting jumpers, see the Jumpers section in *Appendix B, Connectors, headers, and jumpers*.

For information about installing device drivers for the SP6040 and any installed PMC modules, see System software installation on page 7.

When reading this file online, you can immediately view information about any installation topic by placing the mouse cursor over a connector name and clicking.

Task	Page
Inserting the SP6040	6
Removing the SP6040	6
Starting the SP6040	7
System software installation	7



Avoid causing ESD (electrostatic discharge) damage:

- Remove modules from their antistatic bags only in a static-free environment.
- Perform the installation process (described later in this chapter) only in a static-free environment.
- During external cable installation, ensure that the cables are not active. The SP6040 is not designed for hot insertion of a cable interface.

The SP6040 modules, like most other electronic devices, are susceptible to ESD damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

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Inserting the SP6040

You install an SP6040 on the CompactPCI bus backplane.



When handling or inserting the SP6040, avoid touching the circuit board and connector pins, and ensure that the environment is static-free.

1. Remove the SP6040 from its anti-static bag.
2. Ensure that all options are installed on the SP6040.
3. Check the following:
   A. Ensure that the SP6040 has a solder side cover installed to protect against accidental contact with adjacent live adapters.
   B. Ensure that the SP6040's ESD strip on the top and bottom edge of the board is unobstructed so it can mate properly with the ESD clip in the chassis' card guide.
4. Move the extractor handles on the front panel to the eject position by pulling the handles away from each other to their maximum extent. (With the top handle tilted up and the bottom handle tilted down.)
5. Slide the SP6040 into the slot, pushing it in until the extractor handles rest on the latch rail extrusion of the CompactPCI chassis. The board's connector should be partially mated to the backplane.

   If you are inserting a Hot Swap board, push the SP6040 in until the blue Hot Swap LED light turns on.
6. Move the extractor handles on the front panel to the closed position by pressing the extractor handles inwards towards the center of the front panel until the SP6040 is fully seated in the chassis and the extractor handles lock into place.

   If you are inserting a Hot Swap board:
   1. The blue Hot Swap LED turns off.
   2. The SP6040 runs the POST, then the red Fault LED turns off.

      The green Run LED lights indicates that the SP6040 is properly inserted and ready for operation.



If this sequence does not occur, see the diagnostic information in the *Appendix C, Diagnostics*

Removing the SP6040

To remove the SP6040 from the CompactPCI chassis:

1. Move the extractor handles on the front panel to the eject position by pushing the top handle up and the bottom handle down so that the handles appear tilted.

   If you are removing a Hot Swap board:
   A. Move the lower extractor handle to the eject position.
   B. Wait for the blue Hot Swap LED to light. When lit, this LED indicates that the board can be safely removed.

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C. Move the upper extractor handle to the eject position.

2. Slide the SP6040 out of the CompactPCI chassis slot. Pull firmly on the handles to release the module from the connectors.
3. Place the SP6040 in an anti-static bag.

Starting the SP6040

To start the SP6040, do one of these:

- Turn on the system.
- Reset the system.
- If the board is Hot-Swap capable, simply insert the board as described in Inserting the SP6040 on page 6.

After you start the SP6040:

- The POST starts. For details about POST and where POST results are stored, see Appendix C, Diagnostics.
- The SPIRIT-60x0 Monitor (sometimes referred to as SPMON) starts.

  This real-time monitor runs on the i960 IOP (I/O Processor). Basic Monitor system services are available to a single application which can run on “top” of the Monitor, for example, timers, interrupt handlers, and access to peripherals.

Connecting cables to the SP6040



Do not plug cables or connectors into the front panel connectors while the system is powered up. Because electronics equipment generally cannot withstand fluctuations in power, damage can arise from plugging in a device or board while power is on.

System software installation

TASK-6000 software

To run any of the components that comprise the SPIRIT-60x0 BSP (Board Support Package), you must install the BSP. For more information about BSP, see the *Appendix E, Board support package*.

To communicate with and run applications on the IOP and DSP, you must install TASK-6000 software on the Windows NT host. For setup and installation instructions, see chapter three of the *TASK-6000 Installation Guide*.

PMC software options

PMC options installed on the SP6040 are typically configured and managed as private devices on the IOP, these devices are hidden from the Windows NT host. Presently, the IOP monitor or application must provide support for installed options.

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3 Theory of operation

The SP6040 is a highly integrated, intelligent I/O subsystem designed for use in 32-bit CompactPCI telecom applications. It is designed to the *CompactPCI Specification* and includes these features:

- Four 200MHz Texas Instruments TMS320C6201B Digital Signal Processor (C6201) with the following features and resources:
  - 4MB of 100 MHz Synchronous DRAM (SDRAM) per DSP.
  - Two enhanced buffered multi-channel serial ports (MCSP0 and MCSP1) per DSP.
- An Intel i960RD (66/33 MHz) I/O Processor with the following features and resources:
  - 16MB EDO DRAM implemented in one on-board bank of 16 Mbytes. Optionally, one additional 16 Mbyte 72-pin SODIMM module on an expansion socket.
  - 4MB Flash ROM.
  - One 32-bit PMC socket, connected to the local (on-board) PCI bus.
  - Access to the C6201 host port interfaces, via the local (on-board) PCI bus.
  - Configuration access to the H.110 TDM bus interface via the i960RD local bus.
  - RS-232 serial port on the i960RD local bus for a diagnostic and debug port.
  - System monitor stored in Flash ROM.
  - Watchdog timer circuit on the i960RD local bus.
- A DEC/Intel 21554 PCI-PCI bridge for address translation between the host and local PCI buses.
- T8105 H.110 TDM bus interface and time slot interchanger (TDM Switch)
  - ECTF H.110 bus interface.
  - Time slot interchanger (switch) to handle all stream routing.
  - Direct stream connections to each DSP via MCSP0 and MCSP1.
  - Direct stream connections to an optional E1/T1 on PMC connector J13.
  - Direct stream connection to Audio Monitor through a CODEC.

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- Conectors and LEDs:

Panel	Features
Front	• RS-232 (RJ-45) • Cutout to support an option module • LEDs: RUN (green) FAIL (red) Hot Swap (blue)
Rear	• J1 32-bit PCI interface[1] • J3 10/100Base-TX Ethernet interface • J4 H.110 telecom connector[2] • J5 analog telecom I/O[2]

1 As defined in the *CompactPCI Specification*.
2 As defined in the *CompactPCI Computer Telephony Specification*.

Block diagram

Figure 3-1 shows the division and interconnection of the SP6040.

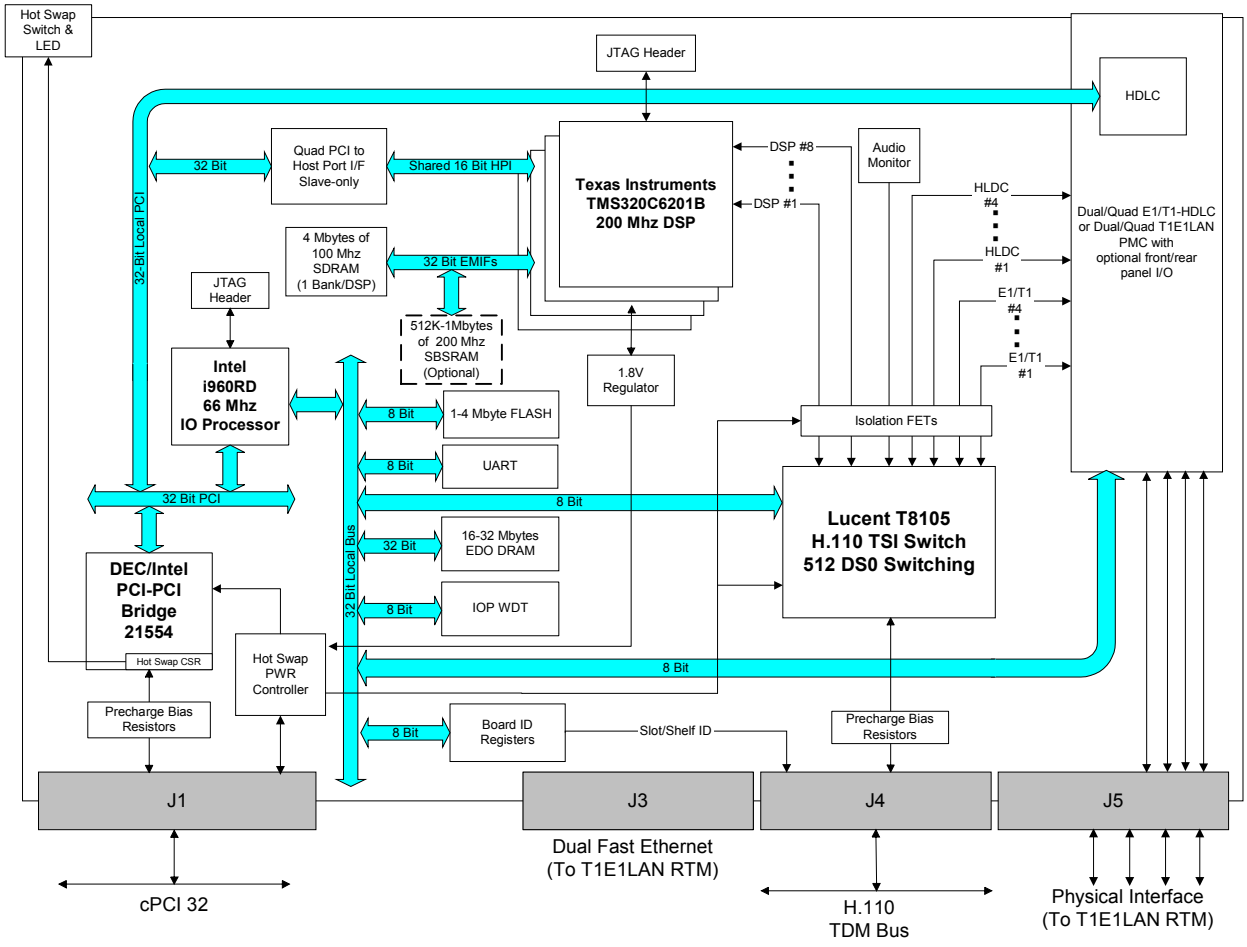


Figure 3-1. Block diagram of the SP6040

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Functional elements

DSP

The TMS320C6201[1] serves as the SP6040's main processing engine. This device delivers up to 1600 MIPS of processing power, contingent on the available parallelism within application code. A 16-bit wide HPI (Host Port Interface) provides the I/O processor (described below) access to the entire C6201's address space. This interface downloads DSP code and transfers application code data. Two enhanced buffered serial ports connect to TDM streams via the T1805 TDM Switch. To optimize C6201 performance, the TASK-6000 kernel controls the loading of telecom applications into C6201 internal program memory. A 14-pin JTAG header provides emulation support for the C6201.



This JTAG chain is 3.3V only and is separate from other JTAG chains connected to several on-board programmable devices and the i960RD processor.

C6201 EMIF

The C6201 EMIF (External Memory Interface) provides a glueless interface to external SDRAM. The address space controlled by the EMIF consists of four sub-spaces: CE0, CE1, CE2, and CE3. The SP6040 maps SBSRAM into CE0 and SDRAM into CE2. SBSRAM is optional on the module and is installed on the default configuration. The EMIF control registers[2] are initialized at startup, as shown in Table A-22, to support the TASK 6000 kernel.

C6201 SDRAM

The DSP includes 4 MB of 100 MHz (half the C6201's clock rate) SDRAM that serve as the DSP's bulk memory. The DSP can provide burst accesses at 400 MB/sec to and from this memory subsystem.



You must set the MTYPE field of the EMIF Space Control registers for CE2 to 011b to indicate its use as SDRAM.

1. The SP6040 powers up.
2. The i960 issues these commands:.



- A pause of 200 ms minimum is required before issuing any commands to the SDRAM.
- The i960 power-up/init/post takes several seconds to complete, while the DSP is held in reset for this period. Thus, the user generally need not be concerned about this.

- SDRAM recharging commands (recharges SDRAM banks).
- Mode Register Set command (configures the SDRAM).
- AutoRefresh command. This command must be issued a minimum of eight times to stabilize the device.

1. *TMS320C6201/B Digital Signal Processor Data Sheet, Revision 2.1/3.0*
2. Described in section 6.2 of the *TMS320C6201/C6701 Peripherals Reference Guide*

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Writing a 1 to the INIT bit of the SDRAM Control register initializes the SDRAM for any space configured as SDRAM. The SDRAM initialize sequence of the C6201 is insufficient to fully initialize the SDRAM. It is necessary to allow the C6201 to perform the eight AutoRefresh commands before the SDRAM is ready for use.

C6201 SBSRAM

The DSP optionally includes either 512KB or 1MB of 200 MHz pipelined SBSRAM, that serves as high speed zero wait-state memory for the DSP. The device uses a footprint capable of supporting both memory densities in a 119-pin PBGA package.

The DSP can produce burst accesses at 800MB/sec to and from this memory system. C6201 EMIF memory space CE0 is used for SBSRAM.



You must set the MTYPE field of the EMIF Space Control registers for CE2 to 011b to indicate its use as SDRAM.

C6201 host port interface

The C6201 HPI (Host Port Interface) is implemented as a slave device on the local PCI bus. As a PCI device, DMA transfers can occur between the HPI port and i960RD DRAM, under the control of the i960RD on-chip DMA controller or address translation unit. The maximum sustained transfer rate through this interface is approximately 13 MB/sec for writes and 15 MB/sec for reads.

The PCI interface is designed using the PLX 9050, a standard PCI target bridge chip. Back-end logic for interfacing to the DSP's HPI port is done in a CPLD. The interface logic performs both address and data cycles to the C6201 HPI interface based on a single 32-bit PCI access. The PLX 9050 supports four independent 28-bit memory spaces configured from the primary PCI interface. The full memory space for the C6201 DSP and its external memory interface uses a 32-bit address space. The address map for the DSP is compressed to fit into the PLX local bus 28-bit space with further decoding in the HPI interface logic. The local side of the PLX interface is configured as a 16-bit data bus. In response to 32-bit PCI cycles, the PLX 9050 generates two 16-bit cycles on the local bus to complete an HPI transaction.

From a programming viewpoint, the HPI is controlled by means of four C6201 internal registers: HPIA, HPID(2), and HPIC (associated with HPI address, data, data with post-increment, and control respectively). These registers are memory-mapped as local PCI device seven by the SP6040 (see Table 3-2). SP6040 boards have multiple C6201 DSPs, a shared 16-bits HPI bus is used for the DSPs with separate chip selects.

The HPIA address register is accessed in pairs of 16-bit (halfword) cycles, under control of SP6040 logic (a PLD). These cycles are, in turn, caused by the address phase of the multiplexed 32-bit PCI accesses to PCI memory space (see Table A-26). The HPID data is accessed using the data portion of the multiplexed PCI memory access. References to these addresses result in accesses to C6201 address space at an index specified by the HPIA address register. In one case, the HPIA register *increments*, following the data access (post-increment) whereas, in the other case, it remains unaltered by the access. Accesses to the HPI interface from the SP6040 Local PCI bus are transparent to a programmer. Table A-26 shows the PCI address mapping of the C6201 DSP memory space, although a programmer still may access the individual HPI internal registers (mapped into PCI offset 00E0 000h to 00EF FFFFh) the entire memory space of the DSP

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is mapped directly into 32-bit PCI space. A programmer only needs to specify the correct PCI offset to access the internal or external memory spaces.

The PCI-HPI interface on the SP6040 supports only 32-bit accesses. The HPI Control register in the C6201 DSP is a 16-bit resource, when writing to this register on the SP6040 the programmer must supply identical upper and lower 16-bit words in the 32-bit PCI access. When reading the HPI Control register on the SP6040, a programmer must use the 16-bit word obtained in the upper half of the 32-bit PCI access; interrupts may be missed if they occur between 16-bit reads to the HPI Control register and the lower 16-bit word is used.

The SP6040 supports HPI interrupts in both directions. The C6201 can interrupt the i960RD (or other local PCI host processor) by setting the HINT bit in the HPI control register (HPIC)[1]. The i960RD, or PCI Master, can clear the interrupt by also setting the HINT bit in the HPIC. The latter mechanism is useful in allowing the C6201 to effectively initiate a transfer to the local PCI Host processor. The local PCI Host processor can interrupt the C6201 by setting the DSPINT bit in the HPIC. The C6201 clears the interrupt by also setting the DSPINT bit. The four DSP interrupt lines are set in an edge sensitive manner in an interrupt status register mapped into DSPA, PCI memory space. The register is used for the system interrupt controller to determine with one access the source of the interrupting processor.

Bootload

Bootloading of the C6201 also occurs via the HPI:

1. The C6201 configures itself at power-up to use the HPI boot process, and to use Memory Map 1 (internal program RAM at address 0).

   In this mode, the C6201 CPU core is held in reset while the remainder of the device comes out of reset.

2. HPI transfers fill the C6201 memory space with DSP applications.

3. The i960 brings the CPUout of reset by setting the DSPINT bit of the HPIC register.

   For a complete description of C6201 HPI operation, see the *TMS320C6201/C6701 Peripherals Reference Guide*.

Resetting C6201 devices occurs individually through a reset register mapped into DSPA, PCI memory space. The register allows for setting each of the DSP reset signals individually.

PLX9050 serial ROM defaults

Table A-1 describes the contents of the Serial ROM defaults used to pre-configure the PLX9050 bridge at power-up. The 9050 provides a total of six address spaces/base address registers. The first two access internal registers within the 9050 itself. The remaining four (PCI base address 2–5) map each of the DSP spaces. These spaces are also referred to as local address space 0–3 in PLX literature.

1. Page 5-11 of the *TMS320C6201/C6701 Peripherals Reference Guide*

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C6201 DSP and HPI clocks

The SP6040 DSP circuits are driven by a single oscillator through a high speed clock buffer. Each device is driven a single, series terminated, clock line to minimize the line reflections seen by the device. The DSP circuits use the x4 internal PLL to generate the core and external memory clocks. The next table shows the SP6040 clock options.

Table 3-1. DSP clock circuit options

Oscillator frequency	DSP core frequency	Eternal memory clock (SDRAM)	External memory clock (SBSRAM)	Supported devices
50.00 MHz	200 MHz	100 MHz	200/100 MHz	C6201B-200 DSP
41.67 MHz	167 MHz	83.5 MHz	167/83.5 MHz	C6201B-167 or C6701 DSP

The HPI port of the DSPs interfaces to the backside of the PLX 9050 bridge chip. The backside of the PLX device can be run asynchronous to the PCI interface clock. A 40 MHz oscillator is used on the SP6040 to drive the local interface of the PLX chip and the HPI glue logic CPLD.

DSP program load sequence

The DSPs are in reset when control is released by the i960 regardless of whether the i960 is in Fail-safe or standard mode. In terms of the module power-up sequence, these steps cannot take place until the POST routines have completed device initialization, functional testing and Local PCI bus memory mapping.

After POST, the Monitor leaves each of the populated DSPs in Reset. Host and IOP APIs are available to, among other things, initialize the DSP, boot load the DSP, read/write from/to the DSP and set up DSP interrupt handlers.

To run a program on the DSP, the following steps occur:

1. The DSP is first taken out of reset. Reset is unasserted by writing a 0 to the proper bit location in the C6201 reset register which is accessible in all the DSP PCI memory maps at offset 0x00F00004. The bit locations are shown in Table A-24 and the DSP PCI memory map is shown in Table A-26.
2. The HWOB bit [bit 0] in the HPI Control register of the desired DSP must be written as a one to allow proper ordering of HPI accesses. The HPI Control register is accessible in the individual DSP memory maps at offset 0x0E000008 as shown in Table A-26.
3. The EMIF control registers must be initialized with the proper values to allow access to the DSP's external memory. The EMIF registers are accessible in the individual DSP memory maps starting at offset 0x0300000 as shown in Table A-26. The contents of each EMIF register are given in Table A-22.
4. At this stage of the initialization the DSP is ready to have code and data loaded by the host processor.
5. To complete the DSP's HPI boot sequence and start program execution the DSP INT bit [bit 1] in the HPI Control register must be set to a one. The HPI Control register is accessible in the individual DSP memory maps at offset 0x0E000008 as shown in Table A-26.

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To stop the existing program on any DSP and reload, the DSP must be placed into reset by asserting reset to the DSP by writing a 1 to the proper bit location in the C6201 reset register which is accessible in all the DSP PCI memory maps at offset 0x00F00000. The bit locations are shown in Table A-24 and the DSP memory map is shown in Table A-26.

CompactPCI interface

The SP6040 implements a 32-bit, 33MHz CompactPCI[1] single slot peripheral board. The module uses the standard 2 mm-pitch, 5-row Hard Metric shielded connector, keyed for Universal signaling. If the SP6040 is intended for use in a CompactPCI Hot Swap application, a 5V PCI signalling key should be installed. This connector has a 5 column by 47 row array of pins divided into two groups corresponding to the physical implementation. The connector shield is used as a ground shield for EMI protection. Of the remaining columns, J1 pins 1–25 provide 32-bit PCI and connector keying implemented as one connector.

The module presents no more than a single load on each PCI bus signal as required by the *CompactPCI Specification.*

The SP6040 uses the DEC 21554 PCI-PCI bridge as the CompactPCI interface on the board. The device was selected to provide a Host interface to an on-board PCI bus, which connects the IOP, DSP and PMC interfaces, as well as for its suitability in the Hot Swap environment. The device is a non-transparent PCI-PCI Bridge compliant with the *PCI Local Bus Specification, Revision 2.1* on both its primary and secondary interfaces. The device is also considered hot swap “Friendly” as outlined in the *CompactPCI Hot Swap Specification*.

The bridge offers posted write data queues (256 Bytes) and delayed read data queues (256 Bytes) in both directions as well as a delayed transaction queue supporting up to four pending transactions.

The DEC 21554 core is powered from 3.3V with 5V tolerant IO buffers, the secondary interface uses the 5V PCI signaling environment. Only PMC modules compatible with PCI 5V signaling can be populated on the SP6040 as the site is keyed for this environment. The primary PCI interface is powered from VIO on the CompactPCI J1 connector, allowing the module to be used in either environment. CompactPCI Hot Swap is supported only for the 5V PCI signaling environment, the module can be used with 3.3V PCI backplane signaling but may not be hot swapped.

The 21554 contains four BARs (Base Address Registers) for downstream transaction forwarding from the host PCI bus to the on-board local PCI bus. One BAR is programmable as memory or IO space and also contains CSRs specific to the 21554, the other three BARs forward only memory transactions. All the BARs on the primary interface provide direct offset address translation. The device also contains three BARs for upstream transaction forwarding from the local PCI bus to the system host. One BAR is programmable for memory or I/O transactions, a second is used for forwarding memory transactions only. Both registers support direct offset address translation. A third BAR is used for forwarding memory transactions using LUT (Look Up Table) based address translation.

1. *CompactPCI Specification*

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The DEC bridge distributes a clock to on-board local PCI bus from its primary PCI clock. An external clock buffer is used to distribute a clock to the on-board PCI devices. On the SP6040, the 21554 PCI interfaces are run synchronously by feeding back a clock output from the external clock buffer to the secondary interface. Both PCI interfaces on the 21554 are 33MHz and 64 bit, the 64 bit PCI extensions are disabled on both interfaces which support 32-bit transactions only. The 21554 also contains a Secondary PCI Arbiter which is used on the SP6040 by the on-board devices to arbitrate for the local PCI bus.

The on-board PCI devices on the SP6040 are mapped on the Local PCI bus as shown in the following table. These devices are configured by the i960RD using Type 0 configuration cycles on its Primary PCI interface. The mapping shown corresponds to the selection of the Interrupt Binding used on the module..

Table 3-2. On-board PCI bus device mapping

Device number	IDSEL line	Function
6	PCI.AD16	PMC site
7	PCI.AD17	PCI-HPI interface
8	PCI.AD18	PCI-PCI bridge
10	PCI.AD20	i960RD I/O processor

DEC/Intel 21554 configuration and initialization

The 21554 contains two sets of configuration registers, one for each PCI interface, as well as device specific configuration and status registers. Certain configuration registers can be pre-loaded at power-up using a serial ROM connected to the bridge. This allows the PCI interfaces in the device to be tailored to the specific implementation prior to the Host or Local processor access to PCI configuration space. The serial ROM unloads automatically at power-up and signals a Target Retry on both PCI interfaces until the serial ROM pre-load sequence completes. On the SP6040, the bridge uses an external pull-up to set the Primary Lockout configuration space bit at power-up. Setting this bit prevents PCI configuration accesses from the Host processor on the Primary interface of the bridge, signaling a Target Retry, until the bit is cleared by the Local processor. In this configuration the local processor can overwrite the configuration values, loaded by the serial ROM at power-up, using Secondary PCI configuration space accesses.

For default register and map values, see the following tables:

- Table A-2 on page 35 defines the Serial ROM default values used to pre-configure the bridge at power-up.
- Table A-3 on page 38 shows the address translation window mapping through the SP6040 bridge. This map may be altered for a specific platform by firmware overwriting the defaults established by the serial ROM pre-load.

I/O processor

An Intel i960RD serves as the on-board I/O processor for the SP6040. The i960RD includes these PCI buses:

- **Primary bus**: Includes a direct connection to the on-board PCI bus.
- **Secondary bus**: Not is not used on the module.

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Attached to the i960RD local bus are a variety of resources described separately below. The i960RD can perform data transfers between its local memory and sources or destinations on its primary PCI bus. Separate DMA channels exist between the individual PCI buses and the i960RD local bus for high-bandwidth transfers.

Debugging of i960RD code can be done via the RS-232 interface or a 16-pin i960RD JTAG header. A small debug kernel running on the i960RD is required to support debug. For more information about this kernel, see the *Appendix E, Board support package*.

Responsibilities of the i960RD include:

- System and diagnostic controller
- Local IO processor for managing and transferring network data
- TDM Switch control and configuration
- Bootloading and data transfer to the C6201 DSP's

IOP DRAM

The i960RD includes with up to 32 Mbytes of high-performance EDO DRAM for application program and data storage. The i960RD internal memory controller manages the DRAM access and refresh cycles using dedicated address and control signals and the i960RD 32-bit local data bus. The SP6040 supports DRAM devices and modules which support single wait-state performance, peak transfers of up to 64 Mbytes per second can be achieved. The SP6040 implementation supports two non-interleaved memory banks of 16 Mbytes each. The module supports one on-board bank of 16 Mbytes that use 3.3V, 4Mx4 50nS EDO DRAMs packaged in TSOP 24/26 packages. Memory expansion is supported by a 72 pin, SODIMM socket which can be populated with one 16 MByte memory module. SODIMM module support is limited to symmetrically addressed devices (for example, 11 row x 11 column).

The Presence Detect bits from the SODIMM module are register-accessible on the i960RD local bus for firmware to determine if the expansion module is populated. The i960RD Memory Controller is restrictive on what memory banks are supported, the memory controller uses the same timing and bank size registers for all banks. For example, if a 60 nS, 16 MByte memory module were populated in the expansion socket, the memory sizing routine detect this and declare this an un-useable memory module. The JEDEC standard defines the presence detect bits from the memory expansion module as shown in the next table:

Table 3-3. SODIMM presence detect bits

Presence detect bits	PD4:1-organization	PD6:5-speed	PD7-refresh type
Definition	4Mx32/36	50nS	Normal
Binary Value	1011[1]	00	1

1 The i960RD processor supports only 11/11 addressing, a module with 12/10 addressing has the same binary code. The firmware must size the module to determine if a compliant module is installed.

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The i960RD on-chip memory controller manages the DRAM refresh cycles. For programming information, see chapter 14 of the *i960RD I/O Microprocessor Developers Manual*.

Flash ROM

The Initial Memory Image (IMI), fail-safe monitor, programmable monitor (SPMON), and optional user code (see Table A-5) resides in flash-updatable ROM on the SP6040. The Flash is memory-mapped into 4MB of i960RD local memory space, 0xFEC00000 to 0xFEFFFFFF. The upper 64KB of the first bank (2MB) is factory-programmed. The remainder of that bank, as well as the entire lower bank (2MB), is writeable from the i960RD and thus, in principle, user programmable. In the case of the 1MB Flash ROM option, the device is aliased into the upper 1MB of the 4MB region.

The monitor regions are not normally reprogrammed by the user. This capability is provided to facilitate changes by RadiSys manufacturing.

RS-232 interface

The i960RD local bus includes a UART (RS-232 interface). This resource is available for both application use and diagnostics. The UART interface is brought out through the front panel via an RJ-45 connector.

IOP watchdog timer

A WDT (WatchDog Timer) function resides on the Local Bus Decode CPLD for monitoring the i960RD I/O processor. The SP6040 has a two-level watchdog timer used to recover from errant code. Each timer has a granularity of 63mS and a software programmable range of 63mS to 4000mS. Once enabled, the timers must be strobed/reset at intervals of less than their programmed range. Timer expiration results in the generation of an i960 non-maskable interrupt or a board reset.

- **Level 1 timer**: Expiration of the level 1 timer causes an NMI to the i960. The expiration of this timer also starts the level 2 timer, if it was previously enabled.
- **Level 2 timer**: If the level 2 timer is allowed to expire, a hard reset to the i960 occurs. Both timers are disabled upon power-up and reset.

For detailed information about programming timers, see Appendix A, Device initialization and memory maps.

IOP memory map

The next figure shows the memory map for the i960 Processor. The map shows the location of all i960 peripherls after board initialization.

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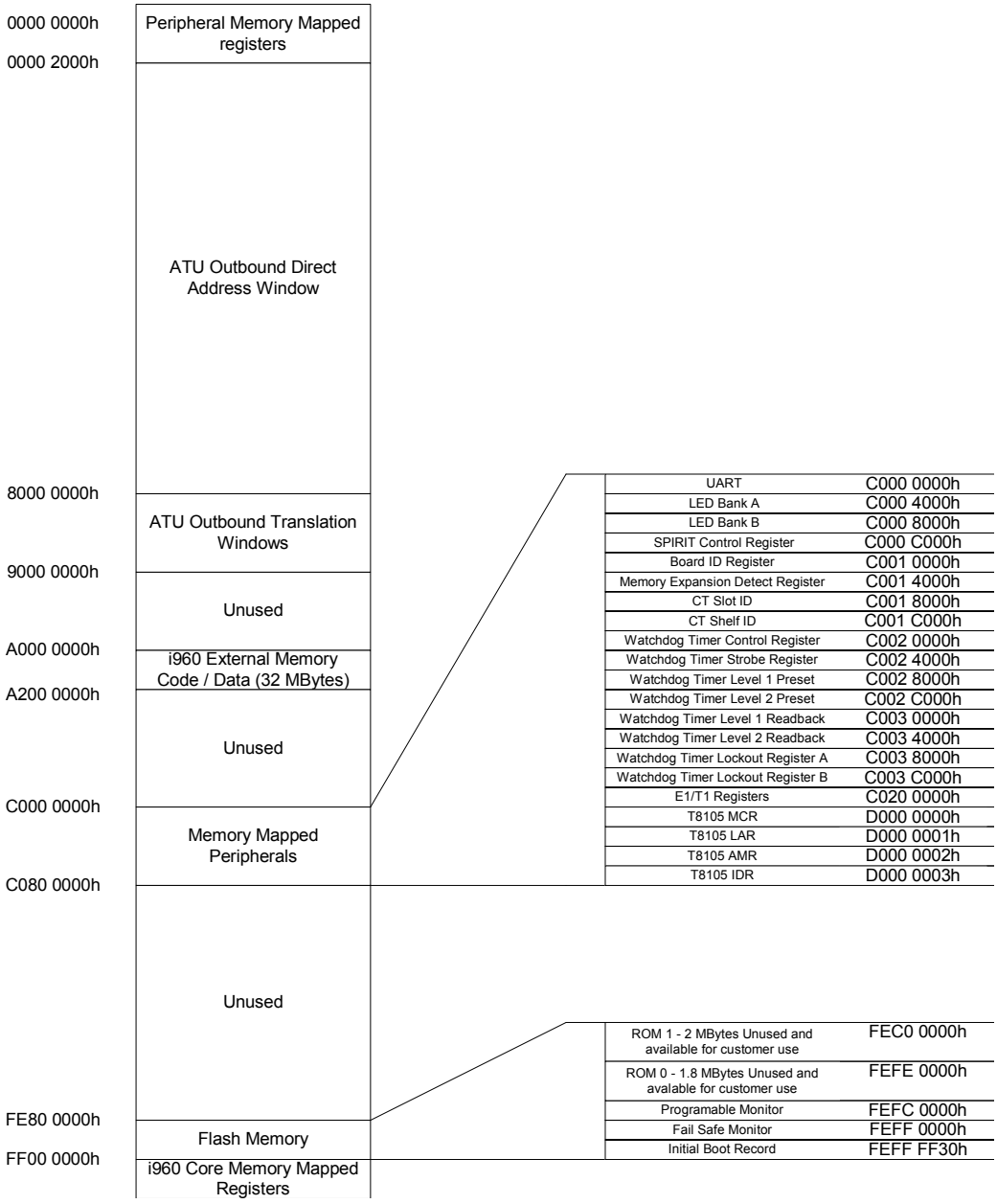


Figure 3-2. SP6040 memory map

H.110 TDM bus interface

A Lucent T8105 H.110 Interface and Time-Slot Interchanger[1] provides high-performance routing of telecom data between the H.110 TDM Bus[2], PMC connector J13, the C6201 DSP and the Audio CODEC. Capabilities provided by the T8105 include:

1. *Lucent Ambassador*† T8100A, T8102, and T8105 H.100/H.110 Interfaces and Time-Slot Interchangers Data Sheet
2. *CompactPCI Computer Telephony Specification*

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- Access to the full 4096 H.110 Bus time slots (32 streams, 128 slots each).
- Programmable switching between local time-slots and H.110 bus, up to 512 connections.
- Programmable switching between local time slots, up to 1024 connections.

Any of the 4096 channels (TDM slots) contained in up to 32 streams with 128 channels each, are accessible from either the C6201 or J13 of the PMC site. Additional connections are provided between the PMC site and the DSPs via the TDM switch. These connections do not consume channels on the backplane H.110 bus. The SP6040 can act as a CT bus clock master to allow connection to external communications equipment.

The T8105 TDM switch is configured and controlled by the i960RD via a conventional 8-bit wide microprocessor bus, mapped into the i960RD local memory space.

The entire memory space is accessible via the microprocessor interface using indirect addressing. The i960Rx local address space[1] includes these addressable registers:

- **MCR (Master Control Register)**: Provides reset and enable control functions and well as status of microprocessor accesses to the T8105.
- **LAR (Lower Address Register) and AMR (Address Mode Register)**: Indirectly address internal memory and control registers in the device. The AMR selects the internal memory space being addressed. LAR is a register offset when the AMR is set to 00h or a time-slot address when the AMR is addressing internal memories.
- **IDR (Indirect Data Register)**: Reads or writes data to a given control register or internal memory after the LAR and AMR have been setup.

For programming information, see chapter 2 of the *Lucent Ambassador*† T8100A, T8102, and T8105 H.100/H.110 Interfaces and Time-Slot Interchangers Data Sheet.

All the local telecom data streams can operate at 2.048 MHz, with the T8105 providing the clocks and frame synchronizations required for the various serial devices. In addition, the data streams connected to the DSP serial ports can be operated at 4.096MHz or 8.192MHz although both serial ports 0 and 1 cannot be operated at 8.192MHz simultaneously.

The T8105 Local Selected Clocks (L_SCn) drives the clocks for the local streams:

- L_SC0 and L_SC1 drive the CLKS inputs of DSP serial ports 0 and 1 respectively.
- L_SC2 clocks TDM data to the PMC connectors and the Audio Monitor.
- L_SC3 is a spare clock output which is connected to PMC connector J13.

The Local Selected Clocks are controlled by T8105 registers CK10 and CK32.

The T8105 has two frame groups, each group having twelve frame pulses (FGA[0..11], FGB[0..11]). The offset of the first frame pulse from the CT_FRAME pulse is programmable, with the remaining pulse being enabled sequentially one time slot apart. The frame group pins may also be configured as programmable output ports from the T8105. There are several combinations of frame group outputs/programmable outputs available from the T8105. PMC connectors and the Audio Monitor use FGA0 with an offset of (–1) 2.048 MHz bit clocks. FGB0, configured to drive out on pin FGA6 and

1. See Table A-7 for this mapping

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FGB0, drives the FSRs (port 0 and 1 respectively) of the DSPs and is configured with an offset of 0.

The DSP serial ports use the sample rate generator and re-synchronize to the FGB0/FGA6 signals received on the FSR pins. The RX and TX data delay should be programmed to 0, and FGB0 configured to fire on the last bit of the frame.

Recovered clocks from network interface devices connected to the PMC connector are routed to the L_REF inputs of the T8105. In the case of the T1/E1 board, these clocks run at 8 KHz.

The T8105 drives a clock out on PMCTCLK0 that can be used by the option module as a transmit time base. In the case of the T1/E1 board, this should be set to 2.048 MHz. The T8105 uses an L_REF (network recovered clock), a CT_Bus derived clock, or its local 16.184 MHz oscillator as the reference for its internal timing and for generating all its output clocks.

The default configuration for the T8105 is to provide clocks, streams and frame groups operating at 2.048MHz. The frame group offsets are programmed to be (–1) 2.048MHz bit clock for the E1/T1 and CODEC, and (0) bit clocks for the DSPs.

T1805 TDM switch stream assignments

The next figure shows local stream resources assigned to the T1805. The SP6040 supports DSPA, DSPB, DSPC, and DSPD. PMC I/O for the SP6040 include T1/E1 data on IO_R/TXD1..4 and HDLC data on IO_R/TXD5..8.

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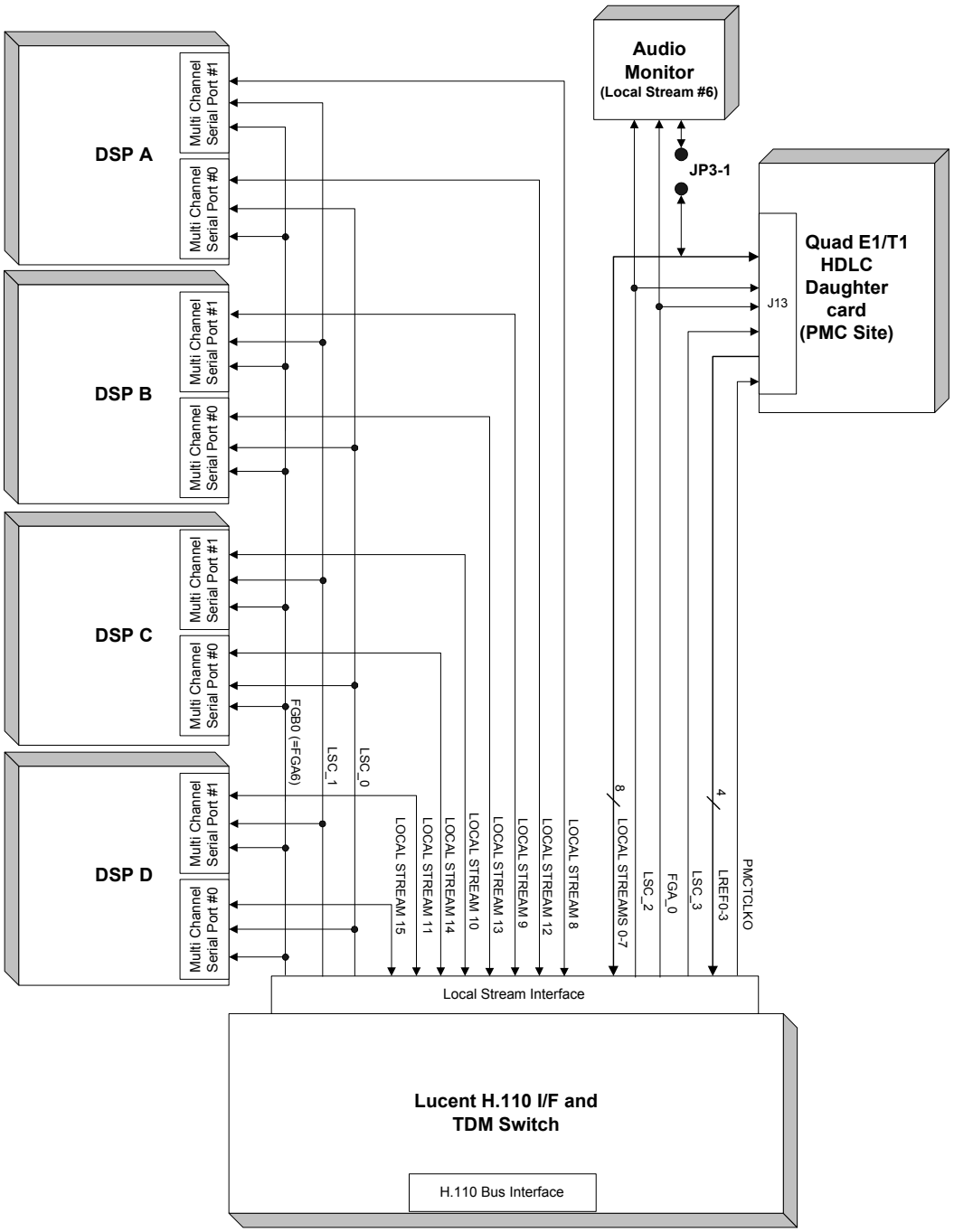


Figure 3-3. SP6040 TDM stream assignments

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PMC socket

The SP6040 supports a single PMC socket (denoted PMC) with these connectors:

- J11 and J12 carry the 32-bit PCI signals.
- J13 and J14 have telecom I/O-specific assignments, and do not conform with the 64-bit PCI extension. These assignments are required, in particular, by RadiSys telecom I/O option modules (see following sections). PMC J13 and J14 also support a custom 10/100Base-TX Ethernet pin-out on the PMC J13 connector.

In applications not that do not require either of these options, the PMC site is available as a compliant 32-bit PMC expansion socket.

Dual/quad E1/T1-HDLC option module

While actually a SP6040 option, this module receives special support through two additional, user-specific, mezzanine connectors, denoted J13 and J14. This includes i960RD local bus selection decode and 8-bit data for configuration of LIU/Framer devices on the option module. This module also has an HDLC controller attached to the secondary PCI bus (J11/J12).

The two E1/T1 physical layer streams (eight signals) are normally brought in to the LIU/Framers from signals attached to RJ-45 connectors, which first pass through surge protection, filtering, and transformer decoupling. The RJ-45 connectors are made available through the PMC mounting panel, together with the LEDs that indicate option module status. Alternatively, the physical layer signals can be brought in directly from J13/J14 (in turn connected to connector J5 on the motherboard). In this case, the option module can support *four* E1/T1 streams (sixteen signals), provided that protection, filtering, and de-coupling is done external to the baseboard. Additional (optional) LIU/framer devices must be installed on the option module for four-channel operation.

Quad E1/T1/LAN option module

This SP6040 option uses J13/J14 PMC connectors for local stream routing to the TDM switch on the baseboard, an 8-bit configuration port to the i960RD IOP, and routing support for four E1/T1 physical layer streams (sixteen signals) and two 10/100Base-T Ethernet physical layer streams with an I2C bus interface to support activity LEDs (twelve signals).

The T1/E1 physical layer streams are connected on the baseboard directly to the CompactPCI J5 connector as specified in the *CompactPCI Computer Telephony Specification*. The Ethernet serial lines and status signals are connected to the CompactPCI J3 connector. A rear transition module is required to gain access to the LAN/WAN data and contains the required protection, filtering and decoupling circuitry.

The module has three devices connected to the baseboard PCI bus (via the PMC J11/J12 connectors), a 128-channel HDLC controller, and two Ethernet controller devices. These devices are considered extensions to the on-board PCI bus and, as such, they each are routed an individual PCI AD bit for IDSEL (on the option module) for configuration. A PCI sub arbiter is available on the option module to allow all three devices to master the on-board PCI bus.

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Analog telecom IO

The J5 CompactPCI I/O connector provides direct physical layer access to telecom data, with four related E1/T1 streams connected from J5 to the user-specific J13/J14 connectors on the PMC module. These stream connections meet the pin-out requirements of the CompactPCI Computer Telephony specification for Safety Extra Low Voltage qualified signaling. In configurations that use the RadiSys Quad E1/T1/LAN option module (see above), inclusion of these streams normally requires that option module protection, filtering, and de-coupling circuitry be depopulated, and equivalent circuitry be provided *externally* (for example, on a rear-panel transition card).

The J3 CompactPCI I/O connector provides direct physical layer access to two 10/100Base-TX Ethernet ports connected between the PMC J13 connector and CompactPCI J3. As stated above for the T1/E1 lines, an external rear transition module contains the protection, filtering ,and de-coupling circuitry for the Ethernet signals.

The CompactPCI CT specification requires feedthrough power and ground signals on this connector to be used byRTMs (Rear Transition Modules) with active circuitry. These signals are fused with re-settable, polymeric PTC fuses as required by the Hot Swap specification.

Audio monitor

Audio input and output signals provide drop/insert functions on a single TDM channel. These signals are converted to or from digital by means of a CODEC. Either μ–law or linear coding can be selected under software control. Optionally, the SP6040 can be factory-configured with an A-law CODEC, with linear coding jumper selectable. These audio input/output signals are available through an on-board 5-pin header (see Table B-10). The Audio Monitor always transmits and receives on the first channel of the stream.

DMA

Both the i960RD and the C6201 have high-performance DMA capabilities.

i960

The i960RD supports these independent DMA channels:

- **Channels 0 and 1**: These channels can effect transfers between the i960RD primary PCI bus and the i960RD local bus. These channels can sustain transfers between i960RD local bus DRAM and the C6201 HPI interface.

  DMA channel 0 in the i960RD supports demand-mode DMA, since there are no devices capable of asserting a DMA request on the i960RD local bus, this feature is not used.

- **Channel 2**: The third channel supports transfers between the i960RD secondary PCI bus and the local bus. There are no devices on the i960's secondary PCI bus. Therefore, this channel is not used.

All the i960RD's DMA channels support a data chaining (scatter/gather) mechanism used to generate a linked list of data blocks to transfer.

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The i960RD DMA controller also contains a hardware packing and unpacking unit to support unaligned transfers to or from the i960RD local bus or PCI bus with full support for all combinations of unaligned data.

Each channel has a 64-byte data queue to increase data transfer performance in either direction. Burst length on all DMA channels is limited to 2Kbytes, with peak burst rates of 64 MB/sec possible.

For DMA controller programming information, see chapter 20 of the *i960RD I/O Microprocessor Developers Manual*.

C6201

The C6201 supports four independent DMA channels, which can effect transfers between points in the C6201's memory map. The DMA channels can be operated in a split mode, allowing a single DMA channel to service both the transmit and receive side of a serial port. A fifth (auxiliary) channel is dedicated to the HPI. For C6201 DMA controller programming information chapter 4 of the *TMS320C6201/C6701 Peripherals Reference Guide*.

Interrupt usage

The i960 core processor has an 8-bit interrupt controller (~XINT7 to ~XINT0) shared by devices on the on-board secondary PCI bus and both internal and external peripherals on the i960RD local bus. SP6040 PMC slot on the local PCI bus drives the four secondary PCI interrupts of the i960RD. The PCI-HPI logic and the DEC 21554 drive individual interrupt lines to the i960RD that correspond to the device mapping on the module. The external peripherals on the SP6040 local bus drive inputs ~XINT7 to ~XINT5 on the i960RD. In some cases, these inputs are shared with peripherals on the i960RD internal local bus. Figure 3-4 shows the configuration of interrupts to the i960RD internal interrupt controller. The C6201 interrupt asserts local PCI ~INTB and is a logical-OR of the individual interrupt conditions in the four DSP processors. The PCI-HPI logic provides a register to determine the source DSP of a given interrupt. This register latches interrupts on the negative edge of the signal and clears when read.

The interrupt controller also supports non-maskable interrupts for both internal and external peripherals for reporting error conditions. The external NMI interrupt is connected on the i960RD to a local bus watchdog timer which under program control can detect errant software on the IOP. For interrupt controller programming information refer to chapter 8 of the *i960RD I/O Microprocessor Developers Manual*. All interrupts are maskable via programmable registers and are hard-coded to an interrupt priority at power-up.

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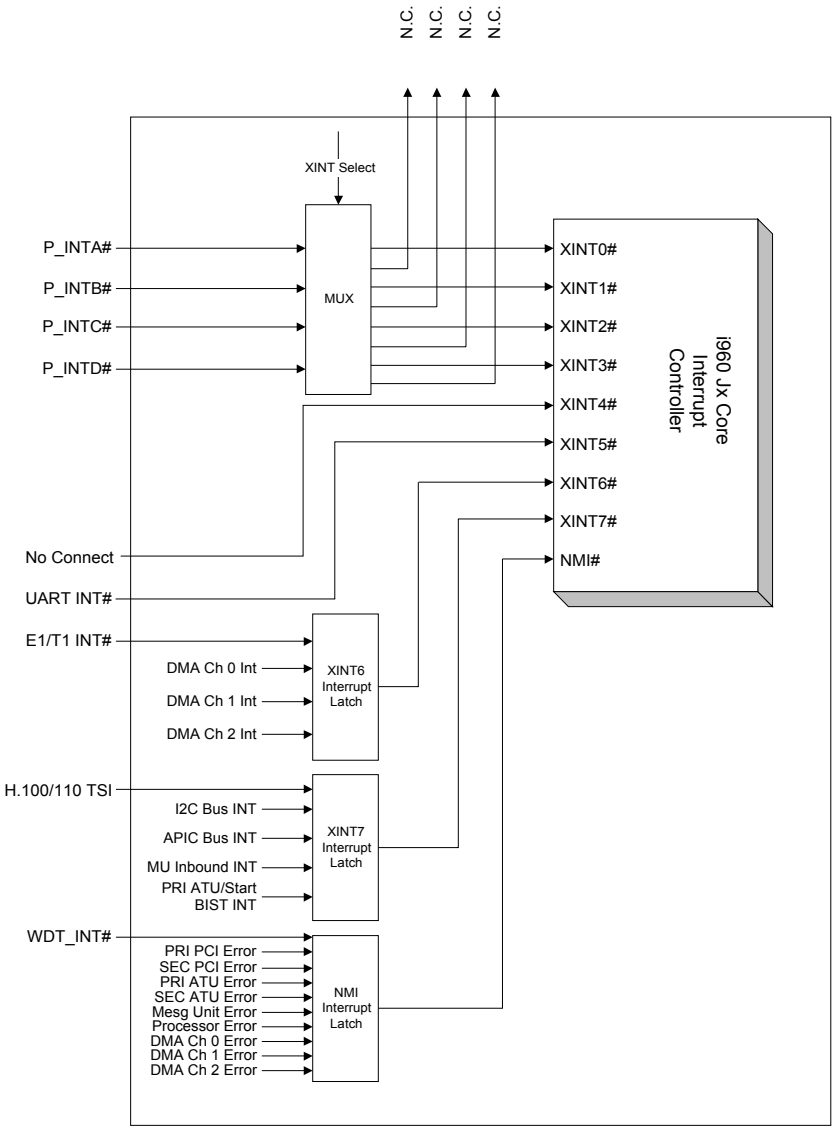


Figure 3-4. SP6040 i960RD interrupt configuration

The i960RD services interrupt requests from the on-board PCI devices. The i960RD has an internal interrupt controller which is used to service interrupts from peripherals on its local bus as well as interrupts from both the primary and secondary PCI interfaces. The next figure illustrates how PCI interrupts are connected on the SP6040 for the on-board PCI bus.

To support an IOP module located on the PMC site, the interrupt from the PCI-HPI interface can be connected (using configuration resistors) to the local PCI bus ~INTA line instead of the standard routing to local ~INTB.

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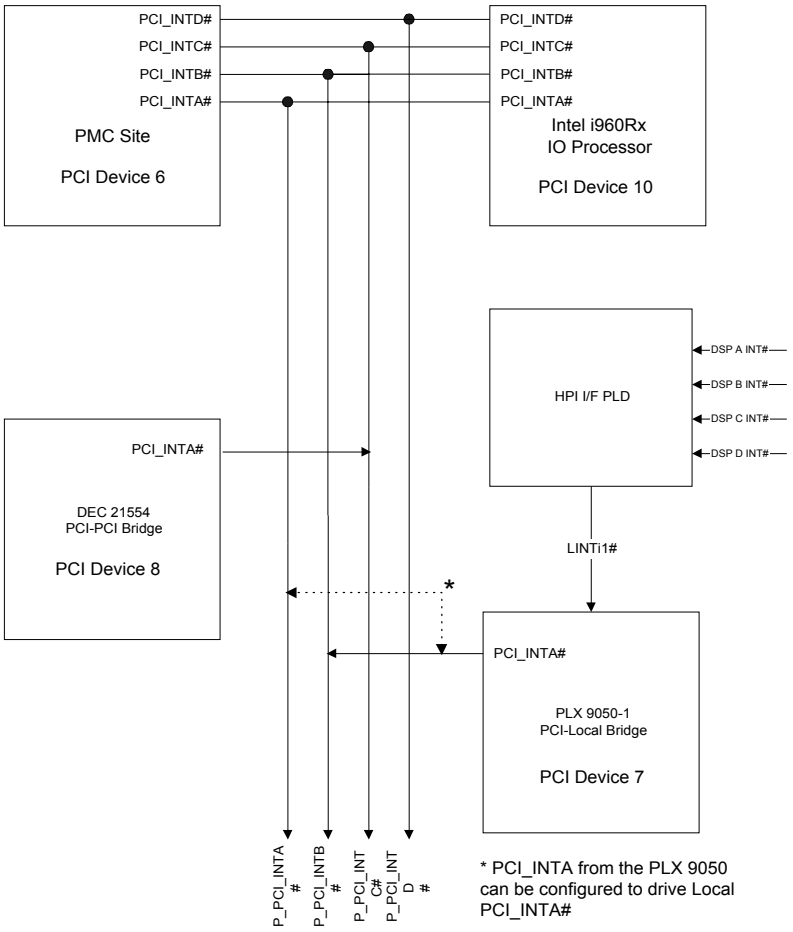


Figure 3-5. SP6040 PCI interrupts

LED indicators

LEDs are provided on the front panel as system indicators:

Table 3-4. LED indicators

Indicator	Color	Description
Run	Green	i960 local bus activity
FAIL	Red	Failure of SP6040 POST
Hot Swap	Blue	(See next section and Appendix C)

Additional LEDs may be present on PMC modules (in particular, through the front panels of those modules), and are documented in the associated descriptions of those units.

Sixteen LEDs display POST faults and monitor status, as detailed in the *Appendix B, Connectors, headers, and jumpers*.

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Hot Swap functionality

Hot Swap defines a process for installing and removing adapter boards without adversely affecting a running system. This allows repair of faulty boards and system reconfiguration during operation, and thus minimizes system downtime. The requirements for implementing Hot Swap are outlined in the *CompactPCI Hot Swap Specification* and *CompactPCI Computer Telephony Specification* respectively for each bus.

The SP6040 supports hot swapping the primary PCI interface and H.110 TDM bus interfaces, and follows the requirements for a Full Hot Swap adapter as outlined in the *CompactPCI Hot Swap Specification*. This adapter model implements all the minimum features of a Hot Swap adapter and adds additional resources for software connection control. This implementation allows a full range of system implementations, including those that support dynamic system configuration and high availability platforms.



- The backplane that the SP6040 is installed in must meet several requirements for a Hot Swap platform, as described in the *CompactPCI Hot Swap Specification* and the *CompactPCI Computer Telephony Specification*.
- The chassis used in a Hot Swap platform must support the IEEE 1101.10 mechanical requirements for ESD protection. Specifically, it must contain an ESD clip, as specified, in the lower card guide.
- If the SP6040 is used in a non-telecom CompactPCI chassis (for example, no H.110 support on J4), the \CT_EN signal on J4-C23 must be grounded on the backplane to power up the module.

Hot swap is defined by these processes:

- **Physical connection**: describes the act of physically inserting or extracting a board from a live system.
- **Hardware connection**: describes the electrical connection or disconnection of the Hardware Layer to the system.
- **Software connection**: describes the connection or disconnection of the software layer to the system.

The following sections briefly outline these processes.

Physical connection process

The physical connection process is the means by which a board is introduced to the platform. It begins with an operator sliding the board into the chassis card guide and ends with the connectors fully mated on the backplane. The following chronology of events serves to illustrate the physical connection process:

1. An operator inserts the board into the chassis card guide.
2. The board front panel is discharged to chassis GND through a bleed resistor. This is accomplished by means of an ESD clip attached to the card guide and the ESD strip described in the mechanical requirements section.
3. The board logic ground is discharged to chassis GND through a bleed resistor.
4. The bleed resistor breaks contact with chassis GND isolating the board logic GND.

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5. The board contacts long pins on the backplane and begins to contact GND, +5V, +3.3V and VIO pins.
6. The board is unstable for a period of time due mainly to pin bounce.
7. Enough pins are connected to establish a stable Early Power.
   - CompactPCI and TDM bus interface logic is powered up and decoupling capacitors attached to early power are charged.
   - The ~LOCAL_PCI_RST signal is asserted and remains asserted throughout the physical connection process. The bus interface devices must asynchronously tri-state all signals which connect to the bus.
   - Early Power has stabilized all bus interface signals to the pre-charge potential.
   - The Hot Swap Blue LED is asserted by the hardware.
8. The board contacts the medium pins on the backplane.
   - The bus interface pins make contact with the bus. The disturbance to active signals does not cause logic thresholds to be violated.
   - The board begins to track levels on the bus and is now receiving a clock.
   - Medium length power pins make contact and short out the current limiting resistors. Input power to the isolation circuitry is established.
9. The board contacts both the ~BD_SEL and \CT_EN signals which are grounded on the backplane. Once both pins make contact (meaning J1 and J4 are fully seated) the backend power-up is started.
   - The backend power is ramped up at a controlled rate to minimize power transients on the backplane power bus.
   - Once back-end power is up and stable, the on-board power controller releases local PCI reset to allow the interface devices to connect to the backplane bus.

The physical disconnection process occurs in essentially the reverse. There are additional requirements to discharge hazardous potentials developed on the board to prevent unintentional contact by an operator.

Hardware connection process

After physically inserting the board into the chassis, the hardware connection process starts and continues to completion, making the board accessible to the host processor for software connection.



If the board indicates a power fault at any time during the connection process it is prevented from connecting to the bus (local PCI reset is not released).

The power controller controls the rate at which the back-end logic powers up to prevent power glitching on the system power supplies, or damage to the power pins on the board or backplane. The power controller also provides current limiting for each backend supply to protect against short circuit conditions. Once the back-end power is up and stable, the power controller generates a ~PWRGD signal to indicate that the backend voltages are

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within tolerance. This signal generates the ~HEALTHY signal used in high availability platforms to indicate that the board is ready to connect.

When ~HEALTHY activates and the PCI bus reset signal is not active, the bus interface devices are taken out of reset (~LOCAL_PCI_RST is released) and are ready to accept bus access cycles. Board specific fault conditions can also be added to the generation of ~HEALTHY to prevent the board from connecting to the bus.

Hardware disconnection is essentially performed in the reverse. In a Full Hot Swap system, disconnection starts by the ~BD_SEL or ~\CT_EN pin breaking contact. The Power controller enable is removed and back end power starts to turn off. Once one backend voltage is out of tolerance, the ~HEALTHY signal de-asserts and ~LOCAL_PCI_RST asserts. The bus interface devices tri-state all bus interface signals and HW asserts the blue LED.

Software connection process

After the board completes the hardware connection process, the software connection process commences. A Full Hot Swap board adds resources to control the software connection process.

- ~ENUM, an open collector signal generated by the Hot Swap board, notifies the Host that a Hot Swap event occurred. This signal is defined and bused in the CompactPCI backplane and eithers generates an interrupt on the Host module or is polled in software.
- A Hot Swap switch integral to the lower module ejector. The switch generates ~ENUM when board extraction is required or signals the end of the insertion process. This signal is sensed in the HS_CSR.
- A blue status LED, visible from the module’s front panel, lights when it is permissible to extract a board. Upon insertion, the LED lights during the hardware connection process.
- Hot Swap Control/Status Register, two control/status bits (INS and EXT) are used by software to determine the reason for an ~ENUM assertion. Two control bits (EIM and LOO) further support the processL
  - **EIM bit**: This bit masks the ~ENUM signal.
  - **LOO bit**: this bit turns the Hot Swap Status LED on or off.

Closing the lower board ejector on the front panel, and the back end power is ~HEALTHY, causes the adapter to generate the ~ENUM signal to inform the Host processor that it is ready to be configured (enumerated). The host processor detects the ~ENUM event, either through polling the bit or through an interrupt request, and attempts to determine the source. This is typically done by reading the HS_CSR in PCI configuration space to determine if a board has been freshly inserted (by setting the INS bit) or is requesting to be extracted (by setting the EXT bit). Upon detecting an insertion request, the system software sets the EIM bit, to mask the ~ENUM signal, and tries to configure the device. If configuration of the board was successful, the INS bit clears and the EIM bit de-activates to arm the board for extraction.

An extraction request is initiated by the removing the lower board ejector from the latched position. The HS_CSR senses the built-in microswitch and generates an ~ENUM request to the host processor. The EXT bit is also set by this action. When the host services the

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~ENUM request it begins to quiesce the board driver associated with the requesting device. After the board driver is shut down, system software asserts the LOO[1] bit in the HS_CSR to assert the blue Hot Swap LED as a visual indication to the system operator that the board may now be removed.

Primary PCI interface

The DEC 21554 PCI-PCI bridge provides the SP6040's primary PCI interface. The CompactPCI Hot Swap specification defines these compatibility levels for compliant PCI devices:

- **Hot Swap Capable**: Existing devices can be considered "Hot Swap capable" if they meet the minimum requirements outlined in the Hot Swap specification. These are attributes of a device that a board designer would not be able to compensate for with external circuitry and are not typically specified in a manufacturer's data sheet. These issues include;
  - The devices ability to tolerate a bias voltage applied to bus interface pins which are in a high impedance state
  - The ability of the device to asynchronously tri-state all its bus interface pins with the assertion of the PCI reset pin and to operate properly when reset is released with an active cycle on the bus.
  - The ability to tolerate VCC from the early power island, this voltage may be non-monotonic and may ramp up very quickly.
  - The ability to maintain limited IO pin leakage with a bias voltage applied.
  - The ability to comply with a modified signaling environment (the use of CMOS drivers).
- **Hot Swap Friendly**: Devices that meet all the requirements of hot swap capable devices and, at a minimum, supply the HS_CSR in PCI configuration space to support dynamic configuration of the device upon insertion. These devices must also support the signaling required to communicate with the Hot Swap switch and Led to assist in inserting and extracting the board.
- **Hot Swap Ready**: Devices that contain all desirable features for the Hot Swap environment including; internal bias support to pre-charge the PCI drivers connecting to the live bus, Hot Swap Control/Status Register (HS_CSR) support in PCI configuration space, and the ability to tolerate early power to the device without back end logic connected to the device being powered.

The DEC/Intel 21554 meets all the requirements to be considered a hot swap "Friendly" device as outlined in the CompactPCI Hot Swap specification. The device implements a Hot Swap Control/Status Register in primary PCI configuration space. The register is accessed using the ECP (Extended Capabilities Pointer) mechanism in PCI configuration space. This pointer defines an offset within PCI configuration space to the base address of the HS_CSR. The register is preferred in PCI configuration space to allow access to the

1. The 21554 PCI-PCI bridge uses a single device pin to both sense the ejector micro switch and to drive the hot swap blue LED. For this reason, if the LOO bit is asserted by the Hot Swap Service running on the Host - re-insertion of an adapter is disabled. If the Hot Swap Service is modified to allow the blue LED to be passively driven, a reinsertion sequence can occur.

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HS_CSR bits prior to configuring the device on insertion and after the board driver has been quiesced (to allow turning on the LED) prior to extraction. The use of the ECP mechanism and a standardized bit location within the register allows portability of the device to general use Hot Swap platforms. The capability ID for Hot Swap is writeable from the serial ROM pre-load (at PCI configuration space offset ECh) to match the industry standard value assigned for Hot Swap (the device was designed prior to this assignment). The actual HS CSR is located at offset EEh in PCI configuration space; see Figure A-27 for a register definition.

PCI bus isolation

The primary PCI bus isolation relies on the interface device to tri-state all of its PCI buffers when its reset line is active. The I/O pins for the device are pre-charged to a bias voltage determined through simulation to minimize the disruption to live signaling on the bus when live inserted. When early power is established on the module, the PCI interface device is powered and its reset line is driven active. Each PCI interface pin that connects to a live bused pin on the backplane is biased using an external pull-up resistor. The pull-up resistor value is determined to minimize the board leakage current while still being able to charge the on-board network to the required bias voltage under pin bounce conditions. Under these conditions, the mechanical “bounce” associated with mating the interface pins to the backplane may try to establish a connection in as little as 5ms. The choice of external pull-up resistor must be responsive enough to condition the bus interface pins in less than 5ms while minimizing the leakage current seen by the bus pins.

H.110 TDM bus interface

The SP6040’s H.110 TDM bus interface is supplied by the Lucent T8105 Ambassador, designed specifically for use in the Hot Swappable H.110 environment. The device tristates all its external interface pins with the assertion of reset and requires an external bias circuit similar to the PCI interface. Pin staging in the CompactPCI J4 connector increases the capacity of the early power planes due to the additional interface.

The CompactPCI CT specification requires that the \CT_EN pin on the CompactPCI J4 connector be OR’d with the CompactPCI ~BD_SEL signal to ensure that the on-board reset signal is not released until both connector interfaces are fully seated.

Hot Swap power controller

The SP6040 uses the Linear Technology LTC1643L as its on-board power controller. The device provides the features necessary for implementing the power isolation and protection circuitry required by the Hot Swap specification. Each supply voltage is monitored for over-current and under-voltage conditions. The device has programmable fold-back current limit feature with a circuit breaker to prevent current spikes and excessive power dissipation during short circuit conditions. The ramp rate for the output voltages is programmable based on a current loop compensation capacitor, the Hot Swap specification requires that this rate not exceed 1.5A/mS.

The controller has a ~FAULT output which latches down the outputs of the power controller, after a programmable hold-off timer which allows the voltages to stabilize at power-up, when over-current conditions are detected. The output of the on-board 2.5/1.8 volt regulator is integrated into the power control circuitry to protect the DSP circuits.

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A Device initialization and memory maps

This appendix details the device and memory maps used by the SP6040.

When reading this file online, you can immediately view information about any installation topic by placing the mouse cursor over a connector name and clicking.

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SP6040 memory map	38
i960RD I/O processor	39
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Hot Swap control and status register	49

Device initialization

PLX9050 serial ROM

Table A-1. PLX9050 serial ROM defaults

EEPROM offset	Register offset	EEPROM value	Register description
0	PCI 02	9050	Device ID.
2	PCI 00	10B5	Vendor ID.
4	PCI 0A	0680	Class code.
6	PCI 08	000x	Class code (revision is not loadable).
8	PCI 2E	6040	Subsystem ID.
A	PCI 2C	1331	Sub system Vendor ID.
C	PCI 3E	xxxx	Maximum latency and minimum grant are not loadable.
E	PCI 3C	01xx	Interrupt pin (interrupt line routing is not loadable).
10	LOCAL 02	FF00	MSW of range for PCI to local address space 0 (1 MB).
12	LOCAL 00	0000	LSW of range for PCI to local address space 0 (1 MB).
14	LOCAL 06	FF00	MSW of range for PCI to local address space 1.
16	LOCAL 04	0000	LSW of range for PCI to local address space 1.
18	LOCAL 0A	FF00	MSW of range for PCI to local address space 2.
1A	LOCAL 08	0000	LSW of range for PCI to local address space 2.
1C	LOCAL 0E	FF00	MSW of range for PCI to local address space 3.
1E	LOCAL 0C	0000	LSW of range for PCI to local address space 3.
20	LOCAL 12	0000	MSW of range for PCI to local expansion ROM (64 KB).

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Table A-1. PLX9050 serial ROM defaults

EEPROM offset	Register offset	EEPROM value	Register description
22	LOCAL 10	0000	LSW of range for PCI to local expansion ROM (64 KB).
24	LOCAL 16	0000	MSW of local base address (re-map) for PCI to local address space 0.
26	LOCAL 14	0001	LSW of local base address (re-map) for PCI to local address space 0.
28	LOCAL 1A	0200	MSW of local base address (re-map) for PCI to local address space 1.
2A	LOCAL 18	0001	LSW of local base address (re-map) for PCI to local address space 1.
2C	LOCAL 1E	0400	MSW of local base address (re-map) for PCI to local address space 2
2E	LOCAL 1C	0001	LSW of local base address (re-map) for PCI to local address space 2
30	LOCAL 22	0600	MSW of local base address (re-map) for PCI to local address space 3.
32	LOCAL 20	0001	LSW of local base address (re-map) for PCI to local address space 3.
34	LOCAL 26	0000	MSW of local base address (re-map) for PCI to local expansion ROM.
36	LOCAL 24	0000	LSW of local base address (re-map) for PCI to local expansion ROM.
38	LOCAL 2A	0040	MSW of bus region descriptors for local address space 0.
3A	LOCAL 28	2007	LSW of bus region descriptors for local address space 0.
3C	LOCAL 2E	0040	MSW of bus region descriptors for local address space 1.
3E	LOCAL 2C	2007	LSW of bus region descriptors for local address space 1.
40	LOCAL 32	0040	MSW of bus region descriptors for local address space 2.
42	LOCAL 30	2007	LSW of bus region descriptors for local address space 2.
44	LOCAL 36	0040	MSW of bus region descriptors for local address space 3.
46	LOCAL 34	2007	LSW of bus region descriptors for local address space 3.
48	LOCAL 3A	0000	MSW of bus region descriptors for expansion ROM space.
4A	LOCAL 38	0000	LSW of bus region descriptors for expansion ROM space.
4C	LOCAL 3E	0100	MSW of CS (chip select) 0 Base and Range register.
4E	LOCAL 3C	0001	LSW of CS (chip select) 0 Base and Range register.
50	LOCAL 42	0300	MSW of CS (chip select) 1 Base and Range register.
52	LOCAL 40	0001	LSW of CS (chip select) 1 Base and Range register.
54	LOCAL 46	0500	MSW of CS (chip select) 2 Base and Range register
56	LOCAL 44	0001	LSW of CS (chip select) 2 Base and Range register.
58	LOCAL 4A	0700	MSW of CS (chip select) 3 Base and Range register.
5A	LOCAL 48	0001	LSW of CS (chip select) 3 Base and Range register.
5C	LOCAL 4E	0000	MSW of Interrupt Control/Status register.
5E	LOCAL 4C	0043	LSW of Interrupt Control/Status register.
60	LOCAL 52	1836	MSW of EEPROM Control and Miscellaneous Control register
62	LOCAL 50	3B40	MSW of EEPROM Control and Miscellaneous Control register

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DEC/Intel 21544

These tables contain the default values for these configuration registers:

- Table A-2 defines the Serial ROM default values used to pre-configure the bridge at power-up.
- Table A-3 shows the address translation window mapping through the SP6040 bridge. This map may be altered for a specific platform by firmware overwriting the defaults established by the serial ROM pre-load.

For information about using these registers, see DEC/Intel 21554 configuration and initialization on page 16

Table A-2. DEC/Intel 21544 serial ROM default values

Byte offset	Description	Pre-load value	Comment
00h	[7] 1 to enable serial pre-load [6:0] 0000000b (Reserved)	80h	Enabled
01h	00000000b (reserved)	00h	
02h	00000000b (reserved)	00h	
03h	00000000b (reserved)	00h	
04h	Primary programming interface	00h	As defined by PCI
05h	Primary sub-class code	80h	As defined by PCI
06h	Primary base class code	06h	As defined by PCI
07h	Subsystem vendor ID [7:0]	31h	RadiSys subsystem vendor ID
08h	Subsystem vendor ID [15:8]	13h	RadiSys subsystem vendor ID
09h	Subsystem ID [7:0]	40h	SP6040
0Ah	Subsystem ID [15:8]	60h	SP6040
0Bh	Primary minimum grant	24h	Minimum burst time required for the 21554 to master the local PCI bus in ¼ ms increments (assuming a 50-byte packet size and 10 clock latency)
0Ch	Primary maximum latency	0Ah	Specifies how often the 21554 needs to master the host PCI bus in ¼ ms increments (10ms/4 DSP)
0Dh	Secondary programming interface	00h	As defined by PCI
0Eh	Secondary sub-class code	80h	As defined by PCI
0Fh	Secondary base class code	06h	As defined by PCI
10h	Secondary minimum grant	24h	Minimum time required for the 21554 to master the local PCI bus in ¼ ms increments
11h	Secondary maximum latency	0Ah	Specifies how often the 21554 needs to master the local PCI bus in ¼ ms increments
12h	Downstream memory 0 setup [7:0] Bits [0, 7:4] are not loaded and should be 0.	00h	4 KB memory space, no pre-fetch

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Table A-2. DEC/Intel 21544 serial ROM default values

Byte offset	Description	Pre-load value	Comment
13h	Downstream memory 0 setup [15:8] Bits [11:8] are not loaded and should be 0.	00h	4 KB memory space, no pre-fetch
14h	Downstream memory 0 setup [23:16]	00h	4 KB memory space, no pre-fetch
15h	Downstream memory 0 setup [31:24]	00h	4 KB memory space, no pre-fetch
16h	Downstream I/O or memory 1 setup [7:0] Bits [5:4] are not loaded and should be 0.	00h	8 Mbyte memory space, no pre-fetch
17h	Downstream I/O or memory 1 setup [15:8]	00h	8 Mbyte memory space, no pre-fetch
18h	Downstream I/O or memory 1 setup [23:16]	80h	8 Mbyte memory space, no pre-fetch
19h	Downstream I/O or Memory 1 Setup [31:24]	FFh	8 Mbyte memory space, no pre-fetch
1Ah	Downstream memory 2 setup [7:0] Bits [0, 7:4] are not loaded and should be 0.	00h	Disabled
1Bh	Downstream memory 2 setup [15:8] Bits [11:8] are not loaded and should be 0.	00h	Disabled
1Ch	Downstream memory 2 setup [23:16]	00h	Disabled
1Dh	Downstream memory 2 setup [31:24]	00h	Disabled
1Eh	Downstream memory 3 setup [7:0] Bits [0, 7:4] are not loaded and should be 0.	00h	Disabled
1Fh	Downstream memory 3 setup [15:8] Bits [11:8] are not loaded and should be 0.	00h	Disabled
20h	Downstream memory 3 setup [23:16]	00h	Disabled
21h	Downstream memory 3 setup [31:24]	00h	Disabled
22h	Downstream memory 3 setup upper 32-bits [7:0]	00h	Disabled
23h	Downstream memory 3 setup upper 32-bits [15:8]	00h	Disabled
24h	Downstream memory 3 setup upper 32-bits [23:16]	00h	Disabled
25h	Downstream memory 3 setup upper 32-bits [31:24]	00h	Disabled
26h	Bit [0]: Primary expansion ROM setup [24] (enable) Bits [3:1]: Not loaded; should be 0. Bits [7:4]: Primary expansion ROM setup [15:11]	00h	Disabled
27h	Primary expansion ROM Setup [23:16]	00h	Disabled
28h	Upstream I/O or memory 0 setup [7:0] Bits [5:4] are not loaded and should be 0.	00h	64 Mbyte memory space, prefetch enabled
29h	Upstream I/O or memory 0 setup [15:8]	00h	64 Mbyte memory space, prefetch enabled
2Ah	Upstream I/O or memory 0 setup [23:16]	00h	64 Mbyte memory space, prefetch enabled
2Bh	Upstream I/O or Memory 0 Setup [31:24]	FCh	64 Mbyte memory space, prefetch enabled

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Table A-2. DEC/Intel 21544 serial ROM default values

Byte offset	Description	Pre-load value	Comment
2Ch	Upstream memory 1 setup [7:0] Bits [0, 7:4] are not loaded and should be 0.	00h	Disabled
2Dh	Upstream memory 1 setup [15:8] Bits [11:8] are not loaded and should be 0.	00h	Disabled
2Eh	Upstream memory 1 setup [23:16]	00h	Disabled
2Fh	Upstream memory 1 setup [31:24]	00h	Disabled
30h	Chip control 0 [7:0]	00h	
31h	Chip control 0 [15:8] Bits [13:12] are not loaded and should be 0.	04h	Primary lockout bit set, must be cleared by the local processor top enable host configuration
32h	Chip control 1 [7:0]	00h	
33h	Chip control 1 [15:8]	00h	Upstream memory 2 BAR disabled, I2O unit disabled
34h	Arbiter control [7:0]	01h	i960 on the high-priority arbiter ring, PMC site on the low-priority ring
35h	Arbiter control [15:7] Bits [15:10] are not loaded and should be 0.	02h	21554 secondary interface on the high-priority arbiter ring
36h	Primary ~SERR disable Bit [7] is not loaded and should be 0.	00h	All conditions unmasked
37h	Secondary ~SERR disable Bit [7] is not loaded and should be 0.	00h	All conditions unmasked
38h	Power management data 0	00h	Not used; disabled
39h	Power management data 1	00h	
3Bh	Power management data 2	00h	
3Bh	Power management data 3	00h	
3Ch	Power management data 4	00h	
3Dh	Power management data 5	00h	
3Eh	Power management data 6	00h	
3Fh	Power management data 7	00h	
40h	Compact PCI Hot Swap ECP ID	06h	Assigned by the PCI SIG
41h	[1:0] 00b (reserved) [2] BiST supported [3] Power Management Data register enable [5:4] Power management control and status [14:13] [7:6] Power Management Capabilities register [1:0]	00h	No BiST support; power management disabled

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Table A-2. DEC/Intel 21544 serial ROM default values

Byte offset	Description	Pre-load value	Comment
42h	[0] Power Management Capabilities register [2] [1] Power Management Capabilities register [5] [7:2] Power Management Capabilities register [14:9]	00h	

Table A-3. 21554 address translation window usage

Base address register	Specific use	Translation type
Downstream CSR and memory 0	Device-specific registers, no forwarding range	Direct address translation (above 4 KB)
Downstream memory or I/O 1	i960 16/32 Mbyte DRAM, (default window setting is lowest 8 Mbytes of IOP memory)	Direct address translation
Downstream memory 2	Direct access to each DSP, 64 Mbytes total (default window setting is 0 Mbytes)	Direct address translation
Downstream memory 3[1]	Not used; disabled	Direct address translation, 64-bit DAC
Upstream memory or I/O 0	Shared and host memory no pre-fetch (when IOP master DMA is available)	Direct address translation (default window setting is disabled)
Upstream memory 1[1]	Not used; disabled	Direct address translation
Upstream memory 2 [1]	Not used; disabled	Look-up table

[1] This mapping may be altered to support an upstream or downstream window for a PMC adapter or to directly map DSP memory to the host.

SP6040 memory map

The SP6040 uses the DEC 21554 PCI-PCI bridge as its PCI interface device. There are four devices mapped onto the on-board PCI bus:

- An IEEE 1386 compliant PMC site
- A PCI-HPI Bridge using the PLX 9050 target only device
- The DEC/Intel 21554 Secondary PCI interface
- The i960RD IO Processor

The devices are mapped as device 6,7,8 and 10 respectively which corresponds to the interrupt binding used on the module. The devices are configured by the local processor (the i960RD) by accessing PCI configuration space based on the PCI_AD bit assigned to the IDSEL pin. The memory space requirements for each device are discussed below.

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i960RD I/O processor

The i960RD is a multifunction PCI device. A PCI-PCI bridge unit comprises PCI function 0 in the device, and an Address Translation Unit (ATU) and Messaging Unit (MU) comprise PCI function 1 in the device. The PCI-PCI bridge unit is not used on the module. The ATU and MU supply access between the PCI bus and i960RD local bus. The i960RD has a 66 MHz core, and a 33 MHz local bus.

Configuration and Memory spaces for the Primary and Secondary PCI busses are described in [Intel 97a]. The i960RD local bus hosts the peripherals on the SP6040, including the control interface to the H.110 I/F and Time Slot Interchange device, the control interface to the IO Daughter Card (E1/T1 Framers), the RS-232 UART, local processor memory and board specific control and status registers. This section describes the mapping of these peripherals into the i960RD local bus memory space.

Local bus physical memory regions

The i960RD local bus physical address space is partitioned into eight 512 MByte regions defined by the upper three i960RD local bus address bits. The regions are numbered as eight paired sections from Region 0–1 to Region 14–15. The only physical memory attribute, which must be programmed for these regions, is bus width. The physical memory attributes are programmed through the Physical Memory Configuration registers (PMCON) loaded at power-up from a data structure which is part of the i960RD Initial Memory Image (IMI). The IMI for the i960RD is located at a fixed location in FLASH, and is loaded by the i960RD at power-up to configure the device. The IMI is located in physical memory region 14–15. The lowest order byte of the first four longwords in the IMI programs PMCON 14–15 register to ensure access to the FLASH bank containing the data structures required for initialization. The table below indicates the physical memory regions that are used by the SP6040 and their associated bus widths.

Table A-4. i960RD local bus physical memory attributes

Physical memory region	Address range	Control register value	Attributes
PMCON0_1	0000 0000h to 1FFF FFFFh	0080 0000h	32-bit, 80960RD Peripheral Memory-Mapped register space[1]
PMCON2_3	2000 0000h to 3FFF FFFFh	0080 0000h	Reserved (default is 32-bit)
PMCON4_5	4000 0000h to 5FFF FFFFh	0080 0000h	Reserved (default is 32-bit)
PMCON6_7	6000 0000h to 7FFF FFFFh	0080 0000h	Reserved (default is 32-bit)
PMCON8_9	8000 0000h to 9FFF FFFFh	0080 0000h	Reserved (default is 32-bit)
PMCON10_11	A000 0000h to BFFF FFFFh	0080 0000h	32-bit, 16 Mbytes x 1 bank of EDO DRAM, memory expansion 16MBytes x 1 banks of EDO DRAM, 80960RD outbound ATU translation windows

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Table A-4. i960RD local bus physical memory attributes

Physical memory region	Address range	Control register value	Attributes
PMCON12_13	C000 0000h to DFFF FFFFh	0000 0000h	8-bit, UART, E1/T1 framers, LED I/F, Spirit Control register, Board ID register, CT Shelf ID Register, CT Slot ID register, H.110 and TSI device interface
PMCON14_15	E000 0000h to FFFF FFFFh	0000 0000h	8 bit, IMI, Flash banks, 80960RD Core Processor memory-mapped register space[1]

1 Internal memory-mapped registers do not use external physical memory attributes (bus width)

The above mapping requires that the BCON (Bus Control) register loaded from the Control Table in the IMI has been configured properly: bit 2 of this register must be set for the PMCON register values to be treated as valid. If cleared, all physical memory regions will use the value assigned to physical memory region PMCON14_15 (8-bit) register as loaded from the IMI.

Details of the i960RD initialization process are given in page 11-11 through 11-22, and 12-1 through 12-9 of the *i960RD I/O Microprocessor Developers Manual*.

Flash ROM

4 MB of Flash ROM is provided. This resource is organized as two 2 MB banks, each implemented by a single device (AMD 29F016B). The Flash ROMs store a compressed image containing the IMI (Initial Memory Image) for the i960RD processor at power-up and a diagnostic monitor containing POST and extended diagnostics for local bus peripherals. An RTOS (Real Time Operating System) which runs on the i960RD, a TASK (Telecom Application Specific Kernel) which runs on the TI DSP, and user applications (such as DSP boot code) are other items that may be stored in Flash. The two Flash ROM banks are mapped to physical memory region 14–15. This region of memory defaults to an 8-bit region at power-up. The IBR (Initial Boot Record) is a data structure that initializes the i960RD. This structure resides in Flash between FEFF FF30h and FEFF FF5Fh. This location is fixed at the top of the upper bank of Flash. The address range FEFF FF60h to FEFF FFFFh just above the mapping for the IBR is reserved for use by the processor. Flash memory accesses are performed using the i960RD embedded memory controller. The memory controller unit supports two independent banks of Flash/SRAM/ROM (or other device type). The memory banks can be programmed to respond to any i960RD local bus address (under control of the i960RD MBBAR0:1 registers), and may be configured as 8 or 32-bit data widths (under control of the associated i960RD PMCON register). The memory controller asserts one of two chip enable (~CE1:0) when a local bus address is presented that falls within the window programmed for one of the banks. The SP6040 uses ~CE0 as chip select for the Flash ROM, causing that memory to respond to *all* local bus addresses programmed for this bank (including aliases).

The memory controller configuration registers are located in the address region from 0000 1500h to 0000 15FFh. (See Appendix E of the *i960RD I/O Microprocessor Developers Manual*.)

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Monitor Flash ROM usage

The Flash ROM is broken down into two logical regions, Monitor and User. The Monitor region contains:

- The IOP Monitor image and its components and is approximately 256 KB (4 sectors) in size.
- User region is the remainder of configured FLASH ROM space. The User region may be used to store a Monitor application or an operating system.

The Monitor region consists of four components: IBR, Boot Loader, Fail Safe Monitor and Programmable Monitor sections.

The IBR, Boot Loader and Fail Safe Monitor fit into a single 64KB sector. This sector is typically not reprogrammed unless there is an update required to the boot loader configuration code. The IBR, Boot Loader and Fail Safe Monitor are built together into a single image and must be burned all at once. With this configuration you can burn the Programmable Monitor section without the potential loss of operable state.

The Fail Safe Monitor image is invoked if the Fail Safe jumper is attached or in the event that the Programmable Monitor image checksum fails. The Fail Safe monitor does not support the Host Interface. The slimmed-down User Interface must be obtained via a serial terminal connection. X modem may be used to download and burn a new image into the programmable monitor section.

Table A-5. FLASH ROM memory map

Address Range	Description	ROM bank
FEC0 0000h to FEDF FFFFh	Application[1]	ROM1
FEE0 0000h to FEFB FFFFh	Application	ROM0
FEFC 0000h to FEFE FFFFh	Programmable monitor	ROM0
FEFF 0000h to FEFF FF2Fh	Fail-safe monitor boot loader	ROM0
FEFF FF30h to FEFF FFFFh	IBR	ROM0

1 This region available only in the 4MB Flash configuration (ROM1 installed).

Table A-6. i960RD memory controller configuration and timing

Register name	Register address	Set value	Description
MBCR	0000 1500 h	0087 0087h	Memory Bank Control register (16 Mbyte space for ~CS0, 16 Mbyte space for ~CS1 to minimize decoding bits)
MBBAR0	0000 1504 h	FEC0 0000h	Memory Bank Address register 0 (Shift ROMs to upper Mbyte of 16-Mbyte space)
MBBAR1	0000 1510 h	C000 0000h	Memory Bank Address register 1
MBRWS0	0000 1508 h	0003 0402h	Memory bank read wait state 0
MBRWS1	0000 1514 h	0004 0002h	Memory bank read wait state 1

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Table A-6. i960RD memory controller configuration and timing

Register name	Register address	Set value	Description
MBWWS0	0000 150C h	0003 0002h	Memory bank write wait state 0
MBWWS1	0000 1518 h	0004 0002h	Memory bank write wait state 1

The FLASH bank containing the IBR must be mapped to Memory Bank 0 in order to be recognized by the processor. At power-up this bank defaults to a base address of FE00 0000h and a memory size of 16 MB.

I/O devices

The SP6040 uses the i960RD embedded memory controller (described in the previous section) to generate non-multiplexed bus cycles for peripherals mapped into the address space enabled by ~CE1. This space uses one set of timing values for all accesses controlled by this chip select (see Table A-6). Table A-7 shows the mapping of peripherals in i960RD physical memory region 12_13. The peripherals use only a subset of the allocated space.

The registers containing the LED interface are write-only. When selected the i960RD decode PLD asserts a select line for the desired LED bank which acts as a clock for an external register which drives the LED signals. The UART and E1/T1 Framers are controlled via a microprocessor bus.

Table A-7. i960RD I/O memory map

Physical memory address	Peripheral description
8-bit wide devices:	
C000 0000h to C000 3FFFh	UART (see UART specification, TL16C550C, for details)
C000 4000h to C000 7FFFh	LED bank A (WO)
C000 8000h to C000 BFFFh	LED bank B (WO)
C000 C000h to C000 FFFFh	SPIRIT Control register (R/W)
C001 0000h to C001 3FFFh	Board ID register (RO)
C001 4000h to C001 7FFFh	Memory Expansion Presence Detect register (RO)
C001 8000h to C001 BFFFh	CT Slot ID (geographical address) register (RO)
C001 C000h to C001 FFFFh	CT Shelf ID register (RO)
C002 0000h to C002 3FFFh	Watchdog Timer Control register (R/W)
C002 4000h to C002 7FFFh	Watchdog Timer Strobe register (WO)
C002 8000h to C002 BFFFh	Watchdog Timer Level 1 Preset register
C002 C000h to C002 FFFFh	Watchdog Timer Level 2 Preset register
C003 0000h to C003 3FFFh	Not used
C020 0000h to C020 7FFFh	E1/T1 framers
D000 0000h	T8100A TDM switch MCR
D000 0001h	T8100A TDM switch LAR
D000 0002h	T8100A TDM switch AMR
D000 0003h	T8100A TDM switch IDR

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Table A-8. SPIRIT control register

Bit number	Bit type	Value at reset	Description
0	RO	N/A	~FAILSAFE: selects alternate monitor
1	R/W	1	~FLT_SUM: ORed with i960RD BIST output to drive board fault LED.
2	RO	N/A	~BURNIN: used to force diagnostics to loop
3	RO	N/A	~ROMWRENABLE: When low enables writing to the Flash ROM
4	RO	N/A	~BUSMODE1 from PMC site
5	RO	N/A	i960 ~DEN output
6	R/W	0	RUNCTRL0—Run LED control bit 0
7	R/W	0	RUNCTRL1—Run LED control bit 1

Table A-9. Run LED control bits

RUNCTRL1	RUNCTRL0	Description
0	0	Run LED, driven by i960_DEN signal
0	1	Run LED, toggled when the WDT is strobed
1	0	Illuminate Run LED; ignore i960_DEN and watchdog
1	1	Extinguish Run LED; ignore i960_DEN and watchdog

Table A-10. Board ID register[1]

Bit 7	Bit 6	Bit 5	Bit 4	Description
0	0	0	0	Reserved
0	0	0	1	SPIRIT-6000 CompactPCI
0	0	1	0	Reserved
0	0	1	1	SPIRIT-6020 Dual PCI
0	1	0	0	SP6040 with PCI-DSP interrupt routed to local PCI ~INTA
0	1	0	1	SP6040 with PCI-DSP interrupt routed to local PCI ~INTB
0	1	1	0	Reserved
0	1	1	1	PFS-123, single DSP version of the SP6040
1	x	x	x	Reserved

1 Bits 3:0 indicate the board revision.

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Table A-11. Memory expansion presence detect register

Bit #	Name	Reset value	Description
7	—	N/A	Not used
6	PD7	1	**Refresh mode**: 1b is normal refresh (15.6 mS) or not installed; 0b is extended refresh which is not supported
5:4	PD6:5	11	**Speed**: 00b is 50 nS access time, 11b is 60 nS access time or not installed[1]
3:0	PD4:1	1111	**Memory configuration**: • **1111b**: No module installed • **1011b**: 16 MByte module installed using 4M devices

1 60 nS expansion modules can be used. However, the slower timing is used for both banks of memory. Support for the slower memory timing must be added to the monitor firmware.

Table A-12. CT slot ID register

Bit 4	Bit 3	Bit 3	Bit 1	Bit0	Description
GA4	GA3	GA2	GA1	GA0	These bits contain a binary-coded CT slot ID which is hardwired on the backplane and unique to an individual slot. There can be up to twenty-one CT cards on a given backplane, which accounts for the five bits.

Table A-13. CT shelf ID register

Bit 4	Bit 3	Bit 3	Bit 1	Bit0	Description
SGA4	SGA3	SGA2	SGA1	SGA0	These bits contain a binary-coded CT shelf ID which is hardwired and bussed to each slot on the CT backplane. This value uniquely identifies a backplane segment within a CT system.

Table A-14. Watchdog timer control register

Bit no.	Bit type	Value at reset	Description
0	R/W	0	Level 1 timer enable (1 = enable)[1]
1	R/W	0	Level 2 timer enable (1 = enable)[1]
2–7	N/A	N/A	Not used

1 Before you enable a watchdog timer, you must set the corresponding Watchdog Timer Preset register. Once enabled, the timer interrupts (NMI, level 1 timer) or resets (level 2 timer) the i960, if not reset or strobed via the Watchdog Timer Strobe register before the preset time expires. The level 2 timer is enabled only if the level 1 timer expires and bit 1 (above) is set.

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The Watchdog timer implements a lockout mechanism that prevents the watchdog from being inadvertently enabled. The enable bits of the control register are accessible only after the correct sequence of accesses to the Lockout registers. The sequence is as follows:

1. Write the value of 0x55 to Lockout register A.
2. Write the value of 0xAA to Lockout register B.
3. The enable bits of the control register may now be modified.
4. The write to the control register resets the protection state machine, disallowing accesses without repeating the unlock sequence.

Table A-15. Watchdog lockout register A

Bit no.	Bit type	Value at reset	Description
7–0	WO	N/A	Lockout register A contents

Table A-16. Watchdog lockout register B

Bit no.	Bit type	Value at reset	Description
7–0	WO	N/A	Lockout register B contents

Table A-17. Watchdog timer level *n* preset register

Bit no.	Bit type	Value at reset	Description
0	R/W	1	Level *n* timer preset bit 0[1]
1	R/W	1	Level *n* timer preset bit 1
2	R/W	1	Level *n* timer preset bit 2
3	R/W	1	Level *n* timer preset bit 3
4	R/W	1	Level *n* timer preset bit 4
5	R/W	1	Level *n* timer preset bit 5
6–7	N/A	N/A	Not used

[1] LSB weight is 62.9mS. Each timer returns to its preset value when reset or strobed via the Watchdog Timer Strobe register, and starts counting if enabled in the Watchdog Timer Control register.

Table A-18. Watchdog timer level *n* output register

Bit no.	Bit type	Value at reset	Description
0	RO	0	Level *n* timer output bit 0
1	RO	0	Level *n* timer output bit 1
2	RO	0	Level *n* timer output bit 2
3	RO	0	Level *n* timer output bit 3
4	RO	0	Level *n* timer output bit 4
5	RO	0	Level *n* timer output bit 5
6–7	N/A	N/A	Not used

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Table A-19. Watchdog timer strobe register

Bit no.	Bit type	Value at reset	Description
0	WO	N/A	Watchdog reset/strobe. A value of one indicates reset. Bit is self clearing.[1]
1–7	N/A	N/A	Not used

1 Resets both timers to preset value.

i960RD local bus DRAM

The SP6040 is populated with one or two banks of non-interleaved, Extended Data Out (EDO), single-wait-state DRAM. The on-board bank is 16 Mbytes using eight 4Mx4 devices.

One additional bank is supported with an optional (build time option) 72-pin SODIMM socket. This socket can support one 16 MByte memory module packaged as a 72 pin SODIMM. Device support on all memory banks is limited to symmetrically addressed memories (for example, 11 rows x 11 columns).

The minimum configuration is 16 Mbytes (1 bank) and the maximum is 32 Mbytes (2 banks).

Table A-20. i960RD DRAM configuration and timing

Register name	Register address	Set value	Description
DBCR	0000 151Ch	0000 0B4Dh	DRAM Bank Control Register
DBAR	0000 1520h	A000 0000h	DRAM Base Address Register
DRWS	0000 1524h	0000 0001h	DRAM Read Wait State Register
DWWS	0000 1528h	0000 0000h	DRAM Write Wait State register
DRIR	0000 152Ch	0000 0204h	DRAM Refresh Interval register (15.6 ms refresh interval)
DPER	0000 1530h	0000 0000h	DRAM Parity Enable register (no parity)

C6201 registers and memory map

C6201 DSP host port interface

The entire memory space of the C6201 DSP can be accessed via the C6201 Host Port Interface (HPI). The detailed workings of this interface are given in chapter 5 of the *TMS320C6201/C6701 Peripherals Reference Guide*. From a programming viewpoint the HPI is controlled by means of four C6201 internal registers:

- HPIA (HPI address)
- HPID(2) (data and data with post-increment)
- HPIC (control)

The SP6040 maps these registers to PCI memory space through the PLX 9050 device. The PLX 9050 has four unique, local address spaces on the backside of the device, each is used

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to map a specific DSP HPI interface. The entire memory map for the C6201 DSP on the SP6040 can be compressed into a little more than 10 Mbytes. For future expansion, the PCI mapping of the DSPs allocates 16 Mbytes of contiguous memory for each processor.

The C6201 device is initialized at power-up to use Memory Map 1, with internal memory mapped at address 0, as defined in pages 7-2 thru 7-5 of the *TMS320C6201/C6701 Peripherals Reference Guide*. The following table shows the organization of memory for the C6201 DSP:

Table A-21. C6201 memory map

Address start	Address end	Allocation (bytes)	SP6040 size (bytes)	Description
0000 0000h	003F FFFFh	4M	64K	Internal program RAM
0040 0000h	013F FFFFh	16M	512K–1M	External memory interface CE 0, SBSRAM
0140 0000h	017F FFFFh	4M	—	External memory interface CE 1, not used
0180 0000h	0183 FFFFh	256K	256K	Internal Peripheral Bus EMIF registers
0184 0000h	0187 FFFFh	256K	256K	Internal Peripheral Bus DMA Controller registers
0188 0000h	018B FFFFh	256K	256K	Internal Peripheral Bus HPI register
018C 0000h	018F FFFFh	256K	256K	Internal Peripheral Bus MCSP 0 registers
0190 0000h	0193 FFFFh	256K	256K	Internal Peripheral Bus MCSP 1 registers
0194 0000h	0197 FFFFh	256K	256K	Internal Peripheral Bus Timer 0 registers
0198 0000h	019B FFFFh	256K	256K	Internal Peripheral Bus Timer 1 registers
019C 0000h	019F FFFFh	256K	256K	Internal Peripheral Bus Interrupt Select registers
01A0 0000h	01FF FFFFh	6M	—	Internal peripheral bus; reserved
0200 0000h	02FF FFFFh	16M	4M	External memory interface CE 2, SDRAM bank
0300 0000h	03FF FFFFh	16M	—	External memory interface CE 3, not used
8000 0000h	8000 FFFFh	4M	64K	Internal data RAM

Table A-22. C6201 EMIF configuration

Register name	Register address	Set value	Description
EMIF global control	0180 0000h	0000 30E8h	
EMIF CE1 space control	0180 0004h	0000 0000h	8-bit ROM (disabled)
EMIF CE0 space control	0180 0008h	0000 0040h	SBSRAM (disabled)
EMIF CE2 space control	0180 0010h	0000 0030h	SDRAM

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Table A-22. C6201 EMIF configuration

Register name	Register address	Set value	Description
EMIF CE3 space control	0180 0014h	0000 0000h	SDRAM (disabled)
EMIF SDRAM control	0180 0018h	0722 9000h	INIT enabled
EMIF SDRAM refresh period	0180 001Ch	0000 016Ah	

Table A-23. DSP MCSP configuration

C6201 register name	Offset (MCSP0, MCSP1)	Register description	Set value
PCR	0x018C0024 0x01900024	Pin Control register	0000 0000 0000 0000 0000 1111 0xxx 0000 b
SRGR	0x018C0014 0x01900014	Sample Rate Generator register	1001 xxxx xxxx xxxx 0000 0000 0000 0000 b
RCR	0x018C000C 0x0190000C	Receive Control register	xxxx xxxx xxxx xx01 xxxx xxxx xxxx xxxx b
XCR	0x018C0010 0x01900010	Transmit Control register	xxxx xxxx xxxx xx01 xxxx xxxx xxxx xxxx b

Table A-24. C6201 reset register

Bit number	Bit type	Value at reset	Description
0	R/W	1	~C6X_RSTA: ORed with PLX local bus reset to drive DSPA hardware reset. Write a zero to remove reset condition.
1	R/W	1	~C6X_RSTB: ORed with PLX local bus reset to drive DSPB hardware reset. Write a zero to remove reset condition.
2	R/W	1	~C6X_RSTC: ORed with PLX local bus reset to drive DSPC hardware reset. Write a zero to remove reset condition.
3	R/W	1	~C6X_RSTD: ORed with PLX local bus reset to drive DSPD hardware reset. Write a zero to remove reset condition.

Table A-25. C6201 interrupt status register

Bit number	Bit type	Value at reset	Description
0	RO	0	~C6X_HINTA detected
1	RO	0	~C6X_HINTB detected
2	RO	0	~C6X_HINTC detected
3	RO	0	~C6X_HINTD detected

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Table A-26. C6201 PCI address map

Address range	Size	Function
Note: All offsets are referenced to the assigned PCI Base Address register for the device.		
0000 0000h to 000F FFFFh	1M	DSPX internal program memory
0010 0000h to 002F FFFFh	2M	DSPX external memory interface CE 0, synchronous burst SRAM
0030 0000h to 0033 FFFFh	256K	DSPX internal peripheral bus EMIF registers
0034 0000h to 0037 FFFFh	256K	DSPX Internal Peripheral Bus DMA Controller registers
0038 0000h to 003B FFFFh	256K	DSPX Internal Peripheral Bus HPI register
003C 0000h to 003F FFFFh	256K	DSPX Internal Peripheral Bus MCSP 0 registers
0040 0000h to 0043 FFFFh	256K	DSPX Internal Peripheral Bus MCSP 1 registers
0044 0000h to 0047 FFFFh	256K	DSPX Internal Peripheral Bus Timer 0 registers
0048 0000h to 004B FFFFh	256K	DSPX Internal Peripheral Bus Timer 1 registers
004C 0000h to 004F FFFFh	256K	DSPX Internal Peripheral Bus Interrupt Select registers
0050 0000h to 00CF FFFFh	8M	DSPX external memory interface CE 2, synchronous DRAM bank
00D0 0000h to 00DF FFFFh	1M	DSPX internal data memory
00E0 0000h to 00EF FFFFh	1M	DSPX HPI registers: • HPI Data = 00Ex_xxx0 (with auto increment) • HPI Data = 00Ex_xxx4 (without auto increment) • HPI Control = 00Ex_xxx8 • HPI Address = 00Ex_xxxC
00F0 0000h to 00FF FFFFh	1M	PLD internal registers[1]: • Global C6201 Reset register = 00Fx_xxx0 • Global Interrupt Status register = 00Fx_xxx4

1 Access to these registers is provided within all four DSP memory spaces.

Hot Swap control and status register

The Hot Swap Control and Status register is accessed using the ECP mechanism in PCI configuration space. The register resides at offset EEh and is described in the following table.

Table A-27. Hot Swap control and status register

Bit number	Bit name	R/W	Description
0	Reserved	R	Reserved, read as 0
1	ENUM_MASK (EIM)	R/W	~ENUM interrupt mask
2	Reserved	R	Reserved, read as 0

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Table A-27. Hot Swap control and status register

Bit number	Bit name	R/W	Description
3	LSTAT CTL (LOO)	R/W	Local status and LED control; 0 = l_stat is tri-state (default/reset) 1 = 21554 is enabled to drive 1_stat
5:4	Reserved	R	Reserved, read as 0
6	REM STAT (EXT)	R/W1TC	Removal status, set to a 1 by the 21554 when 1_stat is sampled high with reset active. This bit drives the p_enum_1 signal on the PCI bus.
7	INS STAT (INS)	R/W1TC	Insertion status, set to a 1 by the 21554 when the serial pre-load has completed and the Primary Configuration Lockout bit is cleared. This bit drives the p_enum_1 signal on the PCI bus.

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B Connectors, headers, and jumpers

This chapter details the connectors and jumpers used by the SP6040 and gives the signal pin-out of each connector.

When reading this file online, you can immediately view information about any connetor by placing the mouse cursor over a connector name and clicking.

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C6201 JTAG emulation header	63
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Connector locations

Figure B-1 shows the positions of LED indicators, connectors, and the PMC cutout. Figure B-2 shows the board outline, with the placement of connectors, jumpers, and major components.

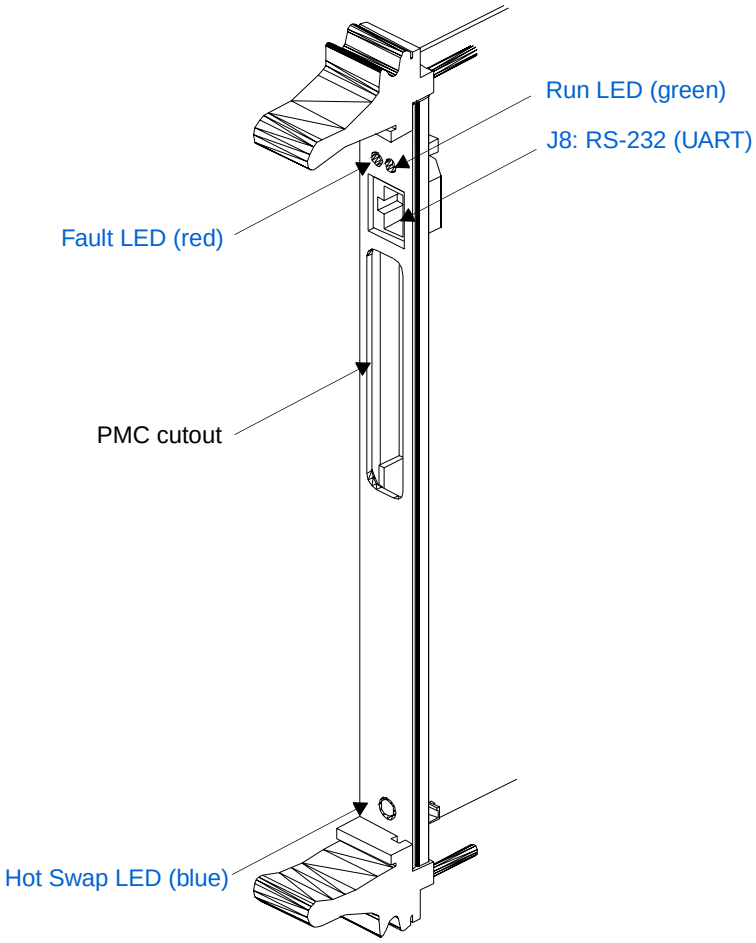


Figure B-1. SP6040 front panel connectors

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When reading this file online, you can immediately view information about any connetor by placing the mouse cursor over a connector label and clicking

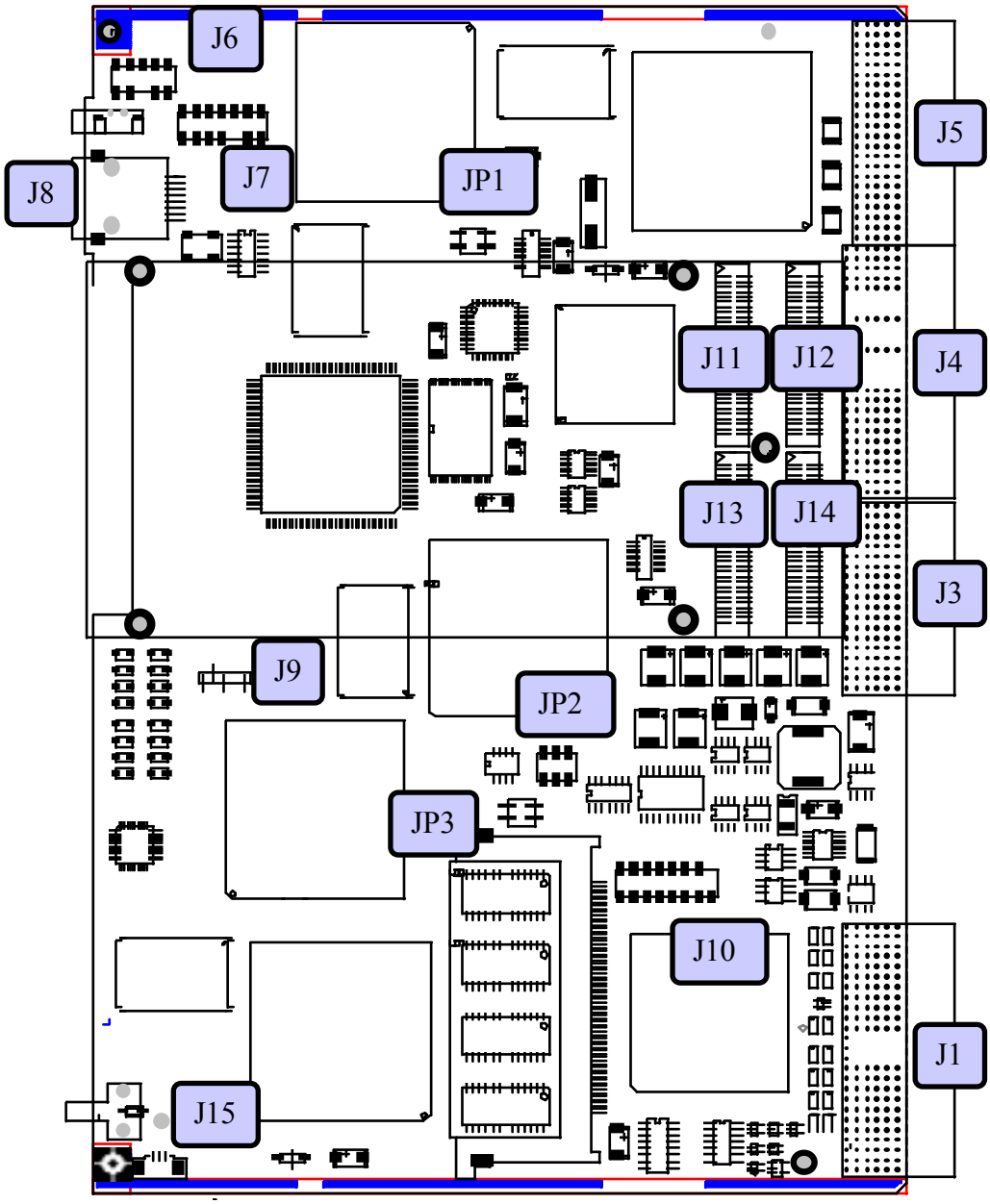


Figure B-2. SP6040 module layout (component side)

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CompactPCI connectors (J1–J5)

CompactPCI connectors include:

- J1 connector: 32-bit CompactPCI interface
- J2: Unused and not populated
- J3 connector: Ethernet interface
- J4 connector: TDM bus interface
- J5 connector: analog telecom I/O

J1 connector: 32-bit CompactPCI interface

Connector pin lengths are denoted by table cell shading as follows:

Short pins

Medium pins

Long pins

Table B-1. CompactPCI J1 connector: 32-bit CompactPCI interface

Pos #	Row A	Row B	Row C	Row D	RowE	Row F
25	5V	~REQ64	~ENUM	3.3V	5V	GND
24	AD1	5V	V(I/O)	AD0	~ACK64	GND
23	3.3V	AD4	AD3	5V	AD2	GND
22	AD7	GND	3.3V	AD6	AD5	GND
21	3.3V	AD9	AD8	GND (M663N)	C/~BE0	GND
20	AD12	GND	V(I/O)	AD11	AD10	GND
19	3.3V	AD15	AD14	GND	AD13	GND
18	~SERR	GND	3.3V	PAR	C/~BE1	GND
17	3.3V	SDONE	~SBO	GND	~PERR	GND
16	~DEVSEL	GND	V(I/O)	~STOP	~LOCK	GND
15	3.3V	~FRAME	~IRDY	~BD_SEL	~TRDY	GND
12–14	Key area					
11	AD18	AD17	AD16	GND	C/~BE2	GND
10	AD21	GND	3.3V	AD20	AD19	GND
9	C/~BE3	IDSEL	AD23	GND	AD22	GND
8	AD26	GND	V(I/O)	AD25	AD24	GND
7	AD30	AD29	AD28	GND	AD27	GND
6	~REQ	GND	3.3V	PCI.CLK	AD31	GND
5	BRSV	BRSV	PCI~RST	GND	~GNT	GND
4	BRSV	~HEALTHY	V(I/O)	NC (INTP)	NT (INTS)	GND
3	~INTA	~INTB	~INTC	5V	~INTD	GND
2	NC (TCK)	5V	NC (TMS)	NC (TDO)	NC (TDI)	GND
1	5V	–12V	NC (~TRST)	+12V	5V	GND

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J3 connector: Ethernet interface

This connector supports 10/100 Base-TX Ethernet.

Pin assignments

Pin	Description
ENETx_TDx	Ethernet transmit pair
ENETx_RDx	Ethernet receive pair
I2C_CLK/DATA_A	I2C bus for T1/E1 port 1-4 (front card PMC 0) status LEDs
I2C_CLK/DATA_B	I2C bus for T1/E1 port 5-8 (front card PMC 1) status LEDs
I2C_CLK/DATA_C	I2C bus for Ethernet link status LEDs

Pinout

Table B-2. CompactPCI J3 connector: Ethernet interface

Pos #	Row A	Row B	Row C	Row D	RowE	Row F
19	NC	NC	NC	NC	NC	GND
18	NC	NC	NC	NC	NC	GND
17	NC	NC	NC	NC	NC	GND
16	NC	NC	NC	NC	NC	GND
15	NC	NC	NC	NC	NC	GND
14	NC	NC	NC	NC	NC	GND
13	NC	NC	NC	NC	NC	GND
12	NC	NC	NC	NC	NC	GND
11	NC	GND	NC	GND	NC	GND
10	NC	GND	NC	GND	NC	GND
9	GND	ENETA_RD+	GND	ENETA_TD+	GND	GND
8	GND	ENETA_RD–	GND	ENETA_TD–	GND	GND
7	NC	GND	NC	GND	NC	GND
6	NC	GND	NC	GND	NC	GND
5	GND	ENETB_RD+	GND	ENETB_TD+	GND	GND
4	GND	ENETB_RD–	GND	ENETB_TD–	GND	GND
3	12C_CLK_C	GND	NC	GND	12C_DATA_C	GND
2	12C_DATA_A	GND	NC	GND	12C_CLK_B	GND
1	12C_CLK_A	NC	NC	NC	12C_DATA_B	GND

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J4 connector: TDM bus interface

This connector supports ECTF H.110 compliant bussed telecom signals.[1]

Pin assignments

Pin	Description
CT_name	H.110 TDM bus signals.
VIO	I/O cell power.
/CT_EN	Last make TDM enable signal for TDM hot swap.
/CT_Reset	Repeated PCI reset to the J4-only CT front cards.
+5V	+5V power.
+3.3V	+3.3V power.
GND	Logic ground.
FG	Frame ground.
RSVD	Reserved for future bussed signals.
NP	A pin and pad REQUIRED to be depopulated to meet safety regulations.
SELVbat	Short loop battery (36V or less).
SELVbatRtn	Short loop battery return.
-Vbat	Telecom power distribution bus.
-VbatRtn	Return bus pin for -Vbat.
SGA0-SGA4	Shelf enumeration bus bits; allows enumeration for up to 32 sub-racks.
GA0-GA4	Geographical address signals- not bussed; allows for up to 32 slots.
VRG	Bus for ringing voltage (single-ended feed *or* ½ of balanced ringing).
VRGRtn	Bus for ringing voltage (return for single-ended ringing applied to VRG or ½ of balanced ringing applied between VRG and VRGRtn).
IN/C	A pin that is REQUIRED to be unconnected to meet safety requirements.
Key area	Area used for key.

1. *CompactPCI Computer Telephony Specification.*

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Pinout

Connector pin lengths are denoted by table cell shading as follows:

- Short pins
- Medium pins
- Long pins

Table B-3. CompactPCI J4 connector: TDM bus interface[1]

Pos #	Row A	Row B	Row C	Row D	RowE	Row F
25	SR4	SR3	SR2	SR1	SR0	FG
24	GA4	GA3	GA2	GA1	GA0	FG
23	+12V	/CT_Reset	/CT_EN	–12V	NC (CT_MC)	FG
22	RSVD	RSVD	RSVD	RSVD	RSVD	FG
21	NC(–SELVbat)	RSVD	RSVD	RSVD	NC (–SELVbatRtn)	FG
20	NP	NP	NP	NP	NP	NP
19	NP	NP	NP	NP	NP	NP
18	NC(VRG)	IN/C	IN/C	IN/C	NC(VRGRtn)	NP
17	NP	NP	NP	NP	NP	NP
16	NP	NP	NP	NP	NP	NP
15	NC(–Bvat)	IN/C	IN/C	IN/C	NC(–VbatRtn)	NP
12–14	Key area					
11	CT_D29	CT_D30	CT_D31	V(I/O)	/CT_FRAME_A	GND
10	CT_D27	+3.3V	CT_D28	+5V	/CT_FRAME_B	GND
9	9CT_D24	CT_D25	CT_236	GND	/FR_COMP	GND
8	CT_D21	CT_D22	CT_D23	+5V	CT_C8_A	GND
7	CT_D19	+5V	CT_D20	GND	CT_C8_B	GND
6	CT_D16	CT_D17	CT_D18	GND	CT_NETREF_1	GND
5	CT_D13	CT_14	CT_15	+3.3V	CT_NETREF_2	GND
4	CT_D11	+5V	CT_D12	+3.3V	SCLK	GND
3	CT_D8	CT_D9	CT_10	GND	SCLKx2	GND
2	CT_D4	CT_D5	CT_D6	CT_D7	GND	GND
1	CT_D0	+3.3V	CT_D1	CT_D2	CT_D3	GND

1 *CompactPCI Computer Telephony Specification*

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J5 connector: analog telecom I/O

This connector interfaces with the physical layer (E1/T1). It is a TNV1-SELV qualified, 4-wire interface.

Pin assignments

Pin	Description
TX*n*_T	Transmit tip.
TX*n*_R	Transmit ring.
RX*n*_T	Receive tip.
RX*n*_R	Receive ring.
IN/C	No-connect required for safety agency insulation requirements.
+*n*V_FT	Positive supply voltage feed-through from CT front card.
–*n*V_FT	Negative supply voltage feed-through from CT front card.
GND_FT	Logic ground feed-through from CT front card.
NP	A position required to be not populated (for example, no conductive element present).
Ui*n*	Universal input - user-defined input signal (input to CT front card).
Uo*n*	Universal output - user-defined output signal (output from CT front card).

Pinout

Table B-4. CompactPCI J5 connector: analog telecom I/O*

Pos #	Row A	Row B	Row C	Row D	RowE	Row F
22	TX1_T	NC(TX5_T)	NC(TX9_T)	IN/C	IN/C	NP
21	TX1_R	NC(TX5_R)	NC(TX9_R)	IN/C	IN/C	NP
20	RX1_T	NC(RX5_T)	NC(RX9_T)	IN/C	IN/C	NP
19	RX1_R	NC(RX5_R)	NC(RX9_R)	IN/C	IN/C	NP
18	TX2_T	NC(TX6_T)	NC(TX10_T)	IN/C	IN/C	NP
17	TX2_R	NC(TX6_R)	NC(TX10_R)	IN/C	IN/C	NP
16	RX2_T	NC(RX6_T)	NC(RX10_T)	IN/C	IN/C	NP
15	RX2_R	NC(RX6_R)	NC(RX10_R)	IN/C	IN/C	NP
14	TX3_T	NC(TX7_T)	NC(TX11_T)	IN/C	IN/C	NP
13	TX3_R	NC(TX7_R)	NC(TX11_R)	IN/C	IN/C	NP
12	RX3_T	NC(RX7_T)	NC(RX11_T)	IN/C	IN/C	NP
11	RX3_R	NC(RX7_R)	NC(RX11_R)	IN/C	IN/C	NP
10	TX4_T	NC(TX8_T)	NC(TX12_T)	IN/C	IN/C	NP
9	TX4_R	NC(TX8_R)	NC(TX12_R)	IN/C	IN/C	NP
8	RX4_T	NC(RX8_T)	NC(RX12_T)	IN/C	IN/C	NP
7	RX4_R	NC(RX8_R)	NC(RX12_R)	IN/C	IN/C	NP
6	IN/C	IN/C	IN/C	IN/C	IN/C	NP
5	IN/C	IN/C	IN/C	IN/C	IN/C	NP
4	Uo0	Uo1	GND_FT	GND_FT	GND_FT	NP
3	Ui0	Ui1	Uo4	Uo5	Uo6	NP

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Table B-4. CompactPCI J5 connector: analog telecom I/O*

Pos #	Row A	Row B	Row C	Row D	RowE	Row F
2	Uo2	Uo3	Ui4	Ui5	Ui6	NP
1	Ui2	Ui3	+5V_FT	+12V_FT	–12V_FT	NP

PMC connectors (J11–J14)

Table B-5. PMC J11 connector: 32-bit PCI interface

Pos#	Signal	Pos#	Signal
1	–	2	–12V
3	GND	4	PCI.~IRQA
5	PCI.~IRQB	6	PCI.~IRQC
7	~BUSMODE1	8	+5V
9	PCI.~IRQD	10	–
11	GND	12	–
13	PCLKS1	14	GND
15	GND	16	PMC.~GNT
17	PMC.~REQ	18	+5V
19	+5V	20	PCI.AD31
21	PCI.AD28	22	PCI.AD27
23	PCI.AD25	24	GND
25	GND	26	PCI.C/~BE3
27	GND	28	PCI.B/~BE3
29	PCI.AD22	30	PCI.AD21
31	+5V	32	PCI.AD17
33	PCI.~FRAME	34	GND
35	GND	36	PCI.~IRDY
37	PCI.~DEVSEL	38	+5V
39	GND	40	PCI.~LOCK
41	PMC.~SDONE	42	PMC.~SBO
43	PCI.PAR	44	GND
45	+5V	46	PCI.AD15
47	PCI.AD12	48	PCI.AD11
49	PCI.AD9	50	+5V
51	GND	52	PCI.C/~BE0
53	PCI.AD6	54	PCI.AD5
55	PCI.AD4	56	GND
57	+5V	58	PCI.AD3
59	PCI.AD2	60	PCI.AD1
61	PCI.AD0	62	+5V
63	GND	64	–

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Table B-6. PMC J12 connector: 32-bit PCI interface

Pos#	Signal	Pos#	Signal
1	+12V	2	–
3	–	4	–
5	–	6	GND
7	GND	8	–
9	–	10	+3.3V
11	BUSMODE2~	12	BUSMODE3~
13	PCI.~RST	14	BUSMODE4~
15	+3.3V	16	GND
17	–	18	PCI.~AD29
19	PCI.AD30	20	PCI.~AD26
21	GND	22	+3.3V
23	PCI.AD24	24	PCI.~AD23
25	IDSEL1(PCI.AD16)	26	PCI.~AD23
27	+3.3V	28	PCI.~AD20
29	PCI.AD18	30	GND
31	PCI.AD16	32	PCI.C/~BE2
33	GND	34	–
35	PCI.~TRDY	36	+3.3V
37	GND	38	PCI.~STOP
39	PCI.~PERR	40	GND
41	+3.3V	42	PCI.~SERR
43	PCI.C/~BE1	44	GND
45	PCI.AD14	46	PCI.AD13
47	GND	48	PCI.AD10
49	PCI.AD8	50	+3.3V
51	PCI.AD7	52	–
53	+3.3V	54	–
55	–	56	GND
57	–	58	–
59	GND	60	–
61	–	62	+3.3V
63	GND	64	–

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Table B-7. PMC J13 connector: TDM stream/Ethernet interface

Pos#	Signal	Pos#	Signal
1	IO_TXD1	2	EARLY_5V
3	NC	4	IO_RXD1
5	IO_TXD2	6	IO_RXD2
7	IO_TXD3	8	NC
9	IO_TXD4	10	IO_RXD3
11	GND	12	IO_RXD4
13	IO_TXD5	14	GND
15	NC	16	IO_RXD5
17	IO_TXD6	18	NC
19	NC	20	IO_RXD6
21	IO_TXD7	22	IO_RXD7
23	IO_TXD8	24	NC
25	NC	26	IO_RXD8
27	NC	28	NC
29	L_REF0	30	NC
31	Not used	32	Not used
33	PMCTCLK0	34	GND
35	I2C_CLK_A	36	I2C_DATA_A
37	L_REF1	38	NC
39	GND	40	NC
41	I2C_DATA_B	42	I2C_CLK_B
43	L_REF2	44	NC
45	ENETA_TD+	46	ENETA_TD–
47	ENETA_RD+	48	H_LSC3
49	L_REF3	50	ENETA_RD–
51	GND	52	IO_TFS1
53	ENETB_TD+	54	ENETB_TD–
55	NC	56	GND
57	ENETB_RD+	58	IO_CLK1
59	NC	60	ENETB_RD–
61	NC	62	NC
63	GND	64	NC

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Table B-8. PMC J14 connector: telecom I/O, local bus interface

Pos#	Signal	Pos#	Signal
1	NC	2	TX3_T
3	TX1_T	4	TX3_R
5	TX1_R	6	GND
7	GND	8	RX3_T
9	RX1_T	10	RX3_R
11	RX1_R	12	NC
13	TX2_T	14	TX4_T
15	NC	16	TX4_R
17	TX2_R	18	GND
19	RX2_T	20	RX4_T
21	NC	22	RX4_R
23	RX2_R	24	NC
25	D0	26	D1
27	NC	28	D3
29	D2	30	NC
31	D4	32	D5
33	GND	34	D7
35	D6	36	ALT_TDI
37	ALT_TMS	38	~CE1
39	MA2	40	ALT_TDO
41	ALT_TCK	42	GND
43	MA4	44	GND
45	MA6	46	MA0
47	GND	48	MA1
49	MA8	50	NC
51	BE~0	52	MA3
53	BE~1	54	MA5
55	W/~R	56	GND
57	~E1/T1_INT	58	MA7
59	GND	60	LA21
61	IO_CLK	62	LA15
63	~LRST	64	LA14

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Front panel connectors

J8: RS-232 (UART)

This RJ-45 connector makes the RS-232 interface available through the module's front panel as a debug port (for running diagnostics) or for downloading applications:

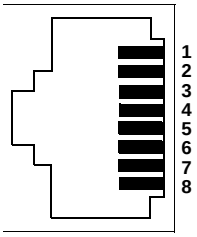


Table B-9. J8 connector: RS-232 interface

Pin	Signal	Pin	Signal
1	No connect	5	Receive data
2	No connect	6	Request to send
3	Ground	7	Clear to send
4	Transmit data	8	No connect

Headers

You must remove the board from the chassis to access these headers. These interfaces are not directly accessible from either the front or rear panel.

Audio monitor header

This 5-pin single-row header is used to connect the CODEC to audio input and output signals:

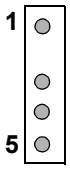


Table B-10. Audio monitor connector (J9)

Pin	Signal	Pin	Signal
1	Audio out	4	Audio in
2	Key	5	Ground
3	Ground		

C6201 JTAG emulation header

This 14-pin dual-row header is brought out for DSP JTAG emulation use:

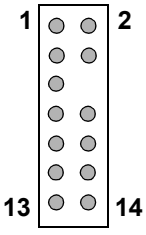


Table B-11. DSP JTAG interface connector (J7)

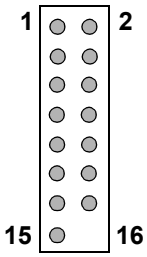
Pin	Signal	Pin	Signal
1	DSP TMS	2	DSP TRST-
3	DSP TDI	4	GND
5	+3.3V	6	KEY
7	DSP TDO	8	GND
9	DSP RET TCLK	10	GND
11	DSP TCLK	12	GND
13	EMU0	14	EMU1

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i960RD JTAG emulation

This interface is available on a 16-pin dual row header (for i960 JTAG emulation use).

Table B-12. i960 JTAG interface connector (J10)

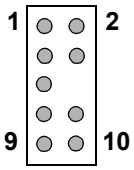


Pin	Signal	Pin	Signal
1	i960 TRST-	2	GND
3	i960 TDI	4	GND
5	i960 TDO	6	GND
7	i960 TMS	8	GND
9	i960 TCK	10	GND
11	ICECLOCK-	12	GND
13	LRST-	14	GND
15	(pulled up)	16	**Key**

Altera EPM7xxxS/ATC (PLD) programming

This interface is available on a 10-pin dual row header (J6) and is used for programming the two AlteraPLDs on the board:

Table B-13. Altera JTAG interface connector (J6)



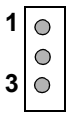
Pin	Signal	Pin	Signal
1	ALT TCK	2	GND
3	ALT TDO	4	+5V
5	ALT TMS	6	KEY
7	N/C	8	N/C
9	ALT TDI	10	GND

Hot Swap header

CompactPCI Hot Swap header

This interface is available on a 3-pin single row header (J15) and is used for connecting the front panel ejector micro switch to the board.)

Table B-14. Hot Swap header (J15)



Pin	Signal
1	HS_STAT
2	N.C.
3	EARLY_+5V

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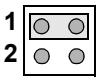
Jumpers

There are six user-configurable jumpers on each SP6040. Board functions controlled by these jumpers include configuration of the audio CODEC stream connection, Flash memory write and Failsafe enables, Altera JTAG chain bypass and RadiSys manufacturing test support.

The jumpers are organized into these blocks:

- **RadiSys manufacturing jumpers (JP1)**: Jumpers JP1-1 and JP1-2 are used only by RadiSys during manufacturing and should remain OPEN for normal operation.

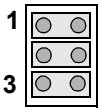
Table B-15. RadiSys manufacturing jumpers (JP1))



Jumper	Signal	Function
JP1-1	~BURNIN	N/A
JP1-2	IMALIVE	N/A

- **Flash control and JTAG bypass jumpers (JP2)**: Jumpers JP2-1 and JP2-2 disable writes to user portions of the Flash ROM, and recover from a corrupted Flash chip, respectively. JP2-3 bypasses the section of the Altera JTAG chain on (uninstalled) PMC module.

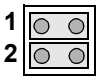
Table B-16. Flash control and JTAG bypass jumpers (JP2)



Jumper	Signal	Function
JP2-1	~ROM WRITE ENABLE	IN = Enable FLASH writes
JP2-2	~FAILSAFE	IN = Recover from corrupted FLASH
JP2-3	Altera JTAG chain	IN = Shunt out PMC section of chain

- **Audio CODEC stream connection (JP3)**.

Table B-17. Audio CODEC stream connection (JP3)



Jumper	Signal	Function
JP3-1	AM_DOUT	Connect audio CODEC stream to the TDM switch
JP3-2	Not used	N/A

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Diagnostic LEDs

Two banks of diagnostic LEDs are provided as shown in the next figure.

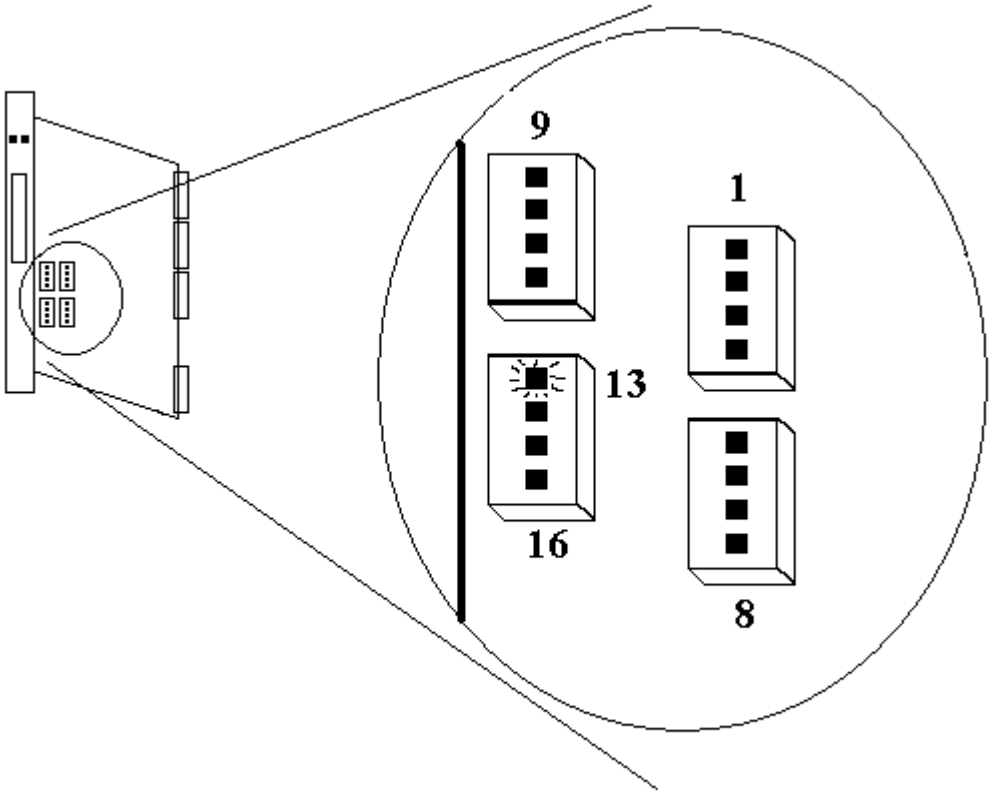


Figure B-3. LEDs: location and numbering convention

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C Diagnostics

This chapter describes the diagnostic software programs included with the SP6040, as shown in the next table.



By default, the diagnostic modules are installed to \SP6KBSP\bin\diags (to the Windows NT root drive).To access these programs, go to your Windows Start menu and select Programs>TASK-6000>SP6k-bsp. A menu similar to the figure at right displays, and lists available diagnostic tests.

From this menu you can access the diagnostic tests as well as reference material, such as guides and manuals. When reading this file online, you can immediately view information about any diagnostic test by placing the mouse cursor over a test name and clicking:

Test	Page
Before you begin	68
POST	69
C6x CODEC diagnostics	71
C6x memory diagnostics	73
Ethernet and HDLC diagnostics	75
i960 memory diagnostics	78
i960 peripheral diagnostics	80
Stream switch diagnostics	83
T1 diagnostics	84



You can also run diagnostics from a Windows NT DOS window using this syntax:

`C:\> rmondb [-pci | -ser COMx] [-g GROUP_ID] [-nop] [-p pass_count] [-dev board_number] diag_name`

where:

-pci or *-ser COMx*
: Indicates PCI or serial connection, respectively.

diag_name
: A diagnostic module name indicated above (for example, `iopmem`).

GROUP_ID
: One of these test groups: MFG, HALT, VISUAL or DEFAULT.

-nop
: Specifies unattended autorun/autoexit.

-dev
: Specifies a target board number (0–7).

-p
: Overrides the default pass count.

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Before you begin

Extended diagnostics are i960 applications which, when run with RMONDB, allow for host-controlled execution of the diagnostics by means of a GUI. RMONDB is a WIN32 console application which contains the diagnostics GUI template. Each diagnostic fills in the template with its list of diagnostics and default input values. The applications communicate with the host via the Monitor's HDI (Host Debugger Interface).

Each diagnostic module includes …\RVGSDK\SP6KBSP\bin\diags*diag_module_name*.hlp, a built-in help file, which you can view in the File Explorer or by pressing the HELP button while running the diagnostic program.

Some diagnostics require external loopback fixtures. These fixtures must be attached *prior* to executing the diagnostic. The next table lists each diagnostic and loopback requirements, if any.

Table C-1. Extended diagnostics

Diagnostic	Module filename	Loopback requirements
C6x memory diagnostics	c6xmem	None
C6x CODEC diagnostics	c6xcodec	Audio port loopback
i960 memory diagnostics	iopmem	None
i960 peripheral diagnostics	iopper	UART loopback (RX ↔ TX)
T8105 stream switch diagnostics	t8100	H.100 Loopback for PCI, H.110 loopback for CompactPCI
E1 or T1 diagnostics	tiowan	E1/T1 loopback cable
Ethernet & HDLC diagnostics	tiolan	Ethernet loopback cable

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Running diagnostic programs

POST

Although not a part of the diagnostic software test suite, the Power-On Self Test (POST) provides information that you can use when troubleshooting problems.

The SPIRIT-60x0 Monitor performs POST diagnostics at initial power-up or upon reset. Extended diagnostics are available to perform more specific and thorough testing of board components.

Power On Self Test (POST) diagnostics are run on Power-up or after a Reset and perform basic verification of the SPIRIT-6000 board. Additional diagnostics may be run in the Monitor environment to perform more thorough testing and/or provide better test coverage or fault isolation. These extended diagnostics are in the form of downloadable applications and must be invoked from a host system.

POST results are stored in these locations:

- In the fixed memory board information structure, SP6K_BOARD_INFO_T, located at offset IOP_FIXED_DATA_OFFSET in IOP local bus memory space. See the SP6K.H board header file for definitions.
- At address 0x3F0 in IOP internal (RAM).

The next figure shows the *post_results* field bit mask definition. Note that the POST complete mask is comprised of the twelve most significant bits.

7	6	5	4	3	2	1	0
T8105 Switch Tests	HPI Register Test	IOP Extended RAM Test	UART_Int. Loopback Test	UART Register Test	QuadWord Memory Test	Walking 1's Memory Test	Monitor Image Checksum

31–20	19–17	16	12–15	11	10	9	8
POST Completed Mask	Reserved	SROM configuration corrupted	Reserved	HDLC / Ethernet Tests	E1/T1 Tests (if present)	C6x BIT Tests	C6x RAM Test via IOP

Figure C-1. POST results bit mask

The serial EEPROM located on the I^2C bus stores board configuration information such as memory sizes and PMC options installed. You can use these commands to access configuration information:

se	set configuration	Saves the current configuration information.
sh	show configuration	Displays current board configuration as detected during power-up. POST uses this configuration information to determine if the memory or PMC option configuration changed due to a failure.

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LEDs

LEDs indicate POST results and progress as well as Monitor status as shown in Table C-2. The LEDs are available in application use for debugging or other purposes.

The SP6040 has two banks of LEDs, with eight LEDs per bank. LEDs of tests which fail POST remain illuminated. For information about LED numbering, see *Appendix B, Connectors, headers, and jumpers*.

The LED Bank registers are located in an 8-bit region of IOP local bus memory as defined by the LED_BANK0_REG and LED_BANK1_REG definitions in the SP6K.H board header file.

Table C-2. LED indicators for POST faults and monitor status

Test	Lit LED:	Indicates:
Pre-init	1	Monitor Flash ROM image checksum failed
	2	Walking One's to IOP Memory Test failed
	3	Quadword IOP Memory test failed
	4	UART Scratch Register Test failed
Post-init	5	UART Internal Loopback failed
	6	IOP Address/Complement Memory Test failed
	7	HPI Register Test failed
	8	T8105 Stream Switch Test failed
	9	C6x RAM Test has failed
	10	C6x BIT has failed
	11	E1/T1 Test failed
	12	HDLC / Ethernet Tests failed
	13	Monitor is listening to the serial port.
	14	Monitor is writing to the serial port.
	15	An application program is being executed.
	16	Monitor is actively transmitting over the PCI "port".

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C6x CODEC diagnostics

This tests the C6x CODEC in both Linear and uLaw mode. The uLaw CODEC test checks the CODEC by using the DSPs as a data source, the T8105 to route the data stream, and a loopback connector placed between the CODEC input and output. Signals to the audio output in some tests may loop back for verification.

When run on the SP6040, the CODEC tests require that jumper JP3-1 be in place to connect AM_DOUT to the T8105. For more information about JP3, see *Appendix B, Connectors, headers, and jumpers*.

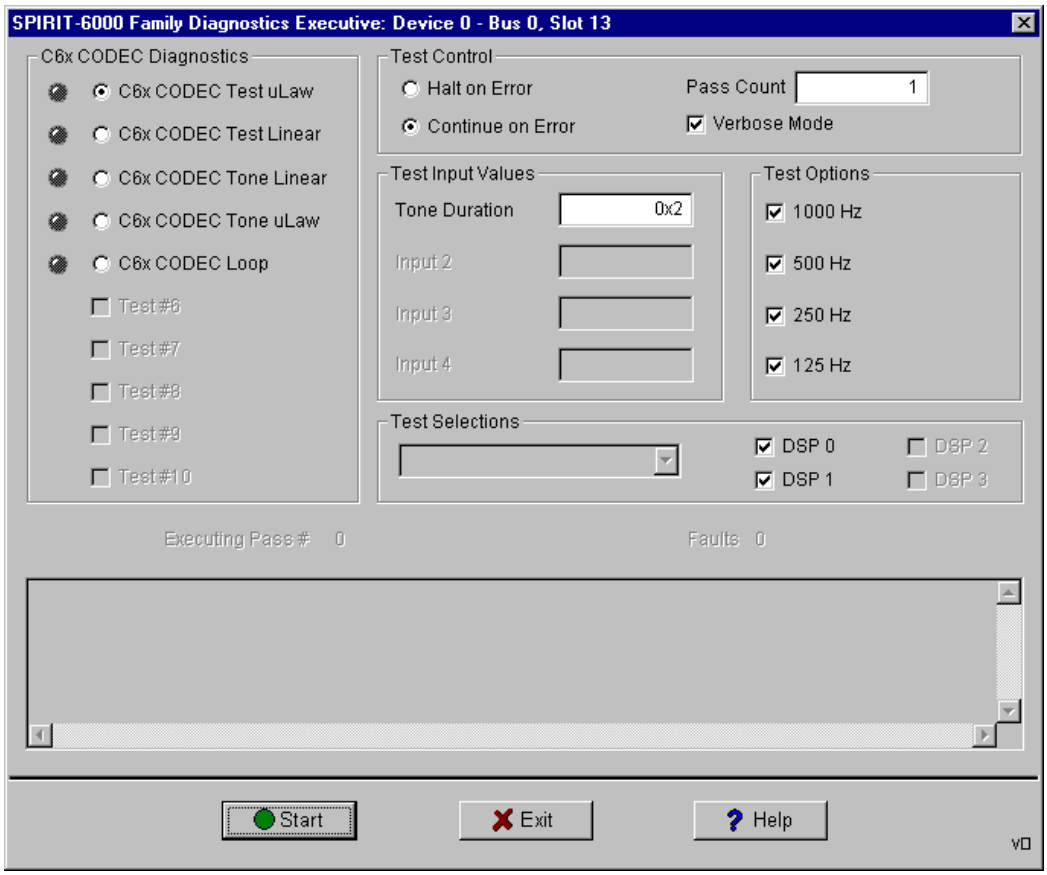


Figure C-2. C6x CODEC diagnostics screen

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Field	Description
C6x CODEC Test uLaw	This test, performed in uLaw mode, does the following: • The DSP creates data that represents sine waves of several different frequencies, then sends the data out MCBSP0. • The T8105 routes the DSP MCBSP0 to CODEC input. • The CODEC converts the data and output the expected sine wave, then receives the sine wave via the loopback connector and converts back to digital. • The T8105 connects the CODEC digital out stream to the DSP MCBSP 0 input. • The DSP evaluates the input data for accuracy and report status to the i960.
C6x CODEC Test Linear	This test, performed in linear mode, does the following: • The DSP creates data that represents sine waves of several different frequencies., then sends the data out MCBSP 0. • The T8105 routes the DSP MCBSP0 to the CODEC input. • The CODEC converts the data and output the expected sine wave, then receives the sine wave via the loopback connector and converts back to digital. • The T8105 connects the CODEC digital out stream to the DSP MCBSP 0 input. The DSP evaluates the input data for accuracy and report status to the i960.
C6x CODEC Tone Linear	Continuously sends a Tone of one of the four selectable frequencies. This test is a debug aid and does not report results. The test runs in linear mode.
C6x CODEC Tone uLAW	Continuously sends a Tone of one of the four selectable frequencies. This test is a debug aid and does not report results. The test runs in uLaw mode.
C6x CODEC Loop	Continuously loops any data received on the analog input to the output. The data may be looped at the T8105 or the DSP. This test is a debug aid and will not report errors.

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C6x memory diagnostics

These tests test the C6x memories. Memory tests originate from both the IOP (via the HPI) and the DSP.

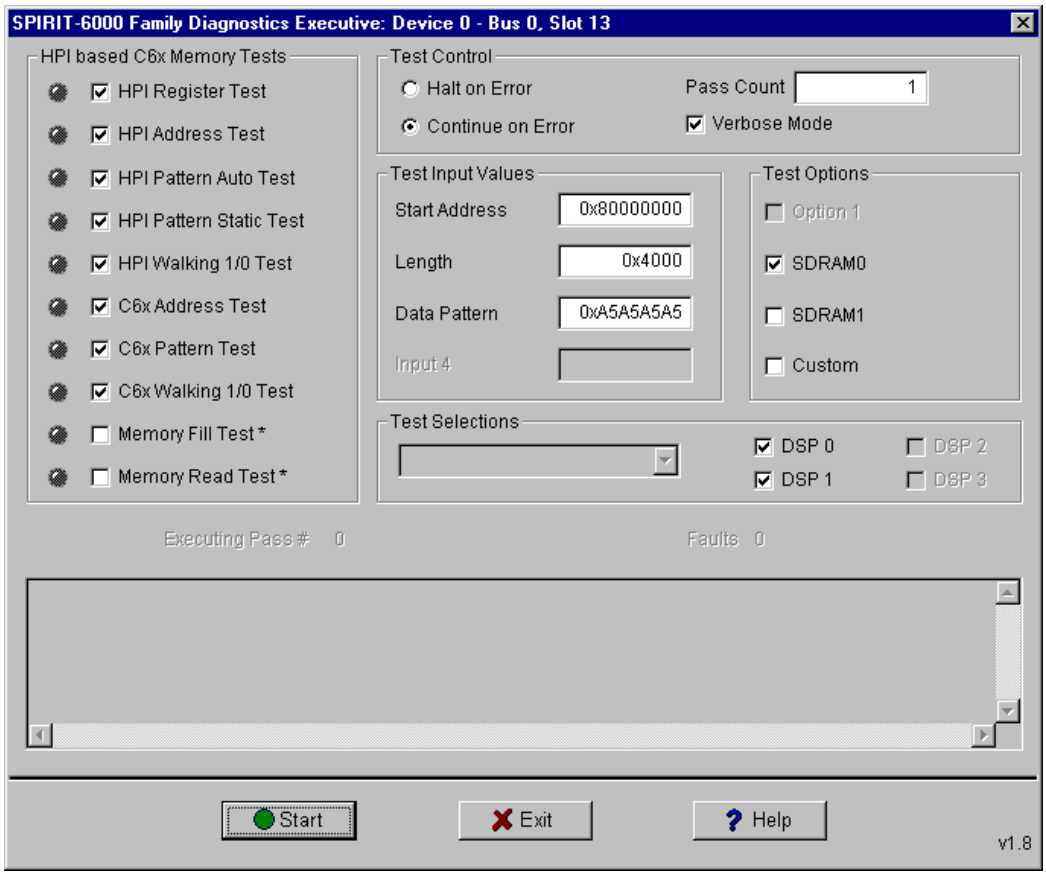


Figure C-3. C6x memory diagnostics screen

Field	Description
HPI Register Test	The HPI register test does a walking one and walking zero test to a register in the Host Port Interface memory mapped region. This test displays the basic ability to communicate with the C6201 from the IOP (i960). This test is not affected by the Options or Input field menus.
HPI Address Test	The HPI Address test does a 32 bit address and complement address test of the specified C6201 memory regions. This test is run on the IOP and test the memory through the HPI. The memory regions tested are selected through the Options menu. The patterns used may not be affected by any menu selections.
HPI Pattern Auto Test	The HPI Pattern test does a set of 32-bit pattern and complement pattern tests to the specified C6x memory regions. The test runs on the IOP and uses the HPI to access C6x memory. The memory regions tested are selected through the Options menu. The patterns used may not be affected by any menu selections.

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Field	Description
HPI Pattern Static Test	To be developed.
HPI Walking I/0 Test	The HPI walking test performs a walking one and a 32 bit walking 0 to the specified C6x memory regions. The test runs on the IOP and uses the HPI to access C6210 memory. The memory ranges tested are selected through the Options menu. The patterns used may not be affected by any menu selections.
C6x Address Test	The C6x Address Test performs a 32 bit address and address complement test to each address in the specified C6201 memory region. The C6201 runs the tests and report the errors to the IOP. The memory regions tested are selected through the Options menu. The patterns used may not be affected by any menu selections.
C6x Pattern Test	The C6x Pattern Test performs a set of tests with a 32 bit pattern and inverted pattern to the specified memory region. The C6201 runs the test and reports the errors to the IOP. The memory regions tested are selected through the Options menu. The patterns used may not be affected by any menu selections.
C6x Walking 1/0 Test	The C6x walking test performs a walking one and a 32 bit walking 0 to the addresses specified. The C6201 runs the tests and reports the results to the IOP. The memory ranges tested are selected through the Options menu.
Memory Fill Test	The Memory Fill Test performs 32 bit writes to the specified C6201 memory region. The memory Fill test ignores the Options menu and uses the Input Fields menu.
Memory Read Test	The Memory Read Test performs a 32-bit read from the specified C6201address. The Memory read menu ignores the Options menu and uses the Input Fields menu.

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Ethernet and HDLC diagnostics

This test detects the presence of one or two ethernet controllers and the GUI allows for selecting any or all of the installed controllers for testing.

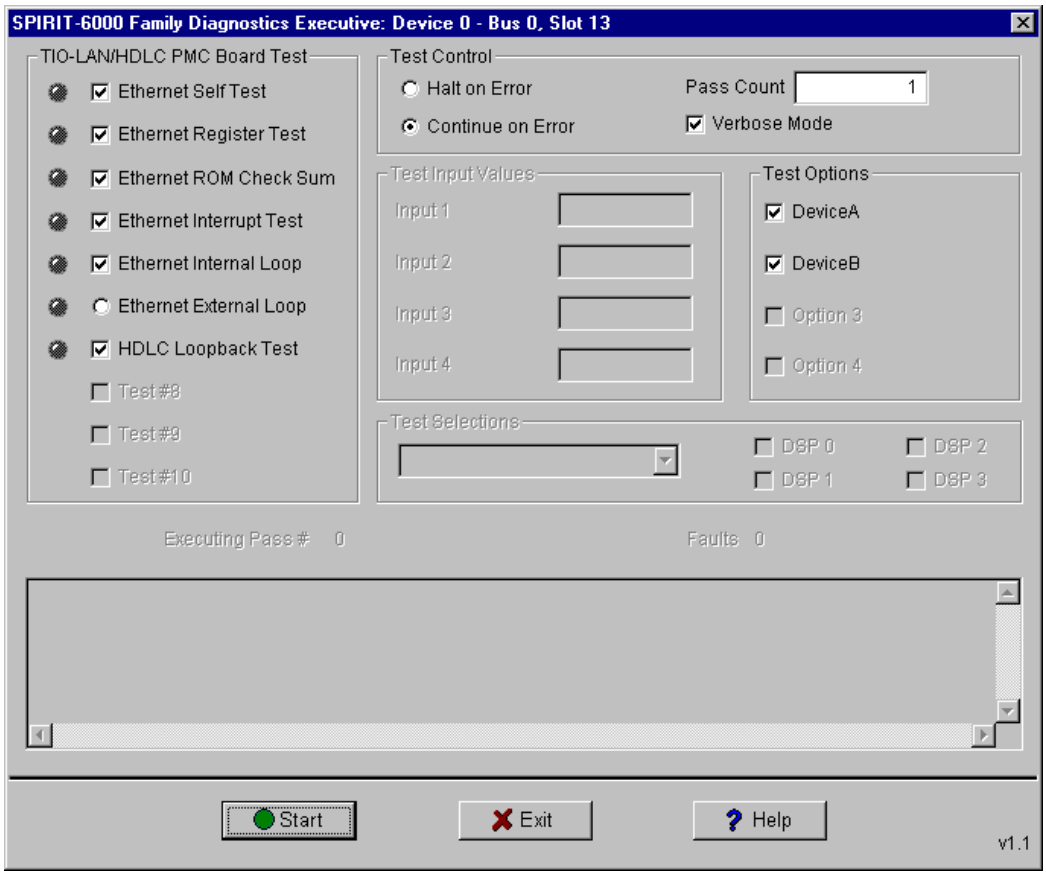


Figure C-4. Ethernet and HDLC diagnostics screen

Field	Description
Ethernet Self Test	The Ethernet controller will be placed into it's selftest mode and the results will be checked by the diagnostic.
Ethernet Register Test	There will be a test of some of the registers of the Ethernet controller PCI interface. A known pattern is writtern to the registers and then verified.
Ethernet ROM Check Sum	The Ethernet Serial Read Only Memory will be checked to make sure that the checksum is valid. The SROM contains some configuration information as well as the unique MAC address of the controller. The checksum is programmed into the device at the time of manufacture.
Ethernet Interrupt Test	The Ethernet controller will be tested to confirm the abillity to inturrupt the i960. The Ethernet controller will be instructed to interrupt the i960, and the i960 will confirm the received interrupt.

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Field	Description
Ethernet Internal Loop	Tests the Ethernet controllers for the ability to send and receive data. The Internal loopback test sets the PHY to loop Transmit port to the Receive port. This test: • Sets up four transmit buffers and four receive buffers on the i960, then fills the transmit buffers with a known pattern. • Commands the RU to receive and commands the SU to send. • Waits for the fourth receive buffer to complete. • Checks data in the receive buffers for accuracy and checks error flags in the receiver and transmitter for status. The Loopback tests are performed at 10 MBPS and 100 MBPS.
Ethernet External Loop	Tests the Ethernet controllers for the ability to send and receive data. The External loopback test configures the PHY to operate in the standard mode. **Note**: A cable is required to loop the data from the Transmit to Receive ports. This test: • Sets up four transmit buffers and four receive buffers on the i960, then fills the transmit buffers with a known pattern. • Commands the RU to receive and commands the SU to send. • Waits for the fourth receive buffer to complete. • Checks data in the receive buffers for accuracy and checks error flags in the receiver and transmitter for status. The Loopback tests are performed at 10 MBPS and 100 MBPS.

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Field	Description
HDLC Loopback Test	The HDLC option of the option module is tested using a loopback through the T8105. The test uses patterns stored in memory on the i960 as the transmit data. After the HDLC controller finishes, the receive buffers on the i960 are verified for accuracy. The Munich 128X uses four separate 32-channel HDLC controllers. • Set up transmit buffers and receive buffers on the i960 • Fill the transmit buffers with a known pattern • Set the T8105 to loop the HDLC Transmit Stream data to the HDLC Receive Stream • Command the HDLC receive unit to receive using i960 buffers • Command the Send Unit to send using i960 buffers • Wait for the completion of the last receive buffer; signaled by an interrupt to the i960 • Check the data in the receiver and transmitter status Repeat for all four internal HDLC controllers

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i960 memory diagnostics

This test allow for extensive testing of the IOP external memories. The tests are restricted to the available memory region (beyond the monitor and diagnostic application).

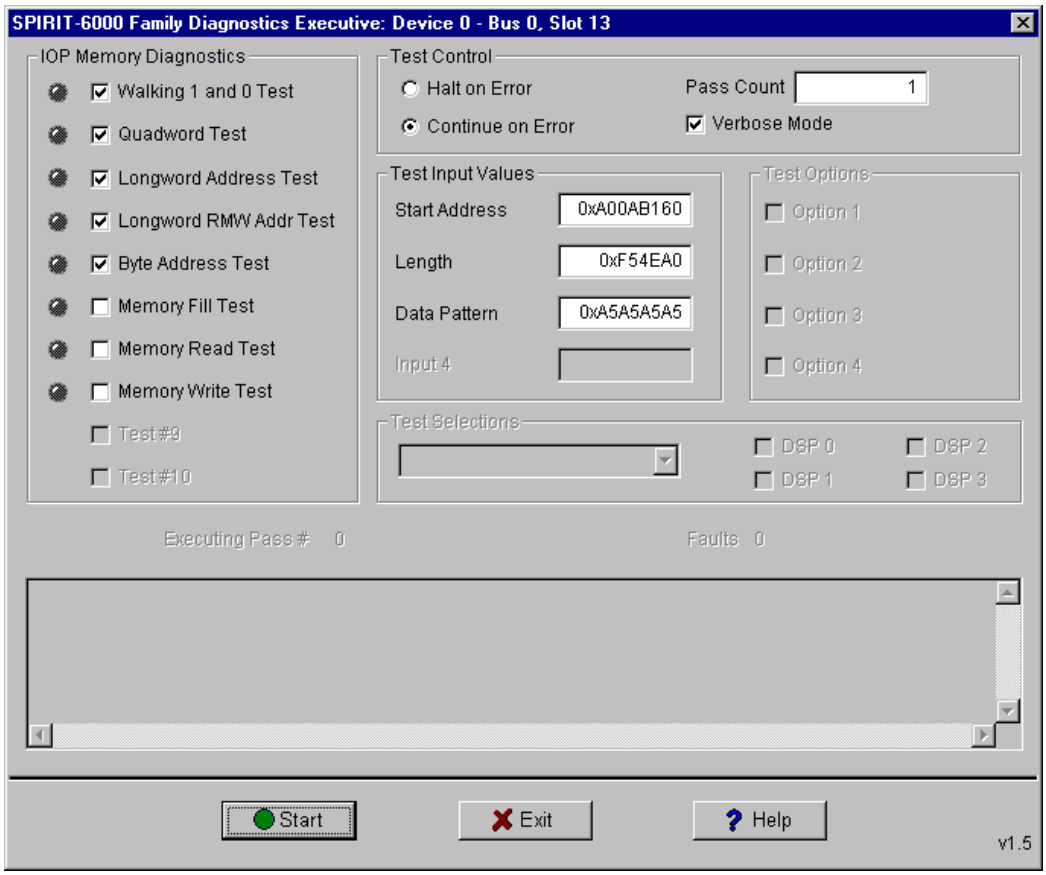


Figure C-5. i960 memory diagnostics screen

Field	Description
Walking 1 and 0 Test	Performs a walking-1s and 0's test to the specified memory region.
Quadword Test	Performs a quadword write/read (128-bit, STQ and LDQ) test to the specified memory region.
Longword Address Test	Performs 32-bit address and address complement tests to the specified memory region.

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Field	Description
Longword RMW Addr Test	Performs 32-bit address and address complement tests with read/modify/write as follows: 1. For the size of the memory test region (word addressing, 4 bytes per address) • Write the unique address less one value to the current address location. • Use “addo” to read the value at the current address, add one and write new value. 2. For the size of the memory test region • Read the value at the current address and compare to current address. 3. Repeat the above procedure using address complement.
Byte Address Test	Byte Address and Byte Address Complement Test to the specified memory region.
Memory Fill Test	This Continuous Write test allows for repeated writes to a specified region in memory.
Memory Read Test	This Continuous Read RAM test allows for repeated reads to a specified address in memory.
Memory Write Test	This Continuous Write test allows for repeated writes to a specified address in memory.

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i960 peripheral diagnostics

These tests The IOP Peripheral Diagnostics allow for thorough testing of several IOP peripherals including the Flash, UART, and LEDs.

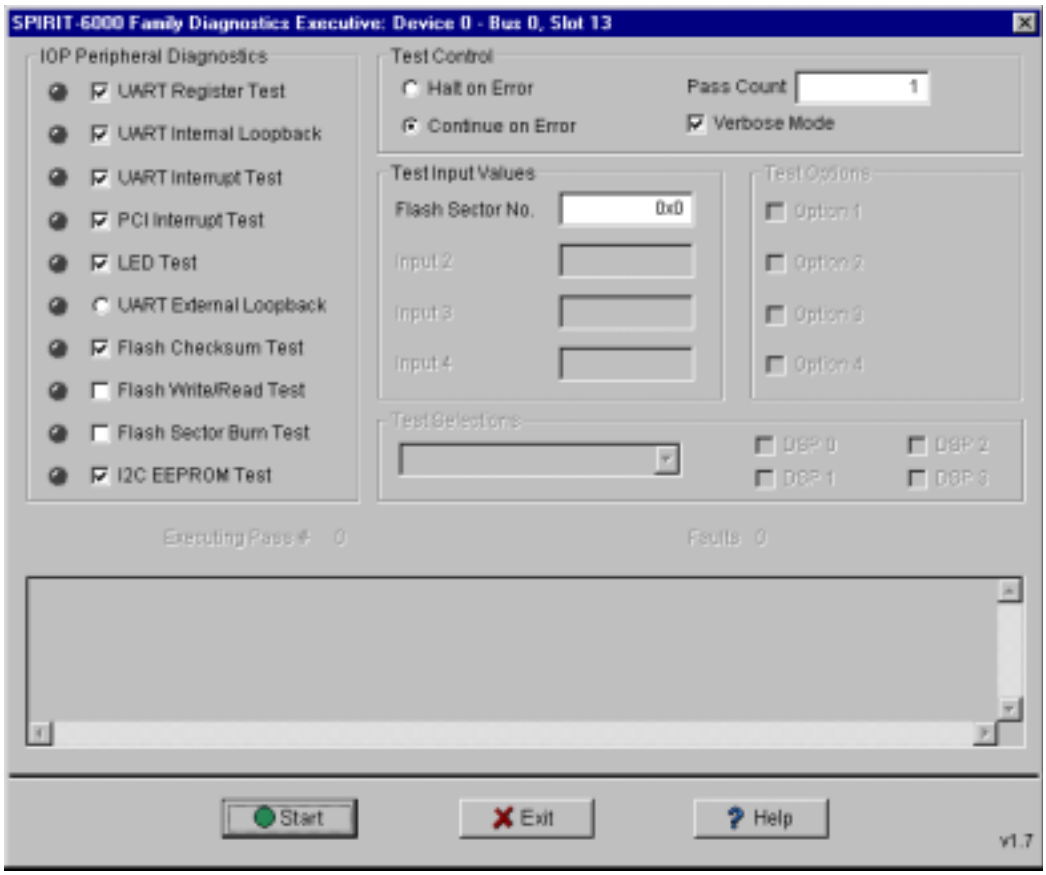


Figure C-6. i960 peripheral diagnostics screen

Test	Description
UART Register Test	This test performs a Walking-1s test to the UART scratch-pad register during which time all eight data lines are written with both 0 and 1.

UART Internal Loopback Test	This test performs the following:
	• Initializes the UART for 9600 bps.
	• Sets the UART to internal loopback mode and performs the loopback test.
	• Transmits the letters of the alphabet:
	  • Sends character and wait for it to loop back.
	  • Verifies that each character is received within timeout period.

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Test	Description
UART Interrupt Test	This test performs the following tasks to verify that the IOP can receive UART (XINT5) interrupts: • Disables UART interrupts. • Initializes and enable UART interrupts. • Sets TX Empty to generate interrupt. • Verifies that the interrupt occurred.
PCI Interrupt Test	This test performs a PCI INT-A interrupt to the host system. In addition, the IOP does the following to verify receipt of an interrupt from the host: • HDC: Sets up interrupt handler on host side. • Enables PCI INT-A interrupt in IOP PCI register. • Generates INT-A. • Requests verification of interrupt from host and reports results. • Receives interrupt from host.
LED Test	This test cycles through the two LED banks (16 LEDs) to verify proper LED operation. • Saves old values • Clears the LED bank • Sequences the LEDs, starting from the ends and working to the middle **Note**: The user must determine if the test passes
UART External Loopback	This test performs functions similar to the internal loopback test with external transceivers enabled. A test fixture is required (shorts RX and TX, pins 2/3 on DB9/ DB25).
Flash Checksum Test	This test performs a checksum of the Programmable Monitor area of the flash device and compare the results with the checksum stored in flash at the end of the Programmable Monitor.
Flash Write/Read Test	Performs a longword address test on all the installed Flash ROM except for the regions that contain the Fail Safe and Programmable Monitors. The test: • Stores the contents of Flash to memory. • Erases all sectors to be tested. • Writes an incrementing pattern to Flash. • Verifies the pattern. • Erases the pattern. • Restores the original contents.

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Test	Description
Flash Sector Burn Test	Performs a longword address test on the sector indicated in the Flash Sector No. input field of the user interface. The test: • Stores the contents of the selected sector to memory. • Erases the sector to be tested. • Writes an incrementing pattern to the Flash sector. • Verifies the pattern in Flash memory. • Erases the pattern from the sector. • Restores the original contents. **WARNING**: Testing sector 31 (for single ROM, 2MB configurations), or sector 63 (dual ROM, 4MB configurations) may result in loss of operable state.
I2C EEPROM Test	This test verifies the I2C SROM connected to the i960 I2C interface is working correctly. • Reads the data stored in the I2C SROM and saves in a temporary buffer. • Writes a pattern to the I2C SROM. • Reads and verifies the pattern written. • Restores the original contents of the I2C SROM.

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Stream switch diagnostics

These tests test the Lucent T8105 H.100/H.110 interface. The tests detect the T8105 switch vesion and tests appropriately.

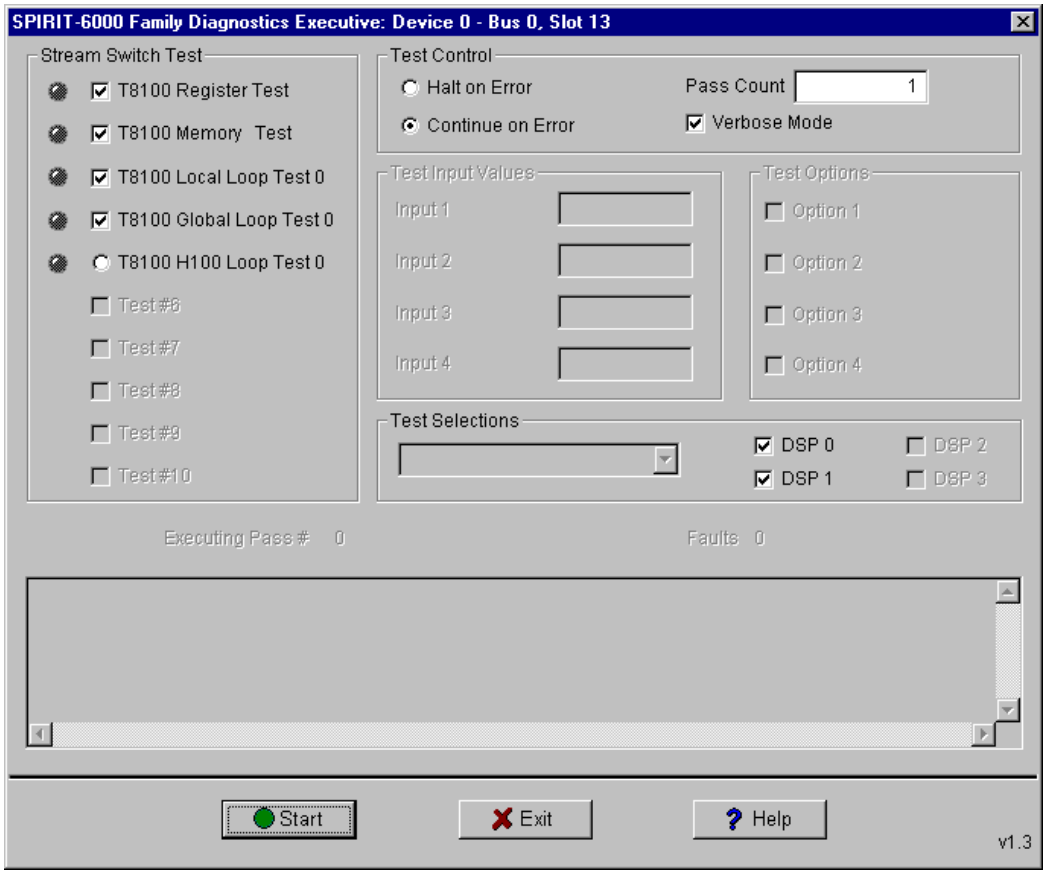


Figure C-7. Stream switch diagnostics screen

Field	Description
T8100 Register Test	Performs a write/read test to several of the registers in the Lucent T8105.
T8100 Memory Test	Performs a write/read test to the internal memory blocks of the T8105. The memory interface the T8105 has slightly different timing than the register interface.
T8100 Local Loop Test 0	Tests the local streams of each DSP by looping the input to the output of each port. Each DSP veifies the ability to receive the data sent from its own output port.
T8100 Global Loop Test 0	Similar to the local loop test, the T8105 is set to cross connect each DSP's port 0 and 1. The DSP tests the ability to receive data on port 1 that was sent out port 0 and vice-versa.

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Field	Description
T8100 H100 Loop Test0	The DSP output serial data is routed to a serial path on the H.100 / H110 bus. There is a loopback fixture to connect the output stream to an input stream. The input stream is routed to the input serial port of the same DSP. The DSP checks the received data for errors. The streams connections made by the loopback fixture are 31 to 0, 30 to 1, ... 16 to 15.

T1 diagnostics

These tests test the PMC-2T1E1LAN and PMC-4T1E1LAN option modules.

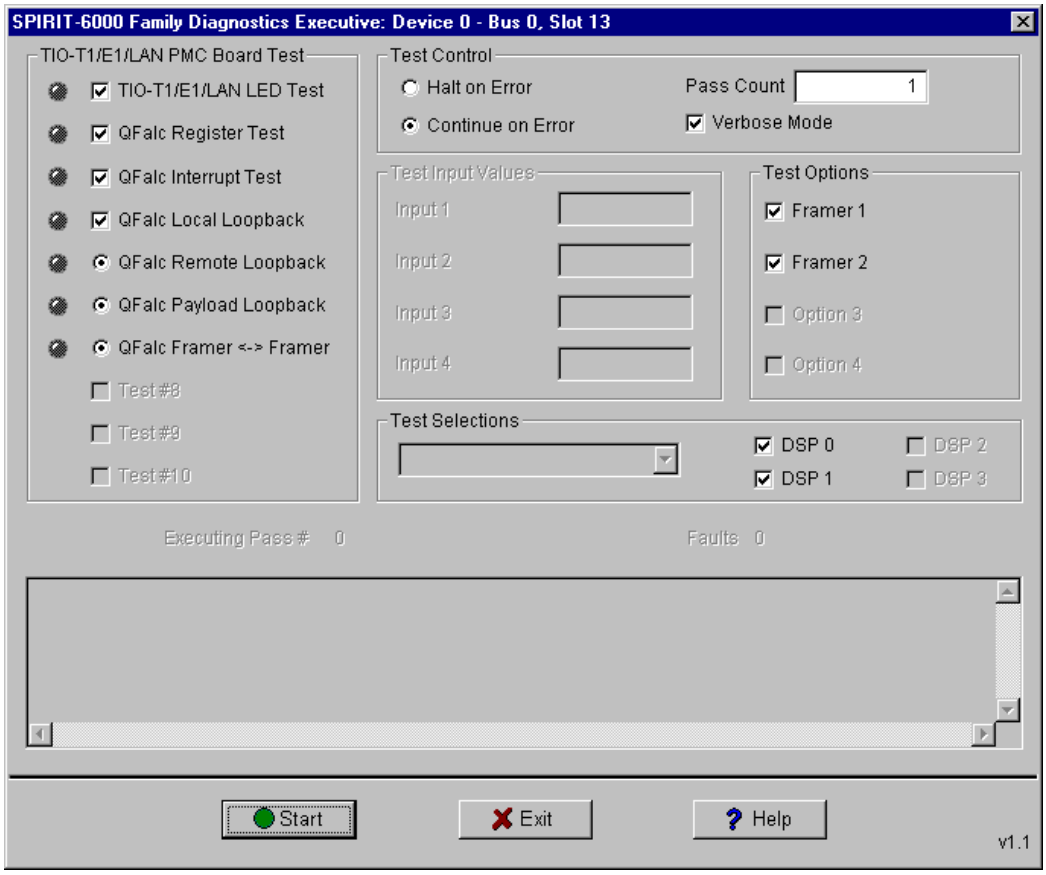


Figure C-8. T1 diagnostic screen

Notes on framer loopback testing

The DSP and the T8105 are used to effect the testing of the framer stream data. Each framer is paired with another framer to allow for testing of Remote, Payload and External loopback modes. The framers are connected via a cable, framer 1 to 2 and framer 3 to 4. Loopback testing consists of:

- Test patterns are created on the DSP.
- The DSP sends the pattern data from one of its serial ports (MCBSPs)

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- The T8105 routes the data to the framer under test
- The framer under test is placed in the mode appropriate for the test being run.
- The T8105 routes the stream data back to the DSP from the framer under test, or its paired framer.
- The DSP checks the data for errors and reports to the i960.

This testing is similar for all modes with the differences primarily in the funcional block of the framer that is being used to loop the data back.

Field	Description
TIO-T1/E1/LAN LED Test	This visual test with no error reporting individually activates each LED in sequence. The operator is responsible for evaluating the test results
QFalc Register Test	Performs a write/read test to several of the registers in each framer.
QFalc Interrupt Test	Verifies the receipt of an interrupt on the i960 from each configured framer.
QFalc Local Loopback	Places the framer under test in Local Loopback mode. The paired framer is idle.
QFalc Remote Loopback	Places the framer under test in Remote Loopback mode. The paired framer is idle.
QFalc Payload Loopback	Places the framer under test in Payload Loopback mode. The paired framer is placed in flow-thru mode.
QFalc Framer <-> Framer	The external loopback validates communication on the T1/E1 between two framers. Both framers are placed in flow-through mode and the Lucent T8105 switch sends data to one framer and recieves the data from the other framer.

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D PMC modules

The SP6040 can accept most 32-bit PMC modules that are mechanically compliant to the PMC standard. The SP6040 supports only the +5V PCI signaling environment. PMC modules which require +3.3V PCI signaling are mechanically prevented from being inserted.

Installing a PMC module on the Main board

You can install a PMC module on the SP6040 as shown below.

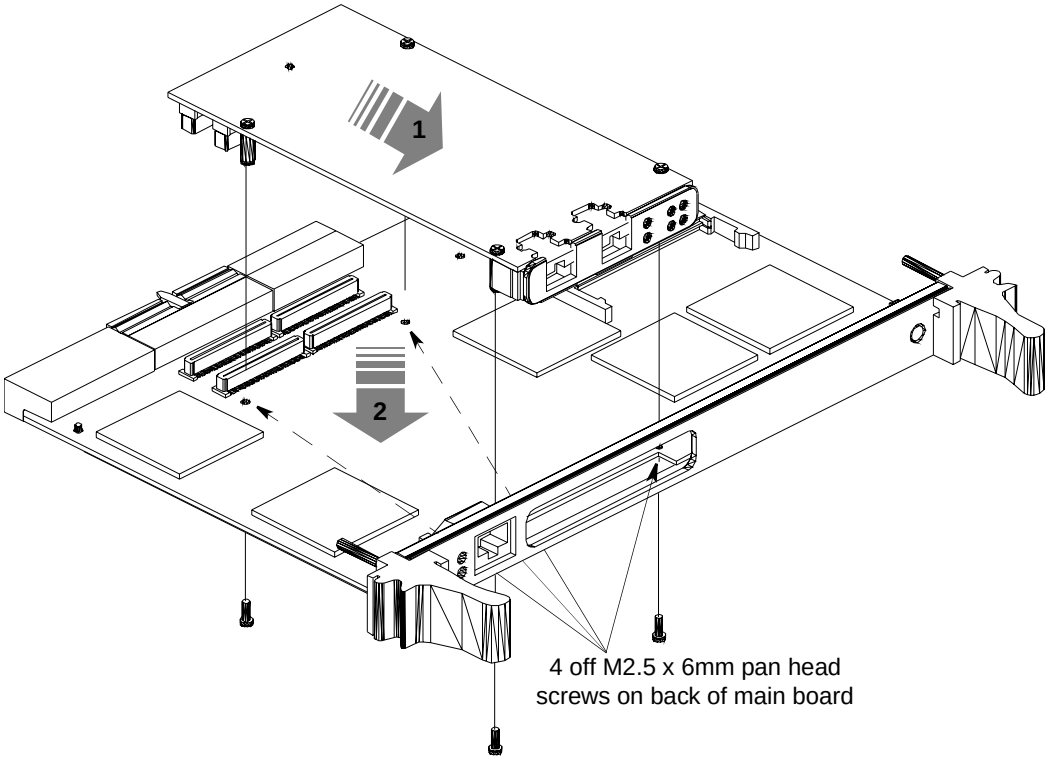


Figure D-1. Inserting a PMC module

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To install a PMC module:



Avoid causing ESD damage:

- Remove modules from their antistatic bags only in a static-free environment.
- Perform the installation process (described later in this chapter) only in a static-free environment.
- During external cable installation, ensure that the cables are not active. The SP6040 is not designed for hot insertion of any interface.

The SP6040 modules, like most other electronic devices, are susceptible to electrostatic discharge (ESD) damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

1. Remove the SP6040 from the CompactPCI chassis as described in *Removing the SP6040* on page 6.
2. Remove and save the blank face plate from the PMC slot in the SP6040 face plate.
3. Position the PMC bezel through the PMC slot on the front panel, then push the rear connectors into the main board.
4. Insert and tighten the screws on the back of the Main board.
5. Replace the SP6040 in the CompactPCI chassis as described in *Inserting the SP6040* on page 6.

Disconnecting the PMC module

If your SP6040 includes an optional PMC module, you must disassemble the board before performing maintenance or upgrades on the SP6040.

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To separate the PMC module and the Main board:

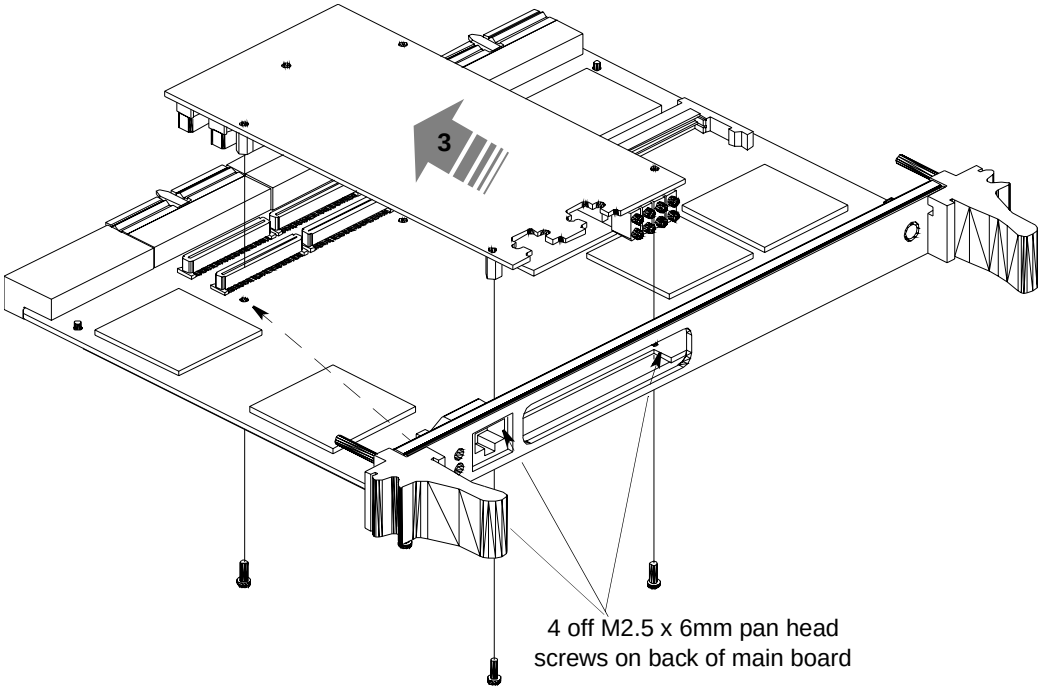


Figure D-2. Inserting a PMC module

1. Remove the SP6040 from the CompactPCI chassis as described in *Removing the SP6040* on page 6.
2. Remove screws on the back of the Main board.
3. Pull the boards apart while keeping them parallel. Continue applying force until the connectors completely disengage.

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E Board support package

The BSP (Board Support Package) is the foundation for SPIRIT-60x0 application development.

The BSP consists of the components shown in the next table. The i960 SDK consists of Monitor source code, i960 and various i960 utilities and documentation.

When reading this file online, you can immediately view information about any BSP component by placing the mouse cursor over a connector name and clicking.

Task	Page
Real time monitor	91
Monitor firmware	91
User interface mode	92
Host interface mode	93
Fail safe monitor	93
Programmable monitor	94
Updating SPIRIT-60x0 monitor firmware	94
Board driver	97
DSP host port interface (HPI)	97
Host debugger interface (HDI)	98

Real time monitor

The SPIRIT-60x0 Monitor (sometimes referred to as SPMON) is a Real Time Monitor which runs on the i960 I/O Processor (IOP). Basic Monitor system services are available to a single application which may be run on “top” of the Monitor, for example, timers, interrupt handlers, access to peripherals and the like.

The SPIRIT-60x0 Monitors are largely consistent with the i960 SDK Monitor’s (MON960) core functionality with the obvious exception of architectural differences (i.e., SPIRIT-60x0 added peripherals such as the DSPs, T8100 and E1/T1).

For configurations where an RTOS is installed, the Monitor runs initially for diagnostics purposes prior to invoking the RTOS boot loader.

Monitor firmware

The SPIRIT-60x0 may be configured with one or two Flash ROMs. This Flash memory is logically divided into Monitor and User regions. The Monitor region contains the Programmable and Fail Safe Monitor images and their components. The Fail Safe Monitor (and IBR) and its components are one sector in size (64 KB) while the Programmable Monitor is three sectors (192 KB) in size. The User region is the remainder of configured Flash ROM space and may be used to store a Monitor application or an operating system (such as VxWorks).

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The Fail Safe Monitor's sector also contains the Initialization Boot Record (IBR) and boot loader. This sector is not typically reprogrammed unless there is an update required to the boot loader configuration code or pre-init diagnostics. A failure during the update may result in loss of operable state.

The Fail Safe Monitor image is activated if the Fail Safe jumper is present or in the event that the Programmable Monitor image checksum fails. In this mode, the Programmable Monitor may be reprogrammed by downloading the image via X-modem terminal emulation software.

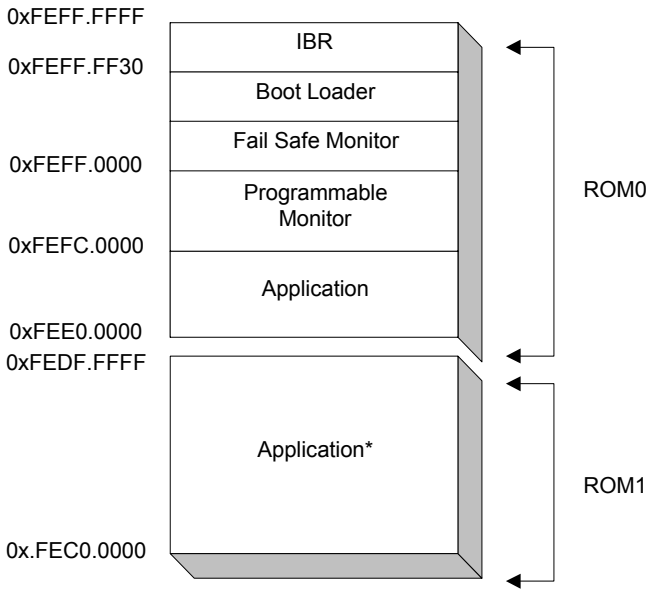


Figure E-1. Flash ROM memory map

The Application* region is only available in the 4MB Flash configuration.

Upon power-up, the i960 accesses the IBR located in Flash ROM at fixed address FEF.F030h. A local bus confidence test is performed using the IBR, and ROM resident Fail Safe Monitor code is executed as indicated by an IBR pointer (see the Intel i960Rx I/O Microprocessor Developer's Manual for details). After initialization and basic memory space validation, either the Fail Safe or Programmable Monitor are unloaded into RAM and control is transferred to code in RAM. POST is performed and the Monitor waits for a connection to be established via serial or PCI interfaces.

User interface mode

User Interface (UI) mode is a special "console" accessed by means of an RS-232 serial interface connected to a "dumb" terminal or terminal emulator.

UI Mode offers various commands as indicated in the *MON960 Debug User's Guide*. You can also enter "?" at the prompt for a list of commands. To exit user mode and restart the built-in application, enter "quit" (or "qu") on the command line. Exiting User Mode resets the SPIRIT-60x0.

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Note that when an application is built-in with the Monitor, UI mode is not available. RMONDB (via the PCI interface) must be used to interrupt the running application and enter Host Interface mode. UI mode is not accessible if the Host Interface mode is active.

Additional UI commands

In addition to the UI commands supported by MON960, the commands listed in Table E-1 are supported by SPMON. Enter "?" followed by the command for syntax.

Table E-1. Additional UI commands supported by SPMON

Command	Description
`ef`	Erase flash ROM region.
`dx`	Display DSP memory
`mc`	Modify character (for C00x.xxxx 8-bit space)
`mx`	Modify DSP memory.
`se`	Set configuration (save to serial EEPROM)
`sh`	Show configuration.

Host interface mode

Host interface (HI) mode requires RMONDB (HDC (Host Diagnostic Control) software). Executing either of these programs on the host may interrupt the application running on the IOP and enter Host Interface Mode. A host connection may be established via the PCI or the serial port communication path.

Note that upon exit of HI mode, the SPRIT-60x0 is reset, POST is performed and IOP restarts execution of the built-in application (if any). HI mode is not accessible if User Interface mode is active. Most User Interface commands are available from Host Interface Mode. Note that if a dumb terminal or computer is attached to the SPIRIT-60x0 serial port, the User interface mode may be selected if the remote equipment transmits several carriage returns after a SPIRIT-60x0 reset.

Fail safe monitor

The Fail Safe image consists of the i960 IBR, a small boot loader and a functionally reduced version of the Programmable Monitor (known as the Fail Safe Monitor) all contained within a single 64KB sector.

The Fail Safe is primarily responsible for performing initial boot loading and initialization of the i960. Do not confuse this area of flash with the Programmable Monitor which changes with firmware releases. This region should not be reprogrammed unless specifically indicated by RadiSys.

Fail Safe mode is activated if the Programmable Monitor fails its checksum test or if the Fail Safe jumper is installed. Note that the Fail Safe Monitor only supports the serial User Interface communication mode.

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Programmable monitor

The Programmable Monitor image is up to 192KB in size. The Programmable Monitor contains the bulk of POST diagnostics and is the fully functional version of the Monitor. The Programmable Monitor optionally runs a built-in application on power-up.

Updating SPIRIT-60x0 monitor firmware

The SPIRIT-60x0 firmware consists of two images:

- **Programmable Monitor**: sp6k_*majornumber-sequence.fls*. For example, sp6k_330-35.fls.
- **Fail Safe Monitor**: fs_sp6k_*majornumber-sequence.fls*. For example, fs_sp6k_330-5.fls.

The latest released firmware is installed in the SP6KBSP directory during installation of the RadiSys Voice Gateway SDK. Firmware COFF files are located in \SP6KBSP\bin:

Monitor version information

SPIRIT-60x0 Programmable Monitor version information may be obtained as follows:

1. Attach a serial cable to the UART port.
2. Connect a terminal or terminal emulator to the serial cable.
3. Set the terminal for 8 bit, No parity, 1 stop bit, XON/XOFF flow control
4. Set serial port the baud rate 9600 bps (19200 bps and 38400 bps are also acceptable).
5. Reset the board to put the board in the state that occurs after POST.



Information may display on the terminal after reset. This is normal.

If the terminal is set to 9600 bps, the POST count-up displays. Otherwise random characters may display.

6. Press the Return key several times to allow the Monitor to autobaud detect the connection.

The Monitor's name and version information display along with a prompt ">>>". Normally, the programmable monitor ("SPIRIT-6000 Monitor") is active. If the Fail Safe monitor displays, either the Fail Safe jumper is installed, or the programmable monitor failed the checksum test. If the Fail Safe monitor is activated and the Fail Safe jumper is not installed, erase and burn a new Programmable Monitor.

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To obtain the Fail Safe monitor's version:

1. Install the Fail Safe jumper and reset the board.
2. Reset the board using the Windows NT SP6K utility, included in the Voice Gateway BSP, by entering this command:

   `sp6k_util -reset -dev board_number`

   where *board_number* is the SPIRIT-60x0 device number (0–7).

   If windows NT is not running you can reset the board using one of these methods:
   - Reset the CompactPCI host computer
   - Cycle the power on the CompactPCI chassis

3. Press the Return key several times to connect via the terminal and display version information.

Remove the Fail Safe jumper and reset the board to allow for host PCI connections.

Updating the Fail Safe Monitor firmware

If the Fail Safe monitor becomes corrupted, contact RadiSys technical support before you try to reprogram this portion of the Flash.

This section is included only for completeness. Under normal circumstances, you should not need to update the Fail Safe Monitor.

To update the Fail Safe monitor firmware, a serial connection is required. The Fail Safe jumper need not be installed. Perform the following steps:

- The terminal (or emulator) must be capable of uploading a file via the X-MODEM protocol.
- This image should not be reprogrammed unless indicated by RadiSys. Do not confuse the Fail Safe Monitor with the Programmable Monitor.

The following conditions may require a Flash ROM replacement at the factory:
- A failure during update of the Fail Safe monitor. This may result in loss of operable state. That is, if the image fails to update correctly, the SPIRIT-60x0 is not accessible.
- Updating the Fail Safe monitor before the system completes the Windows NT boot process. When Windows NT starts, the SP6040 board driver resets the board. This reset may corrupt an in-progress failsafe update.

1. Attach a serial cable to the UART port.
2. Connect a terminal or terminal emulator to the serial cable.
3. Set the terminal for 8-bit, no parity, 1 stop bit, and XON/XOFF flow control.
4. Set the serial port baud rate to 9600 bps (19200 bps and 38400 bps are also acceptable).
5. If you are using two computers, do the following:

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A. Wait for the CompactPCI host computer that controls the system in which the SP6040E-C board is installed to completely boot to Windows NT and complete the login procedure.

B. Prevent Windows NT from booting on the CompactPCI host computer that controls the system in which the SP6040E-C board is installed.

6. If the board has not recently reset, you must reset the board to put the board in the state that occurs after POST.
7. Enter console UI mode by pressing the Return key several times.
8. Invoke the UI Flash erase utility by entering this command at the prompt.

   ```
   ef
   ```

9. Select option “1” to erase the Fail Safe monitor.

   Do not press the Return key.

10. Enter “Y” to confirm erase.

    Do not press the Return key.

11. Verify that the erase completed successfully.
12. Start the download (receive) on the SPIRIT-60x0 by entering this command:

    ```
    do
    ```

13. Start the X-modem upload (send) of the Fail Safe monitor image on the terminal.
14. Do one of these:
    - If the update was successful, reset the board.
    - If the update failed, do *not* reset the board. Repeat the necessary steps, that is, go back to step 3 and erase the Fail Safe region, start download on SPIRIT-60x0 and re-send the image.

Updating the programmable monitor firmware

The programmable monitor firmware may be updated via the serial or PCI connection.

To update via the serial connection:

1. Ensure that the host system completes the Windows NT boot process. The SP6040 board driver resets the board when Windows NT starts.

   If you begin the update before Windows NT boots, you must begin again at step three.

2. Install the ROM Write Enable jumper.
3. Enter console UI mode by pressing the Return key several times.
4. Invoke the UI Flash Erase utility by entering this command at the prompt:

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`ef`

5. Select option “2” to erase the programmable monitor.



Do not press the Return key.

6. Enter “Y” to confirm erase.



Do not press the Return key.

7. Verify that the erase completed successfully.
8. Start the download (receive) on the SPIRIT-60x0 by entering this command at the prompt:

   `do`
9. Start the X-modem upload (send) of the programmable monitor image on the terminal.
10. Reset the board if the update was successful.

To update via the PCI connection:

1. Install the ROM Write Enable jumper.
2. From a DOS Window, run RMONDB by entering this command:

   `rmondb -pci -ef -ne <IMAGE_PATH>\sp6k_`*`majornumber-sequence.fls`*

Board driver

The BSP provides a board driver for communication between a host and the SPIRIT-60x0 boards. The host device driver maps all of the IOP’s (I/O Processor) external memory for each SPIRIT-60x0 into PCI memory space.

During driver initialization by the host operating system, the driver probes the PCI buses in the system looking for the i960 ATU vendor/device ID pair (0x8086, 0x1960). Once found, the driver verifies that the subsystem VID (vendor ID) and DID (device ID) match those of RadiSys and a SPIRIT-60x0. For each SPIRIT-60x0 found in the system, the ATU is configured and memory space is mapped on the host accordingly. For example:

`VID: 0x1331, SPIRIT-6000/SPIRIT-6020 DID: 0x6000, SPIRIT-6040 DID: 0x6040`

The host driver is thread-safe and is opened only once. Individual SPIRIT-60x0 boards in a system are referenced by a device number in the range of 0–7.

DSP host port interface (HPI)

After POST, the Monitor leaves each of the populated DSPs in Reset. Host and IOP APIs are available to, among other things, initialize the DSP, boot load the DSP, read/write from/to the DSP and set up DSP interrupt handlers.

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Host debugger interface (HDI)

An interface known as the HDI (Host Debugger Interface) is used by RMONDB (on a Windows NT host) to communicate with the SPIRIT-60x0 programmable monitor via the PCI or serial interfaces. The host to the i960 communication path is referred to as the HI (Host Interface), and can be used for various tasks such as to examine and modify memory locations, load and debug programs. HDI connectivity is depicted in Figure E-2. This interface is described further in the documentation supplied with the Intel i960 SDK.

When communicating via the PCI interface, the HDI uses the i960 Messaging Unit to transfer messages between the host and IOP. RMONDB is based on the Intel i960 SDK's MONDB utility and has been modified to use the SPIRIT-60x0 device driver.

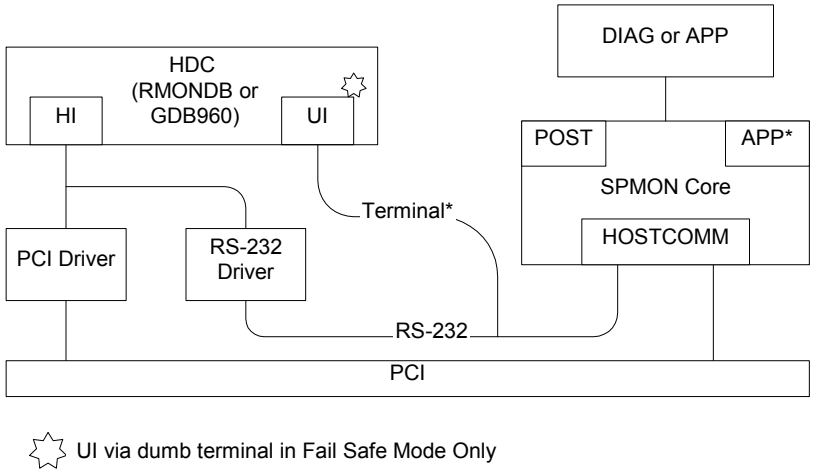


Figure E-2. SPIRIT-60x0 HDI connectivity block diagram

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Glossary

Address: A number that identifies the location of a word in memory. Each word in a memory storage device or system has a unique address. Addresses are always specified as a binary number, although octal, hexadecimal, and decimal numbers are often used for convenience.

ANSI: (American National Standards Institute) An organization dedicated to advancement of national standards related to product manufacturing.

BIOS: (Basic Input/Output System) Firmware in a PC-compatible computer that runs when the computer is powered up. The BIOS initializes the computer hardware, allows the user to configure the hardware, boots the operating system, and provides standard mechanisms that the operating system can use to access the PC's peripheral devices.

Bit: A binary digit.

Boot: The process of starting a microprocessor and loading the operating system from a powered down state (cold boot) or after a computer reset (warm boot). Before the operating system loads, the computer performs a general hardware initialization and resets internal registers.

Boot Device: The storage device from which the computer boots the operating system.

Byte: A group of 8 bits.

CAS: (Column Address Strobe) An input signal from the DRAM controller to an internal DRAM latch register specifying the column at which to read or write data. The DRAM requires a column address and a row address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of column addresses and row addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required.

CNG: (Comfort Noise Generator) A software algorithm that creates a background audio signal to replace the silence created by some software CODECs during the time no speech data is transmitted over the telephone line.

CODEC: (COder/DEcoder) Converts voice signals from analog form to digital signals acceptable to modern digital PBXs and digital transmission systems. It then converts those digital signals back to analog so that you can hear and understand what the other person is saying.

CPU: (Central Processing Unit) A semiconductor device which performs the processing of data in a computer. The CPU, also referred to as the microprocessor, consists of an arithmetic/logic unit to perform the data processing, and a control unit which provides timing and control signals necessary to execute instructions in a program.

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COM Port: A bi-directional serial communication port which implements the RS-232 specification.

CSMA/CD: (Carrier-Sense Multiple Access with Collision Detect) A method whereby workstations on a network listen for transmission in progress (carrier sense) before starting to transmit (multiple access). If two or more workstations transmit at the same time, each workstation stops transmitting (collision detection) for a different amount of time before trying to transmit again.

CSU: (Channel Service Unit) A device to terminate a digital channel on a customer's premises. It performs certain line coding, line-conditioning and equalization functions, and responds to loopback commands sent from the central office.

CT bus: (Computer Telephony Bus) An auxiliary bus used in computer systems. This bus is dedicated to carrying telecom data between the system components.

Default: The state of all user-changeable hardware and software settings as they are originally configured before any changes are made.

Driver: A software component of the operating system which directs the computer interface with a hardware device. The software interface to the driver is standardized such that application software calling the driver requires no specific operational information about the hardware device.

DRAM.: (Dynamic Random Access Memory) Semiconductor RAM memory devices in which the stored data does not remain permanently stored, even with the power applied, unless the data are periodically rewritten into memory during a refresh operation.

DSX: (Digital System Cross-connect Frame) A bay or panel to which T-1 lines and DS1 circuit packs are wired and that permits cross-connections by patch cords and plugs. A DSX panel is used in small office applications where only a few digital trunks are installed.

DSX-1: (Digital Signal Cross-connect Level 1) The set of parameters for cross connecting DS-1 lines.

EEPROM: (Electrically Erasable Programmable ROM) EPROMs that can be erased electrically as compared to other erasing methods.

EDO: (Extended Data Out) A type of DRAM that allows higher memory system performance since the data pins are still driven when CAS# is de-asserted. This allows the next DRAM address to be presented to the device sooner than with Fast Page Mode DRAM.

ESF: (Extended Super Frame or Extended Superframe Format) A T-1 format that uses the 193rd bit as a framing bit. ESF provides frame synchronization, cyclic redundancy checking and data link bits. Frames consist of 24 bits instead of the previous standard 12 bits as in the D4 format. The standard allows error information to be stored and retrieved easily, facilitating network performance monitoring and maintenance.

Flash Memory: A fast EEPROM semiconductor memory typically used to store firmware such as the computer BIOS. Flash memory also finds general application where a semiconductor non-volatile storage device is required.

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Flash Recovery: A process whereby an existing, corrupt BIOS image in the flash boot device is overwritten with a new image. Also referred to as a flash recovery.

Flash Update: A process whereby an existing, uncorrupted BIOS image in the flash boot device is overwritten with a new image. Also referred to as a flash update.

FPM: (Fast Page Mode) A "standard" type of DRAM that is lower performance than EDO.

FPGA: (Field Programmable Gate Array) A large, general-purpose logic device that is programmed at power-up to perform specific logic functions.

Framers: A device used in digital communication systems to create parellel data frames from a serial data stream.

GB or GByte: (Gigabyte) Approximately one billion (US) or one thousand million (Great Britain) bytes. 2^30 = 1,073,741,824 bytes exactly.

Hang: A condition where the system microprocessor suspends processing operations due to an anomaly in the data or an illegal instruction.

HDLC: (High Level Data Link Control) An ITU-TSS link layer protocol standard for point-to-point and multi-point communications. In HDLC, control information is always placed in the same position. And specific bit patterns used for control differ dramatically from those used in representing data, so that errors are less likely to occur.

Header: A mechanical pin and sleeve style connector on a circuit board. The header may exist in either a male or female configuration. For example, a male header has a number and pattern of pins which corresponds to the number and pattern of sleeves on a female header plug.

h: (Hexadecimal) A base 16 numbering system using numeric symbols 0 through 9 plus alpha characters A, B, C, D, E, and F as the 16 digit symbols. Digits A through F are equivalent to the decimal values 10 through 15.

IMI: (Initial Memory Image) A structure in memory the i960 core requires to initialize internal registers before normal operation.

INT: (Interrupt Request) A software-generated interrupt request.

IOP: (Input/Output Processor) A processing element on intelligent adapter boards used to off-load a host processor.

I/O: (Input/Output) The communication interface between system components and between the system and connected peripherals.

IRQ: (Interrupt Reques). In ISAbus systems, a microprocessor input from the control bus used by I/O devices to interrupt execution of the current program and cause the microprocessor to jump to a special program called the interrupt service routine. The microprocessor executes this special program, which normally involves servicing the interrupting device. When the interrupt service routine is completed, the microprocessor resumes execution of the program it was working on before the interruption occurred.

ISR: (Interrupt Service Routine) A program executed by the microprocessor upon receipt of an interrupt request from an I/O device and containing instructions for servicing of the device.

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Jumper: A set of male connector pins on a circuit board over which can be placed coupling devices to electrically connect pairs of the pins. By electrically connecting different pins, a circuit board can be configured to function in predictable ways to suit different applications.

KB or KByte: (Kilobyte) Approximately one thousand bytes. $2^{10} = 1024$ bytes exactly.

LIU: (Line Interface Unit)

Logical Address: The memory-mapped location of a segment after application of the address offset to the physical address.

MAC: (Media Access Controller) A media-specific access control protocol within IEEE 802 specifications for the lower half of the data link layer (layer 2) that defines topology dependent access control protocols for IEEE LAN specifications.

MB or MByte: (Megabyte) Approximately one million bytes. 2^20 = 1,048,576 bytes exactly.

Memory: A designated system area to which data can be stored and from which data can be retrieved. A typical computer system has more than one memory area.

Memory shadowing: Copying information from an extension ROM into DRAM and accessing it in this alternate memory location.

Offset: The difference in location of memory-mapped data between the physical address and the logical address.

PAL: (Programmable Array Logic) A semiconductor programmable ROM which accepts customized logic gate programming to produce a desired sum-of-products output function.

PCI: (Peripheral Component Interconnect) A popular microcomputer bus standard used extensively in personal computer architecture. This 32-bit local bus, used inside PCs, was designed by Intel.

Peripheral Device: An external device connected to the system for the purpose of transferring data into or out of the system.

PHY: (Physical Layer) An ATM layer whose functionality loosely corresponds to the OSI physical layer (Layer 1). ATM Physical Layer functionality includes the Physical Medium sublayer (PM) and the Transmission Convergence (TC) sublayer.

PLL: (Phase-Locked Loop) A semiconductor device which functions as an electronic feedback control system to maintain a closely regulated output frequency from an unregulated input frequency. The typical PLL consists of an internal phase comparator or detector, a low pass filter, and a voltage controlled oscillator which function together to capture and lock onto an input frequency. When locked onto the input frequency, the PLL can maintain a stable, regulated output frequency (within bounds) despite frequency variance at the input.

Physical Address: The address or location in memory where data is stored before it is moved as memory remapping occurs. The physical address is that which appears on the computer's address bus when the CPU requests data from a memory address.

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	When remapping occurs, the data can be moved to a different memory location or logical address.
Pinout:	A diagram or table describing the location and function of pins on an electrical connector.
PMC:	(PCI Mezzanine Card) A new standard form factor for PCI add-in modules. PMCs mate with their respective connectors on the motherboard and are secured with screws.
POST:	(Power On Self Test) A diagnostic routine which a board runs at power up. Along with other testing functions, this comprehensive test initializes the system chipset and hardware, resets registers and flags, performs ROM checksums, and checks disk drive devices and the keyboard interface.
PQFP:	(Plastic Quad Flat Pack) A popular package design for integrated circuits of high complexity.
Program:	A set of instructions a computer follows to perform specific functions relative to user need or system requirements. In a broad sense, a program is also referred to as a software application, which can actually contain many related, individual programs.
RAM:	(Random Access Memory) Memory in which the actual physical location of a memory word has no effect on how long it takes to read from or write to that location. In other words, the access time is the same for any address in memory. Most semiconductor memories are RAM.
ROM:	(Read Only Memory) A broad class of semiconductor memories designed for applications where the ratio of read operations to write operations is very high. Technically, a ROM can be written to (programmed) only once, and this operation is normally performed at the factory. Thereafter, information can be read from the memory indefinitely.
Reflashing:	The process of replacing a BIOS image, in binary format, in the flash boot device.
Register:	An area typically inside the microprocessor where data, addresses, instruction codes, and information on the status on various microprocessor operations are stored. Different types of registers store different types of information.
Reset:	A signal delivered to the microprocessor by the control bus, which causes a halt to internal processing and resets most CPU registers to 0. The CPU then jumps to a starting address vector to begin the boot process.
RS-232:	A popular asynchronous bi-directional serial communication protocol. Among other things, the RS-232 standard defines the interface cabling and electrical characteristics, and the pin arrangement for cable connectors.
RAS:	(Row Address Strobe) An input signal to an internal DRAM latch register specifying the row at which to read or write data. The DRAM requires a row address and a column address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of row addresses and column addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required.

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RTOS: (Real Time Operating System) An operating system that performs tasks at specified times.

Sample rate generator: Software or firmware that the number of times per second that an analog signal is measured and converted to a binary number -- the purpose being to convert the analog signal to a digital analog. The most common digital signal—PCM—samples voice 8,000 times a minute.

SBSRAM: Synchronous Burst Static Random Access Memory.

Serial Port: A physical connection with a computer for the purpose of serial data exchange with a peripheral device. The port requires an I/O address, a dedicated IRQ line, and a name to identify the physical connection and establish serial communication between the computer and a connected hardware device. A serial port is often referred to as a COM port.

SF: (Super Frame) A DS1 framing format in which 24 DSO timeslots plus a coded framing bit are organized into a frame which is repeated 12 times to form the ssuperframe.

Shadow Memory: RAM in the address range 0xC000h through 0xFFFFFh used for shadowing. Shadowing is the process of copying BIOS extensions from ROM into DRAM for the purpose of faster CPU access to the extensions when the system requires frequent BIOS calls. Typically, system and video BIOS extensions are shadowed in DRAM to increase system performance.

SODIMM: (Small Outline Dual Inline Memory Module) A new form factor for memory modules that is smaller and denser than SIMMs.

Standoff: A mechanical device, typically constructed of an electrically non-conductive material, used to fasten a circuit board to the bottom, top, or side of a protective enclosure.

SRAM: (Static Random Access Memory) A semiconductor RAM device in which the data remains permanently stored as long as power is applied, without the need for periodically rewriting the data into memory.

Symmetrically Addressable SIMM: A SIMM, the memory content of which is configured as two independent banks. Each 16-bit wide bank contains an equal number of rows and columns and is independently addressable by the CPU via twin row address strobe registers in the DRAM controller.

TDM: (Time Division Multiplex) A technique originated in satellite communications to interweave multiple conversations into one transponder so as to appear to get simultaneous conversations. This technicque is used on the H.110 bus and the internal DSP serial buses.

TSI: Time-slot interchange. A way of temporarily storing data bytes so they can be sent in a different order than they were received. TSI is a way to switch calls.

UART: (Universal Asynchronous Receiver/Transmitter) A device, usually an integrated circuit chip, that converts digital data to transmit from parallel to serial, and transmitted digital data from serial to parallel. The UART converts incoming serial data from the device connected to the serial port (typically a modem) into the parallel form that your computer handles. UART also

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converts the computer's parallel data into serial data suitable for asynchronous transmission on phone lines.

VoIP: (Voice over Internet Protocol) A protocol that enables devices of disparate manufactures to support voice communication over packet networks such as the Internet.

Wait State: A period of one or more microprocessor clock pulses during which the CPU suspends processing while waiting for data to be transferred to or from the system data or address buses.

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