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PME SIO-4
Manual

Rev. 2

Issue 6

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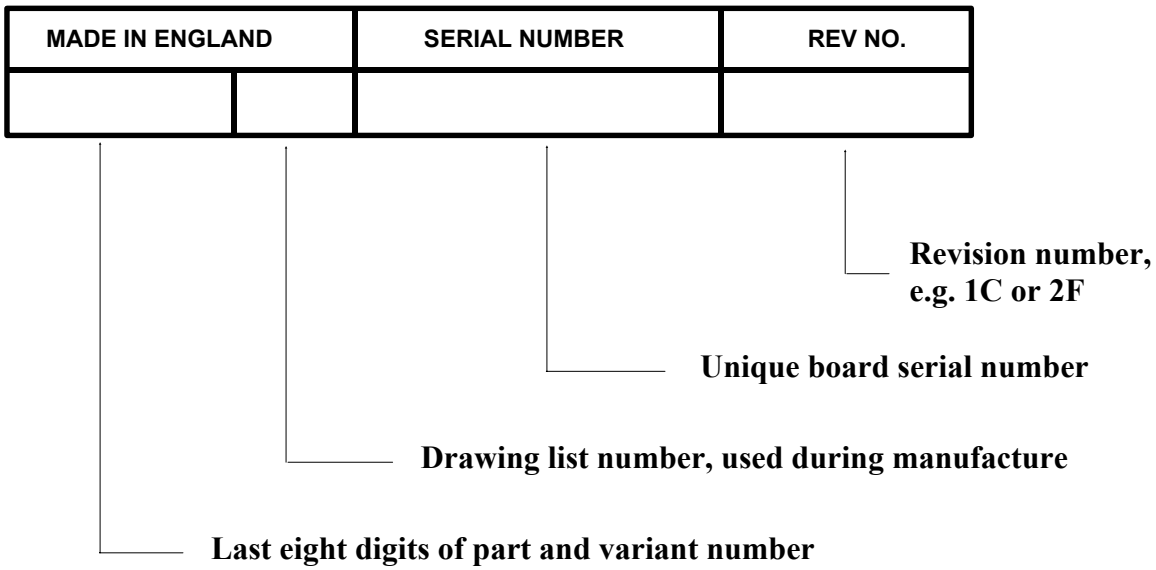
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Chapter 1 - Introduction

Manual Scope

This manual describes the hardware and firmware of the PME SIO-4 Serial Communications Controller.

User Entry Point

All users should verify, and alter if necessary, any link settings that are pertinent to the board operation in their particular environment. See Chapter 4 for details.

For software operation, users who interface to the SIO-4 through a standard UNIX or OS-9 driver only need to see the sections on Control Registers, etc. For driver loading information, see the appropriate Radstone publication (UNIX or OS-9).

SIO-4 Overview

For multi-user, multi-tasking operating systems such as OS-9, UNIX, XENIX or PC-DOS to run, they must support several input/output devices, e.g. disks (hard and floppy), serial ports and graphics devices. If the host CPU has to handle these devices (and possibly more), and run the operating system as well, there will be little residual processing power to support any "users" of the system.

To overcome this performance problem, the control of the I/O devices can be distributed to separate I/O controller cards. These cards support the I/O devices and so decrease the overhead they place on the main CPU.

Performance can be further enhanced by off-loading the I/O data processing to a peripheral card. The SIO-4 carries out this function for serial I/O data. It is a high performance serial input/output subsystem controller card. It provides an interface, via a VMEbus, for up to sixteen asynchronous RS-232C serial lines. It also has an option of two synchronous channels.



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Figure 1. PME SIO-4 Controller

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Features

The SIO-4 has the following features:

- Reduces main CPU and bus loading by intelligent on-board handling of asynchronous I/O data processing
- Sixteen asynchronous RS-232C serial channels
- Optional 68562 Dual Universal Synchronous Communications Controller (DUSCC)
- MC68020 processor running at 12 MHz with no wait-states into 1 Mbyte of local RAM, which is accessible from the VMEbus on a selectable 1 Mbyte boundary
- Up to 1 Mbyte of EPROM containing basic firmware, self-tests, monitor and real time executive
- Raw throughput of 38,400 baud per channel
- 50 to 38,400 baud split speed operation
- Five to eight bit characters, plus parity option with 1, 1.5 or 2 stop bits
- Odd, even or no parity
- All sixteen channels are under individual software control via a command interface in local dual port RAM
- VMEbus interface conforms to ANSI/IEEE Std. 1014-1987
- Access to full 4 Gbyte address range
- Programmable address modifier codes
- Drivers available for UNIX V.3 and OS-9

Ordering Information

PME SIO-4	Serial I/O Sub-System Controller
PME SIO-4FP-1	Front Extension Kit
PME 10K/4	Rear Extension Kit

The PME SIO-4 Extension Kit Application Note (AN1/SIO4/7/92) describes both the front and rear extension kits. The following **P**rocessor **OP**tions (POPs) are available:

POP 1	12.5 MHz 68020 processors	
POP 3	2 Channel DUSCC 68562	
POP 4	Original firmware SIOP-1	mutually
POP 5	Radstone firmware SIOP-2.1	exclusive
POP 6	PLUM firmware	
POP 7	Remote reset ability	

For example, to order an SIO-4 with a 12.5 Mhz 68020 processor, Radstone firmware SIOP-2.1 and a rear extension kit, specify this as:

PME SIO-4, POP1, POP5, PME 10K/4.

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Functional Overview

VMEbus Interface

The SIO-4 appears to the host processor as 1 Mbyte of RAM mapped into the VMEbus memory map on a 1 Mbyte boundary. On-board Dual-In-Line (DIL) switches select the address used. The card has full VME interrupt generation and handling capabilities, and a location monitor facility. As a slave, the card can be set by jumpers to respond simultaneously in the A24 and A32 address spaces.

A VMEbus SYSRESET* signal resets the card, which then reads the reset vector from the on-board EPROM. The actual vector depends on the setting of the reset jumpers.

User Interface

The SIO-4 has sixteen independently programmable input/output channels provided by eight type 68681 Dual Universal Asynchronous Receiver/Transmitters (DUARTs). Each channel has a control structure associated with it in the local memory. A host controls the SIO-4 by accessing control words within these structures in the local memory.

System Monitor Interface

The SIO-4 provides a monitor port to allow a terminal to be connected to the card for diagnostics and firmware monitoring during execution. A ninth DUART (the system DUART), provides access to this port via the P2 connector.

RS-232C Interface

The sixteen RS-232C channels leave the front panel of the SIO-4 via two 64-way connectors. The DUARTs have the following characteristics:

- 5 to 8 data bits plus parity
- Odd, even or no parity
- 1 or 2 stop bits
- Baud rates from 50 to 38,400 baud
- Parity, framing and overrun error detection

Synchronous Interface

An optional DUSCC (type 68562) supports synchronous protocols via the P2 connector.

RAM Interface

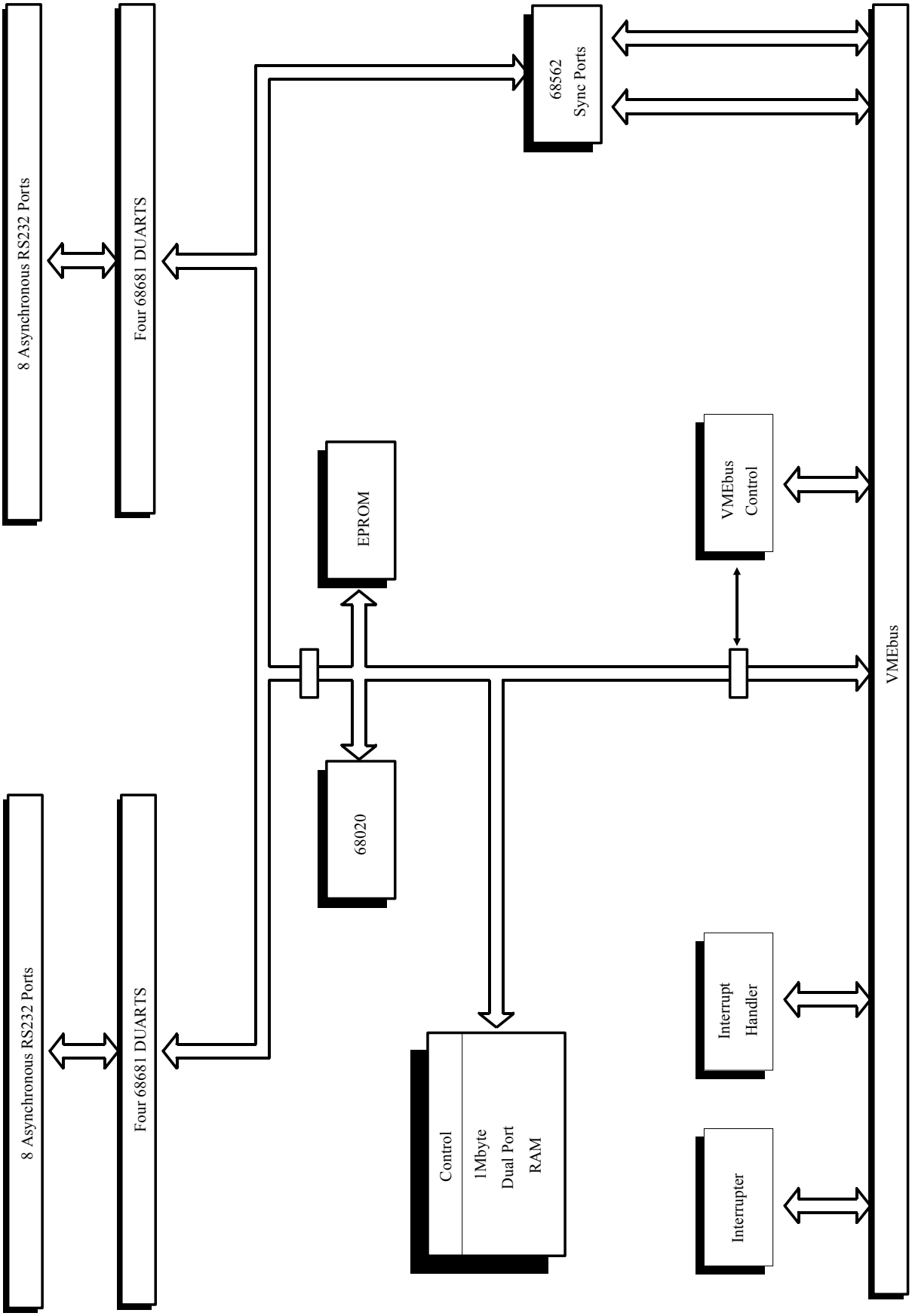
The SIO-4 contains 1 Mbyte of 32-bit wide dual-ported RAM. It uses eight 256k x 4-bit memory devices (1 Mbit chips). The RAM supports zero wait state execution at 12 MHz. The memory supports read-modify-write cycles.

Maintenance

If you comply with the environmental specifications in Chapter 2, then the SIO-4 requires no routine maintenance. Any maintenance is at the card replacement level. The SIO-4 has a comprehensive set of self-tests that run on power-up.

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Figure 2. SIO-4 Block Diagram



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Conventions

This manual uses the following conventions:

The prefix '0x' denotes a hexadecimal number, following the 'C' programming language convention. For example, 0xFFE00040 is the hexadecimal number FFE00040. Octal numbers always begin with a zero, e.g. 0352. Decimal numbers are represented just by the number.

An asterisk denotes an active low signal, e.g. BBSY*.

Jumpers are 'fitted' or 'in' when a link physically connects the pins and 'out' otherwise.

Related Documents

Radstone OS-9 Manual, publication number RT1017.

Radstone UNIX V.3 Reference Manual, publication number 651/HH/19062/000.

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Chapter 2 - Specifications

Technical Specification

VMEbus Compliance	The SIO-4 conforms to ANSI/IEEE Std. 1014 (1987)	
	Bus Master	A24 - D8, D16 A32 - D8, D16, D32
	Bus Slave	A24 - D8, D16 A32 - D8, D16, D32
	Interrupt Handler	I(0-7)
Processor	The processor is a 32-bit MC68020, running at 12 MHz with no wait states.	
Memory	1 Mbyte of shared 32-bit wide DRAM. 64 Kbytes to 1 Mbyte of EPROM in a 32-pin JEDEC socket.	
Counter Timer	A ninth DUART (the system DUART) provides a counter timer for use by on-board firmware. This DUART also allows on-board monitoring of the card.	
Serial I/O	Asynchronous:	Eight DUARTs type 68681
	Synchronous:	One DUSCC type 68562 (optional)
Software Interface	Compatible with the *Termio* section of the UNIX System V manual. Supports all defined data rates plus 19,200 baud.	
Electrical	Voltage supply requirement: + 5V, + 12V and -12V.	
	Current consumption:	6.5 A @ + 5V 100 mA @ + 12V 100 mA @ -12V

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Environmental Specifications

Operating Environment

The SIO-4 will operate under the following conditions:

Temperature Range	0℃ to + 55℃
Cooling Requirements	A linear airflow of at least 2.5 Meters/second (8.5 feet/second) across each card is recommended
Relative Humidity	Up to 95% without condensation
Thermal Shock	± 5℃ per minute
Altitude	-300 to + 3,000 Metres (-1,000 to + 10,000 feet approximately)
Vibration	5 to 100Hz at 2g acceleration
Mechanical Shock	20g for 6 ms (half sine) when mounted in a suitable racking system.

Storage Environment

The SIO-4 may be stored or transported without damage within the following limitations:

Temperature Range	-55℃ to + 85℃
Relative Humidity	0 to 95% without condensation
Thermal Shock	± 10℃ per minute
Altitude	-300 to + 16,000 Metres (-1,000 to + 50,000 feet approximately)
Vibration	0 to 500Hz at 2g acceleration
Mechanical Shock	20g for 6 ms (half sine) when mounted in a suitable racking system

Mean Time Between Failures (MTBF)

The calculated mean time between failures for the SIO-4 is 66,000 hours. The failure rates used in this calculation were derived from the British Telecom Reliability Handbook HRD4 with MIL-HDBK-217D and in-house data.

Mechanical Construction

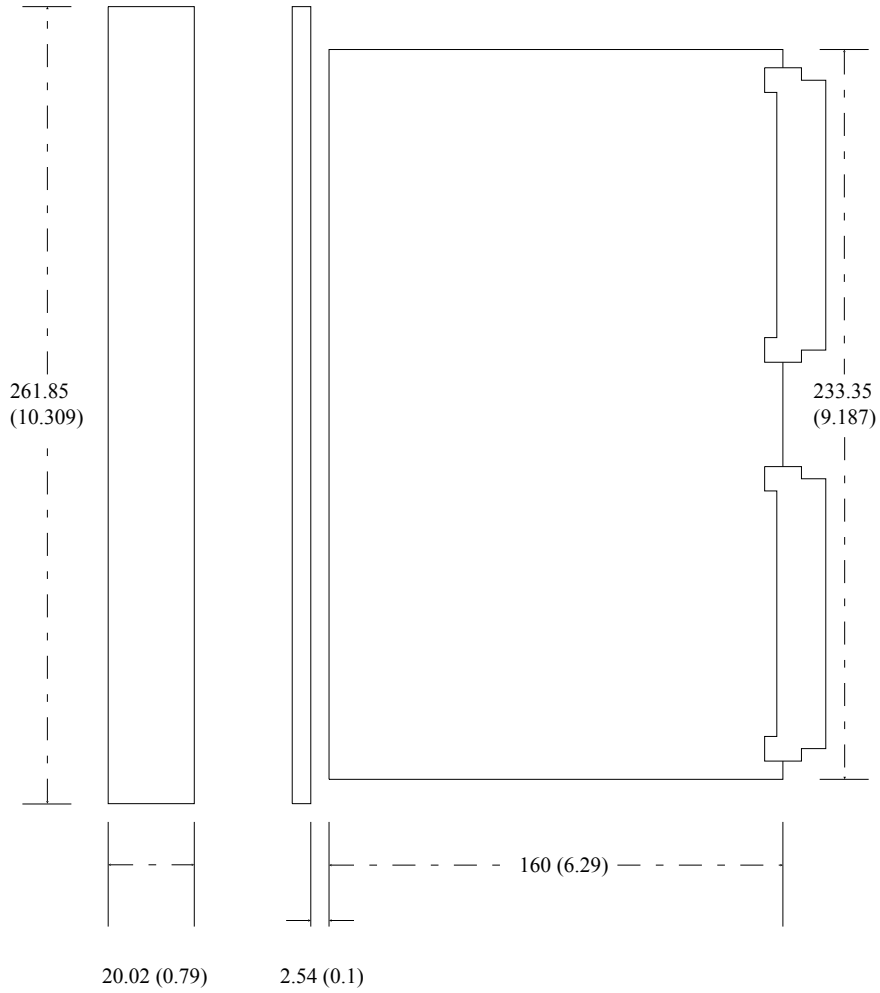
The SIO-4 is a multilayer, single-width, double Eurocard VME board conforming to the VMEbus Specification (ANSI/IEEE Std. 1014-1987) for board size. Figure 3 shows the basic dimensions.

Note: Dimensions are in millimetres, with inches (in parentheses) for reference only.

Figure 4 shows front panel layouts for both the SIO-4 board and its accompanying I/O Extender.

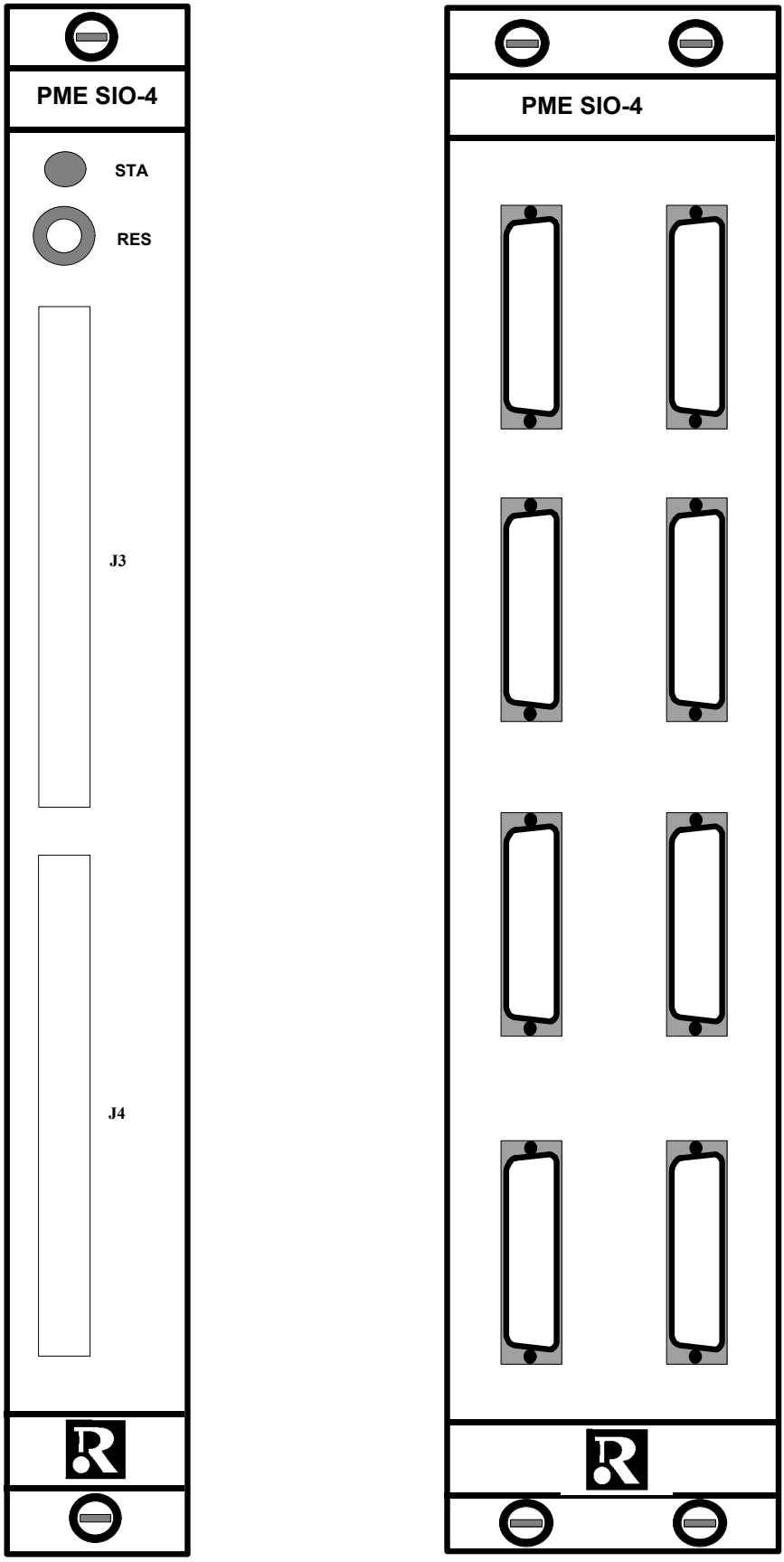
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Figure 3. SIO-4 Physical Dimensions



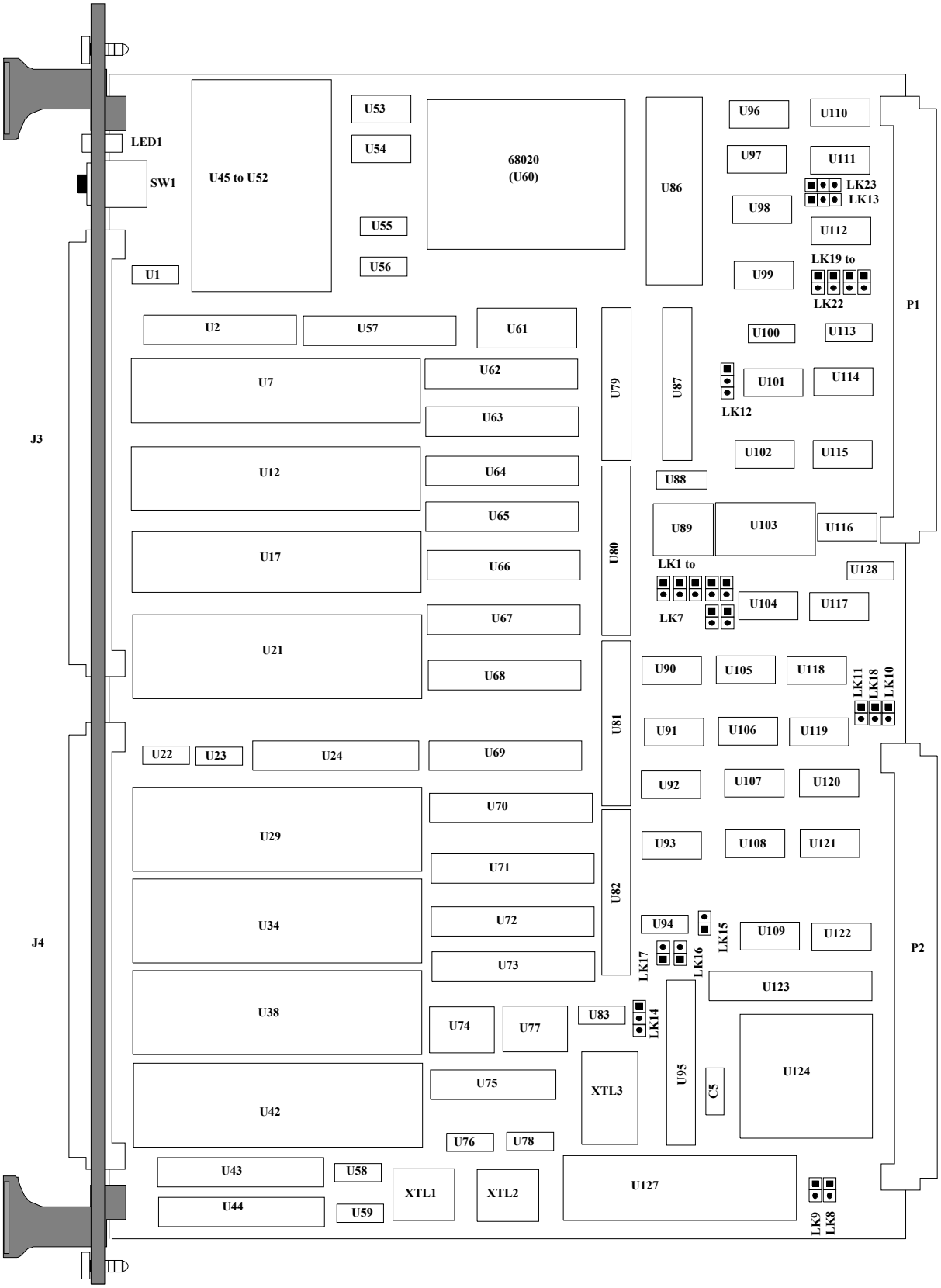
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Figure 4. PME SIO-4 Front Panels



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Figure 5. PME SIO-4 Board Layout



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Chapter 3 - Detailed Description

Introduction

This chapter provides a detailed description of the SIO-4 Serial Communications Controller Card hardware. This section includes a memory map showing the allocation of addresses.

EPROM

The module supports one 32-pin EPROM site using a socket. EPROM sizes between 64 Kbyte and 1 Mbyte can be used. After a hardware reset, the first eight bytes accessed come from the EPROM, to allow a reset vector to be fetched. Four jumpers (LK19, LK20, LK21 and LK22) provide an index into the lower portion of the EPROM, allowing a choice of reset vectors.

Shared Memory

The module contains 1 Mbyte of 32-bit wide local memory dual-ported between the VMEbus and system bus. This memory uses 256k x 4-bit memory devices (1 Mbit). The memory supports read-modify-write and single transfers at all data sizes as well as unaligned transfers. Slave access is at A32, and optionally at A24, at all data widths.

A set of DIL switches sets the start address of the memory when used as a slave. The local memory address can be set to be the same as the slave memory address or at zero (see Memory Maps).

Interrupts

The SIO-4 can be an Interrupt Handler, servicing a combination of on-board interrupts and any link-selected level(s) from the VMEbus. The SIO-4 can also be an Interrupter on any software selected level on the VMEbus.

Interrupt Handler

There are two priorities of interrupts: high and low. The high priority interrupts contain the following levels:

ACFail or System Fail	level 7
DUSCC	level 6
Timer or Diagnostics DUART	level 5
DUARTs	level 4
Mailbox Interrupt	level 3

The low priority interrupts include the interrupts from the VMEbus. The SIO-4 only handles interrupts from the VMEbus that have a jumper link fitted for that level.

> **The SIO-4 services interrupts from high priority levels before those from the low priority levels.**

For example, if a level 3 interrupt from the mailbox occurred with a level 6 interrupt from the VMEbus, the SIO-4 would service the high priority level 3 mailbox interrupt before the low priority level 6 VMEbus interrupt. When no interrupt vector is available for the high priority interrupts, the SIO-4 uses autovectoring.

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The SIO-4 takes the level 7 interrupts (ACFail and System Fail) from the VMEbus. To allow processing to continue, the SIO-4 overrides the interrupt indication from these sources once it has serviced the interrupt. It then removes the interrupt indication when the interrupt completes. The level 7 interrupts are readable, so that their state can be determined when such an interrupt occurs.

Timer Interrupts

A timer interrupt allows operating system clock interrupts.

Mailbox Interrupts

The SIO-4 has mailbox interrupts to support the requirements of multiprocessor operation. It uses the location monitor facility described in the VMEbus specification (ANSI/IEEE Std. 1014-1987). An internal or an external read from memory locations 0x400 to 0x403 generates a mailbox interrupt. The interrupts need to be enabled by writing to specific bits in the control register. The interrupts can be cleared by program control or by a reset, which also disables them.

VME Interrupter

An interrupt can be generated at any level on the VMEbus. The interrupter is a write only register, with addresses from 0xFFE00201 to 0xFFE00207. To generate an interrupt, write the interrupt vector to the location whose least significant byte corresponds to the level of the interrupt. Only one interrupt can be generated at once. A write to address 0xFFE00200 clears any pending interrupts.

Addressing

The addresses for a 1 Mbyte EPROM run from 0xFFF00000 to 0xFFFFFFFF. EPROMs of less than 1 Mbyte have multiple windows within the 1 Mbyte address field. All the other peripherals occupy multiple 1 Kbyte windows in the address range 0xFFE00000 to 0xFFEFFFFF.

DUSCC (optional)

The internal registers of the 68562 DUSCC are from address 0xFFE00000 to 0xFFE0003F. The synchronous communications interface requires the monitoring and control of more signals than the DUSCC can handle. The SIO-4 therefore provides two extra registers (one read and one write) for the other functions. These registers are at address 0xFFE00040 and are described overleaf.

The TTL level signals are brought out on P2.

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DUSCC Write Register

This is at address 0xFFE00040.

Data Bit	Description	Signal Name on P2
0	Signal rate 1 (DTE)	DTERATE1
1	Signal rate 2 (DTE)	DTERATE2
2	Local loopback 1	SLOCLOOP1
3	Local loopback 2	SLOCLOOP2
4	Remote loopback 1	SREMLOOP1
5	Remote loopback 2	SREMLOOP2
6	Spare 1	-
7	Spare 2	-

DUSCC Read Register

This is at address 0xFFE00040.

Data Bit	Description	Signal Name on P2
0	Spare 1	-
1	Spare 2	-
2	Test Indicator Group 2	STEST2
3	Ring Indicator Group 2	SRING2
4	Signal Rate Group 2 (DCE)	DCERATE2
5	Test Indicator Group 1	STEST1
6	Ring Indicator Group 1	SRING1
7	Signal Rate Group 1 (DCE)	DECRATE1

You can also monitor any of the above in groups by reading the Input and Counter/Timer Status Register (ICTSR) of the DUSCC. Bit 1 of ICTSRA monitors the port 1 group inputs and bit 1 of ICTSRB monitors the port 2 group inputs.

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DUARTs

There are nine DUARTs (type 68681) on this module. Eight of them provide sixteen V.24 user ports and one gives diagnostics. The following table gives the DUART register addresses:

DUART	Address (Hex)		Description
	From	To	
1	FFE00100	FFE0010F	ports 1 (side A) and 2 (side B)
2	FFE00110	FFE0011F	ports 3 (side A) and 4 (side B)
3	FFE00120	FFE0012F	ports 5 (side A) and 6 (side B)
4	FFE00130	FFE0013F	ports 7 (side A) and 8 (side B)
5	FFE00140	FFE0014F	ports 9 (side A) and 10 (side B)
6	FFE00150	FFE00 15F	ports 11 (side A) and 12 (side B)
7	FFE00160	FFE0016F	ports 13 (side A) and 14 (side B)
8	FFE00170	FFE0017F	ports 15 (side A) and 16 (side B)
9	FFE00180	FFE0018F	diagnostics port: side A connects to a terminal and side B to a host

Address Modifier Register (AMRWR)

This is a write only register, at 0xFFE00300. It allows software to provide Address Modifier Bits (AM0 to 5). The module uses these when acting as a master.

Bit	Mnemonic	Meaning
0	AMS0	Address modifier source bit 0
1	AMS1	Address modifier source bit 1
2	AMS2	Address modifier source bit 2
3	AMS3	Address modifier source bit 3
4	AMS4	Address modifier source bit 4
5	AMS5	Address modifier source bit 5
6	AMAS	Address Modifier Alternate Source
7	SREG	Select Address Modifier Register

For **SREG** = 0, use the local memory map to generate the address modifier bits:

VME access at addresses 0x00000000 to 0xFDFFFFFF = A32/D32
VME access at addresses 0xFE000000 to 0xFEFFFFFF = A24/D16
VME access at addresses 0xFF000000 to 0xFFDFFFFF = A16/D16

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For **SREG** = 1, use the Address Modifier Source Register:

If **AMAS** = 0, then AM0 to 5 = **AMS0** to 5
If **AMAS** = 1, then AM0 to 2 = CPU FC0 to 2 and AM3 to 5 = **AMS3** to 5

Control Register (FLGWRI)

This is a write only register at address 0xFFE00301.

Bit	Contents
0	SP0 (space type 0)
1	SP1 (space type 1)
2	LMEXTEN
3	LMINTEN
4	JUMP
5	Spare/Remote Reset Enable
6	LSFAIL 1
7	LSFAIL 2

SP0 and **SP1** control the types of accesses to which the slave can respond:

SP1	SP0	Access Type
1	1	Supervisor and User Data, Supervisor and User Code
1	0	Supervisor Data and Supervisor Code
0	1	Supervisor and User Data
0	0	Supervisor Data

Do not change the space type while the card is acting as a slave.

Clearing **LMEXTEN** locks out the location monitor interrupt, via the VMEbus. Clearing **LMINTEN** locks out the location monitor interrupt, via the internal accesses.

Setting **JUMP** allows access to the VME locations that internal accesses to the local RAM and the peripheral space normally mask out. Setting JUMP inverts CPU address bit 31 before sending it on the VMEbus. A master access to the most significant locations at the bottom half of the store range effectively accesses VME locations that the peripheral address space would otherwise mask out. A master access to the least significant locations at the top half of the store range effectively accesses VME locations that the local RAM address space would otherwise mask out.

If **POP 7** is fitted, bit 5 becomes the **Remote Reset Enable** bit. If not, the bit is spare. To enable the remote reset, set bit 5. To disable the remote reset, clear bit 5 or activate a reset.

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LSFAIL1 and **LSFAIL2** can produce a system fail during the power-up sequence, on reset or under program control. System fail can be selected, by a jumper, to either set or clear on power-up.

LSFAIL 1	LSFAIL 2	System Fail
0	0	Same as in power-up sequence
0	1	Clear system fail
1	0	Set system fail
1	1	Opposite to that in power-up sequence

Read Flags (RDFLG)

This is a read only register, at address 0xFFF00302, used to monitor flags on the module.

Bit	Meaning
0	Not used
1	Not used
2	DUSCFIT
3	BRL0
4	BRL1
5	ACFAIL
6	SFAIL
7	LSFAIL

DUSCFIT is 1 (no jumper fitted) when there is a DUSCC fitted.

BRL0 and **BRL1** show the VMEbus request priority level selection (1 = relevant jumper fitted).

BRL0	BRL1	Bus Request Priority
1	1	BR3*
1	0	BR2*
0	1	BR1*
0	0	BR0*

ACFAIL is 0 when there is an AC Fail on the VMEbus. This signal also causes a level 7 interrupt. After the SIO-4 services the interrupt, it overrides the interrupt until AC Fail is removed from the VMEbus. AC Fail can be monitored while it is present on the VMEbus.

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SFAIL shows the state of the VME system fail or local system fail. **LSFAIL** shows the state of the local system fail only.

SFAIL	LSFAIL	Meaning
0	0	Local system fail and maybe VME system fail
0	1	VME system fail only
1	0	This combination can never occur
1	1	Both system fails are clear

Read Switches 1 and 2 (RDSW1, RDSW2)

RDSW1 is a read only register at address 0xFFE00300. It shows the state of the eight most significant switches that select the VME slave window.

Bit	Switch
0	SelA24
1	SelA25
2	SelA26
3	SelA27
4	SelA28
5	SelA29
6	SelA30
7	SelA31

RDSW2 is a read only register at address 0xFFE00301. It shows the state of the four least significant switches that select the VME slave window. This register also allows monitoring of various other conditions.

Bit	Switch
0	LSEL0
1	SEL0
2	SELSL24
3	Reserved
4	SELA20
5	SELA21
6	SELA22
7	SELA23

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LSEL0 and **SEL0** show the start address of the local RAM window. If LSEL0 = 1, then the local RAM is at address 0x00000000. If LSEL0 = 0, then the local RAM address is the same as the slave RAM address. If the slave RAM address is within the top 256 Mbyte of the address range, then the local RAM address is forced to be at 0x00000000. This is because the peripherals occupy the top 256 Mbyte space, and so the local RAM address cannot use it.

LSEL0	SEL0	Meaning
0	0	Local address forced to be 0x00000000 (see above)
0	1	Local address same as slave address
1	0	Local address set at 0x00000000
1	1	Invalid code

When **SELSL24** is 0, the slave responds to A32/D32 accesses only. When **SELSL24** is 1, the slave responds to A24/D16 and A32/D32 accesses.

Clear Mailbox Interrupt (CLVINT)

This is a write only register at address 0xFFE00303. Accessing CLVINT clears the location monitor virtual interrupt. The data bits in this register are irrelevant.

DUSCC General Purpose I/O Pins

Signal	Meaning
GPI1A	DSR1
GPI1B	DSR2
GPI2A	Port 1 group monitor
GPI2B	Port 2 group monitor
GPO1A	DTR1
GPO1B	DTR2
GPO2A	A low on this output enables the transmitter clock (DCE source) of port 1 onto TRXCA
GPO2B	A low on this output enables the transmitter clock (DCE source) of port 2 onto TRXCA

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DUART General Purpose I/O (User)

Signal	Meaning
IP0	CTSA
IP1	CTSB
IP2	DCDA
IP3	DCDB
IP4	DSRA
IP5	DSRB
OP0	RTSA
OP1	RTSB
OP6	DTRA
OP7	DTRB

DUART General Purpose I/O (Diagnostics)

Signal	Meaning
IP0	CTS(T)
IP1	CTS(H)
IP2	1 MHz clock input for timer
IP3	INTEN
IP4	DFIT1
IP5	DFIT2
OP0	RTS(T)
OP1	RTS(H)
OP3	Timer output

When **INTEN** is low, the VME interrupter is busy. The DUART can be programmed to interrupt the CPU, when the VME interrupter becomes free.

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DFIT1 and **DFIT2** are inputs that show the number of user DUARTs the SIO-4 has fitted (1 = relevant jumper fitted).

DFIT1	DFIT2	Meaning
0	0	All user DUARTs fitted
0	1	DUARTs 1 to 4 fitted
1	0	Spare
1	1	No DUARTs fitted

Interfaces

The module has a VMEbus interface conforming to ANSI/IEEE Std. 1014-1987. The interface can support 32 address and 32 data bits. This includes master and slave operation, interrupter and interrupt handler.

A jumper selects VMEbus System Fail (SYSFAIL*) to either set or clear on a reset. It is possible to set and clear it, by an access from the processor to the peripheral field.

A low level on the line System Reset (SYSRESET*) results in a reset to the whole module. Low levels on the inputs AC Fail (ACFAIL*) and System Fail (SYSFAIL*), generate interrupts to the on-card processor at level seven.

Tables 1 and 2 show the connectors' pin-outs.

Read-Modify-Write

This module does not support the CAS2 read-modify-write instruction over the VMEbus. It only supports aligned read-modify-write accesses.

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Table 1. Pin Assignment P1 (VME)

Pin Number	Row a Signal	Row b Signal	Row c Signal
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	**D03**	**BG0IN***	**D11**
5	**D04**	**BG0OUT***	**D12**
6	**D05**	**BG1IN***	**D13**
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	**SYSCLK**	**BG3IN***	**SYSFAIL***
11	**GND**	**BG3OUT***	**BERR***
12	**DS1***	**BR0***	**SYSRESET***
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	**DTACK***	**AM0**	**A22**
17	**GND**	**AM1**	**A21**
18	**AS***	**AM2**	**A20**
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	**IACKOUT***	**SERDAT***	**A16**
23	**AM4**	**GND**	**A15**
24	**A07**	**IRQ7***	**A14**
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	**A03**	**IRQ3***	**A10**
29	**A02**	**IRQ2***	**A09**
30	**A01**	**IRQ1***	**A08**
31	-12V	+ 5VSTDBY	+ 12V
32	+ 5V	+ 5V	+ 5V

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Table 2. Pin Assignment P2

Pin	Row a	Row b (VME)	Row c
1	NU	+ 5V	NU
2	DCETXCLK1 (DU)	GND	TXDA (DU)
3	NU	NU	RXDA (DU)
4	**RTXCA (DU)**	**A24**	**RTSA (DU)**
5	**SLOCLOOP1 (DU)**	**A25**	**CTSA (DU)**
6	**NU**	**A26**	**RTXDA (DU)**
7	RTXDA (DU)	A27	0 V (DU)
8	SREMLOOP1 (DU)	A28	DCDA (DU)
9	SRING1 (DU)	A29	NU
10	**DTERATE1 (DU)**	**A30**	**NU**
11	**TRXCA (DU)**	**A31**	**NU**
12	**STEST1 (DU)**	**GND**	**DCERATE1 (DU)**
13	NU	+ 5V	NU
14	TXDB (DU)	D16	NU
15	RXDB (DU)	D17	DCETXCLK2 (DU)
16	**RTSB (DU)**	**D18**	**NU**
17	**CTSB (DU)**	**D19**	**RTXCB(DU)**
18	**RTXDB (DU)**	**D20**	**SLOCLOOP2 (DU)**
19	0 V (DU)	D21	NU
20	DCDB (DU)	D22	RTXDB (DU)
21	NU	D23	SREMLOOP2 (DU)
22	**NU**	**GND**	**SRING2 (DU)**
23	**NU**	**D24**	**DTERATE2 (DU)**
24	**DCERATE2 (DU)**	**D25**	**TRXCB (DU)**
25	NU	D26	STEST2 (DU)
26	NU	D27	NU
27	NU	D28	NU
28	**CTST (DD)**	**D29**	**NU**
29	**RTST (DD)**	**D30**	**RXDT (DD)**
30	**0 V (DD)**	**D31**	**TXDT (DD)**
31	RXDH (DD)	GND	CTSH (DD)
32	TXDH (DD)	+ 5V	RTSH (DD)

NU = Not used (no connection)

DU = DUSCC signal

DD = Diagnostic DUART signal

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V.24 Asynchronous Ports

The SIO-4 has sixteen serial asynchronous V.24 ports, using type 68681 DUARTs. They can be configured for operation up to 38,400 baud using the internal clock.

The module offers two further asynchronous V.24 ports, which provide either diagnostic or remote operation of the board. One of these ports connects to a terminal and the other to a host, from which code can be downloaded and run.

The SIO-4 also offers an option of two synchronous ports, using a 68562 Dual Universal Synchronous Communications Controller (DUSCC).

V.24 Serial Ports

The sixteen V.24 serial asynchronous ports use 68681 Dual Universal Asynchronous Receiver/Transmitters (DUARTs). Each port is configurable for speeds of between 50 and 38,400 baud. Each port is also configurable for split speed operation, 5 to 8 bits per character, number of stop bits, and odd, even or no parity.

Two 64-way ribbon cables take the signals off the board. The configuration of each 64-way cable means that it can be split into eight separate 8-way ribbon cables and finish with 9-way D-type connectors. See Tables 3 to 5 for the pin assignment of these connectors.

Table 3. 9-Way D-Type Connector Pin-Out

Pin	Signal	Type	Edge Connector Signals
1	Txdata	Output	TXDATA
2	Request To Send	Output	RTS
3	Data Set Ready	Input	DSR
4	Data Terminal Ready	Output	DTR
5	Not Used		
6	Rxdata	Input	RXDATA
7	Clear To Send	Input	CTS
8	Signal Gnd		
9	Data Carrier Detect	Input	DCD

Txdata	This signal is the serial data output from the SIO-4.
Rxdata	This signal is the serial data input to the SIO-4.
Request To Send	This signal is an output from the SIO-4. It can be programmed as a receiver busy signal or as a transmitter request signal.
Clear To Send	This signal is an input to the SIO-4. It may be used to inhibit the transmitter when the receiving device is busy.
Data Set Ready	This signal is an input to the SIO-4. A modem uses the signal to show that it is powered on and ready.

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Data Carrier Detect	This signal is an input to the SIO-4. A modem uses the signal to show the loss of the received input signal.
Data Terminal Ready	This signal is an output from the SIO-4. It tells a modem that the SIO-4 is active.

Note: The interface is connected by eight wires only.

You can also use the CTS input as a ring indicator input. This is selected externally to the module.

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Table 4. Pin Assignment J3

Pin Number	Row A	Row B
1	RXDATA1	TXDATA1
2	CTS1	RTS1
3	SIG GND1	DSR1
4	**DCD1**	**DTR1**
5	**RXDATA2**	**TXDATA2**
6	**CTS2**	**RTS2**
7	SIG GND2	DSR2
8	DCD2	DTR2
9	RXDATA3	TXDATA3
10	**CTS3**	**RTS3**
11	**SIG GND3**	**DSR3**
12	**DCD3**	**DTR3**
13	RXDATA4	TXDATA4
14	CTS4	RTS4
15	SIG GND4	DSR4
16	**DCD4**	**DTR4**
17	**RXDATA5**	**TXDATA5**
18	**CTS5**	**RTS5**
19	SIG GND5	DSR5
20	DCD5	DTR5
21	RXDATA6	TXDATA6
22	**CTS6**	**RTS6**
23	**SIG GND6**	**DSR6**
24	**DCD6**	**DTR6**
25	RXDATA7	TXDATA7
26	CTS7	RTS7
27	SIG GND7	DSR7
28	**DCD7**	**DTR7**
29	**RXDATA8**	**TXDATA8**
30	**CTS8**	**RTS8**
31	SIG GND8	DSR8
32	DCD8	DTR8

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Table 5. Pin Assignment J4

Pin Number	Row A	Row B
1	RXDATA9	TXDATA9
2	CTS9	RTS9
3	SIG GND9	DSR9
4	**DCD9**	**DTR9**
5	**RXDATA10**	**TXDATA10**
6	**CTS10**	**RTS10**
7	SIG GND10	DSR10
8	DCD10	DTR10
9	RXDATA11	TXDATA11
10	**CTS11**	**RTS11**
11	**SIG GND11**	**DSR11**
12	**DCD11**	**DTR11**
13	RXDATA12	TXDATA12
14	CTS12	RTS12
15	SIG GND12	DSR12
16	**DCD12**	**DTR12**
17	**RXDATA13**	**TXDATA13**
18	**CTS13**	**RTS13**
19	SIG GND13	DSR13
20	DCD13	DTR13
21	RXDATA14	TXDATA14
22	**CTS14**	**RTS14**
23	**SIG GND14**	**DSR14**
24	**DCD14**	**DTR14**
25	RXDATA15	TXDATA15
26	CTS15	RTS15
27	SIG GND15	DSR15
28	**DCD15**	**DTR15**
29	**RXDATA16**	**TXDATA16**
30	**CTS16**	**RTS16**
31	SIG GND16	DSR16
32	DCD16	DTR16

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Synchronous Ports (Optional)

The two synchronous ports use a 68562 Dual Universal Synchronous Communications Controller (DUSCC). Each port is configurable for speeds between 50 and 38,400 baud. The hardware can support BiSync, SDLC, HDLC and X25 protocols.

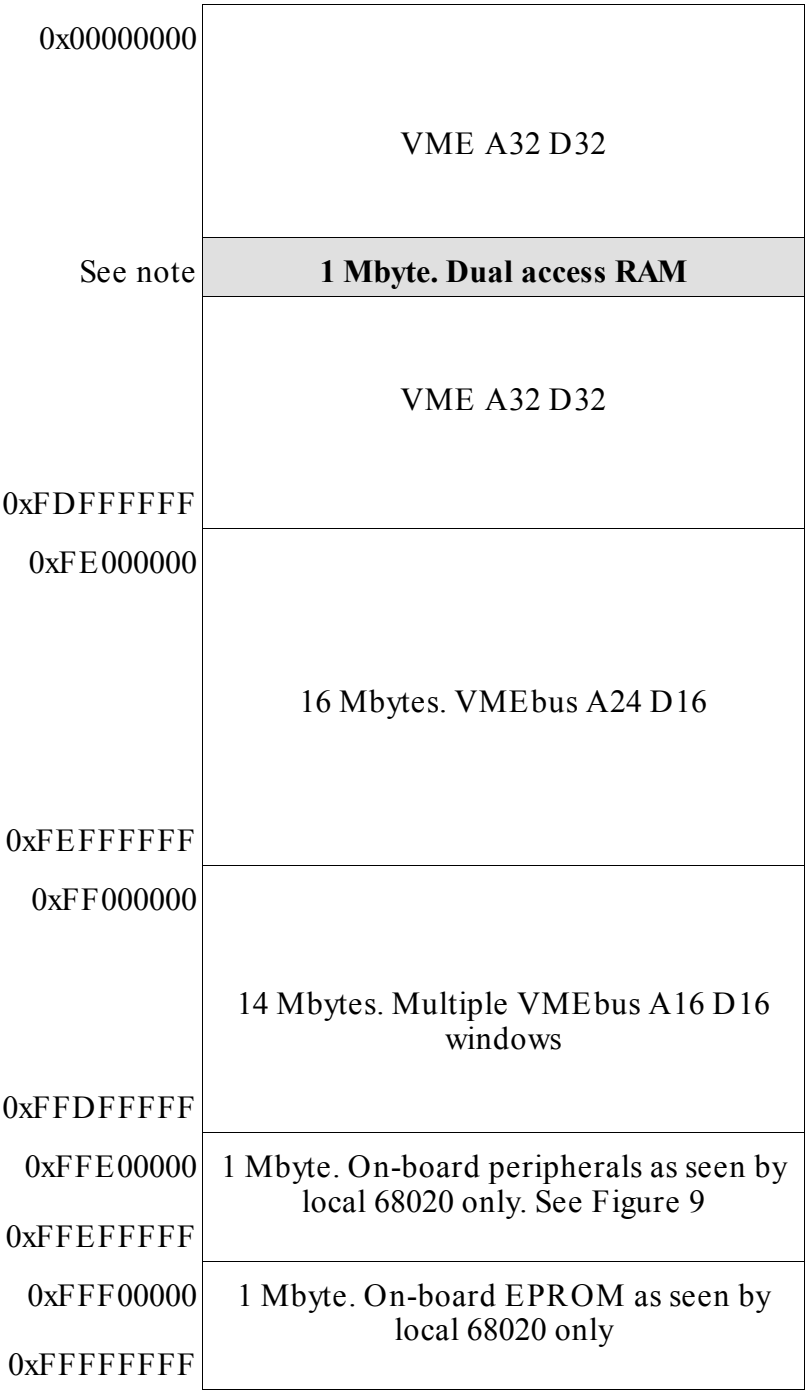
Table 2 shows the P2 connector pin-out (the two synchronous ports use the remaining two rows of connections of the VMEbus P2 connector). The TTL level signals are also brought out via P2.

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Memory Maps

Master Accesses from 68020 Processor

Figure 6. 68020 Processor Memory Map

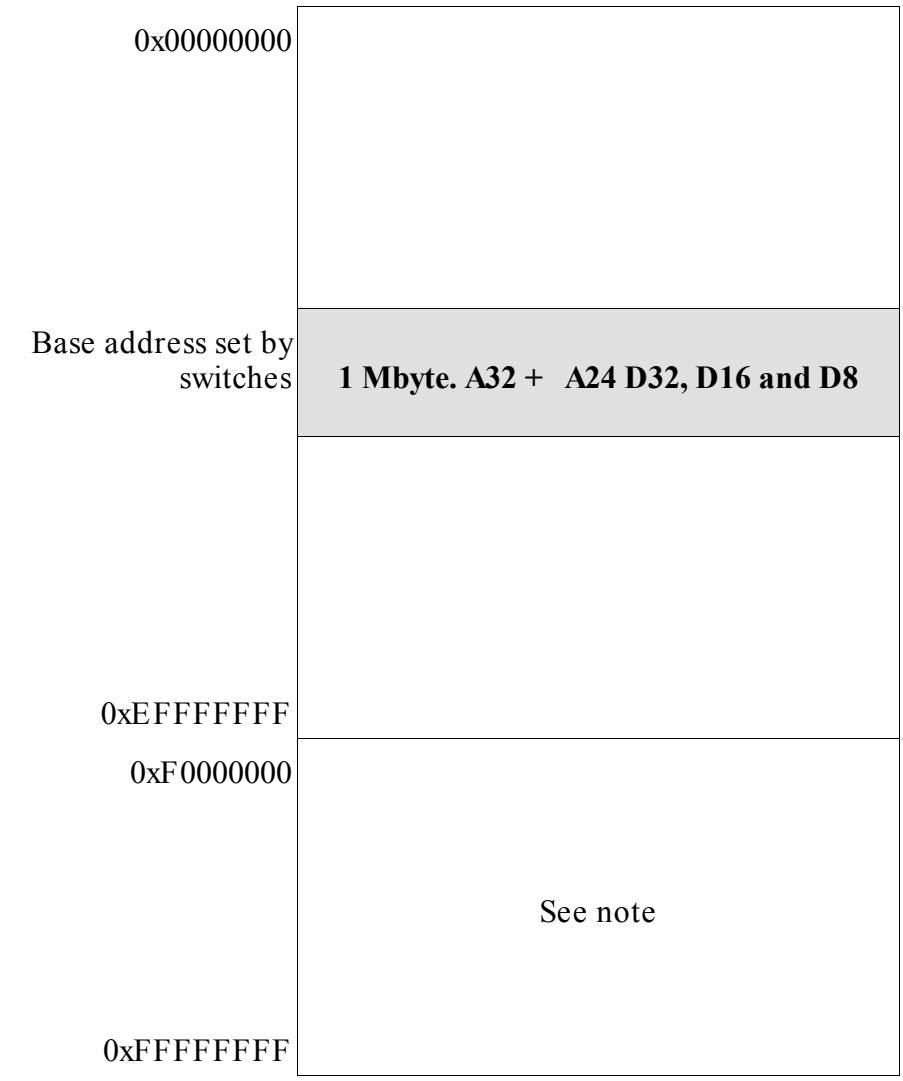


Note: Base address is either 0x00000000 or the address specified by the Slave Select Switches (Link 11 selects between these options). See Figures 7 and 8. For example if the VMEbus slave address is 0xD0000000 and link 11 is fitted, then the 68020 accesses the local RAM at 0xD0000000.

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Slave Accesses

Figure 7. Slave Address Memory Map



Note: In this region, if LK11 is fitted so that the 68020 accesses the dual access RAM at the same address as the VMEbus slave address, there would be a conflict with other local resources. The 68020 is therefore 'forced' to see the RAM at 0x00000000 instead of the VMEbus slave address. See figure 8.

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Figure 8. 1Mbyte Local RAM Window

0x00000000 0x000003FF	M68020 Vector Table
0x00000400	Location Monitor
0x00000404	Board ID Check Code (0x42456546)
0x00000408	Status Word
0x0000040C	Board Type Code (SIOP), loaded from EPROM
0x00000410	Supplementary Type Information, e.g. options
0x00000414	Reserved for future use
0x00000418	Board Firmware Revision Number, loaded from EPROM
0x0000041C	WARM Start Flag
0x00000420	Location Monitor Data Structure Base Pointer
0x00000424	EPROM Number
0x00000428	EPROM Issue Number
0x0000042C 0x0000042F	Reserved for future use
0x00000430	Remote reset (POP 7)
0x00000434 0x0000043F	Reserved for future use
0x00000440 0x0000047F	Self test results (bit pattern, 64 bytes)
0x00000480	Loader Command Poll Address
0x00000484	Firmware Go Address Qualifier
0x00000488	Firmware Go Address
0x0000048C 0x0000049F	Reserved for future Loader use
0x000004A0 0x00002DFC	RT/M Workspace

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Figure 8 continued

0x00002E00 0x00002EFC	FIFO size communication area
0x00002F00	Debug flag
0x00002F04	Fatal error code word
0x00002F08	Reserved
0x00002F0C	Reserved
0x00002F10	BF_CMD
0x00002F14	BF_MODIFIER
0x00002F18	BF_ARG1
0x00002F1C	BF_ARG2
0x00002F20	BF_ARG3
0x00002F24	BF_ARG4
0x00002F28 0x00002F3C	Reserved
0x00002F40	Firmware structures base pointer, FSBP

The board ID check code (0x00000404) and status word (0x00000408) are set up within five seconds of power-on. If they are not, then the host does not recognise the card as a Radstone VME card.

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Peripheral Accesses (can only be accessed by 68020 processor)

Figure 9. Multiple 1 Kbyte Windows in 1 Mbyte Space

0xFFE00000 0xFFE0003F	DUSCC
0xFFE00040	DUSCC Miscellaneous Registers
0xFFE00041 0xFFE000FF	Unused
0xFFE00100 0xFFE0010F	DUART port 1 (side A) and port 2 (side B)
0xFFE00110 0xFFE0011F	DUART port 3 (side A) and port 4 (side B)
0xFFE00120 0xFFE0012F	DUART port 5 (side A) and port 6 (side B)
0xFFE00130 0xFFE0013F	DUART port 7 (side A) and port 8 (side B)
0xFFE00140 0xFFE0014F	DUART port 9 (side A) and port 10 (side B)
0xFFE00150 0xFFE0015F	DUART port 11 (side A) and port 12 (side B)
0xFFE00160 0xFFE0016F	DUART port 13 (side A) and port 14 (side B)
0xFFE00170 0xFFE0017F	DUART port 15 (side A) and port 16 (side B)
0xFFE00180 0xFFE0018F	Diagnostics DUART side A - terminal, side B - host
0xFFE00190 0xFFE0019F	Unused

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Figure 9 continued

0xFFE00200 0xFFE00207	VME Interrupter
0xFFE00208 0xFFE002FF	Unused
0xFFE00300	AMRWR - Address Modifier Register (write) RDSW1 - Read RAM Start Address Switch (read)
0xFFE00301	FLGWR1 - Miscellaneous flags (write) RDSW2 - Read RAM Start Address Switch (read)
0xFFE00302	RDFLG - Miscellaneous flags (read)
0xFFE00303	CLVINT - Clear Virtual Interrupt (write)
0xFFE00304 0xFFE003FF	Unused

Remote Reset

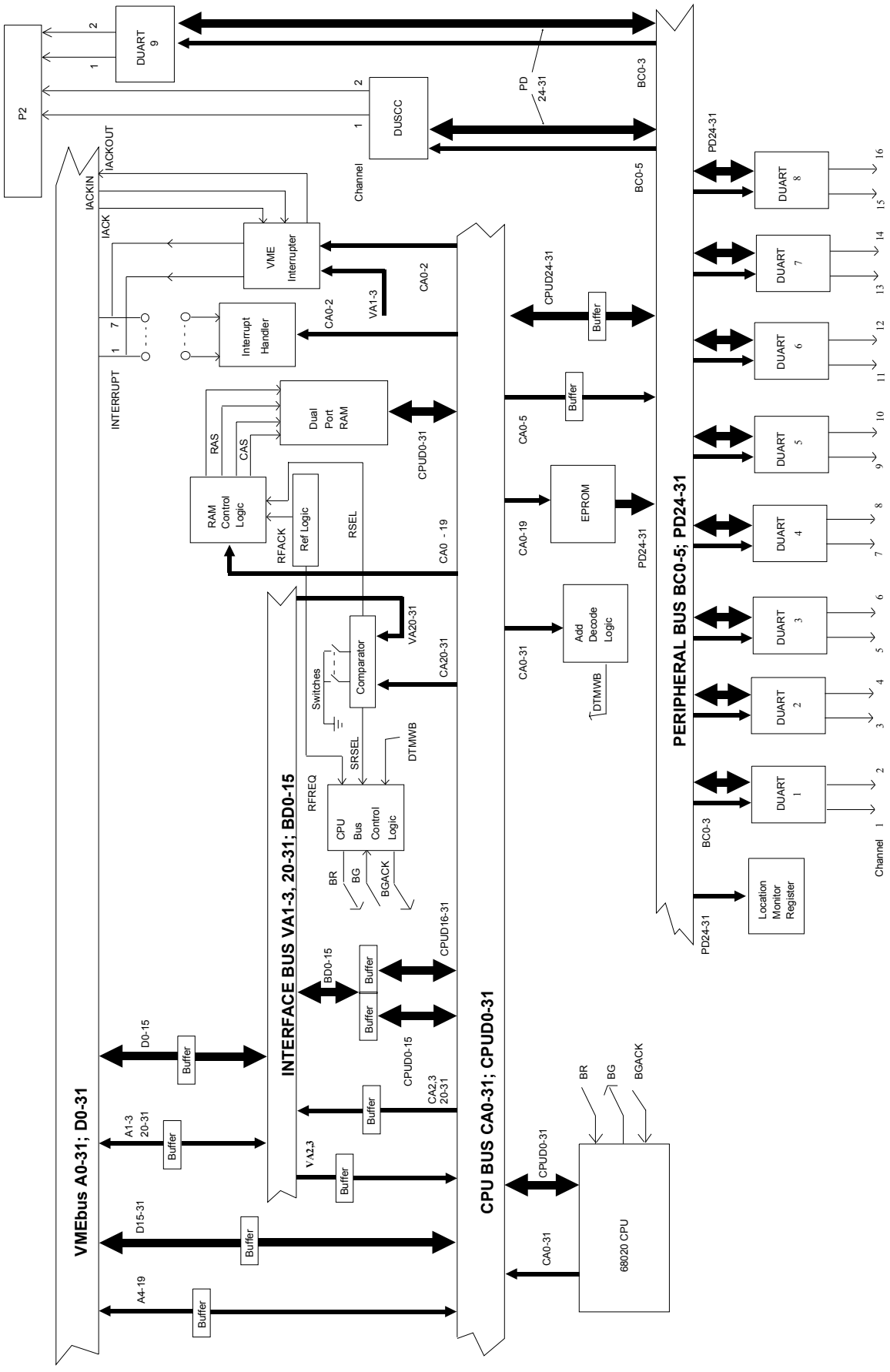
The SIO-4 may be reset remotely without the use of either the Reset button or VME SYSRESET. This facility only exists if POP 7 is fitted. The reset is generated by a 2 stage operation:

1) The reset has to be enabled by writing a 1 to bit 5 of FLGWR1 Control Register.

2) An access, of any type, needs to be made to location 0x00000430 to start the reset.

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Figure 10. Detailed Block Diagram



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Chapter 4 - Configuration

Introduction

This chapter describes how to configure the SIO-4 controller by jumper links.

Switches and Indicators

The SIO-4 has a push-button switch (SW1), shown in Figure 11, that generates an internal reset when pressed.

Dual-In-Line (DIL) switches provide a start address for the slave memory.

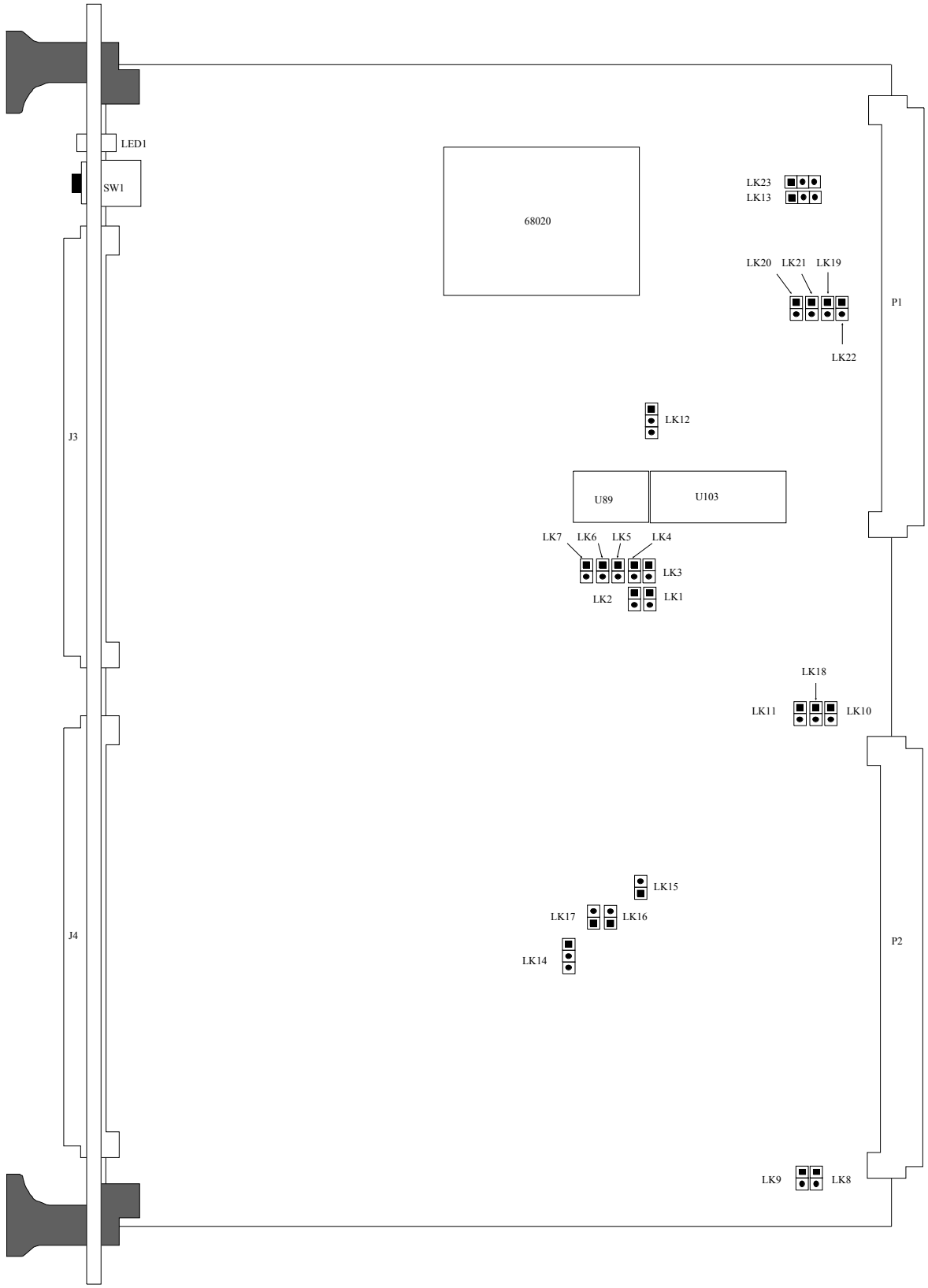
There is a dual-colour LED on the module. When the module has generated a Halt and the system has stopped, this LED shows red. When the system is running with SYSFAIL clear, this LED shows green. When the module is running with SYSFAIL set, both red and green segments are illuminated, producing a yellow colour.

Jumper Settings

Figure 11 shows the position of the jumper links and Table 6 lists the signals associated with each jumper. In the diagrams, a square pin denotes pin 1; pins are then numbered sequentially (2, 3 etc.).

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Figure 11. PME SIO-4 DIL Switch and Link Location



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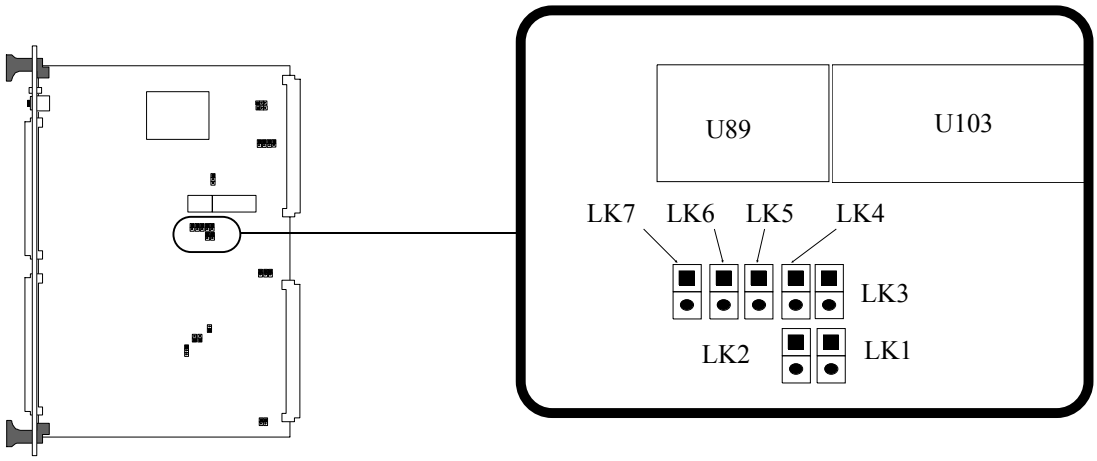
Table 6. Jumper Link/Signal Lines

Jumper	Signal	Default Setting	Comments
1	IRQ1	Out	
2	IRQ2	Out	
3	IRQ3	Out	
4	IRQ4	Out	
5	IRQ5	Out	
6	IRQ6	Out	
7	IRQ7	Out	
8	DFIT1	Out	
9	DFIT2	Out	
10	Reserved	Out	
11	LSEL0	Out	
12	ROA19	2 to 3	
13	ROA18	2 to 3	
14	LSFAIL	1 to 2	
15	DUSCFIT	In	POP 3 not fitted
16	BRL0	In	
17	BRL1	In	
18	SELSL24	Out	
19	SELA6	In	POP 4 fitted
20	SELA5	In	
21	SELA4	In	
22	SELA3	In	
23	ROA17	1 to 2	

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IRQ1 to IRQ7 (Links 1 to 7)

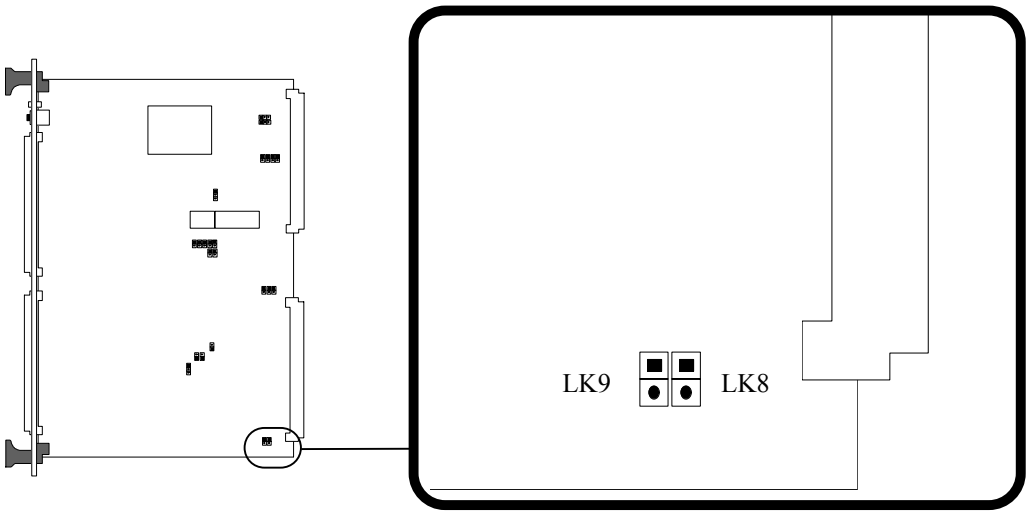
Fitting the appropriate jumper monitors the corresponding VME interrupt level (e.g. LK3 in = level 3 monitored). The default is no jumpers fitted.



DFIT1 and DFIT2 (Links 8 and 9)

The following table lists the settings that the resident firmware uses to test the user DUARTs fitted:

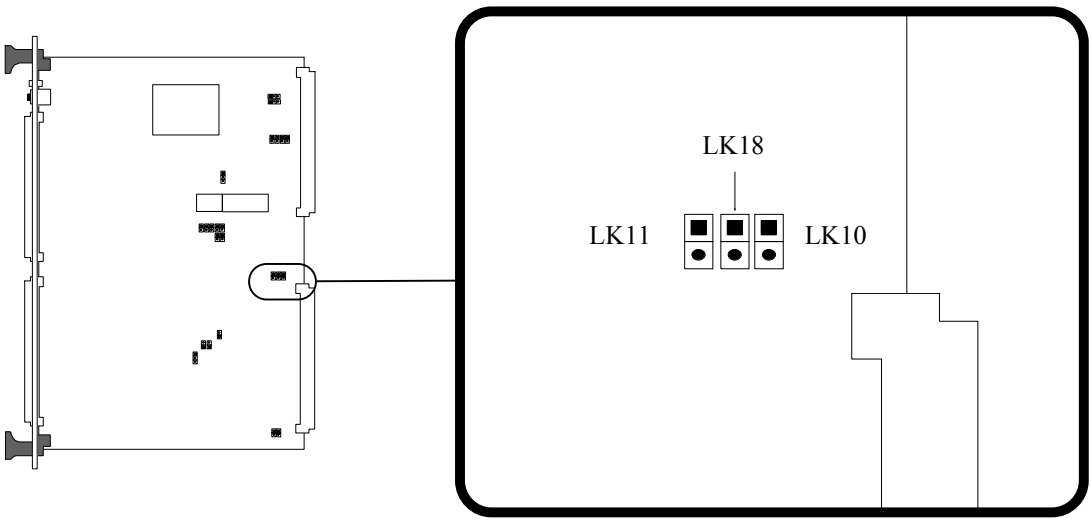
DFIT1	DFIT2	Meaning
Out	Out	Eight user DUARTs (1 to 8) fitted (default)
Out	In	Four user DUARTs (1 to 4) fitted
In	Out	Reserved
In	In	No user DUARTs fitted



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LSEL0 (Link 11)

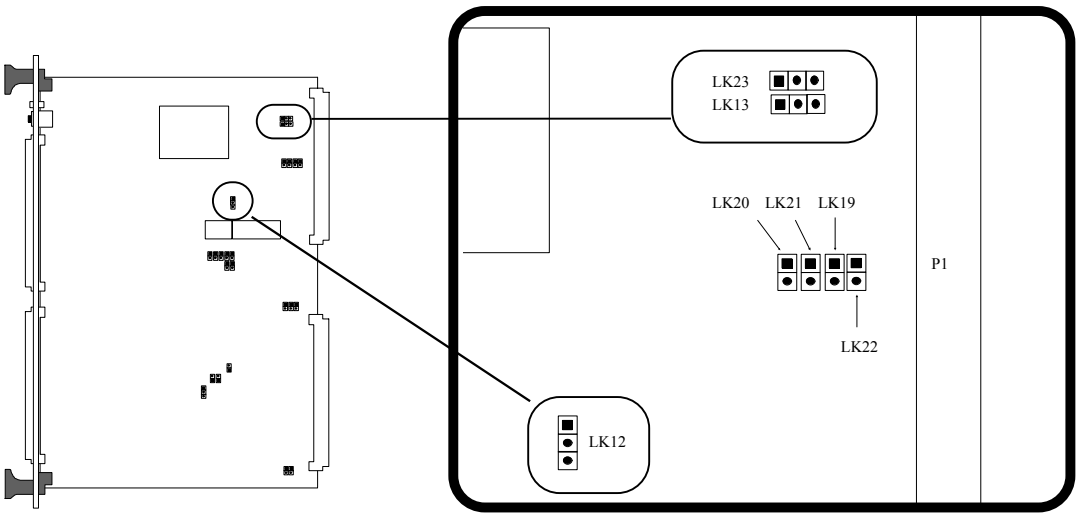
If this jumper is not fitted, the local RAM address is 0 (the default). If the jumper is fitted, the local RAM address window is the same as the VME slave RAM window.



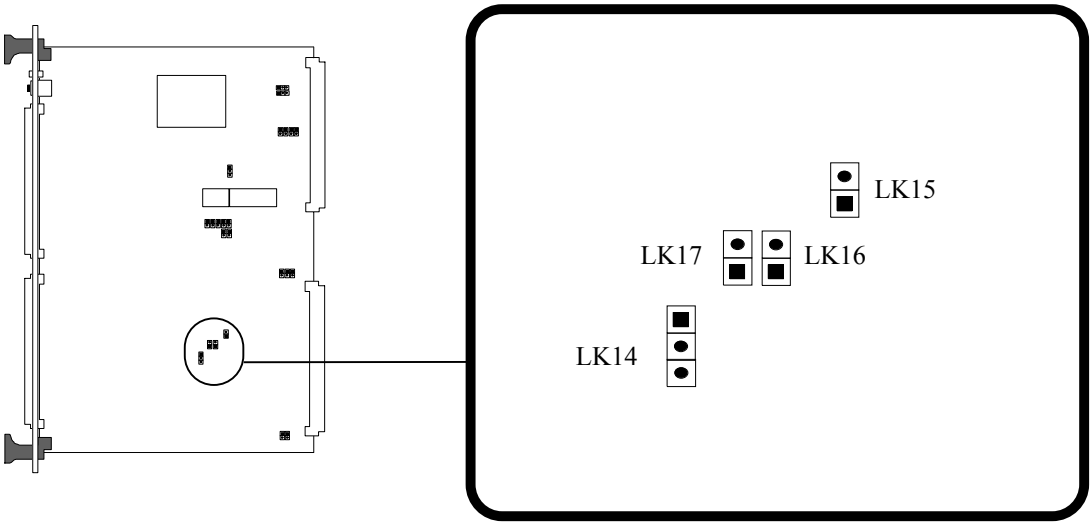
ROA17 to ROA19 (Links 12, 13 and 23)

These links decide the PROM size.

ROA17 (LK23)	ROA18 (LK13)	ROA19 (LK12)	PROM Size
2 to 3	Out	Out	64 Kbytes
Out	2 to 3	2 to 3	128 Kbytes (default)
1 to 2	2 to 3	2 to 3	256 Kbytes
1 to 2	1 to 2	2 to 3	512 Kbytes
1 to 2	1 to 2	1 to 2	1 Mbyte



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LSFAIL (Link 14)

If LK14 is linked pin 1 to pin 2, the local system fail is set on power-up (the default). If LK14 is linked pin 2 to pin 3, the local system fail is clear on power-up.

DUSCFIT (Link 15)

If this jumper is fitted, it shows that the DUSCC is not present (the default). If LK15 is not fitted, then the DUSCC is present. The resident firmware uses this to check whether the DUSCC is present before the self-test runs.

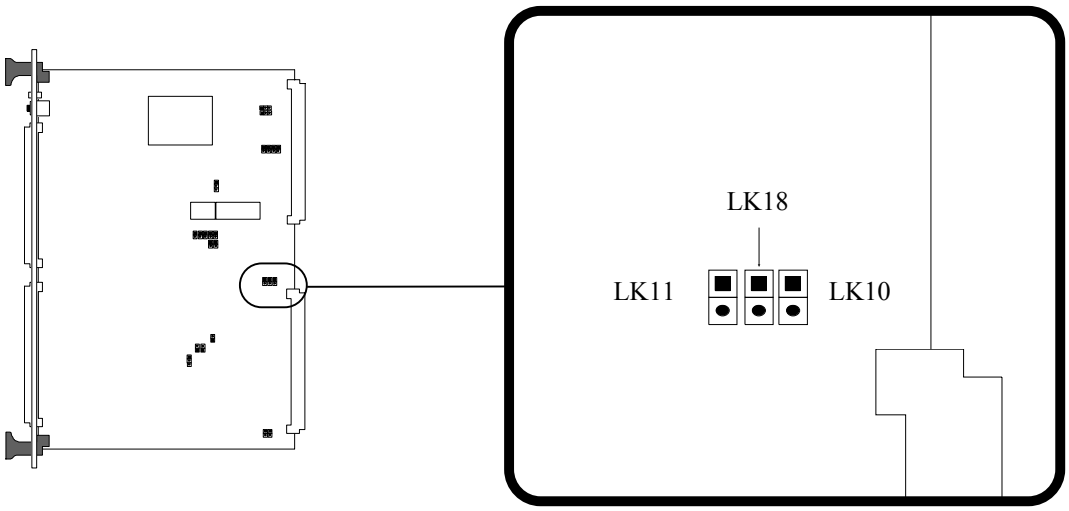
BRL0 and BRL1 (Links 16 and 17)

The following table shows how links 16 and 17 select the VMEbus request level:

BRL0 (LK16)	BRL1 (LK17)	VMEbus Request Level
In	In	3 (highest priority) (default)
In	Out	2
Out	In	1
Out	Out	0 (lowest priority)

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SELSL24 (LK18)



If the SELSL24 jumper is not fitted, then the slave responds to A32 and A24 accesses (the default). If the jumper is fitted, then the slave accesses are at A32 only.

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SELA3 to SELA6 (Links 19 to 22)

Reset Vector Jumper Settings

SELA6 (LK19)	SELA5 (LK20)	SELA4 (LK21)	SELA3 (LK22)	EPROM Reset Vector
In	In	In	In	0 (default POP 6)
In	In	In	Out	1
In	In	Out	In	2
In	In	Out	Out	3
In	Out	In	In	4
In	Out	In	Out	5
In	Out	Out	In	6
In	Out	Out	Out	7
Out	In	In	In	8
Out	In	In	Out	9 (default POPs 4 and 5)
Out	In	Out	In	10
Out	In	Out	Out	11
Out	Out	In	In	12
Out	Out	In	Out	13
Out	Out	Out	In	14
Out	Out	Out	Out	15

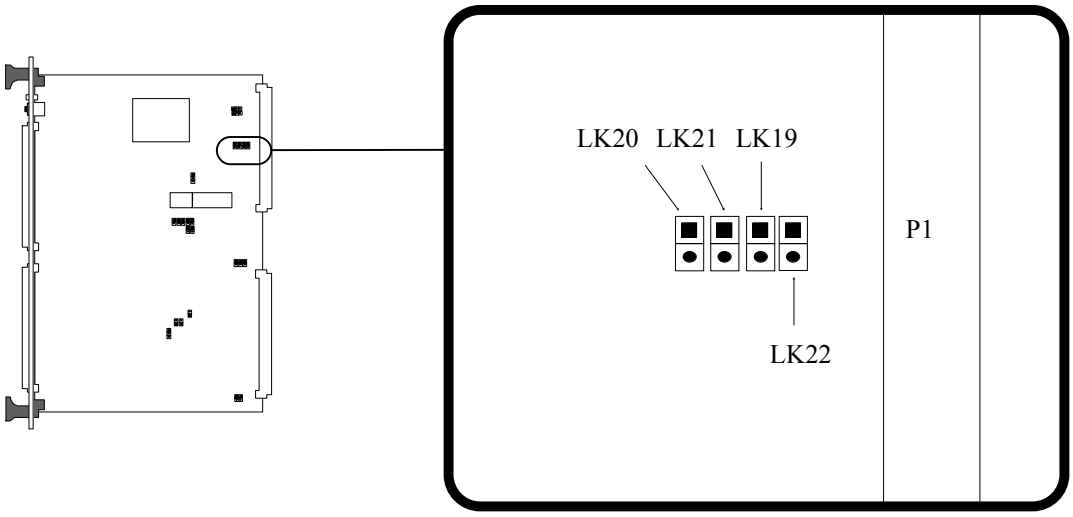
Reset Vectors 8 and 9

Vector 8 checks whether the warm start flag is set. If not (i.e. cold start), vector 8 runs the self-tests, initialises RT/M and then calls the loader. If the warm start flag is set, vector 8 just initialises RT/M and calls the loader (i.e. it doesn't run the self-tests).

Vector 9 checks whether the warm start flag is set. If not (i.e. cold start), vector 9 runs the self-tests, initialises RT/M and then sets up an auto-vector level 7 handler. Vector 9 then clears SYSFAIL and calls the loader.

If the warm start flag is set, the sequence is similar except that the self-tests do not run, i.e. the RT/M is initialised, an auto-vector level 7 handler is set up, SYSFAIL is cleared and the loader is called.

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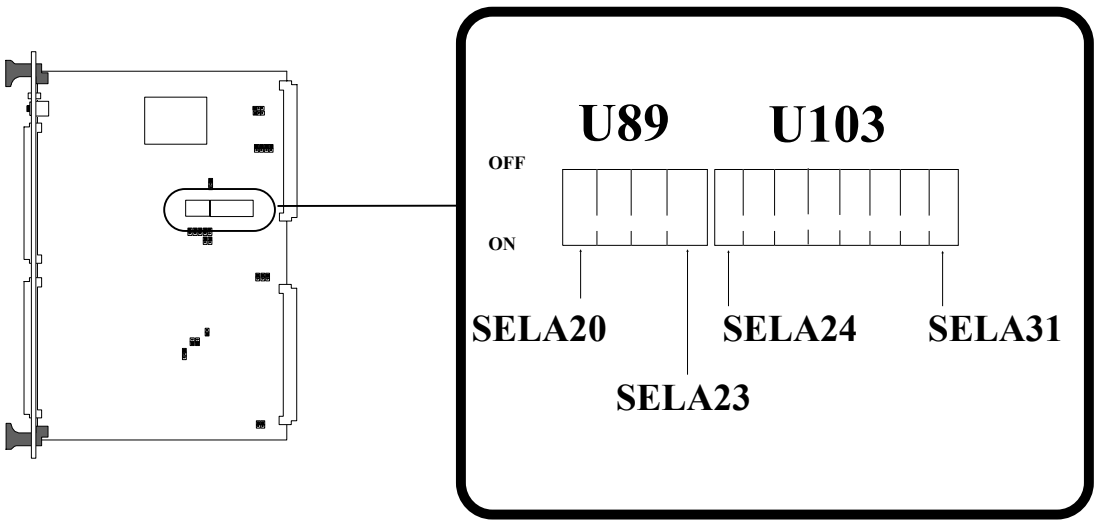


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DIL Switches

There are two DIL switches on the card. U103 is 8-way and U89 is 4-way. The following table shows the DIL settings. If the switch is off, the signal is one. If the switch is on, the signal is zero. The twelve switches selected give a 12-bit address used as bits 31 to 20 of the start address of the VME slave RAM window.

DIL	Signal	Switch Number
8-Way	SELA31	SW1 (**m.s.b.**)
	SELA30	SW2
	SELA29	SW3
	SELA28	SW4
	SELA27	SW5
	SELA26	SW6
	SELA25	SW7
	SELA24	SW8
4-Way	SELA23	SW1
	SELA22	SW2
	SELA21	SW3
	SELA20	SW4 (**l.s.b.**)



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Chapter 5 - Applications Firmware

Introduction

This chapter describes the standard interface to the on-board applications firmware of the SIO-4. This manual calls the SIO-4 applications firmware 'SIOP firmware', standing for **S**erial **I**nput **O**utput **P**rocessor.

The SIOP firmware is implemented under VRTX32. This gives the basic facilities required by the SIOP firmware, such as interrupt handling, memory management, task creation, task scheduling and basic task management facilities. The SIOP firmware provides intelligent front end processing and intelligent post processing for both UNIX and non-UNIX (e.g. OS-9) based systems.

All addresses stated in this chapter assume that the SIO-4 has its local RAM at address 0x00000000. If you use a Base Address other than 0x00000000, then add this to the addresses in this chapter to get the true address for your configuration.

SIOP Firmware

Overview

The SIO-4 provides an interface for up to sixteen asynchronous RS-232C serial lines with a host computer via the VMEbus.

The SIOP firmware provides intelligent processing of serial input/output data. If the host computer is running a UNIX-type operating system (e.g. Motorola System V/68 Release 3), the SIOP firmware can be configured to carry out all the input/output processing as defined by the AT&T System V Interface Definition (SVID) Issue 2 **TERMIO(BA_ENV)** entry. The processing also conforms to the X/OPEN Portability Guides (January 1987) Volume 2 entry **TERMIO(7).** However, for non-UNIX hosts, this processing can be selectively disabled or replaced, by loading new applications firmware into the SIO-4. The firmware can handle different line disciplines in parallel.

In normal operation, the SIO-4 copies the SIOP applications firmware from its on-board PROM into its local RAM before executing the firmware. However, when initializing the card, you can load new applications firmware onto the card over the VMEbus (see the Loading Sequences and Firmware Initialization Sequence sections for details). This facility allows for simple firmware updates and the inclusion of user written code.

You should incorporate the firmware initialization sequence into the host system boot sequence.

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SIO-4 Specifics

In the SIO-4, the following tasks run on the executive:

init Used to begin operations.

server( ) The *server( )* task is analogous to a UNIX daemon-type process, such as the error logging daemon. The *server( )* task wakes up a channel process if it has a command to process, data to read in or data to output. *server( )* also generates a host interrupt on command completion. The task runs 25 times every second, so a single interrupt may be the result of more than one command completing. On an interrupt, the host must therefore inspect all channels.

chanpXX The channel processes range from chanp00( ) to chanp15( ), having one channel process per input/output channel. The channel process is responsible for command execution and data input/output processing. It sleeps if there is no processing to carry out. *server( )* only wakes it when there is some processing to carry out or a command to execute.

SIOP Command Interface

Overview

The SIOP firmware responds to commands issued by a host or any other processor in the system that has VMEbus master capabilities. The host processor directly accesses the data structures that control the execution of the SIOP firmware. There is one control structure per input/output channel, making sixteen data structures located in the shared memory of the SIO-4.

Once a host has set up a command in the shared memory of the SIO-4, there is a latency of up to 1/25th of a second before command execution begins. The reason for this latency is twofold. First; the firmware task *server( )* that controls the sixteen channel processes, chanpXX, only runs once every 40 milliseconds. Second; the channel processes go into a sleep state when there is no processing or command to carry out.

Basic Firmware Structures

The formal C language declarations of these structures are in the SIOP Data Structures section at the end of this chapter:

fifo Stores all input/output data.

duart_channel Holds all control and status information relating to each channel.

term_control Communicates new control options to a channel.

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Command Format

An SIO-4 command has three parts:

- The actual command (for example, open, close)
- Any associated arguments
- The command modifier

The C structure *ics* (interface command structure) stores these elements of the SIO-4 command. *ics* is a sub-structure of the per-channel control structure *duart_channel*. The C declaration of the *duart_channel* structure is in the DUART Channel Control Structure section. To build a command, the address of this shared data structure must be found.

The address resolution normally takes place on card initialization. The host normally stores the address (relative to the host processor) of each of the sixteen *duart_channel* structures locally in an address look-up table. The host stores the resolved address so that it can calculate the address of any shared data structure element on each access.

The sequence for issuing an application's firmware command to the SIO-4 follows:

1) Acquire the flag *dc_cmd_lock* using an indivisible instruction such as the Motorola 680XX series TAS instruction. If the host processor does not have a Motorola 680XX series processor, then use an instruction with the same function. This requires the host to generate the correct signals for a Read-Modify-Write (RMW) cycle. If the host cannot acquire the flag, it must not alter any values in the *ics* structure.

2) Assuming that the task or code thread that executed the TAS instruction now exclusively owns the *ics* structure, no other task or code thread can alter the contents of the *ics* structure until the *dc_cmd_lock* flag is released. At this point, the host verifies that the *dc_cmd* field is 0x00. If not, then there is a possible synchronization fault or firmware fault. This fault can occur if the TAS instruction has not executed as an indivisible instruction.

3) Load any arguments (*dc_arg1* to *dc_arg4*) required by this command.

4) Load any required command modifier *(dc_modifier)*. A command modifier specifies any action that the firmware should carry out on the input and output data streams before executing the actual command. For example, discard all input not yet read by the host. See the Command Modifiers section for a more detailed description.

5) Select the mode for executing the command. There are two possible modes: *interrupt mode* and *poll mode*. Loading the **HOSTCMDWAIT** field of *dc_flags* with a non-zero value, usually 1, selects *interrupt mode*. Do this before setting *dc_cmd*. When this field is set, the SIO-4 generates an interrupt after command completion. The interrupt level and vector definition are part of the card initialization sequence.

   If the **HOSTCMDWAIT** flag is clear, the mode defaults to *poll mode*. In *poll mode*, the host polls (either periodically or continuously) for the command field to clear.

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The **Command Modifiers** section on page 50 of issue 6 is no longer completely up-to-date. A new command modifier to negate RTS has been added. The text up to the table showing the definition for the command word modifier *dc_modifier* remains the same. From there on, the text should now read (with the additions highlighted):

Flag Name	Bit	C #define	Meaning
MOD_OFLUSH	0	0x0001	Flush output buffers
MOD_IFLUSH	1	0x0002	Flush input buffers
MOD_ODRAIN	2	0x0004	Allow output to drain
MOD_RTSNEG	**4**	**0x0010**	**Negate RTS**

For example, to specify a command to flush all buffers before executing, set bits 0 and 1 of *dc_modifier*. Set bits 1 and 2 to drain output and flush input.

The modifier MOD_RTSNEG can be used to negate the RTS and can only be specified on an open or close command. For example, MOD_RTSNEG can be used to set bit 4 of *dc_modifier* so that RTS is negated when a channel is closed. Setting bit 4 of *dc_modifier* for negation of RTS when opening a channel means that RTS will not be asserted at all.

Successful completion of each operation defined by the command modifier *mask* in *dc_modifier* clears the appropriate bit from the mask. The firmware processes the command modifier mask in the following order:

- Drain output
- Flush output
- Flush input
- **Negate RTS**

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6) Having selected the mode, load the command value in *dc_cmd*. Command execution begins up to 1/25th of a second after setting the command field. The host must ensure that if it is going to *sleep( )* while waiting for an interrupt, then the task calls *sleep( )* before servicing the interrupt. This is normally done by increasing the processor priority, while in the critical section of the code, to block the service of an SIO-4 interrupt.

7) Wait for command completion. If **HOSTCMDWAIT** is set, then an interrupt signals completion. Otherwise, the host must poll and wait for the *dc_cmd* field to return to zero.

8) When the command has completed, read the command error word *dc_cmd_err* before releasing the command lock flag *dc_cmd_lock*. Action on error is host specific. The lock flag can be cleared by a CLR instruction on Motorola 680XX series based systems.

   If **HOSTCMDWAIT** is set, then **FWCMDDONE** is set true before interrupt generation. Clear **FWCMDDONE** then **HOSTCMDWAIT** before releasing *dc_cmd_lock*.

Command Modifiers

You can specify a command modifier with any command** that the SIO-4 is to process. A command modifier allows the input and output data streams to be in a defined state before the execution of the command. This means that you can specify that the command will not execute until one (or both) of the following conditions has been met:

- The SIO-4 transmits data waiting for output, i.e. the command waits for the channel output buffer to drain
- The SIO-4 discards data in either the input or output streams (or both); i.e. the command waits until the SIO-4 flushes the channel input or output buffers

** **Any command modifier specified with the SIOSYNC command is ignored. This is an exception to the rules for command modifiers.**

The following table shows the definition for the command modifier word *dc_modifier*:

Flag Name	Bit	C # define	Meaning
MOD_OFLUSH	0	0x0001	Flush output buffers
MOD_IFLUSH	1	0x0002	Flush input buffers
MOD_ODRAIN	2	0x0004	Allow output to drain

For example, to specify a command to flush all buffers before executing, set bits 0 and 1 of *dc_modifier*. Set bits 1 and 2 to drain output and flush input.

Successful completion of each operation defined by the command modifier *mask* in *dc_modifier* clears the appropriate bit from the mask. The firmware processes the command modifier mask in the following order:

- Drain output
- Flush output
- Flush input

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Drain Timeouts

The firmware cannot transmit data if, for example, a hardware control scheme is in use (RTS/CTS) and the remote receiver stops the local transmitter transmitting. If the firmware cannot transmit, the buffers will not drain with a drain output request selected by **MOD_ODRAIN**, and the request will not complete. Usually, this is desirable. However, if the drain request is part of an ordered shutdown sequence of the system, the SIO-4 needs to close its channels regardless of the state of a remote system. To overcome this, you can specify a timeout on all drain requests selected by **MOD_ODRAIN**.

The elements *dc_draintout* and *dc_def_draintout*, in the *duart_channel* structure, control the length of drain timeouts.

1) If *dc_draintout* is non-zero, then its value, in 1/100^{ths} of a second, forms a timeout for the drain request. If the drain does not complete within this timeout period, the buffers are flushed instead.

2) If *dc_draintout* is zero, *dc_def_draintout* (the default drain timeout in 1/100^{ths} of a second) forms a back-up timeout. If this is non-zero and the drain does not complete within this timeout period, the buffers are flushed instead.

3) If *dc_def_draintout* is also zero, there is no timeout of the drain request. To abort the request, the host uses the **SIOSYNC** command to resynchronize all firmware internal status flags. Once used, the firmware clears *dc_draintout*. It is therefore a per-command timeout.

Applications Firmware Commands

The standard applications firmware supplied in PROM ensures that the card never needs to be a VMEbus master. Using this standard firmware, the card never initiates a VMEbus cycle.

When using the SIO-4 as a VMEbus slave, a VMEbus master must provide all data required by the card. So, any request requiring information from the card must be done by a VMEbus master reading the information directly from the card.

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A complete set of commands supported by the standard SIOP applications firmware follows:

Command	Code	Meaning
SIOOPEN	0x0001	Initialize and open a specified channel. Load the required parameters into the terminal control block for that channel. The Input Data Path and Output Data Path sections define the interaction with serial line control signals. All command modifiers are available for use by this command. If bit 0 of *dc_arg4* is set, then wait for DSR, otherwise this is an error. If bit 1 is set, wait for DCD, otherwise continue with the open sequence. *dc_arg1* to *3* must be 0
SIOCLOSE	0x0002	Close the specified channel and restore default parameters to the channel's terminal control block. The Input Data Path and Output Data Path sections define the interaction with serial line control signals. All command modifiers are available for use by this command. If *dc_arg1* is non-zero, the speed changes to 300 baud before closing the channel, to minimise the DUART polling rate
SIOSET	0x0003	Sets the parameters associated with a particular channel. Load the required parameters into the terminal control block for the channel on which the command is to be executed. All command modifiers are available for use by this command
SIOSUSP	0x0004	Suspend a channel from all processing (this can include raw input) while altering firmware data structures (e.g. the echo table). All command modifiers are available for use by this command
SIOREACT	0x0005	Restart a channel process after an SIOSUSP command. All command modifiers are available for use by this command
SIODUMMY	0x0006	This command allows the action specified by the command modifier to be executed. The host processor can use this command to carry out functions such as *wait until output drained* or *flush input and output data streams*. All command modifiers are available for use by this command
SIOBRK	0x0007	Wait for the output to drain. If *dc_arg1* for this channel is 0, send a break (a stream of zero bits sent for 0.25 seconds). All command modifiers are available for use by this command

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Command	Code	Meaning
SIOSYNC	0xFFFF	Resynchronize the firmware flags and states with the host. Use this command after the host has aborted any of the above commands, i.e. the host task stops without waiting for the command to complete. No command modifiers are available for use with this command. The command clears and ignores any modifiers set. **Note:** Do not use interrupt mode with this command, i.e. do not set HOSTCMDWAIT. If it is set, it will be cleared, unless the host is truly waiting for an interrupt response from the command. In this case the host will wait indefinitely. *dc_arg1* contains the command that has aborted. Offset 27 (**SYNCHAND**) of *dc_flags[ ]* is set true when the **SIOSYNC** command completes and *dc_cmd* clears. If the command field becomes zero when **SYNCHAND** is still false, then the **SIOSYNC** command must be reissued

Command Errors

An interrupt or the clearing of the command field, *dc_cmd*, shows command completion. If the command has failed, then the command error word, *dc_cmd_err*, contains one of the following error codes:

Code	Value	Meaning
ECHAN_NOT_OPEN	0x0001	Attempted to execute an SIOCLOSE command on a channel that was not open
ECHAN_NOT_SUSP	0x0002	Attempted to execute an SIOREACT command on a channel that was not in a suspend state due to a previous SIOSUSP command
ECHAN_OPEN	0x0003	Attempted to execute an SIOOPEN command on a channel that was already open
ECHAN_SUSP	0x0004	Attempted to execute an SIOOPEN command on a channel suspended due to an SIOSUSP command
ENOICANON	0x0005	Attempted to select ICANON input mode via *dc_lflag* field on a channel that had an unreleased facility
ESPEED	0x0006	Attempted to select a speed that was invalid or not available
ENODSR	0x0007	No DSR signal on SIOOPEN
ENOT_IMP	0xFFFF	Attempted to use an unreleased facility

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Input Modes

The *dc_iflag* field of the *duart_channel* structure describes the input characteristics of each channel (i.e. the way in which the SIO-4 treats character input). The following table summarises the characteristics:

Flag Name	Bit	C # define	Meaning
IGNBRK	0	0x00000001	Ignore break condition
BRKINT	1	0x00000002	Signal interrupt on break
IGNPAR	2	0x00000004	Ignore characters with parity errors
PARMRK	3	0x00000008	Mark parity errors
INPCK	4	0x00000010	Enable input parity check
ISTRIP	5	0x00000020	Strip character
INLCR	6	0x00000040	Map NL to CR on input
IGNCR	7	0x00000080	Ignore CR
ICRNL	8	0x00000100	Map CR to NL on input
IUCLC	9	0x00000200	Map upper case to lower case on input
IXON	10	0x00000400	Enable start/stop output control
IXANY	11	0x00000800	Enable any character to restart output
IXOFF	12	0x00001000	Enable start/stop input control
IMAX	16	0x00010000	Do not discard data on input FIFO overflow
IMAXBEL	17	0x00020000	If IMAX is set, output BEL character
IECHOTBL	18	0x00040000	If set, use echo table

If **IGNBRK** is set, the break condition is ignored, i.e. it is not put on the input queue and not read by any process. The break condition is a character framing error where data is all zeros.

If **BRKINT** is set, the break condition generates an interrupt signal and flushes both the input and output FIFOS.

If **IGNPAR** is set, characters with framing and parity errors other than break are ignored. If **PARMRK** is set, then a character with a framing or parity error that is not ignored is read as the three character sequence:

0377 , 0 , X ,

where **X** is the data of the character received in error. To avoid ambiguity here, if **ISTRIP** is clear, a valid character of 0377 is read as 0377, 0377. If **PARMRK** is clear, a framing or parity error that is not ignored is read as the character NUL (0x00).

Setting **INPCK** enables input parity checking. Clearing **INPCK** disables input parity checking. This allows output parity generation without input parity errors.

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If **ISTRIP** is set, valid input characters are first stripped to 7 bits. Otherwise, all 8 bits are processed.

Setting **INLCR** translates a received NL character into a CR character. If **IGNCR** is set, a received CR character is ignored (not read). Otherwise, setting **ICRNL** translates a received CR character into an NL character.

Setting **IUCLC** translates a received upper case alphabetic character into the corresponding lower case character.

Setting **IXON** enables start/stop output control. A received STOP character suspends output and a received START character restarts output. All start/stop characters are ignored and not read. If **IXANY** is set, any input character restarts suspended output.

If **IXOFF** is set, the system transmits start/stop characters when the input queue is nearly empty/full.

If **IMAX** is set and the input FIFO overflows, further input is not stored but input already present in the input FIFO is not discarded. Clearing **IMAX** discards all input present in the input FIFO if the FIFO overflows. To re-enable input, issue an **SIOREACT** command.

If **IMAXBEL** is also set, the ASCII BEL character is output if the input FIFO overflows. If **IMAXBEL** is clear, no BEL character is output on FIFO overflow. **IMAXBEL** set on its own is ignored until IMAX is also set.

The power-up default value is all bits clear.

Water Marks

The high and low water marks are a function of the baud rate, but the host may also set them to non-default values. It does this by direct alteration of the high and low water values in the relevant FIFO data structure.

Note: Do not change water marks when a data stream is active or has data in it. A flush or drain request with an SIOSUSP command is strongly recommended.

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Output Modes

The *dc_oflag* field of the *duart_channel* structure describes the output characteristics of each channel (i.e. the way in which the SIO-4 treats output). The following table summarises the characteristics:

Name	Bit(s)	C # define	Meaning
OPOST	0	0x00000001	Postprocess output
OLCUC	1	0x00000002	Map lower to upper case on output
ONLCR	2	0x00000004	Map NL to CR-NL on output
OCRNL	3	0x00000008	Map CR to NL on output
ONOCR	4	0x00000010	No CR output at column 0
ONLRET	5	0x00000020	NL carries out CR function
OFILL	6	0x00000040	Use fill characters for delay
OFDEL	7	0x00000080	Fill is DEL, otherwise it is NUL
NLDLY	8	0x00000100	Select new line delays
NL0		0x00000000	
NL1		0x00000100	
CRDLY	9 and 10		Select carriage return delays
CR0		0x00000000	
CR1		0x00000200	
CR2		0x00000400	
CR3		0x00000600	
TABDLY	11 and 12		Select horizontal tab delays
TAB0		0x00000000	
TAB1		0x00000800	
TAB2		0x00001000	
TAB3		0x00001C00	Expand tabs to spaces
BSDLY	13	0x00002000	Select backspace delays
BS0		0x00000000	
BS1		0x00002000	
VTDLY	14	0x00004000	Select vertical tab delays
VT0		0x00000000	
VT1		0x00004000	
FFDLY	15	0x00008000	Select form feed delays
FF0		0x00000000	
FF1		0x00008000	
OWRAP	16	0x00010000	Insert an NL at right margin

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Setting **OPOST** post-processes output characters, as the remaining flags dictate. Otherwise, characters are transmitted without change.

Setting **OLCUC** transmits a lower case alphabetic character as the corresponding upper case character. This function is often used with **IUCLC**.

Setting **ONLCR** transmits the NL character as the CR/NL character pair. Setting **OCRNL** transmits the CR character as the NL character. If **ONOCR** is set, no CR character is transmitted when at column 0 (first position). If **ONLRET** is set, the NL character is assumed to do the carriage return function. The column pointer is set to 0 and the delays specified for CR are used. Otherwise, the NL character is assumed to do just the line feed function; the column pointer remains unchanged. The column pointer is only reset to 0 if the CR character is also transmitted.

The delay bits specify how long transmission stops to allow for mechanical or other movement when sending certain characters to the terminal. In all cases, a value of 0 shows no delay. Setting **OFILL** transmits fill characters for delay instead of a timed delay. This is useful for high baud rate terminals that only need a small delay. If **OFDEL** is set, the fill character is DEL, otherwise it is NUL.

If a form feed or vertical tab delay is specified, it lasts for about two seconds. New line delay lasts about 0.10 seconds. Setting **ONLRET** uses the carriage return delays instead of the new line delays. Setting **OFILL** transmits two fill characters.

Carriage return delay type 1 is about 0.05 seconds, type 2 is about 0.10 seconds and type 3 is about 0.15 seconds. If **OFILL** is set, delay type 1 transmits two fill characters and type 2 transmits four fill characters.

Horizontal tab delay type 1 depends on the current column position. Type 2 is about 0.10 seconds. Type 3 specifies that tabs are to be expanded into spaces. Setting **OFILL** transmits two fill characters for any delay.

Backspace delay lasts about 0.05 seconds. Setting **OFILL** transmits one fill character. The actual delays may vary slightly depending on system load.

Setting **OWRAP** sends a 4CR" when at the right hand margin, as defined in *dc_width*.

The power-up default value is all bits clear.

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Hardware Control Flags

The *dc_cflag* field of the *duart_channel* structure describes the hardware control of the terminal, as the following table shows:

Flag Name	Bit(s)	C # define	Meaning
CBAUD	0 to 3		Baud rate
B0		0x00000000	Hang up
B50		0x00000001	50 baud
B75		0x00000002	75 baud
B110		0x00000003	110 baud
B134		0x00000004	134.5 baud
B150		0x00000005	150 baud
B200		0x00000006	200 baud
B300		0x00000007	300 baud
B600		0x00000008	600 baud
B1200		0x00000009	1,200 baud
B1800		0x0000000A	1,800 baud
B2400		0x0000000B	2,400 baud
B4800		0x0000000C	4,800 baud
B9600		0x0000000D	9,600 baud
B19200		0x0000000E	19,200 baud
B38400		0x0000000F	38,400 baud
CSIZE	4 and 5		Character size
CS5		0x00000000	5 bits
CS6		0x00000010	6 bits
CS7		0x00000020	7 bits
CS8		0x00000030	8 bits
CSTOPB	6	0x00000040	Select two stop bits
CREAD	7	0x00000080	Enable receiver
PARENB	8	0x00000100	Parity enable
PARODD	9	0x00000200	Select odd parity
HUPCL	10	0x00000400	Hang up on last close

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Flag Name	Bit(s)	C # define	Meaning
CLOCAL	11	0x00000800	Local line if set, Dial up line if not
RCBAUD	16 to 19	0x000F0000	Baud rate, bit patterns follow:
RB0		0x00000000	No split speed operation
RB50		0x00010000	50 baud (receive)
RB75		0x00020000	75 baud
RB110		0x00030000	110 baud
RB134		0x00040000	134.5 baud
RB150		0x00050000	150 baud
RB200		0x00060000	200 baud
RB300		0x00070000	300 baud
RB600		0x00080000	600 baud
RB1200		0x00090000	1,200 baud
RB1800		0x000A0000	1,800 baud
RB2400		0x000B0000	2,400 baud
RB4800		0x000C0000	4,800 baud
RB9600		0x000D0000	9,600 baud
RB19200		0x000E0000	19,200 baud
RB38400		0x000F0000	38,400 baud
CLLOOP	20	0x00100000	Local loopback mode

The **CBAUD** bits specify the baud rate. The zero baud rate, **B0**, hangs up the connection. If **B0** is specified, the data-terminal-ready signal is not asserted. Normally, this disconnects the line. For any particular hardware, impossible speed changes are ignored.

See Table 7 for possible baud selection for a given state.

The **CSIZE** bits specify the character size in bits for both transmission and reception. This size does not include the parity bit, if any.

If **CSTOPB** is set, two stop bits are used, otherwise only one stop bit is used. For example, 110 baud requires two stops bits.

Setting **PARENB** enables parity generation and detection and adds a parity bit to each character. If parity is enabled, setting **PARODD** specifies odd parity, otherwise even parity is used.

Setting **CREAD** enables the receiver. Otherwise, no characters are received.

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Setting **HUPCL** disconnects the line when the last process with the line open either terminates or closes it, i.e. the data-terminal-ready signal is not asserted.

If **CLOCAL** is set, the line is assumed to be a local, direct connection with no modem control. Otherwise, modem control is assumed.

The power-up default value after open is B9600, CS8, CREAD, CLOCAL.

If the split speed feature is in operation, then bits 16 to 19 describe the receive speed.

DUART Type 68681

The SIO-4 uses type 68681 DUARTs. These devices can support split speed operation in the range 50 to 38,400 baud. Select the required baud rate by setting the appropriate bit pattern in a DUART control register. Two tables of baud rates are available and not all the baud rates supported by the device are simultaneously available.

Table 7. DUART Baud Rates

Table 0	Table 1
50	75
110	110
134.5	134.5
200	150
300	300
600	600
1,200	1,200
1,050	2,000
2,400	2,400
4,800	4,800
7,200	7,800
9,600	9,600
38,400	19,200

The bit pattern forms an index into the currently selected table to select the baud rate. In certain circumstances however, a particular baud rate selection request may not be available to a user. One solution would be to change the currently selected baud rate table as required. There is one baud rate table for each DUART. Each table therefore controls two RS-232C channels. A change in the current baud rate table can only take place if both tables support the DUART's current baud rate.

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Below are some examples of the scheme implemented by the firmware. The two DUART channels are called A and B.

Example 1

Request: Channel A is set to 50 baud, so selecting table 0. Channel B requests 75 baud.

Result: Channel B would not be allowed to select 75 baud because table 0 does not support this rate. A change to table 1 could not be allowed, as table 1 does not support 50 baud, which is in use by channel A.

Example 2

Request: Channel A is set to 300 baud and table 0 is currently selected. Channel B requests 150 baud.

Result: 150 baud is supported by table 1. A change to the currently selected baud rate table is therefore required. In this case, the change is permissible as table 1 supports the baud rate currently used by the channel A, i.e. 300 baud. This results in a change to the current baud rate table.

Note: Baud rates of 1050, 2000 and 7200 are not available as there are no bit patterns in the *dc_cflag* field reserved to select these speeds.

Line Discipline Modes

Firmware line discipline uses the *dc_lflag field* to control terminal functions. The following table shows the basic line discipline.

Name	Bit	C# define	Meaning
ISIG	0	0x00000001	Enable signals
ICANON	1	0x00000002	Canonical input (erase and kill processing)
XCASE	2	0x00000004	Canonical upper/lower presentation
ECHO	3	0x00000008	Enable echo
ECHOE	4	0x00000010	Echo erase character as BS-SP-BS
ECHOK	5	0x00000020	Echo NL after kill character
ECHONL	6	0x00000040	Echo NL
NOFLSH	7	0x00000080	Disable flush after interrupt or quit
IFTORAW	18	0x00040000	Always flush input on change to raw mode
IFTOCAN	19	0x00080000	Always flush input on change to canonical mode

Setting **ISIG** checks each input character against the special control characters INTR and QUIT. If an input character matches one of these control characters, the function associated with that character is carried out. If **ISIG** is clear, no checking is done. These special input functions are therefore possible only if ISIG is set. These functions may be disabled individually by changing the value of the control character to an unlikely or impossible value (e.g. 0377).

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Receipt of a special control character sets the dc_flags HOSTINZAP and HOSTFLUSH to show that host action is required. The host may flush the FIFOs if required. Until these flags are cleared, the channel will not receive or transmit any characters, although it does continue processing commands from the host. Closing the port with the SIOCLOSE command does NOT clear these flags.

Setting **ICANON** enables canonical processing. This enables the erase and kill edit functions, and the assembly of input characters into lines delimited by NL, EOF and EOL. If **ICANON** is clear, read requests are satisfied directly from the input queue. **A read is not satisfied until at least MIN characters have been received or the timeout value, TIME, has expired.** This allows fast bursts of input to be read efficiently while still allowing single character input.

The **MIN** and **TIME** values are stored in the position for the EOF and EOL characters respectively. The time value represents tenths of seconds.

If **XCASE** and **ICANON** are set, an upper case letter is accepted on input by preceding it with a **character**, and is output preceded by a **character**. In this mode, the following table shows the escape sequences that are generated on output and accepted on input:

For:	Use:
‘	\ ‘
|	\ !
~	\ ~
{	\ (
}	\ )
\	\ \

For example, A is input as \ a; \ n as \ \ n; and \ N as \ \ \ n.

Setting **ECHO** echoes the characters as they are received. When **ICANON** is set, the following echo functions are possible:

Setting **ECHO** and **ECHOE** echoes the erase character as ASCII BS-SP-BS, which clears the last character from a CRT screen.

Setting **ECHOE** and clearing **ECHO** echoes the erase character as ASCII SP-BS.

Setting **ECHOK** echoes the NL character after the kill character, to emphasize that the line will be deleted.

Note: An escape character preceding the erase or kill character removes any special function.

Setting **ECHONL** echoes the NL character, even if **ECHO** is clear. This is useful for terminals set to local echo (so called “half duplex”). The EOF character is not echoed, unless it is escaped. Terminals that respond to EOT are prevented from hanging up, because EOT is the default EOF character.

Setting **NOFLSH** prevents the normal flush of the input and output queues associated with the quit and interrupt characters.

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Setting **IFTORAW** flushes all input buffers when going to raw input mode. Raw input mode is defined in this context as non-canonical mode. Clearing the **ICANON** bit and setting **IFTORAW** therefore forces a flush to take place.

Setting **IFTOCAN** flushes all input buffers when going to canonical input mode. Setting the **ICANON** and **IFTOCAN** bits therefore forces a flush to take place.

The power-up default value is all bits clear.

RS-232C Signals

The **CLOCAL** flag in *dc_cflag* controls the use of the following RS-232C control signals:

DSR (Data Set Ready)
DCD (Data Carrier Detect)
DTR (Data Terminal Read)
RTS (Request To Send)
CTS (Clear To Send)

If **CLOCAL** is set, a direct connection is assumed and the following rules apply:

1) RTS/CTS are enabled to provide a hardware handshake flow control scheme.

2) DTR is asserted when the channel is opened. DTR is only cleared on close if HIOPCL is set.

3) DCD/DSR is ignored

If **CLOCAL** is clear, a modem connection is assumed and the following rules apply:

1) RTS/CTS follow rule 1 above. If RTS/CTS cannot be provided, then wire the signals locally to provide a hard-wired input to the SIO-4 on CTS to signify always Clear To Send.

2) DTR follows rule 2 above. When using a modem, HUPCL is normally asserted so that DTR is cleared on the last close. When the modem finds DTR clear, it normally resets the phone line.

3) After detecting DCD, if it is lost for more than two seconds, then this is signalled to the host in the *dc_flags* field DCDLOST.

4) DSR is required for the SIOOPEN to complete.

Input Data Path

The character input data path within the standard applications firmware has three basic elements to it. They are:

- The DUART scanner
- Raw (non-canonical) data processing
- Canonical data processing

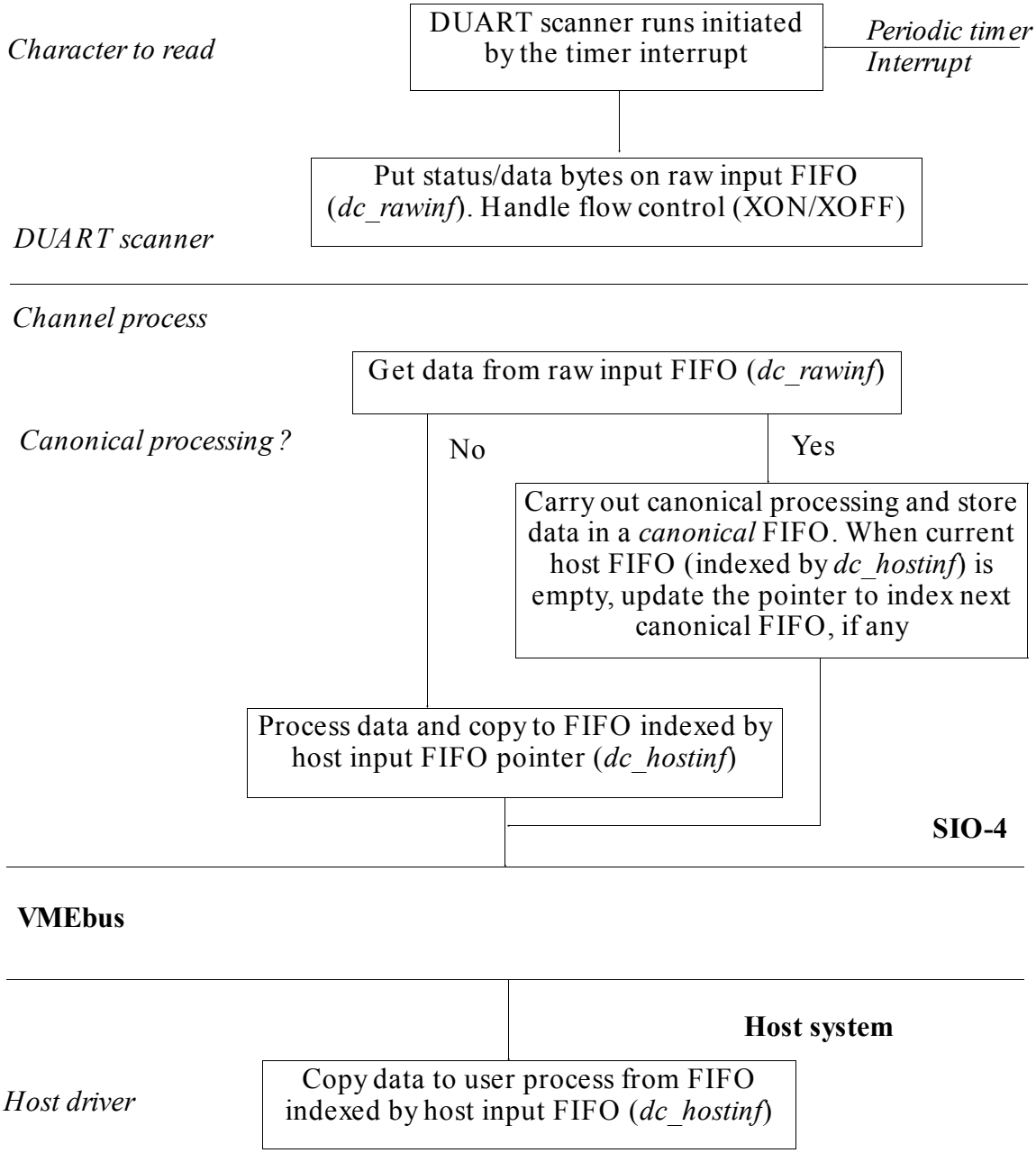
The SIO-4 Specifics section describes the scheduling of the channel process task that carries out this processing. The *chanpXX* task carries out both input and output data processing. Input and output cannot be scheduled separately.

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DUART Scanner

When the DUART scanner is running and a character is to be read, the DUART status and the associated character are loaded into the raw input word FIFO, *dc_rawinf*. The channel process reads the input data that is to be processed from this FIFO.

The following figure shows the process involved in the input data flow:



Non-Canonical Data Processing

In non-canonical mode the data path is linear. The firmware reads the status and associated character from the raw input FIFO, *dc_rawinf*. The firmware processes the status byte first to handle BREAK conditions, parity errors etc. If these conditions are present, the action taken depends on the current setting of the input mode control flags in *dc_iflag*.

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After processing the status byte, the firmware reads the associated input character. The firmware then processes the character as defined by the *dc_iflags*. It also carries out local echo as defined by the *dc_lflag* to minimize host loading.

Canonical Data Processing

In canonical mode, the data processing is linear, but there is also a cyclic array of canonical input FIFOs. This scheme eliminates the copying of canonically processed data from a temporary FIFO, where the input line is constructed, into the host input FIFO. Instead, the pointer to the current host input FIFO, *dc_hostinf*, is simply updated to point to the next complete line of input once the host system has fully read the current line. With this exception, the data path and status handling are the same as for the non-canonical data path.

Output Data Path

The character data path within the standard applications firmware has the following elements:

- The DUART scanner
- Output data processing

There is no dynamic FIFO buffer management on the output data stream. The SIO-4 Specifics section describes the scheduling of the channel process, chanpXX(0).

DUART Scanner

Figure 13 shows the use of the DUART scanner. It carries out the following basic functions on output:

- Send single character control data (e.g. XON, XOFF)
- Send data in priority output FIFO
- Send normal data from *dc_rawoutf* FIFO

Output Data Processing

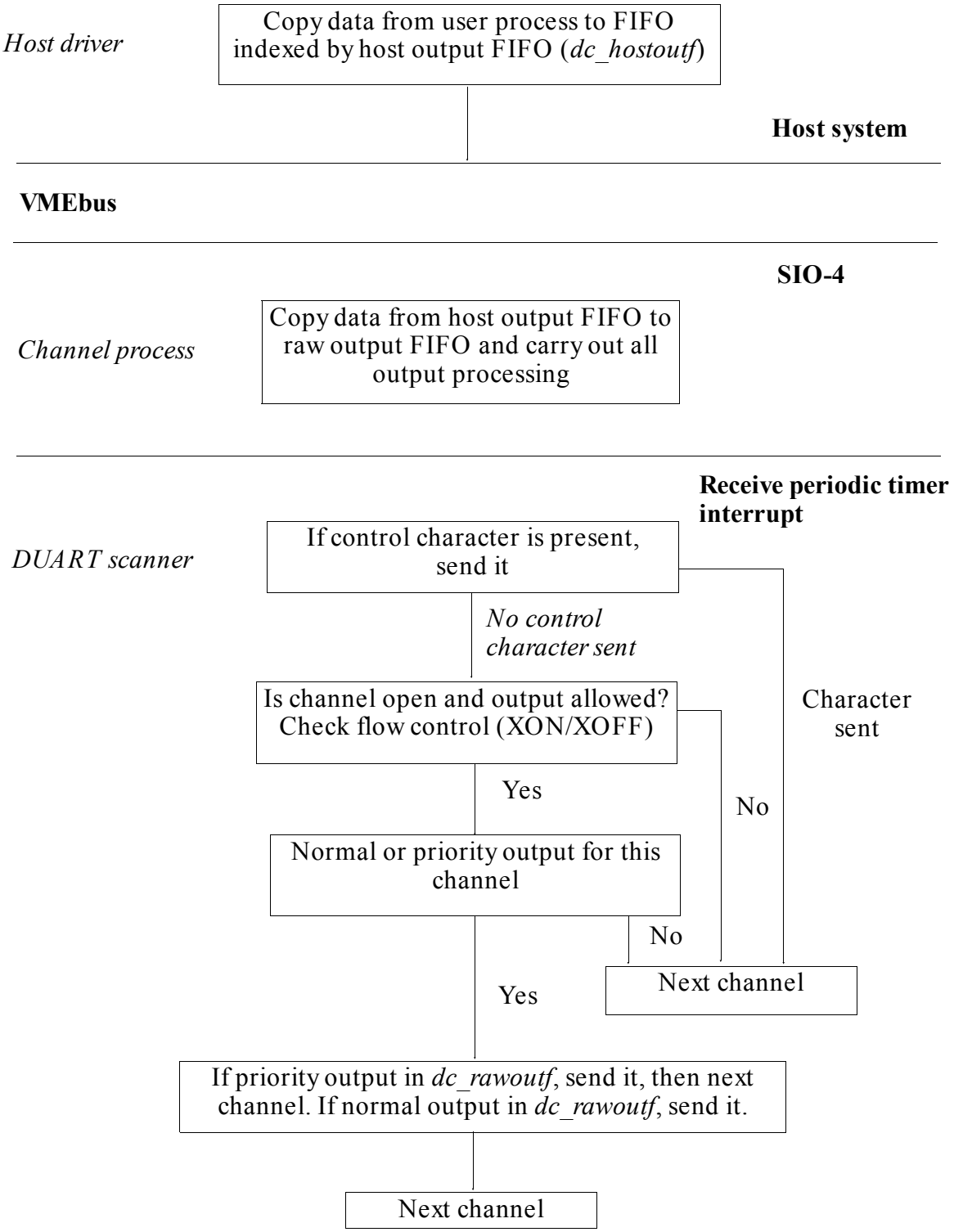
There are two FIFO based output data streams from the interface to the host. The normal stream uses *dc_hostoutf*. The channel process, chanpXX, defined by the *dc_oflag* field of the *duart_channel* structure, processes this stream. The output goes to the raw output FIFO *dc_rawoutf*. If an output delay is required, e.g. due to sending an NL character, then this causes a delay drain write, i.e. no more output is sent until the time delay specified has passed.

The other output data stream is from the FIFO *dc_rawpoutf*. This FIFO is directly available to the host. It may be used to send data, ahead of any data being processed, from the *dc_hostoutf* FIFO to the DUART scanner via the normal FIFO *dc_rawoutf*. Both these FIFOs are subject to flow control.

The firmware sends flow control characters via the single character output variable *dc_sendchar*.

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Figure 12. Output Data Flow



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Interrupts

The host receives an interrupt under the following conditions:

1) In modem operation (i.e. CLOCAL not set) if the DCD signal from the modem is lost for more than two seconds. The flag **HOSTDCDLOST** in *dc_flags* is set non-zero and must be cleared after servicing the interrupt.

2) If **ISIG** is set on receipt of a **QUIT, INTR** or **HOSTSWITCH** signal. The flag **FWSIGNAL** is set in *dc_flags* and must be cleared after servicing the interrupt. The *dc_signal* location reflects the cause of the interrupt.

3) If the input FIFO is empty and the host is waiting for input data, then it can set **HOSTIPWAIT**. An input character entering the host input FIFO sets **FWREADINTR** non-zero and generates an interrupt. **FWREADINTR** must be cleared after servicing the interrupt.

4) If the output FIFO is full and the host has data to send, then it can set **HOSTOPWAIT**. Space becoming available sets **FWWRITEINTR** and generates an interrupt. **FWWRITEINTR** must be cleared after servicing the interrupt.

5) When **HOSTCMDWAIT** is set and a command has completed.

Loading Sequences

Having completed self-test, the SIO-4 enters “loading mode”. It reflects this to the host by setting the bottom twelve bits of the card status word (situated at address 0x408) to 0x001 (HOST_LOAD_WAIT).

The SIO-4 waits for the host to load a valid base level command into address 0x480 (Loader Command Poll Address), which the SIO-4 constantly polls. Valid commands are:

LD_MLOADGO 0x62AE0003 Code to be loaded over VMEbus and executed.

LD_PLOADGO 0x62AE0005 Code to be loaded for EPROM and executed.

LD_PLOADGO requires a delay of 250mS before accessing the board.

LD_MLOADGO

When using this command, the host loads the code and data to the correct address on the SIO-4 via the VMEbus. This load operation should only start once the firmware has acknowledged the LD_MLOADGO command by setting the status to 0x002 (READY_LOAD).

After loading the code, the start address for the code is loaded to address 0x488. Location 0x484 is then changed to any non-zero value to begin execution of the code at the specified start address on the SIO-4.

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LD_PLOADGO

When using this command, there is no interaction between the host and the loader. The EPROM stores all load information as shown below:

+ 0x000 'Load from' address in EPROM

+ 0x004 'Load to' address in local RAM

+ 0x008 Code and data size in EPROM in bytes

+ 0x00C Start execution address in local RAM

+ 0x100 Normally the code and data would start here

Note: Addresses are relative to the base address of the EPROM plus 32 K. The EPROM load address is therefore 0xFFF08100.

Firmware Initialization Sequence

When the applications firmware starts to execute, the LED on the front of SIO-4 module turns green. The firmware then carries out a series of handshakes with the host to configure itself.

The firmware sets the status to 0x14 (HOST_MDEF) and the BF_CMD address at 0x2F10 to 0x62AE0002 (INITFMEM). The host reply should be loaded into BF_ARG1. If the host wishes to use the default firmware values, the reply should be F_DEFAULT (0x44464C54). If, however, the host needs to define all sixteen channels, the reply should be F_CONFIG (0x434E4647).

BF_ARG2 contains the amount of memory required to hold all the FIFOs. The memory requirement must be specified in clicks (512 bytes). To "release" the firmware, the host clears BF_CMD to zero. The F_CONFIG sequence is defined overleaf.

After completion of the FIFO and DUART initialization, the firmware requests the host to specify the interrupt level and vector.

The flow sets the status to 0x028 (HOST_IDEF) and a BF_CMD of INITINTR. The host responds via the *arg* fields as follows:

BF_ARG1 must be SINGLE_INTR(0x00000001)

BF_ARG2 Interrupt level

BF_ARG3 Vector number

BF_ARG4 must contain the required card access bits in bits 0 and 1. A code of 0x3 is any access and a code of 0x1 is supervisor and data (see Control Register FLGWRI in Chapter 3). Do not access the card for 12.5 microseconds after clearing BF_CMD.

The host clears BF_CMD to release the flow again.

The final test is a location monitor test of the SIO-4. The host must wait for a status of 0x040 (LM_TEST). On detecting this status, the host accesses the location monitor on the SIO-4 at offset address 0x400. The host should then wait for a status of LM_TEST_DONE (0x042). The result of the test is PASS (0x50414343) or FAIL (0x4641494C) in BF_CMD. The firmware waits for BF_CMD to clear.

When initialization is complete, the host waits for a status of 0x400 (SIO_READY) before resolving the *duart_channel* address.

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FIFO Defaults

Raw input FIFO	512 words
Raw output FIFO	512 bytes
Raw priority output FIFO	32 bytes
Host output FIFO	512 bytes
Non-canonical host input FIFO	1,024 bytes
Canonical input	Eight FIFOs of 256 bytes

F_CONFIG Sequence

After the F_CONFIG response, the firmware sets BF_ARG1 to 0xFF (the eight-bit negation of the channel number, the first being 0). The firmware also sets BF_CMD to INITFIFO and the status to 0x01C (HOST_FDEF).

When BF_ARG1 equals the 8-bit negation of the channel number, the host loads the FIFO size communications area at 0x2E00 with a fifo_sizes structure. The firmware waits until BF_ARG1 clears before reading this structure. The host must set BF_ARG2 before clearing BF_ARG1 to F_CONFIG. If, for a given channel, the defaults are to be used, then BF_ARG2 can be set to F_DEFAULT. In this case, the firmware initialises the fifo_sizes structure.

The first interaction with the host is to define the amount of memory that the firmware must allocate for its FIFO buffers.

A software reset command can be issued to the firmware at any time by loading the software reset command register (0x0000042C) with the software reset command (0x4B494C4C = ‘K’ ‘I’ ‘L’ ‘L’). The software should then delay for about half a second before re-initialising the board.

Duart_channel Address Resolution

Address 0x2F40 contains a pointer to an array of sixteen 32-bit values. These values are pointers to the sixteen DUART channel structures. The host resolves these addresses during its initialization sequence. The address at 0x2F40 is only valid when the status word exceeds 0x02C.

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SIOP Data Structures

This section describes the following SIOP firmware data structures.

fifo	FIFO data structure used by the host driver and firmware as data buffers.
duart_channel	Used for control of each process. It contains *ics* as a sub-structure.
term_control	Used to define I/O characteristics for the I/O processes.
input_fifo_control	Holds FIFO addressing and control information for input FIFOs.

All the structure definitions are in C declarations.

SIOP FIFO Structure

```
struct      fifo {
   unsigned short       f_tasok;          /* 0 Internal use only */
   unsigned char        ff_rdlock;        /* 2 FIFO read TAS byte */
   unsigned char        f_remrdflg;       /* 3 Internal use only */
   unsigned char        ff_wrlock;        /* 4 FIFO write TAS byte */
   unsigned char        f_remwrflg;       /* 5 Internal use only */
   short                f_size;           /* 6 Maximum number of elements */
   short                f_rdindex;        /* 8 Read index */
   short                f_wrindex;        /* 10 Write index */
   unsigned long        f_rdlcnt;         /* 12 Count of read TAS fails */
   unsigned long        f_wrlcnt;         /* 16 Count of write TAS fails */
   short                f_lowmark;        /* 20 Low water mark */
   short                f_highmark;       /* 22 High water mark */
   short                f_semaphore;      /* 24 Internal use only */
   char                 f_data[2];        /* 26 FIFO data area
                                             (actual size varies) */
};
```

The fields *ff_rdlock* and *ff_wrlock* are used exclusively to lock the FIFO. To ensure that no corruption of the FIFO occurs during some data manipulations, the hardware must support a test and set (TAS) instruction (read-modify-write cycle). The two pointers index into the FIFO.

SIOP *fifo_sizes* Structure

The *fifo_sizes* structure is used if the host issues an F_CONFIG command at FIFO initialization time.

```
struct      fifo_sizes {
   short    fs_rawin, fs_rawout, fs_rawpout;    /* 0, 2, 4 */
   short    fs_hostout, fs_hostnoncin;          /* 6, 8 */
   short    fs_ifc_no;                          /* 10 */
   short    fs_ifcs[32];                        /* 12 */
};
```


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DUART Channel Control Structure

The following structure defines the command and control interface between the host CPU and the SIO-4:

```
struct duart_channel {
   struct duart_channel *dc_other;        /* 0 */
   struct mc68681       *dc_duart_ptr;    /* 4 */
   short                dc_pid;           /* 8 Process id */
   ushort               dc_available;     /* 10 Channel is OK and
                                             FIFOs assigned */

   /*
   * Error words ...
   */

   ushort         dc_working;       /* 12 */
   ushort         dc_number;        /* 14 */
   unsigned long  dc_state;         /* 16 */
   ushort         dc_vector;        /* 20 */
   ushort         dc_level;         /* 22 */
union {                              /* 24 */
   struct { ushort p0_proc_error; ushort p0_cmd_error; } dc_p0;
   unsigned long dc_p1;
} error_union;
   unsigned long  dc_errslost;      /* 28 */
   unsigned long  dc_rawtim;        /* 32 */
   unsigned long  dc_brktim;        /* 36 */
   ushort         dc_delay;         /* 40 */

   /*
   * Horizontal movement control
   */

   ushort         dc_column;        /* 42 */
   ushort         dc_width;         /* 44 */
   unsigned long  dc_cflag;         /* 46 */
   unsigned long  dc_lflag;         /* 50 */
   unsigned long  dc_iflag;         /* 54 */
   unsigned long  dc_oflag;         /* 58 */
   unsigned char  dc_c_cc[16];      /* 62 */
   unsigned short dc_brgss;         /* 78 baud rate gen set sel */
   char           dc_flags[32];     /* 80 */

   /*
   * Drain support variables
   */

   unsigned long  dc_def_draintout; /* 112 */
   unsigned long  dc_draintout;     /* 116 */
   unsigned long  dc_dstart;        /* 120 drain start time */
   char           dc_line;          /* 124 */
```


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```
   /*
   * The dc_tmprawrd index forms a temporary read index into the
   * raw input FIFO to allow scanning of the FIFO for
   * interrupt characters even though the FIFO is not being fully
   * processed. This variable is only used in ICANON mode. Its value
   * is only valid while dc_current_fw_fifo is NULL.
   */
   short                       dc_tmprawrd;            /* 126 raw rd index */
   char                        dc_tmprawrd_invalid;    /* 128 */
   char                        dc_havedcd, dc_lostdcd; /* 129,130 */
   char                        dc_op, dc_ip;           /* 131, 132 */
   char                        *dc_echotbl;            /* 134 */
   unsigned long               dc_lchar;               /* 138 Last char state */
   unsigned long               dc_raw_sent;            /* 142 */
   unsigned long               dc_spare00;             /* 146 */
   unsigned long               dc_spare01;             /* 150 */
   unsigned long               dc_spare02;             /* 154 */
   unsigned long               dc_spare03;             /* 158 */
   struct term_control         *dc_tcp;                /* 162 */
   struct input_fifo_control   *dc_ifc;                /* 166 */
   struct fifo                 *dc_current_fw_fifo;    /* 170 */
   struct fifo                 *dc_hostinf;            /* 174 */
   struct fifo                 *dc_hostoutf;           /* 178 */
   struct port                 *dc_paddr;              /* 182 */

   struct scan {                                       /* 186 */
            struct scan        *sc_link;          /* 0 link to next struct */
            uword              sc_outcnt;         /* 4 output delay counter */
            uword              sc_iflag16;        /* 6 copy of control flags */
            uword              sc_odly;           /* 8 per char output delay */
            char               sc_pad0;           /* 10 pad character */
            char               sc_halt;           /* 11 output halted flag */
            char               *sc_saddr;         /* 12 duart status register */
            char               *sc_daddr;         /* 16 DUART data register */
            struct fifo        *sc_priority;      /* 20 priority output FIFO
            struct fifo        *sc_rawf;          /* 24 raw input FIFO */
            struct fifo        *sc_outf;          /* 28 normal output FIFO */
            uchar              sc_vstop;          /* 32 stop character */
            uchar              sc_vstart;         /* 33 start character */
            uchar              sc_overflow;       /* 34 rawf overflow flag */
            uchar              sc_iflagn8;        /* 35 iflag bits 16 to 23 */
            ulong              sc_chout;          /* 36 char transmit counter */
            ulong              sc_pchout;         /* 40 prio transmit counter */
            ulong              sc_chin;           /* 44 char receive counter */
            ulong              sc_ctrlcnt;        /* 48 ctrl char counter */
            char               sc_ctrlchar;       /* 52 control chars */
            char               sc_sp0;
            uword              sc_sp1;
   } dc_scan;

   struct ics {                                        /* 242 */
            ushort             ics_tas;           /* 0 */
            ushort             ics_cmd;           /* 2 */
            ushort             ics_modifier;      /* 4 */
            ushort             ics_arg1;          /* 6 */
            ushort             ics_arg2;          /* 8 */
            ushort             ics_arg3;          /* 10 */
            ushort             ics_arg4;          /* 12 */
            ushort             ics_signal;        /* 14 */
            unsigned long      ics_response;      /* 16 */
   } dc_ics;
};
```


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```
/*
 * #defines for dc_flags[ ]
 */

#define HOSTIPWAIT      0           /* Host waiting for data from SIOP */
#define FWREADINTR      1           /* F/W interrupt, data ready to read */
#define HOSTOPWAIT      2           /* Host waiting for output to drain */
#define FWWRITEINTR     3           /* F/W interrupt, data written */
#define HOSTCMDWAIT     4           /* Host waiting for command done.
                                    Will always generate an interrupt */
#define FWCMDDONE       5           /* F/W interrupt, command done */
#define FWSIGNAL        6           /* Have a dc_signal or HOSTSWITCH */
#define SYNCHAND        27          /* SIOSYNC handshake*/
#define HOSTLOSTDCD     28          /* Lost DCD signal */
#define HOSTCLIST       29          /* Host is using clists */
#define HOSTINZAP       30          /* Set by F/W to show hostinf zap */
#define HOSTFLUSH       31          /* Set by F/W to show host flush */

#define dc_cmd_lock           dc_ics.ics_tas
#define dc_cmd                dc_ics.ics_cmd
#define dc_modifier           dc_ics.ics_modifier
#define dc_arg1               dc_ics.ics_arg1
#define dc_arg2               dc_ics.ics_arg2
#define dc_arg3               dc_ics.ics_arg3
#define dc_arg4               dc_ics.ics_arg4
#define dc_signal             dc_ics.ics_signal

/*
* dc_lchar
*/

#define LCHAR_CR        0x0002          /* last char CR; next must be NL */
#define LCHAR_BS        0x0004          /* last char BS; next must be BS */
#define LCHAR_ESC       0x0008          /* last char ESC */
#define LCHAR           0x1000          /* last char horizontal tab */

/* dc_state */

#define CHANNEL_SUSP          0x80000000  /* Chan suspended by SIOSUSP cmd */
#define CHAN_NO_OPEN          0x40000000  /* nochan_init called by sinittab.
                                          Do not run channel process. */
#define READ_INTR_FLAG        0x20000000  /* Read interrupt flag */
#define TMP_BLK_OPEN          0x10000000  /* temp stop open, baud flip active */
#define SEND_SIGINTR          0x08000000  /* Ready to send a dc_signal intr */
#define HIFNF_MSG             0x04000000  /* Host input FIFO msg sent */
#define CHANNELA_VAILABLE     0x8000      /* chan process available to run */
#define CHANNEL_OPEN          0x4000      /* DUART open - do I/P processing */
#define SERVICE               0x1407      /* service condition for chan proc */
#define RAWTO                 0x0001      /* raw timeout in progress */
#define RAW_TIMEOUT_ACTIVE    0x00000001
#define CMD_DONE              0x0010      /* command request done */
#define OQAVA                 0x0020      /* outqueue got available */
#define RQCHR                 0x0040      /* rawqueue got character */
#define FOCHR                 0x0080      /* outFIFO got character */
#define FIAVA                 0x0100      /* inFIFO got available */
#define BLOCK                 0x0200      /* i/p blocked while rawq filled */
#define WAIT_OUTFIFO_EMPTY    0x0400      /* wait for raw o/p FIFO empty */
#define WBRK                  0x2000      /* wait for break complete */
#define WAIT_DRAIN            0x0800      /* wait for drain to complete,
                                             possible with timeout */
```


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```
/*
* MC68681 status register bit codes
*/
#define RECV_BRK        0x80        /* received break */
#define FRAME_ERR       0x40        /* framing error */
#define PARITY_ERR      0x20        /* parity error */
#define OVERRUN_ERR     0x10        /* overrun error */
#define DUART_ERR       0xF0        /* All the 68681 errors */

#define dc_cmd_error error_union.dc_p0.p0_cmd_error   /* Error in command */

#define dc_proc_error error_union.dc_p0.p0_proc_error /* process error, can
   be set by chanproc or the data processing code (sioinput/siooutput) */

#define dc_error error_union.dc_p1
```

Terminal Control Block

The structure used by SIOSETS to supply a new structure follows:

```
struct      term_control {
   unsigned long        tc_cflag;               /* 0 control modes */
   unsigned long        tc_lflag;               /* 4 F/W line discipline modes */
   unsigned long        tc_iflag;               /* 8 input modes */
   unsigned long        tc_oflag;               /* 12 output modes */
   unsigned char        tc_control_chars[16];   /* 16 control chars */
};

/* Control character offsets */
#define VINTR     0           /* signal character (default 0x7F = <del>) */
#define VQUIT     1           /* signal character (default 0x1C = ^) */
#define VERASE    2           /* erase char (default '#') */
#define VKILL     3           /* kill character (default '@') */
#define EOF       4           /* end of file character (default 0x04 = ^D) */
#define EOL       5           /* end of line character (default 0x00) */
#define EOL2      6           /* end of line character 2 (default 0x00) */
#define VSWTCH    7           /* signal character (default 0x7F) */
#define VSTOP     8           /* X-off (default 0x13 = ^S) */
#define VSTART    9           /* X-on (default 0x11 = ^Q) */
/* offset 10 to 15 not used (default 0x00) */
```

RAM Memory Layout

Typical Host Structures

Termio

The current System V termio structure follows:

```
#define     NCC 8

struct      termio {
   unsigned short       c_iflag;          /* 0 input modes */
   unsigned short       c_oflag;          /* 2 output modes */
   unsigned short       c_cflag;          /* 4 control modes */
   unsigned short       c_lflag;          /* 6 line discipline modes */
   char                 c_line;           /* 8 line discipline */
   unsigned char        c_cc[NCC];        /* 9 control chars */
};
```


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RADSTONE TECHNOLOGY

PME SIO-4 Extension Kit Application Note

The following two options are provided for converting the two 64-way connectors on the front of the SIO-4 into 25-way D-type connectors:

1) The Front Extension Kit (PME SIO-4FP-1) for users who require the outputs at the front of the rack.

2) The Rear Extension Kit (PME 10K/4) for users who wish to take the outputs to the rear of the rack.

Front Extension Kit

This has the following two components:

1) A PCB and front panel assembly with eight 25-way D-type connectors.

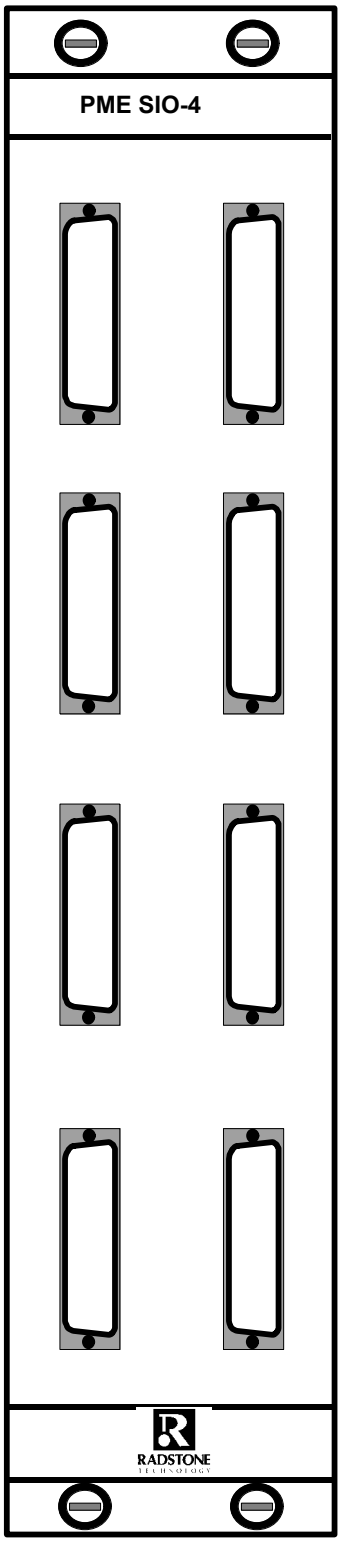
2) A cable with a 96-way Insulation Displacement Connector (IDC) at one end and a 64-way connector at the other.

The PCB/panel assembly has two 96-way connectors. This allows easy connection to either the upper or lower 64-way connectors on the SIO-4. To use all 16 channels on the SIO-4, two assemblies are required, with one cable in the upper socket and one in the lower.

Table 1.

Channel	DTE	DCE	Link
1 (9)	H1	H2	LK1
2 (10)	H3	H4	LK2
3 (11)	H5	H6	LK3
4 (12)	H7	H8	LK4
5 (13)	H9	H10	LK5
6 (14)	H11	H12	LK6
7 (15)	H13	H14	LK7
8 (16)	H15	H16	LK8

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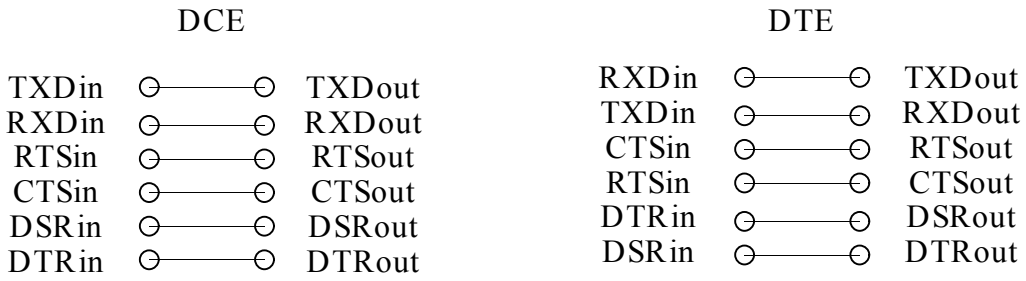
The diagram alongside shows the front extension kit front panel.

Associated with each channel on the SIO-4 are three sets of headers on the extension PCB (see Table 1). These allow the 25-way sockets to be configured for either Data Terminal Equipment (DTE) or Data Communication Equipment (DCE). To select DTE, insert all links in the DTE header. To select DCE, insert all links in the DCE header. The following table shows the configurations that the two options produce:

Pin	DCE Signal	DTE Signal
1	GND	GND
2	TXD	RXD
3	RXD	TXD
4	RTS	CTS
5	CTS	RTS
6	DSR	DTR
7	SGND	SGND
8	DCD	DCD
9	-	-
10	-	-
11	-	-
12	-	-
13	-	-
14	-	-
15	-	-
16	-	-
17	-	
18	-	
19	-	
20	DTR	DSR
21	-	-
22	-	-
23	-	-
24	-	-
25	-	-

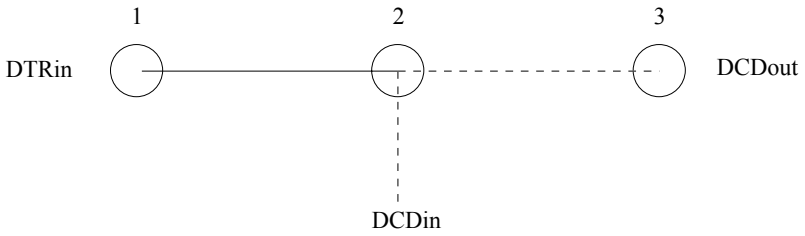
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The following diagram shows the arrangement of the headers (viewed from the component side of the board with the two 64-way DIN connectors on the right):



where 'in' implies connection to the SIO-4 and 'out' implies connection to the 25-way D-type connectors.

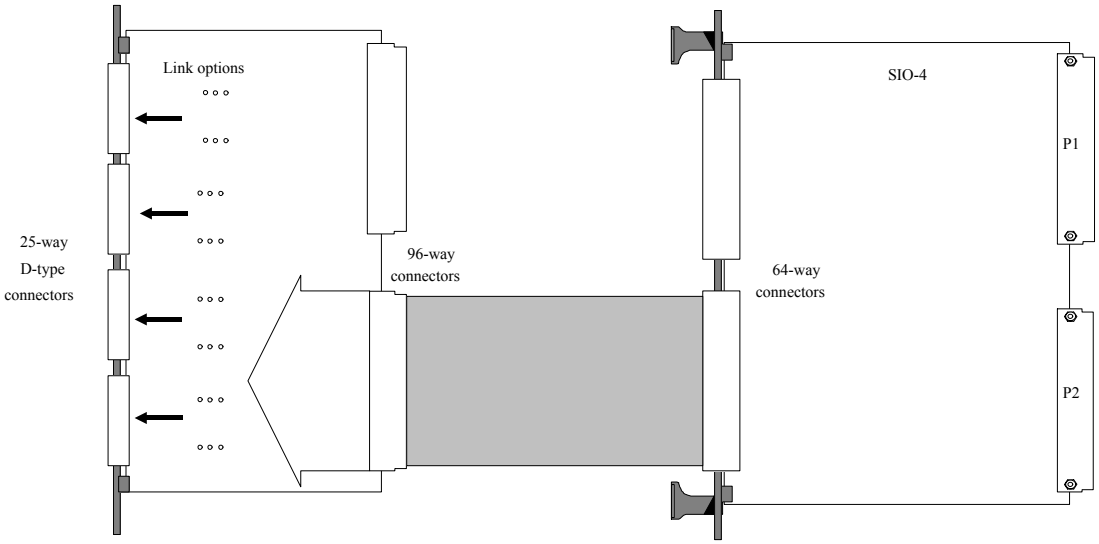
Links LK1 to LK8 select whether DCDin is connected to DCDout or DTRin, as follows:



By default, links 1 and 2 are joined, connecting DTRin to DCDin.

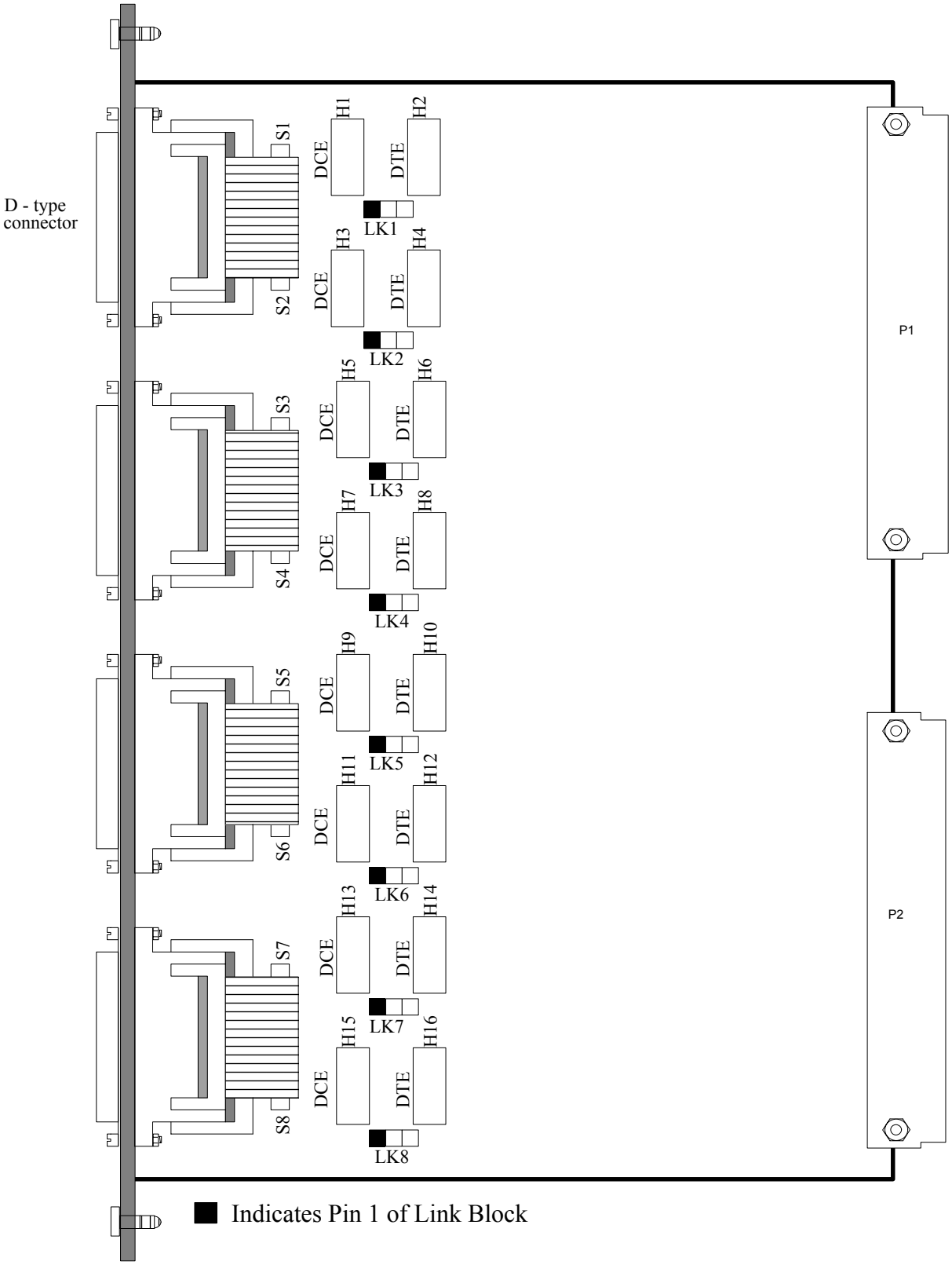
Fitting Instructions

To attach the extension kit, first plug the cable into either the upper or lower socket on the extension kit PCB. Holding the cable on the back of the PCB, fix the front panel into the rack using the four screws. Finally, insert the 64-way connector into the appropriate connector on the SIO-4. If two extension kits are to be used, then the cable to the right-hand kit needs to be plugged in first, so that it can be routed around the back of the left hand kit. The eight channels from each SIO-4 connector appear on the front panel as indicated by the numbers under each socket.



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Front Extension Kit Layout



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Rear Extension Kit

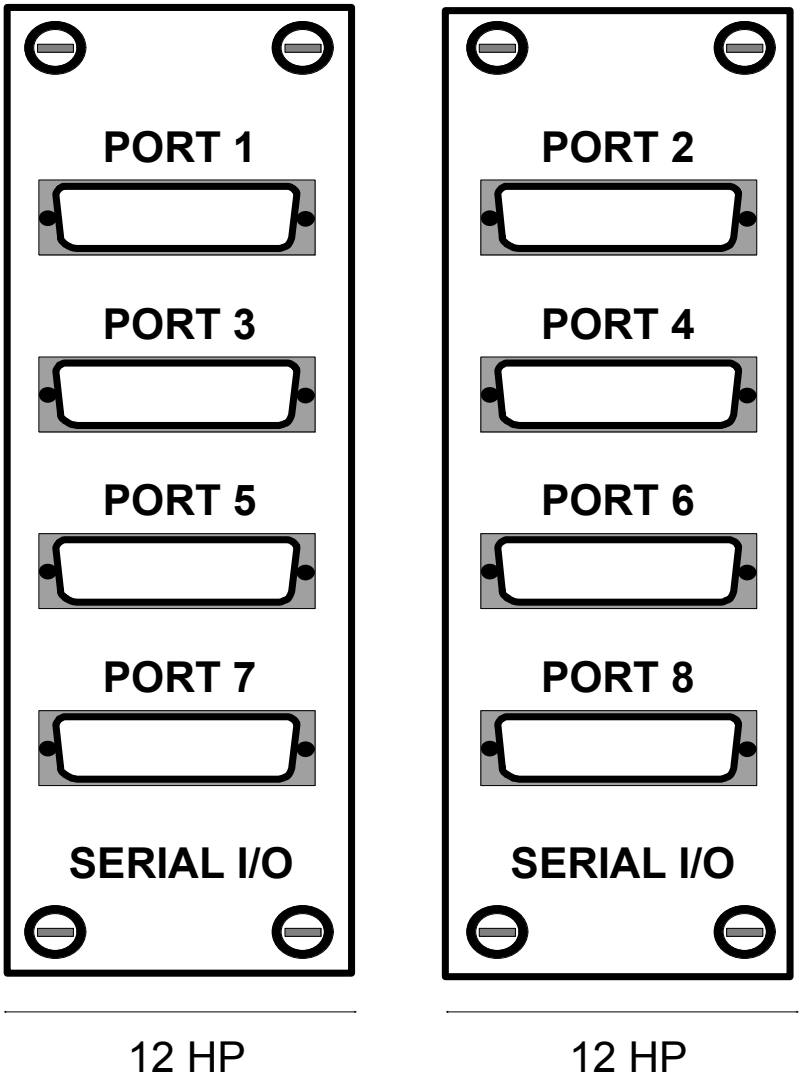
An SIO-4 board requires two IOK/4 rear extension kits for 16-channel operation. Each rear extension kit has the following three assemblies:

1) A PCB.

2) A 64-way ribbon cable with a 64-way IDC connector at one end and a 96-way IDC at the other.

3) Two ribbon cables with a 50-way header connector at one end and four D-type connectors on a panel at the other.

The fixing holes on the PCB allow it to be bolted between two 3U rails in a rack using M2.5 screws. Routing of the cables depends on the system layout, but it is recommended that the SIO-4 is placed in the rightmost available slot. The ribbon cables can then be routed to avoid blocking the airflow over the boards. The top 64-way socket on the SIO-4 provides channels 1 to 8 and the lower socket channels 9 to 16. The following diagram shows the rear extension kit front panel layout:



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Associated with each channel on the SIO-4 are three sets of headers on the extension PCB. These allow the 25-way sockets to be configured for either DTE or DCE operation. The following figure shows the headers associated with each channel:

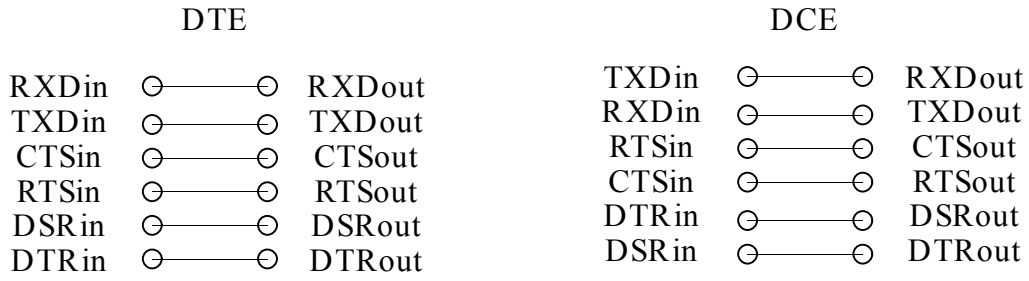
Channel	DCE	DTE (default)	Link
1 (9)	H1	H2	LK1
2 (10)	H3	H4	LK2
3 (11)	H5	H6	LK3
4 (12)	H7	H8	LK4
5 (13)	H9	H10	LK5
6 (14)	H11	H12	LK6
7 (15)	H13	H14	LK7
8 (16)	H15	H16	LK8

To select DTE, insert all links in the DTE header. To select DCE, insert all links in the DCE header. The following table shows the configurations that the two options produce:

Pin	DCE Signal	DTE Signal (default)
1	SHIELD	SHIELD
2	TXD	RXD
3	RXD	TXD
4	RTS	CTS
5	CTS	RTS
6	DSR	DTR
7	SGND	SGND
8	DCD	DCD
9	-	-
10	-	-
11	-	-
12	-	-
13	-	-
14	-	-
15	-	-
16	-	-
17	-	-
18	-	-
19	-	-
20	DTR	DSR
21	-	-
22	-	-
23	-	-
24	-	-
25	-	-

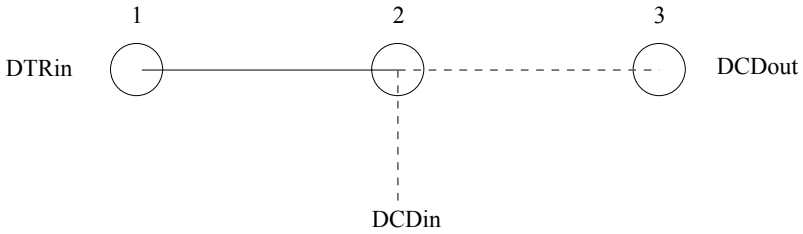
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The following diagram shows the arrangement of the headers (viewed from the component side of the board with the 64-way DIN connector on the right):



where 'in' implies connection to SIO-4 and 'out' implies connection to the 25-way D-type connectors.

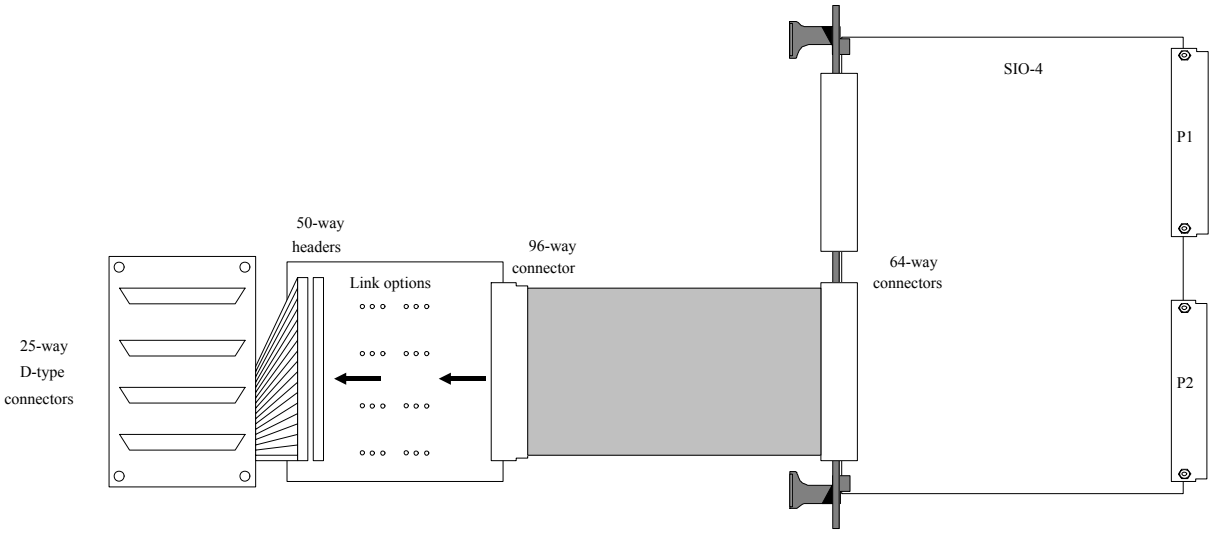
Links LK1 to LK8 select whether DCDin is connected to DCDout or DTRin, as follows:



By default, links 1 and 2 are joined, connecting DTRin to DCDin.

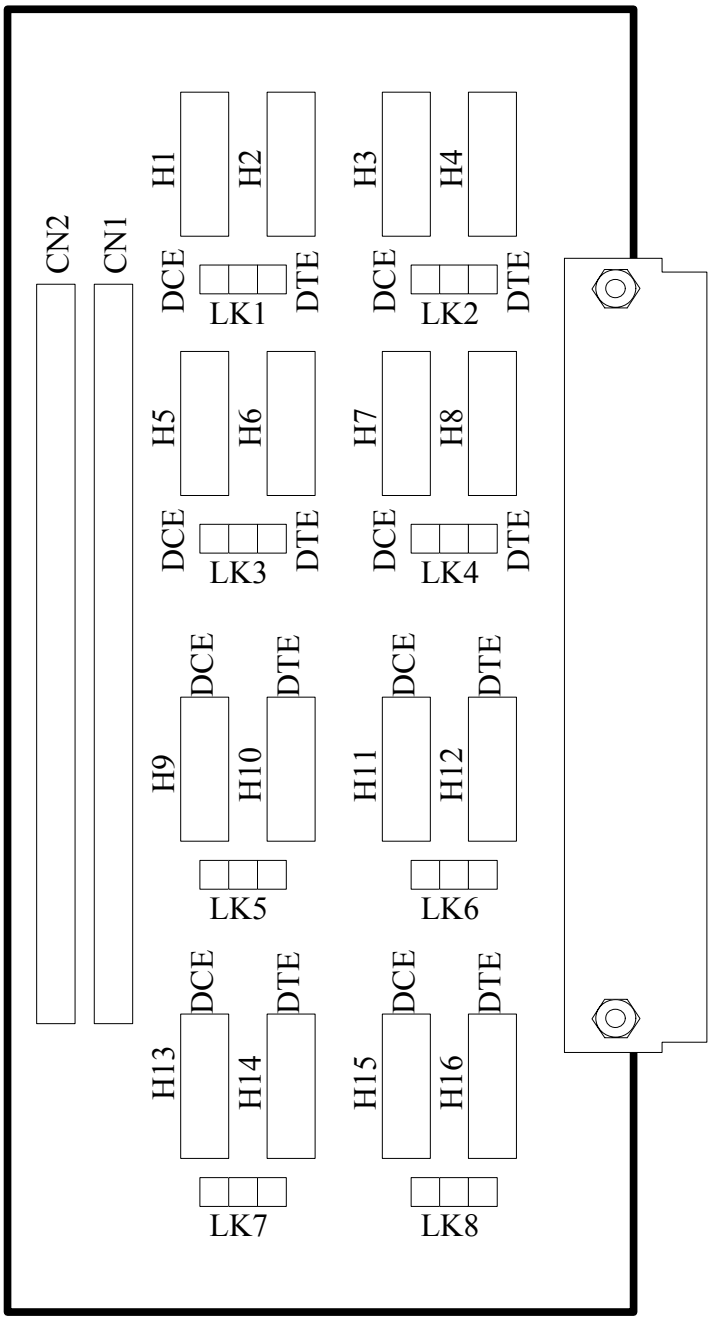
The connectors CN1 and CN2 on the PCB connect to the rear panels. CN1 carries ports 2, 4, 6 and 8; CN2 carries ports 1, 3, 5 and 7.

Rear Extension Kit Connection



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Rear Extension Kit Layout



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