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# Appendix C - PPC7A

This appendix contains hardware information for PPC7A boards. The information contained in this document must be used in conjunction with PowerX Quick Start, PowerX User Guides and/or the PowerX product Manual.

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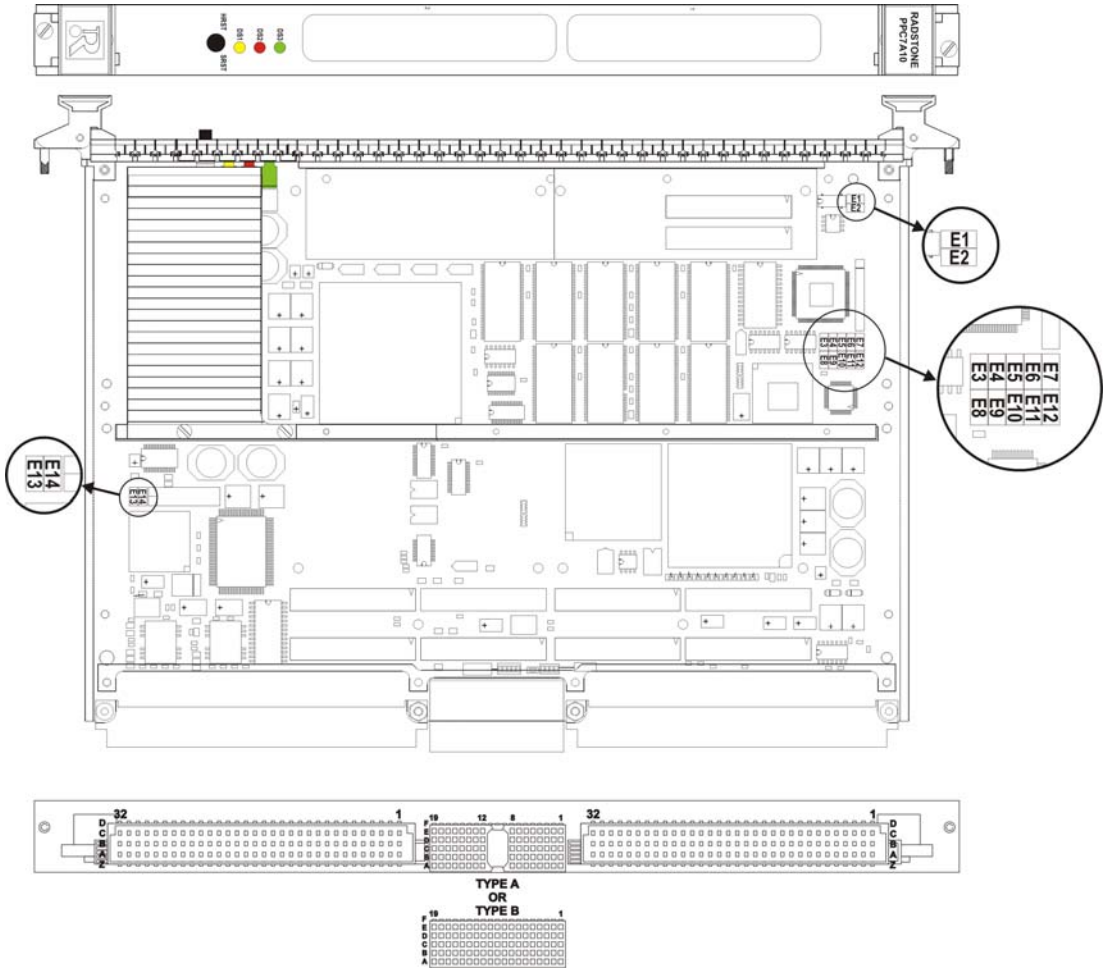


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# Link Settings

This section describes the configuration of links on the PPC7A. The board is delivered with push-on jumper links, but for more rugged or military applications, link pins must be connected using wire wraps.

**Figure C.1- Link Locations**




## Default Link Settings

The following table shows the factory default link settings:

| Link | Setting | Action |
|---|---|---|
| E1 | Out | Standby supply voltage is 5 volts |
| E3 | Out | User FLASH Write Protected |
| E4 | Out | Boot from System FLASH |
| E5 | Out | FLASH Write Protected |
| E6 | Out | ECC Disabled |
| E7 | Out | Select main Boot Image |

| Link | Setting | Action |
|---|---|---|
| E8 | Out | Boot from System FLASH |
| E9 | Out | System FLASH Write Protected |
| E13 | Out | On-board SCSI terminators disabled |
| E14 | Out | Reset Switch enable |
| E2, E10, E11,E12 | Out | ID links (board ID = 15) |

If you wish to change any of these linkable options, refer to the appropriate section(s) in the following pages.

**Note:** If you are about to install your board and power-up for the first time, leaving your board in the default configuration (as above), will enable board operation to be proved prior to tackling any more configuration issues.



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## RTC Standby Supply Voltage Link (E1)

This link selects the voltage of the standby supply to the I²C RTC (DS1337). As the normal VME standby voltage is 5 Volts, the link should not normally be fitted. However, the PPC7A can be linked to use a backup supply of 3.3 Volts.

**Note:** If the link is fitted the Backup supply should never be allowed to go above 3.5 Volts otherwise damage to the DS1337 device might result.

| SETTING | FUNCTION |
|---|---|
| In | 3.3 Volt standby |
| Out (default) | 5 Volt standby |

## FLASH Write Enable Links (E3 and E9)

Each link enables or disables erasure/reprogramming of a section of the FLASH. E3 controls the User FLASH and E9 controls the System FLASH, these links are used in conjunction with E5 (overall Flash write enable) . See the Functional Description section for details of FLASH operation.

| SETTING | FUNCTION |
|---|---|
| In | Enables erasure/reprogramming of the section of FLASH |
| Out (default) | Disables erasure/reprogramming of the section of FLASH |

**Note:** Regardless of any link settings for the FLASH write protection the Boot Recovery can't be write enabled and also the Boot data area can't be write protected. See the Functional Description section for more details of these FLASH areas. There is also software write protection that also inhibits write cycles to the flash, see software Flash write protection register 0x086A.

## VME Boot Link (E4)

This link holds the CPU in reset to allow a VME master to program boot code to the FLASH devices. To program the boot code into the FLASH devices the VME master will need to program both the Universe and the GT-64260 to enable a window from VME into the FLASH devices.

| SETTING | FUNCTION |
|---|---|
| In | VME programming mode |
| Out (default) | Normal boot mode |

Use of this link relies on the default Universe II configuration (see the VMEbus Interface Configuration section).

## Overall FLASH Write Enable Links (E5)

This link enables or disables erasure/reprogramming of a both sections of the FLASH. This link works in conjunction with E3 & E9 Flash write enable links.

| SETTING | FUNCTION |
|---|---|
| In | Enables erasure/reprogramming of the FLASH |
| Out (default) | Disables erasure/reprogramming of the FLASH |

**Note:** To give more flexibility to the system builder, the FLASH can also be write enabled by linking pin A2 of the P0 connector to Ground or Z1 of the P2 connector. There is also software write protection that also inhibits write cycles to the flash, see software Flash write protection register 0x086A.

## ECC Enable Link (E6)

This link enables or disables ECC on the SDRAM, as follows:



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| SETTING | FUNCTION |
|---|---|
| In | Enables ECC |
| Out (default) | Disables ECC |

**Note:** This link only provides status information in register 0x0866, the software running on the PPC7 will control the operation of the ECC, therefore it is possible that this feature may not be supported by the software.

## FLASH Boot Image Select Link (E7 & E8)

The System FLASH is divided into four sections, with all sections accessible all the time. Using these links, the four sections can be swapped around in the memory map. This allows for two (three if the data area is not required) boot images to be blown into the FLASH and a Factory blown Boot recovery image, with the links selecting which image is used at boot time. The state of the links is reflected in the Memory Configuration Register (Port 0x0804). Normally, these links are not fitted and the PPC7A boots from the default boot area from FLASH (see the Functional Description section for details of FLASH operation). However, when either of the links are fitted, the PPC7A boots from an alternate boot image. After boot time, the link setting can be overridden by software to select the different images.

| E7 | E8 | FUNCTION |
|---|---|---|
| Out (default) | Out (default) | Normal FLASH boot image operation |
| Out | In | Alternate FLASH boot image |
| In | Out | Recovery Boot image |
| In | In | 2nd Alternate FLASH boot image (Data area) |

## On-board SCSI Terminator Enable Link (E13)

This link enables or disables the on-board SCSI terminators, as follows:

| SETTING | FUNCTION |
|---|---|
| In | Enable on-board SCSI terminators |
| Out (default) | Disable on-board SCSI terminators |

If you are using the SCSI bus, you are recommended to locate the PPC7A at one end and enable the terminator by fitting link E13. If you want to use the PPC7A somewhere other than at the end of the SCSI bus, ensure that E13 is not fitted.

**Note:** Fitting E13 when the PPC7A is not located at the end of a SCSI bus may cause erroneous SCSI operation. This link can be overridden by a control register.

## Enable Front Panel Reset Switch Link (E14)

This link enables or disables the front panel reset/abort switch, as follows:

| SETTING | FUNCTION |
|---|---|
| In | Disable reset switch |
| Out (default) | Enable reset switch |

**Note:** The function of this link is the opposite of most other Radstone PPC cards.



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## Geographical Addressing/Board ID Links (E11, E2, E12 and E10)

These links form a 4-bit board ID that may be read from the ID Link register (see the Functional Description section). The links are decoded as follows:

| Board ID | E10 | E12 | E2 | E11 |
|---|---|---|---|---|
| 15 (default) | Out | Out | Out | Out |
| 14 | Out | Out | Out | In |
| 13 | Out | Out | In | Out |
| 12 | Out | Out | In | In |
| 11 | Out | In | Out | Out |
| 10 | Out | In | Out | In |
| 9 | Out | In | In | Out |
| 8 | Out | In | In | In |
| 7 | In | Out | Out | Out |
| 6 | In | Out | Out | In |
| 5 | In | Out | In | Out |
| 4 | In | Out | In | In |
| 3 | In | In | Out | Out |
| 2 | In | In | Out | In |
| 1 | In | In | In | Out |
| 0 | In | In | In | In |

Links E11, E2, E12 and E10 are also connected to the VME64 GA0~ to GA3~ signals respectively on P1 row D (see the P1 connector description in the Connectors section). If you wish to sense the status of the Geographical Address signals, do not fit these links, as they connect the signals to 0 Volts.

### VME Slave Address Configuration

The board ID should be set up according to the system slot into which the board is inserted, as shown in the following table. The board ID also sets the board's VME slave addresses, as shown, so take care to avoid an address clash with other boards in the system.

| Slot | Slot 1 Functions | Board ID | A32 Address | A24 Address |
|---|---|---|---|---|
| 1 | Yes | 0 | 0x0000 0000 | 0x00 0000 |
| 2 | No | 1 | 0x1000 0000 | 0x40 0000 |
| 3 | No | 2 | 0x2000 0000 | 0x80 0000 |
| 4 | No | 3 | 0x3000 0000 | 0xC0 0000 |
| 5 | No | 4 | 0x4000 0000 | None |
| 6 | No | 5 | 0x5000 0000 | None |
| 7 | No | 6 | 0x6000 0000 | None |
| 8 | No | 7 | 0x7000 0000 | None |
| 9 | No | 8 | 0x8000 0000 | None |
| 10 | No | 9 | 0x9000 0000 | None |
| 11 | No | A | 0xA000 0000 | None |
| 12 | No | B | 0xB000 0000 | None |
| 13 | No | C | 0xC000 0000 | None |
| 14 | No | D | 0xD000 0000 | None |
| 15 | No | E | 0xE000 0000 | None |
| 16 | No | F | 0xF000 0000 | None |

**Note:** Any change to the Board ID links will require the hardware registers to be 'relearned' if BIT is not to fail.



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## VMEbus Interface Configuration

Several operating features of the Universe II VME interface are set at power-up or reset by surface mount jumper links. All of these, except local register access, may be overridden by software. The default settings are:

| Operating Feature | Setting |
|---|---|
| Register access slave image from vmebus | Enabled in A32 space at 0x8000 0000 |
| VME cr/csr slave image | Disabled |
| PCI slave image 0 | Enabled in PCI memory space at 0xF000 0000 to 0xFFFF FFFF |
| Local register access | PCI I/O space |
| Auto-id scheme | Disabled |

Changing the default power-up options requires surface-mount rework tools and would normally only be done at the factory. Further details are available from technical support at Radstone.



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# Functional Description

## Introduction

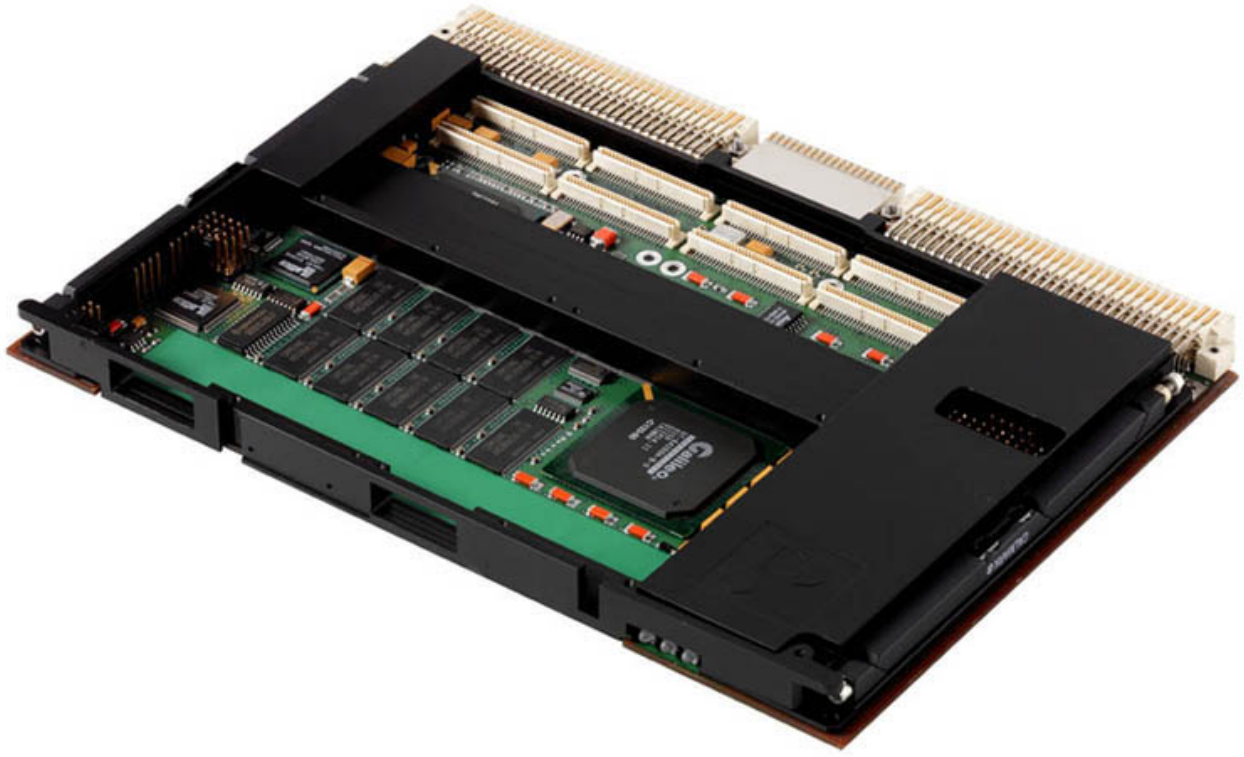
The PPC7A is a highly integrated, VMEbus processor using the PowerPC 745x RISC CPU with integrated L2 cache and a private L3 cache bus or the PowerPC 7410/755 RISC CPU with a private L2 cache bus. The product offers an extensive range of standard functions including processors clocked at 1000 MHz and above, 2 Mbytes of L2 (or L3 if 745x fitted) cache, user SDRAM up to 1024 Mbytes on-board with ECC, on-board serial, parallel, and two channels of 10/100 base Ethernet, up to 256 Mbytes of FLASH memory, and Ultra-SCSI processor, a 64-bit VMEbus interface, and direct connection for a keyboard and mouse.

Expansion capabilities are provided by two 64-bit/66 MHz PCI interface slots. PCI (IEEE P1386.1) provides an industry-standard, high-speed (528 Mbytes/second) local expansion bus, designed for graphics, high-speed communications (e.g. ATM, FDDI, ISDN, etc.), multi-media and user-defined custom functions. PCI has established itself as the leading local interconnect standard, and the wide availability of compatible devices, coupled with its adoption on an array of platforms, ensures that PCI-based modules are both high-performance and low cost.

The highly integrated nature of the PPC7A makes it a true single board computer. In many ways, the PPC7A resembles a high performance PC motherboard, although in a more rugged, lower profile and more compact form factor.

The PPC7A has been designed to be a plug in upgrade/replacement of the PPC range of PowerX boards. To enhance the connection capabilities, the PPC7A uses 5-row P1 and P2 connectors, but still retains the PPC basic pinout.

**Figure C.2 - PPC7A General View**





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## Features

- Various PowerPC processor options including the PowerPC 7457 CPU at 1000 MHz and above (**contact your nearest Sales office for details of speed grades**) gives low power, low cost, high performance PowerPC RISC CPU and system interfaces all on one device as main system resource
- Up to 1024 Mbytes of SDRAM with optional ECC for memory intensive applications
- Two 64-bit/66 MHz PCI expansion slots on-board give system expansion using IEEE P1386.1 standard single or double width PMCs
- Optional PCI expansion bridge (on a short PMC card) and PMC carrier cards future proof your system design by enabling PCI sub-system expansion to add new, low cost interface capability as required
- Two on-board Ethernet controllers giving 10/100BaseT
- Radstone COTS software support includes BIT, Boot firmware, BSPs and ESPs (with BCS) for LynxOS/LynxOS HA, Tornado II / VxWorks and INTEGRITY
- Wide range of shrink-wrapped application software available
- 2 Mbytes of cache memory on a private cache bus
- 256 Mbytes of FLASH ROM
- 32 Kbytes of NOVRAM
- Real Time Clock (TOD/calendar) with battery backup using VME standby supply
- Temperature Sensor
- Ultra-SCSI I/O processor
- 2 off RS232 serial I/O channels up to 115.2 kbaud
- 2 off RS232/RS422 (factory selected) serial I/O channels up to 115.2 kbaud
- 2 off RS485/422/232 software selectable serial I/O channels up to 1 Mbaud
- Parallel printer port
- 16 bit wide IO interface
- Keyboard/mouse interface
- Floppy disk controller
- VME64 interface using Tundra Universe II VMEbus interface chip
- High-resolution VGA graphics
- Single slot 6U VME form factor for reduced system cost and slot count
- Range of 3U rear-mounting I/O modules
- ANSI/VITA 1-1994 VME64 and VME64 extensions (5 row P1 and P2) compatible
- Five build standards
- Optional software maintenance giving automatic software revision updates and technical support
- Optional hardware and on-board firmware configuration management service giving a unique part number requiring customer authorisation for changes in product revision status



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## PowerPC Platform

The PowerPC Platform is an example implementation of a philosophy designed to allow software compatibility across different platforms based on the PowerPC processor. Aiming to achieve an open standard, the PowerPC Platform encourages the use of industry standard components and buses, and a wide range of operating systems.

As well as providing a detailed hardware design specification, the PowerPC Platform also embodies a software mechanism that allows the hardware to be isolated from the application by abstraction layers. It is these abstraction layers (in effect very low-level system drivers) that are the key to differentiation, scalability and future-proofing. Operating systems, applications and drivers can 'sit' on these layers without needing to be aware of the underlying hardware (other than general functionality). This is fundamentally different from PCs, which use a BIOS that ultimately constrains operating systems and applications alike.

The major purpose of the PowerPC Platform architecture "... is to give direction to system designers, while still enabling differentiation in areas where real value can be added, thus allowing the PowerPC microprocessor industry to build a reusable body of OS and application software...". The knowledge that both OS and application programs will run on any host that complies with the PowerPC Platform architecture provides security for today's valuable software investments, as well as expansion capabilities for the future.

## PowerPC Processors

### MPC7457

The PowerPC 7457 is a 32-bit superscalar RISC processor, clocked at 1000 MHz and above, with the following features:

- A 32-bit implementation of the PowerX architecture
- 32 Kbytes, 8-way set associative instruction and data caches
- A separate 64-bit wide, two-way set associative L3 cache bus
- 64-bit external data bus
- On-chip 32 Kbyte instruction and data caches
- On-chip 256 Kbyte of L2 Cache
- Enhanced branch prediction capabilities
- MMU and integral FPU
- On-chip L3 cache controller that connects to a private L3 cache bus operating at up to 200 MHz

The PowerPC 7457 implements a fully static architecture and offers sophisticated power management capabilities. As a result, its maximum power consumption is less than 20 Watts at 1000 MHz.

| PowerPC CPU | CPU Frequency (MHz) | SPECint95 | SPECfp95 |
|---|---|---|---|
| 7457 | 733 | 32.1 | 23.9 |

The processor has a 32-bit physical address bus and a 64-bit data bus.

| Processor Type | Bus Frequency (MHz) | L3 Frequency (MHz) | Core Frequency (MHz) |
|---|---|---|---|
| MPC7457 | 100 | 166 to 266 | 1000 and above |



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### L3 Cache

The L3 cache has the following features:

- Two-way set associative
- 32-byte line size
- 64 bits wide
- Capable of operating in write-through or write-back modes
- Operation at speeds up to 266 MHz through a dedicated L3 cache bus interface
- Can caches memory accesses in the address range 0x0000 0000 to 0x4000 0000 (i.e. SDRAM)
- Entries in write-through mode can be valid or invalid
- Entries in write-back mode can be invalid, valid-unmodified or valid-modified

Having the L3 cache controller inside the MPC7455 allows performance to be further enhanced by parallel compares on L1, L2 and L3 tags, and filtering L3 cache traffic from the system bus. Full coherency on the system bus can be maintained.

L3 cache access times from the processor for a 32-byte burst are:

| | 200 MHz L3 Interface | Transfer Rate |
|---|---|---|
| Burst read hit non-pipelined | 3,1,1,1 | 1066 Mbytes/second |
| Burst read hit pipelined | 1,1,1,1 | 1600 Mbytes/second |

### PowerPC 7410

The PowerPC 7410 is a 32-bit superscalar RISC processor, clocked at 500 MHz and above, with the following features:

- 64-bit external data bus
- On-chip 32 Kbyte instruction and data caches
- Enhanced branch prediction capabilities
- MMU and integral FPU
- On-chip L2 cache controller that connects to a private L2 cache bus operating at up to 200 MHz
- A 32-bit implementation of the PowerX architecture
- 32 Kbytes, 8-way set associative instruction and data caches
- A separate 64-bit wide, two-way set associative L2 cache bus

The processor has a 32-bit physical address bus and a 64-bit data bus.

| Processor Type | Bus Frequency (MHz) | L2 Frequency (MHz) | Core Frequency (MHz) |
|---|---|---|---|
| MPC7410 | 100 | 166 to 266 | 500 and above |

The PowerPC 7410 implements a fully static architecture and offers sophisticated power management capabilities. As a result, its maximum power consumption is less than 12 Watts at 500 MHz.

| PowerPC CPU | CPU Frequency (MHz) | SPECint95 | SPECfp95 |
|---|---|---|---|
| 7410 | 500 | 22.8 | 17 |

**Note:** The above estimated values are supplied by Motorola Semiconductor, and illustrate the performance and power dissipation of the CPU. Radstone PowerX SBCs are designed to take the processor, providing a balanced general-purpose platform. The actual performance and power dissipation may vary depending on the application being run and resource usage of the configured system.



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### L2 Cache

The L2 cache has the following features:

- Two-way set associative
- 32-byte line size
- 64 bits wide
- Capable of operating in write-through or write-back modes
- Operation at speeds up to 266 MHz through a dedicated L2 cache bus interface
- Can caches memory accesses in the address range 0x0000 0000 to 0x4000 0000 (i.e. SDRAM)
- Entries in write-through mode can be valid or invalid
- Entries in write-back mode can be invalid, valid-unmodified or valid-modified

Having the L2 cache controller inside the MPC7410 allows performance to be further enhanced by parallel compares on L1 and L2 tags, and filtering L2 cache traffic from the system bus. Full coherency on the system bus can be maintained.

L2 cache access times from the processor for a 32-byte burst are:

| | 200 MHZ L3 INTERFACE | TRANSFER RATE |
|---|---|---|
| Burst read hit non-pipelined | 3,1,1,1 | 1066 Mbytes/second |
| Burst read hit pipelined | 1,1,1,1 | 1600 Mbytes/second |

## PCI

PCI has become a highly desirable local interface bus, due to its high bandwidth, glueless interface and low cost. PCI provides a synchronous 32 or 64-bit multiplexed address and data bus at speeds of 33 or 66 MHz, allowing burst data transfers to 528 Mbytes/second. The PPC7A uses PCI to provide a high-speed backbone for local interconnection of on-board devices (processor, VGA, Ultra-SCSI, South bridge and VME64, all of which have direct PCI connectivity). The Tundra Universe II chip provides full PCI to VME bridge capability.

As well as local interconnection of on-board devices, PCI also allows communication with optional mezzanine expansion modules (PMCs). The PCI mezzanine format also provides 64 I/O pins for user definition. A range of PMCs are available from Radstone, including high-performance graphics, MIL-STD-1553, asynchronous serial, Fast Ethernet, FLASH memory, Fibre Channel and ATM, all fully compliant with the IEEE P1386.1 standard.

Using the PCI to PCI bridge device on the PMCPCI bridge card (see overleaf), the PPC7A can maintain concurrent bus operation. This allows applications using PMCs for routing and communications to operate efficiently and in parallel without being blocked.

### PCI Bridge and Memory Controller

The Galileo GT-64260 Discovery provides the CPU to Memory-PCI bridge. This interfaces the processor to the SDRAM, FLASH and the two PCI buses.

### PCI Expansion Bus

Two PMC slots are provided as standard on the PPC7A. These PCI slots are 64 bits wide and run at 66 MHz. If a PCI card is fitted that is not capable of running at 66 MHz, then the PPC7A will reduce the frequency to 33 MHz for both PCI slots.



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For those configurations requiring additional PCI functionality, the PMC to PCI Bridge card (PMCPCI) bridges the on-board PCI bus out via the P0 connector, allowing use of a range of P0 PMC carriers, or interfacing the PPC7A directly to Radstone's range of SHARC-based DSP boards.

To connect the PPC7A to P0-based carrier cards such as the P0CC1, a series of P0 add-on backplanes are available. These are PCBs for attaching to a system backplane that has J0 connectors fitted. The following variants are available:

| Variant | PCI Backplane Slots | Master Slots | P0cc1 Slots |
|---|---|---|---|
| P0BP1-502 | 2 | 1 | 1 |
| P0BP1-503 | 3 | 1 | 2 |
| P0BP1-504 | 4 | 1 | 3 |
| P0BP1-505 | 5 | 1 | 4 |

The P0BP1 backplane must be soldered onto the J0 system backplane, and can be used with either type A or type B J0. These backplanes are intended to have a host SBC with PMCPCI card plugged into the master slot, which is the left-most slot of the P0 PCI backplane. For further information about P0 backplanes, please contact Radstone directly or talk to your nearest Sales Office.

### PCI Configuration

The boot process must configure the base address and space type (memory or I/O) of all the PCI attached peripherals. The memory requirements of each PCI device are given in the appropriate device descriptions in this section.

Each PCI device also has several registers located in PCI configuration space, which is accessed by the processor through the GT64260 PCI bridge and memory controller using the CONFIG_ADDR and CONFIG_DATA registers. A full description of PCI configuration can be found in the GT64260 specifications.

The device number mapping for the PCI bus 0 attached to the GT64260 is as follows:

| Device No. | Function |
|---|---|
| 0 to 15 | Not implemented |
| 16 | 53C860 SCSI controller |
| 17 | Not implemented |
| 18 | South bridge |
| 19 | Not implemented |
| 20 | Universe II VME controller |
| 21 | Graphics |
| 22 to 30 | Not implemented |

The device number mapping for the PCI bus is as follows:

| Device Number | Function |
|---|---|
| 0 TO 22 | Not implemented |
| 23 | PMC2 |
| 24 | PMC1 |
| 25 TO 30 | Not implemented |



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### PCI Buses

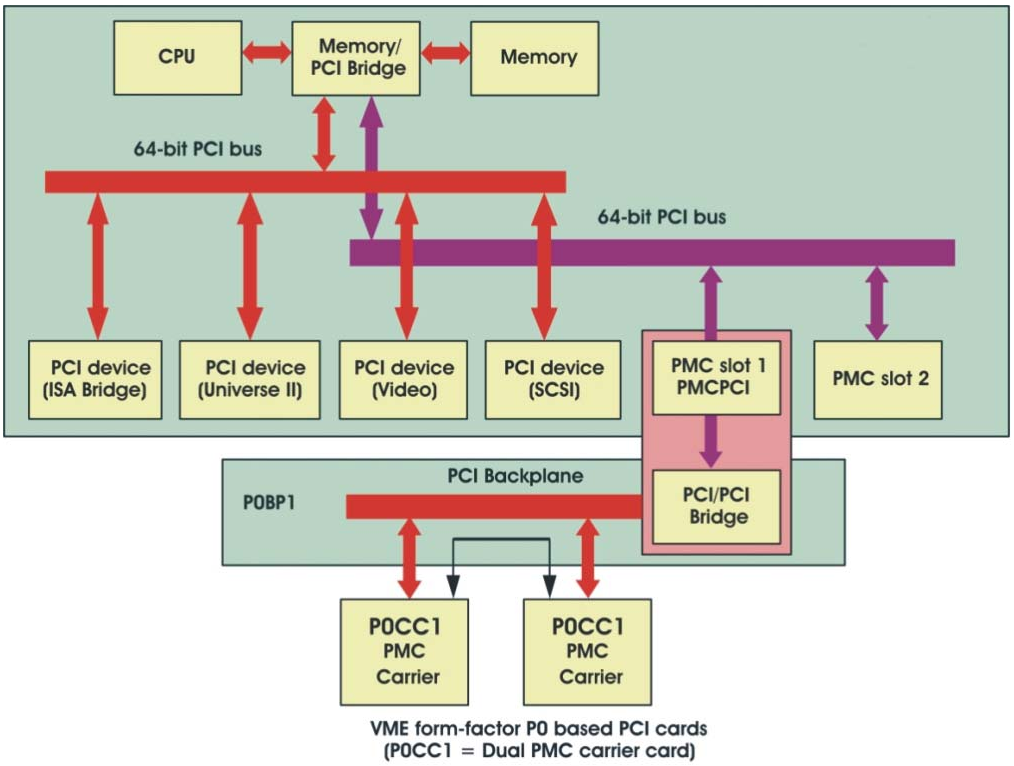
There are two PCI buses on the PPC7A.

PCI0 is connected to all of the on-board PCI devices. This bus is implemented as a 64-bit PCI bus running at 33 MHz (64-bit to Universe device only). This gives a burst rate up to 264 Mbytes/second between PCI agents.

PCI1 is the PCI bus that is routed to the PMC sites, the CPU Host bridge interface. This bus is implemented as a 64-bit PCI bus running at up to 66 MHz. This gives a burst rate up to 528 Mbytes/second between PCI agents.

The PCI bus structure of the PPC7A is shown below:

**Figure C.3 – PCI Bus Diagram**




### Memory/PCI Bridge

The Memory/PCI Bridge on the PPC7A is provided by a Galileo GT64260 Discovery device:

- This device provides:
- Host Bridge between the processor bus and the two PCI buses
- PCI arbiters
- SDRAM memory controller and FLASH interface (see the Memory section)
- 2 off Ethernet MACs
- 2 off Serial channels (COMs 3 & 4)



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### Ethernet Controller

The GT64260 device provides two ethernet MACs. To interface these to the physical interface two National Semiconductor DP83846s are used.

The DMA controllers handle data transfers between CPU memory and on-chip memory with the Ethernet Controller arbitrating between DMA channels to minimise underflow or overflow.

Automatic packet deletion on receive (runt packets or after a collision) and packet re-transmission after a collision on transmission are supported. This minimises bus traffic by removing unnecessary accesses to shared memory. The network addresses (Ethernet number) are factory configured.

Connection to the Ethernet controller is via the P2 connector (see the Connectors section). Eight associated status LEDs (DS16 to DS23) are mounted on the rear of the board near the Ethernet PHY chips (see the Software Programmable LEDs section). The default functions of these LEDs are link, TX activity, RX activity status, and 100BaseT, but they may be overridden by the software.

### SCSI Scripts Processor

The NCR53C860 SIOP executes commands, in the form of SCSI scripts. It has a PCI interface and a DMA controller, which are used to access the scripts and data held in system memory. The SIOP can transfer data at 7 Mbytes/second asynchronously and 20 Mbytes/second synchronously or 14 Mbytes/second asynchronously. Connection to the SCSI bus is made through the P2 connector. The pinout is given in the Connectors section.

The PPC7A has an on-board active SCSI terminator, which may be enabled or disabled with a jumper (see the E13 description in the Jumper Settings section). The SCSI specification allows a maximum cable stub length of 10 cm. If the SCSI bus connections are taken directly from the backplane J2 connector, then the PPC7A may be located anywhere on the SCSI bus and the terminator should only be enabled if the PPC7A is at the end of the SCSI bus. Otherwise, the PPC7A must be at the end of the SCSI bus and the terminator must be enabled.

A software programmable SCSI Activity LED (LED DS11) is mounted on the back of the board. See the Software Programmable LEDs section and the SCSI Activity LED Register description for more details.

### VGA graphics Processor

The PPC7A uses an Asiliant Technologies 69000 or 69030 PCI to VGA graphics processor device. This is a totally integrated high performance graphics accelerator with integrated 2Mbytes (4Mbytes with the 69030) of fast graphics SDRAM.

The 69000 can provide pixel clock rates at up to 135Mhz (170Mhz with the 69030) and pixel colour depths of up to 24 bit. This gives the maximum resolutions of:

- 1280 x 1024 x 8 @ 75Hz (1280 x 1024 x 24 @ 75 Hz with 69030)
- 1024 x 768 x 16 @ 85Hz (1024 x 768 x 24 @ 85 Hz with 69030)
- 800 x 600 x 24 @ 85Hz

### Universe II

This provides the VMEbus Interface. See later.



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### South Bridge

An ALI-M1535 provides a bridge from the PCI bus to the ISAbus for connection of native I/O devices. This device also provides the following functions:

| FUNCTION | EQUIVALENT TO FUNCTION OF |
|---|---|
| 7 channel DMA between ISAbus and PCI bus | Two 83C37s |
| Timer block | One 82C54 |
| Interrupt controller | Two 8259s |
| PCI bus arbiter | - |

The south bridge positively decodes some I/O cycles on the PCI bus for internal resources. It subtractively decodes and claims all PCI memory and I/O cycles not claimed by other PCI targets, and forwards them to the ISAbus.

Apart from the south bridge, there are no other ISAbus masters in the PPC7A architecture.

### PMC Sites

The PPC7A has two sets of connectors ({J11, J12, J13, J14} and {J21, J22, J23, J24}) that allow standard PMCs to be connected to the PCI bus. The PPC7A can accept either air-cooled or conduction cooled PMCs, as long as adequate cooling is provided. Air-cooled PMCs are defined in the IEEE 1386 Standard. Front panel I/O is fully supported.

The PMC I/O connectors are routed to the backplane connectors to allow backplane I/O. J14 (PMC site 1) is connected to P0 and J24 is partially connected to P2.

Fitting a PMCPCI card allows the PCI bus to come out to the backplane via P0 (must be fitted in PMC slot 1).

## VMEbus Interface

The Tundra Semiconductors CA91C142 Universe II PCI to VME bridge provides the VMEbus interface. This complies with the VME64 specification and provides:

- All slot 1 (system controller) functions
- Interrupt control
- A DMA controller
- Interprocessor communications
- Block transfer support

The Specification section details the VMEbus compliance and basic VMEbus performance of the PPC7A.

**Note:** The Universe II does not self-address.

### VMEbus Master Access

Four general-purpose, software-programmable PCI slave images are available for access to the VMEbus.

- All of these can be configured to access VMEbus A32, A24 or A16 address space
- An offset may be applied to translate the local address to a different address on the VMEbus, allowing any local address to access any VMEbus address
- The start and end addresses of the A32, A24 and A16 PCI slave images may be set on any 64 Kbyte boundary in PCI memory or I/O space that is not allocated to other PCI-attached devices or the user FLASH
- One image may be set on 4 Kbyte boundaries to accommodate access to A16 space



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One further, special purpose, PCI slave image allows mapping of A16 and A24 space.

- This slave image uses a 64 Mbyte window, aligned to any 64 Mbyte address in PCI memory space
- The window is divided into four 16 Mbyte quadrants
- The top 64 Kbytes of each quadrant maps to A16 space, while the rest of each quadrant maps to A24 space
- The Address Modifiers generated are software configurable for each quadrant

VMEbus master cycles may be coupled or write posted.

- Coupled cycles are retried on the PCI bus until the Universe II has ownership of the VMEbus and are not terminated on the PCI bus until all data has been transferred over the VMEbus
- Posted writes are queued in a FIFO until the VMEbus is available for the data to be transferred

### VMEbus Slave Access

Four general-purpose, software-programmable VMEbus slave images are available.

- All of these may be defined in VMEbus A32, A24 or A16 space
- An offset may be applied to translate the VMEbus address to a different address on the local bus, allowing any VMEbus address to access any on-board address
- The start and end addresses of the A32, A24 and A16 images may be set on any 64 Kbyte boundary

One further, special purpose, VMEbus slave image, the Register Access Slave Image, allows a VMEbus master to access to the Universe II control and staus registers.

VMEbus slave accesses to the PPC7A may be coupled, write posted or pre-fetched block read.

- Coupled slave transfers can only proceed once the slave posted write FIFO is empty
- Slave posted write cycles are queued in a FIFO until the PCI bus is available for the data to be transferred

## Utility I/O and Auxiliary Function Bus

To take full advantage of low-cost, industry standard components, general purpose I/O and auxiliary functions are implemented through an South bridge bus interface. Facilities provided include:

- Parallel/printer port
- Four PC-compatible serial interfaces
- Floppy disk controller
- Real-time clock
- Keyboard/mouse interface
- USB

## Input/Output

The PPC7A has a wide variety of possible I/O connectivity, including the following ports:

- Ultra-SCSI
- Ethernet
- Serial



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- Mouse/keyboard
- Parallel/printer
- USB
- VGA-Graphics

To maximise the flexibility of connecting to these ports, a range of I/O modules are available, attached by a VME P2 transition module. Using rear I/O minimises the effort needed to remove boards from a rack, so improving maintainability and reliability.

## Software Support

Radstone's software strategy for PPC boards allows fully integrated system-level solutions to be realised easily and with confidence. Off-the-shelf, layered software modules deliver the most from low-level hardware features while exploiting the best high level debug and run-time functionality of popular COTS operating systems and communications modules.

The software products described below build on those available for previous generations of the PowerX family, so providing a common look, feel and interface for technology inserts.

Radstone has invested more than 50 man-years of engineering talent into the PowerX architecture so that customers can develop market-leading products using the O/S and development environment best suited to their long term program requirements.

## Boot Firmware

Developed as an integral part of the Radstone PowerX strategy, the Boot firmware provides a foundation layer to interface between the raw Radstone board hardware, with its highly programmable device set-ups and flexibility, and the supported Operating Systems, which require a straight-forward booting and device interface model.

The PPC Boot Firmware includes comprehensive configuration facilities, interactive or auto-boot sequencing from a range of device types, automatic PCI resource allocation at initialisation, PCI display/interrogation utilities and other valuable features for system integrators.

Memory or other speed and feature enhancements are seamlessly absorbed by the Boot firmware, giving the same look and feel to the O/S and the user application as the Radstone hardware models advance. This allows the constant use of latest technology in required areas without system impact. Where particular operating systems define the use of alternate boot methods (e.g. VxWorks bootroms), the Boot firmware technology is absorbed into such boot methodology.

## Built In Test

PPC BIT probes from the lowest level of discrete on-board hardware up to Line Replaceable Unit level within a system, ensuring the highest degree of confidence in system integrity. BIT includes comprehensive configuration facilities, allowing automatic initialisation tests to be defined for the desired mix of system functionality and options. Further tests can be invoked interactively, giving BIT a valuable role as a field service tool. Both object and source code products are available.

## Background Condition Screening

BCS supplements the BIT initialisation test coverage with further health screening that can co-exist with a standard COTS Operating System.

In contrast to a traditional BIT-style test, the intensity and coverage of which makes it destructive to operating systems, the configurable BCS package allows functions such as periodic check-summing, memory scrubbing, and others to be tailored for operation alongside the application in on-line conditions. Results are stored in FLASH in the same format as BIT results. Code is available for reading out BIT/BCS results under LynxOS and VxWorks.



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## Operating System Support

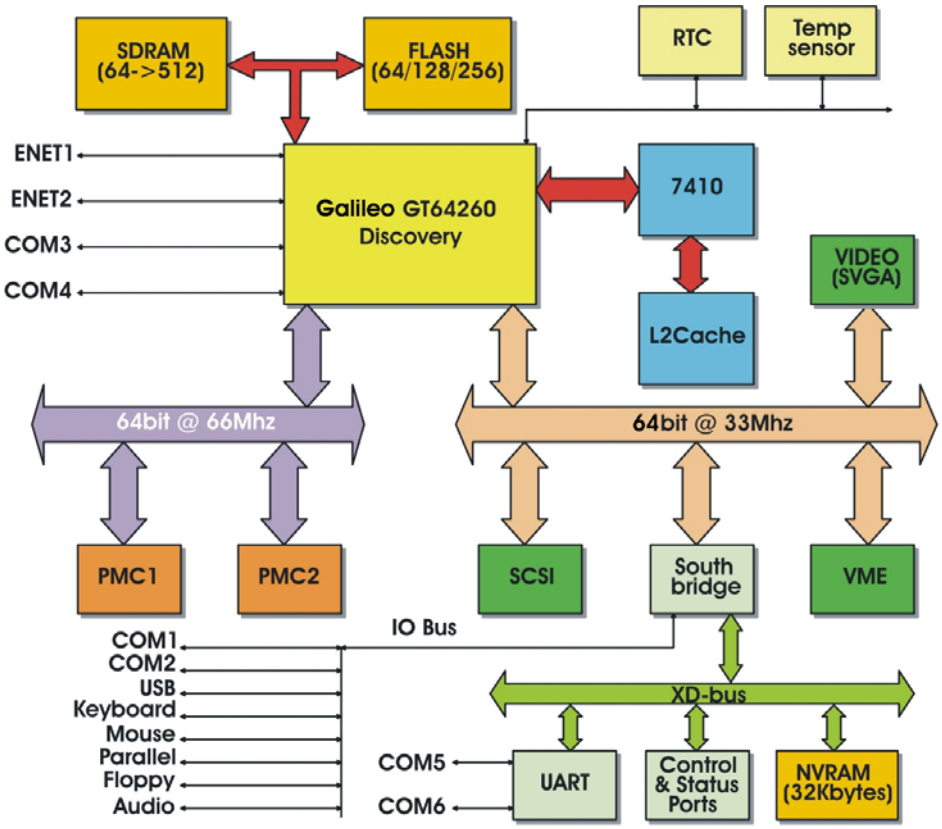
In-house porting expertise for PowerX based boards is focused on key operating systems, including Wind River Systems' Tornado II / VxWorks, and LynxOS from LynuxWorks. Hardware support code is delivered by Radstone, to complement the main operating system code shipped by the O/S vendor.

Other operating system ports (including INTEGRITY from Green Hills Systems), drivers for third party hardware and layered products, are provided through strategic partnerships with dedicated third party vendors, able to offer high quality products and services complementary to the Radstone range. In this way, state of the art development environments and debug tools that are part of the above software products, are made available for use on Radstone's flexible hardware architectures. Please contact Radstone for availability of these offerings.

### BSPs and ESPs

Board Support Packages provide 'standard' support for the above operating systems, as defined by the operating system vendors. Radstone also provide Enhanced Support Packages, for comprehensive hardware support *in addition* to that defined by the operating system vendors. ESP features may be added or removed as desired during development.

**Figure C.4 - PPC7A Block Diagram**




**Notes:**

1. Due to the increasingly short lifetimes of system components, the I/O devices used on the PPC7A are not guaranteed to remain fixed in the future.
2. Hardware should be accessed only through mechanisms provided by the Operating System's "Hardware Independence" mechanism (BSP, HAL, residual data, etc.), and not directly by application software.
3. If a standard operating system is not being used, then it is recommended that applications are written in such a way as to minimize direct access to hardware resources, bearing in mind that changes may be necessary to support future iterations of the hardware.
4. Radstone supported Operating Systems guarantee compatibility at the application level through the Hardware Independence mechanisms mentioned above.



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## Resetting the PPC7A

There are two types of reset that may be applied to the PPC7A: 'Hard' and 'Soft'.

### Hard Reset

This causes the processor to begin executing code from address 0xFFF0 0100 in the System FLASH. By fitting a hardware jumper (E2), the System FLASH addresses may be passed to the VME instead of the FLASH. In this way, the processor can begin executing code from a VME source.

The following table summarizes events that may cause a hard reset:

| Source | | Action | SYSRESET~ Generation |
|---|---|---|---|
| Hardware Events | Power-on | Hard reset all devices | Yes |
| | Received SYSRESET~ | | No |
| | Watchdog time-out | | If System Controller |
| | Front-panel hard reset | | |
| | P0 (where fitted) hard reset signal (pin C1) | | |
| Software Events | SW_LRST bit | Hard reset excluding VMEbus Interface | No |
| | VCSR bit | | |
| | SW_SYSRESET bit | Hard reset if System Controller | If System Controller |

The SW_LRST, VCSR and SW_SYSRESET bits are located in the Universe II PCI-VME bridge.

The front panel hard reset may be disabled under software control or by fitting hardware jumper E14.

**Note:** Integrity of SDRAM data cannot be guaranteed during hard reset, since the memory controller is reset and SDRAM refresh disabled. Similarly, integrity of FLASH or EEPROM data cannot be guaranteed if a hard reset occurs during a FLASH or EEPROM write cycle, respectively.

See the SDRAM section for SDRAM initialization requirements following a hard reset.

### Soft Reset

This causes the processor to reach a recoverable state and then branch to either 0x0000 0100 or 0xFFF0 0100, depending on the state of the IP bit in the processor's Machine State Register.

The following table summarizes events that may cause a soft reset:

| Source | |
|---|---|
| Hardware Events | Front-panel Soft Reset |
| | P0 (where fitted) soft reset signal (pin C2) |
| | P8 (on-board connector) soft reset signal (pin 11) |
| Software Events | HOT_RESET bit in ISA-bridge |

The front panel soft reset switch may be disabled under software control or by fitting hardware jumper E14.

The standard boot firmware does not support the use of soft reset.



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### VMEbus Remote Reset

Another VME master may reset the PPC7A via the Universe II control registers. This causes a hard reset.

### Watchdog Reset

If enabled and triggered (via the Watchdog control register), the watchdog will cause a hard reset unless re-triggered (via the Watchdog Trigger Register) every 1.6 seconds.

## Memory

### System RAM

Between 64 and 1024 Mbytes (using 512 Mbit devices) of system memory is available. The SDRAM is configured as two banks, with the GT64260 directly controlling both. The GT64260 data protection is by two methods:

- Error Correction Coding - capable of detecting all single bit, double bit and nibble errors, and correcting single bit errors
- Parity - aids the detection of errors, but offers no correction

### System FLASH

Up to 8 Mbytes of System FLASH is provided. This holds initialisation and operating system boot routines. The System FLASH is configured as a 32-bit wide device.

### User FLASH

Between 24 and 248 Mbytes of User FLASH may be fitted. The data width is configured as a 32-bit wide device.

### NOVRAM

For maintenance of general system parameters, such as boot options, Ethernet addresses and VME configuration, 32 Kbytes of on-board NOVRAM provides a convenient non-volatile storage area.

### Level 2 or 3 Cache

The PPC7A provides 2 Mbytes of L2 or 4 Mbytes of L3 (with PowerPC 745x) cache, connected to a separate cache bus. By using this private cache bus, the cache traffic does not consume memory bus bandwidth. The amount of cache that can be fitted depends on the CPU that is fitted to the PPC7A, for example the MPC7410 limits the external cache to 24 Mbytes of L2 cache.

On the PowerPC 745x the L3 cache can be used as private memory instead of cache or split between L3 cache and private memory.

### Controller

The Galileo GT64260 device provides an SDRAM memory controller and a FLASH interface.

### Maps

The PPC7A supports programmable memory maps. No memory maps are provided in this manual as no memory locations are fixed in hardware. Please refer to the manuals for the software that is installed on the PPC7A for more information.



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### SDRAM

The following table shows the options available for SDRAM on-board the PPC7A:

| SDRAM SIZE (MBYTES) | BANKS | SDRAM ORGANISATION |
|---|---|---|
| 64 | 1 | 8M x 8 |
| 128 | 2 | 8M x 8 |
| 128 | 1 | 16M x 8 |
| 256 | 2 | 16M x 8 |
| 256 | 1 | 32M x 8 |
| 512 | 2 | 32M x 8 |
| 512 | 2 | 32M x 8 |
| 1024 | 2 | 64M x 8 |

The SDRAM is protected by eight ECC bits per 64 data bits. All single bit, double bit and nibble errors can be detected, and single bit errors can be corrected.

Following a hard reset, the Galileo GT64260 PCI Bridge/Memory Controller must be set up for the size and number of banks of SDRAM and the appropriate number of wait states to match the SDRAM speed. This is done by the standard Boot firmware. The size of the SDRAM may be checked by reading the Memory Configuration register (see the Control and Status Registers section).

At least 100µs must have elapsed from the negation of reset before enabling the SDRAM. After being enabled, the SDRAM must not be accessed until at least 8 refreshes have occurred. If ECC is to be enabled, then it is necessary to initialize the SDRAM to set-up valid ECC bits.

SDRAM access times from the processor, for a 32 byte burst are shown in the table:

| BUS SPEED | CLOCKS ACCESS | DATA TRANSFER RATE |
|---|---|---|
| 100 Mhz (no page hit) | 16:1:1:1 | 168 Mbytes/sec |
| 100 Mhz (pipelined) | 5:1:1:1 | 400 Mbytes/sec |
| 100 Mhz (pipelined & page hit) | 2:1:1:1 | 640 Mbytes/sec |

SDRAM access times from the PCI, referenced to the 33 MHz PCI clock, for a 32-byte burst with no interference from L1, L2 or L3 caches, are shown in the table:

| | CLOCK CYCLES INITIAL ACCESS/SUBSEQUENT | EQUIVALENT TRANSFER RATE (MBYTES/SECOND) |
|---|---|---|
| Burst Read | 2:1:1:1:1:1:1:1 | 118Mbytes/sec |
| Burst Write | 2:1:1:1:1:1:1:1 | 118Mbytes/sec |

### FLASH

The FLASH array is divided into two sections; one bank is termed the BOOT FLASH and the other is referred to as USER FLASH. Both FLASH sections are configured as 32 wide and the GT64260 bus burst is supported to allow for maximum bus bandwidth.



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### Boot FLASH

This section is a total of 8 Mbytes in size. The area is broken down into 4 areas, each area being 2 Mbytes in size: Main BOOT, Alternate BOOT, Recovery BOOT and extended BOOT. All areas can be seen (depending on memory map set-up) at anytime but the areas may be swapped around depending on the boot link configuration and/or FLASH control register set-up.

The FLASH has a write capacity of 100,000 cycles per block (128 Kbyte block size) and the software should write to the FLASH as 32-bits.

**Notes:** Integrity of FLASH data cannot be guaranteed if a hard reset occurs during a FLASH write cycle.

Instead of fitting the link E5 (Overall FLASH Write Enable), the signal (FLASH_WREN~) is available on P0 pin A2 (if fitted) or P2 pin Z1 (if J24 option is not fitted). Pulling this signal low is the same as fitting the link.

### Main BOOT

This area is used as the main default boot area of the PPC7. This area would be the area that the user would put his boot firmware. This area is selected for booting by not fitting E8 (BOOT_ALTERNATE) and E7 (BOOT_RECOVERY) links.

To write to this area, Links E5 (Overall FLASH Write Enable) and E9 (System FLASH Write Protected) need to be fitted. On later board revisions there is an extra register has been added "Software Flash Write Protection (Port 0x86a)" and the WE_BOOT bit needs to be set to enable writes.

### Alternate BOOT

This area would normally contain a backup or alternate boot image. This is useful when developing boot code to be able to switch between two images to check operation. If an alternate boot image is not required, this area can be used to hold User data or for extended boot code. This area is selected for booting from when the link E8 (BOOT_ALTERNATE) is fitted.

To write to this area, Links E5 (Overall FLASH Write Enable) and E9 (System FLASH Write Protected) need to be fitted. On later board revisions there is an extra register has been added "Software Flash Write Protection (Port 0x86a)" and the WE_BOOT bit needs to be set to enable writes.

### Recovery BOOT

This area contains a boot image that is designed to recover the boot areas when the main and alternate boot areas have been made so that the PPC7A will not boot from them. This area is selected for booting from by fitting the link E7 (BOOT_RECOVERY~).

The recovery image is programmed in the factory. As this area is designed to be able to recover the boot code it has been made so that the user can NOT modify this area. There are no link settings that make this area writeable by the user.

The recovery image only uses 1 Mbyte of the 2 Mbytes of space, the 1 Mbytes of space that is left over is an area of FLASH that is NEVER write protected whatever the write protection links are set to.

### Extended BOOT

This area would normally contain data or extended boot code for the boot firmware. If required, a second alternate boot image can be programmed into this area. This boot image is selected by fitting links E8 (BOOT_ALTERNATE) & E7 (BOOT_RECOVERY).

To write to this area, Links E5 (Overall FLASH Write Enable) and E9 (System FLASH Write Protected) need to be fitted. On later board revisions there is an extra register has been added "Software Flash Write Protection (Port 0x86a)" and the WE_BOOT bit needs to be set to enable writes.

### User FLASH

This FLASH array is for the user to place application code or data. It is a contiguous array of 56, 120, or 248 Mbytes (depends on FLASH array size).



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To write to this area, links E5 (Overall FLASH Write Enable) and E3 (WRITE_ENABLE_USER) need to be fitted. On later board revisions there is an extra register has been added "Software Flash Write Protection (Port 0x86a)" and the WE_USER bit needs to be set to enable writes.

## VME Programming Option

Fitting link E4 (see Jumper Settings section) allows the PPC7A to have new boot firmware programmed via the VMEbus.

This link is intended for factory use only. Normally, if the Boot firmware gets corrupted the Recovery boot option should be used to restore the Boot firmware.

This link holds the onboard processor in reset. This is required when the onboard FLASH contents are unknown and new boot firmware is required to be loaded into the FLASH from VME.

To load new firmware from VME, the VME master relies on the reset configuration of the Universe. The register set of the Universe appears at address 0x8000 0000 on VME, by default. The VME master will use these registers to set up windows onto the PCI bus from VME.

The GT64260 will have its register set available at address 0x1400 0000. The PowerPC's boot FLASH can be accessed at address 0xFFF0 0000 on PCI. These areas will need mapping onto VME to allow access of the FLASH memory

For correct operation of the FLASH memory, 0xF428 1278 should be written to the GT64260 registers at offset 0x46C. The FLASH memory can now be read or written to. Writes to the FLASH memory should always be done as a 32 bit write.

The boot area that can be accessed at 0xFFF0 0000 will depend on the Boot link settings (E7 & E8). Also, the write protection of the boot areas is also controlled by the link settings (E5 & E9).

**Note:** The Recovery boot area cannot be written to by configuration of either the Boot links (E7 & E8) or the write protection links (E5 & E9). The Recovery boot area has been designed to only be programmed in the factory.

Once you have programmed the boot section of the FLASH, remove link E4 and carry out a hard reset. Normal booting now occurs from the FLASH and both User and Boot sections are accessible again at their normal addresses.

## JTAG

All of the JTAG chain connections are routed to connector P10 (see the Connectors section for more details).

There are three chains on the PPC7A. One chain is solely for the purpose of programming the CPLD device, which contains various functions, including the main PPC7A ISAbus registers. This device is programmed via JTAG. The second chain is for the CPU to allow debug tools to be used. The third chain is for all the other JTAG devices on the PPC7A, which can include any PMC JTAG devices.

The JTAG signals from P10 connect into the “CPLD” JTAG signals. They have the following terminations:

| | | |
|---|---|---|
| TCK | ⇒ | +3.3V via a 4.7 kΩ pull-up resistor |
| TMS | ⇒ | +3.3V via a 4.7 kΩ pull-up resistor |
| TDI | ⇒ | +3.3V via a 4.7 kΩ pull-down resistor |

The JTAG signals from P8 connect into the “CPU” JTAG signals. They have the following terminations:

| | | |
|---|---|---|
| TCK | ⇒ | +3.3V via a 1 kΩ pull-down resistor |
| TMS | ⇒ | +3.3V via a 10 kΩ pull-up resistor |
| TDI | ⇒ | +3.3V via a 1 kΩ pull-down resistor |
| TRST~ | ⇒ | +3.3V via a 1 kΩ pull-up resistor |



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The JTAG signals from J11 & J12 (PMC site) connect into the "MAIN" JTAG signals on the PPC7A. They have the following terminations:

| | | |
|---|---|---|
| TCK | ⇒ | +5V via a 4.7 kΩ pull-up resistor |
| TMS | ⇒ | +5V via a 4.7 kΩ pull-up resistor |
| TDI | ⇒ | +5V via a 4.7 kΩ pull-up resistor |
| TRST~ | ⇒ | +5V via a 1 kΩ pull-up resistor |

The chain consists of the following in the order listed:

- PMC Slot 2 - linked out if no PMC is fitted
- Universe II (CA91C042)
- GT64260
- L2 or L3 Cache SRAMs (if JTAG devices are fitted, otherwise linked out)

### JTAG Clock Frequencies

Different parts in the JTAG chain may have different maximum TCK frequencies. The main chain on the PPC7A has the following clock limitations:

| | |
|---|---|
| Universe II | ⇒ 20 MHz |
| GT64260 | ⇒ 3 MHz |
| L2 or L3 cache | ⇒ 50 MHz |
| PowerPC 7410/745x | ⇒ 33 MHz |

The JTAG clock should not exceed the maximum clock frequency of the slowest element in the JTAG chain. Using the data from the above components, the chain clock frequency should not exceed 10 MHz.

### JTAG and PMC

The "MAIN" JTAG chain from J11 & J12 visits the other PMC site. These individually auto-bypass if a PMC is not fitted at the site. To achieve this, the PPC7A has BUSMODE2 to BUSMODE4 wired to 1, 0, 0 respectively. This effectively interrogates the PMC site as to whether it has a PCI compliant card fitted. The response from the PMC is returned on BUSMODE1. If the answer is yes (BUSMODE1 = 0), then the PMC site is included in the JTAG chain. If there is no PMC fitted, then a pull-up resistor on the PPC7A forces BUSMODE1 to 1 and the JTAG is bypassed.

**Notes:**

1. The PCI specification (section 2.2.10 on the optional JTAG pins) requires that if a PMC cannot support JTAG, then it must have TDI connected to TDO. This means that the "MAIN" JTAG chain is complete even if there are PMC cards fitted that do *not* support JTAG.
2. The PMC sites cannot *source* the JTAG since, being part of a chain, they are expected to *receive* the JTAG signals.



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## South Bridge Peripheral Components

The South Bridge, connected to the PCIbus, contains a floppy disk controller, 16-bit digital IO, two serial ports, a parallel port and a keyboard/mouse controller.

### Floppy Disk Controller

Connection to the FDC is through P2. This interface is only available with the digital IO build option and requires software to direct the FDC to the interface pins. The pinout is given in the Connectors section. The FDC is software compatible with the DP8473, 765A and NS82077.

### Serial I/O

The Ultra I/O provides two serial channels (COM1 and COM2) containing FIFOs, software compatible with the INS8250N-B, PC16550A and PC16450. The baud rates are programmable from 50 baud up to 115.2 kbaud, including the MIDI data rate.

Connection to the serial ports is primarily through the P2 connector, although access may be obtained through front panel connectors (depending on options fitted). See the Connectors section for pinouts.

### Parallel I/O

The parallel port includes extended capabilities conforming to IEEE P1284. Connection to the parallel port is through the P2 connector. This interface is only available on the Parallel port build option. The pinout is given in the Connectors section.

### Keyboard and Mouse Controller

A PS/2 compatible Keyboard and Mouse interface with Phoenix BIOS is integrated into the Ultra I/O. Connections to the mouse and keyboard are through the P2 connector. This interface is not available if the USB build option is fitted. See the Connectors section for pinouts.

## Watchdog Timers

The PPC7A contains a Maxim 706 microprocessor supervisory circuit with a watchdog timer. Once enabled, this timer must be re-triggered every 1.6 seconds or a hard reset results. The trigger control registers is 0x82C and is enabled via Control register 0x828.

**Note:** Once this bit is enabled as an output, software needs to write to the trigger register to keep the board from resetting. Disabling this pin once it has been enabled does not disable the Watchdog.

The GT64260 also contains a watchdog timer. This timer has a programmable timeout interval. The watchdog output pin needs to be enabled in the GT64260 as MPP bit 9 before the watchdog can reset the PPC7A.

## Coms 5 & 6

The PPC7A has a Exar ST16C2550 dual UART (software compatible with INS8250 & NS16C550). Each UART channel has 16-Byte transmit and receive FIFO's. The CLK input to this device is 12MHz. Due to pin-out restrictions only RX, TX, CTS & RTS signals are supported on each channel. The interface standard is fixed by a factory build option at either RS232 or RS422.



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## Front Panel Switches and Indicators

This section describes the features found on the PPC7A front panel.

### Air-cooled Versions

#### PMC Slots

There are two PMC slots in the front panel. However, if you have not ordered PMCs for the sites then Radstone will fit a blanking plate in the slot(s) for EMC protection.

If you are fitting a non-Radstone PMC, it must comply with the standard for rugged, conduction-cooled PMCs to ensure that it mates correctly with the PPC7A mechanics. This will be the case for Radstone PMCs.

If you are fitting a PMC yourself, before fitting the module, remove the corresponding blanking plate from the desired PMC slot. The PMC's bezel will fill the slot and will usually provide connection to the module. PMCs are delivered with a full kit of parts for mounting them, and the manual for the module normally contains instructions on how to fit the module.

#### LEDs

Three software programmable LEDs (DS1 to DS3) are mounted on the front panel. DS1 is yellow, DS2 is red and DS3 is green. See the Software Programmable LEDs section below for more details.

#### Switches

A momentary action toggle switch is fitted to allow generation of a hard reset or abort. With the board in the orientation as shown in the Figure below, moving the switch to the left causes an abort, and moving the switch to the right causes a hard reset.

### Conduction-cooled Versions

#### PMC Slots

There are two conduction-cooled PMC slots in the front panel, allowing limited access to PCI signals. If you are fitting a non-Radstone PMC, it must comply with the standard for rugged, conduction-cooled PMCs to ensure that it mates correctly with the PPC4 mechanics. This will be the case for Radstone PMCs.

#### LEDs

Three software programmable LEDs (DS1 to DS3) are mounted on the front panel. DS1 is yellow, DS2 is red and DS3 is green. See the Software Programmable LEDs section below for more details.

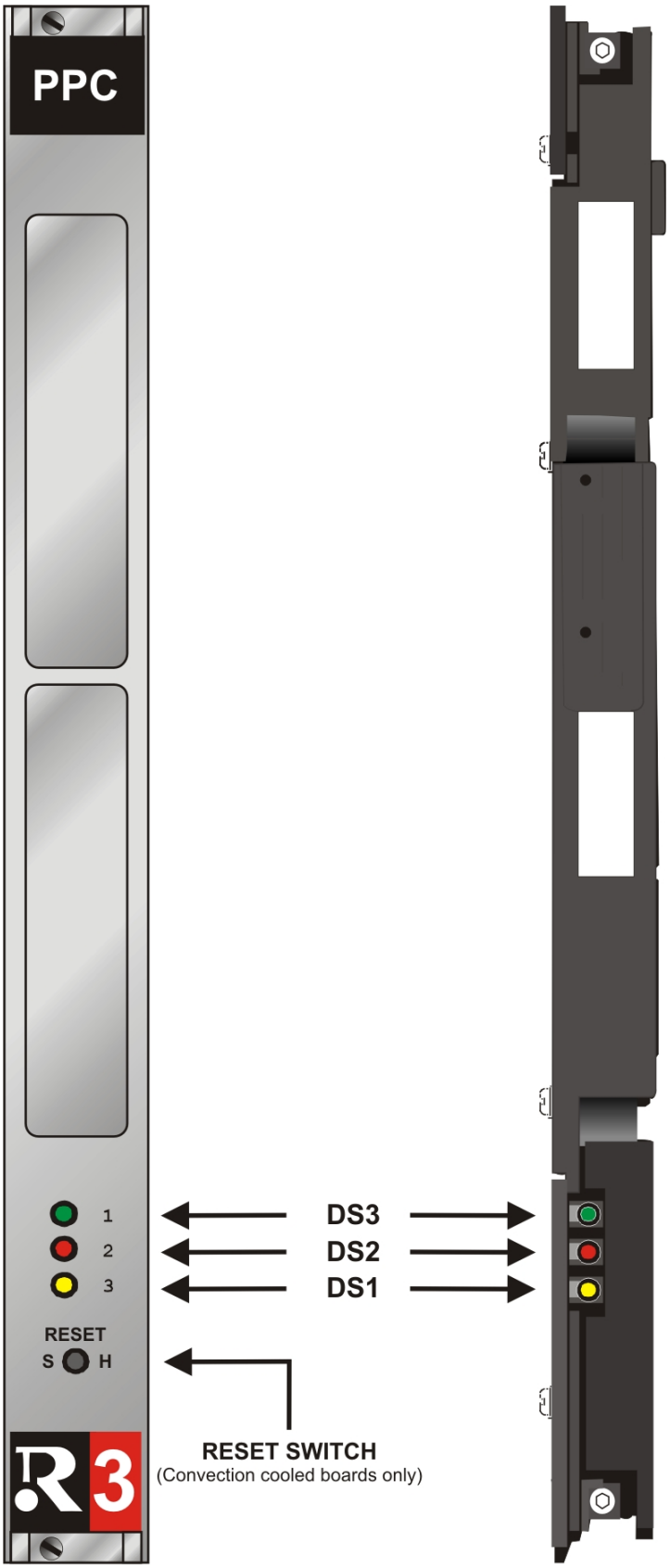
#### Switches

There are no switches on the conduction-cooled front panel.



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**Figure C.5 - PPC7A Front Panel**






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## Software Programmable LEDs

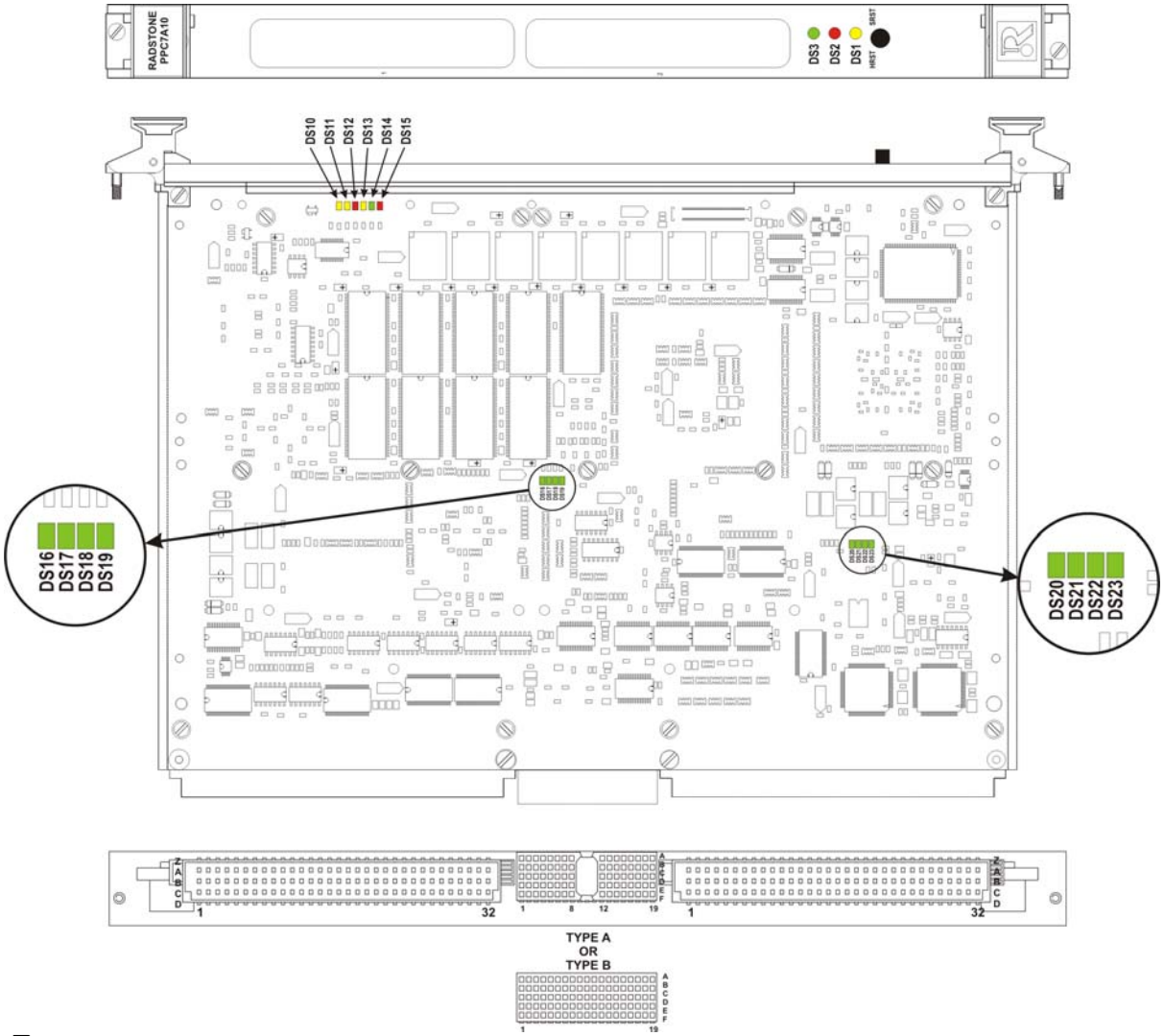
The PPC7A has the following software programmable LEDs:

Control register 0x820 provides four signals, which are connected to four of the LEDs. There is a separate control bit for each LED. Three are visible in the front panel (DS1/2/3) with five on the back of the board as DS10, DS11, DS12, DS13 and DS14.

The other 8 LEDs are all surface mounted on the back of the PCB.

DS16, DS17, DS18, and DS19 are Ethernet status LEDs for channel 1, and DS20, DS21, DS22, and DS23 are for channel 2. The default functions of these LEDs are link, TX activity, RX activity status, and 100BaseT respectively, but the software may override these.

**Figure C.6 – Position of LEDs (Back of the Board)**




Note: DS15 indicates all board power supplies are healthy. The board is held in Reset if any supply is outside specification.



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## Control and Status Registers

| ISA I/O Port (Hex) | Description | Row A |
|---|---|---|
| 0000 to 000F | South Bridge DMA 1 Control | |
| 0020 and 0021 | South Bridge Interrupt 1 Control | |
| 0040 to 0043 | South Bridge Counter Control | |
| 0060 | Keyboard | |
| 0061 | South Bridge NMI Status and Control | |
| 0064 | Keyboard | |
| 0071 and 0072 | RTC | R/W |
| 0078 to 007B | South Bridge BIOS Timer | |
| 0080 to 0090 | South Bridge DMA Pages | |
| 00A0 and 00A1 | South Bridge Interrupt 2 Control | |
| 00C0 to 00DE | South Bridge DMA 2 Control | |
| 02E8 to 02EF | COM6 | R/W |
| 02F8 to 02FF | South Bridge COM2 | R/W |
| 03E8 to 03EF | COM5 | R/W |
| 03F8 to 03FF | South Bridge COM1 | R/W |
| 040A | South Bridge DMA Scatter/Gather | RO |
| 040B | DMA 1 Extended Mode | WO |
| 0410 to 043F | South Bridge DMA Scatter/Gather | |
| 0481 to 048B | South Bridge DMA High Pages | |
| 04D0 and 04D1 | South Bridge Edge/Level Control | |
| 04D6 | DMA 2 Extended Mode | WO |
| 0804 | Memory Configuration | RO |
| 0806 | Memory Configuration Extend | RO |
| 0808 | SCSI Activity LED | R/W |
| 080C | Equipment Present 1 | RO |
| 080E | Equipment Present 2 | RO |
| 0810 | Equipment Present 3 | RO |
| 0818 | Key Lock | RO |
| 0820 | LEDS | R/W |
| 0824 | COMs | R/W |
| 0826 | RTS | R/W |
| 0828 | Reset | R/W |
| 082C | Watchdog Trig | R/W |
| 0854 | Board Revision | RO |
| 0858 | Extended ID | RO |
| 0864 | ID Link | RO |
| 0866 | Motherboard Type | RO |
| 0868 | FLASH Write control | RO |
| 086A | Software FLASH Write control | R/W |
| 086E | FLASH Control | R/W |

Where: R/W = Read/Write RO = Read Only WO = Write Only

The control and status registers exist on the PPC7A for controlling or reading the status of the hardware. The addresses are as seen by the processor.

Certain registers are described in detail in the following pages. The others are registers in the ISA Bridge or other major devices, which are described in the detail in the appropriate device data sheet (which will also give the appropriate ‘Type’ column entry).



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In the following register descriptions, the bit significance is shown in big-endian mode (i.e. from the viewpoint of the PowerPC 750 programmer).

### Memory Configuration Register (Port 0x0804)

This register provides information on the SDRAM fitted.

MSB = D0, LSB = D7

D0: Memory type

1 = SDRAM

D1: NVRAM type

0 = FRAM

1 = NVSRAM

D2 to D4: Reserved always read as '0'

D5: Reserved always read as '0'

D6: SDRAM Bank 1 Fitted

0 = Fitted
1 = Not fitted

D7: SDRAM Bank 0 Fitted, always read as '0'

### Memory Configuration Extend Register (Port 0x0806)

This register provides size information for the SDRAM and FLASH memory banks.

MSB = D0, LSB = D7

D0 and D1: SDRAM Bank size

0 = 64 Mbytes
1 = 128 Mbytes
2 = 256 Mbytes
3 = 512 Mbytes

D2 to D4: Reserved

D5 to D7: FLASH banks and size configuration

| D5 | D6 | D7 | Device Size | No. Of Banks | Mbytes |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 256 M bit | 1 | 128 |
| 0 | 0 | 1 | 128 M bit | 1 | 64 |
| 0 | 1 | 0 | Reserved | 1 | Reserved |
| 0 | 1 | 1 | 64 M bit | 1 | 32 |
| 1 | 0 | 0 | 256 M bit | 2 | 256 |
| 1 | 0 | 1 | 128 M bit | 2 | 128 |
| 1 | 1 | 0 | Reserved | 2 | Reserved |
| 1 | 1 | 1 | 64 M bit | 2 | 64 |



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### SCSI Activity LED Register (Port 0x0808)

This register allows control of the SCSI activity LED (DS11).

MSB = D0, LSB = D7

D0 to D6: Reserved.

D7: SCSI activity LED

0 = LED off
1 = LED on

### Equipment Present Register 1 (Port 0x080C)

This register provides information on hardware options and the state of the SCSI Terminator power fuse.

MSB = D0, LSB = D7

D0: Hardware ID0 (see the Motherboard Type Register for details)

D1: SCSI_FUSE_GOOD

0 = SCSI fuse bad
1 = SCSI fuse good

**Note:** This is a re-settable fuse that re-engages when the overcurrent condition is removed.

D2: PRSNT1_2~

0 = Slot 2 PMC present
1 = Slot 2 empty

D3: PRSNT1_1~

0 = Slot 1 PMC present
1 = Slot 1 empty

D4: PCI1 bus speed

0 = 33 Mhz
1 = 66 Mhz

D5 and D6: Cache Size

| D5 (SIZE1) | D6 (SIZE0) | SIZE (MBYTES) |
|---|---|---|
| 0 | 0 | 4 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | None |

D7: Reserved, always reads ‘0’



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### Equipment Present Register 2 (Port 0x080E)

This register provides information on hardware options fitted to the PPC7A.

MSB = D0, LSB = D7

D0: Universe II Fitted

0 = Not fitted
1 = Fitted

D1: Reserved, always reads '0'

D2: COMs 3 to 6 Fitted

0 = Not fitted
1 = Fitted

D3: USB Fitted

0 = Not fitted
1 = Fitted

D4: LPT Fitted

0 = Not fitted
1 = Fitted

D5 and D6: Cache Speed

| D5 | D6 | Speed (MHz) |
|---|---|---|
| 0 | 0 | Reserved |
| 0 | 1 | Reserved |
| 1 | 0 | 200 |
| 1 | 1 | 166 |

D7: Cache Type

1 = Double data rate
0 = Standard data rate



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### Equipment Present Register 3 (Port 0x0810)

This register provides information on hardware options fitted to the PPC7A.

MSB = D0, LSB = D7

D0 to D3: Reserved. Always reads '0'

D4: PMC IO voltage

0 = 5 Volt
1 = 3.3 Volt

D5: 3.3Volt PMC power

0 = Powered by onboard power supply
1 = Power from taken from 3.3V pins on VME connectors

D6 and D7: SCSI clock speed

| D6 | D7 | SPEED (MHZ) |
|---|---|---|
| 0 | 0 | Reserved |
| 0 | 1 | 40 |
| 1 | 0 | 80 |
| 1 | 1 | Reserved |

### Key Lock Register (Port 0x0818)

This register provides information on the state of the keylock signal. See the Keylock section for more details.

MSB = D0, LSB = D7

D0 to D6: Reserved

D7: Keylock

0 = Keylock signal low
1 = Keylock signal high



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### LED Register (Port 0x0820)

This register provides control for the 4 user LEDs fitted to the PPC7A.

MSB = D0, LSB = D7

D0: SCSI_TERM_REQ

0 = SCSI terminator not required (SCSI link not fitted)
1 = SCSI terminator required (SCSI link fitted)

D1: SCSI_TERM_EN

0 = Disable SCSI terminator
1 = Enable SCSI terminator

D2 and D3: Selects the NVRAM page (each page is 8Kbytes)

D4: DS10, yellow

0 = LED off, OFFLINE~ High
1 = LED on, OFFLINE~ Low

D5: DS13 and DS1, Yellow

0 = LED on, SYSFAIL~ Low
1 = LED off, SYSFAIL~ High

D6: DS12 and DS2, Red and S+YSFAIL~ (P0 B1) signal

0 = LED off
1 = LED on

D7: DS14 and DS3, Green and SYSFAIL~ (P0 B2) signal

0 = LED off
1 = LED on

See the Software Programmable LEDs section below for the location of these LEDs.



**Note:** DS12 and DS2 are on by default after power-up.
The on-board SCSI terminator can be enabled by the SCSI link (E13), or by setting SCSI_TERM_EN to 1.



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### COMs Register (Port 0x0824)

This register provides control for COMs 3 & 4, for the Clocks and interface configuration.

MSB = D0, LSB = D7

D0: COM3_CLK_EN, this bit enables the TSCLK3 signal out on to COM3_TT (transmit clock)

0 = Disabled
1 = Enabled

D1: TSCLK3_EN, when enabled COM3_RT (receive transmit clock) is linked to TSCLK3 is

0 = Disabled
1 = Enabled

D2: COM3_RS232, selects which interface is used for COM3

0 = RS232
1 = RS422

D3: COM3_TX_EN, when enabled allows all of the COM3 interface buffers.

0 = Disabled
1 = Enabled

D4: COM4_CLK_EN, this bit enables the TSCLK4 signal out on to COM4_TT (transmit clock)

0 = Disabled
1 = Enabled

D5: TSCLK4_EN, when enabled COM4_RT (receive transmit clock) is linked to TSCLK4 is

0 = Disabled
1 = Enabled

D6: COM4_RS232, selects which interface is used for COM4

0 = RS232
1 = RS422

D7: COM4_TX_EN, when enabled allows all of the COM4 interface buffers.

0 = Disabled
1 = Enabled



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### RTS Register (Port 0x0826)

This register provides options for when the COMs channel data transmitters are enabled. This selection logic only works in RS422 interface mode.

MSB = D0, LSB = D7

D0 & D1: Reserved always reads '0'

D2 and D3: COM3 transmitter function select

| D3 | D2 | Transmit Function Selected |
|---|---|---|
| 0 | 0 | Not enabled |
| 0 | 1 | Enabled |
| 1 | 0 | Enabled by RTS3 |
| 1 | 1 | Enabled by RTS3 & stretched |

D4 & D5: Reserved always reads '0'

D6 and D7: COM4 transmitter function select

| D7 | D6 | Transmit Function Selected |
|---|---|---|
| 0 | 0 | Not enabled |
| 0 | 1 | Enabled |
| 1 | 0 | Enabled by RTS4 |
| 1 | 1 | Enabled by RTS4 & stretched |

### Watchdog Register (Port 0x0828)

This register controls the watchdog resets features of the PPC7A.

MSB = D0, LSB = D7

D0: Last reset was a watchdog

0 = Normal reset
1 = Last board reset was caused by a watchdog timeout

D1: Enable NMI from GT-64260

0 = Disabled
1 = NMI can be generated from GT-64260 CPUINT output pin

D2 to D5: Reserved – Reads '0'

D6: Watchdog enable

0 = Trig output disabled
1 = Trig output enabled

Once the trig output is enabled the Watchdog trig register (0x082C) needs to be accessed every 1.5 seconds, or a hard reset of the entire PPC7A occurs.

D7: RESET_SW_EN (output)

0 = Disable the front panel reset switch logic.
1 = Enable the front panel reset switch logic.

**Note:** This bit has no effect if the switch logic is not present or if link E14 is fitted.



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### Watchdog Trig (Port 0x082C)

This is a dummy register that is written to trigger the watchdog.

MSB = D0, LSB = D7

D0 to D7: Don't care for writes, undefined for reads

**Note:** Data written is not used and Reads don't trigger the watchdog.

### Board Revision Register (Port 0x0854)

This register provides information on the build state of the PPC7A.

MSB = D0, LSB = D7

D0 to D2: Number revision of hardware build state

1 = Revision 1
2 = Revision 2
3 = Revision 3
All other values are Reserved.

D3 to D7: Letter revision of hardware build state

0x0 = Revision A
0x1 = Revision B
...
0x18 = Revision Y
0x19 = Revision YA
...
0x1F = Revision YG

### Extended ID Register (Port 0x0858)

This register provides Board hardware type.

MSB = D0, LSB = D7

D0 to D7: Board ID register

0x0E = PPC7A - 7410/755
0x0F = PPC7A – 745x
0x10 = PPC7FW (MPC7410 with Firewire)

All other patterns mean the board is not a PPC7A



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### ID Link Register (Port 0x0864)

This register allows you to read the Board ID links (E2, E10, E11 and E12) or the VME Geographical address pins.

MSB = D0, LSB = D7

D0: Reserved

D1: Reserved

D2: Reserved

D3: GA4 (VME64 Geographical Address bit 4)

D4: E10/GA3

0 = Link fitted
1 = Link not fitted

D5: E12/GA2

0 = Link fitted
1 = Link not fitted

D6: E2/GA1

0 = Link fitted
1 = Link not fitted Reserved

D7: E11/GA0

0 = Link fitted
1 = Link not fitted

**Note:** Bits D0, D1, D2 and D3 are also connected to the VME64 Geographical Address bits GA0, GA1, GA2 and GA3 respectively. Do not fit the links if you wish to read the status of the Geographical Address bits, as the links connect these bits to 0 Volts.



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### Motherboard Type Register (Port 0x0866)

This register provides information on the type of motherboard and SDRAM ECC operation. The bits used in this register are compatible with the other members of the current Radstone PPC product range.

MSB = D0, LSB = D7

D0: HW_ECC ENABLE

0 = Non-ECC
1 = ECC enabled

D1: PLL2 (see table below)

D2: ECC_TYPE

0 = Reserved
1 = ECC

D3: ECC

0 = ECC not fitted
1 = ECC fitted

D4: PLL1 (see table below)

D5: PLL0 (see table below)

| PLL2 | PLL1 | PLL0 | BUS SPEED (MHZ) |
|---|---|---|---|
| 1 | 1 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 0 | 1 | Reserved |
| 1 | 0 | 0 | 133 |
| 0 | 1 | 1 | Reserved |
| 0 | 1 | 0 | 100 |
| 0 | 0 | 1 | 66 |
| 0 | 0 | 0 | Reserved |

D6 and D7: Hardware ID2 and ID1 respectively. Used with Hardware ID0 (bit 0 of Equipment Present Register 1) to define the hardware type as follows:

| ID2 TO ID0 | HARDWARE TYPE |
|---|---|
| 111 | PPC1/PPC3 |
| 110 | PPC2 |
| 101 | PPC1A |
| 100 | PPC2A |
| 011 | PPC4 |
| 010 | PPC4A |
| 000 | Use Extended ID |



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### FLASH Write Protection (Port 0x0868)

This register provides information on the FLASH write protection.

MSB = D0, LSB = D7

D0: FLASH write enable link

0 = link not fitted
1 = link fitted

D1: Status of the P2 or P0 FLASH_WREN~ signal

0 = Signal not active (Pin high)
1 = Signal active (Pin low)

D2: FLASH BOOT write enable link

0 = link not fitted
1 = link fitted

D3: FLASH USER write enable link

0 = link not fitted
1 = link fitted

D4: Always reads '0'

D5: Writes to FLASH recovery section

0 = Disabled
1 = Enabled

D6: Writes to FLASH BOOT section

0 = Disabled
1 = Enabled

D7: Writes to FLASH USER section

0 = Disabled
1 = Enabled

### Software FLASH Write Protection (Port 0x086a)

This register provides information on the FLASH write protection.

MSB = D0, LSB = D7

D0 to D5: Reserved reads '0'

0 = link not fitted
1 = link fitted

D6: WE_BOOT write enable software bit

0 = writes disabled
1 = writes enabled

D7: WE_USER write enable software bit

0 = writes disabled
1 = writes enabled

**Note:** This register is only present on boards with hardware letter revision later than C (see Board Revision Register Port 0x854).



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### FLASH Control Register (Port 0x086E)

This register provides status and control signals for the Boot sections of the FLASH devices.

When the PPC7A is reset, this register is reset to reflect the status of the BOOT links (E8, E4 & E7), after boot software can then override these link settings by writing to bits D5 & D7 in this register.

Status signals BOOT_ALTERNATE, BOOT_FROM_VME & BOOT_RECOVERY show the real link settings. Signals SELECT_ALTERNATE & SELECT_RECOVERY show what image is really selected.

MSB = D0, LSB = D7

D0: NVRAM Write Protect

0 = NVRAM is write protected
1 = Writes to NVRAM are enabled

D1: BOOT_ALTERNATE (reflects the status of user link E8). This bit is read-only.

0 = Link not fitted
1 = Link fitted

D2: VME_BOOT_MODE (reflects the status of user link E4). This bit is read-only.

0 = Link not fitted
1 = Link fitted

D3: BOOT_RECOVERY (reflects the status of user link E7). This bit is read-only.

0 = Link not fitted
1 = Link fitted

D4: Reserved reads '0'

D5: SELECT_ALTERNATE

D6: FLASH_CONTROL_WRITTEN

0 = Register not written
1 = Register written

D7: SELECT_RECOVERY

| SELECT_ALTERNATE | SELECT_RECOVERY | AREA SELECTED |
|---|---|---|
| 0 | 0 | Main |
| 0 | 1 | Recovery |
| 1 | 0 | Alternate |
| 1 | 1 | Extended |



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## Control and Status Registers on CS0

These registers are accessed via the GT64260 CS0 address window (see GT64260 for more information for setting up this address window).

| CS0 I/O Port (Hex) | Description | Type |
|---|---|---|
| 0000 | Board ID | RO |
| 0002 | Last Reset source | RO |
| 0003 | Reset register | R/W |
| 0004 to 0007 | Board ID string | RO |

Where: R/W = Read/Write RO = Read Only

### Board ID (Port 0x0)

This register provides Board hardware type.

MSB = D0, LSB = D7

D0 to D7: Board ID register

0x0E = PPC7A - 7410/755
0x0F = PPC7A – 745x
0x10 = PPC7FW (MPC7410 with Firewire)

All others patterns mean the board is not a PPC7A

### Last Reset Source (Port 0x2)

This register provides information about what caused the last reset.

MSB = D0, LSB = D7

D0 to D2: Reserved

D3: GT64260 watchdog timed out

0 = Did not cause the last reset
1 = Caused the last reset

D4: MAX706 Watchdog Timed out

0 = Did not cause the last reset
1 = Caused the last reset

D5: Reset switch

0 = Did not cause the last reset
1 = Caused the last reset

D6: Universe

0 = Did not cause the last reset
1 = Caused the last reset

D7: RiscWatch connector reset driven

0 = Did not cause the last reset
1 = Caused the last reset



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### Reset Register (Port 0x3)

This register provides a 4bit register that is not cleared or changed on any reset apart from a power up when it is cleared to '0'.

MSB = D0, LSB = D7

D0 to D3: Reserved Reads '0'

D4 to D7: 4 bit register

### Board ID String (Port 0x4 to 0x7)

This register provides a board ID string, which shows 'PPC7A' when read as a 32 bit value.

### Port 0x4

MSB = D0, LSB = D7

D0 to D7: Reads 0x50 ('P')

### Port 0x5

MSB = D0, LSB = D7

D0 to D7: Reads 0x50 ('P')

### Port 0x6

MSB = D0, LSB = D7

D0 to D7: Reads 0x43 ('C')

### Port 0x7

MSB = D0, LSB = D7

D0 to D7: Reads 0x37 ('7')

## Status Registers on CS1

These registers are accessed via the GT64260 CS1 address window (see GT64260 for more information for setting up this address window).

| CS0 I/O Port (Hex) | Description | Type |
|---|---|---|
| 0000 to 0003 | Checker board 1 | RO |
| 0004 to 0007 | Checker board 2 | RO |

Where: RO = Read Only

### Checker Board 1 (Port 0x0 to 0x3)

This register provides a checker board value of 0x5555 5555 when read as a 32 bit value.

### Checker Board 2 (Port 0x4 to 0x7)

This register provides a checker board value of 0xAAAA AAAA when read as a 32 bit value.



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## Interrupts and Error Reporting

The following table shows the various external interrupt sources to the processor and their relative priorities. It also shows whether the previous state of the processor is recoverable.

| PRIORITY | INTERRUPT | CAUSE | RECOVERABILITY |
|---|---|---|---|
| 0 | System Reset | Power on,<br>Hard reset | Non-recoverable |
| 1 | Machine Check | Address or Data Parity error,<br>Machine Check Input (MCP~),<br>Non-maskable Interrupt (NMI~) | Non-recoverable in most cases |
| 2 | System Reset | Soft reset | Recoverable unless Machine Check occurs |
| 3 | System Management Interrupt | SMI~ input | Recoverable unless Machine Check or System Reset occurs |
| 4 | External Interrupt | INT~ input | Recoverable unless Machine Check or System Reset occurs |

### System Resets

See the Resetting the PPC7A in this section.

### Machine Check Exception

The South Bridge can be configured the signal NMI on certain conditions. The hardware on the PPC7A routes this signal to the CPU as the MCP~ (Machine Check) interrupt.

The South Bridge can drive this signal due to the following conditions:

- PCI bus error
- PCI SERR~ signal driven active

The PCI SERR~ signal can be driven low by other PCI devices to report a error condition.

The processor may be configured to take a machine check exception or enter the checkstop state.

### System Management Interrupt (SMI~)

The System Management Interrupt pin of the CPU is connected to the GT64260. This allows the GT64260 to interrupt the processor for events such as an SDRAM parity error.

To allow the GT64260 to provide a SMI~ interrupt to the CPU the output pin MPP[8] needs to be set to Int[0]* (see GT64260 register MPP Control1 - offset - 0xF004). The events that can cause this interrupt to be driven is by register CPU Int[0]* (0xE60).



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### External Interrupt (INT~)

The processor external interrupt pin (INT~) is asserted for a pending interrupt from the interrupt controller in the South Bridge.

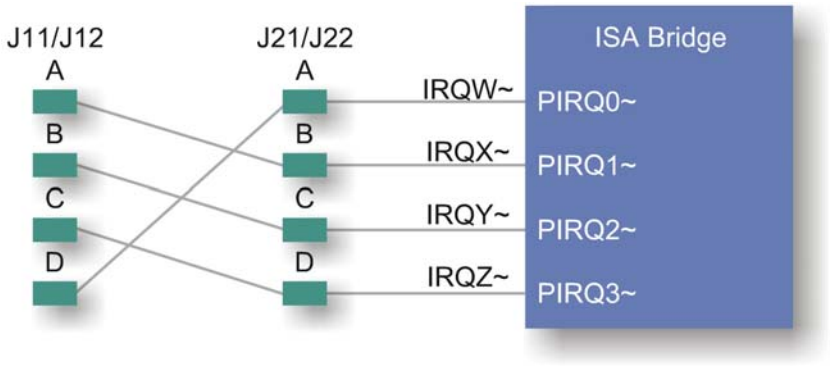
Interrupt priorities and modes are assigned as the firmware running on the PPC7A.

### PCI Interrupts

There are 4 interrupt lines for the PMC expansion slots on the motherboard and the PMC carrier. These are connected to the PIRQ~ inputs of the interrupt controller. The PIRQ~ inputs may be routed to any IRQ that is set to level sensitive mode.

The interrupt routing follows the recommendations in the PCI specification and the PCI system design guide with a “rotation” between each slot.

The interrupt lines for the two on-board PMC slots are routed as shown below:




Two single function PMCs (which always use INTA~) are able to use unique IRQs with appropriate programming of the interrupt controller.

## Keylock

The keylock input signal allows the software to interrogate an external keyswitch. For example, the boot firmware could request a password if the keyswitch is in the locked position and a password is set up in the NVRAM.

The keylock signal defaults to high if no external connection is made.



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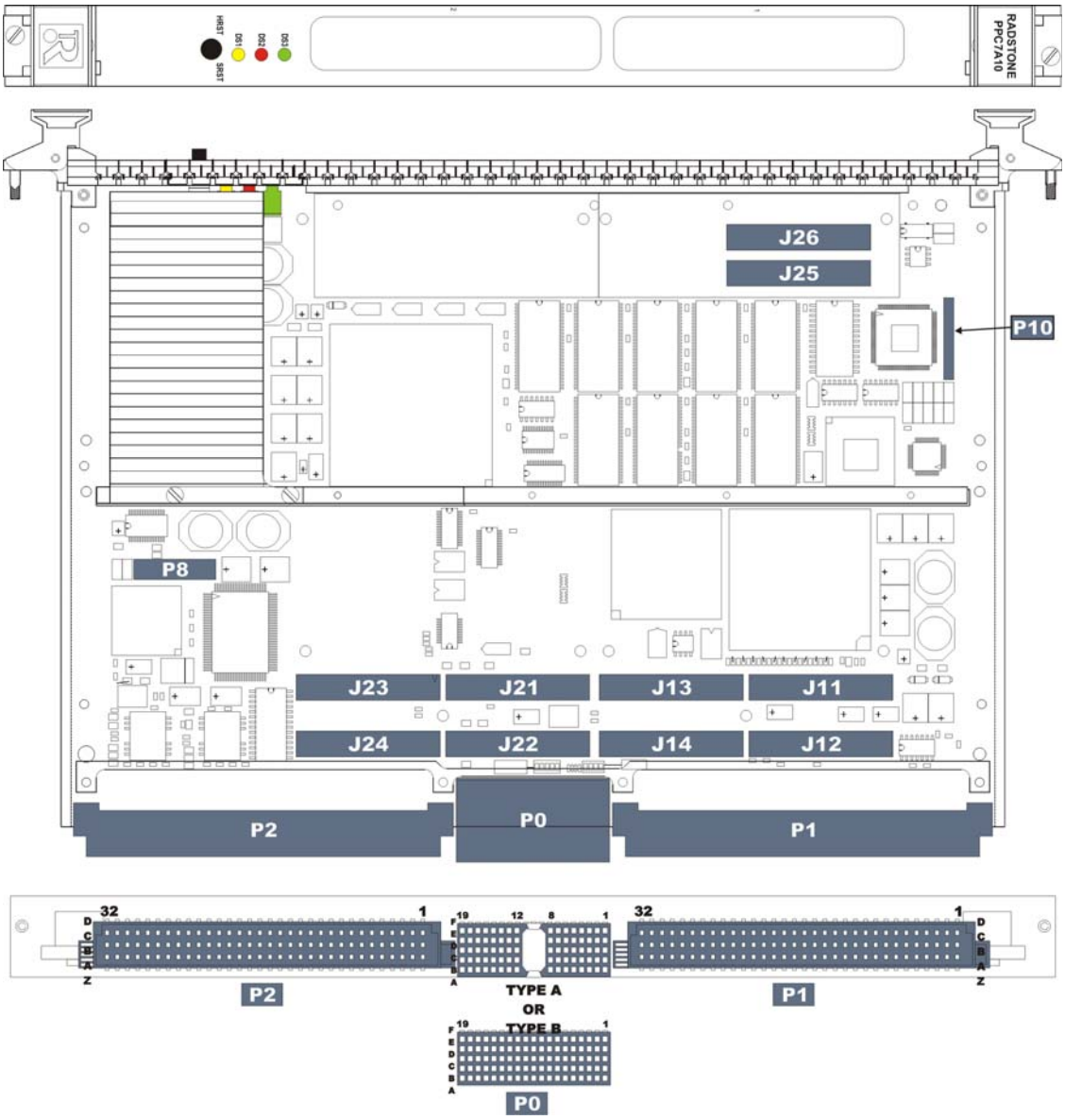
# Connectors

This section gives the pinouts and signal descriptions for the connectors on the PPC7A.

The following table shows the function of the connectors on the PPC7A:

| Connector | Function |
|---|---|
| P1 | VMEbus |
| P2 | VMEbus/Rear I/O |
| P0 | PMC site 1 I/O |
| J11, J12, J14 | PMC (site 1) |
| J21, J22, J24 | PMC (site 2) |
| J25, J26 | I/O expansion |
| P8 | RISCWatch |
| P10 | JTAG (Factory use) |

**Figure C.7 - Connector Positions**






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## Backplane Connectors

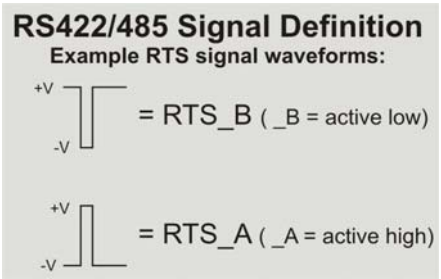
### P1 (VMEbus) Pin Assignments

The PPC7A P1 connector conforms to the VME64x standard. For pin assignments and signal descriptions, refer to the Standard Interfaces section.

### P2 Pin Assignments (Standard Pinout)

The following P2 pinout is correct if the J24 connector is not fitted.

| Pin No. | Row Z | Row A | Row B | Row C | Row D |
|---|---|---|---|---|---|
| 1 | FLASH_WREN~ | DB0~ (SCSI) | +5V | RX0+ | COM3_TXD_A |
| 2 | GND | DB1~ (SCSI) | GND | RX0- | COM3_TXD_B |
| 3 | EXT_RESET~ | DB2~ (SCSI) | Reserved | TX0+ | COM3_RXD_A |
| 4 | GND | DB3~ (SCSI) | A24 | TX0- | COM3_RXD_B |
| 5 | EXT_ABORT~ | DB4~ (SCSI) | A25 | RX1+ | COM3_RTS_A |
| 6 | GND | DB5~ (SCSI) | A26 | RX1- | COM3_RTS_B |
| 7 | N/C | DB6~ (SCSI) | A27 | VSYNC | COM3_CTS_A |
| 8 | GND | DB7~ (SCSI) | A28 | GPIO0 | COM3_CTS_B |
| 9 | COM4_TXD_A | DBP0~ (SCSI) | A29 | GPIO1 | COM5_TXD |
| 10 | GND | ATN~ (SCSI) | A30 | GPIO2 | COM5_RTS |
| 11 | COM4_TXD_B | BSY~ (SCSI) | A31 | GPIO3 | COM6_TXD |
| 12 | GND | ACK~ (SCSI) | GND | GPIO4 | COM6_RTS |
| 13 | COM4_RXD_A | RST~ (SCSI) | +5V | GPIO5 | COM5_RXD |
| 14 | GND | MSG~ (SCSI) | D16 | GPIO6 | COM5_CTS |
| 15 | COM4_RXD_B | SEL~ (SCSI) | D17 | GPIO7 | COM3_TT_A |
| 16 | GND | C/D (SCSI) | D18 | GPIO8 | COM3_TT_B |
| 17 | COM4_CTS_A | REQ~ (SCSI) | D19 | GPIO9 | COM3_ST_A |
| 18 | GND | I/O (SCSI) | D20 | GPIO10 | COM3_ST_B |
| 19 | COM4_CTS_B | TERMPWR (SCSI) | D21 | GPIO11 | COM3_RT_A |
| 20 | GND | USBP0/MOUSE_CLK | D22 | GPIO12 | COM3_RT_B |
| 21 | N/C | USBP0~/MOUSE_DATA | D23 | GPIO13 | COM4_RTS_A |
| 22 | GND | KBD_5V | GND | GPIO14 | COM4_RTS_B |
| 23 | N/C | USBP1/KBD_CLK | D24 | GPIO16 | COM6_RXD |
| 24 | GND | USBP1~/KBD_DATA | D25 | GPIO17 | COM6_CTS |
| 25 | COM4_ST_A | COM2_TXD | D26 | SPEAKER_OUT | N/C |
| 26 | GND | COM2_RXD | D27 | KEYLOCK_IN | N/C |
| 27 | COM4_ST_B | COM2_RTS | D28 | COM1_TXD | COM4_TT_A |
| 28 | GND | HSYNC | D29 | COM1_RXD | COM4_TT_B |
| 29 | COM4_RT_A | COM2_CTS | D30 | COM1_RTS | N/C |
| 30 | GND | RED | D31 | COM1_CTS | N/C |
| 31 | COM4_RT_B | GREEN | GND | TX1+ | GND |
| 32 | GND | BLUE | +5V | TX1- | +5V |






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### P2 Pin Assignments (with J24 is fitted)

The following P2 pinout is correct if the J24 connector is fitted.

| Pin No. | Row Z | Row A | Row B | Row C | Row D |
|---|---|---|---|---|---|
| 1 | PMC2_IO_2 | DB0~ (SCSI) | +5V | RX0+ | PMC2_IO_1 |
| 2 | GND | DB1~ (SCSI) | GND | RX0- | PMC2_IO_3 |
| 3 | PMC2_IO_5 | DB2~ (SCSI) | Reserved | TX0+ | PMC2_IO_4 |
| 4 | GND | DB3~ (SCSI) | A24 | TX0- | PMC2_IO_6 |
| 5 | PMC2_IO_8 | DB4~ (SCSI) | A25 | RX1+ | PMC2_IO_7 |
| 6 | GND | DB5~ (SCSI) | A26 | RX1- | PMC2_IO_9 |
| 7 | PMC2_IO_11 | DB6~ (SCSI) | A27 | VSYNC | PMC2_IO_10 |
| 8 | GND | DB7~ (SCSI) | A28 | GPIO0 | PMC2_IO_12 |
| 9 | PMC2_IO_14 | DBP~ (SCSI) | A29 | GPIO1 | PMC2_IO_13 |
| 10 | GND | ATN~ (SCSI) | A30 | GPIO2 | PMC2_IO_15 |
| 11 | PMC2_IO_17 | BSY~ (SCSI) | A31 | GPIO3 | PMC2_IO_16 |
| 12 | GND | ACK~ (SCSI) | GND | GPIO4 | PMC2_IO_18 |
| 13 | PMC2_IO_20 | RST~ (SCSI) | +5V | GPIO5 | PMC2_IO_19 |
| 14 | GND | MSG~ (SCSI) | D16 | GPIO6 | PMC2_IO_21 |
| 15 | PMC2_IO_23 | SEL~ (SCSI) | D17 | GPIO7 | PMC2_IO_22 |
| 16 | GND | C/D (SCSI) | D18 | GPIO8 | PMC2_IO_24 |
| 17 | PMC2_IO_26 | REQ~ (SCSI) | D19 | GPIO9 | PMC2_IO_25 |
| 18 | GND | I/O (SCSI) | D20 | GPIO10 | PMC2_IO_27 |
| 19 | PMC2_IO_29 | TERMPWR (SCSI) | D21 | GPIO11 | PMC2_IO_28 |
| 20 | GND | USBP0/MOUSE_CLK | D22 | GPIO12 | PMC2_IO_30 |
| 21 | PMC2_IO_32 | USBP0~/MOUSE_DATA | D23 | GPIO13 | PMC2_IO_31 |
| 22 | GND | KBD_5V | GND | GPIO14 | PMC2_IO_33 |
| 23 | PMC2_IO_35 | USBP1/KBD_CLK | D24 | GPIO16 | PMC2_IO_34 |
| 24 | GND | USBP1~/KBD_DATA | D25 | GPIO17 | PMC2_IO_36 |
| 25 | PMC2_IO_38 | COM2_TXD | D26 | SPEAKER_OUT | PMC2_IO_37 |
| 26 | GND | COM2_RXD | D27 | KEYLOCK_IN | PMC2_IO_39 |
| 27 | PMC2_IO_41 | COM2_RTS | D28 | COM1_TXD | PMC2_IO_40 |
| 28 | GND | HSYNC | D29 | COM1_RXD | PMC2_IO_42 |
| 29 | PMC2_IO_44 | COM2_CTS | D30 | COM1_RTS | PMC2_IO_43 |
| 30 | GND | RED | D31 | COM1_CTS | PMC2_IO_45 |
| 31 | PMC2_IO_46 | GREEN | GND | TX1+ | GND |
| 32 | GND | BLUE | +5V | TX1- | +5V |



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### Alternate P2 Pin Assignments for GPIO Pins

The following pinout table shows alternate P2 Row C pin functions.

| Pin No. | GPIO | Floppy | LPT |
|---|---|---|---|
| 8 | GPIO0 | RDATA~ | STROBE~ |
| 9 | GPIO1 | WGATE~ | LPTD0 |
| 10 | GPIO2 | WDATA~ | LPTD1 |
| 11 | GPIO3 | HDSEL~ | LPTD2 |
| 12 | GPIO4 | FD_DIR~ | LPTD3 |
| 13 | GPIO5 | STEP~ | LPTD4 |
| 14 | GPIO6 | DSKCHG~ | LPTD5 |
| 15 | GPIO7 | DRV2~ | LPTD6 |
| 16 | GPIO8 | DRV1~ | LPTD7 |
| 17 | GPIO9 | MOT0~ | ACK~ |
| 18 | GPIO10 | MOT1~ | BUSY |
| 19 | GPIO11 | WPROT~ | PERROR |
| 20 | GPIO12 | TRK0~ | SELECT |
| 21 | GPIO13 | INDEX~ | AUTOFD~ |
| 22 | GPIO14 | DENSEL | ERR~ |
| 23 | GPIO16 | GPIO16 (ACGAME3) | INIT~ |
| 24 | GPIO17 | GPIO17 (ACGAME4) | SLCTIN~ |

**Notes:** There is no connection to GPIO15 of the south bridge from the P2 connector.
There are three build options on these pins:

GPIO and Floppy (standard)

LPT (parallel port)

GPIO or Floppy section is via software control of the south bridge.

Build options also exist for selection of USB ports or Mouse and Keyboard. Standard build is for Mouse and keyboard.



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### P0 Pin Assignments

### Type B (95-way)

P0 is routed to J14 and partially to J24.

**Note:** Due to the large amount of I/O required to be handled by the PPC7A, Type B connectors are preferred to the Type A (80-pin) shown overleaf, and are fitted by default no particular type is specified.

| Pin No. | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 1 | NC | REDLED~ | EXTRESET~ | TCE7 | TCE6 | GND |
| 2 | FLASH_WREN~ | GREENLED~ | EXTABORT~ | TCT7 | TCT6 | GND |
| 3 | 3.3V† | 3.3V† | 3.3V† | +5V | +5V | GND |
| 4 | PMC1_IO_5 | PMC1_IO_4 | PMC1_IO_3 | PMC1_IO_2 | PMC1_IO_1 | GND |
| 5 | PMC1_IO_10 | PMC1_IO_9 | PMC1_IO_8 | PMC1_IO_7 | PMC1_IO_6 | GND |
| 6 | PMC1_IO_15 | PMC1_IO_14 | PMC1_IO_13 | PMC1_IO_12 | PMC1_IO_11 | GND |
| 7 | PMC1_IO_20 | PMC1_IO_19 | PMC1_IO_18 | PMC1_IO_17 | PMC1_IO_16 | GND |
| 8 | PMC1_IO_25 | PMC1_IO_24 | PMC1_IO_23 | PMC1_IO_22 | PMC1_IO_21 | GND |
| 9 | PMC2_IO_50 | PMC2_IO_49 | PMC2_IO_62 | PMC2_IO_56 | PMC2_IO_55 | GND |
| 10 | PMC2_IO_48 | PMC2_IO_47 | GND | PMC2_IO_64 | PMC2_IO_63 | GND |
| 11 | PMC2_IO_52 | PMC2_IO_51 | PMC2_IO_61 | PMC2_IO_58 | PMC2_IO_57 | GND |
| 12 | PMC1_IO_30 | PMC1_IO_29 | PMC1_IO_28 | PMC1_IO_27 | PMC1_IO_26 | GND |
| 13 | PMC1_IO_35 | PMC1_IO_34 | PMC1_IO_33 | PMC1_IO_32 | PMC1_IO_31 | GND |
| 14 | PMC1_IO_40 | PMC1_IO_39 | PMC1_IO_38 | PMC1_IO_37 | PMC1_IO_36 | GND |
| 15 | PMC1_IO_45 | PMC1_IO_44 | PMC1_IO_43 | PMC1_IO_42 | PMC1_IO_41 | GND |
| 16 | PMC1_IO_50 | PMC1_IO_49 | PMC1_IO_48 | PMC1_IO_47 | PMC1_IO_46 | GND |
| 17 | PMC1_IO_55 | PMC1_IO_54 | PMC1_IO_53 | PMC1_IO_52 | PMC1_IO_51 | GND |
| 18 | PMC1_IO_60 | PMC1_IO_59 | PMC1_IO_58 | PMC1_IO_57 | PMC1_IO_56 | GND |
| 19 | +5V | PMC1_IO_64 | PMC1_IO_63 | PMC1_IO_62 | PMC1_IO_61 | GND |

† The 3.3V pins are *not* connected to a 3.3V supply. They are merely bussed together with the 3.3V pins on the VME P1 connector, the external PMC option is fitted then this is routed to the PMC connectors J12/J22, and capacitively decoupled to ground.

EXTRESET~ generates a Hard Reset and EXTABORT~ generates a Soft Reset. See the Resetting the PPC7A section for more details.

**Note:** Analogue signals should not be routed through P0.



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### Type A (80-way)

P0 is routed to J14.

**Note:** Due to the large amount of I/O required to be handled by the PPC7A, Type B (95-way) connectors are preferred to Type A, and are fitted by default no particular type is specified.

| Pin No. | Row A | Row B | Row C | Row D | Row E | Row F |
|---|---|---|---|---|---|---|
| 1 | NC | REDLED~ | EXTRESET~ | TCE7 | TCE6 | GND |
| 2 | FLASH_WREN~ | GREENLED~ | EXTABORT~ | TCT7 | TCT6 | GND |
| 3 | 3.3V† | 3.3V† | 3.3V† | +5V | +5V | GND |
| 4 | PMC1_IO_5 | PMC1_IO_4 | PMC1_IO_3 | PMC1_IO_2 | PMC1_IO_1 | GND |
| 5 | PMC1_IO_10 | PMC1_IO_9 | PMC1_IO_8 | PMC1_IO_7 | PMC1_IO_6 | GND |
| 6 | PMC1_IO_15 | PMC1_IO_14 | PMC1_IO_13 | PMC1_IO_12 | PMC1_IO_11 | GND |
| 7 | PMC1_IO_20 | PMC1_IO_19 | PMC1_IO_18 | PMC1_IO_17 | PMC1_IO_16 | GND |
| 8 | PMC1_IO_25 | PMC1_IO_24 | PMC1_IO_23 | PMC1_IO_22 | PMC1_IO_21 | GND |
| 9 | PMC1_IO_30 | PMC1_IO_29 | PMC1_IO_28 | PMC1_IO_27 | PMC1_IO_26 | GND |
| 10 | PMC1_IO_35 | PMC1_IO_34 | PMC1_IO_33 | PMC1_IO_32 | PMC1_IO_31 | GND |
| 11 | PMC1_IO_40 | PMC1_IO_39 | PMC1_IO_38 | PMC1_IO_37 | PMC1_IO_36 | GND |
| 12 | PMC1_IO_45 | PMC1_IO_44 | PMC1_IO_43 | PMC1_IO_42 | PMC1_IO_41 | GND |
| 13 | PMC1_IO_50 | PMC1_IO_49 | PMC1_IO_48 | PMC1_IO_47 | PMC1_IO_46 | GND |
| 14 | PMC1_IO_55 | PMC1_IO_54 | PMC1_IO_53 | PMC1_IO_52 | PMC1_IO_51 | GND |
| 15 | PMC1_IO_60 | PMC1_IO_59 | PMC1_IO_58 | PMC1_IO_57 | PMC1_IO_56 | GND |
| 16 | +5V | PMC1_IO_64 | PMC1_IO_63 | PMC1_IO_62 | PMC1_IO_61 | GND |

† The 3.3V pins are *not* connected to a 3.3V supply. They are merely bussed together with the 3.3V pins on the VME P1 connector, the external PMC option is fitted then this is routed to the PMC connectors J12/J22, and capacitively decoupled to ground.

EXTRESET~ generates a Hard Reset and EXTABORT~ generates a Soft Reset. See the Resetting the PPC7A section for more details.

**Note:** Analogue signals should not be routed through P0.



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## Backplane I/O Signal Descriptions

| Mnemonic | Signal Description |
|---|---|
| DB0~ to DB7~ | SCSI bus data |
| DBP~ | SCSI bus data parity |
| ATN~ | SCSI bus Attention |
| BSY~ | SCSI bus Busy |
| ACK~ | SCSI bus Acknowledge |
| RST~ | SCSI bus Reset |
| MSG~ | SCSI bus Message phase |
| SEL~ | SCSI bus Select |
| C/D | SCSI bus Command/Data phase |
| REQ~ | SCSI bus Request |
| I/O | SCSI bus I/O phase |
| TERMPWR | SCSI bus terminator power. Supplies power for external SCSI bus terminators. Rated at 1 Amp† |
| MOUSE_CLK | Mouse Clock. Clock drive for mouse |
| MOUSE_DATA | Mouse Data. Mouse data line |
| KBD_5V | Keyboard 5V. Supplies power for the keyboard and mouse or USB supply when USB is fitted. Rated at 1A† |
| KBD_CLK | Keyboard Clock. Clock drive for the keyboard |
| KBD_DATA | Keyboard Data. Keyboard data line |
| COM1/2/3/4/5/6_TXD | COM1/2/3/4/5/6 Transmit Data |
| COM1/2/3/4/5/6_RXD | COM1/2/3/4/5/6 Receive Data |
| COM1/2/3/4/5/6_RTS | COM1/2/3/4/5/6 Request-To-Send |
| COM1/2/3/4/5/6_CTS | COM1/2/3/4/5/6 Clear-To-Send |
| COM3/4_TT | COM3/4 Terminal timing |
| COM3/4_RT | COM3/4 Receive timing |
| COM3/4_ST | COM3/4 Send timing |
| KEYLOCK_IN | Keylock input. Used to detect the state of an external keyswitch. May be used to implement system password protection |
| SPEAKER_OUT | Loudspeaker Output. Outputs Timer2 Audio. May be used to drive 4Ω or 8Ω loudspeaker |
| NSELECTIN | Parallel port Select In |
| nINIT | Parallel port INIT |
| nFAULT | Parallel port FAULT |
| nAUTOFD | Parallel port AUTOFD |
| SELECT | Parallel port SELECT |
| PERROR | Parallel port PERROR |

| Mnemonic | Signal Description |
|---|---|
| BUSY | Parallel port BUSY |
| nACK | Parallel port ACK |
| D1 to D8 | Parallel port data bits |
| nSTROBE | Parallel port STROBE |
| TX0±/TX1± | 10/100BaseT transmit data |
| RX0±/RX± | 10/100BaseT receive data |
| FLASH_WREN~ | Global FLASH write enable |
| EXT_RESET~ | External Reset (Hard Reset) |
| EXT_ABORT~ | External Abort (Soft Reset) |
| USBP0/USBP0~ | USB interface Port 0 |
| USBP1/USBP1~ | USB interface Port 1 |
| RED, GREEN, BLUE, VSYNC, HSYNC | VGA port |
| PMC2_IO_1 to PMC2_IO_46 | I/O signals from PMC site 2 |
| REDLED~ | Driven identically to the corresponding LED except that this signal has a separate buffer with a 180Ω series resistor |
| GREENLED~ | Driven identically to the corresponding LED except that this signal has a separate buffer with a 180Ω series resistor |
| FLASH_WP~ | FLASH Write Protect signal |
| EXTRESET~ | Generates a Hard Reset. See the Resetting the PPC7A section for more details |
| EXTABORT~ | Generates a Soft Reset. See the Resetting the PPC7A section for more details |
| NC | No connection |
| TCE6 & TCE7 | GT-64260 Timer counter enable |
| TCT6 & TCT7 | GT-64260 Timer counter terminal count |
| 3.3V | These pins are not connected to a 3.3V supply |
| +5V | +5 Volts DC power |
| PMC1_IO_1 to PMC2_IO_64 | I/O signals from PMC site 1 |
| PMC2_IO_48 to PMC_IO_52, PMC2_IO_55 to PMC_IO_58 and PMC2_IO_61 to PMC_IO_64 | I/O signals from PMC site 2.<br>PMC2_IO_48, PMC2_IO_50, PMC_IO_52, PMC2_IO_56, PMC2_IO_58, PMC2_IO_62 and PMC2_IO_64 are not available when a Fibre Channel PMC with rear I/O is fitted |
| GND | The DC voltage reference for the system |

† This is a resettable fuse. The fuse rating is the current rating that the fuse can carry. In 20°C still air, the fuse trips at twice the rated current.



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## PMC Connectors

J11/J21 and J12/J22 give the signals for 32-bit PCI. J13/J23 give the signals for 64-bit PCI and J14/J24 give the user I/O signals.

### J11/J21, J12/J22 and J13/23 Pin Assignments

These PPC4A PMC connectors conform to the IEEE standards. For pin assignments and signal descriptions, refer to the Standard Interfaces section.

**Note:** 3.3V pins are connected to the PPC7A main 3.3V supply.

**CAUTION**

**Do not fit a PMC that requires more than 8 watts from the 3.3V supply.**

**Note:** The PPC7A supports PMC clocking at speeds up to 66 MHz. However, if a PMC is fitted to the PPC7A that does not support the 66 MHz clocking speed, then *both* sites are limited to 33 MHz.

**Note:** The PPC7A has two build options for the VIO supply to the PMCs, 3.3Volts or 5Volts.

As both PMC's are routed to the same PCI bus the VIO supply is then routed to both PMC sites.

When the 5Volt option is fitted the PMC keying pins are fitted in the J11 to J14 or J21 to J24 area, only 5volt or 5volt tolerant PMC's should be fitted. When the VIO is set for 3.3volts the keying posts are removed, ONLY 3.3volt PMC's can be fitted in this mode.

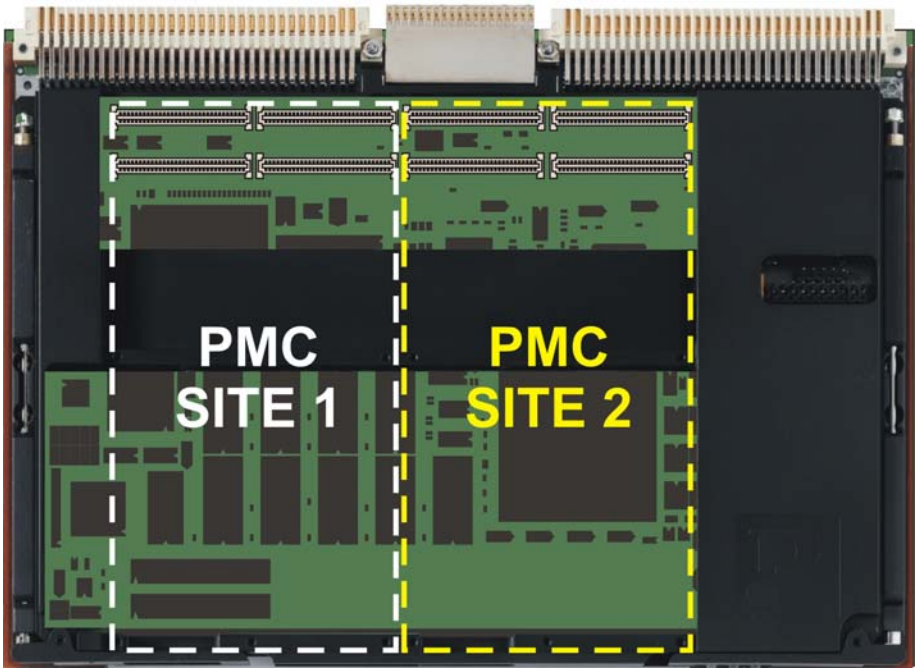
**WARNING**

**Check PMC VIO supply setting before installing any PMC to the PPC7A.**

### J14 PMC I/O Pin Assignments

J14 is routed to P0 conform to ANSI/VITA 35-2000. For pin assignments, refer to the Standard Interfaces section or the ANSI/VITA document.

**Figure C.8 - PMC Positions**






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## J24 PMC I/O and Partial P2 Option

J24 may be partially routed to the P2 connector, depending on the build option. If used, then COM3 and COM4 are no longer routed to P2. P2 now has the connections shown in the following table:

| J24 Pin No. | PMC Signal | Connections | | J24 Pin No. | PMC Signal | Connections | |
|---|---|---|---|---|---|---|---|
| | | P2 | P0 | | | P2 | P0 |
| 1 | PMC2_IO_1 | D1 | | 2 | PMC2_IO_2 | Z1 | |
| 3 | PMC2_IO_3 | D2 | | 4 | PMC2_IO_4 | D3 | |
| 5 | PMC2_IO_5 | Z3 | | 6 | PMC2_IO_6 | D4 | |
| 7 | PMC2_IO_7 | D5 | | 8 | PMC2_IO_8 | Z5 | |
| 9 | PMC2_IO_9 | D6 | | 10 | PMC2_IO_10 | D7 | |
| 11 | PMC2_IO_11 | Z7 | | 12 | PMC2_IO_12 | D8 | |
| 13 | PMC2_IO_13 | D9 | | 14 | PMC2_IO_14 | Z9 | |
| 15 | PMC2_IO_15 | D10 | | 16 | PMC2_IO_16 | D11 | |
| 17 | PMC2_IO_17 | Z11 | | 18 | PMC2_IO_18 | D12 | |
| 19 | PMC2_IO_19 | D13 | | 20 | PMC2_IO_20 | Z13 | |
| 21 | PMC2_IO_21 | D14 | | 22 | PMC2_IO_22 | D15 | |
| 23 | PMC2_IO_23 | Z15 | | 24 | PMC2_IO_24 | D16 | |
| 25 | PMC2_IO_25 | D17 | | 26 | PMC2_IO_26 | Z17 | |
| 27 | PMC2_IO_27 | D18 | | 28 | PMC2_IO_28 | D19 | |
| 29 | PMC2_IO_29 | Z19 | | 30 | PMC2_IO_30 | D20 | |
| 31 | PMC2_IO_31 | D21 | | 32 | PMC2_IO_32 | Z21 | |
| 33 | PMC2_IO_33 | D22 | | 34 | PMC2_IO_34 | D23 | |
| 35 | PMC2_IO_35 | Z23 | | 36 | PMC2_IO_36 | D24 | |
| 37 | PMC2_IO_37 | D25 | | 38 | PMC2_IO_38 | Z25 | |
| 39 | PMC2_IO_39 | D26 | | 40 | PMC2_IO_40 | D27 | |
| 41 | PMC2_IO_41 | Z27 | | 42 | PMC2_IO_42 | D28 | |
| 43 | PMC2_IO_43 | D29 | | 44 | PMC2_IO_44 | Z29 | |
| 45 | PMC2_IO_45 | D30 | | 46 | PMC2_IO_46 | Z31 | |
| 47 | PMC2_IO_47 | | B10 | 48 | PMC2_IO_48 | | A10 |
| 49 | PMC2_IO_49 | | B9 | 50 | PMC2_IO_50 | | A9 |
| 51 | PMC2_IO_51 | | B11 | 52 | PMC2_IO_52 | | A11 |
| 53 | PMC2_IO_53 | | | 54 | PMC2_IO_54 | | |
| 55 | PMC2_IO_55 | | E9 | 56 | PMC2_IO_56 | | D9 |
| 57 | PMC2_IO_57 | | E11 | 58 | PMC2_IO_58 | | D11 |
| 59 | PMC2_IO_59 | | | 60 | PMC2_IO_60 | | |
| 61 | PMC2_IO_61 | | C11 | 62 | PMC2_IO_62 | | C9 |
| 63 | PMC2_IO_63 | | E10 | 64 | PMC2_IO_64 | | D10 |

**Note:** P0 pins A9, A10, A11, C9, D9, D10 and D11 are not available if a Fibre Channel PMC with rear I/O is fitted.



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## P10 PLD Connector Pinout

P10 is the programming JTAG chain this is normally for factory use.

| Pin No. | Description |
|---|---|
| 1 | VCC |
| 2 | PLD_TDO |
| 3 | PLD_TDI |
| 4 | N/C |
| 5 | KEYWAY |
| 6 | PLD_TMS |
| 7 | GND |
| 8 | PLD_TCK |

For more information on JTAG, see the Functional Description section.

## P8 RISCWatch Connector Pinout

P8 is the RISCWatch connector allowing the connection of software debugging tools that use the processor's JTAG port to control the operation of the processor.

| Pin No. | Signal | Pin No. | Signal |
|---|---|---|---|
| 1 | TDO_CPU | 2 | EMU~/QACK_IN~ |
| 3 | TDI_CPU | 4 | TRST~ |
| 5 | QREQ~ | 6 | +3.3V pull-up |
| 7 | TCK | 8 | NC |
| 9 | TMS | 10 | NC |
| 11 | SRESET_CPU~ | 12 | GND |
| 13 | HRESET_CPU~ | 14 | NC |
| 15 | CHECKSTOP~ | 16 | GND |

For more information on JTAG, see the Functional Description section.

### P8 Signal Descriptions

| Signal | Description |
|---|---|
| TDO_CPU | Processor JTAG Test Data Out |
| EMU~ | When connected to GND, creates QACK~ to the processor. This connection should be made with an emulator |
| TDI_CPU | Processor JTAG Test Data In |
| TRST~ | Processor JTAG Test Reset |
| +3.3V PULL-UP | Power-on status signal to RISCWatch hardware |
| TCK | Processor JTAG Test Clock |
| TMS | Processor JTAG Test Mode Select |
| SRESET_CPU~ | Processor Soft Reset |
| GND | Signal ground |
| HRESET_CPU~ | Processor Hard Reset |
| CHECKKSTOP~ | Processor Checkstop output |
| GND | Signal ground |

For more information on JTAG, see the Functional Description section.



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### EST Emulator Connection

| Pin No. | Signal | Description |
|---|---|---|
| 1 | TDO_CPU | Processor JTAG Test Data Out |
| 2 | QACK_IN~ | Quiescent grant to Processor |
| 3 | TDI_CPU | Processor JTAG Test Data In |
| 4 | TRST~ | Processor JTAG Test Reset |
| 5 | QREQ~ | Processor Quiescent request |
| 6 | +3.3V pull-up | Power-on status signal to EST hardware |
| 7 | TCK | Processor JTAG Test Clock |
| 9 | TMS | Processor JTAG Test Mode Select |
| 11 | SRESET_CPU~ | Processor Soft Reset |
| 12 | GND | Signal ground |
| 13 | HRESET_CPU~ | Processor Hard Reset |
| 15 | CHECKKSTOP~ | Processor Checkstop output |
| 16 | GND | Signal ground |



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# Specifications

## Mechanical Construction

| | |
|---|---|
| **Weight** | 680g approx. As most of this is due to the heatsink, the weight is more or less the same for all build styles. |
| **Dimensions** | The air-cooled PPC7A is constructed on a multi-layer double Eurocard and conforms to the dimensions specified in the ANSI/VITA 1-1994 specification. For layout drawings, refer to the Standard Interfaces section.<br>The Conduction-cooled PPC4A is constructed on a multi-layer double Eurocard and conforms to the dimensions specified in the IEEE 1101.2. For layout drawings, refer to the Standard Interfaces section. |

## Local Resources

| | | |
|---|---|---|
| **Processor** | PowerPC 745x at 1000 MHz or above. | |
| **SDRAM** | 64 to 1024 Mbytes with ECC. | |
| **L2 or L3 Cache** | 1 to 4 Mbyte on private cache bus. | |
| **Graphics** | Totally integrated 2D graphics processor with 2Mbytes of graphics SRAM on chip.<br>With 69000:<br>Pixel clocks up to 135Mhz, up to 24 bit colour depths per pixel.<br>1280 x 1024 x 8 @ 75Hz, 1024 x 768 x 16 @ 85 Hz, 800 x 600 x 24 @ 85 Hz<br>With 69000:<br>Pixel clocks up to 170Mhz, up to 24 bit colour depths per pixel.<br>1280 x 1024 x 24 @ 80Hz, 1024 x 768 x 24 @ 85 Hz, 800 x 600 x 24 @ 85 Hz | |
| **FLASH** | Up to 256 Mbytes, with 8 Mbytes reserved for Boot FLASH banks | |
| **RTC** | I²C RTC backed up by connection to VMEbus 5VSTDBY pin. | |
| **NVRAM** | 32 Kbytes. | |
| **PCI** | 64-bit @ 66 MHz. | |
| **SCSI** | 8 bit fast Ultra-SCSI via the P2 connector. | |
| **Ethernet** | 2 off, Ethernet 10/100BaseT via the P2 connector. | |
| **PMC Slots** | Air-cooled: Two 5V, 32-bit IEEE P1386.1 compliant slots with front panel and P0 I/O, and restricted P2 I/O. | |
| **Serial I/O** | Six serial I/O channels via the P2 connector. Two channels are equipped with clocks for synchronised operation with interfaces that allow for RS422 or RS232. | |
| **Keyboard and Mouse** | PS/2 compatible Keyboard and Mouse interface via the P2 connector. | |
| **Parallel I/O** | Centronics style port via the P2 connector. | |
| **Floppy Disk Interface** | MFM 1.44/2.88 Mbyte via P2 connector. | |
| **Counter/Timers** | Eight 32-bit timers with a resolution of one bus clock (100 Mhz). | |
| **Reset/Abort switch** | Front panel mounted | |
| **Operating Systems** | LynxOS, VxWorks/Tornado, INTEGRITY | |
| **PCI Expansion** | PCI through P0 via PMCPCI card. | |
| **I/O Modules** | P2 (3U mounting) | SCSI,<br>Six serial,<br>Parallel, floppy<br>Mouse and keyboard,<br>Ethernet: 10/100BaseT |
| | Miscellaneous | P2 transition module<br>(including 50-way SCSI header) |



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## EMC Regulatory Compliance and Safety

Air-cooled versions of PPC7A are designed for use in systems meeting VDE class B, EN and FCC regulations for EMC emissions and susceptibility.

All PCBs are manufactured by UL approved manufacturers and have a flammability rating of 94V-0.

## Power Requirements

| Supply Voltage | PPC7A-7410 128 Mbyte SDRAM | PPC7A-7410 256 Mbyte SDRAM |
|---|---|---|
| +5V +5 %, -2.5 % | 3.5A | 3.5A |

These figures are based on a 500 MHz MPC7410 running at 500 MHz with a 100 MHz processor bus. The card was running a comprehensive memory test and gave measured values for +5V supply current of 3500 mA for the 128 Mbyte SDRAM version and 3500 mA for the 256 Mbyte SDRAM version.

**Note:** When using PMCs, ensure that they do not cause the specified maximum supply current to be exceeded, especially from the +5V supply. The VME specification allows a maximum of 7.5 Amps to be drawn from the +5V supply in a single slot over the PPC7A's specified operating temperature range. It may not be possible to support all combinations of SDRAM and PMCs within this limit.

The PPC7A uses the undefined pins (rows a, c, d and z) of the VMEbus P2 connector for I/O and power/ground connections. 3.3V is connected to both of the PMC sites.

**⚠ WARNING**

**Do not exceed the maximum rated input voltages or apply reversed bias to the assembly.**

**If such conditions occur, toxic fumes may be produced due to the destruction of components.**

**⚠ CAUTION**

**Only use the PPC7A in backplanes that supply power on both the J1 and J2 connectors.**



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## VMEbus Compliance

The PPC7A conforms to the ANSI/VITA 1-1994 standard for VME64.

| | |
|---|---|
| **Master:** | A16, A24 and A32<br>ADO, ADOH<br>A16:LCK, A24:LCK, A32:LCK<br>D08(EO), D08(EO):RMW, D08(EO):BLT<br>D16, D16:RMW, D16:BLT<br>D32, D32:RMW, D32:BLT, D32:UAT<br>D64:MBLT |
| **Slave:** | A16, A24 and A32<br>ADO, ADOH<br>A16:LCK, A24:LCK, A32:LCK<br>D08(EO), D08(EO):RMW, D08(EO):BLT<br>D16, D16:RMW, D16:BLT<br>D32, D32:RMW, D32:BLT, D32:UAT<br>D64:MBLT |
| **Interrupt Handler:** | D08(O), IH(1-7) |
| **Interrupter:** | I(1-7) |
| **VMEbus Arbiter:** | SGL, RRS, PRI, BCLR~ generation |
| **VMEbus Requester:** | ROR, RWD<br>Early BBSY~ release<br>Bus capture and hold |
| **Bus Time-out Module:** | 16, 32, 64, 128, 256, 512, 1024 µS, disabled |
| **Other Slot 1 Functions:** | Slot 1 detector, IACK~ daisy chain driver,<br>SYSCLK driver |
| **Auto Slot ID:** | VME64 specified and SCV64 compatible modes or geographical addressing via 5-row P1 connector |

## Reliability (MTBF)

The following table shows the calculated MTBFs for the PPC7A-1BA-10:

| Environment | Fail Rate (Failures Per Million Hours) | MTBF (Hours) |
|---|---|---|
| **Ground benign 30°c** | 6.298724 | 158,762 |
| **Ground fixed 40°c** | 14.72659 | 67,904 |
| **Ground mobile 45°c** | 26.94278 | 37,116 |
| **Naval sheltered 40°c** | 23.7376 | 42,127 |
| **Naval unsheltered 45°c** | 38.72897 | 25,820 |
| **Airborne inhabited cargo 55°c** | 31.34095 | 31,907 |
| **Airborne inhabited fighter 55°c** | 41.45621 | 24,122 |
| **Airborne uninhabited cargo 70°c** | 52.65228 | 18,993 |
| **Airborne uninhabited fighter 70°c** | 79.78461 | 12,534 |
| **Airborne rotary wing 55°c** | 56.9936 | 17,546 |
| **Space flight 30°c** | 5.5010268 | 181,784 |
| **Missile flight 45°c** | 32.6502 | 30,628 |
| **Missile launch 55°c** | 78.40276 | 12,755 |

These failure rates are based only on the components and connectors fitted to the board at delivery and take no account of user fitted PMCs.

The failure rates used in this calculation are based on MIL-HDBK-217F Notice 1 (parts count method) with commercial or non-military quality level. Where a component did not comply with the MIL-HDBK, the closest equivalent, compliant component was used.



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## Product Codes

**PPC7A10 -** X X X X X X X

**SOFTWARE**

| |
|---|
| 1 = SilverChip |
| 2 = BIT/SilverChip |
| 3 = VxWorks |
| 4 = BIT/VxWorks |
| 5 = PPCBoot |
| 6 = BIT/PPCBoot |

**P0 CONNECTOR OPTIONS**

| |
|---|
| O = No P0 |
| A = TYPE A |
| B = TYPE B |

**COMMS OPTIONS/P2 PMC I/O**

| |
|---|
| 1 = 2 x 10/100BaseT Ethernet, P2 PMC I/O |
| A = Reserved |
| B = 2 x 10/100BaseT Ethernet & COM 3 & 4, COM 5 & 6 RS232 |
| C = 2 x 10/100BaseT Ethernet & COM 3 & 4, COM 5 & 6 RS422 |

**FLASH / USB / GPIO**

| | |
|---|---|
| 0 = 64MB, USB, GPIO | 1 = 64MB, Keyboard, Mouse, GPIO |
| 2 = 64MB, USB, Parallel | 3 = 64MB, Keyboard, Mouse, Parallel |
| 4 = 128MB, USB, GPIO | 5 = 128MB, Keyboard, Mouse, GPIO |
| 6 = 128MB, USB, Parallel | 7 = 128MB, Keyboard, Mouse, Parallel |
| 8 = 256MB, USB, GPIO | 9 = 256MB, Keyboard, Mouse, GPIO |
| A = 256MB, USB, Parallel | B = 256MB, Keyboard, Mouse, Parallel |

**MEMORY**

| |
|---|
| 0 = Reserved |
| 1 = 128MB / 5 V PMC Signalling |
| 2 & 3 = Reserved |
| 4 = 256MB / 5V PMC Signalling |
| 5 = 512MB / 5V PMC Signalling |
| 6 = 128MB / 3.3V PMC Signalling |
| 7 = 256MB / 3.3V PMC Signalling |
| 8 = 512MB / 3.3V PMC Signalling |
| 9 = 1GB / 3.3V PMC Signalling |
| A = 1GB / 5V PMC Signalling |

**PROCESSOR**

| | |
|---|---|
| 0 to 4 = Reserved | A & B = Reserved |
| 5 = 755 @ 400MHz | C = 7410 @ 500MHz |
| 6 to 9 = Reserved | D = Reserved |

**RUGGEDISATION LEVEL**

1, 2, 3, 4, 5

**Notes:** P0 options are available on all build levels.

Due to the large amount of I/O required to be handled by the PPC7A, Type B (95-way) connectors are preferred to Type A (80-pin), and are fitted by default no particular type is specified.

PPC7A5x product codes are on the next page.



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**PPC7A5x -** X X X X X X X

**SOFTWARE**
1 = SilverChip
2 = BIT/SilverChip
3 = VxWorks
4 = BIT/VxWorks
5 = PPCBoot
6 = BIT/PPCBoot

**P0 CONNECTOR OPTIONS**
O = No P0
A = TYPE A
B = TYPE B

**COMMS OPTIONS/P2 PMC I/O**
1 = 2 x 10/100BaseT Ethernet, P2 PMC I/O
A = Reserved
B = 2 x 10/100BaseT Ethernet & COM 3 & 4, COM 5 & 6 RS232
C = 2 x 10/100BaseT Ethernet & COM 3 & 4, COM 5 & 6 RS422

**FLASH / USB / GPIO**

| | |
|---|---|
| 0 = 64MB, USB, GPIO | 1 = 64MB, Keyboard, Mouse, GPIO |
| 2 = 64MB, USB, Parallel | 3 = 64MB, Keyboard, Mouse, Parallel |
| 4 = 128MB, USB, GPIO | 5 = 128MB, Keyboard, Mouse, GPIO |
| 6 = 128MB, USB, Parallel | 7 = 128MB, Keyboard, Mouse, Parallel |
| 8 = 256MB, USB, GPIO | 9 = 256MB, Keyboard, Mouse, GPIO |
| A = 256MB, USB, Parallel | B = 256MB, Keyboard, Mouse, Parallel |

**MEMORY**
0 = Reserved
1 = 128MB / 5 V PMC Signalling
2 & 3 = Reserved
4 = 256MB / 5V PMC Signalling
5 = 512MB / 5V PMC Signalling
6 = 128MB / 3.3V PMC Signalling
7 = 256MB / 3.3V PMC Signalling
8 = 512MB / 3.3V PMC Signalling
9 = 1GB / 3.3V PMC Signalling
A = 1GB / 5V PMC Signalling

**PROCESSOR**
0 to 9 = Reserved
A to C = Reserved
D = 7457 @ 1GHz

**RUGGEDISATION LEVEL**
1, 2, 3, 4, 5

**Notes:** P0 options are available on all build levels.

Due to the large amount of I/O required to be handled by the PPC7A, Type B (95-way) connectors are preferred to Type A (80-pin), and are fitted by default no particular type is specified.

PPC7A10 product codes are on the previous page.



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## P2 I/O Module

Compatible Backplane Transition Modules for the PPC7A are the P25X606 and the P25X606A. For installation instructions and pin assignments, refer to the I/O Modules Manual, Publication Number RT5154.



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## Troubleshooting

If you are experiencing a problem with your PPC7A, there follow some general suggestions of actions you may take, which may resolve the problem without the need to contact Radstone's technical support.

- Ensure that the board is firmly seated and secured in the rack and that all male/female connectors mate together correctly
- Check the links on the board and the system backplane
- If you are unsure of which link configuration to use, try the default configuration initially
- Check that the VME rack has terminators, if these are not built in (the manual for your rack should tell you whether the terminators are built in)
- Using a digital volt meter, check that the power supply is within VME limits on +5V, +12V and -12V

**⚠ WARNING**

**Power supply problems should only be dealt with by qualified personnel.**

- Check that there is only one board configured as system controller in a system and that this is in slot 1 of the rack
- Check that there are no vacant slots in the rack without jumpers (or that an automatic daisy chaining backplane is being used)
- Prove the PPC7A's operation in isolation before adding it into a multi-board system
- If you are using the SCSI bus, then check that the cable stub length is less than 10 cm. You are also recommended to locate the PPC7A at one end and enable the bus terminator by fitting link E13. If you want to use the PPC7A somewhere other than at the end of the SCSI bus, ensure that E13 is not fitted. **Fitting E13 when the PPC7A is not located at the end of a SCSI bus may cause erroneous SCSI operation.**
- If you have made your own cable for connection between P7 or P2 and a terminal/hyperterminal, check that the pinout is correct
- Check that the terminal is set up for DTE (9.6 kbaud, 8 bits/character, 1 stop bit, parity disabled)
- Ensure that air-cooled PPC7As receive sufficient air-flow. If you need to operate your PPC7A on an extender card, this requires an additional fan to supply the necessary air flow
- Ensure that conduction cooled PPC7As are fully installed in the conduction cooled box and that the wedgelocks are correctly tightened. If, for any reason, you need to operate a conduction cooled PPC7A on an extender card, you must maintain an airflow of at least 300 feet/minute over it
- If you are having problems programming the FLASH, then check that the appropriate write enable link, E3 or E9, is fitted, and that the backplane signal, FLASH_WP~ (P0 pin A2) is connected to GND or E5 is fitted. See the FLASH section and the E3, E5 and E9 descriptions for more details



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# Glossary

**Note:** See the general Radstone Glossary, Publication Number RT5116.

**BCS**
Background Condition Screening.

**CR/CSR**
Configuration ROM/Control and Status Register.

**LRU**
Line Replaceable Unit.

**PPC7A**
Radstone's PowerPC-based processor card. The PPC7A is based on the PowerPC 745x/7410 processor with integral L3/L2 cache controller and uses SDRAM.



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