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Hardware Reference Manual

CP945FP-12 CompactPCI, RM945FP-12 VME, & RM948 With Embedded Layer 2 Switch, Front Input/Output

DDC No. Rx-URMH 122 Rev A
Issued 5 December 2003

it's all about connexions

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1 Introduction

RAMiX has designed the CP945FP-12 CompactPCI and RM945FP-12 VME economical, configurable 10/100 Layer 2 embedded Ethernet switches. Both modules are available with:

- Full wire speed Layer 2 switch fabrics
- 12 ports 10/100BaseTX, front I/O
- Full duplex operation in both 10/100 modes
- Auto negotiation capability on all ports

The CP945FP-12 and RM945FP-12 are fully integrated 12-port Ethernet switches with front panel I/O, designed to support the low-cost requirements of unmanaged switch applications.

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1.1 Key Features

As with all CompactPCI products from RAMiX, the CP945FP-12 module offers Hot Swap insertion capability for higher reliability and rapid service.

The RM945FP-12 is a standalone switch and will work independently of any operating system. On power-up, the switch will automatically boot up and begin switching in Layer 2 mode without any input from the operator or host central processing unit (CPU).

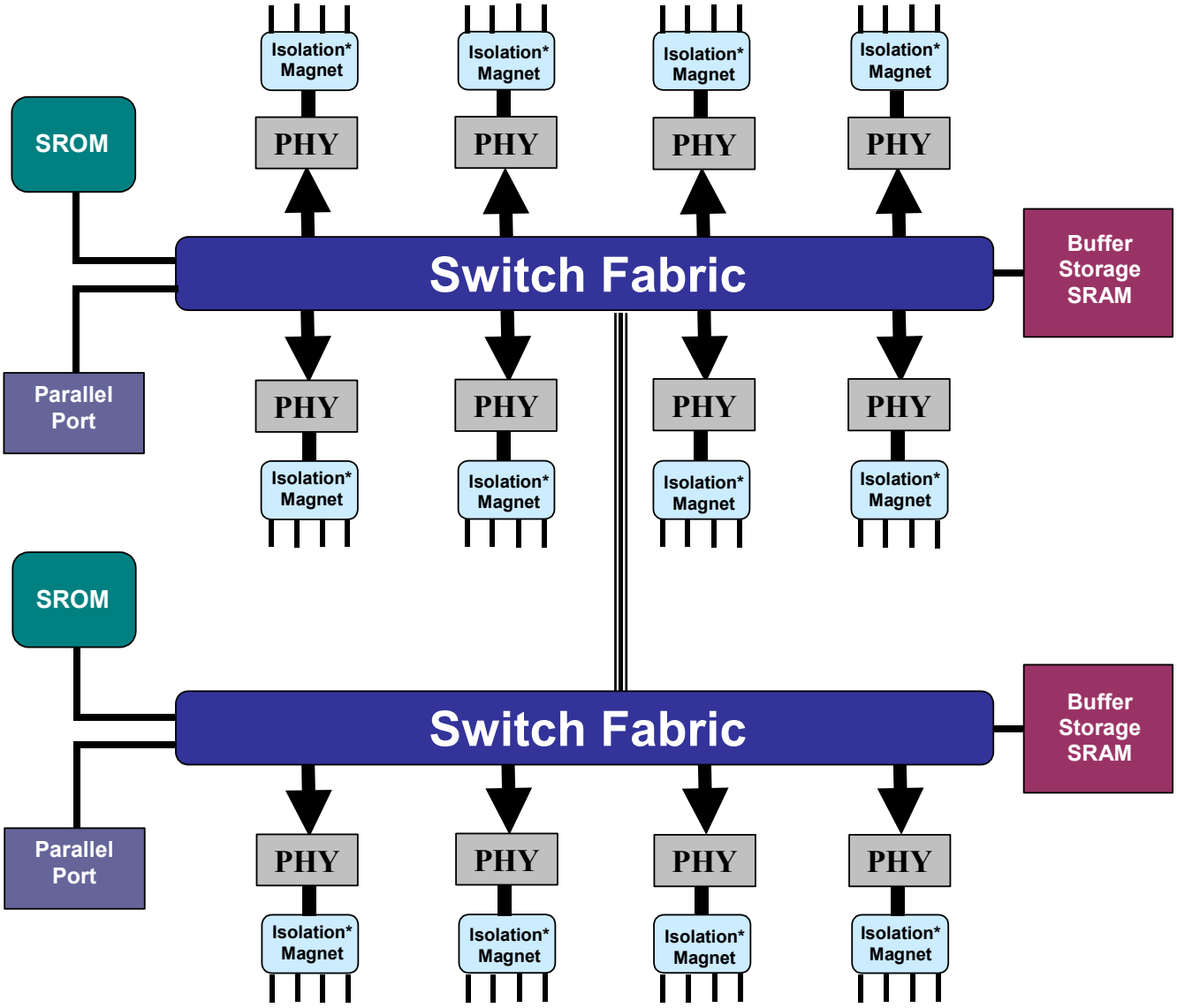
The key features of both modules are:

- 12 ports (via RJ45 connectors) of 10/100BaseTX, auto-negotiating, front I/O panel
- Full wire speed layer 2 switching on all ports
- 1k MAC address table
- Auto address learning
- Auto address aging Leading edge QoS capabilities, based on 802.1p and IP TOS/DS field
- Up to 8 port based VLANs
- Offers port trunking
- Supports port mirroring
- Provides both Full/Half duplex ports
- Flow Control capabilities
    - Back pressure for half-duplex
    - 802.3x flow control for full-duplex

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2 Theory Of Operation

The switch architecture is illustrated in the block diagram below. Total port count is achieved by combining two ZarlinkMDS 108 8 port fabrics via their uplink.



By definition, a Network Switch differs from a hub in that each packet received into the switch is transmitted to the minimum number of ports. This greatly improves aggregate data rate (i.e., multiple pairs of ports can be involved in data transfer at a single point in time). As each packet arrives at the switch, both the source and destination address of the packet are examined. The source is retained and associated with the arrival port as the location of that device. If the packet is unicast (i.e., destined for a single receiver) and the destination is known, the packet will only be transmitted to the port associated with the destination address. Since the learning is automatic, no operator intervention is needed. As attached workstations (or other network capable devices) communicate, their locations are learned and traffic can be localized to the port.

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The xx945 switches are implemented with two fabrics connected by a private uplink. One fabric provides 8 of the ports, the other the remaining 4. The ports and configuration of each fabric is initialized by a(n) (independent) SROM device. The contents of the SROM may be modified using a standard PC Parallel port (connected via the DB25 to RJ45 connector, see details in section ***3 Handling and Installation***.

In default configuration, the CP945FP-12 and RM945FP-12 switches deliver a fully auto-configuring interconnect. Each port will negotiate speed and duplex with the connected interface. Once a link has been established, incoming packets are examined and the source MAC address added to the table associated with that port. When the destination address has been associated with a port (from an earlier transmission), the packet is forwarded only to that port. This process is independent for each port, so that the aggregate throughput of the switch fabric is much higher than that of a single channel.

Where the destination has not yet been acquired, the packet is sent to all ports. Refer to section ***2.1.1 Port Based VLAN*** for behavior when this option has been configured.

Because the negotiation and learning process is automatic, there is no operator or start-up interaction required. The SRAM buffer provides local storage to allow for dealing with multiple incoming packets with a single destination port. Packets will be sequenced and buffered to avoid data loss. The QoS (optional) offers a mechanism to prioritize traffic.

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2.1 Operational Configuration Options

The switch fabric has a number of performance operations usually found only in managed switch products. These options include:

- Port based VLAN
- QoS
- Port speed/duplex forced configuration

All of these parameters are set via the SROM. This can either be programmed prior to manufacturing or configured in the field from the front panel parallel port.

2.1.1 Port Based VLAN

The switch fabric provides the designer with the ability to define a single port-based VLAN for each of the 12 ports. This VLAN is individually defined for each port, assigning a VLAN ID (value between 0–11) for each port.

When packets arrive at an input of the switch, the search engine will determine the VLAN ID for that port, and will then determine which of the other ports are also members of that VLAN by matching their assigned VLAN ID values. The packet will then be transmitted to each port with the same VLAN ID as the source port.

2.1.2 QoS

QoS provides a new level of capability to unmanaged switch applications with two transmit queues per output port.

The fabric manages the output transmission queues for all ports of the fabric. Once the destination address search is complete, the packet is inserted into the appropriate output queue. Packet entry into high or low priority queue is controlled by either the VLAN tag information or the TOS field in the IP header. Each of these priority fields can used to select the transmission queue priority as well as a packet drop probability. The mapping of the tag and TOS fields to either the high or low priority queue is configured on power-up from the SROM.

The fabric utilizes Weighted Round Robin (WRR), Random Early Drop with In/Out (RED/RIO) bit, and a timestamp method of scheduling packets for transmission. WRR uses an efficient method to ensure that each of the transmission queues gets at least a minimum service level. With two output transmission queues, the fabric will transmit “X” packets from the high priority queue before transmitting “Y” packets from the low priority queue. The “X” and “Y” weights are user definable. The high priority weight can be set to a value between 0-16. The low priority weight is fixed at the value 1. If the high priority weight is set to the value 4, then the fabric will transmit four high priority packets before transmitting each low priority packet.

The timestamp method of scheduling packets for transmission allows the fabric to offer latency guarantees to high priority packets. This is ideal for voice and video packets that have strict latency requirements. Packets are given a timestamp when they arrive at the input port. Once they are scheduled into a transmission queue, the fabric will keep track of the packets delay time through the chip. Under heavy congestion the timestamp may be utilized to change the order of packet transmission to ensure timely delivery of packets and orderly service of congested queues.

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The following are the transmission scheduling exceptions:

1. Packets with high priority and low priority drop will be transmitted before any in the low priority queue.
2. If the high priority delay is => 2ms, then transmit from the high priority queue.
3. If the high priority delay is < 1ms and the low priority queue is congested, then transmit from the low priority queue.
4. If the high priority delay is < 2ms and the low priority queue is full, then transmit from the low priority queue.

The QoS capabilities of the fabric are enabled by loading the appropriate values into the configuration registers and by either enabling or disabling the flow control. The values are loaded from SROM. To alter the QoS characteristics, modify the SROM configuration.

When Flow Control and QoS are enabled, the fabric will utilize WRR to schedule packet transmission, and will use either backpressure or 802.3x flow control to handle situations of buffer memory congestion. When Flow Control is disabled and Qos is enabled, the fabric will use RED/RIO to drop random packets in order to handle situations of buffer memory congestion. In this method, only certain packet flows are slowed down, while the remaining see no impact from the network traffic congestion. RED/RIO is a method of handling traffic congestion in the absence of Flow Control mechanisms. When Flow Control is enabled, all devices that are connected to a switch node that is exercising flow control are effectively unable to transmit, even nodes that are not directly responsible for the congestion problem. RED/RIO allows traffic to continue flowing into ports on a switch and randomly drops packets with different probabilities based upon each packet's priority markings. As the switch congestion increases, the probability of dropping an input packet increases. As congestion decreases, the probability of dropping an input packet decreases. In this manner, only traffic flows that have had packets dropped will be affected by the congestion. Other traffic flows will see no effect.

2.1.3 Port Configuration

By setting parameters in the SROM, each port can be individually configured in speed (i.e., 10 or 100Mbs) and duplex (i.e., full or half).

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2.2 Setting Optional Characteristics

As described in section **2 *Theory of Operation*** section, the switch fabric can be configured to support QoS, VLAN and port profile information. This data is captured in an on-card SROM that is loaded into the fabric control engine during power on. The contents of the SROM can be altered using a standard parallel port and PC.

Contact RAMiX to receive a copy of the programming tool (for Windows 95/98 and NT). There is no charge for this program.

SROM contents may also be set at the factory, consult your RAMiX sales representative for information on this service.

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3 Handling and Installation

3.1 Handling Precautions

Electronic assemblies use devices that are sensitive to static discharge. Observe anti-static procedures when handling these boards. All products should be in an anti-static plastic bag or conductive foam for storage or shipment. Work at an approved anti-static workstation when unpacking boards.

3.2 Unpacking and Verification

RAMiX products are shipped in individual, reusable shipping boxes. When receiving the shipping container, inspect it for any evidence of physical damage. If the container is damaged, request that the carrier's agent be present during the unpacking of individual boxes and the inspection of each unit.

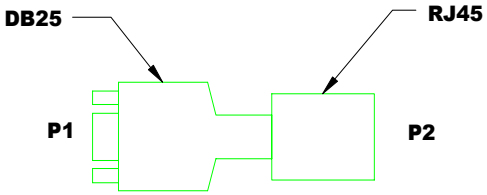
Remove the RM94X card from the shipping box and anti-static packaging. Verify that it is not damaged and that all items are present by referring to the packing list.

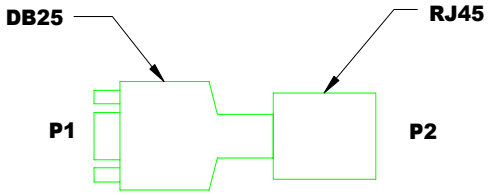
3.3 Installation

Installation is done generically as with the commercial versions of the card. Follow any specific procedures recommended by the manufacturer of the chassis used.

3.4 Cable Adapter Pin Outs

Both the CP945FP-12 and RM945FP-12 are designed for use with a female RJ45 to male DB25 cable adapter. The cable adapter, RAMiX part number 06-0714025, is illustrated below, and can be wired using the DB25-1 and DB25-2 cable pin outs shown below.





DB25-1 Pin Out	
P1	P2
1	1
2	2
10	4
21	6

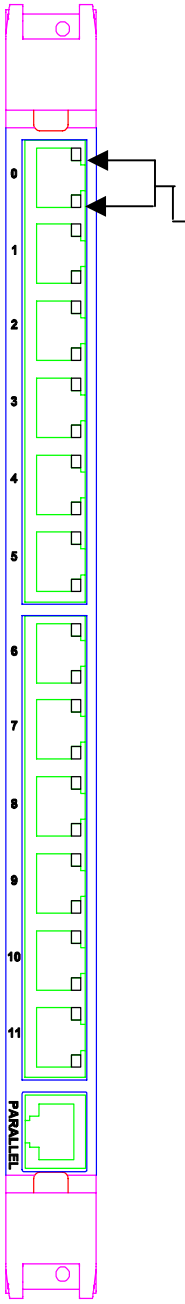
DB25-2 Pin Out	
P1	P2
1	7
2	8
10	5
21	10

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4 Front Panel Connectors and Indicators

4.1 CP945FP-12 and RM945FP-12

The CP945FP-12 and RM945FP-12 use an identical front panel—face and side illustrations below not to actual size. The RJ45 connectors have 10/100BaseTX network connections. They are wired per industry specification. Any standard network cable may be used to connect them with a NIC card.



Link/Activity LEDs

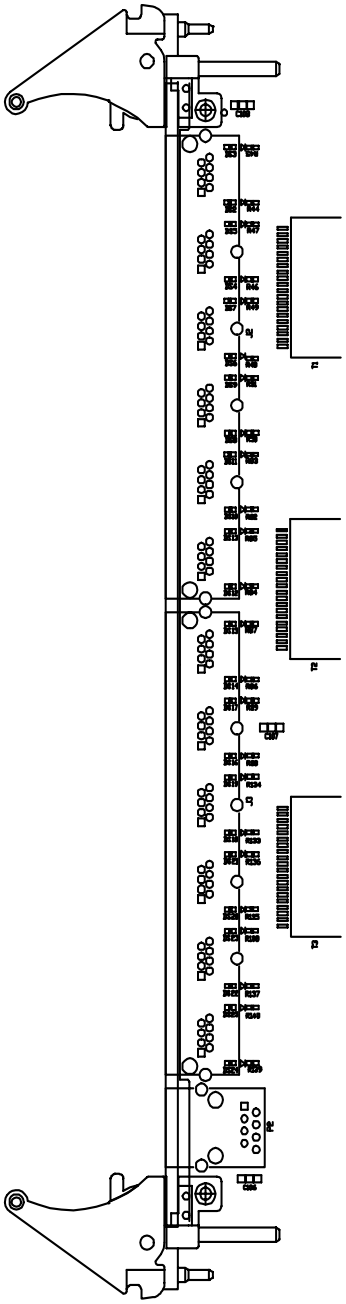
Each of the 12 ports (0 – 11) has an associated set of Link/Activity LEDs. The LEDs will illuminate when valid links are detected. Until a valid link is present, no activity can take place on a port.

A solid LED illumination indicates a valid link, but no traffic. A blinking LED indicates port activtata traffic is on the port when packets are received or transmitted.

Parallel Port

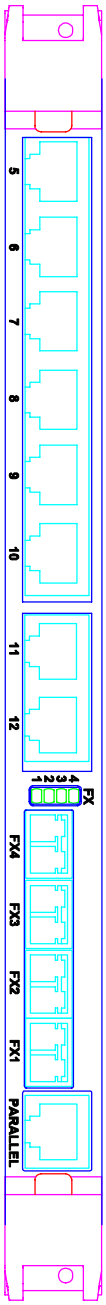
The parallel port can be connected to a PC parallel port.

The contents of the SROM can be altered using the parallel port and a PC.



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4.2 RM948



Link/Activity LEDs

Each of the 12 ports (0 – 11) has an associated set of Link/Activity LEDs. The LEDs will illuminate when valid links are detected. Until a valid link is present, no activity can take place on a port.

A solid LED illumination indicates a valid link, but no traffic. A blinking LED indicates port activity—data traffic is on the port when packets are received or transmitted.

Parallel Port

The parallel port can be connected to a PC parallel port.

The contents of the SROM can be altered using the parallel port and a PC.

Connectors

8 RJ45 Copper ports
4 LC Fiber ports

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4.3 Network Connections (CPCI Products Only)

There is a single PCI/Ethernet chip which mates to the PCI Bus. This allows the host to connect directly to the switch fabric without any external cables. This port can also be used as a second interface Ethernet in addition to the host. The network interface runs at the 100Mbit full duplex into the switch fabric.

Note: Connecting to another Ethernet HUB or SWITCH: A "crossover" cable must be used, or the connection must be to the "uplink" port of the hub or switch.

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5 Functional Specifications

5.1 CP945FP-12 Port CompactPCI Embedded Layer 2 Switch, Front I/O

Power	4 Total Watts
@ 3.3 V	1.2 Amps
Form Factor	
cPCI	6U Single Slot
MTBF	
MIL 217-F Nav Shel 25 Deg. C	283000 Hours
Temperature	
Operating	0 to +60° C
Storage	-40 to +85° C
Humidity	
Operating	5% to 95% Non-Condensing
Storage	5% to 95% Non-Condensing

Conformal Coating	Yes, additional charge

PCI Standards	
Hot Swap	Yes

Switches	
Ports	
10/100 Base-TX	12
Port Routing	
Front	(12) RJ45 10/100BaseTX
Switching	
Management	Unmanaged
Layer	2

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5.2 RM945FP-12 Port VME Embedded Layer 2 Switch, Front I/O

Power	**4 Total Watts**
@ 5 V	**0.8 Amps**
Form Factor	
cPCI	**6U Single Slot**
MTBF	
MIL 217-F Nav Shel 25 Deg. C	**283000 Hours**
Temperature	
Operating	**0 to +60° C**
Storage	**-40 to +85° C**
Humidity	
Operating	**5% to 95% Non-Condensing**
Storage	**5% to 95% Non-Condensing**

Conformal Coating	**Yes, additional charge**

PCI Standards	
Hot Swap	**Yes**

Switches	
Ports	
10/100 Base-TX	**12**
Port Routing	
Front	**(12) RJ45 10/100BaseTX**
Switching	
Management	**Unmanaged**
Layer	**2**

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5.3 RM948

Power	**4 Total Watts**
@ 5 V	**0.8 Amps**
Form Factor	
VME	**6U Single Slot**
MTBF	
MIL 217-F Nav Shel 25 Deg. C	**283000 Hours**
Temperature	
Operating	**0 to +60° C**
Storage	**-40 to +85° C**
Humidity	
Operating	**5% to 95% Non-Condensing**
Storage	**5% to 95% Non-Condensing**

Conformal Coating	**Yes, additional charge**

Switches	
Ports	
10/100 Base-TX	**12**
Port Routing	
Front	**(8) RJ45 10/100BaseTX (4) LC 100BaseFX (Fiber)**
Switching	
Management	**Unmanaged**
Layer	**2**

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