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PM Series

User's Manual

Single Site PMC Carriers for CompactPCI and PCI:

PMA-P, PMB-P, and PMA-C

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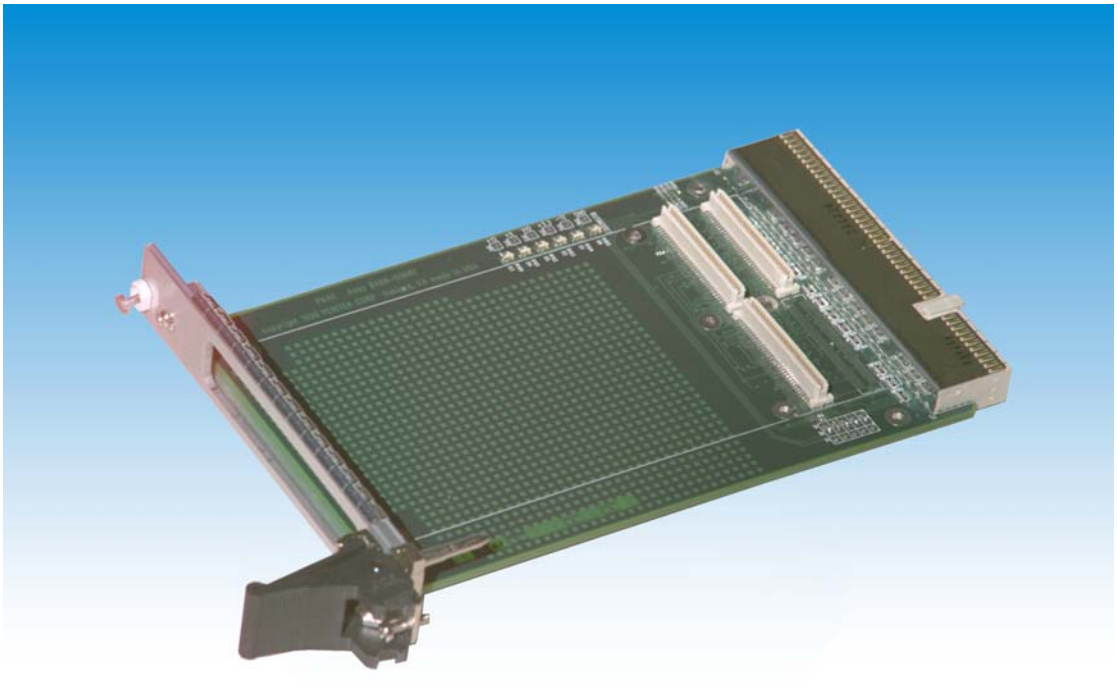
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Introduction

This manual provides information about how to configure, install, and program the Rastergraf PM Series single site PMC Carriers for 32-bit and 64-bit PCI and 3U CompactPCI computers.

This manual is broken down into five chapters:

Chapter 1: General Information
Chapter 2: Specifications
Chapter 3: Connector Pinouts and Cable Information
Chapter 4: Installing Your Rastergraf Graphics Board
Chapter 5: Troubleshooting

Chapter 1 provides background material about the PM Series boards, and it is not essential for the hardware or software installation. If you want to perform the installation as quickly as possible, start with Chapter 4. If you have problems installing the hardware, refer to Chapter 5 for help.

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Getting Help

This installation manual gives specific steps to take to install your Rastergraf board. There are, however, variables specific to your computer configuration and monitor that this manual cannot address. Normally, the default values given in this manual will work. If you have trouble installing or configuring your system, first read Chapter 6, "Troubleshooting". If this information does not enable you to solve your problems, do one of the following:

1) call Rastergraf technical support at (541) 923-5530

2) fax your questions to (541) 923-6475

3) send E-mail to support@rastergraf.com .

Board Revisions

This manual applies to the following board revision levels:

PMA-P Fab Rev 0-3

PMB-P Fab Rev 0-1

PMA-C Fab Rev 0-2

Manual Revisions

Revision 1.0	October 1, 2002	First released version
Revision 1.1	December 2, 2002	Some revisions
Revision 1.2	September 16, 2003	Roll in the PMB-P
Revision 1.3	September 23, 2003	Add info on JTAG header
Revision 1.4	October 9, 2003	Fixed some PMB-P typos
Revision 2.0	March 4, 2008	Rastergraf version

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Notices

Information contained in this manual is disclosed in confidence and may not be duplicated in full or in part by any person without prior approval of Rastergraf. Its sole purpose is to provide the user with adequately detailed documentation to effectively install and operate the equipment supplied. The use of this document for any other purpose is specifically prohibited.

The information in this document is subject to change without notice. The specifications of the PMA-P, PMB-P, and PMA-C PMC Carrier boards and other components described in this manual are subject to change without notice. Although it regrets them, Rastergraf assumes no responsibility for any errors or omissions that may occur in this manual. Customers are advised to verify all information contained in this document.

The electronic equipment described herein generates, uses, and may radiate radio frequency energy, which can cause radio interference. Rastergraf assumes no liability for any damages caused by such interference.

Rastergraf products are **not** authorized for ***any*** use as critical components in flight safety or life support equipment without the written consent of the president of Rastergraf, Inc.

These products have been designed to operate in user-provided PMC-compatible computers. Connection of incompatible hardware is likely to cause serious damage. Rastergraf assumes no liability for any damages caused by such incompatibility.

Rastergraf assumes no responsibility for the use or reliability of software or hardware that is not supplied by Rastergraf, or which has not been installed in accordance with this manual.

The PMA-P, PMB-P, and PMA-C PMC Carrier boards are manufactured and sold under license from Curtiss-Wright Controls Embedded Computing (CWCEC). Contact Rastergraf, Inc. for additional information.

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Conventions Used In This Manual

The following list summarizes the conventions used throughout this manual.

`Code fragments`	Code fragments, file, directory or path names and user/computer dialogs in the manual are presented in the `courier` typeface.
Commands or **program names**	Commands, or the names of executable programs, except those in code fragments, are in bold.
System prompts and commands	Commands in code fragments are preceded by the system prompt, a percentage sign (%), the standard prompt in UNIX's C shell, or the hash-mark (#), the standard UNIX prompt for the Super-User.
Keyboard usage	**<CR>** stands for the key on your keyboard labeled "RETURN" or "ENTER"

Note	Note boxes contain information either specific to one or more platforms, or interesting, background information that is not essential to the installation.

Caution	Caution boxes warn you about actions that can cause damage to your computer or its software.

Warning!	Warning! boxes warn you about actions that can cause bodily or emotional harm.

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Chapter 1
General Information

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1.1 Introduction

The Rastergraf PM Series is part of Rastergraf's line of active and passive interface PMC carriers for PCI and CompactPCI computers

The PM Series mezzanine carrier boards hold one PMC module in a PCI or 3U CompactPCI slot. The PM Series carrier board is ideal for use in high performance industrial, COTS, and telephony CompactPCI systems that require I/O expansion using the PMC module form factor.

The PM Series products include both ***passive*** and ***active*** adapters.

A Rastergraf ***passive*** adapter (e.g. PMA-P or PMA-C) has a direct, bridgeless, 64-bit path between the PCI or CompactPCI connectors and the on-board PMC connectors. Because it has no bridge, no software is required to use the PMA boards.

The PMA boards are fine for 33 MHz applications, and will also work at 66 MHz with many, but not all, PMC boards. This is due to the fact that the PCI traces on a passive carrier necessarily extend well beyond the customary standard PCI peripheral board trace length. At 33 MHz, this is not a problem, but since the timing margins are tighter at 66 MHz, some boards won't work reliably. In this case, an active carrier is required.

A Rastergraf ***active*** adapter has a 64-bit path with a PCI-PCI bridge between the PCI or CompactPCI connectors and the on-board PMC connectors. The active board is needed for applications with more than one PMC site, such as the Rastergraf PMB-C (see PMB-C manual). An active board is such as the PMB-P is intended for use with those PMC boards that will not work at 66 MHz (such as the Rastergraf VSG series graphics boards).

As of the latest board revisions, the PMA and PMB boards comply with the IEEE 1386-2001 PMC specification (***except*** maximum trace length on the PMA boards). The PMA-C CompactPCI carrier board complies with the PICMG 2.0, version 3.0 CompactPCI specification and is also Processor PMC (PrPMC) "friendly".

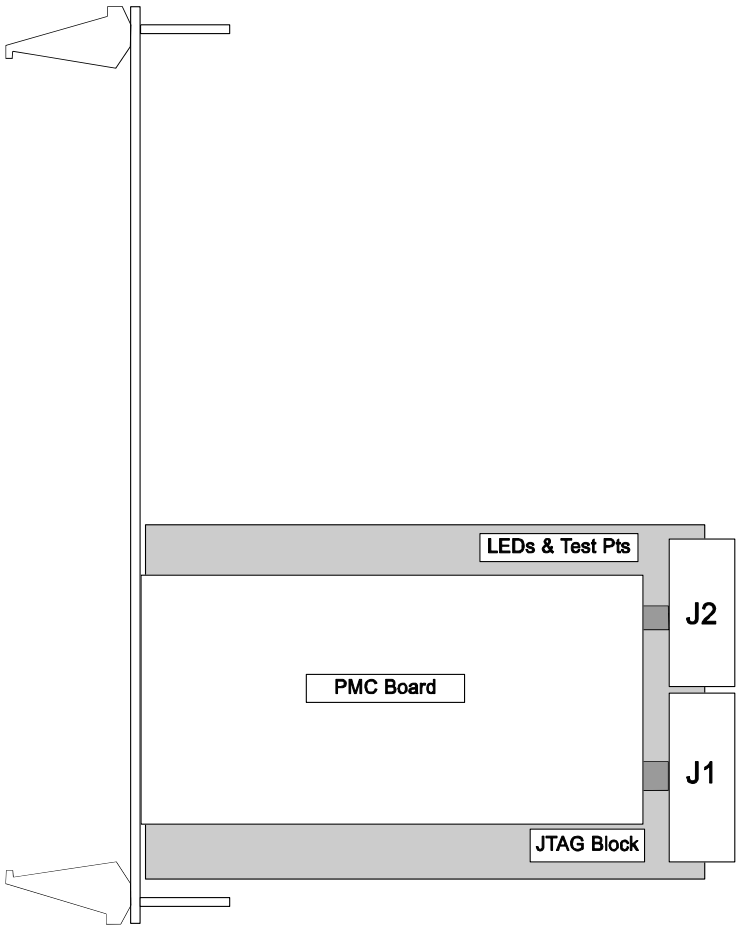
For information about all of Rastergraf's products, please contact Rastergraf Worldwide Sales at (541) 923-5530 or, consult Rastergraf's web page at http://www.rastergraf.com.

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1.2 PMA-C Feature Summary

- 3U CompactPCI carrier board holds one PMC module
- Passive (busless) guarantees total software compatibility
- 32/64-bit, 33/66 MHz operation
- LEDs for VIO, +12, -12, 5, 3.3 power (red) and BUSMODE1 (green)
- Basic support for Processor PMC (PrPMC)
- CompactPCI specification, PICMG 2.0, version 3.0 compliant
- 3U or 6U card handle options for CompactPCI carrier
- Universal PCI signaling
- Optional JTAG Header

Figure 1-1 PMA-C Functional Outline

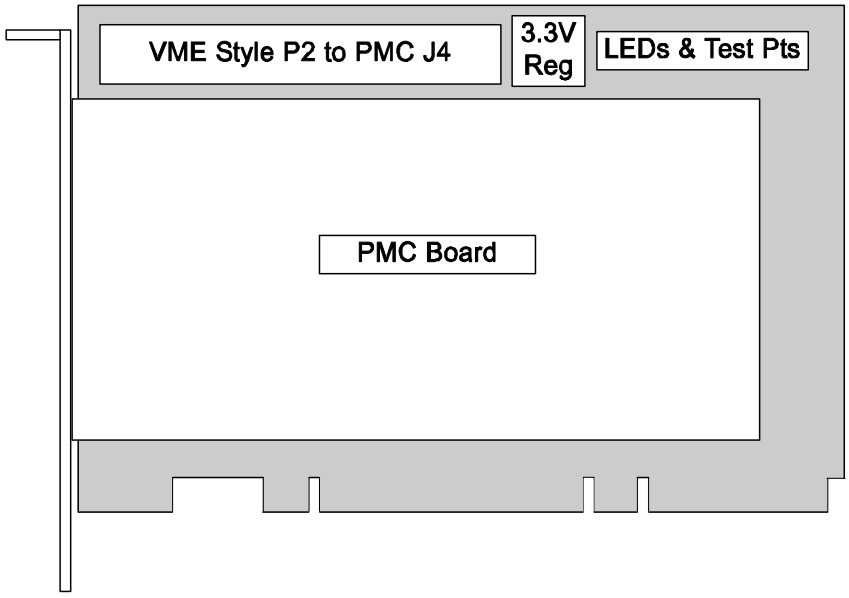


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1.3 PMA-P Feature Summary

- Short PCI carrier board holds one PMC module
- 32/64-bit, 33 MHz operation, restricted 66 MHz (see Section 1.1)
- Passive (busless) guarantees total software compatibility
- LEDs for VIO, +12, -12, 5, 3.3 power (red) and BUSMODE1 (green)
- Supports standard IEEE 1386-2001 PMC mezzanine module
- PCI 2.1 specification compliant (IEEE PMC spec only meets 2.1)
- Optional VME “P2” style I/O connector for PMC J4
- Jumper selectable on-board 3.3V regulator for older PCI systems
- Universal PCI signaling
- Optional JTAG Header

Figure 1-2 PMA-P Functional Outline

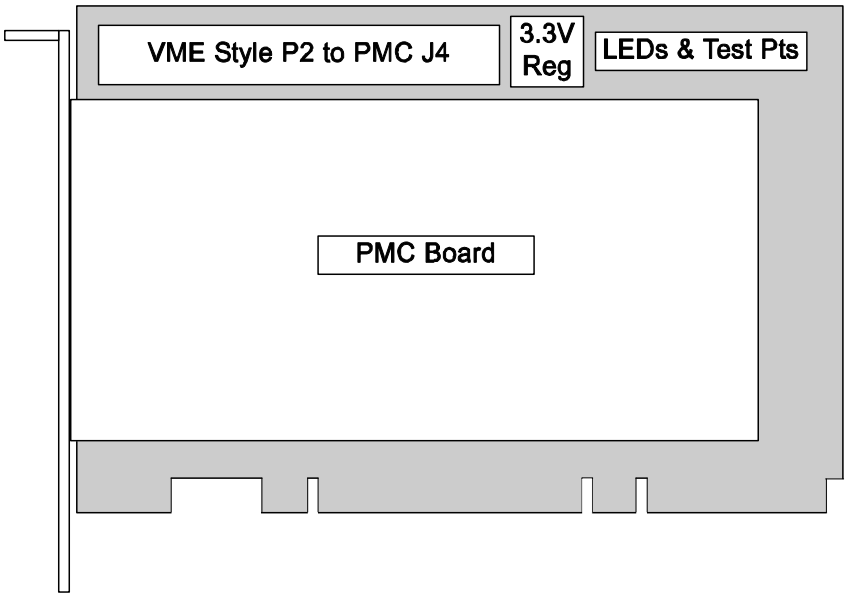


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1.4 PMB-P Feature Summary

- Short PCI carrier board holds one PMC module
- 32/64-bit, 33/66 MHz operation
- Uses PLX PCI6154 Transparent, Async/Sync PCI-PCI Bridge
- Active interface ensures PMC hardware compatibility at 66 MHz
- Programmable clock allows flexible local clock speed settings
- LEDs for VIO, +12, -12, 5, 3.3 power (red) and BUSMODE1 (green)
- Supports standard IEEE 1386-2001 PMC mezzanine module
- PCI 2.1 specification compliant (IEEE PMC spec only meets 2.1)
- Optional VME “P2” style I/O connector for PMC J4
- Jumper selectable on-board 3.3V regulator for older PCI systems
- Universal PCI signaling on both host and local buses
- Optional JTAG Header

Figure 1-3 PMB-P Functional Outline



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1.5 Additional References

You can find Rastergraf documentation and other technical literature on the Rastergraf web page (http://www.rastergraf.com).

The ***CompactPCI Specification – PICMG R2.0 R3.0***, the ***CompactPCI Hot Swap Specification – PICMG 2.1 R2.0*** and the ***CompactPCI Hot Swap Infrastructure Interface Specification PICMG 2.12 R1.0*** standards and other information are available from **PICMG:**

Web Page: http://www.picmg.org/index.stm

The ***PCI Local Bus 2.2 Specification*** is maintained by the **PCI Special Interest Group** (PCISIG)

Web Page: http://www.pcisig.com/home

A lot of the VITA specifications are available from Rastergraf's technical library:

Web Page: http://www.rastergraf.com/standards_library.htm

1156.2-1996:
IEEE Standard for Environmental Specifications for Computer Systems 1996 (includes IEEE 1101)

http://shop.ieee.org/store/product.asp?prodno=SS94426

1386-2001 and 1386.1-2001:
IEEE Standard for a Common Mezzanine Card Family: CMC and IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards

http://shop.ieee.org/store/product.asp?prodno=SS94922

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Chapter 2
Specifications

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2.1 Specifications for the PMA-C

Form Factor:	3U, 166.25 mm x 160 mm
Front Panel Options:	IEEE 1101.10 style, 3U or 6U, specified at order time.
CompactPCI Interface:	Direct CompactPCI to PMC connection via 10 ohm series resistors, 32/64-bit, 33/66 MHz, Universal PCI Signaling.
Indicators:	Red LEDs for VIO, +12V, -12V, +5V, and 3.3V. Green LED for BUSMODE1 (PrPMC PRESENT#) asserted.
Printed Circuit Board:	6 layer. Trace length for standard PCI signals is between 75 and 105 mm. Signals are impedance controlled, verified with SPECCTRA advanced noise rules and simulated with less than 75 mV trace to trace, parallel or layer to layer.
Standards Compatibility:	PICMG 2.0 Rev 3 with ESD control, IEEE 1101.10, IEEE 1386-2001, and PCI Specification Revision 2.2.
Hot Swap Support:	not supported
CompactPCI Bus Loading:	One PCI 2.2 compatible load
PMC Interface	One PMC or PrPMC module.
ProcessorPMC (PrPMC):	Provides support for basic, single IDSEL version of PrPMC. Connects: PrPMC MONARCH# (Pn2-64) to CPCI SYSEN# (J2-C2) PrPMC EREADY (Pn2-58) to CPCI ENUM# (J1-C25) PrPMC RSTOUT# (Pn2-60) to CPCI PRST# (J2-C17)
I/O Access	Front Panel only.
Power Requirements:	+/-12V @ 20 mA each; +5V @ 20 mA; +3.3V @ 50 mA. Additional power is consumed by the PMC module and is NOT current limited by the PMA-C.
Weight	0.26 kg (0.56 lb)
Environmental	Operating temperature: 0 to 70°C Storage: -40 to +85°C Humidity: 5 to 95% non-condensing

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2.2 Specifications for the PMA-P

Form Factor:	Short PCI, standard height: 168.3 mm x 108 mm.
PCI Interface:	Direct connection, 32/64-bit, 33 MHz, restricted 66 MHz (see Section 1.1), Universal PCI Signaling.
Indicators:	Red LEDs for VIO, +12V, -12V, +5V, and 3.3V. Green LED for BUSMODE1 asserted.
Printed Circuit Board:	6 layer stackup. Trace length (connector to connector) for each standard PCI signal is between 75 and 105 mm. Signal traces are impedance controlled, verified with SPECCTRA advanced noise rules and simulated with less than 300 mV trace to trace, parallel or layer to layer.
Standards Compatibility:	IEEE 1386-2001 and PCI Specification Revision 2.2.
PCI Bus Loading:	One PCI 2.2 compatible load
PMC Interface	One PMC module.
I/O Access	Front Panel or optional VME-style P2 connector.
Power Requirements:	+/-12V @ 20 mA each; +5V @ 20 mA; +3.3V @ 50 mA. Additional power is consumed by the PMC module and is NOT current limited by the PMA-P.
Onboard 3.3V Regulator:	Non-ATX PCI systems do not usually supply 3.3V. Therefore, the PMA-P has an on-board, 3.3V @ 3A linear regulator that can be jumpered in. Note that it will drive the 3.3V pins on the connector.
Weight	0.26 kg (0.56 lb)
Environmental	Operating temperature: 0 to 70°C Storage: -40 to +85°C Humidity: 5 to 95% non-condensing

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2.3 Specifications for the PMB-P

Form Factor:	Short PCI, standard height: 168.3 mm x 108 mm.
PCI Interface:	32/64-bit, 33/66 MHz. Uses a PLX PCI6154 Transparent, Async/Sync PCI-PCI Bridge with universal PCI Signaling on both host and local buses. A combination of jumper and I^2C programmable options allows local clock to be async or sync to the host and range from of 1:1 to 1:2.5 of host clock.
Indicators:	Red LEDs for Local and Host VIO, +12V, -12V, +5V, and 3.3V. Green LED for BUSMODE1 asserted.
Printed Circuit Board:	6 layer stackup. Trace length (host connector to bridge) for each standard PCI signal is less than 40 mm. Signal traces are impedance controlled, verified with SPECCTRA advanced noise rules and simulated with less than 300 mV trace to trace, parallel or layer to layer.
Standards Compatibility:	IEEE 1386-2001 and PCI Specification Revision 2.2.
PCI Bus Loading:	One PCI 2.2 compatible load
PMC Interface	One PMC module.
I/O Access	Front Panel or optional VME-style P2 connector.
Power Requirements:	+/-12V @ 20 mA each; +5V @ 20 mA; +3.3V @ 50 mA. Additional power is consumed by the PMC module and is NOT current limited by the PMB-P.
Onboard 3.3V Regulator:	Non-ATX PCI systems do not usually supply 3.3V. Therefore, the PMB-P has an on-board, 3.3V @ 3A linear regulator that can be jumpered in. Note that it will drive the 3.3V pins on the connector.
Weight	0.26 kg (0.56 lb)
Environmental	Operating temperature: 0 to 70°C Storage: -40 to +85°C Humidity: 5 to 95% non-condensing

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2.4 Ordering Options

2.4.1 PMA-C

3U Front Panel (/3U)

The PMA-C is physically a 3U CompactPCI board. However, it can be used in 6U or 3U systems. The standard board comes with a 6U panel.

JTAG Header (/JTAG)

If the PMA-C is to be used with a PrPMC or other PMC card that uses the JTAG connections, then it may be desirable to order the JTAG option.

This option removes the hardwired connections between the CompactPCI and PMC JTAG lines. A three-row header is installed which allows the CompactPCI and PMC JTAG lines to be connected with shunts. These can be removed to allow a JTAG cable to connect to the PMC board.

2.4.2 PMA-P and PMB-P

JTAG Header (/JTAG)

If the PMA-P or PMB-P is to be used with a PrPMC or other PMC card that uses the JTAG connections, then it may be desirable to order the JTAG option.

This option removes the hardwired connections between the PCI and PMC JTAG lines. A three-row header is installed which allows the PCI and PMC JTAG lines to be connected with shunts. These can be removed to allow a JTAG cable to connect to the PMC board.

VME-Style P2 Connector (/P2)

The PMA-P and PMB-P can be supplied with a VME P2-style header which breaks out the PMC Pn4 (I/O) connections into a ANSI/Vita 35 compatible pinout.

Note that the /P2 option ***includes the /JTAG option***.

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Chapter 3
Connector Pinouts

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3.1 PMA-C Connectors

3.1.1 CompactPCI Bus J1 Connector

Position	A	B	C	D	E	F
1	VCC (5V)	-12V	n/c	+12V	VCC (5V)	GND
2	n/c	VCC (5V)	n/c	TDOH	TDIH	GND
3	INTA#	INTB#	INTC#	VCC (5V)	INTD#	GND
4	n/c	HEALTHY#	VIO	n/c	n/c	GND
5	n/c	n/c	RST#	GND	GNT#	GND
6	REQ#	GND	VDD (3.3V)	CLK	AD[31]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
8	AD[26]	GND	VIO	AD[25]	AD[24]	GND
9	CBE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
10	AD[21]	GND	VDD (3.3V)	AD[20]	AD[19]	GND
11	AD[18]	AD[17]	AD[16]	GND	CBE[2]#	GND
12	keyway	keyway	keyway	keyway	keyway	keyway
13	keyway	keyway	keyway	keyway	keyway	keyway
14	keyway	keyway	keyway	keyway	keyway	keyway
15	VDD (3.3V)	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
16	DEVSEL#	GND	VIO	STOP#	LOCK#	GND
17	VDD (3.3V)	SMB_SCL	SMB_SDA	GND	PERR#	GND
18	SERR#	GND	VDD (3.3V)	PAR	CBE[1]#	GND
19	VDD (3.3V)	AD[15]	AD[14]	GND	AD[13]	GND
20	AD[12]	GND	VIO	AD[11]	AD[10]	GND
21	VDD (3.3V)	AD[09]	AD[08]	M66EN	CBE[0]#	GND
22	AD[07]	GND	VDD (3.3V)	AD[06]	AD[05]	GND
23	VDD (3.3V)	AD[04]	AD[03]	VCC (5V)	AD[02]	GND
24	AD[01]	VCC (5V)	VIO	AD[00]	ACK64#	GND
25	VCC (5V)	REQ64#	ENUM#	VDD (3.3V)	VCC (5V)	GND

Note: PrPMC EREADY (Pn2-58) to CPCI ENUM# (J1-C25)

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3.1.2 CompactPCI Bus J2 Connector

Position	A	B	C	D	E	F
1	n/c	GND	n/c	n/c	n/c	GND
2	n/c	n/c	SYSEN#	n/c	n/c	GND
3	n/c	GND	n/c	n/c	n/c	GND
4	VIO	GND	C/BE[7]#	GND	C/BE[6]#	GND
5	C/BE[5]#	64EN#	VIO	C/BE[4]#	PAR64	GND
6	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
7	AD[59]	GND	VIO	AD[58]	AD[57]	GND
8	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
9	AD[52]	GND	VIO	AD[51]	AD[50]	GND
10	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
11	AD[45]	GND	VIO	AD[44]	AD[43]	GND
12	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
13	AD[38]	GND	VIO	AD[37]	AD[36]	GND
14	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
15	n/c	GND	n/c	n/c	n/c	GND
16	n/c	n/c	n/c	GND	n/c	GND
17	n/c	GND	PRST#	n/c	n/c	GND
18	n/c	n/c	n/c	GND	n/c	GND
19	n/c	n/c	n/c	n/c	n/c	GND
20	n/c	n/c	n/c	GND	n/c	GND
21	n/c	n/c	n/c	n/c	n/c	GND
22	GA4	GA3	GA2	GA1	GA0	GND

Note: PrPMC MONARCH# (Pn2-64) to CPCI SYSEN# (J2-C2)
PrPMC RSTOUT# (Pn2-60) to CPCI PRST# (J2-C17)

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3.1.3 PMC Bus Connector – J1

Pin	Notes	PMC/ PrPMC		PMC/ PrPMC	Notes	Pin
1		TCK		-12V		2
3		GND		INTAL		4
5		INTBL		INTCL		6
7		BUSMD1L	PRSNTL	VCC (5V)		8
9		INTDL		PCI-RSVD	N/C	10
11		GND		3.3Vaux	N/C	12
13		PCICLK		GND		14
15		GND		PMCGNTL		16
17		PMCREQL		VCC (5V)		18
19		Vio		AD31H		20
21		AD28H		AD27H		22
23		AD25H		GND		24
25		GND		C/BE3L		26
27		AD22H		AD21H		28
29		AD19H		VCC (5V)		30
31		Vio		AD17H		32
33		FRAMEL		GND		34
35		GND		IRDYL		36
37		DEVSELL		VCC (5V)		38
39		GND		LOCKL		40
41	N/C	PCI-RSVD		PCI-RSVD	N/C	42
43		PAR		GND		44
45		Vio		AD15H		46
47		AD12H		AD11H		48
49		AD09H		VCC (5V)		50
51		GND		C/BE0L		52
53		AD06H		AD05		54
55		AD04H		GND		56
57		Vio		AD03H		58
59		AD02H		AD01H		60
61		AD00H		VCC (5V)		62
63		GND		REQ64L		64

Color means PrPMC usage

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3.1.4 PMC Bus Connector – J2

Pin	Notes	PMC/ PrPMC		PMC/ PrPMC		Notes	Pin
1		+12V		TRSTL			2
3		TMSH		TDOH			4
5		TDIH		GND			6
7		GND		PCI_RSVD		N/C	8
9		PCI_RSVD		PCI_RSVD		N/C	10
11	PUP	BUSMODE2L	PUP	VDD (3.3V)			12
13		PCIRSTL		BUSMODE3L	PDN	PDN	14
15		VDD (3.3V)		BUSMODE4L	PDN	PDN	16
17	N/C	PMEL		GND			18
19		AD30H		AD29H			20
21		GND		AD26H			22
23		AD24H		VDD (3.3V)			24
25		IDSEL		AD23H			26
27		VDD (3.3V)		AD20H			28
29		AD18H		GND			30
31		AD16H		C/BE2L			32
33		GND		PMC_RSVD		N/C	34
35		TRDYL		VDD (3.3V)			36
37		GND		STOPL			38
39		PERRL		GND			40
41		VDD (3.3V)		SERRL			42
43		C/BE1L		GND			44
45		AD14H		AD13H			46
47		GND		AD10H			48
49		AD08H		VDD (3.3V)			50
51		AD07H		PMC_RSVD		N/C	52
53		VDD (3.3V)		PMC_RSVD		N/C	54
55	N/C	PMC_RSVD		GND			56
57	N/C	PMC_RSVD		PMC_RSVD	N/C	EREADY	58
59		GND		PMC_RSVD	N/C	RSTOUT#	60
61		ACK64L		VDD (3.3V)			62
63		GND		PMC_RSVD	N/C	MONARCH#	64

PDN means pull down resistor to ground. PUP means pull up resistor to VIO

Color means PrPMC usage

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3.1.5 PMC Bus Connector – J3

Pin	Notes	Signal Name	Signal Name	Notes	Pin
1	N/C	RSVD-B63	GND		2
3		GND	C/BE7L		4
5		C/BE6L	C/BE5L		6
7		C/BE4L	GND		8
9		Vio	PAR64H		10
11		AD63H	AD62H		12
13		AD61H	GND		14
15		GND	AD60H		16
17		AD59H	AD58H		18
19		AD57H	GND		20
21		Vio	AD56H		22
23		AD55H	AD54H		24
25		AD53H	GND		26
27		GND	AD52H		28
29		AD51H	AD50H		30
31		AD49H	GND		32
33		GND	AD48H		34
35		AD47H	AD46H		36
37		AD45H	GND		38
39		Vio	AD44H		40
41		AD43H	AD42H		42
43		AD41H	GND		44
45		GND	AD40H		46
47		AD39H	AD38H		48
49		AD37H	GND		50
51		GND	AD36H		52
53		AD35H	AD34H		54
55		AD33H	GND		56
57		Vio	AD32H		58
59	N/C	RSVD-A92	RSVD-B92	N/C	60
61	N/C	RSVD-B93	GND		62
63		GND	RSVD-A94	N/C	64

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3.1.6 PMC Bus Connector – J4

The pinout is listed here but it is not connected to anything.

Pin	Signal Name	Signal Name	Pin
1	PMC-J4_IO1	PMC-J4_IO2	2
3	PMC-J4_IO3	PMC-J4_IO4	4
5	PMC-J4_IO5	PMC-J4_IO6	6
7	PMC-J4_IO7	PMC-J4_IO8	8
9	PMC-J4_IO9	PMC-J4_IO10	10
11	PMC-J4_IO11	PMC-J4_IO12	12
13	PMC-J4_IO13	PMC-J4_IO14	14
15	PMC-J4_IO15	PMC-J4_IO16	16
17	PMC-J4_IO17	PMC-J4_IO18	18
19	PMC-J4_IO19	PMC-J4_IO20	20
21	PMC-J4_IO21	PMC-J4_IO22	22
23	PMC-J4_IO23	PMC-J4_IO24	24
25	PMC-J4_IO25	PMC-J4_IO26	26
27	PMC-J4_IO27	PMC-J4_IO28	28
29	PMC-J4_IO29	PMC-J4_IO30	30
31	PMC-J4_IO31	PMC-J4_IO32	32
33	PMC-J4_IO33	PMC-J4_IO34	34
35	PMC-J4_IO35	PMC-J4_IO36	36
37	PMC-J4_IO37	PMC-J4_IO38	38
39	PMC-J4_IO39	PMC-J4_IO40	40
41	PMC-J4_IO41	PMC-J4_IO42	42
43	PMC-J4_IO43	PMC-J4_IO44	44
45	PMC-J4_IO45	PMC-J4_IO46	46
47	PMC-J4_IO47	PMC-J4_IO48	48
49	PMC-J4_IO49	PMC-J4_IO50	50
51	PMC-J4_IO51	PMC-J4_IO52	52
53	PMC-J4_IO53	PMC-J4_IO54	54
55	PMC-J4_IO55	PMC-J4_IO56	56
57	PMC-J4_IO57	PMC-J4_IO58	58
59	PMC-J4_IO59	PMC-J4_IO60	60
61	PMC-J4_IO61	PMC-J4_IO62	62
63	PMC-J4_IO63	PMC-J4_IO64	64

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3.2 PMA-P and PMB-P Connectors

3.2.1 PCI Bus 32-Bit Connector

Pin	Signal Name
A1	TRST
A2	+12V
A3	TMS
A4	TDI
A5	VCC (5V)
A6	INTA#
A7	INTC#
A8	VCC (5V)
A9	RSVD-A09
A10	VIO
A11	RSVD-A11
A12	[KEY]
A13	[KEY]
A14	3.3Vaux
A15	PCIRST#
A16	VIO
A17	GNT#
A18	GND
A19	PMEL
A20	AD[30]
A21	VDD (3.3V)
A22	AD[28]
A23	AD[26]
A24	GND
A25	AD[24]
A26	IDSEL
A27	VDD (3.3V)
A28	AD[22]
A29	AD[20]
A30	GND
A31	AD[18]
A32	AD[16]

Signal Name	Pin
-12V	B1
TCK	B2
GND	B3
TDO	B4
VCC (5V)	B5
VCC (5V)	B6
INTB#	B7
INTD#	B8
PRSNT1#	B9
RSVD-B10	B10
PRSNT2#	B11
[KEY]	B12
[KEY]	B13
RSVD-B14	B14
GND	B15
PCICLK	B16
GND	B17
REQ#	B18
VIO	B19
AD[31]	B20
AD[29]	B21
GND	B22
AD[27]	B23
AD[25]	B24
VDD (3.3V)	B25
CBE[3]#	B26
AD[23]	B27
GND	B28
AD[21]	B29
AD[19]	B30
VDD (3.3V)	B31
AD[17]	B32

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3.2.1 PCI Bus 32-Bit Connector (continued)

Pin	Signal Name	Signal Name	Pin
A33	VDD (3.3V)	CBE[2]#	B33
A34	FRAME#	GND	B34
A35	GND	IRDY#	B35
A36	TRDY#	VDD (3.3V)	B36
A37	GND	DEVSEL#	B37
A38	STOP#	GND	B38
A39	VDD (3.3V)	LOCK#	B39
A40	RSVD-A40	PERR#	B40
A41	RSVD-A41	VDD (3.3V)	B41
A42	GND	SERR#	B42
A43	PAR	VDD (3.3V)	B43
A44	AD[15]	CBE[1]#	B44
A45	VDD (3.3V)	AD[14]	B45
A46	AD[13]	GND	B46
A47	AD[11]	AD[12]	B47
A48	GND	AD[10]	B48
A49	AD[09]	M66EN	B49
A50	[KEY]	[KEY]	B50
A51	[KEY]	[KEY]	B51
A52	CBE[0]#	AD[08]	B52
A53	VDD (3.3V)	AD[07]	B53
A54	AD[06]	VDD (3.3V)	B54
A55	AD[04]	AD[05]	B55
A56	GND	AD[03]	B56
A57	AD[02]	GND	B57
A58	AD[00]	AD[01]	B58
A59	VIO	VIO	B59
A60	REQ64#	ACK64#	B60
A61	VCC (5V)	VCC (5V)	B61
A62	VCC (5V)	VCC (5V)	B62
	[KEY]	[KEY]	
	[KEY]	[KEY]	

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3.2.2 PCI Bus 64-Bit Connector

Pin	Signal Name	Signal Name	Pin
A63	GND	RSVD-B63	B63
A64	CBE[7]#	GND	B64
A65	CBE[5]#	CBE[6]#	B65
A66	VIO	CBE[4]#	B66
A67	PAR64	GND	B67
A68	AD[62]	AD[63]	B68
A69	GND	AD[61]	B69
A70	AD[60]	VIO	B70
A71	AD[58]	AD[59]	B71
A72	GND	AD[57]	B72
A73	AD[56]	GND	B73
A74	AD[54]	AD[55]	B74
A75	VIO	AD[53]	B75
A76	AD[52]	GND	B76
A77	AD[50]	AD[51]	B77
A78	GND	AD[49]	B78
A79	AD[48]	VIO	B79
A80	AD[46]	AD[47]	B80
A81	GND	AD[45]	B81
A82	AD[44]	GND	B82
A83	AD[42]	AD[43]	B83
A84	VIO	AD[41]	B84
A85	AD[40]	GND	B85
A86	AD[38]	AD[39]	B86
A87	GND	AD[37]	B87
A88	AD[36]	VIO	B88
A89	AD[34]	AD[35]	B89
A90	GND	AD[33]	B90
A91	AD[32]	GND	B91
A92	RSVD-A92	RSVD-B92	B92
A93	GND	RSVD-B93	B93
A94	RSVD-A94	GND	B94

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3.2.3 PMC Bus Connector – J1

Pin	Notes	Signal Name	Signal Name	Notes	Pin
1		TCK	-12V		2
3		GND	INTA#		4
5		INTB#	INTC#		6
7		BUSMODE1#	VCC (5V)		8
9		INTDL	RSVD-B14		10
11		GND	3.3Vaux		12
13		PCICLK	GND		14
15		GND	GNT#		16
17		REQ#	VCC (5V)		18
19		VIO	AD[31]		20
21		AD[28]	AD[27]		22
23		AD[25]	GND		24
25		GND	CBE[3]#		26
27		AD[22]	AD[21]		28
29		AD[19]	VCC (5V)		30
31		VIO	AD[17]		32
33		FRAME#	GND		34
35		GND	IRDY#		36
37		DEVSEL#	VCC (5V)		38
39		GND	LOCK#		40
41		RSVD-A40	RSVD-A41		42
43		PAR	GND		44
45		VIO	AD[15]		46
47		AD[12]	AD[11]		48
49		AD[09]	VCC (5V)		50
51		GND	C/BE[0]#		52
53		AD[06]	AD[05]		54
55		AD[04]	GND		56
57		VIO	AD[03]		58
59		AD[02]	AD[01]		60
61		AD[00]	VCC (5V)		62
63		GND	REQ64#		64

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3.2.4 PMC Bus Connector – J2

Pin	Notes	Signal Name	Signal Name	Notes	Pin
1		+12V	TRST#		2
3		TMS	TDO		4
5		TDI	GND		6
7		GND	RSVD-A09		8
9		RSVD-B10	RSVD-A11		10
11		BUSMODE2#	VDD (3.3V)		12
13		PCIRST#	BUSMODE3#		14
15		VDD (3.3V)	BUSMODE4#		16
17		PME#	GND		18
19		AD[30]	AD[29]		20
21		GND	AD[26]		22
23		AD[24]	VDD (3.3V)		24
25		IDSEL	AD[23]		26
27		VDD (3.3V)	AD[20]		28
29		AD[18]	GND		30
31		AD[16]	CBE[2]#		32
33		GND	PMC_RSVD	NC	34
35		TRDY#	VDD (3.3V)		36
37		GND	STOP#		38
39		PERR#	GND		40
41		VDD (3.3V)	SERR#		42
43		CBE[1]#	GND		44
45		AD[14]	AD[13]		46
47		GND	AD[10]		48
49		AD[08]	VDD (3.3V)		50
51		AD[07]	PMC_RSVD	NC	52
53		VDD (3.3V)	PMC_RSVD	NC	54
55	NC	PMC_RSVD	GND		56
57	NC	PMC_RSVD	PMC_RSVD	NC	58
59		GND	PMC_RSVD	NC	60
61		ACK64#	VDD (3.3V)		62
63		GND	PMC_RSVD	NC	64

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3.2.5 PMC Bus Connector – J3

Pin	Notes	Signal Name	Signal Name	Notes	Pin
1		RSVD-B63	GND		2
3		GND	CBE[7]#		4
5		CBE[6]#	CBE[5]#		6
7		CBE[4]#	GND		8
9		VIO	PAR64		10
11		AD[63]	AD[62]		12
13		AD[61]	GND		14
15		GND	AD[60]		16
17		AD[59]	AD[58]		18
19		AD[57]	GND		20
21		VIO	AD[56]		22
23		AD[55]	AD[54]		24
25		AD[53]	GND		26
27		GND	AD[52]		28
29		AD[51]	AD[50]		30
31		AD[49]	GND		32
33		GND	AD[48]		34
35		AD[47]	AD[46]		36
37		AD[45]	GND		38
39		VIO	AD[44]		40
41		AD[43]	AD[42]		42
43		AD[41]	GND		44
45		GND	AD[40]		46
47		AD[39]	AD[38]		48
49		AD[37]	GND		50
51		GND	AD[36]		52
53		AD[35]	AD[34]		54
55		AD[33]	GND		56
57		VIO	AD[32]		58
59		RSVD-A92	RSVD-B92		60
61		RSVD-B93	GND		62
63		GND	RSVD-A94		64

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3.2.6 PMC Bus Connector – J4

PMC-J4 Pin	Signal Name	Signal Name	PMC-J4 Pin
1	PMC-J4_IO1	PMC-J4_IO2	2
3	PMC-J4_IO3	PMC-J4_IO4	4
5	PMC-J4_IO5	PMC-J4_IO6	6
7	PMC-J4_IO7	PMC-J4_IO8	8
9	PMC-J4_IO9	PMC-J4_IO10	10
11	PMC-J4_IO11	PMC-J4_IO12	12
13	PMC-J4_IO13	PMC-J4_IO14	14
15	PMC-J4_IO15	PMC-J4_IO16	16
17	PMC-J4_IO17	PMC-J4_IO18	18
19	PMC-J4_IO19	PMC-J4_IO20	20
21	PMC-J4_IO21	PMC-J4_IO22	22
23	PMC-J4_IO23	PMC-J4_IO24	24
25	PMC-J4_IO25	PMC-J4_IO26	26
27	PMC-J4_IO27	PMC-J4_IO28	28
29	PMC-J4_IO29	PMC-J4_IO30	30
31	PMC-J4_IO31	PMC-J4_IO32	32
33	PMC-J4_IO33	PMC-J4_IO34	34
35	PMC-J4_IO35	PMC-J4_IO36	36
37	PMC-J4_IO37	PMC-J4_IO38	38
39	PMC-J4_IO39	PMC-J4_IO40	40
41	PMC-J4_IO41	PMC-J4_IO42	42
43	PMC-J4_IO43	PMC-J4_IO44	44
45	PMC-J4_IO45	PMC-J4_IO46	46
47	PMC-J4_IO47	PMC-J4_IO48	48
49	PMC-J4_IO49	PMC-J4_IO50	50
51	PMC-J4_IO51	PMC-J4_IO52	52
53	PMC-J4_IO53	PMC-J4_IO54	54
55	PMC-J4_IO55	PMC-J4_IO56	56
57	PMC-J4_IO57	PMC-J4_IO58	58
59	PMC-J4_IO59	PMC-J4_IO60	60
61	PMC-J4_IO61	PMC-J4_IO62	62
63	PMC-J4_IO63	PMC-J4_IO64	64

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3.2.7 Optional VME-Style P2 Connector (based on ANSI/Vita 35)

VME-P2 Pin	Signal Name	VME-P2 Pin	Signal Name	VME-P2 Pin	Signal Name
P2-1C	PMC-J4_IO1	P2-1B	VCC	P2-1A	PMC-J4_IO2
P2-2C	PMC-J4_IO3	P2-2B	GND	P2-2A	PMC-J4_IO4
P2-3C	PMC-J4_IO5	P2-3B		P2-3A	PMC-J4_IO6
P2-4C	PMC-J4_IO7	P2-4B		P2-4A	PMC-J4_IO8
P2-5C	PMC-J4_IO9	P2-5B		P2-5A	PMC-J4_IO10
P2-6C	PMC-J4_IO11	P2-6B		P2-6A	PMC-J4_IO12
P2-7C	PMC-J4_IO13	P2-7B		P2-7A	PMC-J4_IO14
P2-8C	PMC-J4_IO15	P2-8B		P2-8A	PMC-J4_IO16
P2-9C	PMC-J4_IO17	P2-9B		P2-9A	PMC-J4_IO18
P2-10C	PMC-J4_IO19	P2-10B		P2-10A	PMC-J4_IO20
P2-11C	PMC-J4_IO21	P2-11B		P2-11A	PMC-J4_IO22
P2-12C	PMC-J4_IO23	P2-12B	GND	P2-12A	PMC-J4_IO24
P2-13C	PMC-J4_IO25	P2-13B	VCC	P2-13A	PMC-J4_IO26
P2-14C	PMC-J4_IO27	P2-14B		P2-14A	PMC-J4_IO28
P2-15C	PMC-J4_IO29	P2-15B		P2-15A	PMC-J4_IO30
P2-16C	PMC-J4_IO31	P2-16B		P2-16A	PMC-J4_IO32
P2-17C	PMC-J4_IO33	P2-17B		P2-17A	PMC-J4_IO34
P2-18C	PMC-J4_IO35	P2-18B		P2-18A	PMC-J4_IO36
P2-19C	PMC-J4_IO37	P2-19B		P2-19A	PMC-J4_IO38
P2-20C	PMC-J4_IO39	P2-20B		P2-20A	PMC-J4_IO40
P2-21C	PMC-J4_IO41	P2-21B		P2-21A	PMC-J4_IO42
P2-22C	PMC-J4_IO43	P2-22B	GND	P2-22A	PMC-J4_IO44
P2-23C	PMC-J4_IO45	P2-23B		P2-23A	PMC-J4_IO46
P2-24C	PMC-J4_IO47	P2-24B		P2-24A	PMC-J4_IO48
P2-25C	PMC-J4_IO49	P2-25B		P2-25A	PMC-J4_IO50
P2-26C	PMC-J4_IO51	P2-26B		P2-26A	PMC-J4_IO52
P2-27C	PMC-J4_IO53	P2-27B		P2-27A	PMC-J4_IO54
P2-28C	PMC-J4_IO55	P2-28B		P2-28A	PMC-J4_IO56
P2-29C	PMC-J4_IO57	P2-29B		P2-29A	PMC-J4_IO58
P2-30C	PMC-J4_IO59	P2-30B		P2-30A	PMC-J4_IO60
P2-31C	PMC-J4_IO61	P2-31B	GND	P2-31A	PMC-J4_IO62
P2-32C	PMC-J4_IO63	P2-32B	VCC	P2-32A	PMC-J4_IO64

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3.3 JTAG Connections (all boards)

Position	JP2	JP1-A	JP1-B	PMA-C JP2-JP1A Jumpers	PMA-P JP2-JP1A Jumpers	PMB-P JP2-JP1A Jumpers
1	PCI_TCK	PMC_TCK	n/c	etch	etch	etch
2	PCI_TMS	PMC_TMS	GND	etch	etch	etch
3	PCI_TDI	PMC _TDI	VCC	etch	etch	etch
4	PCI_TDO	PMC _TDO	GND	etch	etch	etch
5	PCI_TRST#	PMC _TRST#	n/c	etch	etch	etch

To use the JTAG:

No JTAG Header installed

a) cut the etch traces between JP1A (JP1 pins 1, 3, 5, 7, 9) and JP2.

b) install a .1” 2 x 5 header in location JP1.

c) note that this operation isolates the PMC JTAG from the PCI JTAG.

JTAG Header installed

a) remove shunts between JP1A (JP1 pins 1, 3, 5, 7, 9) and JP2.

b) plug application JTAG cable into JP1.

c) note that this operation isolates the PMC JTAG from the PCI JTAG.

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Chapter 4
Installing Your PM Series Board

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4.1 Introduction

Using the PM Series necessarily involves some system integration issues. The PM Series is a carrier for PMC cards, so, of course, you have to know what you are putting on the PM Series.

It is beyond the scope of this manual to deal with selection and use of PMC modules, solving I/O problems, or software. There are several steps involved in getting your PM Series board to work in your system.

- Unpack the PM Series board
- Install the PMC module
- Install the PM Series board

4.2 Unpacking Your Board

When you unpack your board, inspect the contents to see if any damage occurred in shipping. If there has been physical damage, file a claim with the carrier at once and contact Rastergraf for information regarding repair or replacement. Do not attempt to use damaged equipment.

> **Caution**
>
> Be careful not to remove the board from its antistatic bag or container until you are ready to install it. It is preferable to wear a grounded wrist strap whenever handling computer boards.

The PM Series includes both CompactPCI and PCI board form factors. In order to ease the procedure, there follows individual sections that deal with each board type.

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4.3 PCI Bus Signaling Level (VIO)

The PCI bus I/O voltage (VIO) can be operated either at 3.3V or 5V signaling, which determines the voltage level for a “high” or “one” in the PCI bus signal transitions.

The PCI specification requires 66 MHz systems to use 3.3V in order to improve system performance. 33 MHz systems may use either 3.3V or 5V.

Many current ICs are 5V tolerant and even if nominally 3.3V devices, they can tolerate 5V. Some devices support “Universal PCI” operation which means they do sense whether VIO is 3.3V or 5V.

A keying pin can be used to control whether a 3.3V or 5V VIO compatible board can be installed. This method depends on the PMC card having a matching hole. Note that if the PMC card has 2 keying holes, it is “Universal PCI” board.

Although it is beyond the scope of this manual tell you how to change you system to 3.3 or 5V signaling, make sure that it is set to 3.3V if you are running at 66 MHz. Please consult the backplane documentation for information on how to do this.

4.3.1 PMA-P and PMA-C

Since the PM Series are connected directly to the PCI bus, the signaling level for the PMC module is determined by the host bus VIO setting. The PMA-P and PMA-P do not enforce a particular signaling voltage, and, because they have both 5V and 3.3V PMC signaling holes, they are called “Universal PCI” compatible.

4.3.2 PMB-P

Unlike the PMA boards, the PMB-P does have a bridge, and as such, really does have a local PCI bus. The bridge will work at 3.3V or 5V signaling, hence it is “Universal PCI” compatible (see Section 4.6.5 for more information).

Note that if you are running at 66 MHz, you must set the board’s local VIO to 3.3V.

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4.4 Preparing for Installation of the PMA-C

Changing Jumpers on the PMA-C

In the following subsections, please refer ***Figure 4-1*** for jumper locations.

4.4.1 66 MHz Enable

The M66EN signal was introduced in PCI Specification 2.1 and PMC Specification IEEE 1386-2001 to enable PMC and CompactPCI boards to report that a module can run at 66 MHz. System software can then correctly configure the local CompactPCI bus system clocks.

Note that to run at 66 MHz, ALL devices connected to the bus MUST be 66 MHz capable. M66EN was a ground pin on the earlier revision IEEE 1386.1 PMC boards, so if you think that your system SHOULD run at 66 MHz but doesn't, some board may be grounding M66EN. Also, prior to PMA-C Revision 2, M66EN was grounded with a 0 Ohm resistor, R108. Now, with PMA-C Rev 2, the PMC module alone controls it. Since M66EN may be grounded on an older PMC module in the PMA-C, you will have to cut the trace grounding this pin on the PMC module to fix this. Of course, make sure that the module really will run at 66 MHz.

4.4.2 JA-JC JTAG and JEDEC Programming Jumpers

The PMA-C can be used with a standard Lattice JEDEC programming cable to program PLDs connected to a PMC module's JTAG loop. Many Rastergraf boards use this convention. A 2 x 5 .1" header can be installed in location JB-JCs. By default, cPCI host bus JTAG pins loop through the PMA-C board and bypass the PMC module. The JTAG pins are connected together (JA to JB). As of Fab Rev 2, this is done with etch jumpers instead of wires

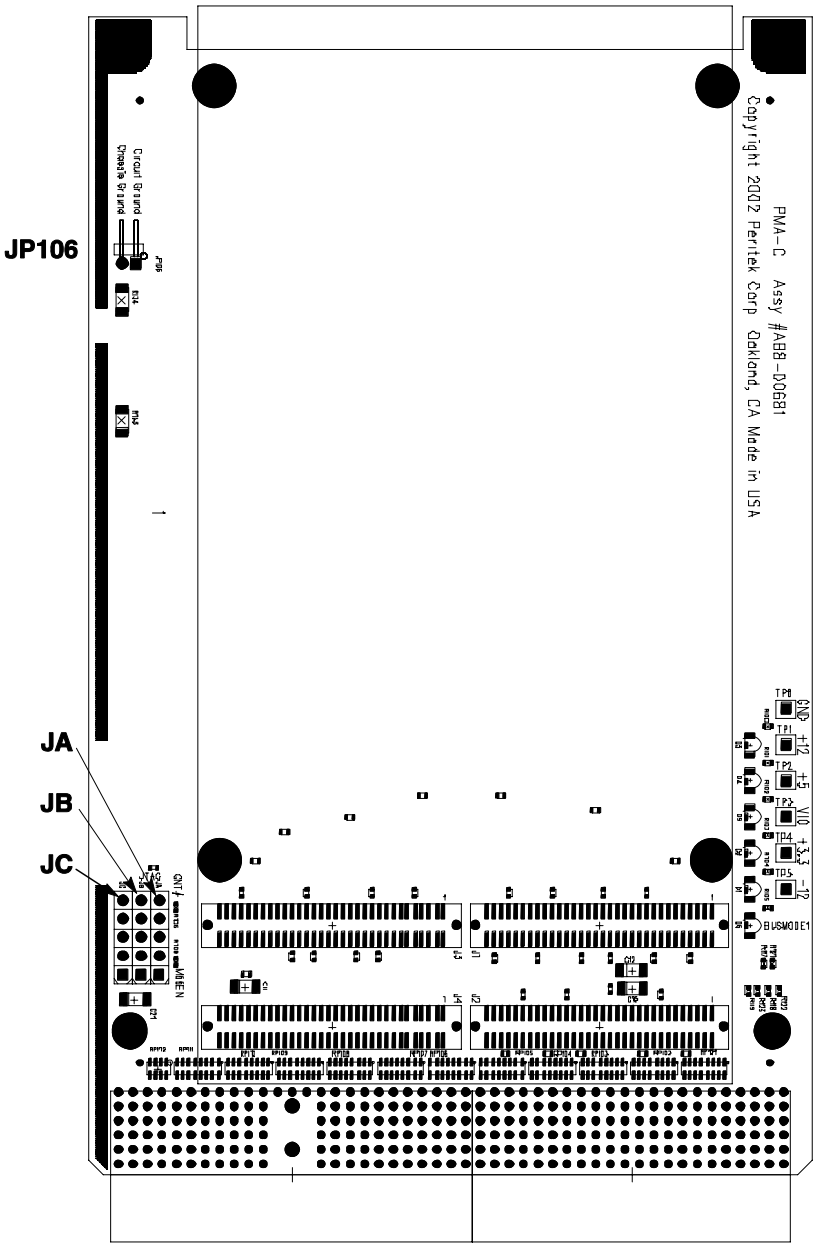
4.4.3 JP106: CompactPCI Frame Ground to Chassis Ground Jumpers

Ordinarily, frame ground and chassis ground are isolated from each other. ***Install*** JP1 to connect them together.

> **Note:**
>
> **Make sure before installing the jumper that this does not expose the system to any electrical hazards.**

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Figure 4-1 Jumper Locations for the PMA-C



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4.5 Preparing for Installation of the PMA-P

Changing the Jumpers on the PMA-P

In the following subsections, please refer ***Figure 4-2*** for jumper locations.

4.5.1 JP3 and JP4: Select the Source for the 3.3V for the PMC

Non-ATX PCI systems and others that only meet PCI Specification 2.1 and before most likely will not supply 3.3V on the PCI connectors. Just for these instances, the PMA-P has an on-board regulator that can be connected to supply a local 3.3V. Note that if you use the local 3.3V regulator, it will "backdrive" the 3.3V pins on the PCI backplane. This should not matter, since they aren't connected to anything.

The PMA-P is default jumpered for 3.3V power from the backplane, which means that JP3 is installed. You can check for the presence of 3.3V on the backplane by installing the PMA-P into the backplane. ***First, make sure that JP3 is NOT installed.*** Then, turn on power. If the 3.3V LED does not light, then you do not have 3.3V on your backplane.

In this case, remove JP4 (this may be a wire-wrap jumper) and install JP3, which will enable the on-board 3.3V regulator to supply 3.3V to the PMC module. To test the jumper, insert the PMA-P into the backplane and turn on power. If the 3.3V LED lights up, then you have 3.3V.

4.5.2 R7 and R8: Power Level Reporting

The PCI bus uses the state of the PRSNT1# and PRSNT2# pins to define the power requirements of the PMA-P (or any PCI card). R7 and R8 determine the reported value:

R7	R8	Power Level
Out	Out	No Board Installed
In	Out	25 Watts
Out	In	15 Watts
In	In	7.5 Watts

Since the power of a PMC module is supposed to be 7.5 Watts, the PMA-P is factory configured to that level.

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4.5.3 66 MHz Enable

The M66EN signal was introduced in PCI Specification 2.1 and PMC Specification IEEE 1386-2001 to enable PMC and PCI boards to report that a module can run at 66 MHz. System software can then correctly configure the local PCI bus system clocks.

Note that to run at 66 MHz, ALL devices connected to the bus MUST be 66 MHz capable. M66EN was a ground pin on the earlier revision IEEE 1386.1 PMC boards, so if you think that your system SHOULD run at 66 MHz but doesn't, some board may be grounding M66EN. Also, prior to PMA-P Revision 3, M66EN was grounded with a 0 Ohm resistor, R6. Now, with PMA-P Rev 3, the PMC module alone controls it. Since M66EN may be grounded on an older PMC module in the PMA-P, you will have to cut the trace grounding this pin on the PMC module to fix this. Of course, make sure that the module really will run at 66 MHz.

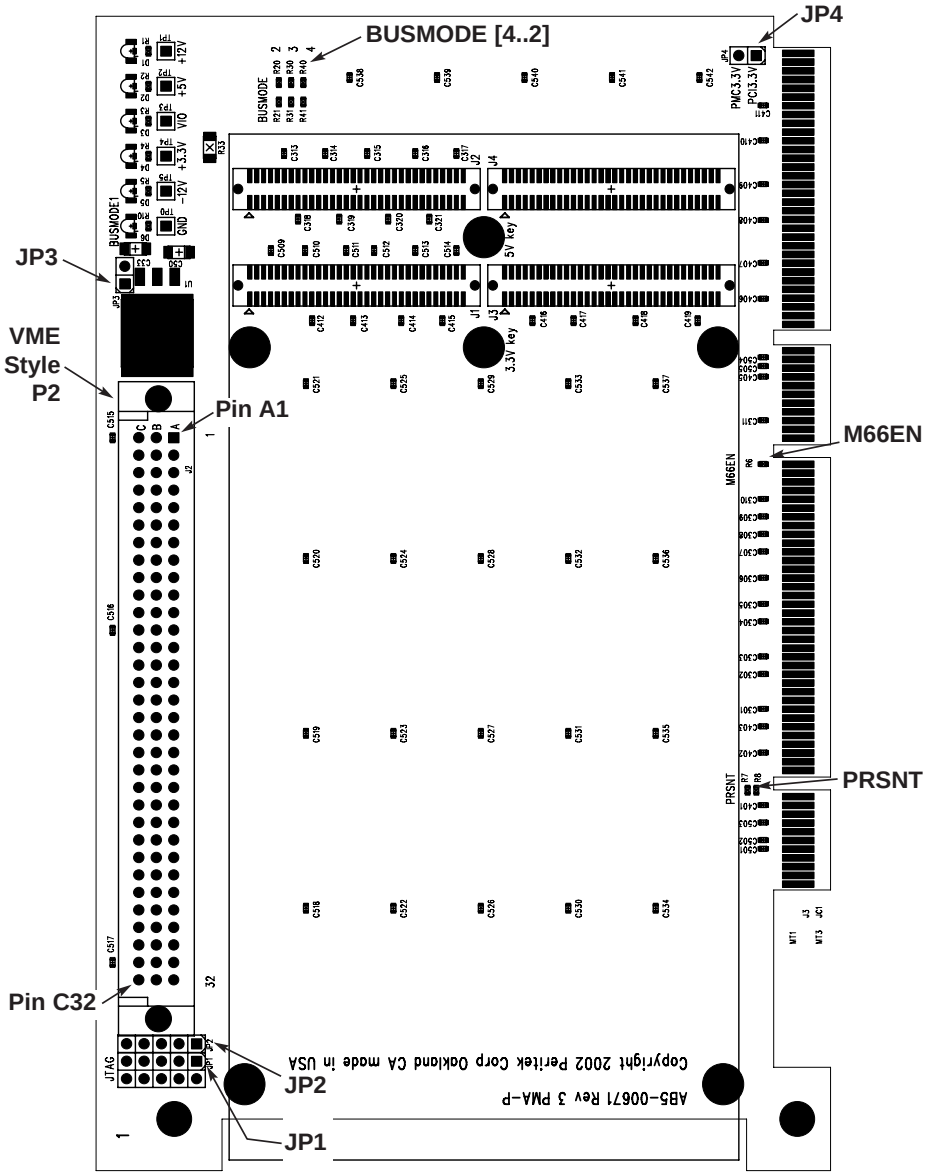
4.5.4 JP1 and JP2 JTAG and JEDEC Programming Jumpers

The PMA-P can be used with a standard Lattice JEDEC programming cable to program PLDs connected to a PMC module's JTAG loop. Many Rastergraf boards use this convention. A 2 x 5 .1" header can be installed in location JP1 to accomplish this.

By default, PCI host bus JTAG pins loop through the PMA-P board and bypass the PMC module. The JTAG pins are connected together (JP1 to JP2) with etch jumpers instead of wires.

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Figure 4-2 Jumper Locations for the PMA-P



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4.6 Preparing for Installation of the PMB-P

Changing the Jumpers on the PMB-P

In the following subsections, please refer ***Figure 4-3*** for jumper locations.

4.6.1 JP3: Select the Source for the 3.3V for the PMC

Non-ATX PCI systems and others that only meet PCI Specification 2.1 and before most likely will not supply 3.3V on the PCI connectors. Just for these instances, the PMA-P has an on-board regulator that can be connected to supply a local 3.3V. Note that if you use the local 3.3V regulator, it will "backdrive" the 3.3V pins on the PCI backplane. This should not matter, since they aren't connected to anything.

The PMB-P is default jumpered for 3.3V power from the backplane, which means that JP3 is ***not*** installed. You can check for the presence of 3.3V on the backplane by installing the PMB-P into the backplane. ***First, make sure that JP3 is NOT installed.*** Then, turn on power. If the 3.3V LED does not light, then you do not have 3.3V on your backplane.

In this case, install JP3, which will enable the on-board 3.3V regulator to supply 3.3V to the PMC module. To test the jumper, insert the PMB-P into the backplane and turn on power. If the 3.3V LED lights up, then you have 3.3V.

4.6.2 R7 and R8: Power Level Reporting (PRSNT)

The PCI bus uses the state of the PRSNT1# and PRSNT2# pins to define the power requirements of the PMA-P (or any PCI card). R7 and R8 determine the reported value:

R7	R8	Power Level
Out	Out	No Board Installed
In	Out	25 Watts
Out	In	15 Watts
In	In	7.5 Watts

Since the power of a PMC module is supposed to be 7.5 Watts, the PMA-P is factory configured to that level.

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4.6.3 JP9: Local Side Clock Source and 66 MHz Enables

The M66EN signal was introduced in PCI Specification 2.1 and PMC Specification IEEE 1386-2001 to enable PMC and PCI boards to report that a module can run at 66 MHz. System software can then correctly configure the local PCI bus system clocks.

Note that to run at 66 MHz, ALL devices connected to the bus MUST be 66 MHz capable. M66EN was a ground pin on the earlier revision IEEE 1386.1 PMC boards, so if you think that your system SHOULD run at 66 MHz but doesn't, some board may be grounding M66EN. Since M66EN may be grounded on an older PMC module in the PMA-P, you will have to cut the trace grounding this pin on the PMC module to fix this. Of course, make sure that the module really will run at 66 MHz.

Table 4-1 Jumper Functions for JP9

<table>
<tr><th>PCI</th><th>PCI M66EN</th><th>PMC</th><th>PMC M66EN</th><th>BRIDGE M66EN</th><th>OSCSEL#</th><th>Default</th></tr>
<tr><td>33</td><td rowspan="2">Jumper in to force 33</td><td>33</td><td rowspan="2">Jumper in to force 33</td><td rowspan="3">In</td><td rowspan="3">Out</td><td rowspan="3">Only BRIDGE M66EN Jumper installed</td></tr>
<tr><td>66</td><td rowspan="2">33</td></tr>
<tr><td>66</td><td rowspan="2">Jumper out to allow bus to set speed</td><td rowspan="2">66</td><td rowspan="2">Jumper out to allow bus to set speed</td></tr>
<tr><td rowspan="2">33 or 66</td><td>Jumper in to force 33</td><td rowspan="2">Variable (U33 power on default is 66)</td><td rowspan="2">Out</td><td rowspan="2">Out</td><td rowspan="2">In</td><td rowspan="2">Only OSCSEL# Jumper installed</td></tr>
<tr><td>Jumper out to allow bus to set speed</td></tr>
</table>

IC U33 is a Cypress 22150 I2C programmable clock generator. Its default clock frequency is 66 MHz, but it can be programmed for quite a wide range. Please contact Rastergraf for more information regarding the use and programming of U33.

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4.6.4 JP1 and JP2: JTAG and JEDEC Programming Jumpers

The PMB-P can be used with a standard Lattice JEDEC programming cable to program PLDs connected to a PMC module's JTAG loop. Many Rastergraf boards use this convention. A 2 x 5 .1" header can be installed in location JP1 to accomplish this.

By default, PCI host bus JTAG pins loop through the PMB-P board and bypass the PMC module. The JTAG pins are connected together (JP1 to JP2) with etch jumpers instead of wires.

4.6.5 JP4: Local PMC VIO Select

The PMB-P local PCI bus (the bus between the PMC boards and the bridge) can be operated either at 3.3V or 5V signaling, which determines the voltage level for a "high" or "one" in the PCI bus signal transitions.

The PCI specification requires 66 MHz systems to use 3.3V in order to improve system performance. 33 MHz systems may use either 3.3V or 5V.

Many current ICs are 5V tolerant and even if nominally 3.3V devices, they can tolerate 5V. Some devices support "Universal PCI" operation which means they do sense whether VIO is 3.3V or 5V.

A keying pin can be used to control whether a 3.3V or 5V VIO compatible board can be installed. This method depends on the PMC card having a matching hole and the user setting JP4 correctly. Note that if the PMC card has 2 keying holes, it is a "Universal PCI" board.

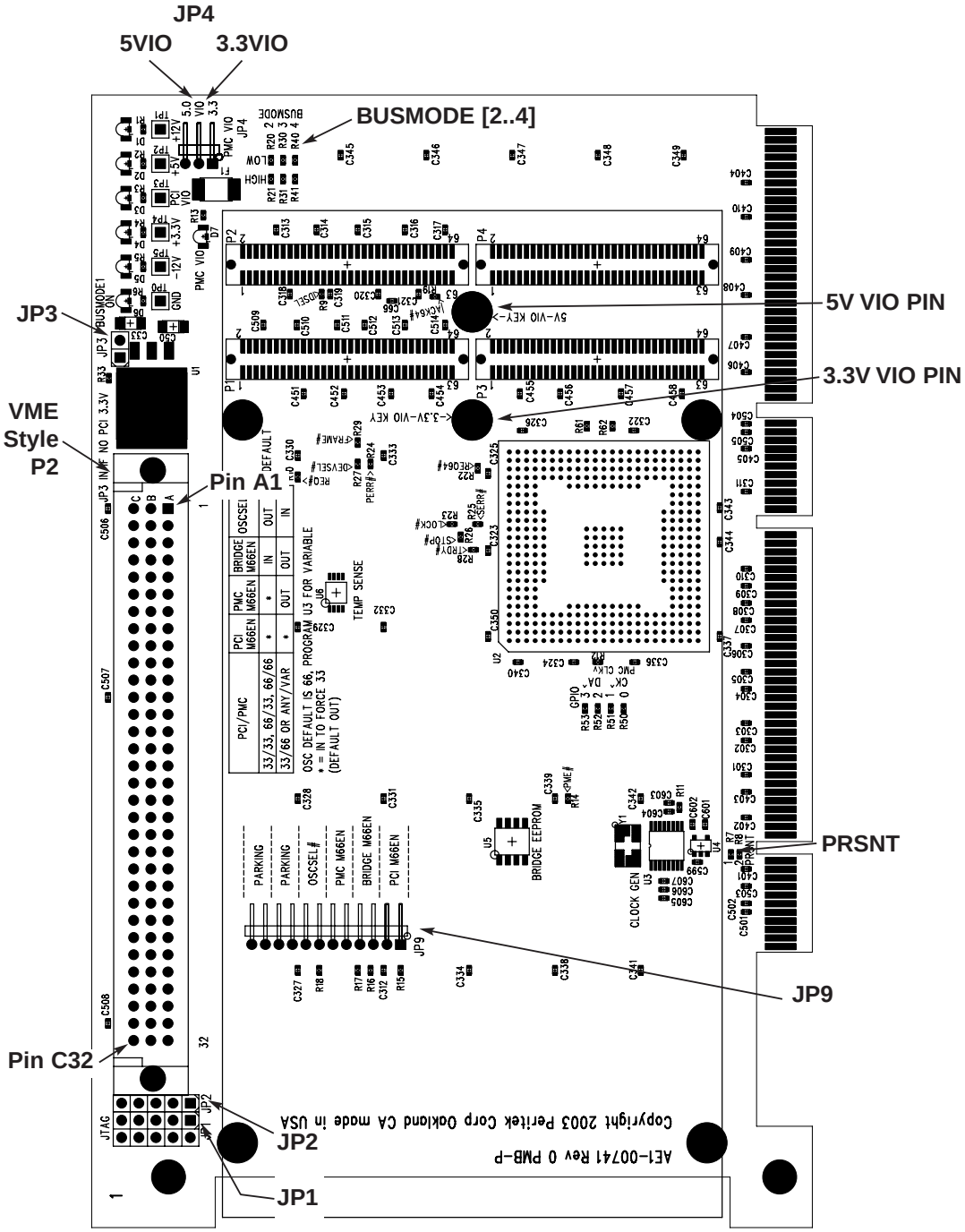
The PMB-P is set by default to have a pin in the 3.3V key pin location and to have JP4 set to 3.3 VIO.

Clearly, JP4 must be installed according to the VIO pin installed:

JP4	VIO Level	Keying Pin
1-2	3.3V	3.3V Hole
2-3	5V	5V Hole

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Figure 4-3 Jumper Locations for the PMB-P



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4.7 PMC Board Installation

The PM Series carriers provide a single-wide PMC 32 or 64-bit, 33 or 66 MHz IEEE 1386-2001 compatible location. The slots accept any standard PMC or CCPMC module.

Note that a Processor PMC (PrPMC) card most likely will ***not*** work correctly with in the PMA-P or PMB-P because the PCI bus does not have the extra signals that the PrPMC usually requires. The PMA-C (Revision 2) is designed to support the standard, basic (single IDSEL) PrPMC and should work correctly with them.

The PMA-P and PMB-P are available with an optional VME-style P2 three row Euro-DIN connector that makes the PMC-J4 I/O available.

The PMA-C supports PMC I/O only at the front panel using connectors mounted on the PMC card. There are no J4 connections made to cPCI connector J2.

Installing the PMC Board

1. If you just received it, unpack your PM Series board and place it component side up on a clean anti-static surface.

2. Referring to Section 4.4-4.6, make sure that any jumpers or other changes to the PM Series card are made now.

3. Make sure that jumpers or other changes to the PMC card are made now.

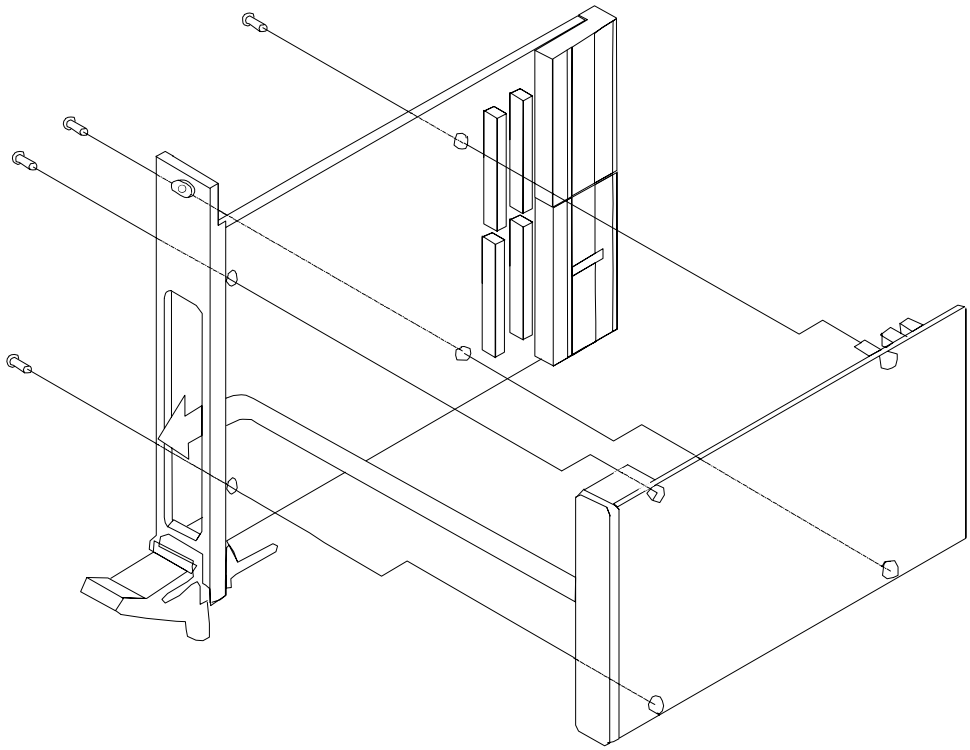
4. Determine whether you are going to use front or rear panel I/O (PMA-P with P2 option).

5. Note that PM Series boards do not have 5V or 3.3V signaling key pins installed because they are “Universal PCI” boards. The signaling level is set by VIO, which comes from the host backplane. It is assumed that your PMC board will work correctly in this configuration. If your PMC board will not work with 5V signaling (which is what you might get from the backplane), go no further. Please contact the factory.

6. Otherwise, insert the PMC card as shown in the figure on the next page and secure it with the mounting screws.

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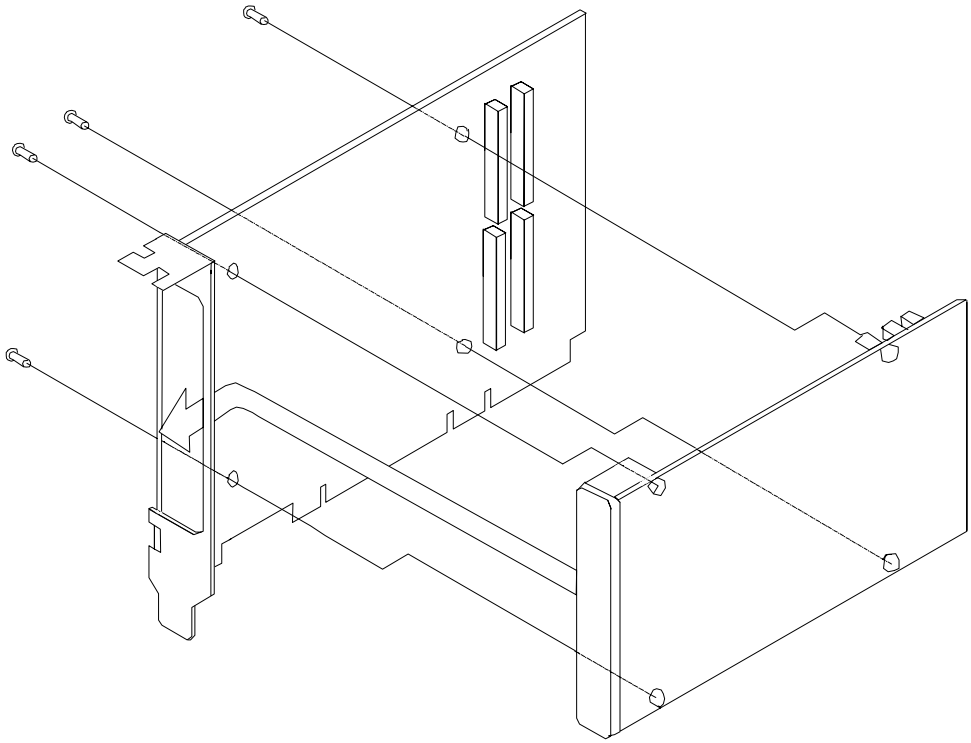
Figure 4-4 Installation of a PMC Module onto a PMA-C



Now, go to Section 4.8.

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Figure 4-5 Installation of a PMC Module onto a PMA-P



Now, go to Section 4.9.

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4.8 Installing the PMA-C Board

The PM Series board can plug into any 32 or 64-bit, 5V or 3.3V signaling CompactPCI 6U slot.

Note:

Refer to ***Section 2.4*** for the instructions for configuring the PMA-C.

1. Shut down the operating system and **turn off the power**.

Warning!

Never open the computer without turning off the power supply. Unless internal AC wiring is exposed, leave the power cord plugged in, so as to ground the computer chassis. You can easily get shocked, ruin computer parts or both unless you turn off the power. Even with power switched off, lethal voltages can exist in the equipment.

2. Open the computer and identify the empty slot in the card cage that is closest to the CPU. Do not leave any slots empty between the PMA-C and the CPU.

   The PMA-C is a Universal PCI device and can be plugged into a slot which uses either 5V or 3.3V signaling protocol. Therefore, a J1 connector signaling key plug is not necessary.

3. In the interest of allowing air flow, and if you have a choice, block off any unused slots in the cardcage so that fan air will not flow through them.

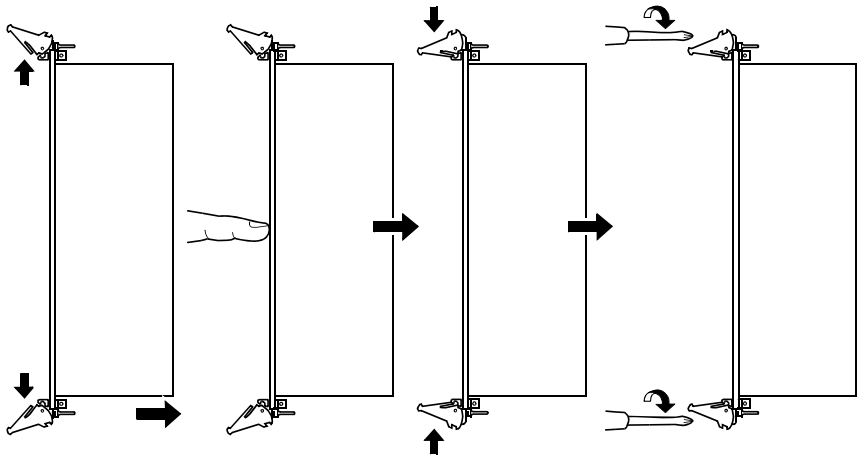
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Caution

The static electricity that your body builds up normally can seriously damage the components on the computer boards.

4. Wear a grounded wrist strap and touch a metal part of the computer chassis. Remove the card slot blocking plate from the chassis. Then, slide the PMA-C (with PMC card already installed) into the slot.

Figure 4-6 Installing a CompactPCI Board



5. After making sure the board is seated correctly, lever the card in with the injector(s) and tighten the screwlock on each end of the faceplate. Close up the computer as appropriate.

6. There is nothing on the PMA-C itself that requires software support. It is assumed that the operating system will already know how to deal with the PMC module you installed on the PMA-C.

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4.9 Installing the PMA-P or PMB-P Board

The PMA-P and PMB-P boards are “Universal PCI” devices. They can be plugged into any standard PCI 2.2 compatible backplane which uses either 5V or 3.3V signaling protocol (See Section 1.1 for more info).

Notes:

The PMA-P and PMB-P boards require both 3.3V and 5V. Most AT style motherboards do not supply 3.3V to the PCI connectors. If the computer is listed as PCI 2.0 or 2.1 compliant, it probably does not supply 3.3V.

Please go to Section 4.5 for the PMA-P or 4.6 for the PMB-P to see how to enable its local 3.3V regulator. Please contact Rastergraf for assistance.

Refer to ***Section 4.5*** for the **PMA-P** or **Section 4.6** for the **PMB-P** for the instructions for configuring the PMA-P.

1. Shut down the operating system and **turn off the power**.

Warning!

Never open the computer without turning off the power supply. Unless internal AC wiring is exposed, leave the power cord plugged in, so as to ground the computer chassis. You can easily get shocked, ruin computer parts or both unless you turn off the power. Even with power switched off, lethal voltages can exist in the equipment.

2. Open the computer and find an empty PCI slot.

   When installing the card you have to watch out because the slot (see Figure 2-5) between the 32-bit and 64-bit parts of the PCB connector is quite narrow. PCs sometimes have PCI connectors that have overly thick moldings, requiring the slot to be widened. Should you encounter this problem, please contact Rastergraf for assistance.

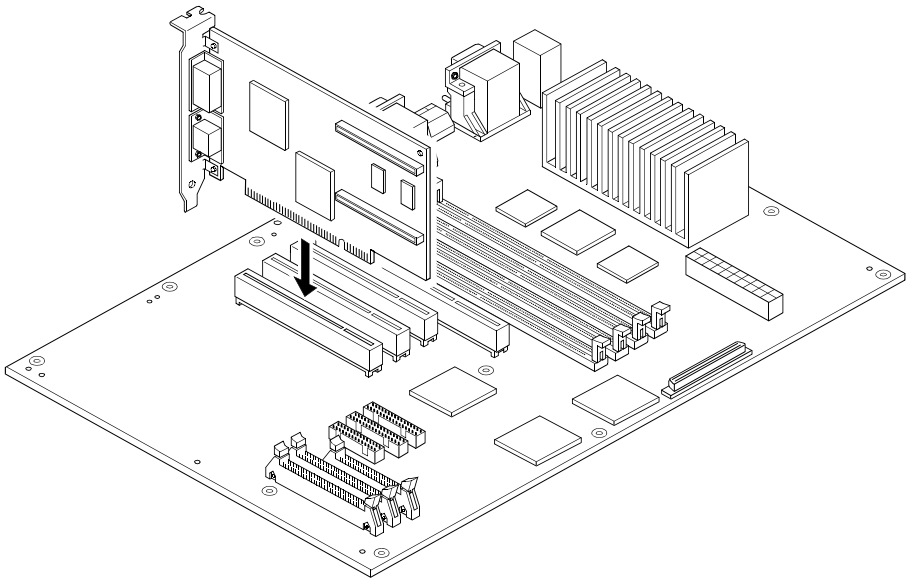
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Caution

The static electricity that your body builds up normally can seriously damage the components on the circuit board.

3. Wear a grounded wrist strap and touch a metal part of the computer chassis. Remove the card slot blocking plate from the chassis. Then, slide the PMA-P (with PMC card already installed) into the slot.

Figure 4-7 Installation of a PCI Module into a Motorola MTX



4. After making sure the board is seated correctly, install the screw into the place where the blocking plate was and which (now) holds the PM board's front panel. Close up the computer as appropriate.

5. There is nothing on the PMA-P itself that requires software support, but the PMB-P does have a bridge. In either case, it is assumed that the operating system will already know how to deal with the PMC module you installed on the PMA-P or PMB-P. Rastergraf does not supply software for any PM Series board.

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Chapter 5 Troubleshooting

Introduction

This chapter contains information which should assist you in tracking down installation and functional problems with your board.

5.1 General procedures

5.2 Dealing with the PCI bus

5.3 Maintenance, Warranty, and Service

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5.1 General Procedures

The PM Series boards were designed with reliability and durability in mind. Nevertheless, it may happen that a problem will occur. This section is devoted to aiding the user in tracking down the problem efficiently and quickly.

You may be able to locate minor problems without technical assistance. If the problem can not be remedied, Rastergraf can then issue a Return Material Authorization (RMA) so that the board can be returned to the factory for quick repair.

It can happen that installing a new board will overload the computer's power supply if the power supply margins are exceeded. The first step in ascertaining if this is the problem is to calculate a power supply budget. This involves adding up the power requirements of each board in the system to see if you are within specification. Consult your computer's technical manual for information on how to correctly determine this. A typical PM Series will draw a total of less than 1 Amp at +5 and +3.3 Volts.

When attempting to verify that the power supply is working properly, it is not unusual to unplug everything and measure the supply without a load. While this practice is acceptable for linear supplies, switching supplies (which are very commonly used in computers) require a certain load before proper regulation is achieved. Typically, at least 5 Amps must be drawn from the +5 Volt supply before the +12 volt supplies will give the proper readings.

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5.2 Dealing with the PCI Bus

Because of the nature of the PCI protocol and the way support has been implemented in the Operating Systems for PCI bus devices such as the PM Series, it is not possible to follow the same debugging strategies.

In fact, there are no address jumpers for these boards. Everything is configured in software through a set of on-board registers, which control the characteristics of the board as required by the PCI Specification.

The information used to program these registers is supplied to Operating System (OS) specific functions by Rastergraf's software. Ordinarily, several address map translations occur, including the CPU physical and virtual address maps and the CPU to PCI bridge address map.

While x86 systems generally follow the standards required to meet PC compatibility and mask these details, PowerPC systems do not. Among PowerPC vendors, there are no standards which ensure interoperability among CPU boards, even when they use the same CPU and PCI bridge.

Therefore, if you plan to use an PM Series board in a PowerPC based system, it is vital to ensure that Rastergraf can vouch for the board's operation before you order the board. Otherwise, you may go crazy trying to figure out why it doesn't work. Please contact us at support@rastergraf.com or (541) 923-5530 if you have problems.

5.3 Maintenance, Warranty, and Service

Maintenance

The PM Series requires no regular service, but if used in a particularly dirty environment, periodic cleaning with dry compressed air is recommended.

Because of the heat generated by normal operation of the board and other boards in the system, forced crossflow ventilation is required. If forced ventilation is not used IC temperatures can rise to 60 degrees C or higher. Such high temperature operation causes IC failures and reduced MTBF. With proper forced air cooling IC temperatures will be less than 35 degrees C.

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Warranty

The PM Series boards are warranted to be free from defects in material or manufacture for a period of 12 months from date of shipment from the factory. Rastergraf's obligation under this warranty is limited to replacing or repairing (at its option) any board which is returned to the factory within this warranty period and is found by Rastergraf to be defective in proper usage. This warranty does not apply to modules which have been subjected to mechanical abuse, electrical abuse, overheating, or other improper usage. This warranty is made in lieu of all other warranties expressed or implied. **All warranty repair work will be done at the Rastergraf factory.**

Return Policy

Before returning a module the customer must first request a Return Material Authorization (RMA) number from the factory. The RMA number must be enclosed with the module when it is packed for shipment. A written description of the trouble should also be included.

Customer should prepay shipping charges to the factory. Rastergraf will prepay return shipping charges to the customer. Repair work is normally done within ten working days from receipt of module.

Out of Warranty Service

Factory service is available for modules which are out of warranty or which have sustained damage making them ineligible for warranty repair. A flat fee will be charged for normal repairs and must be covered by a valid purchase order. If extensive repairs are required, Rastergraf will request authorization for an estimated time and materials charge. If replacement is required, additional authorization will be requested.

All repair work will be done at the Rastergraf factory in Redmond, Oregon, unless otherwise designated by Rastergraf.

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