RG-741

VME Graphics Board User's Manual

Rastergraf

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Preface

This manual contains hardware and operating information for the RG-741 color graphics board. The standard configuration for the RG-741 includes 512k bytes of DRAM for instruction storage, 1Mbyte of VRAM, an RS-232 serial interface for mouse or serial use, an AT keyboard interface, on-board AFGIS firmware, interface PAL set -PS0, and programmable video displayed in a 60Hz non-interlace format for use with VGA & SVGA video monitors.

The RG-741 offers the following six programmable resolutions and video pages:

Resolution	Video Pages
640h x 480v x 4	2
640h x 480v x 8	2
800h x 600v x 4	2
800h x 600v x 8	1
1024h x 768v x 4	2
1024h x 768v x 8	1

The RG-741 is available in one basic configuration with the options listed below.

Options

To specify an option(s), add the option letter(s) to the basic part number. For example, RG-741-M 2 would specify the basic configuration with 2 Mbytes of DRAM.

Option	Description	A24 Address
-PS0	Interface PAL Set	E00000h/D00000h
-PS1	Interface PAL Set	C00000h/B00000h
-PS2	Interface PAL Set	A00000h/900000h
-CP	Custom Interface PAL Set	xxxxxxh/xxxxxxh
-6U	Specifies 6U front panel	
-50Hz	Specifies 50 Hz video timing	
-M2	Specifies 2 Mbytes of DRAM	

Related Documents

AFGIS Instruction Set Manual
AFGIS Programming Manual
AFGIS Assembler Manual
AFGIS C Graphics Library Instruction Set Manual
AFGIS C Programming Manual
AFGIS Application Interface Manual
TMS34010 User's Guide (available from Texas Instruments)

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3. Damage results from connecting the hardware to incompatible equipment.

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1. Introduction

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The RG-741 Color Graphics Board

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The RG-741 Color Graphics Board

Overview

The RG-741 is a high performance 3U graphics board, powered by the TMS34010 graphics processor, and designed for VMEbus applications. Major features of the RG-741 are its on-board AFGIS firmware with over 250 highly optimized graphics primitives for easy graphics programing, its ability to support real-time multi-tasking operating systems with its unique pointer based graphics environment, its advanced hardware architecture with mouse and keyboard interfaces, and extensive C programing support.

The RG-741 is ideal for simple embedded system applications, because it is easy to program and because it does its own local graphics processing, freeing the VMEbus host to do other things while the RG-741 is creating graphics in parallel.

The real power and versatility of the RG-741 is evident when it is used with real-time multi-tasking operating systems that require several tasks to independently generate graphics on the video screen. Each task can have its own colors, font, screen position, etc., and can independently create graphics on the video screen without affecting the colors, font, screen position, etc. of any other task.

Each task can have its own private pointer based graphics environment with all the necessary buffers, variables, and low level drawing parameters. The host processor (typically the driver) selects the environment for the current task by updating a pointer in Fixed RAM before the task runs any graphics code. Because the graphics environment is pointer based, switching the environment takes little time, typically less than 15 usecs, which has a minimal impact on the task's allocated time slice.

The RG-741 is supported with the AFGIS C Graphics Library which has over 125 high level C functions which have been optimized for use with the on-board AFGIS firmware. A driver is typically required for use with the AFGIS C Graphics Library and today's modern real-time operating systems. Drivers are available for several of the popular real-time operating systems, and custom driver development is available from Rastergraf, Inc. for operating systems not currently supported with drivers.

The driver and AFGIS C Graphics Library are easy to install, and once installed, allow the user to begin using the RG-741 without regard for the details of the hardware interface, as these are handled by the driver. The C functions provided by the AFGIS C Graphics Library are linked at compile time, and in effect extend the C functions of the system's C compiler to include those provided by the AFGIS C Graphics Library.

The RG-741 Color Graphics Board

The combination of advanced hardware architecture, optimized on-board graphics primitives, and extensive C programing support, make the RG-741 an ideal low cost, high performance solution for many of today's challenging graphics opportunities.

Features

The RG-741 provides the following major features and options:

- Programmable Resolutions

  640h x 480v x 4/8
  800h x 600v x 4/8
  1024h x 768v x 4/8

- 16/256 Colors
- TMS34010 Graphics Processor
- 1/2 Mbyte of DRAM (option for 2 Mbytes)
- 1 Mbyte of VRAM
- Mouse and Keyboard Interfaces
- Video DAC with 256x24 color look up table (Bt478)
- On-board firmware with over 250 highly optimized graphics primitives to draw text, windows, circles, arcs, polygons, fills, fatlines, pattern fills and more!
- Fast graphics environment switching, less than 15 usec to support real-time tasks
- Supports parallel processing for improved system performance
- 6U front panel option
- Interrupts to and from the VMEbus
- Sync polarity options
- Sync on green option
- Application interface to extend the on-board graphics primitives with downloaded TMS34010 code.
- AFGIS C Graphics Library for easy graphics programing
- Drivers for OS-9, PSOS, and PDOS real-time operating systems

2. Installation

This chapter contains information on the following topics:

Board Installation

Board Layout

Jumper and Connector Options

J1 Interrupt Request Select
J2 Debug Enable
J3 Address Select
J4 Run/Halt at Power-up
J5 AT Keyboard Connector
J6 Manual Test Switch
J7 Manual Reset
J8 Serial Port Handshake Line Option
J9 Serial Port Handshake Line Option
J10 Video Output Connector
J14 Mouse/RS-232 Serial Connector
P1 VMEbus Connector, P1

Board Installation

Install the RG-741 graphics board in a VMEbus card slot. The RG-741 must plug into VMEbus connector P1. Use an RG-741 with the -6U front panel option if installing the board in a 6U system.

> **CAUTION:**
> **Switch off power to the VMEbus before installing the RG-740 to avoid possible damage to the graphics board or host hardware.**

Board Layout

The RG-741 graphics board contains several jumper options, a video connector, and status LEDs, as shown in Figure 2.1. Connectors are provided for interfacing the RG-741 to a VGA or SVGA RGB color monitor (J10), Serial device (J14), and keyboard (J5).

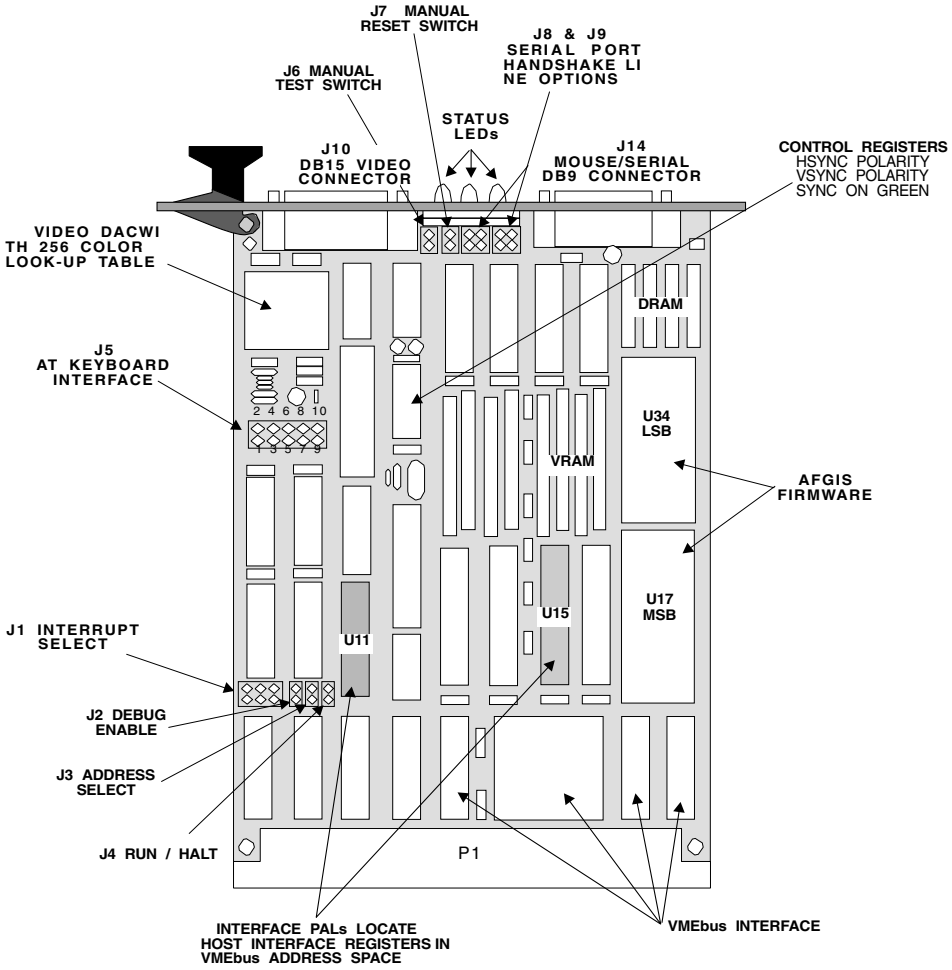

Figure 2.1 RG-741 Board Layout

Jumper and Connector Options

The following jumper options and connectors, shown in Figure 2.2, are available on the RG-741. Figure 2.1 indicates the jumper and connector locations. Use shorting clips or wirewrap wire to select the jumper options.

JUMPER	DESCRIPTION
J1	Interrupt Request Select
J2	Debug Enable
J3	Address Select
J4	Run/Halt
J5	AT Keyboard Connector (2x5 Header)
J6	Manual TestSwitch
J7	Manual Reset
J8	Serial Port Handshake Line Options
J9	Serial Port Handshake Line Options
J10	Video Connector (DB15)
J11	not used
J12	not used
J13	not used
J14	Mouse/Serial Port Connector (DB9)

Figure 2.2 Jumper & Connector Summary

Jumper and Connector Options (continued)

J1 Interrupt Request Select

The RG-741 generates an interrupt to the host and outputs an 8 bit interrupt vector in response to an interrupt acknowledge, as shown in Figure 2.3a. The interrupt can be routed to any of the 7 VMEbus interrupt lines, IRQ1-IRQ7, by installing jumpers in J1 as shown below in Figure 2.3.

IRQ	J1 (2 4 6 / 1 3 5)
IRQ1	5-6
IRQ2	3-4
IRQ3	3-4, 5-6
IRQ4	1-2
IRQ5	1-2, 5-6
IRQ6	1-2, 3-4
IRQ7	1-2, 3-4, 5-6

Figure 2.3 IRQ Select

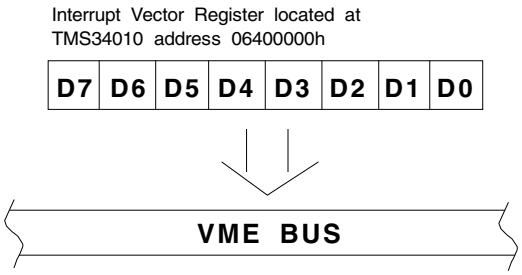

Figure 2.3a Interrupt Vector Register

J2 Debug Enable

This function enables or disables the serial debugger

	J2 (2 / 1)
DEBUG NOT ENABLED	
DEBUG ENABLED	

Figure 2.4 Debug Enable

Jumper and Connector Options (continued)

J2 Host Interface Register Address Select

The VMEbus interfaces to the RG-741 via four 16-bit Host Interface Registers located in a 256-byte page in VMEbus memory space (see Figure 2.5). All data transfers between the VMEbus and the RG-741 are via these registers. The four 16-bit Host Interface Registers can be located at one of the two base addresses in VMEbus address space by configuring jumper J3 (see Figure 2.6).

The base addresses are determined by the Interface Register PALs U11 and U15, and can be changed by programing a new PAL set (see Appendix A for PAL equations) or by ordering a custom Interface PAL set from Rastergraf, Inc.

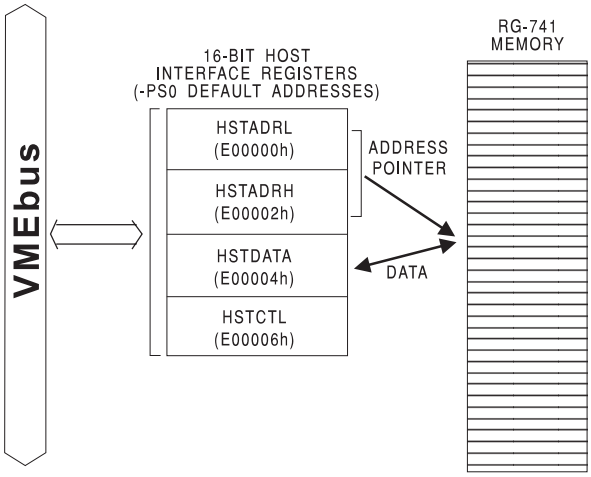

Figure 2.5 VMEbus Interface

PAL OPTION	J3 2 1	J3 2 1
PS0	E00000	D00000
PS1	C00000	B00000
PS2	A00000	900000

Figure 2.6 Address Select

J4 Run/Halt

The RG-741 can be jumpered at J4 to come up running (no jumper at J4) or halted (jumper installed in J4) at power-up. For normal operation, the RG-741 should be jumpered to come up running.

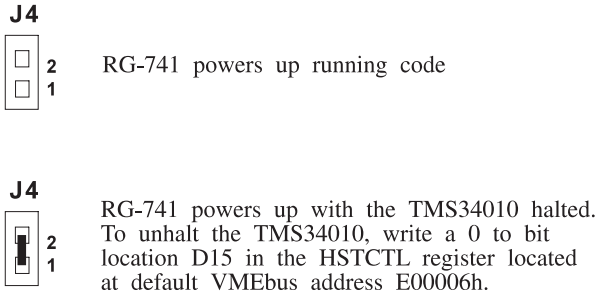

Figure 2.7 Run/Halt At Power-Up Jumper

Jumper and Connector Options (continued)

J5 AT Keyboard Connector

Connector J5 provides an interface to a standard AT keyboard. An adaptor cable is required to connect the standard AT 5-pin keyboard connector to the RG-741 board 10-pin header connector (see Figure 2.8). The RG-741 keyboard firmware works with an AT style keyboard. It does not operate with PC or XT keyboards, which have a different interface.

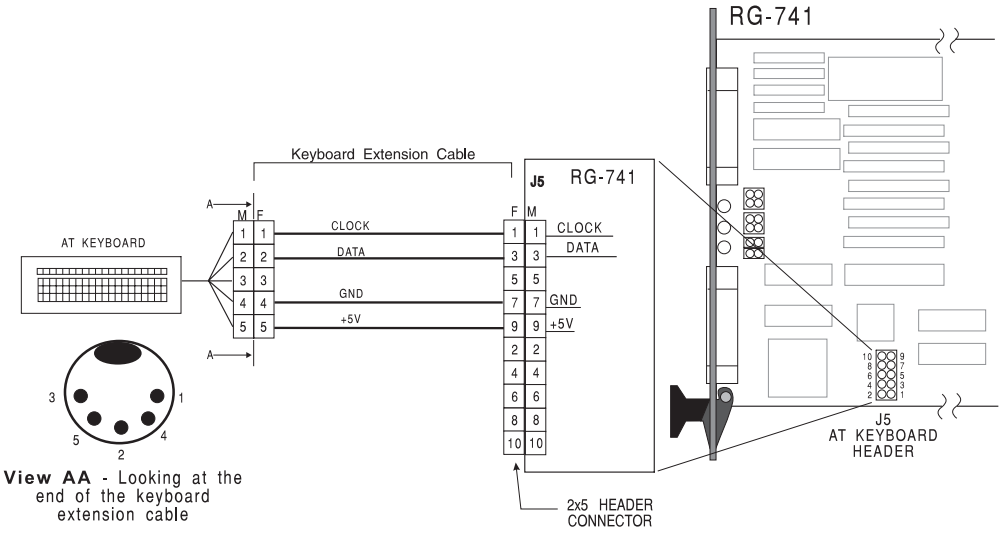

Figure 2.8 AT Keyboard Connector

J6 Manual Test Switch

Momentarily shorting J6 will cause the built-in test to be displayed on the monitor.

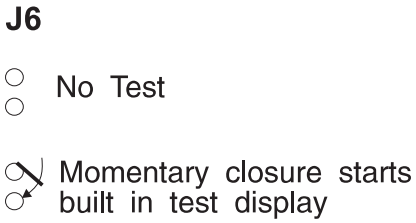

Figure 2.9 Manual Test Switch

J7 Manual Reset

Momentarily shorting J7 will reset the RG-741. The VMEbus will not be affected

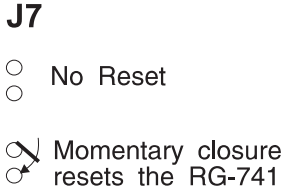

Figure 2.10 Manual Reset Switch

Jumper and Connector Options (Continued)

J8 & J9 Serial Interface Handshake Line Option

The serial interface can be configured for a serial mouse or RS-232 use, depending on the jumpers installed in J8 and J9

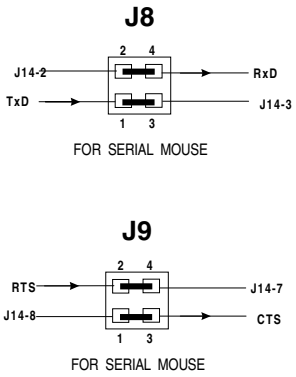

Figure 2-11 J8 & J9 Configured for Serial Mouse

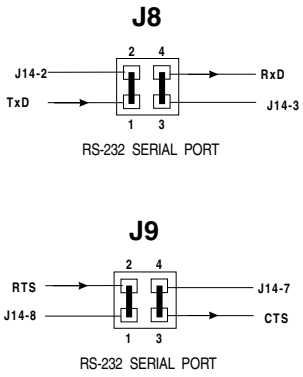

Figure 2-12 J8 & J9 Configured for RS-232

J10 S-Video Connector (DB15)

Connect video from the RG-741's DB15 video connector, J10, to the VGA or SVGA video monitor as shown below. Sync on green & sync polarity are programmable. The sync polarity and sync on green options are controlled by setting the appropriate bits in the control register, using the CONTREG opcode. DO NOT set the control register bits directly by writing to memory location 0580 0000h.

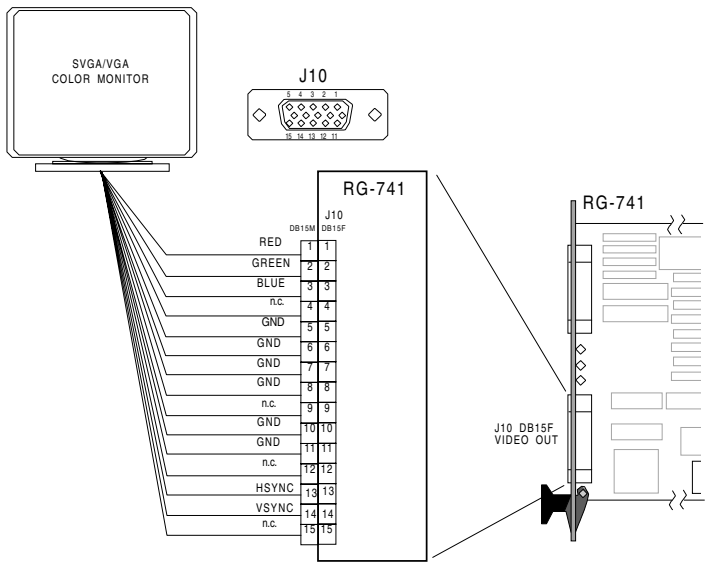

Figure 2.13 Video Monitor Connection

Jumper and Connector Options (continued)

J14 Mouse/Serial Port Connector (DB9)

A serial mouse or RS-232 device may be connected to the RG-741 at J14 as shown below. Jumpers at J8 & J9 must be installed appropriately.

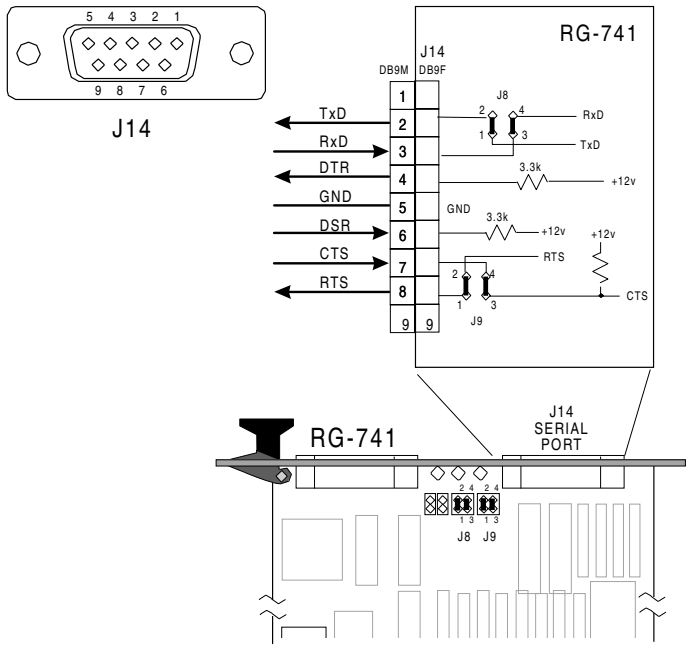

Figure 2-14 RS-232 Serial Configuration

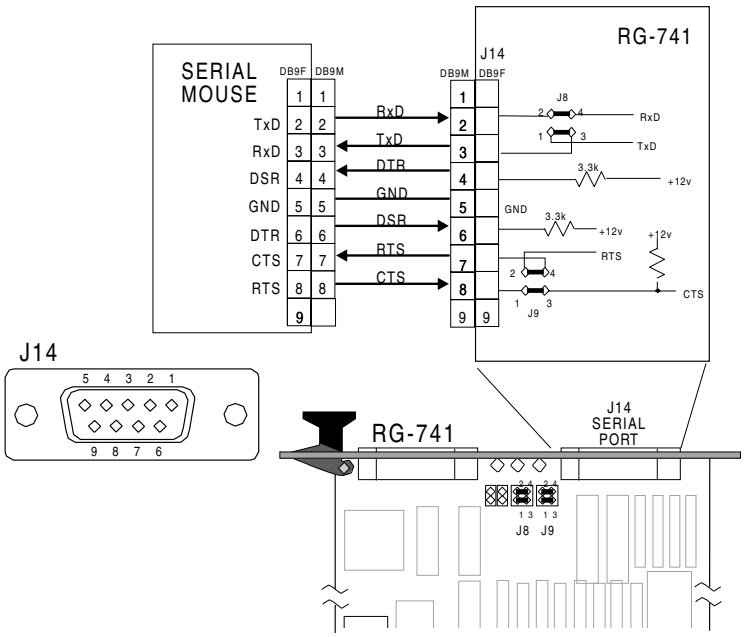

Figure 2-15 Serial Mouse Configuration

Jumper and Connector Options (continued)

VMEbus Pin Assignments

Figure 2.16 shows the pins on VMEbus P1 used by the RG-741 graphics board.

P1			
PIN #	**ROW A**	**ROW B**	**ROW C**
1	D0		D8
2	D1		D9
3	D2		D10
4	D3	BG0IN*	D11
5	D4	BG0OUT*	D12
6	D5	BG1IN*	D13
7	D6	BG1OUT*	D14
8	D7	BG2IN*	D15
9		BG2OUT*	
10		BG3IN*	
11		BG3OUT*	
12	DS1*	BR0*	
13	DS0*		LWORD*
14	WRITE*		AM5
15			A23
16	DTACK*	AM0	A22
17		AM1	A21
18	AS*	AM2	A20
19		AM3	A19
20	IACK*		A18
21	IACKIN*		A17
22	IACKOUT*		A16
23	AM4		A15
24	A7	IRQ7*	A14
25	A6	IRQ6*	A13
26	A5	IRQ5*	A12
27	A4	IRQ4*	A11
28	A3	IRQ3*	A10
29	A2	IRQ2*	A9
30	A1	IRQ1*	A8
31	-12VDC		+12VDC
32			+5 VDC

Figure 2-16 VMEbus P1 Connector Pin Assignments

3. Operation

This chapter contains information on the following topics:

Power Up Display

Operation Overview

RG-741 Host Interface Registers

Data Transfer Convention

Transferring Data

RG-741 Memory

RG-741 Memory Map

EPROM

DRAM

VRAM

RS-232 Interface Keyboard Interface

Video DAC

Control Register

Remapping DRAM with ROMDIS

LEDs

Interrupts

From host to RG-741

Resetting the RG-741 with NMI

From RG-741 to host

Coordinate System

Overview of RG-741 Operation

Power Up Display

The RG-741 creates a display at power up, indicating the resolution of the current display mode. The display resolution is programmable, and can be changed with the CONFIG opcode. The parameter following the CONFIG opcode changes the resolution as follows:

0000 = 640h x 480v x 4
0001 = 640h x 480v x 8
0002 = 800h x 600v x 4
0003 = 800h x 600v x 8
0004 = 1024h x 768v x 4
0005 = 1024h x 768v x 8

The default resolution is 640h x 480v x 4.

Operation Overview

When programing the RG-741 using an RGI driver and AFGIS C graphics library, the details of loading and executing instructions are transparent to the user, as the driver interfaces to both the operating system and the RG-741. The user merely calls the specified C graphics functions from the AFGIS C graphics library, and the resulting code is passed to the driver, which interfaces appropriately with the RG-741.

However, the RG-741 can be programed directly with AFGIS opcodes. AFGIS opcodes are 16 bit instructions which may have 16 bit parameters, similar to most assembly languages. AFGIS opcodes are executed by the on-board firmware after they have been loaded into RG-741 memory. The default location for loading AFGIS opcodes is 03100000h. Execution of these opcodes begins when the host issues a HINT0 interrupt to the RG-741. The list of AFGIS opcodes (display list) must end with the EODL opcode, which causes display execution to cease when the EODL opcode is processed. When the EODL instruction has been executed by the RG-741, AFGIS firmware will issue an interrupt to the VMEbus or set the EODLFLAG, indicating to the host that display execution has been completed.

HINT0 causes execution to begin at the address in Fixed RAM location HINT0_AFG_ENTRY. The default value in HINT0_AFG_ENTRY is 03100000h, but can be changed by the host to any valid TMS34010 address, and display execution will begin at the specified address in response to HINT0. HINT0_AFG_ENTRY is located in Fixed RAM at 030000C0h.

See the AFGIS Programing Manual for more information.

RG-741 Host Interface Registers

The VMEbus interfaces to the RG-741 via four 16-bit Host Interface Registers located in a 256-byte page in VMEbus address space. All data transfers between the VMEbus and the RG-741 are via these registers and data must be transferred 16 bits at a time. The four 16-bit Host Interface Registers can be located at one of two base addresses by configuring jumper J3. The two base addresses are determined by the Interface Register PALs U11 and U15, and can be changed by programing new PALs (see Appendix A for PAL equations) or by ordering a custom Interface PAL set from Rastergraf, Inc.

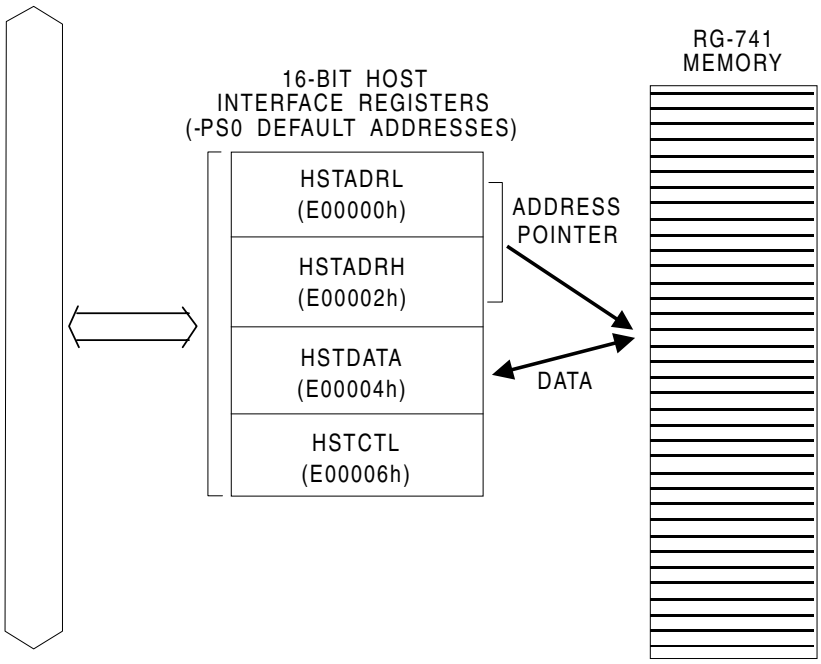

Figure 3.1 Host Interface Registers

Data Transfer Convention

The RG-741 supports little endian format. Words, 16 bit values, can be transferred from VMEbus memory to RG-741 memory across the VMEbus without modification. Bytes (8 bit values) must be byte swapped and longs (32 bits values) must be word swapped before transfer. See Appendix B for more information.

RG-741 Host Interface Registers (continued)

Transferring Data

Data is transmitted to or from the RG-741 by specifying the TMS34010 32-bit memory address in HSTADRL and HSTADRH, and then by writing or reading a 16-bit data word to or from the HSTDATA register. The TMS34010 moves the data from RG-741 memory to the HSTDATA register for a read operation, or from the HSTDATA register to the specified memory location on the RG-741 graphics board for a write operation. The TMS34010 is a bit-addressable machine. AFGIS opcodes must be loaded on word boundaries (the four lsbs of the address loaded into HSTADRL must be zero). Bits in the HSTCTL register can be set to cause the address value in HSTADRL/H to increment automatically on reads or writes, to pass interrupts to the RG-741, and to control the TMS34010 graphics processor. See the TMS34010 User's Guide available from Texas Instruments for a complete description of the TMS34010 host interface.

HSTADRL

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

HSTADRH

A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16

HSTDATA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

HSTCTL

BIT	NAME	DESCRIPTION
15	HLT	Halts TMS34010 processing
14	CF	Flushes the cache
13	LBL	Lower byte last
12	INCR	Increments address after each read
11	INCW	Increments address after each write
10		reserved
9	NMIM	Selects the mode for the nonmaskable interrupt
8	NMI	Enables the nonmaskable interrupt
7	INTOUT	Sends output interrupt from TMS34010 to host
4-6	MSGOUT	Buffers an output message code
3	INTIN	Sets input interrupt from host to TMS34010
0-2	MSGIN	Buffers an input message code

Figure 3.2 Host Interface Registers Bit Assignments

RG-741 Memory

Memory on the RG-741 board includes EPROM, DRAM, video RAM, and memory-mapped registers, as shown in Figure 3.3.

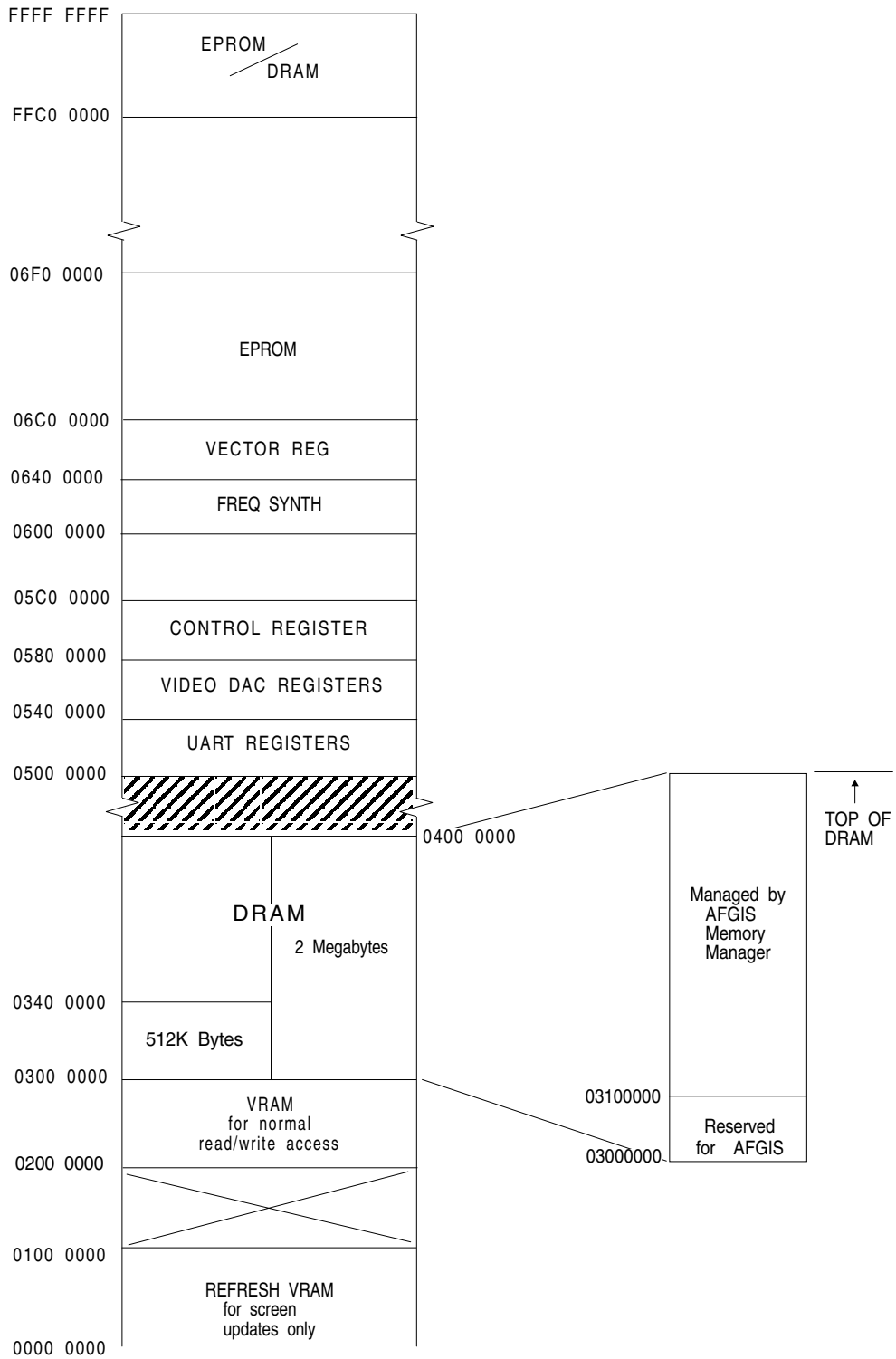

Figure 3.3 RG-741 Memory Map

RG-741 Memory (continued)

EPROM

AFGIS firmware resides in two 27020 EPROMs on the RG-741 graphics board. U17 is the msb EPROM, which contains data bits D8 through D15. U34 is the lsb EPROM, which contains data bits D0 through D7.

DRAM

The RG-741 can be configured with 1/2 or 2 Mbytes of DRAM. DRAM is used by AFGIS firmware for instruction storage, for temporary storage of screen data, and for downloaded code. The first 64k words of DRAM are reserved for use by AFGIS firmware. The rest of DRAM, starting at 03100000h, is available for user code, and is managed by the AFGIS memory manager.

The AFGIS memory manager returns an address to the start of a block of DRAM requested by the user with the ALLOC opcode. Memory is allocated starting at the beginning of available DRAM (03100000h).

The default location for downloading and executing AFGIS opcodes is also 03100000h. DRAM at this address and above (AFGIS heap) is controlled by the AFGIS memory manager and will be allocated to the first request for memory with the ALLOC opcode. To avoid memory usage conflict, a block of memory should be requested from the AFGIS memory manager for AFGIS opcode processing (If the ALLOC opcode is never used to allocate memory for any other purpose, AFGIS opcodes can be safely run at 03100000h without allocating memory for opcode processing).

Fixed DRAM Interface

The first 24 words of DRAM, starting at 03000000h are designated as Fixed RAM and contain flags, addresses, and parameters for access by the VMEbus host. Fixed RAM values are either 16 or 32 bits long, and may have restricted access. R means the location may be read by the host, but it may not be modified. R/W means that the location may be read from or written to by the host. Fixed RAM is organized as shown on the next page.

See the AFGIS programing Manual for additional information

RG-741 Memory (continued)

ADDRESS	NAME	SIZE	ACCESS	DESCRIPTION
03000000h	EODLFLAG	16	R/W	= 0 when the RG-741 is busy. = 1 when the RG-741 is not busy.
03000010h	KBDFLAG	16	R/W	= 0 when there is no keyboard data. = 1 when keyboard data is available.
03000020h	MSEFLAG	16	R/W	= 0 when there is no mouse/serial data. = 1 when mouse/serial data is available.
03000030h	ERRFLAG	16	R/W	= 0 when no errors have been detected = 1 when an error has been detected.
03000040h	IDLEFLAG	16	R/W	Set to 1 on each pass of the idle loop, approx every 10 usecs. Not cleared by AFGIS.
03000050h	DI_COUNT	16	R	60hz continuous counter, updated by AFGIS.
03000060h	INTOUTMASK	16	R/W	RG-741 to host interrupt enable mask.
03000070h	HOST_FIELD0	16	R/W	Reserved for host use.
03000080h	HOST_FIELD1	32	R/W	Reserved for host use.
030000A0h	ENV_PTR	32	R/W	Address of current graphics environment.
030000C0h	HINT0_AFG_ENTRY	32	R/W	AFGIS display list address. Used by HINT0
030000E0h	HINT1_TMS_ENTRY	32	R/W	TMS assembly code address. Used by HINT1
03000100h	GPTABLE_PTR	32	R	Address of global pointer table.
03000120h	DEFAULT_ENV_PTR	32	R	Address of default environment.
03000140h	DPAGEADDR	32	R	Current display page address.
03000160h	DPAGE	16	R	Current display page number (0,1,...).

Figure 3.4 Fixed RAM Parameters

VRAM

Video RAM, VRAM, holds the image displayed on the video screen. VRAM is normally written to by the TMS34010 graphics processor on the RG-741 as a consequence of AFGIS opcode processing. However, image data can also be downloaded directly into VRAM by the VMEbus host. The beginning of VRAM, 02000000h, corresponds to the top left corner of the video screen. For configurations with two video pages (See Preface) the second video page starts at 02800000h.

VRAM is organized as a 1K x 1K buffer for 8 bits/pixel configurations, and as a 1K x 2K buffer for 4 bits/pixel configurations.

RG-741 Memory (continued)

RS-232 Serial Interface

The RS-232 Serial Interface can be used for a serial mouse (with Microsoft format) or it can be used to connect a serial device to the RG-741. The handshake lines (RTS, DTR, etc.) can be reversed at J8 and J9 to allow use of a flat cable connected to a DB9 connector. The serial interface uses the Signetics 2691 UART, which is a programmable device with many options. The bit assignments for the 2691 registers are shown below.

Programing the 2691 UART

The 2691 Universal Asynchronous Receiver/Transmitter (UART) has quadruple buffered receiver data registers and a fully programmable data format. The baud rate for the receiver and transmitter can be selected from 9 fixed rates. The UART contains eight registers that determine its mode of operation (see Figure 3.5 and Figure 3.6). Refer to the Signetics 2691 UART data sheet for additional information.

ADDRESS	DESCRIPTION	DEFAULT CONTENTS
05000000h	MR1 - Mode Register 1	13h
05000000h	MR2 - Mode Register 2	17h
05000010h	CSR - Channel Status Register	0BBh
05000020h	CR - Command Register	0A5h
05000040h	ACR - Auxillary Control Register	78h
05000050h	IMR - Interrupt Mask Register	04h
05000060h	CTUR - Counter Register High	00h
05000070h	CTLR - Counter Register Low	FFh

Figure 3.5 2691 UART Power Up Register Values

The 2691 UART is configured by the AFGIS firmware at power up as follows:

- 9600 baud
- 8bits/character
- 1 stop bit
- no parity
- Transmit Data line controlled by CTS handshake
- RTS asserted. RTS is deasserted when the receive buffer becomes full.
- DTR always asserted
- DSR always asserted

Use the SERUART opcode to reprogram the 2691.

RG-741 Memory (continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MR1	RxRTS CONTROL	RxINT SELECT	ERROR MODE	PARITY MODE		PARITY TYPE	BITS PER CHAR	
	0=no 1=yes	0=RXRDY 1=FULL	0 = char 1=block	00 = with parity 01 = force parity 10 = no parity 11 = special mode		0 = even 1 = odd	00 = 5 01 = 6 10 = 7 11 = 8	
MR2	CHANNEL MODE		Tx RTS CONTROL	Tx CTS ENABLE	STOP BIT LENGTH			
	00 = normal 01 = auto echo 10 = local loop 11 = remote loop		0=no 1=yes	0=no 1=yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4=0.183 5=0.875 6=0.938 7=1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F=2.000
CSR	RECEIVER CLOCK SELECT				TRANSMITTER CLOCK SELECT			
	ACR (7) = 0: 50 - 38.4k baud ACR(7) = 1: 75 - 19.2k baud				ACR (7) = 0: 50 - 38.4k baud ACR (7) = 0: 50 - 38.4k baud			
CR	MISCELLANEOUS COMMANDS				DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
	see UART data sheet				0 = no 1=yes	0=no 1=yes	0=no 1 = yes	0=no 1=yes
ACR	BRG SET SELECT	COUNTER MODE & SOURCE			POWER DOWN MODE	MPO FUNCTION SELECT		
	0=set1 1=set2	see UART data sheet			0 = on 1=off	see UART data sheet		
ISR	MPI PIN CHANGE	MPI PIN STATE		COUNTER READY	DELTA BREAK	RxRDY/ FULL	TxEMT	TxRDY
	0=no 1=yes	0=low 1 = high	not used	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1 = yes	0=no 1=yes
CTUR	8 MSBs OF COUNTER/TIMER VALUE							
CTLR	8 LSBs OF COUNTER/TIMER VALUE							

Figure 3.6: 2691 UART Register Contents

Keyboard Interface

An AT style keyboard can be connected to the RG-741 at J5. An adapter cable is required to connect from the 2x5 header on the RG-741 to the keyboard 5 pin DIN connector. AFGIS firmware decodes the keyboard scan codes, stores the ASCII codes in RAM, and informs the VMEbus host of available keyboard data via an interrupt or a polling register in Fixed RAM.

RG-741 Memory (continued)

Video DAC (Bt478)

RS-343 video is generated by the RG-741 with a Bt478 type Video DAC. The Video DAC has a 256 x 24 color look up table, allowing a user to select 256 colors from a palette of 16 million. The Video DAC registers are located as shown below:

ADDRESS	DESCRIPTION	ADDRESS	DESCRIPTION
05400000h	Write Address Register	05420000h	Pixel Read Mask Register
05410000h	Data Register	05430000h	Read Address Register

Figure 3.7 Video DAC Registers

Control Register

The RG-741 has a Control Register to control on-board hardware functions. The Control Register is located at 05800000h and has the following bit assignments. Use the CONTREG opcode to modify the contents of the Control Register.

	D15	Red Led	0 = off, 1= on
	D14	Debug Enable	0 = off, 1= on
*	D13	ROMDIS	0 = EPROM 1= RAM
*	D12	Vsync Polarity	0 = active low 1 = active high
*	D11	Hsync Polarity	0 = active low 1 = active high
	D10	Not used	
	D9	Split/Scroll	0 = 640/800 1 = 1024 x 8/800 x 8
	D8	Green Led	0 = off, 1= on
*	D7	Sync on Green	0 = sync on green 1 = no sync on green
	D6	Keyboard Serial Data	
	D5	Keyboard clock	
	D4	Memory Devices Installed	0 = 1 Mbyte 1 = 4 Mbyte
	D3	8 bit video.	0 = 4 bit video 1 = 8 bit video
	D2	Not used	
	D1	Not used	
	D0	Shift Clock enable	0 = off 1 = enabled

* These bits are user configurable

Figure 3.8 Control Register Bit Assignments

RG-741 Memory (continued)

Remapping DRAM with ROMDIS (D13)

The ROMDIS bit, D13, in the Control Register remaps DRAM to the top portion of the address space (see Figure 3.9). This feature allows code to be downloaded into DRAM for execution independent of AFGIS firmware. If 1/2 Mbyte of DRAM is installed, DRAM is mapped to the top of the address space, starting at FFC00000h. If 2 Mbytes of DRAM are installed, DRAM starts at FF000000h.

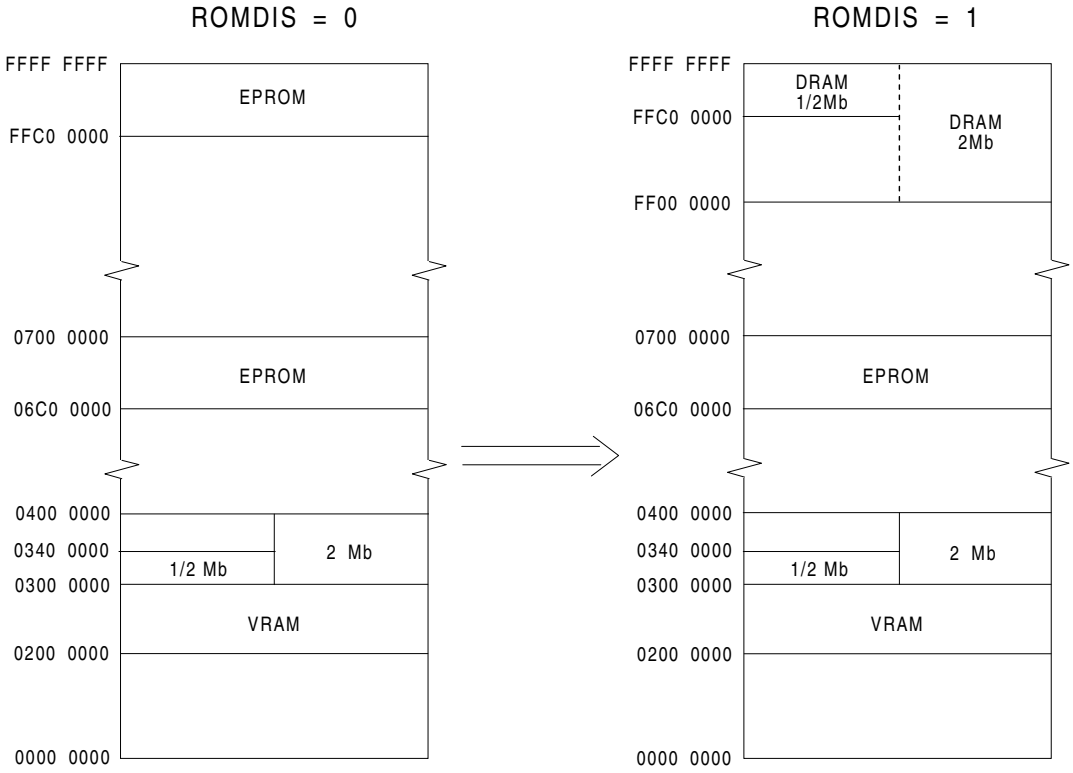

Figure 3.9 EPROM/DRAM Swap

LEDs

Three LEDs on the RG-741 provide status information (see Figure 2.1).

Red LED: The red LED lights when an error is detected. It can be user programed with the LED opcode.

Yellow LED: The yellow LED lights when the board is accessed by the VMEbus.

Green LED: The green LED blinks when the TMS34010 is in the idle loop. It can be user programed with the LED opcode.

Interrupts

Interrupts are sent to the RG-741 from the VMEbus host to initiate display list processing, to run TMS34010 code, and to reset the RG-741. Interrupts are sent to the RG-741 by setting the appropriate bits in the HSTCTL register, located at VMEbus Host Interface Register address xxxx06h.

Interrupts can also be sent from the RG-741 to the VMEbus host to indicate the completion of display list processing; to indicate that RS-232, mouse, or keyboard data is ready; to indicate a 60Hz interrupt, or to indicate an error condition.

Interrupts are sent to the VMEbus from the RG-741 by setting the appropriate bits in HSTCTLL and by selecting the appropriate IRQ line (1-7) with jumper J1. The contents of the 8-bit interrupt vector register, located at TMS34010 address 06400000h, are placed on the data bus in response to an interrupt acknowledge signal. The interrupt register must first be programed by the VMEbus host with the desired vector.

Interrupts to the RG-741 from the VMEbus

Two types of interrupts can be sent to the RG-741 from the host CPU via the HSTCTL register: host interrupts and non-maskable interrupts.

BIT	NAME	DESCRIPTION
15	HLT	Halts TMS34010 processing
14	CF	Flushes the cache
13	LBL	Lower byte last
12	INCR	Increments address after each read
11	INCW	Increments address after each write
10		reserved
9	NMIM	Selects the mode for the nonmaskable interrupt
8	NMI	Enables the nonmaskable interrupt
7	INTOUT	Sends output interrupt from TMS34010 to host
4-6	MSGOUT	Buffers an output message code
3	INTIN	Sets input interrupt from host to TMS34010
0-2	MSGIN	Buffers an input message code

Figure 3.9 HSTCTL Bit Assignments

***Interrupts to the RG-741 from the VMEbus** (continued)*

Host Interrupts

Host interrupts are sent to the RG-741 via the VMEbus, and are used to initiate display list processing and execute TMS34010 code. A host interrupt is asserted by setting bit D3 (INTIN)=1 in the TMS34010 HSTCTL register. A host interrupt is identified by bits D(0-2) (MSGIN) in the HSTCTL register. Use HINT0 to execute a display list starting at the address contained in HINT0_AFG_ENTRY located at addresss 030000C0h (its default value is 03100000h). HINT0 is asserted by writing 0008h to the HSTCTL register at the -PS0 default address (E00006h). HINT1 is asserted by writing 0009h to HSTCTL. Use HINT1 to execute TMS34010 assembly code at the address contained in HINT1_TMS_ENTRY located at address 030000E0h (its default value is also 03100000h).

MSGIN NUMBER	MSGIN NAME	HSTCTL D2	HSTCTL D1	HSTCTL D0	DESCRIPTION
0	HINT0	0	0	0	Process AFGIS opcodes beginning at the address specified in HINT0_AFG_ENTRY (at RAM location 0300 00C0h). The default address in HINT0_AFG_ENTRY is 03100000h.
1	HINT1	0	0	1	Process TMS34010 opcodes at address specified in HINT1_TMS_ENTRY (at RAM location 0300 00E0h). The default address in HINT1_TMS_ENTRY is 03100000h.
2	HINT2	0	1	0	reserved
3	HINT3	0	1	1	reserved
4	HINT4	1	0	0	reserved
5	HINT5	1	0	1	reserved
6	HINT6	1	1	0	reserved
7	HINT7	1	1	1	reserved

Figure 3.10 Host Interrupts to RG-741

Resetting The RG-741 With The NMI Interrupt

An NMI interrupt with message value 1 may be used to abort display list processing, and cause the RG-741 to enter the idle loop. NMI 1 does not affect DRAM parameters.

An NMI interrupt with a message value of 0 totally resets the RG-741, putting it into a power up condition.

An NMI interrupt is issued by setting the NMI bit, D8, in the HSTCTL register and by setting the appropriate message bits in D0-D2.

Interrupts to the VMEbus from the RG-741 (continued)

The RG-741 can send an interrupt to the VMEbus host by setting D7=1 in HSTCTLL along with a 3 bit code (D4 - D6) identifying the interrupt (see Figure 3.11). The interrupts are individually enabled or disabled by setting the corresponding bits in the INTOUTMASK RAM location (03000060h). The code (or message number) for the interrupt is determined by bits D4-D6 in the HSTCTL register and identifies 1 of 8 interrupts. The VMEbus interrupt service routine would normally read the HSTCTL register to determine which of the eight interrupts occurred. *On exit, the interrupt service routine **must** clear HSTCTL bit D7 (set D7=0), as the RG-741 will not issue another interrupt until bit D7 in HSTCTL has been **cleared.***

MSGOUT NUMBER	MSGOUT NAME	INTOUTMASK BIT	HSTCTL D6	HSTCTL D5	HSTCTL D4	DESCRIPTION
0	RGIOUT0	D0	0	0	0	An AFGIS EODL instruction has been executed.
1	RGIOUT1	D1	0	0	1	A character is ready from the keyboard port.
2	RGIOUT2	D2	0	1	0	Data is ready from the serial/mouse port.
3	RGIOUT3	D3	0	1	1	An error has occurred and is recorded in DRAM.
4	RGIOUT4	D4	1	0	0	An interrupt is generated at approximately 60 Hz.
5	RGIOUT5	D5	1	0	1	Reserved
6	RGIOUT6	D6	1	1	0	Reserved.
7	RGIOUT7	D7	1	1	1	Reserved.

Figure 3.11 Interrupt Output Messages to VMEbus

Note: HSTCTL is a 16 bit register located at the -PS0 default address E00006h, and has the bit assignments shown in Figure 3.9. When viewed from the TMS34010 side, the HSTCTL appears as two 16 bit registers, HSTCTLL and HSTCTLH, with each register containing half the data bits (in the same bit positions as shown for HSTCTL) that are in HSTCTL. HSTCTLL is located at C0000F0h, and HSTCTLH is located at C000100h.

BIT	NAME	DESCRIPTION
8-15	Reserved	Not Used
7	INTOUT	Sends output interrupt from TMS34010tohost
4-6	MSGOUT	Buffers an output message code
3	INTIN	Sets input interrupt from host to TMS34010
0-2	MSGIN	Buffers an input message code

Figure 3.12 HSTCTLL

BIT	NAME	DESCRIPTION
15	HLT	Halts TMS34010 processing
14	CF	Flushes the cache
13	LBL	Lower byte last
12	INCR	Increments address after each read
11	INCW	Increments address after each write
10		reserved
9	NMIM	Selects the mode for the nonmaskable interrupt
8	NMI	Enables the nonmaskable interrupt
0-7	Reserved	Not Used

Figure 3.13 HSTCTLH

Interrupts to the VMEbus from the RG-741 (continued)

The TMS34010 generates an interrupt to the VMEbus when HSTCTLL bit D7 is set to 1 and if the corresponding message value is enabled by the contents of Fixed RAM location INTOUTMASK. When D7=1 in HSTCTL, the HINT line, which is connected to the VMEbus interrupt line via a PAL, is enabled active low, initiating the interrupt. The VMEbus interrupt line used by the PAL (IRQ 1-7) is selected using jumper J1. An 8-bit interrupt vector register, located at TMS34010 address 06400000h, is programmed by the VMEbus host with its appropriate vector, and the vector is placed on the data bus in response to an interrupt acknowledge signal.

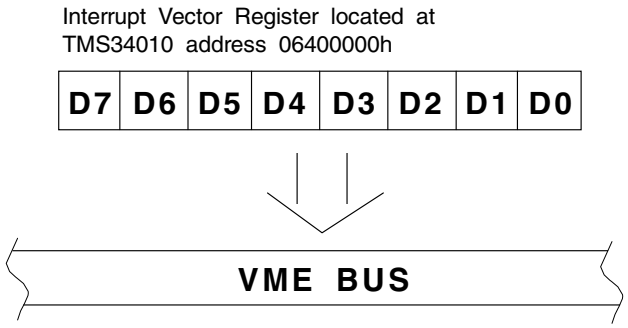

Figure 3.14 Interrupt Vector Register

Coordinate System

Coordinate System

The screen coordinates are shown in Figure 3.15. 0,0 is in the upper left, x increases to the right, and y increases downward.

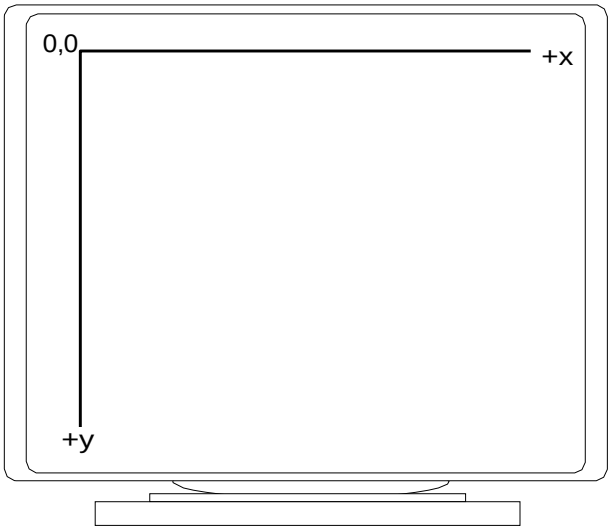

Figure 3.15 Display

4. Specifications

This chapter contains information on the following topics:

Operating Environment

Operating Temperature: 0°C to 55°C

Storage Temperature: -40°C to 65°C

Relative Humidity: 0% to 95% (non-condensing)

Altitude: 7500 ft.

DC Power Requirements

+5V at 3.0 Amps

+12V at 0.2 Amps

-12V at 0.2 Amps

Video Output

Analog 1.0V, RS-343 video , with sync on green and sync polarity (options) is output at DB15F, J10.

Video Timing

The RG-741 video timing is resolution dependent, as shown in Figures 4.1 through 4.3

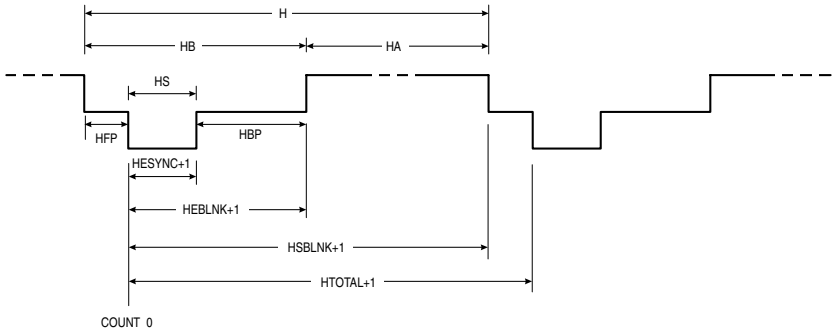

Figure 4.1 Horizontal Video Timing

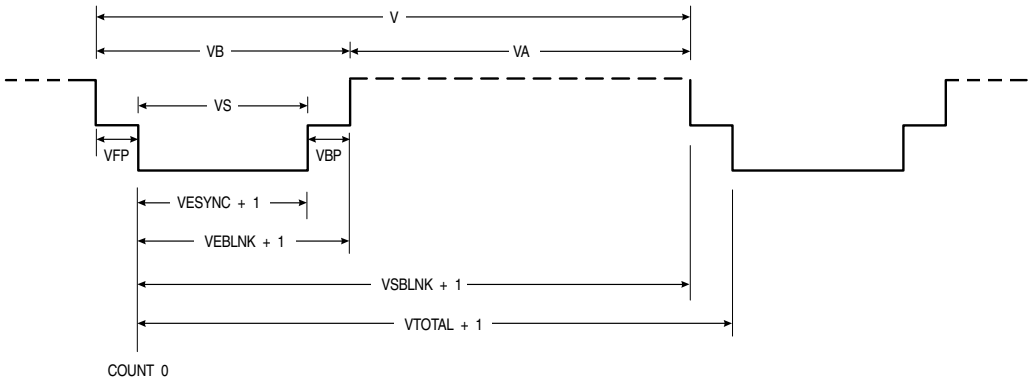

Figure 4.2 Vertical Video Timing

	640h x 480v	800 x 600	1024 x 768
PCLOCK	25.175MHz	36.000MHz	63.960MHz
HFREQ	31.468KHz	35.156KHz	48.454KHz
H	31.777mS	28.444mS	20.638mS
HS	3.495mS	2.000mS	1.001mS
HBP	1.90mS	3.555mS	2.877mS
HA	25.422mS	22.222mS	16.010mS
HFP	0.953mS	0.666mS	0.758mS
HB	6.333mS	6.222mS	4.628mS
VFREQ	59.940Hz	56.250Hz	59.968Hz
V	16,683mS	17,777mS	16,675mS
VS	63mS	56mS	82mS
VBP	1,016mS	625mS	661mS
VA	15,253mS	17,060mS	15,850mS
VFP	349mS	28mS	82mS
VB	1,430mS	717mS	825mS
HESYNC	10 (000A)	8(0008)	7 (0007)
HEBLNK	16 (0010)	24 (0018)	30 (001E)
HSBLNK	96 (0060)	124 (007C)	158 (009E)
HTOTAL	99 (0063)	127 (007F)	164 (00A4)
VESYNC	1 (0001)	1(0001)	3 (0003)
VEBLNK	33 (0021)	23(0019)	35 (0023)
VSBLNK	513 (0201)	623 (026F)	803 (0323)
VTOTAL	524(020C)	624 (0270)	807 (0327)

Figure 4.3 Video Timing

Appendix A: Interface PAL Equations

RG-741 Interface PAL Set, U11 and U15.

This appendix contains the PAL equations, written in PALASM format, for the -PS0 PAL set. The PALs U11 and U15 may be reprogrammed by the user to locate the RG-741 at a different location in VMEbus address space.

The RG-741 is located in VMEbus address space with the interface PALs U11 and U15. The U11 and U15 decode a 256 byte page in VMEbus address space. The RG-741 Host Interface Registers are located in this 256 byte page.

The default PAL set, U11 and U15 (-PS0) locates the RG-741 at E00000h or at D00000h, depending on the jumper configuration of J3.

U11 decodes the AM lines and the upper 12 address lines, A12-A23. The AM decode determines the data transfer modes that the RG-741 will respond to. The -PS0 PAL U15 decodes the following AM codes:

3E Standard Supervisory Program Access

3D Standard Supervisory Data Access

3A Standard Non-privileged Program Access

39 Standard Non-privileged Data Access

The address line A12-A23 decode a 4K block of memory. Inthe case of the -PS0 PAL, U15 decodes a 4K block of memory starting at E00000h or D00000h, depending on the jumper configuration of J3.

U11 decodes address lines A8-A11, which selects a 256 byte page within the 4K block decoded by U15. In the case of the -PS0 PAL, U15 decodes the first page (0) of 256 bytes in the 4K block. Thus, the RG-741 is located at E00000h or at D00000h.

```
Title     RG-741 High Address Decode PAL     Blow Count _____________
Pattern   hiaddr.pds
Revision  1.0                                Checksum _____________
Author    Tim Kelly
Company   Rastergraf, Inc.
Date      22 JAN 1993

;  RGI PART NUMBER:      HIADDR
;  PAL Type:             20L8B (15 nsec)
;  Board Location:       U11
;  Schematic Page:       1
;  DEFAULT ADDR: E00000H;  W/JUMPER INSTALLED IN J3,  ADDR. = D00000H

Chip  HIADDR            PAL20L8

; 1[I]        2[I]        3[I]        4[I]        5[I]        6[I]
 AM5         AM4         AM3         AM2         AM1         AM0

; 7[I]        8[I]        9[I]        10[I]       11[I]       12[GND]
 VA23        VA22        VA21        VA20        VA19        GND

;13[I]       14[I]       15[O]       16[I/O]     17[I/O]     18[I/O]
 VA18        VA17       /HIDEC       VA16        VA15        VA14

;19[I/O]     20[I/O]     21[I/O]     22[O]       23[I]       24[VCC]
 VA13        VA12       /S0          nc           nc          VCC

Equations
; 24 BIT ADDR:
;            3E  -STANDARD SUPERVISORY PROGRAM ACCESS
;            3D  -STANDARD SUPERVISORY DATA ACCESS
;            3A  -STANDARD NONPRIVILEGED PROGRAM ACCESS
;            39  -STANDARD NONPRIVILEGED DATA ACCESS

; 24 BIT WITH NO JUMPER

HIDEC =
    /S0 *  AM5 *  AM4 *  AM3 *  AM1 * /AM0 *
    VA23 *  VA22 *  VA21 * /VA20 *
    /VA19 * /VA18 * /VA17 * /VA16 *
    /VA15 * /VA14 * /VA13 * /VA12
    + /S0 *  AM5 *  AM4 *  AM3 * /AM1 *  AM0 *
    VA23 *  VA22 *  VA21 * /VA20 *
    /VA19 * /VA18 * /VA17 * /VA16 *
    /VA15 * /VA14 * /VA13 * /VA12

; D00000h
   +  S0 *  AM5 *  AM4 *  AM3 *  AM1 * /AM0 *
    VA23 *  VA22 * /VA21 *  VA20 *
    /VA19 * /VA18 * /VA17 * /VA16 *
    /VA15 * /VA14 * /VA13 * /VA12
   +  S0 *  AM5 *  AM4 *  AM3 * /AM1 *  AM0 *
    VA23 *  VA22 * /VA21 *  VA20 *
    /VA19 * /VA18 * /VA17 * /VA16 *
    /VA15 * /VA14 * /VA13 * /VA12
```

```
Title     RG-741 Low Address Decode PAL      Blow Count _______
Pattern   loaddr.pds
Revision  1.0                                Checksum   _______
Author    Tim Kelly
Company   Rastergraf, Inc.
Date      22 JAN 1993

;  PAL Type:       20L8B (15 nsec)
;  Board Location: U15
;  Schematic Page: 1

Chip      LOADDR          PAL20L8

 ; 1[I]     2[I]       3[I]     4[I]     5[I]       6[I]
   /S0      /HALT     /HIDEC   /LWORD    /AS       /DS1

 ; 7[I]     8[I]       9[I]     10[I]    11[I]     12[GND]
  /DS0      /WR       VA11     VA10      VA9        GND

 ;13[I]    14[I]      15[O]   16[I/O]  17[I/O]    18[I/O]
   VA8     /RESET     /HRD     /HCS     /HUDS      /HLDS

;19[I/O]  20[I/O]    21[I/O]   22[O]    23[I]     24[VCC]
 /DOUT     /DEN      /IACK     /HWR    /DTACK      VCC

Equations

HCS  = /S0   *  HIDEC * /IACK *  AS * /RESET *
       /VA11 * /VA10 * /VA9   * /VA8
     +  S0   *  HIDEC * /IACK *  AS * /RESET *
       /VA11 * /VA10 * /VA9   * /VA8
     + /HALT *  RESET

HWR  =  WR *  DS0 * /RESET * /DTACK
     +  WR *  DS1 * /RESET * /DTACK

HRD  = /WR *  DS0 * /RESET
     + /WR *  DS1 * /RESET

HLDS =  DS0 *  RESET

HUDS =  DS1 * /RESET

DEN  =  HCS * /RESET

DOUT =  HCS *  DS0 * /RESET * /WR
     +  HCS *  DS1 * /RESET * /WR
```

APPENDIX B

Chapter Contents:

B.1 Transferring Data from 680x0 memory to TMS34010 memory

The following discussion describes how data should be transferred from 680x0 memory via the VMEbus to TMS34010 memory on Rastergraf graphics boards.

This discussion is primarily intended for users who want to develop their own interface to the graphics board.

B.2 Data in 680x0 Memory

Data in 680x0 memory is typically described as shown in Figure B.1, and can be bytes, words, or longs. Bytes are numbered left to right (in the direction of increasing memory) and are identified as byte(0), byte(1), byte(2), and byte(3) and have the corresponding 680x0 hex addresses xxxxx0, xxxxx1, xxxxx2, and xxxxx3 (or xxxxxxx0, etc. for 32 bit addressing mode).

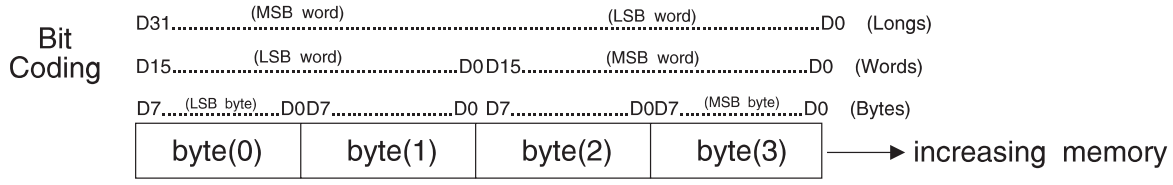

Figure B.1 680x0 Bit and Byte Numbering Conventions

Sixteen bit data (two bytes) are transferred across the VMEbus as shown in Figure B.2.

680x0	VMEbus Data Lines	
Byte Locations	**D15-D8**	**D7-D0**
byte(0-1)	byte (0)	byte (1)
byte(2-3)	byte (2)	byte (3)

Figure B.2 16 Bit Data Transfers Across the VMEbus

B.2 Data in 680x0 Memory *(continued)*

Data may only be transferred to or from Rastergraf TMS34010 based graphics boards 16 bits at a time, and only with one of the two byte sets; byte(0), byte(1) or byte(2), byte(3). Figure B.3 shows how a long (32 bits) would be transferred from 680x0 memory to long aligned TMS34010 memory (the start address in TMS34010 memory could be any bit value, but AFGIS firmware requires that the AFGIS opcodes be loaded on word boundaries).

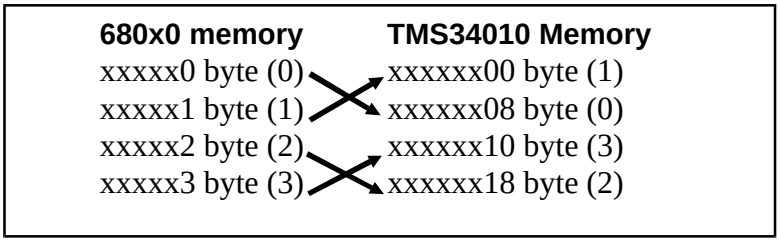

Figure B.3 32 Bit Data Transfers

In Figure B.1, byte(0) is the lsb byte in the byte sequence byte(0), byte(1), byte(2), and byte(3). For words, byte (0), byte(1) is the lsb word, and byte(2), byte(3) is the msb word (the next word). For a long, all four bytes are used to represent the long, and the byte pair byte(0), byte(1) is the msb word of the long, and byte pair byte(2), byte(3) is the lsb word of the long.

The two byte pairs byte(0), byte(1) and byte(2), byte(3) that may be transferred across the VMEbus to the graphics board have a different meaning for the data types bytes, words, and longs.

Our objective, for successful data transfer, is to maintain the order of bytes, words, and longs when the data is transferred from 680x0 memory to TMS34010 memory.

Data in TMS34010 memory is typically described as shown in Figure B.4.

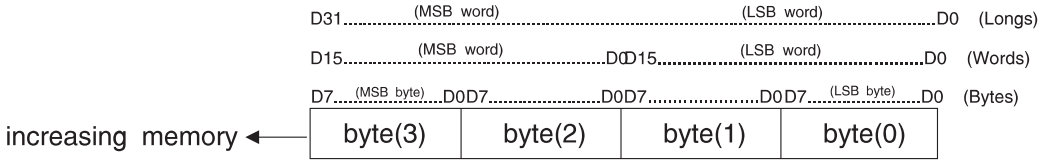

Figure B.4 TMS34010 Bit and Byte Numbering Conventions

In Figure B.4, byte(0) is the lsb byte in the byte sequence byte(0), byte(1), byte(2), and byte(3). For words, byte(1), byte(0) is the lsb word, and byte(3), byte(2) is the msb word (the next word). For a long, all four bytes are used to represent the long, and byte pair byte(3), byte(2) is the msb word of the long, and byte(1), byte(0) is the lsb word of the long.

B.2 Data in 680x0 Memory (continued)

As can be seen by examining Figures B.1, B.2, B.3, and B.4, data transferred from 680x0 memory directly to TMS34010 memory without modification only meets our objective if the data being transferred are words.

B.3 Transferring Bytes

If the data being transferred are bytes, it is evident that the byte pairs byte(0), byte(1) or byte(2), byte(3) end up in the wrong order in TMS34010 memory. The solution is to swap the order of the bytes before the byte pair is transferred across the VMEbus as shown in Figure B.5.

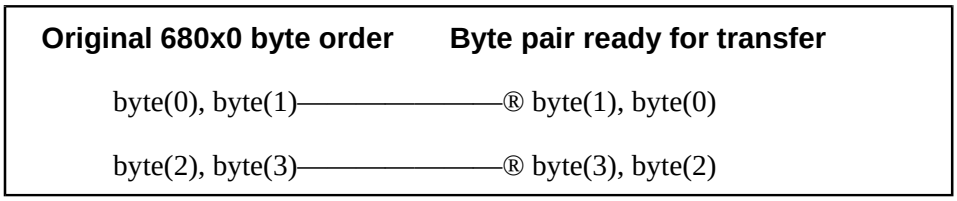

Figure B.5 Transferring Bytes

B.4 Transferring Words

If the data being transferred across the VMEbus are words, the data may be transferred without modification, as can be seen by examining Figures B.1, B.2, B.3, and B.4.

B.5 Transferring Longs

If the data being transferred across the VMEbus are longs, it is evident from Figures B.1, B.2, B.3, and B.4 that the msb and lsb words of the long are interchanged if transferred to TMS34010 memory directly from 680x0 memory without additional processing. The solutions is to transfer the lsb word first [byte(2), byte(3)], and then transfer the msb word [byte(0), byte(1)] as shown in Figure B.6.

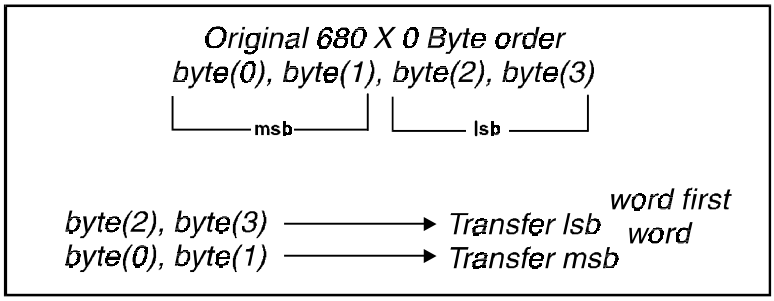

Figure B.6 Transferring a Long Word

