

ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Visit our website - *Click HERE*

USER'S MANUAL

PT-PMC334
Quad Communications Controller

Document Number 126P0319

REVISION CONTROL

Rev	Reason	Pages Affected	Date
10	Initial Release	All	11/23/98

Copyright Notice

© 1998 by Performance Technologies, Incorporated.
315 Science Parkway, Rochester, New York 14620
Printed in USA.

Trademarks

CompactPCI is a trademark of the PCI Industrial Computer Manufactures' Group.

All other brands or names are trademarks of their respective holders.

All rights reserved. This document is the sole property of Performance Technologies, Incorporated.

PERFORMANCE TECHNOLOGIES, INC

NOTICE

This document presents information for users of the Performance Technologies, Incorporated Model PT-PMC334 PMC Quad Communications Controller.

Although the information contained within this document is considered accurate and characteristic of the subject product, Performance Technologies, Incorporated reserves the right to make changes to this document and any products described herein to improve reliability, function, or design. Performance Technologies, Incorporated does not assume any liability arising out of the application or use of any product or circuit described herein.

No part of this document may be copied or reproduced in any form or by any means without the prior permission of Performance Technologies, Incorporated.

FCC Declaration of Conformance

The following products:

Model PT-PMC334-10912 (RS-442)	Front Panel I/O RS422/RS449 Four Port
Model PT-PMC334-10997 (RS-442) Rear I/O	Rear Panel I/O RS422/RS449 Four Port
Model PT-PMC334-10962 (RS-232C)	Front Panel I/O RS232C Four Port
Model PT-PMC334-10998 (RS-232C) Rear I/O	Rear Panel I/O RS232C Four Port
Model PT-PMC334-10963 (V.35)	Front Panel I/O V.35 Four Port
Model PT-PMC334-10999 (V.35) Rear I/O	Rear Panel I/O V.35 Four Port

have not been tested within the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules.

Safety Information

This section is provided as a summary of the safety recommendations throughout this manual. Performance Technologies, Incorporated (PTI) recommends that all safety precautions are followed to prevent harm to yourself or the equipment. Please follow all warnings marked on the equipment.

Safety Precautions

- Follow all warnings and instructions marked on the equipment.
- Ensure that the voltage and frequency of your power source matches the voltage and frequency inscribed on the equipments electrical rating label.
- Never push objects of any kind through the openings in the equipment. Dangerous voltages may be present. Conductive foreign objects could produce a short circuit that could cause fire, electrical shock, or damage your equipment.

Symbols

The following symbols appear in this document.



CAUTION: There is risk of personal injury or equipment damage. Follow the instructions.



WARNING: Hazardous voltages are present. To reduce the risk of electric shock and danger to personal heath, follow the instructions.

PERFORMANCE TECHNOLOGIES, INC

Table of Contents

Section 1 INTRODUCTION 1

Scope **1**

Required Additional Documents 2

Model Designations 3

Features 4

MC68360 4

PCI9080 5

Serial Ports 6

Other Features 6

Glossary 7

Section 2 INSTALLATION 9

Configuring the PT-PMC334 10

Optional Clock 15

PT-PMC334 Installation 17

Installing the PT-PMC334 card 17

Logic Analyzer Connectors **19**

Section 3 FUNCTIONAL DESCRIPTION 21

PT-PMC334 Block Diagram **22**

MC68360 Quad Integrated Communications Controller (QUICC) **23**

QUICC Setup 23

QUICC Interrupts 29

Timers 30

Resets 30

Optional BDM Port **31**

PCI Interface **31**

Endian Conversion 31
PCI9080 Setup 32
Modes Of Operation 36
PCI User In/Out 37
Local bus Arbitration Priority 38
PCI9080 Interrupt Requests 38
DRAM Array 39
Timing 39
Fast Page Mode 40
Parity 40
Flash PROM 40
Line Drivers/Receivers 40
Frontpanel RS-232C 41
Frontpanel RS-442 41
Frontpanel V.35 41
Clock Steering 41
Connector & Cabling 42
RS-232C Cabling 42
RS-232C Backpanel I/O Connections 46
RS-449 Cabling 47
RS-449 Backpanel I/O Connections 50
RS-530 Cabling 52
V.35 Cabling 56
V.35 Cabling Backpanel I/O Connections 59
Debug Port (P3 on RS232/422 and P4 on V.35 card) 60
Registers 61
TCSL Register 61
RCSL Register 63
Status Register 63
QUICC Interrupt Register 64
PMC Interrupt Register 65
Misc Register 66
Board Configuration Register 67

PROM Write Enable Register. 68
QUICC I/O Ports 69
Power Budget 74
Section 4 APPENDICES 75
Product Warranty 75
Product Return Procedure 76
Product Support 78
Installation Notes 79
PT-PMC334 Initialization 80
quicc.i 80
PLX9080.i 89
PMC334.i 91
init334.s 93
Background Debug Port Pin Assignments 106
Logic Analyzer Connection Pin Assignments 107
PMC Pin Assignments 112
Section 5 INDEX 119

Section 1

INTRODUCTION

Scope

This document provides information for users of the Model PT-PMC334 PMC Quad Communications Controller.

This manual is not intended as a stand-alone document. If you plan on writing software for this product the references cited in the Applicable Documents section are necessary to have a complete understanding of all the features and functions of the hardware.

This manual does provide the information necessary to understand the operation and features of the board. A prime objective was to answer those questions raised by system developers as to whether the PT-PMC334 will complement their architecture. When combined with the required documentation listed below, a complete description of PT-PMC334 facilities are presented.

Section 1 Provides an introduction and general overview of the PT-PMC334. It is intended as a quick summary of PT-PMC334 features and provides a framework for the rest of the document.

Section 2 Describes the physical setup and installation procedures.

Section 3 The Functional Description provides a detailed description of PT-PMC334 architecture and functional blocks.

Section 4 Appendices.

Section 5 Index.

Required Additional Documents

a. PCI Local Bus Specification; Revision 2.1, 1995. PCI Special Interest Group; P. O. Box 14070, Portland, OR 97214.

b. PICMG 2.3 R2.1 PMC on CompactPCI Specification; March 12, 19987 PCI Industrial Computer Manufactures' Group.

c. MC68360 PowerQUICC, MPC860 User's Manual; MC860UM/AD; Motorola Incorporated. Motorola Literature Distribution; P.O. Box 20912; Phoenix, AZ 85036.

d. PLX PCI9080 Datasheet[1]; Product Catalog. PLX Technology; 625 Clyde Avenue; Mountain View, CA 94043.

e. PT-PMC334 Prom Monitor User's Manual; Part Number 106P0842_, Performance Technologies, Incorporated, 315 Science Parkway, Rochester, NY 14620.

f. IEEE P1386.1/Draft 2.0 (April 4, 1995)[2]; Physical and Environmental Layers for PCI Mezzanine Cards, IEEE--The Institute of Electrical and Electronics Engineers, Inc. IEEE Customer Service, 445 Hoes Lane, P.O. Box 1331 , Piscataway, NJ 08855-1331 USA

g. CMC: IEEE P1386/Draft 2.0 (April 4, 1995)[2]; Common Mezzanine Card Family, IEEE--The Institute of Electrical and Electronics Engineers, Inc. IEEE Customer Service, 445 Hoes Lane, P.O. Box 1331 , Piscataway, NJ 08855-1331 USA

---

1 This can be found at www.plxtech.com/toolbox/9080.htm.

2 This can be found at http://www.forcecomputers.com/technology/draft/pmc_draft.pdf with more information at http://www.forcecomputers.com/technology/papers/vme.htm.

Model Designations

The PT-PMC334 is available in the following model configurations:

Model PT-PMC334-10912 (RS-442) Front Panel I/O RS422/RS449 Four Port, PowerQUICC 25MHz, 4-MB DRAM, on board, no parity

Model PT-PMC334-10997 (RS-442) Rear I/ORear Panel I/O RS422/ RS449 Four Port, PowerQUICC 25MHz, 4-MB DRAM, on board, no parity

Model PT-PMC334-10962 (RS-232C) Front Panel I/O RS232C Four Port, PowerQUICC 25MHz, 4-MB DRAM, on board, no parity

Model PT-CPC334-10998 (RS-232C) Rear I/ORear Panel I/O RS232C Four Port, PowerQUICC 25MHz, 4-MB DRAM, on board, no parity

Model PT-PMC334-10963 (V.35) Front Panel I/O V.35 Four Port, PowerQUICC 25MHz, 4-MB DRAM, on board, no parity

Model PT-PMC334-10999 (V.35) Rear I/ORear Panel I/O V.35 Four Port, PowerQUICC 25MHz, 4-MB DRAM, on board, no parity

The following accessories are available for the PT-PMC334:

Model PT-ACC334-10622 4-port V.35 Hydra Style Cable

Model PT-ACC334-10623 4-port RS-232C Hydra Style Cable

Model PT-ACC334-10722 4-port RS-449 Hydra Style Cable (Male)

Model PT-ACC334-10741 4-port RS-449 Hydra Style Cable (Female)

Features

MC68360

- CPU32+ Processor (4.5 MIPS at 25 MHz)
  32-Bit Version of the CPU32 Core (Fully Compatible with the CPU32)
  Background Debug Mode
  Byte-Misaligned Addressing
- Four General Purpose Timers
  Superset of MC68302 Timers
  Four 16-Bit Timers or Two 32-Bit Timers
- Two Independent DMAs (IDMAs)
  Single Address Mode for Fastest Transfers
  Buffer Chaining and Auto Buffer Modes
  Automatically Performs Efficient Packing
- System Integration Module (SIM60)
  Bus Monitor
  Double Bus Fault Monitor
  Software Watchdog
  Periodic Interrupt Timer
  Low Power Stop Mode
  Breakpoint Logic Provides On-Chip Hardware Breakpoints
- Four Serial Communication Controllers (SCC)
  HDLC/SDLC™
  Signaling System #7
  Binary Synchronous Communication (BISYNC)
  Totally Transparent (Bit Streams)
  Totally Transparent (Frame Based with Optional Cyclic Redundancy Check (CRC))
  Asynchronous HDLC
  DDCMP™
  V.14
  X.21

- Two Serial Management Controllers (SMC)
  UART
  Transparent
  General Circuit Interface (GCI) Controller

- Communications Processor Module (CPM)
  RISC Controller
  224 Buffer Descriptors
  Supports Continuous Mode Transmission and Reception on All Serial Channels
  2.5 KBytes of Dual-Port RAM
  14 Serial DMA Channels

- Four Baud Rate Generators
  Independent (can be connected to any SCC or SMC)
  Allows Changes During Operation
  Autobaud Support Option

PCI9080

- PCI Version 2.1 Complaint
- Universal PCI signalling supported (The PMC334 is keyed to allow operation in both 3.3 Volt or 5 Volt PCI signalling level systems)
- PCI Bus Master Transfers up to 132 MBsec
- Two Independent DMA Channels
- Bi-Directional Chaining DMA Controller
- Four Bi-Directional FIFOs
- Eight 32-bit Mailboxes and Two 8-bit Doorbell Registers
- I_20 Compatible Messaging Unit
- Upward Compatibility w/ PCI 9060 PLX Interface.

Serial Ports

- Full RS-232C, RS-449, RS-530, or V.35 Support on All Four Ports.
- Optional On-Board Clock Provision
- Internal or External Serial Data Clocks
- Five Modem Control Signals per Port (Seven for V.35)

Other Features

- 1 Mbyte (8Mbit) Flash PROM (boot)
- On-board RS-232 Debug Port
- Mechanical - PMC Single Width, 5-V, 32-bit PCI Card, IEEE P1386/Draft 2.0 and P1386.1/Draft 2.0
- PCI Compliance Checklist Rev. 2.0B Compliant
- Compact PCI Rev 2.1 Compliant
- Compliant with PICMG 2.3 P 1.0 for JN4 pinouts
- 4MB DRAM (Dual Ported RAM)

Glossary

Bps .....Bytes per second.

bps .....Bits per second.

CPCI.....Compact PCI (Peripheral Component Interconnect)

CPU.....Central Processing Unit.

DMA .....Direct Memory Access, hardware controller block data transfers.

DMAC.....Direct Memory Access Controller.

DRAM.....Dynamic Random Access Memory.

half-word.....In this manual, this term indicates a 16-bit value.

HDLC.....High-Level Data Link Control.

Keying Holes...Holes in the PMC daughter card that allow the card to mate with 5 Volt or 3.3 Volt PCI signalling level hosts.

Lbus.....Local PT-PMC334 onboard bus.

MByte.....Megabyte.

MB/sec .....Megabytes per second.

MPU .....Micro-Processor Unit.

ms. .....Millisecond.

PCI9080 .....PCI Bus Master Interface Chip.

QUICC .....Quad Integrated Communications Controller.

reserved .....The term used for bits, bytes, fields, code values, etc. that are set aside for future use.

SCC .....QUICC Serial Communications Controller.

SDLC .....Synchronous Data Link Control.

SMC .....QUICC Serial Management Controllers.

word .....In this manual, this term indicates a 32-bit value.

xxh.....Numbers followed by lowercase h are hexadecimal values. All other numbers are decimal values To help with readability, large hexadecimal values use a '.' to indicate 16 bit (4 nibble) boundaries. In this document, the period does **NOT** indicate a decimal place in a hexadecimal number.

Section 1 INTRODUCTION

Section 2

INSTALLATION

Installation is a 3 step process:

Step 1 Configure the PT-PMC334 for your application.

Step 2 Power down the PMC mother board or chassis.

Step 3 Install the PT-PMC334.

Step 4 Power up the PMC mother board or chassis.

Configuring the PT-PMC334

Figure 1: PT-PMC334 RS232 & RS442 Layout & Jumpers

TOP SIDE

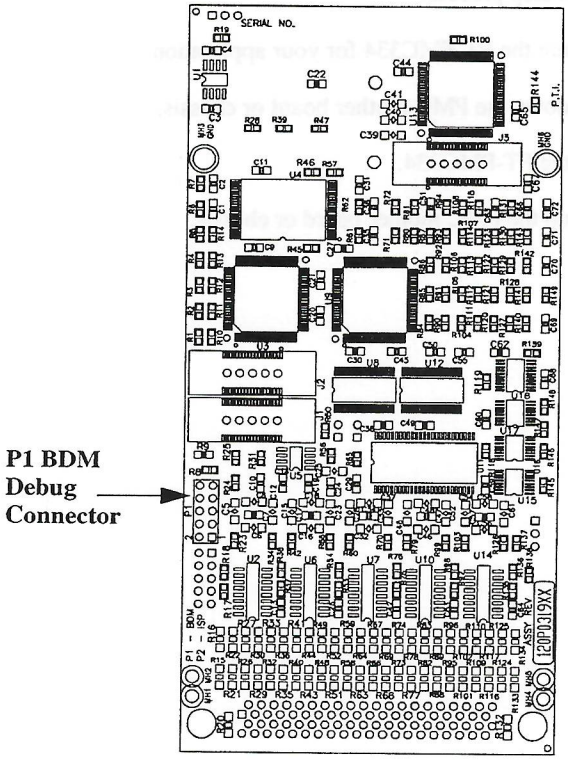


Figure 2: PT-PMC334 RS232 & RS442 Layout & Jumpers

BOTTOM SIDE

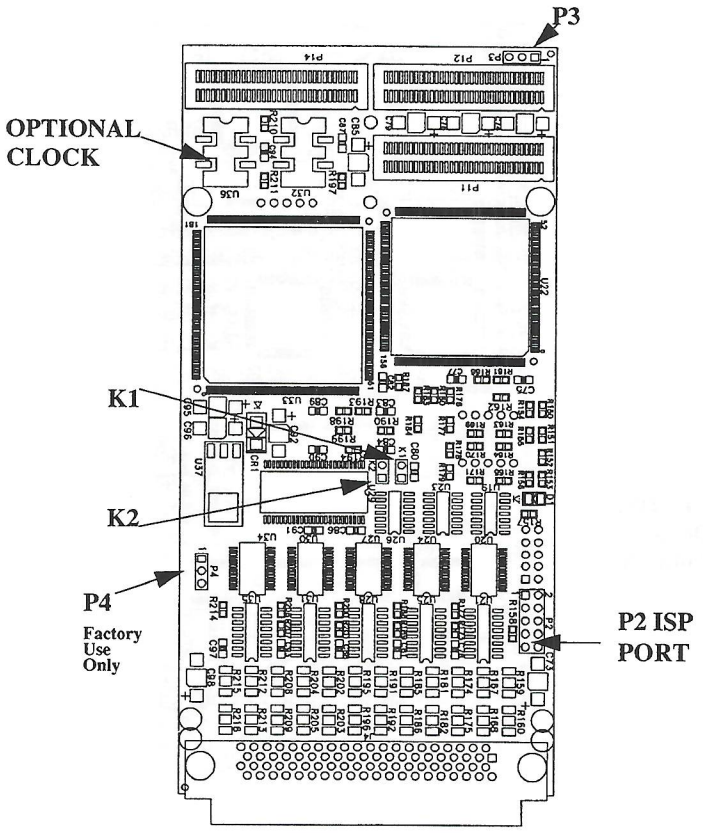


Figure 3: PT-PMC334 V.35 Layout & Jumpers

TOP SIDE

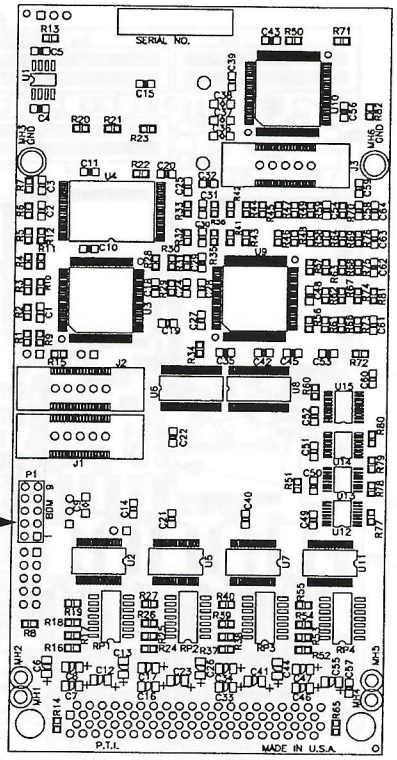
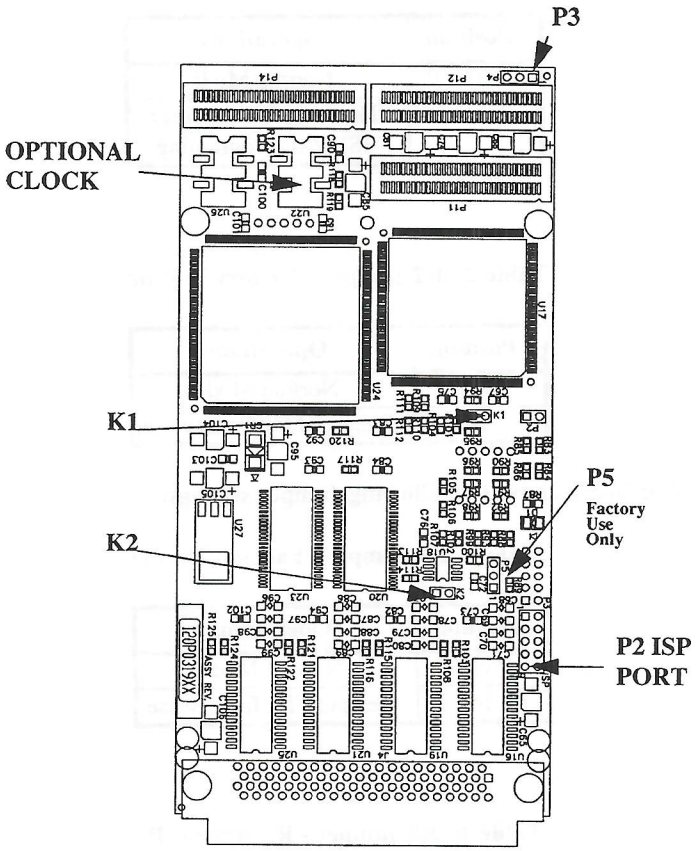


Figure 4: PT-PMC334 V.35 Layout & Jumpers

BOTTOM SIDE



The user may change the position of the jumpers located at the K1 and K2 header blocks. No special tools are required. Adjust the jumper as defined in the following tables. * indicates the factory default settings.

RS232/422 boards have the folllowing Jumper settings:

Table 1: K1 Jumper - Reset for ISP

Position	Operations
*OUT	Normal Mode
IN	Holds card in reset for ISP PAL programing

Table 2: K2 Jumper - Factory Testing

Position	Operations
*OUT	Normal Mode
IN	Reserved for factory use

V.35 boards have the following Jumper settings:

Table 3: K1 Jumper - Factory Testing

Position	Operations
*OUT	Normal Mode
IN	Reserved for factory use

Table 4: K2 Jumper - Reset for ISP

Position	Operations
*OUT	Normal Mode
IN	Holds card in reset for ISP PAL programing

See " Resets" on page 30.

Optional Clock

If your application has a need for a receive clock frequency different than the standard PT-PMC334 serial interface, an optional crystal oscillator can be installed on the PT-PMC334. The location is silkscreened "U32" for the RS323 & RS442, "U26" for V.35 and is located on the component side near the PMC connectors. This location can be populated with a surface mount oscillator of the desired frequency.

Figure 5: RS232 & RS442 Option Clock Position

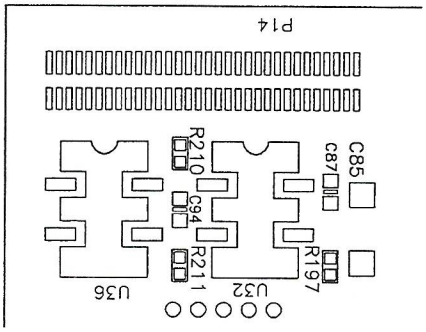
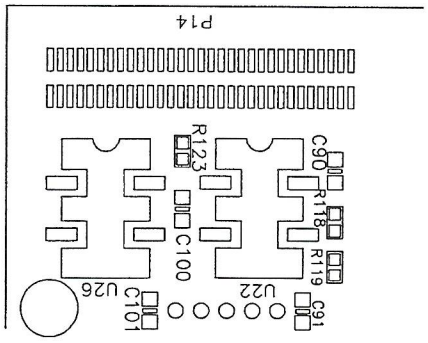


Figure 6: V.35 Option Clock Position



The optional clock[1] is configured for a four pin surface mount oscillator. Pin 1 is a pulled-up output enable, pin 2 is connected to ground, pin 3 is the TTL output of the oscillator, and pin 4 is connected to +5V. Installa-

[1] The optional Oscillator U36 is a suface mount oscillator Epson SG615P series or equivalent..

tion of the oscillator requires soldering the new component in. Do not remove the standard oscillator at location U32 or U26, this is needed for the on-board systems.

A view of the RS232/RS442 and the V.35 board is shown, identifying the position of the Option Clock oscillator on the PT-PMC334. The view is component side up and the CPCI connector towards the bottom. Pin 1 of the location is in the lower left hand corner. When installing the oscillator, check the orientation and component height carefully.

PT-PMC334 Installation

Installing the PT-PMC334 card

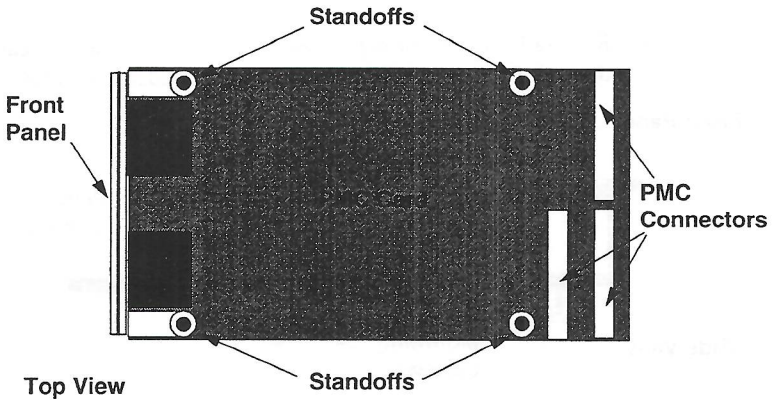


CAUTION: Electronic components on printed circuit boards are extremely sensitive to static electricity. Ordinary amounts of static electricity generated by your clothing or work environment can damage the electronic equipment. It is recommended that when installing the PMC334 in a system that anti-static grounding straps and anti-static mats are used to help prevent damage due to electrostatic discharge.

Step 1 Quit all applications. Power down the PMC mother board or carrier and any attached peripherals.

Step 2 Configure the PT-PMC334. See "Configuring the PT-PMC334" on page 10 for a complete description of setup issues and jumper configuration procedures.

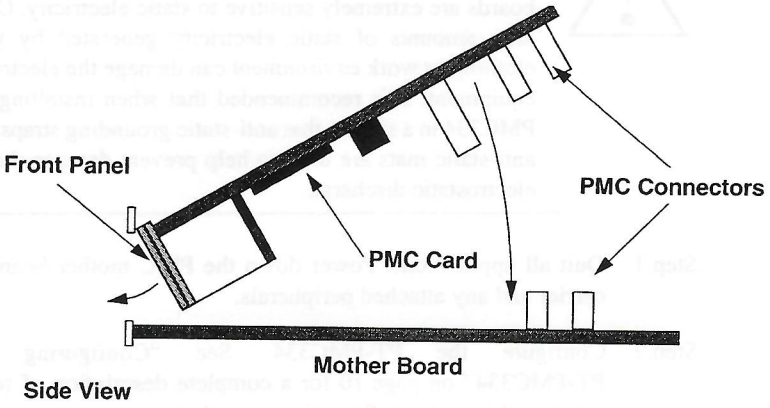
Step 3 Remove the four mounting screws from the standoffs and retain for reuse.



Step 4 Using anti-static procedures (grounding straps and anti-static mats), place the PMC carrier board on a flat surface with the PMC connectors up.

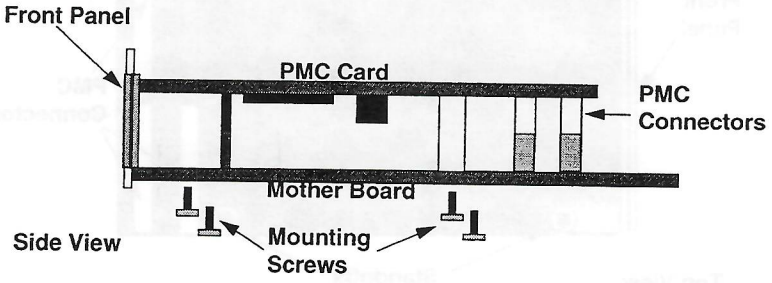
Step 5 Select an available PMC slot.

Step 6 Using proper anti-static grounding procedures insert the face plate end of the PT-PMC334 through the front panel access hole. For front I/O boards be sure that the ESD gasket is in place flush against the front panel. Rear I/O boards make sure that the rubber ESD gasket is in place in the grove of the front panel before installation.



Step 7 Then line up the three PMC connectors and press the PT-PMC334 down into the connectors until they are fully seated.

Step 8 Reinstall the mounting screws that were removed earlier through the Keying Holes and into the threaded standoffs.



Step 9 Install the supplied Adapter cable(s) to the PMC334.

Front Panel Cabling

The PT-PMC334 provides external connectivity through a passive cabling system. A "Hydra style" connector provides front panel serial port connectivity to four DB25 connectors for the RS-232C, RS449 (Male & Female type) and V.35 versions (M34 connectors for V.35) in DTE configuration (pins).

Rear I/O Cabling

The PMC334 can also be purchased in a Rear I/O configuration. For Compact PCI use the CompactPCI CRIS-P family of Rear I/O adapters.

For Compact PCI the Rear I/O versions of the PMC334 cards have been designed to be compliant with PICMG 2.3 P 1.0 for JN4 pinouts. **The actual routing of these signals to the back-plane pins are done by the PMC host that is being used.**

Step 10 Reinstall the PMC mother board or carrier and any attached peripherals.

Step 11 Re-connect any cables from the peripheral devices.

This completes the hardware installation. At this point, turn power back on to the units and proceed to any Software Installation Instructions that may have been provided.

Logic Analyzer Connectors

The PT-PMC334 permits the optional installation of connectors for use by a logic analyzer or other test equipment. The connectors must be installed on the primary side of the board. The pin assignments for these connectors can be found in "APPENDIX F: Background Debug Port Pin Assignments" on page 106.

Section 3

FUNCTIONAL DESCRIPTION

The PT-PMC334 PMC Quad Communications Controller provides four serial channel interfaces for high performance synchronous communications on a PMC host system. The design incorporates a Motorola MC68360 Quad Integrated Communications Controller (QUICC) and a PLX PCI9080 with DMA capability. Code storage and data buffering are provided by a DRAM array which is shared between the QUICC and the PCI9080.

Serial line electrical interfacing is available on-board providing voltage level adaptation to a Recommended Standard, such as RS-232C, RS-449, RS-530, or V.35.

The frontplate interface connection on the PT-PMC334 uses an 80-pin amplimite receptacle containing the signals for all four ports. To provide an industry standard connection for each port, hydra style adapter cables are offered. Adapter cable wiring details for each style cable is also provided.

For Compact PCI use the CompactPCI CRIS-P family of Rear I/O adapters.

For VMEbus or other bus types, the Rear I/O versions of the PMC334 cards have been designed to be compliant with PICMG 2.3 P 1.0 for JN4 pinouts. **The actual routing of these signals to the backplane pins are done by the PMC host that is being used.**

The PT-PMC334 is available with an optional crystal oscillator to provide custom synchronous clock speeds.

The block diagram in Figure 8 on page 22, demonstrates the major components of this design.

PT-PMC334 Block Diagram

Figure 7: Block Diagram of a Front Panel I/O PT-PMC334

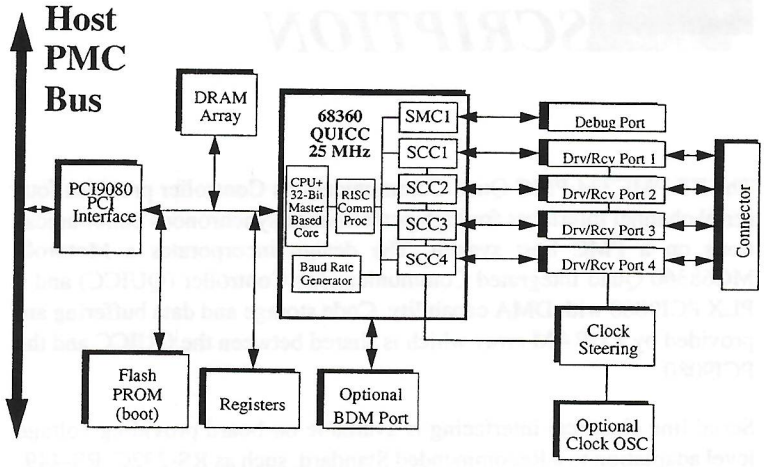
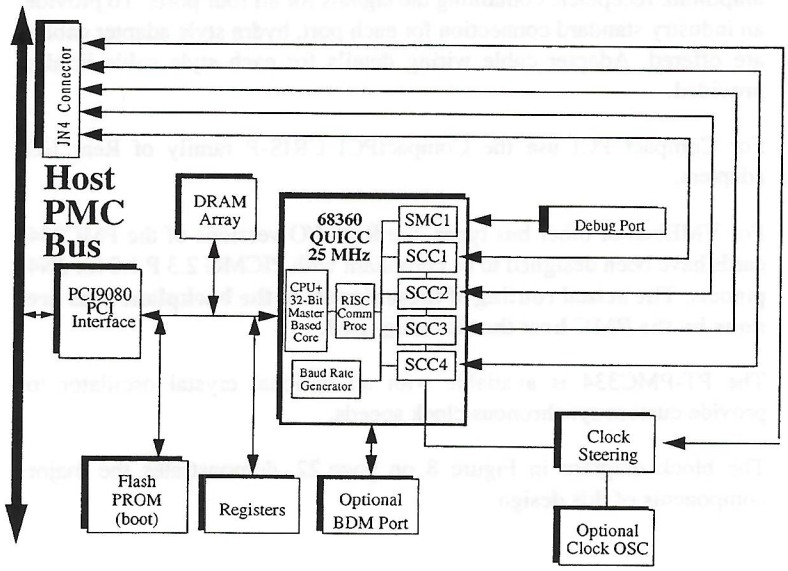


Figure 8: Block Diagram of a Backpanel I/O PT-PMC334



MC68360 Quad Integrated Communications Controller (QUICC)

QUICC Setup



NOTE: Many register addresses presented in this manual are based on PT-PMC334 being initialized per the code fragment provided in "APPENDIX E: PT-PMC334 Initialization" on page 80. I/O port setup is dictated by the PT-PMC334 circuit design. It is **highly** recommended that you use the example code fragment to initialize the PT-PMC334.

The QUICC requires concentrated effort in the set up of its configuration register set. The *MC68360 Quad Integrated Communications Controller, User's Manual* is the best source for information into the details of programming and operation of the QUICC.

The PT-PMC334 internal address space is divided into eight major areas using the General-Purpose Chip-Select feature of the QUICC. The decoding provided by the Chip Select logic is controlled by the Global Memory Register (GMR) and the Memory Controller Status Register (MSTAT). The initialization of these registers is performed by the code in "APPENDIX E: PT-PMC334 Initialization" on page 80. Also see the QUICC User's Manual for more information on the GMR and MSTAT registers.

The address map of each functional element is provided in "Table 5: Device Address Map" on page 25. The QUICC occupies 8 KBytes of address space for internal memory and registers. The base address for these are stored in the Memory Base Address Register (MBAR) which resides at the fixed address of 0003.FF00h. Since the MBAR is programmable, the beginning addresses for the internal Dual-Ported RAM (DPRBASE) and the internal registers (REGB) are relocatable.

This map applies for QUICC and PMC slave accesses. A single PROM device contains the QUICC Boot Firmware as well as the PMC configuration information. The QUICC has access to the entire address range as shown in this table. The PMC Bus has access to the entire range with the exception of the local boot PROM.

PCI slave accesses to the Local bus arbitrate for Local bus with the QUICC chip. When the PCI9080 is master of the Local bus, the address and control signals are enabled and the QUICC's System Integration Module (SIM60) provides address decoding for the various resources. The function code is generated by logic, and is fixed at the value of 05h (Supervisory Data space).

Table 5: Device Address Map

Device	Size[a]	Data Width[b]	QUICC Address	PCI Address[c]	Purpose	Pin
PROM	128 KB	Byte	0000.0000h	NA	Boot Firmware (note: only first 128KB of 1MB is accessable at this address - See CS4)	CS0
QUICC	1 W	Word	0003.FF00h	0003.FF00h	MBAR	
QUICC	4 KB	varies	0004.0000h	0004.0000h	DPRBASE	
QUICC	4 KB	varies	0004.1000h	0004.1000h	REGB	
PCI9080 Registers	200 B	Word	0010.0000h	CFG/Host[d]	PCI9080 Registers	CS7
Status Register	1 B	Word	0010.1000h	0010.1000h	Board Status	CS6
QUICC Interrupt Register	1 b	Word	0010.1100h	0010.1100h	QUICC L7 Interrupt	CS6
PCI Interrupt Register	1 b	Word	0010.1200h	0010.1200h	PCI Interrupt	CS6
Misc Register	1 B	Word	0010.1300h	0010.1300h	Misc PCI9080 Control	CS6
Board Info Register	1 B	Word	0010.1400h	0010.1400h	System Slot Information	CS6
Reserved	1 B	Word	0010.1500h	0010.1500h	Reserved	CS6
Board Config Register	1 B	Word	0010.1600h	0010.1600h	Misc Configuration Info	CS6
PROM WE Register	1 b	Word	0010.1700h	0010.1700h	PROM Write Enable	CS6
TCSL Register	1 B	Word	0011.0200h	0011.0200h	Transmit Clock Select	CS5
RCSL Register	1 B	Word	0011.0300h	0011.0300h	Receive Clock Select	CS5
DRAM	4 MB	variable	0040.0000h	0040.0000h	Code/Data	CS1

Table 5: Device Address Map

Device	Size[a]	Data Width[b]	QUICC Address	PCI Address[c]	Purpose	Pin
DRAM Reserved						CS2
PROM	1 MB	Byte	D000.0000	N/A	Alias to Boot Firmware to access all 1MB	CS4
PCI Direct Master Space	4GB[e]	variable	F000.0000	N/A	Direct Access to PCI Address Space	CS3
Reserved						CS4

a. B = Byte, b = bit.
b. Word = 32 bits.
c. PCI Address indicates offset from PMC Base Address Local Address Space 0 value loaded by the host.
d. PCI Address for PCI9080 Registers (Local Config, Shared Run Time) indicates offset from PMC Base Address for Mapped Runtime Registers value loaded by the host. PCI9080 PMC Config Registers (Table 10 on page 33) are accessed by PMC Configuration (CFG) cycles.
e. The PMC334 does not request anything in this address space during its configuration cycles.

QUICC Register Setup

All internal memory and registers of the QUICC occupy a single 8-KByte memory block that is relocatable along 8-KByte boundaries. The location is fixed by writing the desired base address of the 8-KByte memory block to the Memory Base Address Register (MBAR). The MBAR resides at a fixed location in 0003.FF00. The MBAR is a write only register.

The 8-KByte block is divided into two 4-KByte sections. The dual port RAM occupies the first section; the internal registers occupy the second section. The starting addresses of these two sections are referred to in the

QUICC manual as the Dual-Port RAM Base (DPRBASE) and the Register Base (REGB), respectively.

The MBAR is loaded at initialization time with a value of 0004.0000. This determines the values of DPRBASE and REGB. Note that these are not actually registers but base addresses. "Table 6: QUICC Register Addresses" on page 27 is a list of the critical QUICC registers and settings for proper board operation.

Table 6: QUICC Register Addresses

Register	QUICC Address	Width in bits	Setting
MBAR	0003.FF00h[a]	32	0x00040000
DPRBASE	0004.0000h[b]	32	NA
REGB	0004.1000h[c]	32	NA
MCR	0004.1000h	32	0x0000ec7f
AVR	0004.1008h	8	0xa0
CLKOCR	0004.100Ch	8	0x0c
PLLCR	0004.1010h	16	0x8000
CDVCR	0004.1014h	16	0x0780
PEPAR	0004.1016h	16	0x0460
SYPCR	0004.1022h	8	0x0c
GMR	0004.1040h	32	0x18ac0000
BR0	0004.1050h	32	0x00000001
OR0	0004.1054h	32	0x3ffe0004
BR1	0004.1060h	32	0x00400001
OR1	0004.1064h	32	0x1fc00001
BR2	0004.1070h	32	0x0
OR2	0004.1074h	32	0x0
BR3	0004.1080h	32	0xf0000001
OR3	0004.1084h	32	0xf0000006
BR4	0004.1090h	32	0xd0000001
OR4	0004.1094h	32	0x3ff00004
BR5	0004.10a0h	32	0x00110001
OR5	0004.10a4h	32	0x4ffff800

Table 6: QUICC Register Addresses

Register	QUICC Address	Width in bits	Setting
BR6	0004.10b0h	32	0x00101001
OR6	0004.10b4h	32	0x4ffff800
BR7	0004.10c0h	32	0x00100001
OR7	0004.10c4h	32	0xfffff800

a. MBAR is at a fixed address. The value in MBAR determines the value of DPRBASE and REGB.
b. Base Address of QUICC Dual-Port RAM section.
c. Base Address of QUICC Register section

The base and option register settings correspond to the device address map provided in "Table 5: Device Address Map" on page 25, and the device access timing provided for reference in "Table 7: QUICC Access Timing" on page 28.

The QUICC I/O ports are explained on page 69.

Table 7: QUICC Access Timing

Device Type	Device Speed	Tcyc[a]	Memory Cycle Time[b]	# Wait States
PROM	120 ns.	3	200 ns.	2
DRAM	70 ns.	1	160 ns.	1
Regis-ters	15 ns.	8	400 ns.	7
PCI Master		N.A.		-

a. Tcyc = Value loaded into memory controller's option register for the internally generated DSACKs.
N.A. means Not Applicable because the DSACK signals are generated by logic external to the 68360.
b. 68360 Address Strobe period plus one clock cycle.

QUICC Interrupts

The QUICC receives an interrupt at level 7 from the QUICC Interrupt Register accessible by the PMC Bus at the address defined in Table 6 on page 27. This interrupt is asserted by setting the MSb (D31). The interrupt is removed when this bit is cleared (write D31 = 0). The value of this latch may be read at any time. This interrupt is defined on the QUICC as auto-vectored and its state may be verified by reading the D31 bit. This register contains a Flip-Flop that maintains the state of the interrupt request. This interrupt is also cleared when reset is asserted, removing any pending requests. The QUICC Interrupt Register is described in full on page 64.

A QUICC level 7 interrupt may also be generated from a software watchdog option available on the QUICC. This option is controlled in the QUICC SYPCR.

The QUICC receives an interrupt at level 5 from several sources via the PCI9080. This interrupt can be cleared by disabling the source's enable bit or clearing the cause of the interrupt. See the section on PMC Interrupts on page 65 for more information.

Table 8 defines interrupts to the QUICC and the process by which they are removed.

Table 8: QUICC Interrupt Source Map

Source	Level	Vector[a]	Removal Service
PCI9080 Local Interrupt	5	Auto-vectored	Clear source or remove enable
QUICC Interrupt Register	7	Auto-vectored	Clear MSB in register
Software Watchdog Option[b]	7	Auto-vectored	Acknowledge Cycle

a. Those auto-vectored interrupts must be programmed as such by means of the MC68360 IP's Auto Vector Register.
b. The software watchdog timer (SWT) can be programmed to generate a board Reset or a level 7 interrupt with programmable vector number.

Timers

The QUICC has four general purpose timer modules, a periodic interrupt timer, a software watchdog timer, and a bus cycle period monitor.

The software watchdog timer may be used to interrupt the CPU, or reset the PT-PMC334 logic and CPU. This QUICC reset output does not initialize the PCI9080.

Bus cycles performed by the CPU, are monitored by a timer within the QUICC. This is controlled by the BME bit and the BMT field of the SYPCR (register).

Resets

The Power on Reset control circuity holds the PT-PMC334 in reset until the Vcc has sufficiently stabilized above the 4.75 volt threshold level. Installing the K2 jumper holds this power on Reset circuit in Reset Mode continuously. This mode is used for ISP PAL programming operations.

The PMC Reset signal has the effect of initializing all of the PMC334 logic. This signal is normally asserted during a power up PMC reset by the Host system. The PMC Reset is distributed to the QUICC Soft Reset (RESETS) pin and other onboard logic.

The QUICC may generate a Soft RESET by execution of the RESET instruction, or a watchdog timeout. This initializes the QUICC and its control logic and resets the Local Bus portion of the PCI9080, re-initializing all local configuration registers.

The QUICC can also be reset by asserting the signal on the Hard RESET pin. This pin is attached to the optional background debug mode connector. Asserting this signal initializes the QUICC and its control logic and resets the Local Bus portion of the PCI9080, re-initializing all local configuration registers.

A host may also hold the PMC334 in reset by setting the PMC Adapter Software Reset bit in the PCI9080 EEPROM control, PMC command codes, User I/O control, Init control register. Setting this bit generates a continuous Soft Reset.

Optional BDM Port

The PT-PMC334 permits the addition of a 10 pin header strip in position P4 for the software developer so that a Background Debug Mode (BDM) Connector may be added (Samtec[1], part number TSM-15-01-S-DV). P4 allows a thru-hole header on the component side of the board. P4 is defined in the QUICC manual Section 9.9 (page 9- 94). A momentary reset switch may be attached to the RESETH pin (P4 PIN 7) to provide a convenience during development. The pinout for the BDM Port is shown in Appendix E.

PCI Interface

The PCI9080 requires concentrated effort in the setup of its configuration and runtime registers. The PLX PCI9080 Datasheet[2] contains the PCI9080 data sheet. This is the best source for information into the details of programming and operating the PCI9080.

Endian Conversion

Proper care must be taken when accessing local addresses from the PMC Bus and PCI9080 Registers from the local bus. The hardware does not handle endian conversion from the big endian local bus to the little endian PMC Bus (and interface). Accesses from the PMC Bus less than 32-bits wide must change the lower two address bits for proper data bytes to be read/written as shown in Table 9.

---

1 Samtec can be reached at (800) 726-8329 or (812) 944-6733.

2 This can be found at www.plxtech.com/toolbox/9080.htm.

The QUICC has the capability to transmit and receive SCC data using little endian byte ordering instead of the standard big endian byte ordering. This is set up in the QUICC's RFCR and TFCR registers.

Table 9: Addressing for Endian Conversion

Data	Local Address Offset	PCI Address Offset
D31-D24 (byte)	00b	11b
D23-D16 (byte)	01b	10b
D15-D8 (byte)	10b	01b
D7-D0 (byte)	11b	00b
D31-D16 (half-word)	00b	10b
D15-D0 (half-word)	10b	00b
D31-D0 (word)	00b	00b

PCI9080 Setup

PCI9080 registers can be accessed by either the QUICC or the PMC Host. The PCI9080 address decode mode signal (ADMODE) and input address select signal (S0) are set to properly decode accesses to internal PCI9080 register. The allocated register space for the PCI9080 registers is shown in "Table 5: Device Address Map" on page 25. When initialization of PCI9080 registers is complete, the user should set the Local Init Status bit in the PCI9080 EEPROM Control, PMC Command Codes, User I/O Control, Init Control Register. Until this bit is set, the PMC334 will issue retrys to all PMC accesses.

Please check the PLX Web site for more information:

www.plxtech.com/toolbox/9080.htm

PCI Registers

The PMC registers must be programmed locally from the PROM device, since the serial EEPROM option of the PCI9080 is not used. Until the Local Init Done bit in the PCI9080 Init Control Register is set, indicating the configuration registers have been loaded, PMC cycles will be termi-

nated with retrys by the PCI9080. Both Configuration Read (type 0 or 1) and Configuration Write (type 0 or 1) PMC cycles are supported.

Doorbell Registers

There are two 32-bit doorbell interrupt/status registers in the PCI9080. One is assigned to the PMC bus interface, while the other is assigned to the Local bus interface. Doorbell registers are used to pass interrupts between the PMC bus and Local bus.

Mailbox Registers

There are eight 32-bit mailbox registers in the PCI9080. These registers are used to pass command and status information between the PMC Host and the QUICC.

Table 10: PCI9080 PMC Configuration Register Addresses

Register	Local Address	Width in bits	Setting
Device ID	0010.0000h	16	0xD334
Vendor ID	0010.0002h	16	0x1214
Status[a]	0010.0004h	16	n/a
Command[a]	0010.0006h	16	n/a
Class Code	0010.0008h	24	0x7800000[b]
Revision ID	0010.000bh	8	0x10
BIST	0010.000ch	8	0x00
Header Type	0010.000dh	8	0x00
Latency Timer	0010.000eh	8	0x42
Cache Line Size	0010.000fh	8	0x00
PCI BA Mem Mapped Reg	0010.0010h	32	Host
PCI BA I/O Mapped Reg	0010.0014h	32	Host
PCI BA Local AddrSpace 0	0010.0018h	32	Host
Subsystem Device ID	0010.002ch	16	0xc334
Subsystem Vendor ID	0010.002eh	16	0x1214
PCI BA Local Exp ROM	0010.0030h	32	Host

Table 10: PCI9080 PMC Configuration Register Addresses

Register	Local Address	Width in bits	Setting
Max_lat	0010.003ch	8	0x00
Min Gnt	0010.003dh	8	0x00
Interrupt Pin	0010.003eh	8	0x01

a. Communication Controller
b. The host system will respond with data here. The values found here will have different values based on the host system and time frame.

Table 11: PCI9080 Local Configuration Register Addresses

Register	Local Address	Width in bits	Setting
PCI-Local Range	0010.0080h	32	0xff800000
PCI-Local Base	0010.0084h	32	0x00000001
PCI-ROM Range	0010.0090h	32	0xffff0000
PCI-ROM Range	0010.0094h	32	0x0
PCI-Local Desc	0010.0098h	32	0x40430043
DM-PCI Range	0010.009ch	32	0x0
DM-PCI Mem BA	0010.00a0h	32	0x0
DM-PCI Cfg LBA	0010.00a4h	32	0x0
DM-PCI PBA	0010.00a8h	32	0x0
DM-PCI Cfg PCA	0010.00ach	32	0x0

Table 12: PCI9080 Shared Run Time Register Addresses

Register	Local Address	Width in bits	Setting
Mailbox Reg 0[a]	0010.00c0h	32	0x0
Mailbox Reg 1	0010.00c4h	32	0x0
Mailbox Reg 2	0010.00c8h	32	0x0
Mailbox Reg 3	0010.00cch	32	0x0

Table 12: PCI9080 Shared Run Time Register Addresses

Register	Local Address	Width in bits	Setting
Mailbox Reg 4	0010.00d0h	32	0x0
Mailbox Reg 5	0010.00d4h	32	0x0
Mailbox Reg 6	0010.00d8h	32	0x0
Mailbox Reg 7	0010.00dch	32	0x0
PCI-Loc Doorbell	0010.00e0h	32	0x0
Loc-PCI Doorbell	0010.00e4h	32	0x0
Interrupt Ctrl/Status	0010.00e8h	32	0x0f010100
Misc Control[b]	0010.00ech	32	0x8801767e

a. Mailbox Register 0 and Mailbox Register 1 are always accessible at PCI Address/Local Address 78h/C0h and 7Ch/C4h respectively. When I_2O is disabled in the PLX9080 (bit 0 of QSR Register (PCI Address/ Local Address E8h/168h) is cleared to zero) Mailbox Registers 0 and 1 are accessible at PCI Address 40h and 44h respectively for compatibility with the PLX PCI9080. This is the factory default mode. When I_2O is enabled, the Inbound and Outbound Queue pointers are accessed at PCI Address 40h and 44h respectively replacing the Mailbox Register 0 and Mailbox Register 1 in the PCI Address space. Also, please note that the power on reset value of the Interrupt Ctrl/Status Register (Local Address 0x001000e8) listed in Table 10 has changed from the PLX PCI9080. The PLX9080 power on reset value is 0x0f010100 where the PCI334 power on reset value was 0x00010100. Contact PLX for further information.

b. Also known as the EEPROM Control, PMC Command Codes, User I/O Control, Init Control Register.

Table 13: PCI9080 Local DMA Register Addresses

Register	Local Address	Width in bits	Setting
DMA Ch 0 Mode	0010.0100h	32	0x00000043
DMA0 PMC Addr	0010.0104h	32	0x0
DMA0 Loc Addr	0010.0108h	32	0x0

Table 13: PCI9080 Local DMA Register Addresses

Register	Local Address	Width in bits	Setting
DMA0 Trans Cnt	0010.010ch	32	0x0
DMA0 Desc Ptr	0010.0110h	32	0x0
DMA Ch 1 Mode	0010.0114h	32	0x00000043
DMA1 PMC Addr	0010.0118h	32	0x0
DMA1 Loc Addr	0010.011ch	32	0x0
DMA1 Trans Cnt	0010.0120h	32	0x0
DMA1 Desc Ptr	0010.0124h	32	0x0
DMA Cmd/Status	0010.0128h	32	0x0
DMA Arb Reg 0[a]	0010.012ch	32	0x0
DMA Arb Reg 1	0010.0130h	32	0x0

a. Same as MARBR register at PCI9080 Local address 88h. See the PLX PCI9080 data sheet.

Modes Of Operation

Direct Master

The PT-PMC334 supports Direct Master access to the PMC bus by the QUICC. As a factory default setting Direct Master mode is enabled in the PCI9080 Command Register. The QUICC can perform only memory cycles. In a Direct Master Write, the QUICC (Master) writes data to the PMC (Slave). Direct Master Read, the QUICC (Master) reads data from the PMC (Slave). For single cycle reads the PCI9080 asserts the same PCI bus byte enables as asserted on the local bus. Multiple cycle reads, PCI9080 reads entire longword (all PCI byte enables are asserted), regardless of local bytes enables.

The direct master interface contains a 128-byte write FIFO and a 64-byte read FIFO. PMC base address registers are provided in the PCI9080 configuration space to set up the adapter's location in PMC memory and I/O space. Byte (8-bit), Half-Word (16-bit), and Word (32-bit) accesses are supported to local DRAM, local registers, and the QUICC internal

registers. The maximum range supported by the PMC334 for Direct Master accesses is 4GBytes. See the PLX PCI9080 Data Sheet for more information.

Direct Slave

The PT-PMC334 supports both memory mapped (Memory Read, Memory Read Multiple, Memory Read Line) and I/O mapped (I/O Read) accesses to the Local bus from the PMC bus. The direct slave interface contains a 16-byte FIFO. PMC base address registers are provided in the PCI9080 configuration space to set up the adapter's location in PMC memory and I/O space. Byte (8-bit), Half-Word (16-bit), and Word (32-bit) accesses are supported.

Setup of the PCI9080 Local Configuration Registers must include enabling the Ready Input and disabling the Bterm input for Memory Space 0. The Burst Enable bit may be set but offers no advantage. All sourced burst accesses from the PCI9080 are broken up into non-burst local accesses by hardware.

DMA Operation

The PCI9080 supports two independent DMA channels capable of transferring data from the Local bus (DRAM) to the PMC bus. Both chaining and non-chaining DMA transfers are supported. DMA channel 0 contains a 64-byte bi-directional FIFO and DMA channel 1 contains a 32-byte bi-directional FIFO. DMAs can generate Memory Read, Memory Write, Memory Read Multiple, and Memory Read Line PMC cycles. Demand mode DMA is not supported.

The DMA registers inside the PCI9080 are accessible only from the Local bus (QUICC). Setup of the PCI9080's Local DMA Registers must include enabling the Ready Input and disabling the Bterm input for both DMA channels. The Burst Enable bit may be set but offers no advantage. All sourced burst accesses from the PCI9080 are broken up into non-burst local accesses by hardware.

PCI User In/Out

The PCI9080 contains two user defined bits. The User Out bit is an output of the PCI9080 which can be read from the Status Register

defined on page 63. The User In bit is an input to the PCI9080 which can be set in the Misc Register as described on page 66. Both User bits are found in the PCI9080 EEPROM Control, PMC Command Codes, User I/O Control, Init Control Register.

Local bus Arbitration Priority

QUICC internal masters and DRAM refresh have highest priority during arbitration requests, followed by PMC accesses via the PCI9080. The QUICC's CPU32 core has the lowest priority. The arbitration between the CPU32, QUICC internal masters (such as IDMA or SDMA), and DRAM refresh is handled internal to the QUICC.

PCI9080 Interrupt Requests

PCI Interrupt Requests

A level A PMC interrupt (INTA#) can be generated from the PCI9080 Local to PMC Doorbell Register, the PMC Interrupt Register, or a PCI9080 master/target abort status condition. The level A PMC Interrupt signal or individual sources of the interrupt can be enabled or disabled through the PCI9080 Interrupt Control/Status Register. This register also provides interrupt status for each source of the interrupt. The PMC Interrupt can be cleared by disabling a source's interrupt enable bit or by clearing the cause of the interrupt.

PCI supports four interrupt levels (A,B,C,D). The level A PMC interrupt is the only PMC interrupt signal supported by the PMC334. The PMC Interrupt Pin Register in the PCI9080 configuration space indicates the PMC interrupt level used and must be programmed to reflect the use of INTA#.

The PMC Interrupt Register is a programmable latch described in the following table. A PMC interrupt can be generated when bit 31 of this location is set. The interrupt is removed when this bit is cleared. The

value of this latch may be read at any time. The PMC Interrupt Register

Table 14: PCI Interrupt Register Programming Details

Interrupted Device	Interrupt Request Level	Register	Address
PCI	A	PCI Interrupt Register	0010.1200h

is described in detail on page 65.

PCI to QUICC Interrupt Requests

The PCI9080 PMC to Local Doorbell Register, a PMC BIST interrupt, or a PCI9080 DMA channel interrupt can generate a QUICC level 5 interrupt. The PCI9080 local interrupt pin (LINTO#) or individual sources of the interrupt can be enabled or disabled through the PCI9080 Interrupt Control/Status Register. This register also provides interrupt status for each source of interrupt. The interrupt can be cleared by disabling a source's interrupt enable bit or by clearing the cause of the interrupt.

DRAM Array

The DRAM array has a 32-bit data width. DRAM control is embedded in the QUICC chip and it provides 1 Wait State (4 clocks @ 25MHz) Read and Write cycle period for MC68360 accesses (for 70-ns DRAM). 60-ns DRAM can run with 0 Wait States. Fast page mode is supported.

Timing

All DRAM control signals and timing are controlled directly from the QUICC. RAS and CAS timing, refresh timing, page mode support, DRAM page size, etc. are set up through the QUICC's GMR, BRx, and ORx. For DRAM timing information see "Table 7: QUICC Access Timing" on page 28.

Fast Page Mode

To turn on fast page mode, set the DWQ bit (bit-7) in the QUICC's GMR register, then set the PGME bit (bit-3) in the QUICC's OR1 (and any other OR used by DRAM). Since it is difficult to predict the performance impact of fast page mode, the user may wish to try the application software with and without fast page mode enabled, and compare the results.

Parity

Parity is not supported on DRAM accesses.

Flash PROM

The Flash PROM device is an 1M x 8-bit (1-Mbyte), AM29F800BB-120 48-pin TSOP device. Updating can be performed by setting the PROM_WE bit in the PROM WE Register as shown on page 68 and performing an erase and reprogramming algorithm per the manufacturer's specifications.

The Flash PROM is not accessible from the PMC Bus. If programming from the host is desired, first transfer the data into local DRAM, then locally program the PROM via the QUICC.

Line Drivers/Receivers

For the Front I/O models there are line drivers and receivers provide electrical adaptation from TTL levels to the appropriate communications interface signal levels. Currently RS-232C, EIA-530 (RS-422), and V.35 interfaces are available. Serial ports 1-4 are connected to QUICC SCC1-4, respectively. The electrical interface supported by a PT-PMC334 can be read from the Board Configuration Register as shown on page 67.

The Rear Panel I/O models of the PT-PMC334 do not provide line level drivers out to the PMC JN4 connector. The signals are routed from the QUICC directly to the PMC JN4 connector for all ports. A separate rear I/O modules with the TTL to line interface conversion logic must

perform this functionality. For CompactPCI applications PTI provides a line of CRIS transition modules that provide the line level drivers.

Frontpanel RS-232C

The PT-PMC334-10962 (RS-232C) will service each port with six RS-232C inputs and four RS-232C outputs. The RS232 driver/receivers will operate up to 120Kbps.

Frontpanel RS-442

The PT-PMC334-10912 (RS-442) will service each port with six RS-422 inputs and four RS-422 outputs. The six inputs for each port are electrically terminated with a resistor SIP of 120-ohms between the designated "A" and "B" circuits of each. The RS-422 drivers/receivers operate up to 10-Mbaud. Cabling is available for RS-449 with both mail and female connectors. PTI does not provide a RS-530 interface cable. The pin outs for RS-530 are provided as a courtesy so that you can create your own cables.

Frontpanel V.35

The PT-PMC334-10963 (V.35) will service each port with seven V.35/ Bell 306 inputs and five V.35/Bell 306 outputs. The V.35 drivers/ receivers operate up to 10-MBaud.

Clock Steering

For synchronous serial applications, transmit and receive data signals may be accompanied by external transmit and/or receive clock signals. To manage the options for each clock line source and destination, a clock multiplexer is provided. The source and direction of the clocks are set up in the TCSL Register and the RCSL Register as shown on page 63.

The transmit clock of any channel may be sourced from the QUICC's transmit clock signals (*TXCx*) or from the serial port's transmit clock in signal (*TXCIx*).

The receive clock of any serial channel can be sourced from the serial port receive clock signals (*RCLKx*) or can be sourced from an optional clock (*OPTCLK*). The user may install a surface mount oscillating module of any desired frequency and tolerance. For diagnostic mode, the receive clock may be sourced from inside the QUICC.

Connector & Cabling

All versions of the PT-PMC334 have a 80-pin amplimite connector providing the signals for all four serial ports. The pinout of the amplimite connector is described in the cabling sections below.

RS-232C Cabling

A shielded, hydra style breakout cable providing four 25-pin, D-shell (DB-25) DTE (pins) connectors is available for the PT-PMC334-10962 (RS-232C) version. The pin assignments for the cabling and connectors are shown in Table 15.

Table 15: RS-232C Connector Pin Assignments

80-Pin Amp. Pin No.	Signal Name	RS-232C Name	RS-232C DB25 Pin No.	Description
1	-RXD1	BB	3	Port 1 Receive Data
2			16	
3	-DTR1	CD	20	Port 1 Data Terminal Ready
4			23	
5	-TXD1	BA	2	Port 1 Transmit Data
6			14	
7	-RTS1	CA	4	Port 1 Request To Send
8			19	
9	TXC1	DA	24	Port 1 Transmit Clock
10			11	

Table 15: RS-232C Connector Pin Assignments

80-Pin Amp. Pin No.	Signal Name	RS-232C Name	RS-232C DB25 Pin No.	Description
11	TXCI1	DB	15	Port 1 Transmit Clock In
12			12	
13	DCD1	CF	8	Port 1 Data Carrier Detect
14			10	
15	DSR1	CC	6	Port 1 Data Set Ready
16			22	
17	CTS1	CB	5	Port 1 Clear To Send
18	GND1	AB	7	Port 1 Signal Ground
19	RXC1	DD	17	Port 1 Receive Clock
20			9	
21	RXD2	BB	3	Port 2 Receive Data
22			16	
23	DTR2	CD	20	Port 2 Data Terminal Ready
24			23	
25	TXD2	BA	2	Port 2 Transmit Data
26			14	
27	RTS2	CA	4	Port 2 Request To Send
28			19	
29	TXC2	DA	24	Port 2 Transmit Clock
30			11	
31	TXCI2	DB	15	Port 2 Transmit Clock In
32			12	
33	DCD2	CF	8	Port 2 Data Carrier Detect
34			10	

Table 15: RS-232C Connector Pin Assignments

80-Pin Amp. Pin No.	Signal Name	RS-232C Name	RS-232C DB25 Pin No.	Description
35	DSR2	CC	6	Port 2 Data Set Ready
36			22	
37	CTS2	CB	5	Port 2 Clear To Send
38	GND2	AB	7	Port 2 Signal Ground
39	RXC2	DD	17	Port 2 Receive Clock
40			9	
41	RXD3	BB	3	Port 3 Receive Data
42			16	
43	DTR3	CD	20	Port 3 Data Terminal Ready
44			23	
45	TXD3	BA	2	Port 3 Transmit Data
46			14	
47	RTS3	CA	4	Port 3 Request To Send
48			19	
49	TXC3	DA	24	Port 3 Transmit Clock
50			11	
51	TXCI3	DB	15	Port 3 Transmit Clock In
52			12	
53	DCD3	CF	8	Port 3 Data Carrier Detect
54			10	
55	DSR3	CC	6	Port 3 Data Set Ready
56			22	
57	CTS3	CB	5	Port 3 Clear To Send
58	GND3	AB	7	Port 3 Signal Ground

Table 15: RS-232C Connector Pin Assignments

80-Pin Amp. Pin No.	Signal Name	RS-232C Name	RS-232C DB25 Pin No.	Description
59	RXC3	DD	17	Port 3 Receive Clock
60			9	
61	RXD4	BB	3	Port 4 Receive Data
62			16	
63	DTR4	CD	20	Port 4 Data Terminal Ready
64			23	
65	TXD4	BA	2	Port 4 Transmit Data
66			14	
67	RTS4	CA	4	Port 4 Request To Send
68			19	
69	TXC4	DA	24	Port 4 Transmit Clock
70			11	
71	TXCI4	DB	15	Port 4 Transmit Clock In
72			12	
73	DCD4	CF	8	Port 4 Data Carrier Detect
74			10	
75	DSR4	CC	6	Port 4 Data Set Ready
76			22	
77	CTS4	CB	5	Port 4 Clear To Send
78	GND4	AB	7	Port 4 Signal Ground
79	RXC4	DD	17	Port 4 Receive Clock
80			9	

RS-232C Backpanel I/O Connections

The following is the pinout for backpanel I/O for the CPC334 RS232 out to the PMC JN4 connector.

Table 16: RS-232C Backpanel Pin Assignments

RS-232C Mnemonic	Signal Name w/ polarity	JN4 Pin (to PMC Host)	Signal Decription
BB	+RXD1	1	Port 1 Receive Data
CD	-DTR1	6	Port 1 Data Terminal Ready
BA	+TXD1	11	Port 1 Transmit
CA	-RTS1	16	Port 1 Request to Send
DA	-TXC1	21	Port 1 Transmit Clock
DB	-TXCI1	26	Port 1 Transmit Clock In
CF	-DCD1	31	Port 1 Data Carrier Detect
CC	-DSR1	36	Port 1 Data Set Ready
CB	-CTS1	41	Port 1 Clear to Send
DD	-RXC1	46	Port 1 Receive Clock
BB	+RXD2	2	Port 2 Receive Data
CD	-DTR2	7	Port 2 Data Terminal Ready
BA	+TXD2	12	Port 2 Transmit
CA	-RTS2	17	Port 2 Request to Send
DA	-TXC2	22	Port 2 Transmit Clock
DB	-TXCI2	27	Port 2 Transmit Clock In
CF	-DCD2	32	Port 2 Data Carrier Detect
CC	-DSR2	37	Port 2 Data Set Ready
CB	-CTS2	42	Port 2 Clear to Send
DD	-RXC2	47	Port 2 Receive Clock
BB	+RXD3	3	Port 3 Receive Data
CD	-DTR3	8	Port 3 Data Terminal Ready
BA	+TXD3	13	Port 3 Transmit
CA	-RTS3	18	Port 3 Request to Send
DA	-TXC3	23	Port 3 Transmit Clock
DB	-TXCI3	28	Port 3 Transmit Clock In
CF	-DCD3	33	Port 3 Data Carrier Detect
CC	-DSR3	38	Port 3 Data Set Ready
CB	-CTS3	43	Port 3 Clear to Send
DD	-RXC3	48	Port 3 Receive Clock
BB	+RXD4	4	Port 4 Receive Data

Table 16: RS-232C Backpanel Pin Assignments

RS-232C Mnemonic	Signal Name w/ polarity	JN4 Pin (to PMC Host)	Signal Decription
CD	-DTR4	9	Port 4 Data Terminal Ready
BA	+TXD4	14	Port 4 Transmit
CA	-RTS4	19	Port 4 Request to Send
DA	-TXC4	24	Port 4 Transmit Clock
DB	-TXCI4	29	Port 4 Transmit Clock In
CF	-DCD4	34	Port 4 Data Carrier Detect
CC	-DSR4	39	Port 4 Data Set Ready
CB	-CTS4	44	Port 4 Clear to Send
DD	-RXC4	49	Port 4 Receive Clock

RS-449 Cabling

A shielded, hydra style breakout cable providing four 25-pin, D-shell (DB-25) DTE (pins) with male or female connectors is available for the PT-PMC334-10912 (RS-442) version. The pin assignments for the cabling and connectors are shown in Table 17.

Table 17: RS-449 Connector Pin Assignments

80-Pin Amp. Pin No.	RS-449 Signal Name	RS-449 DB-37 Pin No.	Description
1	RXD1(A)	6	Port 1 Receive Data
2	RXD1(B)	24	Port 1 Receive Data
3	DTR1(A)	12	Port 1 Data Terminal Ready
4	DTR1(B)	30	Port 1 Data Terminal Ready
5	TXD1(A)	4	Port 1 Transmit Data
6	TXD1(B)	22	Port 1 Transmit Data
7	RTS1(A)	7	Port 1 Request To Send
8	RTS1(B)	25	Port 1 Request To Send
9	TXC1(A)	17	Port 1 Transmit Clock
10	TXC1(B)	35	Port 1 Transmit Clock
11	TXCI1(A)	5	Port 1 Transmit Clock In
12	TXCI1(B)	23	Port 1 Transmit Clock In
13	DCD1(A)	13	Port 1 Data Carrier Detect
14	DCD1(B)	31	Port 1 Data Carrier Detect
15	DSR1(A)	11	Port 1 Data Set Ready

Table 17: RS-449 Connector Pin Assignments

80-Pin Amp. Pin No.	RS-449 Signal Name	RS-449 DB-37 Pin No.	Description
16	DSR1(B)	29	Port 1 Data Set Ready
17	CTS1(A)	9	Port 1 Clear To Send
18	CTS1(B)	27	Port 1 Clear To Send
19	RXC1(A)	8	Port 1 Receive Clock
20	RXC1(B)	26	Port 1 Receive Clock
21	RXD2(A)	6	Port 2 Receive Data
22	RXD2(B)	24	Port 2 Receive Data
23	DTR2(A)	12	Port 2 Data Terminal Ready
24	DTR2(B)	30	Port 2 Data Terminal Ready
25	TXD2(A)	4	Port 2 Transmit Data
26	TXD2(B)	22	Port 2 Transmit Data
27	RTS2(A)	7	Port 2 Request To Send
28	RTS2(B)	25	Port 2 Request To Send
29	TXC2(A)	17	Port 2 Transmit Clock
30	TXC2(B)	35	Port 2 Transmit Clock
31	TXCI2(A)	5	Port 2 Transmit Clock In
32	TXCI2(B)	23	Port 2 Transmit Clock In
33	DCD2(A)	13	Port 2 Data Carrier Detect
34	DCD2(B)	31	Port 2 Data Carrier Detect
35	DSR2(A)	11	Port 2 Data Set Ready
36	DSR2(B)	29	Port 2 Data Set Ready
37	CTS2(A)	9	Port 2 Clear To Send
38	CTS2(B)	27	Port 2 Clear To Send
39	RXC2(A)	8	Port 2 Receive Clock
40	RXC2(B)	26	Port 2 Receive Clock
41	RXD3(A)	6	Port 3 Receive Data
42	RXD3(B)	24	Port 3 Receive Data
43	DTR3(A)	12	Port 3 Data Terminal Ready
44	DTR3(B)	30	Port 3 Data Terminal Ready
45	TXD3(A)	4	Port 3 Transmit Data
46	TXD3(B)	22	Port 3 Transmit Data
47	RTS3(A)	7	Port 3 Request To Send
48	RTS3(B)	25	Port 3 Request To Send
49	TXC3(A)	17	Port 3 Transmit Clock
50	TXC3(B)	35	Port 3 Transmit Clock
51	TXCI3(A)	5	Port 3 Transmit Clock In

Table 17: RS-449 Connector Pin Assignments

80-Pin Amp. Pin No.	RS-449 Signal Name	RS-449 DB-37 Pin No.	Description
52	TXCI3(B)	23	Port 3 Transmit Clock In
53	DCD3(A)	13	Port 3 Data Carrier Detect
54	DCD3(B)	31	Port 3 Data Carrier Detect
55	DSR3(A)	11	Port 3 Data Set Ready
56	DSR3(B)	29	Port 3 Data Set Ready
57	CTS3(A)	9	Port 3 Clear To Send
58	CTS3(B)	27	Port 3 Clear To Send
59	RXC3(A)	8	Port 3 Receive Clock
60	RXC3(B)	26	Port 3 Receive Clock
61	RXD4(A)	6	Port 4 Receive Data
62	RXD4(B)	24	Port 4 Receive Data
63	DTR4(A)	12	Port 4 Data Terminal Ready
64	DTR4(B)	30	Port 4 Data Terminal Ready
65	TXD4(A)	4	Port 4 Transmit Data
66	TXD4(B)	22	Port 4 Transmit Data
67	RTS4(A)	7	Port 4 Request To Send
68	RTS4(B)	25	Port 4 Request To Send
69	TXC4(A)	17	Port 4 Transmit Clock
70	TXC4(B)	35	Port 4 Transmit Clock
71	TXCI4(A)	5	Port 4 Transmit Clock In
72	TXCI4(B)	23	Port 4 Transmit Clock In
73	DCD4(A)	13	Port 4 Data Carrier Detect
74	DCD4(B)	31	Port 4 Data Carrier Detect
75	DSR4(A)	11	Port 4 Data Set Ready
76	DSR4(B)	29	Port 4 Data Set Ready
77	CTS4(A)	9	Port 4 Clear To Send
78	CTS4(B)	27	Port 4 Clear To Send
79	RXC4(A)	8	Port 4 Receive Clock
80	RXC4(B)	26	Port 4 Receive Clock

RS-449 Backpanel I/O Connections

The following is the pinout for backpanel I/O for the CPC334 RS232 out to the PMC JN4 connector.

Table 18: RS-449 Backpanel I/O Connector Pin Assignment

RS-449 Mnemonic	Signal Name w/ polarity	JN4 Pin (to PMC Host)	Signal Decription
RD	+RXD1	1	Port 1 Receive Data
TR	-DTR1	6	Port 1 Data Terminal Ready
SD	+TXD1	11	Port 1 Transmit
RS	-RTS1	16	Port 1 Request to Send
TT	-TXC1	21	Port 1 Transmit Clock
ST	-TXCI1	26	Port 1 Transmit Clock In
RR	-DCD1	31	Port 1 Data Carrier Detect
DM	-DSR1	36	Port 1 Data Set Ready
CS	-CTS1	41	Port 1 Clear to Send
RT	-RXC1	46	Port 1 Receive Clock
RD	+RXD2	2	Port 2 Receive Data
TR	-DTR2	7	Port 2 Data Terminal Ready
SD	+TXD2	12	Port 2 Transmit
RS	-RTS2	17	Port 2 Request to Send
TT	-TXC2	22	Port 2 Transmit Clock
ST	-TXCI2	27	Port 2 Transmit Clock In
RR	-DCD2	32	Port 2 Data Carrier Detect
DM	-DSR2	37	Port 2 Data Set Ready
CS	-CTS2	42	Port 2 Clear to Send
RT	-RXC2	47	Port 2 Receive Clock
RD	+RXD3	3	Port 3 Receive Data
TR	-DTR3	8	Port 3 Data Terminal Ready
SD	+TXD3	13	Port 3 Transmit
RS	-RTS3	18	Port 3 Request to Send
TT	-TXC3	23	Port 3 Transmit Clock
ST	-TXCI3	28	Port 3 Transmit Clock In
RR	-DCD3	33	Port 3 Data Carrier Detect

Table 18: RS-449 Backpanel I/O Connector Pin Assignment

RS-449 Mnemonic	Signal Name w/ polarity	JN4 Pin (to PMC Host)	Signal Decription
DM	-DSR3	38	Port 3 Data Set Ready
CS	-CTS3	43	Port 3 Clear to Send
RT	-RXC3	48	Port 3 Receive Clock
RD	+RXD4	4	Port 4 Receive Data
TR	-DTR4	9	Port 4 Data Terminal Ready
SD	+TXD4	14	Port 4 Transmit
RS	-RTS4	19	Port 4 Request to Send
TT	-TXC4	24	Port 4 Transmit Clock
ST	-TXCI4	29	Port 4 Transmit Clock In
RR	-DCD4	34	Port 4 Data Carrier Detect
DM	-DSR4	39	Port 4 Data Set Ready
CS	-CTS4	44	Port 4 Clear to Send
RT	-RXC4	49	Port 4 Receive Clock

RS-530 Cabling

PTI does not provide a RS-530 cable. The following table is provided so that you can create your own cable if needed. The pin assignments for the cabling and connectors are shown in Table 19.

Table 19: RS-530 Connector Pin Assignments

80-Pin Amp. Pin No.	Signal Name	EIA-530 Name	EIA-530 DB-25 Pin No.	Description
1	RXD1-	BB(A)	3	Port 1 Receive Data
2	RXD1+	BB(B)	16	Port 1 Receive Data
3	DTR1-	CD(A)	20	Port 1 Data Terminal Ready
4	DTR1+	CD(B)	23	Port 1 Data Terminal Ready
5	TXD1-	BA(A)	2	Port 1 Transmit Data
6	TXD1+	BA(B)	14	Port 1 Transmit Data
7	RTS1-	CA(A)	4	Port 1 Request To Send
8	RTS1+	CA(B)	19	Port 1 Request To Send
9	TXC1-	DA(A)	24	Port 1 Transmit Clock
10	TXC1+	DA(B)	11	Port 1 Transmit Clock
11	TXCI1-	DB(A)	15	Port 1 Transmit Clock In
12	TXCI1+	DB(B)	12	Port 1 Transmit Clock In
13	DCD1-	CF(A)	8	Port 1 Data Carrier Detect
14	DCD1+	CF(B)	10	Port 1 Data Carrier Detect
15	DSR1-	CC(A)	6	Port 1 Data Set Ready
16	DSR1+	CC(B)	22	Port 1 Data Set Ready

Table 19: RS-530 Connector Pin Assignments

80-Pin Amp. Pin No.	Signal Name	EIA-530 Name	EIA-530 DB-25 Pin No.	Description
17	CTS1-	CB(A)	5	Port 1 Clear To Send
18	CTS1+	CB(B)	13	Port 1 Clear To Send
19	RXC1-	DD(A)	17	Port 1 Receive Clock
20	RXC1+	DD(B)	9	Port 1 Receive Clock
21	RXD2-	BB(A)	3	Port 2 Receive Data
22	RXD2+	BB(B)	16	Port 2 Receive Data
23	DTR2-	CD(A)	20	Port 2 Data Terminal Ready
24	DTR2+	CD(B)	23	Port 2 Data Terminal Ready
25	TXD2-	BA(A)	2	Port 2 Transmit Data
26	TXD2+	BA(B)	14	Port 2 Transmit Data
27	RTS2-	CA(A)	4	Port 2 Request To Send
28	RTS2+	CA(B)	19	Port 2 Request To Send
29	TXC2-	DA(A)	24	Port 2 Transmit Clock
30	TXC2+	DA(B)	11	Port 2 Transmit Clock
31	TXCI2-	DB(A)	15	Port 2 Transmit Clock In
32	TXCI2+	DB(B)	12	Port 2 Transmit Clock In
33	DCD2-	CF(A)	8	Port 2 Data Carrier Detect
34	DCD2+	CF(B)	10	Port 2 Data Carrier Detect
35	DSR2-	CC(A)	6	Port 2 Data Set Ready

Table 19: RS-530 Connector Pin Assignments

80-Pin Amp. Pin No.	Signal Name	EIA-530 Name	EIA-530 DB-25 Pin No.	Description
36	DSR2+	CC(B)	22	Port 2 Data Set Ready
37	CTS2-	CB(A)	5	Port 2 Clear To Send
38	CTS2+	CB(B)	13	Port 2 Clear To Send
39	RXC2-	DD(A)	17	Port 2 Receive Clock
40	RXC2+	DD(B)	9	Port 2 Receive Clock
41	RXD3-	BB(A)	3	Port 3 Receive Data
42	RXD3+	BB(B)	16	Port 3 Receive Data
43	DTR3-	CD(A)	20	Port 3 Data Terminal Ready
44	DTR3+	CD(B)	23	Port 3 Data Terminal Ready
45	TXD3-	BA(A)	2	Port 3 Transmit Data
46	TXD3+	BA(B)	14	Port 3 Transmit Data
47	RTS3-	CA(A)	4	Port 3 Request To Send
48	RTS3+	CA(B)	19	Port 3 Request To Send
49	TXC3-	DA(A)	24	Port 3 Transmit Clock
50	TXC3+	DA(B)	11	Port 3 Transmit Clock
51	TXCI3-	DB(A)	15	Port 3 Transmit Clock In
52	TXCI3+	DB(B)	12	Port 3 Transmit Clock In
53	DCD3-	CF(A)	8	Port 3 Data Carrier Detect
54	DCD3+	CF(B)	10	Port 3 Data Carrier Detect

Table 19: RS-530 Connector Pin Assignments

80-Pin Amp. Pin No.	Signal Name	EIA-530 Name	EIA-530 DB-25 Pin No.	Description
55	DSR3-	CC(A)	6	Port 3 Data Set Ready
56	DSR3+	CC(B)	22	Port 3 Data Set Ready
57	CTS3-	CB(A)	5	Port 3 Clear To Send
58	CTS3+	CB(B)	13	Port 3 Clear To Send
59	RXC3-	DD(A)	17	Port 3 Receive Clock
60	RXC3+	DD(B)	9	Port 3 Receive Clock
61	RXD4-	BB(A)	3	Port 4 Receive Data
62	RXD4+	BB(B)	16	Port 4 Receive Data
63	DTR4-	CD(A)	20	Port 4 Data Terminal Ready
64	DTR4+	CD(B)	23	Port 4 Data Terminal Ready
65	TXD4-	BA(A)	2	Port 4 Transmit Data
66	TXD4+	BA(B)	14	Port 4 Transmit Data
67	RTS4-	CA(A)	4	Port 4 Request To Send
68	RTS4+	CA(B)	19	Port 4 Request To Send
69	TXC4-	DA(A)	24	Port 4 Transmit Clock
70	TXC4+	DA(B)	11	Port 4 Transmit Clock
71	TXCI4-	DB(A)	15	Port 4 Transmit Clock In
72	TXCI4+	DB(B)	12	Port 4 Transmit Clock In
73	DCD4-	CF(A)	8	Port 4 Data Carrier Detect

Table 19: RS-530 Connector Pin Assignments

80-Pin Amp. Pin No.	Signal Name	EIA-530 Name	EIA-530 DB-25 Pin No.	Description
74	DCD4+	CF(B)	10	Port 4 Data Carrier Detect
75	DSR4-	CC(A)	6	Port 4 Data Set Ready
76	DSR4+	CC(B)	22	Port 4 Data Set Ready
77	CTS4-	CB(A)	5	Port 4 Clear To Send
78	CTS4+	CB(B)	13	Port 4 Clear To Send
79	RXC4-	DD(A)	17	Port 4 Receive Clock
80	RXC4+	DD(B)	9	Port 4 Receive Clock

Note: See the RS449 chart for information on how the Backpanel connections are made for RS-350

V.35 Cabling

A shielded, hydra style breakout cable providing four M-34, DTE (pins) connectors is available for the PT-PMC334-10963 (V.35) version. The pin assignments for the cabling and connector are shown in Table 20.

Table 20: V.35 Connector Pin Assignments

80-Pin Amp. Pin No.	Signal Name	V.35 Name	M-34 Pin No.	Description
1	RXD1-	104	R	Port 1 Receive Data
2	RXD1+	104	T	Port 1 Receive Data
3	DTR1	108	H	Port 1 Data Terminal Ready
4				
5	TXD1-	103	P	Port 1 Transmit Data

Table 20: V.35 Connector Pin Assignments

80-Pin Amp. Pin No.	Signal Name	V.35 Name	M-34 Pin No.	Description
6	TXD1+	103	S	Port 1 Transmit Data
7	RTS1-	105	C	Port 1 Request To Send
8	GND1	102	B	Port 1 Signal Ground
9	TXC1-	113	U	Port 1 Transmit Clock
10	TXC1+	113	W	Port 1 Transmit Clock
11	TXCI1-	114	Y	Port 1 Transmit Clock In
12	TXCI1+	114	AA	Port 1 Transmit Clock In
13	DCD1	109	F	Port 1 Data Carrier Detect
14	RI1	125	J	Port 1 Ring Indicator
15	DSR1	107	E	Port 1 Data Set Ready
16	LT1		K	Port 1 Line Test
17	CTS1	106	D	Port 1 Clear To Send
18				
19	RXC1-	115	V	Port 1 Receive Clock
20	RXC1+	115	X	Port 1 Receive Clock
21	RXD2-	104	R	Port 2 Receive Data
22	RXD2+	104	T	Port 2 Receive Data
23	DTR2	108	H	Port 2 Data Terminal Ready
24				
25	TXD2-	103	P	Port 2 Transmit Data
26	TXD2+	103	S	Port 2 Transmit Data
27	RTS2-	105	C	Port 2 Request To Send
28	GND2	102	B	Port 2 Signal Ground
29	TXC2-	113	U	Port 2 Transmit Clock
30	TXC2+	113	W	Port 2 Transmit Clock
31	TXCI2-	114	Y	Port 2 Transmit Clock In
32	TXCI2+	114	AA	Port 2 Transmit Clock In
33	DCD2	109	F	Port 2 Data Carrier Detect
34	RI2	125	J	Port 2 Ring Indicator
35	DSR2	107	E	Port 2 Data Set Ready
36	LT2		K	Port 2 Line Test
37	CTS2	106	D	Port 2 Clear To Send
38				
39	RXC2-	115	V	Port 2 Receive Clock
40	RXC2+	115	X	Port 2 Receive Clock
41	RXD3-	104	R	Port 3 Receive Data

Table 20: V.35 Connector Pin Assignments

80-Pin Amp. Pin No.	Signal Name	V.35 Name	M-34 Pin No.	Description
42	RXD3+	104	T	Port 3 Receive Data
43	DTR3	108	H	Port 3 Data Terminal Ready
44				
45	TXD3-	103	P	Port 3 Transmit Data
46	TXD3+	103	S	Port 3 Transmit Data
47	RTS3-	105	C	Port 3 Request To Send
48	GND3	102	B	Port 3 Signal Ground
49	TXC3-	113	U	Port 3 Transmit Clock
50	TXC3+	113	W	Port 3 Transmit Clock
51	TXCI3-	114	Y	Port 3 Transmit Clock In
52	TXCI3+	114	AA	Port 3 Transmit Clock In
53	DCD3	109	F	Port 3 Data Carrier Detect
54	RI3	125	J	Port 3 Ring Indicator
55	DSR3	107	E	Port 3 Data Set Ready
56	LT3		K	Port 3 Line Test
57	CTS3	106	D	Port 3 Clear To Send
58				
59	RXC3-	115	V	Port 3 Receive Clock
60	RXC3+	115	X	Port 3 Receive Clock
61	RXD4-	104	R	Port 4 Receive Data
62	RXD4+	104	T	Port 4 Receive Data
63	DTR4	108	H	Port 4 Data Terminal Ready
64				
65	TXD4-	103	P	Port 4 Transmit Data
66	TXD4+	103	S	Port 4 Transmit Data
67	RTS4-	105	C	Port 4 Request To Send
68	GND4	102	B	Port 4 Signal Ground
69	TXC4-	113	U	Port 4 Transmit Clock
70	TXC4+	113	W	Port 4 Transmit Clock
71	TXCI4-	114	Y	Port 4 Transmit Clock In
72	TXCI4+	114	AA	Port 4 Transmit Clock In
73	DCD4	109	F	Port 4 Data Carrier Detect
74	RI4	125	J	Port 4 Ring Indicator
75	DSR4	107	E	Port 4 Data Set Ready
76	LT4		K	Port 4 Line Test

Table 20: V.35 Connector Pin Assignments

80-Pin Amp. Pin No.	Signal Name	V.35 Name	M-34 Pin No.	Description
77	CTS4	106	D	Port 4 Clear To Send
78				
79	RXC4-	115	V	Port 4 Receive Clock
80	RXC4+	115	X	Port 4 Receive Clock

V.35 Cabling Backpanel I/O Connections

The following is the pinout for backpanel I/O for the CPC334 V.35 out to the PMC JN4 connector.

Table 21: V.35 Backpanel I/O Connector Pin Assignments

V.35 Mnemonic	Signal Name w/ polarity	JN4 Pin (to PMC Host)	Signal Decription
RD	+RXD1	1	Port 1 Receive Data
DTR	-DTR1	6	Port 1 Data Terminal Ready
SD	+TXD1	11	Port 1 Transmit
RTS	-RTS1	16	Port 1 Request to Send
SCTE	-TXC1	21	Port 1 Transmit Clock
SCT	-TXCI1	26	Port 1 Transmit Clock In
RLSD	-DCD1	31	Port 1 Data Carrier Detect
DSR	-DSR1	36	Port 1 Data Set Ready
CTS	-CTS1	41	Port 1 Clear to Send
SCR	-RXC1	46	Port 1 Receive Clock
RD	+RXD2	2	Port 2 Receive Data
DTR	-DTR2	7	Port 2 Data Terminal Ready
SD	+TXD2	12	Port 2 Transmit
RTS	-RTS2	17	Port 2 Request to Send
SCTE	-TXC2	22	Port 2 Transmit Clock
SCT	-TXCI2	27	Port 2 Transmit Clock In
RLSD	-DCD2	32	Port 2 Data Carrier Detect
DSR	-DSR2	37	Port 2 Data Set Ready

Table 21: V.35 Backpanel I/O Connector Pin Assignments

V.35 Mnemonic	Signal Name w/ polarity	JN4 Pin (to PMC Host)	Signal Decription
CTS	-CTS2	42	Port 2 Clear to Send
SCR	-RXC2	47	Port 2 Receive Clock
RD	+RXD3	3	Port 3 Receive Data
DTR	-DTR3	8	Port 3 Data Terminal Ready
SD	+TXD3	13	Port 3 Transmit
RTS	-RTS3	18	Port 3 Request to Send
SCTE	-TXC3	23	Port 3 Transmit Clock
SCT	-TXCI3	28	Port 3 Transmit Clock In
RLSD	-DCD3	33	Port 3 Data Carrier Detect
DSR	-DSR3	38	Port 3 Data Set Ready
CTS	-CTS3	43	Port 3 Clear to Send
SCR	-RXC3	48	Port 3 Receive Clock
RD	+RXD4	4	Port 4 Receive Data
DTR	-DTR4	9	Port 4 Data Terminal Ready
SD	+TXD4	14	Port 4 Transmit
RTS	-RTS4	19	Port 4 Request to Send
SCTE	-TXC4	24	Port 4 Transmit Clock
SCT	-TXCI4	29	Port 4 Transmit Clock In
RLSD	-DCD4	34	Port 4 Data Carrier Detect
DSR	-DSR4	39	Port 4 Data Set Ready
CTS	-CTS4	44	Port 4 Clear to Send
SCR	-RXC4	49	Port 4 Receive Clock

Debug Port (P3 on RS232/422 and P4 on V.35 card)

A 3-pin header is provided for the debug port which is connected to the QUICC's SMC1 port. The TTL signals of SMC1 are converted to RS-232C voltage levels on-board. This connector is 3-pins 0.025" in diameter, spaced 0.100" apart. Table 22 indicates the wiring for a console cable to a DB-25 connector for the debug port. A console cable is

provided with the *PT-Bug PROM and Console Cable* accessory (PT-ACC334-10771).

Table 22: P3 Debug Port Pin Assignments

Signal Name	Header Pin No.	DB-25 Pin No.
TXD	1	2
RXD	2	3
GROUND	3	7

During SMC1 initialization, a break sequence can be enabled to generate an interrupt. If the debug port is left unconnected to a terminal, the QUICC's SMC1 port will receive all 0s, thus generating break sequences. Therefore, do not enable the break sequence interrupt to prevent unwanted interrupts.

Registers



NOTE: Unused bits in local registers should be written to 0. Unused bits have undefined values during local register reads.

TCSL Register

The TCSL (transmit clock select) Register provides the PT-PMC334 with control of the source of the transmit clocks for each serial port. The TCSL Register is a 32-bit register located at local address 0011.0200h. The TCSL Register is readable and writable. The TCSL Register is described in Table 23.

Table 23: TCSL Register

Bit	Mnemonic	Function	Reset Value
31	TCSL1	Transmit Clock Select 1	0
30	TCSL2	Transmit Clock Select 2	0

Table 23: TCSL Register

Bit	Mnemonic	Function	Reset Value
29	TCSL3	Transmit Clock Select 3	0
28	TCSL4	Transmit Clock Select 4	0
27-0	-	Unused	-

Transmit Clock Select

The Transmit Clock Select (TCSLx) bit controls the source of the port's transmit clock. When set, the transmit clock is sourced from the serial interface or from the Transmit Clock In Pin on the clock connector (J4 for front I/O and P14 for rear I/O) for Port X. When the bit is cleared, the transmit clock is sourced from the QUICC's transmit clock output.

RCSL Register

The RCSL (receive clock select) Register provides the PT-PMC334 with control of the source of the receive clocks for each serial port. The RCSL Register is a 32-bit register located at address 0011.0300h. The RCSL Register is readable and writable. The RCSL Register is described in Table 24.

Table 24: RCSL Register

Bit	Mnemonic	Function	Reset Value
31	RCSL1	Receive Clock Select 1	0
30	RCSL2	Receive Clock Select 2	0
29	RCSL3	Receive Clock Select 3	0
28	RCSL4	Receive Clock Select 4	0
27-0	-	Unused	-

Receive Clock Select

The Receive Clock Select bit controls the source of the port's receive clock. When set, the receive clock is sourced from the optional oscillator. When the bit is cleared, the receive clock is sourced from the serial interface.

Status Register

The Status Register provides status of on-board signals for monitoring The Status Register is a read only, 32-bit register located at local address 0010.1000h. The Status Register is described in Table 25.

Table 25: Status Register

Bit	Mnemonic	Function	Reset Value
31	-	Reserved	0
30	-	Reserved	0

Table 25: Status Register

Bit	Mnemonic	Function	Reset Value
29	-	Reserved	0
28	-	Reserved	0
27	-	Reserved	1
26	USERO	PCI User Out	1
25	MODE	Mode	MODE
24	-	Reserved	0
23-0	-	Unused	-

PCI User Out

The PMC User Out bit indicates the status of the PCI9080 User Out pin. This is a general purpose output of the PCI9080 that is controlled from the PCI9080 EEPROM Control, PMC Command Codes, User I/O Control, Init Control Register (PCI9080 configuration space, PMC6Ch, LOC ECh).

Mode

The Mode bit indicates the status of jumper K1. When the jumper is installed, the Mode bit will be clear (0), enabling a mode reserved for the factory if the PT-Bug PROM is installed. When the jumper in not installed, the Mode bit will be set (1), indicating normal operation under PT-Bug.

QUICC Interrupt Register

The QUICC Interrupt Register controls the QUICC interrupts. The QUICC Interrupt Register is a 32-bit register located at local address

0010.1100h. The QUICC Interrupt register is readable and writable. The QUICC Interrupt Register is described in Table 26.

Table 26: QUICC Interrupt Register

Bit	Mnemonic	Function	Reset Value
31	IR7	QUICC Interrupt Level 7	0
30-24	-	Reserved	0
23-0	-	Unused	-

Interrupt 7

The Interrupt 7 bit (IR7) causes a QUICC level 7 interrupt when set high. Clearing the bit removes the interrupt.

PMC Interrupt Register

The PMC Interrupt Register controls the PMC interrupts. The PMC Interrupt Register is a 32-bit register located at local address 0010.1200h. The PMC Interrupt register is readable and writable. The PMC Interrupt Register is described in Table 27.

Table 27: PCI Interrupt Register

Bit	Mnemonic	Function	Reset Value
31	PINT	PCI Interrupt	0
30-24	-	Reserved	0
23-0	-	Unused	-

PMC Interrupt

The PMC Interrupt (PINT) bit causes a PMC Interrupt when set. Clearing this bit removes the interrupt. The PMC Interrupt is mapped to PMC INTA#, INTB#, INTC#, or INTD# through the PCI9080 PMC Interrupt Pin Register (PCI9080 configuration space, offset 3Dh). Hardware requires this register must map the PMC Interrupt to INTA#.

Misc Register

The Misc Register controls the miscellaneous functions of the PT-PMC334. The Misc register is a 32-bit register located at local address 0010.1300h. The Misc Register is both readable and writable. The Misc Register is described in Table 28.

Table 28: Misc Register

Bit	Mnemonic	Function	Reset Value
31	-	Unused	-
30	-	Unused	-
29	USERI	PCI User In	0
28	-	Reserved	0
27	LED_DIS	LED Disable (Green LED)	1
26-24	-	Reserved	0
23-0	-	Unused	-

PCI User In

The PMC User In (USERI) bit indicates the status of the PCI9080 User In pin. This is a general purpose input of the PCI9080 that is controlled from the PCI9080 EEPROM Control, PCI Command Codes, User I/O Control, Init Control Register (PCI9080 configuration space, PCI6Ch, LOC ECh).

LED Disable

The LED Disable (LED_DIS) bit is connected to the on-board Green LED. When set (1), the LED will be disabled (off). When the bit is 0, the LED is on. This LED is factory configured to indicate when the PTBug program is running on the PMC334.

Board Configuration Register

The Board Configuration Register is a read only register that includes information on the configuration of the PT-PMC334. The Board Configuration register is a 32-bit register located at local address 0010.1600h. The Board Configuration is described in Table 29.

Table 29: Board Configuration Register

Bit	Mnemonic	Function	Reset Value
31	-	Reserved	0
30	-	Reserved	0
29	INT2	Electrical Interface 2	INT2
28	INT1	Electrical Interface 1	INT1
27	INT0	Electrical Interface 0	INT0
26	ID2	Revision ID 2	ID2
25	ID1	Revision ID 1	ID1
24	ID0	Revision ID 0	ID0
23-0	-	Unused	-

Electrical Interface

The Electrical Interface (INT[2:0]) bits indicate the electrical interface supported by the card. Available supported interfaces are listed in Table 30.

Table 30: Electrical Interface ID

Int[2:0]	Interface
000	RS-232C
001	RS-422 (RS-530 or RS-449)
010	V.35

Table 30: Electrical Interface ID

Int[2:0]	Interface
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	None Installed

Revision ID

The Revision ID (ID[2:0]) bits indicate the revision of the PT-PMC334. A revision ID of 000 is the lowest ID.

PROM Write Enable Register

The PROM Write Enable Register contains the protection bit for enabling/disabling writing to the PROM. The PROM Write Enable Register is a 32-bit register located at local address 0010.1700h. The PROM Write Enable Register is readable and writable. The PROM Write Enable Register is described in Table 31.

Table 31: PROM Write Enable Register

Bit	Mnemonic	Function	Reset Value
31	PWE	PROM Write Enable	0
30-24	-	Reserved	0
23-0	-	Unused	-

PROM Write Enable

The PROM Write Enable (PWE) bit, when set, enables programming of the PROM. When cleared (0), the PROM is a read only device.

QUICC I/O Ports

The QUICC has three general purpose I/O ports A, B and C. Each pin in I/O ports may be configured as a general-purpose I/O pin or as a dedicated peripheral interface pin. The PT-PMC334 design uses these ports as described below.

QUICC Port A

Assignment of Port A pins including their direction is accomplished by configuring the PAPAR, PADIR, and PAODR registers on the QUICC. An example configuration for Port A is shown in the Table 32.

Table 32: Port A Configuration Settings

QUICC Register	QUICC Address	Value
PAPAR	0004.1552h	0xffff
PADIR	0004.1550h	0x5500
PAODR	0004.1554h	0x0000
PADAT	0004.1556h	Value

The PT-PMC334 uses Port A on the QUICC for serial port transmit and receive clocks and data. Bit assignments are shown in Table 33. Transmit Clocks (TXCx) may be configured as either inputs or outputs. The definition is dependent upon the clock steering settings for transmit clocks. The Direction column in Table 33 indicates the direction of the signal with respect to the QUICC.

Table 33: QUICC Port A Mapping

Port A (16-bit)				
QUICC pin/cell	Use	Signal Name	QUICC Name	Direct.
PA00	Receive Data Port 1	RXD1	RXD1	I
PA01	Transmit Data Port 1	TXD1	TXD1	O
PA02	Receive Data Port 2	RXD2	RXD2	I
PA03	Transmit Data Port 2	TXD2	TXD2	O

Table 33: QUICC Port A Mapping

Port A (16-bit)				
QUICC pin/cell	Use	Signal Name	QUICC Name	Direct.
PA04	Receive Data Port 3	RXD3	RXD3	I
PA05	Transmit Data Port 3	TXD3	TXD3	O
PA06	Receive Data Port 4	RXD4	RXD4	I
PA07	Transmit Data Port 4	TXD4	TXD4	O
PA08	Transmit Clock Port 1	TXC1	CLK1/BRG01	I/O
PA09	Receive Clock Port 1	RXC1	CLK2	I
PA10	Transmit Clock Port 2	TXC2	CLK3/BRG02	I/O
PA11	Receive Clock Port 2	RXC2	CLK4	I
PA12	Transmit Clock Port 3	TXC3	CLK5/BRG03	I/O
PA13	Receive Clock Port 3	RXC3	CLK6	I
PA14	Transmit Clock Port 4	TXC4	CLK7/BRG04	I/O
PA15	Receive Clock Port 4	RXC4	CLK8	I

QUICC Port B

Assignment of Port B pins including their direction is accomplished by configuring the PBPAR, PBDIR, and PBODR registers on the QUICC. An example configuration for Port B is shown in Table 34.

Table 34: Port B Configuration Settings

QUICC Register	QUICC Address	Value
PBPAR	0004.16bch	0x0000
PBDIR	0004.16b8h	0xf00f
PBODR	0004.16c2h	0x0000
PBDAT	0004.16c4h	Value

The PT-PMC334 uses Port B on the QUICC for modem control signals and the debug port transmit and receive signals. Bit assignments are shown in Table 35. RTS signals may be configured as a dedicated signal used by the QUICC's SCC or as a general purpose output pin. The Direc-

tion column in Table 35 indicates the direction of the signal with respect to the QUICC.

Table 35: QUICC Port B Mapping

Port B (18-bit)				
QUICC pin/cell	**Use**	**Signal Name**	**QUICC Name**	**Direct.**
PB00	Line Test Port 1 (V.35 only)	LT1	PORT B0	O
PB01	Line Test Port 2 (V.35 only)	LT2	PORT B1	O
PB02	Line Test Port 3 (V.35 only)	LT3	PORT B2	O
PB03	Line Test Port 4 (V.35 only)	LT4	PORT B3	O
PB04	Data Set Ready Port 1	DSR1	PORT B4	I
PB05	Data Set Ready Port 2	DSR2	PORT B5	I
PB06	Debug Port Transmit Data	TXD	SMTXD1	I
PB07	Debug Port Receive Data	RXD	SMRXD1	O
PB08	Data Set Ready Port 3	DSR3	PORT B8	I
PB09	Data Set Ready Port 4	DSR4	PORT B9	I
PB10	Ring Indicator Port 1 (V.35 only)	RI1	PORT B10	I
PB11	Ring Indicator Port 2 (V.35 only)	RI2	PORT B11	I
PB12	Request To Send Port 1	RTS1	PORT B12/$\overline{\text{RTS1}}$	O
PB13	Request To Send Port 2	RTS2	PORT B13/$\overline{\text{RTS2}}$	O
PB14	Request To Send Port 3	RTS3	PORT B14/$\overline{\text{RTS3}}$	O

Table 35: QUICC Port B Mapping

Port B (18-bit)				
QUICC pin/cell	**Use**	**Signal Name**	**QUICC Name**	**Direct.**
PB15	Request To Send Port 4	RTS4	PORT B15/$\overline{\text{RTS4}}$	O
PB16	Ring Indicator Port 3 (V.35 only)	RI3	PORT B16	I
PB17	Ring Indicator Port 4 (V.35 only)	RI4	PORT B17	I

QUICC Port C

Assignment of Port C pins including their direction is accomplished by configuring the PCPAR, PCDIR, PCSO, and PMCNT registers on the QUICC. An example configuration for Port C is shown in Table 36. Each of the Port C pins may be programmed individually to cause an interrupt to the QUICC CPU32 core as described in the MC68360 User's Manual.

Table 36: Port C Configuration Settings

QUICC Register	QUICC Address	Value
PCPAR	0004.1562h	0x0000
PCDIR	0004.1560h	0x000f
PCSO	0004.1564h	0x0000
PCDAT	0004.1566h	Value
PCINT	0004.1568h	0x0000

The PT-PMC334 uses Port C on the QUICC for modem control signals. The assignment of Port C pins is illustrated in Table 37. CTS and DCD signals may be configured as dedicated signals used by the QUICC's

SCC or as general purpose output pins. The Direction column in Table 37 indicates the direction of the signal with respect to the QUICC.

Table 37: QUICC Port C Pin Mapping

Port C (12-bit)				
QUICC pin/cell	**Use**	**Signal Name**	**QUICC Name**	**Dir.**
PC00	Data Terminal Ready Port 1	DTR 1	PORT C0	O
PC01	Data Terminal Ready Port 2	DTR 2	PORT C1	O
PC02	Data Terminal Ready Port 3	DTR 3	PORT C2	O
PC03	Data Terminal Ready Port 4	DTR 4	PORT C3	O
PC04	Clear To Send Port 1	CTS 1	PORT C4/ $\overline{\text{CTS1}}$	I
PC05	Data Carrier Detect Port 1	DCD 1	PORT C5/$\overline{\text{CD1}}$	I
PC06	Clear To Send Port 2	CTS 2	PORT C6/ $\overline{\text{CTS2}}$	I
PC07	Data Carrier Detect Port 2	DCD 2	PORT C7/$\overline{\text{CD2}}$	I
PC08	Clear To Send Port 3	CTS 3	PORT C8/ $\overline{\text{CTS3}}$	I
PC09	Data Carrier Detect Port 3	DCD 3	PORT C9/$\overline{\text{CD3}}$	I
PC10	Clear To Send Port 4	CTS 4	PORT C10/ $\overline{\text{CTS4}}$	I
PC11	Data Carrier Detect Port 4	DCD 4	PORT C11/ $\overline{\text{CD4}}$	I

Power Budget

Typical and maximum power consumption of the PT-PMC334 is described in Table 38.

Table 38: PT-PMC334 Power Consumption

Board Type	Voltage	Typical	Maximum
PT-PMC334-10962 (RS-232C)	+5V	0.83A	1.25A
PT-PMC334-10962 (RS-232C)	+12V	13mA	20mA
PT-PMC334-10962 (RS-232C)	-12V	8mA	12mA
PT-PMC334-10912 (RS-442)	+5V	1.1A	1.75A
PT-PMC334-10912 (RS-442)	+12V	9.5mA	14mA
PT-PMC334-10912 (RS-442)	-12V	4.2mA	6mA
PT-PMC334-10963 (V.35)	+5V	1.1A	1.75A
PT-PMC334-10963 (V.35)	+12V	9.5mA	14mA
PT-PMC334-10963 (V.35)	-12V	4.5mA	6.5mA

Section 4

APPENDICES

APPENDIX A: Product Warranty

Performance Technologies Inc. (hereinafter "PTI") warrants that its products sold hereunder will at the time of shipment be free from defects in material and workmanship and will conform to PTI's applicable specifications or, if appropriate, to Buyer's specifications accepted by PTI in writing. If products sold hereunder are not as warranted, PTI shall, at its option, refund the purchase price, repair, or replace the product provided proof of purchase and written notice of nonconformance are received by PTI within 12 months of shipment, or in the case of software and integrated circuits within ninety (90) days of shipment and provided said nonconforming products are returned F.O.B. to PTI's facility no later than thirty days after the warranty period expires. Products returned under warranty claims must be accompanied by an approved Return Material Authorization number issued by PTI and a statement of the reason for the return. Please contact PTI, or its agent, with the product serial number to obtain an RMA number. If PTI determines that the products are not defective, Buyer shall pay PTI all costs of handling and transportation. This warranty shall not apply to any products PTI determines to have been subject to testing for other than specified electrical characteristics or to operating and/or environmental conditions in excess of the maximum values established in applicable specifications, or have been subject to mishandling, misuse, static discharge, neglect, improper testing, repair, alteration, parts removal, damage, assembly or processing that alters the physical or electrical properties. This warranty excludes all cost of shipping, customs clearance and related charges outside the United States. Products containing batteries are warranted as above excluding batteries.

THIS WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES WHETHER EXPRESS, IMPLIED OR STATUTORY INCLUDING IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS. IN NO EVENT SHALL PTI BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES DUE TO BREACH OF THIS WARRANTY OR ANY OTHER OBLIGATION UNDER THIS ORDER OR CONTRACT.

APPENDIX B: Product Return Procedure

If you find that your Performance Technologies, Incorporated (PTI) product must be returned for repair, please use a copy of the following form and include it with the returned product:

1

To obtain an RMA number, please contact the PTI's Customer Service Group at (716) 256-0248, FAX: (716) 256-0791). Outside of North America, customers should contact their PTI agent.

PTI will request the serial number of the unit and the reason for the return at the time the RMA is issued. RMA# = _____

2

What address do you want us to return the product to? If you do not give us an address it will be shipped back to the Ship To Address as listed on the invoice. Model Number: _____

3

Please enter in the information that the PTI Technical Support representative has given you for the reason for return of this product.

Description of problem: _____

_____

_____

_____

4

Return products should be shipped in the original packaging if possible. Ship via a traceable carrier and properly insure the package. No C.O.D.s are accepted and any shipping charges are non-refundable. Send your returns to:

Performance Technologies, Inc.
Attn: RMA# (Your RMA# goes here)
315 Science Parkway
Rochester, N.Y. 14620, U.S.A.

(Customers outside of North America, should follow the return shipment instructions issued by your PTI agent.) The RMA number should be clearly marked on the outside of the shipping box to expedite correct handling at the PTI factory.

Repairs will be performed only on complete units. Return of incomplete equipment may delay the repair.

Please note that removal of original parts or product modification by a customer can void the warranty. (This does not apply to jumpers or socketed user programmable parts.)

"Out of warranty repairs" cannot proceed without a Purchase Order to cover estimated cost of the repair.

PTI will supply repair information on all returns and warrants all repairs for 90 days after product is returned to the user.

APPENDIX C: Product Support



NOTE: If You Encounter Difficulty In Using This Performance Technologies, Inc. Product, You Can Contact Our Support Personnel In One Of Three Ways.

A) Preferred - If you have Internet services, email us at support@pt.com. Outline your problem in detail. Please include your return email address, and a telephone number.

B) FAX - If you have FAX service, contact us at U.S. Area Code 716, FAX Number 256-0791. Mark you FAX to Attention: Product Support. Outline your problem in detail. Please include your return FAX number and a telephone number.

C) Contact us via telephone at U.S. Area Code 716-256-0248. Request Product Support. Our offices are open between 8:00 am and 5:00 pm Eastern Time, Monday through Friday.

If you are located outside North America, we encourage you to contact the local PTI distributor or agent for support. Many of our distributors or agents maintain technical support staffs.

APPENDIX D: Installation Notes



CAUTION: ELECTRONIC COMPONENTS ON PRINTED CIRCUIT BOARDS ARE EXTREMELY SENSITIVE TO STATIC ELECTRICITY. ORDINARY AMOUNTS OF STATIC ELECTRICITY GENERATED BY YOUR CLOTHING OR WORK ENVIRONMENT CAN DAMAGE THE ELECTRONIC EQUIPMENT. IT IS RECOMMENDED THAT WHEN INSTALLING THE PT-PMC334 IN A SYSTEM OR THE COMPONENTS ON THE BOARD ITSELF THAT ANTI-STATIC GROUNDING STRAPS AND ANTI-STATIC MATS ARE USED TO HELP PREVENT DAMAGE DUE TO ELECTROSTATIC DISCHARGE.

APPENDIX E: PT-PMC334 Initialization

Following is an example of PT-PMC334 initialization written in CPU32 assembly language.



NOTE: Many of the initialization parameters contained in these files cannot be changed due to the hardware configuration of the PT-PMC334.

quicc.i

Assembly language include file for the QUICC.

```
*******************************************************
*       Header File for the QUICC ( MC68360 )         *
*       UART Example User's Manual Page 7-170         *
*******************************************************


****************** DUAL PORT RAM ***********************
MBAR   =        $03FF00    | Module Base Address, (MBAR)=REGB
*MBAR  =        $03FF04    | Module Base Address, in SLAVE mode
MBARE  =        $03FF08    | Module Base Address Enable SLAVE

DPRBASE =       $00040000     | Base address of dual-port RAM
RXBD   =        DPRBASE+$0000 | Receive Buffer Descriptor address
TXBD   =        DPRBASE+$0010 | Transmit Buffer Descriptor address
RXBD2  =        DPRBASE+$0020 | Receive Buffer Descriptor address
TXBD2  =        DPRBASE+$0030 | Transmit Buffer Descriptor address
RXBD3  =        DPRBASE+$0040 | Receive Buffer Descriptor address
TXBD3  =        DPRBASE+$0050  | Transmit Buffer Descriptor address
RXBD4  =        DPRBASE+$0060 | Receive Buffer Descriptor address
TXBD4  =        DPRBASE+$0070 | Transmit Buffer Descriptor address
REGB   =        DPRBASE+$1000| Base address of Internal Registers
SCC1PB =        DPRBASE+$0C00 | SCC1 Protocol Base address
SCC2PB =        DPRBASE+$0D00| SCC2 Protocol Base address
SCC3PB =        DPRBASE+$0E00 | SCC3 Protocol Base address
SCC4PB =        DPRBASE+$0F00 | SCC4 Protocol Base address
SPIPB  =        DPRBASE+$0D80 | SPI Protocol Base
SMC1PB =        DPRBASE+$0E80 | SMC1 Protocol Base
```

```
SMC2PB =        DPRBASE+$0F80 | SMC2 Protocol Base
IDMA1PB =       DPRBASE+$0E70 | IDMA1 Protocol Base
IDMA2PB =       DPRBASE+$0F70 | IDMA2 Protocol Base

********** SIM Module registers **********
MCR   =         REGB+$0000    | Module Configuration
AVR   =         REGB+$0008    | Auto Vector
RSR   =         REGB+$0009    | Reset Status
CLKOCR =        REGB+$000C    | CLKO Control
PLLCR  =        REGB+$0010    | PPL Control
CDVCR  =        REGB+$0014    | Clock Divider Control
*
PEPAR  =        REGB+$0016    | Port E Pin Assignment
*
SYPCR  =        REGB+$0022    | System Protection Control
SWIV   =        REGB+$0023    | S/w Interrupt Vector
PICR   =        REGB+$0026    | Periodic Interrupt Control
PITR   =        REGB+$002A    | Periodic Interrupt Timing
SWSR   =        REGB+$002F    | S/w Service
BKAR   =        REGB+$0032    | Breakpoint Address
BKCR   =        REGB+$0034    | Breakpoint Control
*
GMR    =        REGB+$0040    | Global Memory
MSTAT  =        REGB+$0044    | MEMC Status
*
BR0    =        REGB+$0050    | Base Register 0
OR0    =        REGB+$0054    | Option Register 0
BR1    =        REGB+$0060    | Base Register 1
OR1    =        REGB+$0064    | Option Register 1
BR2    =        REGB+$0070    | Base Register 2
OR2    =        REGB+$0074    | Option Register 2
BR3    =        REGB+$0080    | Base Register 3
OR3    =        REGB+$0084    | Option Register 3
BR4    =        REGB+$0090    | Base Register 4
OR4    =        REGB+$0094    | Option Register 4
BR5    =        REGB+$00A0    | Base Register 5
OR5    =        REGB+$00A4    | Option Register 5
BR6    =        REGB+$00B0    | Base Register 6
OR6    =        REGB+$00B4    | Option Register 6
BR7    =        REGB+$00C0    | Base Register 7
OR7    =        REGB+$00C4    | Option Register 7

********** CPM Module registers **********
ICCR   =        REGB+$0500    | Channel Configuration
*** IDMA1, 2
CMR1   =        REGB+$0504    | IDMA1 Mode
```

```
SAPR1  =          REGB+$0508   | IDMA1 Source Address Pointer
DAPR1  =          REGB+$050C   | IDMA1 destination Address Pointer
BCR1   =          REGB+$0510   | IDMA1 Byte Count
FCR1   =          REGB+$0514   | IDMA1 Fuction Code
CMAR1  =          REGB+$0516   | IDMA1 Channel Mask
CSR1   =          REGB+$0518   | IDMA1 Channel Status
*
CMR2   =          REGB+$0526   | IDMA2 Mode
SAPR2  =          REGB+$0528   | IDMA2 Source Address Pointer
DAPR2  =          REGB+$052C   | IDMA2 destination Address Pointer
BCR2   =          REGB+$0530   | IDMA2 Byte Count
FCR2   =          REGB+$0534   | IDMA2 Fuction Code
CMAR2  =          REGB+$0536   | IDMA2 Channel Mask
CSR2   =          REGB+$0538   | IDMA2 Channel Status
*** SDMA
SDSR   =          REGB+$051C   | SDMA Status
SDCR   =          REGB+$051E   | SDMA Configuration Register
SDAR   =          REGB+$0520   | SDMA Address Register
*** CP Interrupt
CICR   =          REGB+$0540   | CP Interrupt Configuration
CIPR   =          REGB+$0544   | CP Interrupt Pending
CIMR   =          REGB+$0548   | CP Interrupt Mask
CISR   =          REGB+$054C   | CP Interrupt In-service
*** Port A, B, C
PADIR  =          REGB+$0550   | Port A Data Direction Assignment
PAPAR  =          REGB+$0552   | Port A Pin Function Assignment
PAODR  =          REGB+$0554   | Port A Open Drain Assignment
PADAT  =          REGB+$0556   | Port A Data Content
*
PBDIR  =          REGB+$06B8   | Port B Data Direction Assignment
PBPAR  =          REGB+$06BC   | Port B Pin Function Assignment
PBODR  =          REGB+$06C0   | Port B Open Drain Assignment
PBDAT  =          REGB+$06C4   | Port B Data Content
*
PCDIR  =          REGB+$0560   | Port C Data Direction Assignment
PCPAR  =          REGB+$0562   | Port C Pin Assignment
PCSO   =          REGB+$0564   | Port C Special Options
PCDAT  =          REGB+$0566   | Port C Data Content
PCINT  =          REGB+$0568   | Port C Interrupt Control
*** Timer 1, 2, 3, 4
TGCR   =          REGB+$0580   | Timer Global Configuration
*
TMR1   =          REGB+$0590   | Timer1 Mode
TMR2   =          REGB+$0592   | Timer2 Mode
TRR1   =          REGB+$0594   | Timer1 Reference
TRR2   =          REGB+$0596   | Timer2 Reference
```

```
TCR1  =          REGB+$0598   | Timer1 Capture
TCR2  =          REGB+$059A   | Timer2 Capture
TCN1  =          REGB+$059C   | Timer1 Counter
TCN2  =          REGB+$059E   | Timer2 Counter
*
TMR3  =          REGB+$05A0   | Timer3 Mode
TMR4  =          REGB+$05A2   | Timer4 Mode
TRR3  =          REGB+$05A4   | Timer3 Reference
TRR4  =          REGB+$05A6   | Timer4 Reference
TCR3  =          REGB+$05A8   | Timer3 Capture
TCR4  =          REGB+$05AA   | Timer4 Capture
TCN3  =          REGB+$05AC   | Timer3 Counter
TCN4  =          REGB+$05AE   | Timer4 Counter
*
TER1  =          REGB+$05B0   | Timer1 Event
TER2  =          REGB+$05B2   | Timer2 Event
TER3  =          REGB+$05B4   | Timer3 Event
TER4  =          REGB+$05B6   | Timer4 Event
*** CP
CR    =          REGB+$05C0   | CP Command
RCCR  =          REGB+$05C4   | RISC Configuration
RTER  =          REGB+$05D6   | RISC Timer Event Register
RTMR  =          REGB+$05DA   | RISC Timer Mask Register
* BRG 1, 2, 3, 4
BRGC1 =          REGB+$05F0   | BRG1 Configuration
BRGC2 =          REGB+$05F4   | BRG2 Configuration
BRGC3 =          REGB+$05F8   | BRG3 Configuration
BRGC4 =          REGB+$05FC   | BRG4 Configuration
*** SCC 1, 2, 3, 4
* SCC1
GSMR_L1 =        REGB+$0600   | SCC1 General Mode
GSMR_H1 =        REGB+$0604   | SCC1 General Mode
PSMR1 =          REGB+$0608   | SCC1 Protocol Specific Mode
TODR1 =          REGB+$060C   | SCC1 Transmit On Demand
DSR1  =          REGB+$060E   | SCC1 Data Sync
SCCE1 =          REGB+$0610   | SCC1 Event
SCCM1 =          REGB+$0614   | SCC1 Mask
SCCS1 =          REGB+$0617   | SCC1 Status
* SCC2
GSMR_L2 =        REGB+$0620   | SCC2 General Mode
GSMR_H2 =        REGB+$0624   | SCC2 General Mode
PSMR2 =          REGB+$0628   | SCC2 Protocol Specific Mode
TODR2 =          REGB+$062C   | SCC2 Transmit On Demand
DSR2  =          REGB+$062E   | SCC2 Data Sync
SCCE2 =          REGB+$0630   | SCC2 Event
SCCM2 =          REGB+$0634   | SCC2 Mask
```

```
SCCS2  =          REGB+$0637    | SCC2 Status
* SCC3
GSMR_L3 =         REGB+$0640    | SCC3 General Mode
GSMR_H3 =         REGB+$0644    | SCC3 General Mode
PSMR3  =          REGB+$0648    | SCC3 Protocol Specific Mode
TODR3  =          REGB+$064C    | SCC3 Transmit On Demand
DSR3   =          REGB+$064E    | SCC3 Data Sync
SCCE3  =          REGB+$0650    | SCC3 Event
SCCM3  =          REGB+$0654    | SCC3 Mask
SCCS3  =          REGB+$0657    | SCC3 Status
* SCC4
GSMR_L4 =         REGB+$0660    | SCC4 General Mode
GSMR_H4 =         REGB+$0664    | SCC4 General Mode
PSMR4  =          REGB+$0668    | SCC4 Protocol Specific Mode
TODR4  =          REGB+$066C    | SCC4 Transmit On Demand
DSR4   =          REGB+$066E    | SCC4 Data Sync
SCCE4  =          REGB+$0670    | SCC4 Event
SCCM4  =          REGB+$0674    | SCC4 Mask
SCCS4  =          REGB+$0677    | SCC4 Status
*** SMC 1, 2
SMCMR1 =          REGB+$0682    | SMC1 Mode
SMCE1  =          REGB+$0686    | SMC1 Event
SMCM1  =          REGB+$068A    | SMC1 Mask
*
SMCMR2 =          REGB+$0692    | SMC2 Mode
SMCE2  =          REGB+$0696    | SMC2 Event
SMCM2  =          REGB+$069A    | SMC2 Mask
*** SPI
SPMODE =          REGB+$06A0    | SPI Mode
SPIE   =          REGB+$06A6    | SPI Event
SPIM   =          REGB+$06AA    | SPI Mask
SPCOM  =          REGB+$06AD    | SPI Command
*** PIP
PIPC   =          REGB+$06B2    | PIP Configuration
PTRR   =          REGB+$06B6    | PIP Timing Parameter
*** Serial Interface
SIMODE =          REGB+$06E0    | SI Mode
SIGMR  =          REGB+$06E4    | SI Global Mode
SISTR  =          REGB+$06E6    | SI Status
SICMR  =          REGB+$06E7    | SI Command
SICR   =          REGB+$06EC    | SI Clock Routing
SIRP   =          REGB+$06F0    | SI RAM Pointer
SIRAM  =          REGB+$0700    | SI Routing RAM

********** END of SIM/CPM Register MAP
**********
```

```
****************** SCC Parameters ************************
****** SCC1
RBASE1 =          SCC1PB+$000   | SCC1 RX BD Base Address
TBASE1 =          SCC1PB+$002   | SCC1 TX BD Base Address
RFCR1  =          SCC1PB+$004   | SCC1 RX Function Code
TFCR1  =          SCC1PB+$005   | SCC1 TX Function Code
MRBLR1 =          SCC1PB+$006   | SCC1 MAX Buffer Length - RX
RSTATE1 =         SCC1PB+$008   | SCC1 RX Internal State
RBPRT1 =          SCC1PB+$010   | SCC1 RX BD Pointer
TSTATE1 =         SCC1PB+$018   | SCC1 TX Internal State
TBPRT1 =          SCC1PB+$020   | SCC1 TX BD Pointer
RCRC1  =          SCC1PB+$028   | SCC1 Temp Receive CRC
TCRC1  =          SCC1PB+$02C   | SCC1 Temp Transmit CRC
****** SCC2
RBASE2 =          SCC2PB+$000   | SCC2 RX BD Base Address
TBASE2 =          SCC2PB+$002   | SCC2 TX BD Base Address
RFCR2  =          SCC2PB+$004   | SCC2 RX Function Code
TFCR2  =          SCC2PB+$005   | SCC2 TX Function Code
MRBLR2 =          SCC2PB+$006   | SCC2 MAX Buffer Length - RX
RSTATE2 =         SCC2PB+$008   | SCC2 RX Internal State
RBPRT2 =          SCC2PB+$010   | SCC2 RX BD Pointer
TSTATE2 =         SCC2PB+$018   | SCC2 TX Internal State
TBPRT2 =          SCC2PB+$020   | SCC2 TX BD Pointer
RCRC2  =          SCC2PB+$028   | SCC2 Temp Receive CRC
TCRC2  =          SCC2PB+$02C   | SCC2 Temp Transmit CRC
****** SCC3
RBASE3 =          SCC3PB+$000   | SCC3 RX BD Base Address
TBASE3 =          SCC3PB+$002   | SCC3 TX BD Base Address
RFCR3  =          SCC3PB+$004   | SCC3 RX Function Code
TFCR3  =          SCC3PB+$005   | SCC3 TX Function Code
MRBLR3 =          SCC3PB+$006   | SCC3 MAX Buffer Length - RX
RSTATE3 =         SCC3PB+$008   | SCC3 RX Internal State
RBPRT3 =          SCC3PB+$010   | SCC3 RX BD Pointer
TSTATE3 =         SCC3PB+$018   | SCC3 TX Internal State
TBPRT3 =          SCC3PB+$020   | SCC3 TX BD Pointer
RCRC3  =          SCC3PB+$028   | SCC3 Temp Receive CRC
TCRC3  =          SCC3PB+$02C   | SCC3 Temp Transmit CRC
****** SCC4
RBASE4 =          SCC4PB+$000   | SCC4 RX BD Base Address
TBASE4 =          SCC4PB+$002   | SCC4 TX BD Base Address
RFCR4  =          SCC4PB+$004   | SCC4 RX Function Code
TFCR4  =          SCC4PB+$005   | SCC4 TX Function Code
MRBLR4 =          SCC4PB+$006   | SCC4 MAX Buffer Length - RX
RSTATE4 =         SCC4PB+$008   | SCC4 RX Internal State
RBPRT4 =          SCC4PB+$010   | SCC4 RX BD Pointer
```

```
TSTATE4 =          SCC4PB+$018   | SCC4 TX Internal State
TBPRT4  =          SCC4PB+$020   | SCC4 TX BD Pointer
RCRC4   =          SCC4PB+$028   | SCC4 Temp Receive CRC
TCRC4   =          SCC4PB+$02C   | SCC4 Temp Transmit CRC
CRC_C4  =          SCC4PB+$030   |SCC4CRCConstantTotal-Transparent
CRC_P4  =          SCC4PB+$034   | SCC4 CRC Preset Total-Transparent
****** SMC1 => SMCA, simplify assembly coding
RBASEA  =          SMC1PB+$000   | SMC1 RX BD Base Address
TBASEA  =          SMC1PB+$002   | SMC1 TX BD Base Address
RFCRA   =          SMC1PB+$004   | SMC1 RX Function Code
TFCRA   =          SMC1PB+$005   | SMC1 TX Function Code
MRBLRA  =          SMC1PB+$006   | SMC1 MAX Buffer Length - RX
RSTATEA =          SMC1PB+$008   | SMC1 RX Internal State
RBPRTA  =          SMC1PB+$010   | SMC1 RX BD Pointer
TSTATEA =          SMC1PB+$018   | SMC1 TX Internal State
TBPRTA  =          SMC1PB+$020   | SMC1 TX BD Pointer
****** SMC1 => SMCB
RBASEB  =          SMC2PB+$000   | SMC2 RX BD Base Address
TBASEB  =          SMC2PB+$002   | SMC2 TX BD Base Address
RFCRB   =          SMC2PB+$004   | SMC2 RX Function Code
TFCRB   =          SMC2PB+$005   | SMC2 TX Function Code
MRBLRB  =          SMC2PB+$006   | SMC2 MAX Buffer Length - RX
RSTATEB =          SMC2PB+$008   | SMC2 RX Internal State
RBPRTB  =          SMC2PB+$010   | SMC2 RX BD Pointer
TSTATEB =          SMC2PB+$018   | SMC2 TX Internal State
TBPRTB  =          SMC2PB+$020   | SMC2 TX BD Pointer


****************** Specific Parameters **********************

* SCC1, UART Specific Parameters
MAXIDL1 =          SCC1PB+$38    | SCC1 MAX IDLe cchars
IDLC1   =          SCC1PB+$3A    | SCC1 temp IDLe Counter
BRKCR1  =          SCC1PB+$3C    | SCC1 BReaK Count Register (TX)
PAREC1  =          SCC1PB+$3E    | SCC1 Parity Error Counter (RX)
FRMER1  =          SCC1PB+$40    | SCC1 Framing Error Counter (RX)
NOSEC1  =          SCC1PB+$42    | SCC1 Noise Counter (RX)
BRKEC1  =          SCC1PB+$44    | SCC1 BReaK Condition Counter (RX)
BRKLN1  =          SCC1PB+$46    | SCC1 Last BReaK Length (RX)
UADDR11 =          SCC1PB+$48    | SCC1 UART Address Character 1
UADDR21 =          SCC1PB+$4A    | SCC1 UART Address Character 2
RETMP1  =          SCC1PB+$4C    | SCC1 Temp storage
TOSEQ1  =          SCC1PB+$4E    | SCC1 TX out of sequence Character
CCHAR11 =          SCC1PB+$50    | SCC1 Control Character 1
CCHAR21 =          SCC1PB+$52    | SCC1 Control Character 2
```

```
CCHAR31 =       SCC1PB+$54    | SCC1 Control Character 3
CCHAR41 =       SCC1PB+$56    | SCC1 Control Character 4
CCHAR51 =       SCC1PB+$58    | SCC1 Control Character 5
CCHAR61 =       SCC1PB+$5A    | SCC1 Control Character 6
CCHAR71 =       SCC1PB+$5C    | SCC1 Control Character 7
CCHAR81 =       SCC1PB+$5E    | SCC1 Control Character 8
RCCM1   =       SCC1PB+$60    | SCC1 RX Control Character Mask
RCCR1   =       SCC1PB+$62    | SCC1 RX Control Character
RLBC1   =       SCC1PB+$64    | SCC1 RX Last Break Character

* SCC2, UART Specific Parameters
MAXIDL2 =       SCC2PB+$38    | SCC1 MAX IDLe cchars
IDLC2   =       SCC2PB+$3A    | SCC1 temp IDLe Counter
BRKCR2  =       SCC2PB+$3C    | SCC1 BReaK Count Register (TX)
PAREC2  =       SCC2PB+$3E    | SCC1 Parity Error Counter (RX)
FRMER2  =       SCC2PB+$40    | SCC1 Framing Error Counter (RX)
NOSEC2  =       SCC2PB+$42    | SCC1 Noise Counter (RX)
BRKEC2  =       SCC2PB+$44    | SCC1 BReaK Condition Counter (RX)
BRKLN2  =       SCC2PB+$46    | SCC1 Last BReaK Length (RX)
UADDR12 =       SCC2PB+$48    | SCC1 UART Address Character 1
UADDR22 =       SCC2PB+$4A    | SCC1 UART Address Character 2
RETMP2  =       SCC2PB+$4C    | SCC1 Temp storage
TOSEQ2  =       SCC2PB+$4E    | SCC1 TX out of sequence Character
CCHAR12 =       SCC2PB+$50    | SCC1 Control Character 1
CCHAR22 =       SCC2PB+$52    | SCC1 Control Character 2
CCHAR32 =       SCC2PB+$54    | SCC1 Control Character 3
CCHAR42 =       SCC2PB+$56    | SCC1 Control Character 4
CCHAR52 =       SCC2PB+$58    | SCC1 Control Character 5
CCHAR62 =       SCC2PB+$5A    | SCC1 Control Character 6
CCHAR72 =       SCC2PB+$5C    | SCC1 Control Character 7
CCHAR82 =       SCC2PB+$5E    | SCC1 Control Character 8
RCCM2   =       SCC2PB+$60    | SCC1 RX Control Character Mask
RCCR2   =       SCC2PB+$62    | SCC1 RX Control Character
RLBC2   =       SCC2PB+$64    | SCC1 RX Last Break Character

* SCC3, UART Specific Parameters
MAXIDL3 =       SCC3PB+$38    | SCC1 MAX IDLe cchars
IDLC3   =       SCC3PB+$3A    | SCC1 temp IDLe Counter
BRKCR3  =       SCC3PB+$3C    | SCC1 BReaK Count Register (TX)
PAREC3  =       SCC3PB+$3E    | SCC1 Parity Error Counter (RX)
FRMER3  =       SCC3PB+$40    | SCC1 Framing Error Counter (RX)
NOSEC3  =       SCC3PB+$42    | SCC1 Noise Counter (RX)
BRKEC3  =       SCC3PB+$44    | SCC1 BReaK Condition Counter (RX)
BRKLN3  =       SCC3PB+$46    | SCC1 Last BReaK Length (RX)
UADDR13 =       SCC3PB+$48    | SCC1 UART Address Character 1
UADDR23 =       SCC3PB+$4A    | SCC1 UART Address Character 2
```

```
RETMP3 =        SCC3PB+$4C   | SCC1 Temp storage
TOSEQ3 =        SCC3PB+$4E   | SCC1 TX out of sequence Character
CCHAR13 =       SCC3PB+$50   | SCC1 Control Character 1
CCHAR23 =       SCC3PB+$52   | SCC1 Control Character 2
CCHAR33 =       SCC3PB+$54   | SCC1 Control Character 3
CCHAR43 =       SCC3PB+$56   | SCC1 Control Character 4
CCHAR53 =       SCC3PB+$58   | SCC1 Control Character 5
CCHAR63 =       SCC3PB+$5A   | SCC1 Control Character 6
CCHAR73 =       SCC3PB+$5C   | SCC1 Control Character 7
CCHAR83 =       SCC3PB+$5E   | SCC1 Control Character 8
RCCM3  =        SCC3PB+$60   | SCC1 RX Control Character Mask
RCCR3  =        SCC3PB+$62   | SCC1 RX Control Character
RLBC3  =        SCC3PB+$64   | SCC1 RX Last Break Character

* SCC4, UART Specific Parameters
MAXIDL4 =       SCC4PB+$38   | SCC4 MAX IDLe cchars
IDLC4  =        SCC4PB+$3A   | SCC4 temp IDLe Counter
BRKCR4 =        SCC4PB+$3C   | SCC4 BReaK Count Register (TX)
PAREC4 =        SCC4PB+$3E   | SCC4 Parity Error Counter (RX)
FRMER4 =        SCC4PB+$40   | SCC4 Framing Error Counter (RX)
NOSEC4 =        SCC4PB+$42   | SCC4 Noise Counter (RX)
BRKEC4 =        SCC4PB+$44   | SCC4 BReaK Condition Counter (RX)
BRKLN4 =        SCC4PB+$46   | SCC4 Last BReaK Length (RX)
UADDR14 =       SCC4PB+$48   | SCC4 UART Address Character 1
UADDR24 =       SCC4PB+$4A   | SCC4 UART Address Character 2
RETMP4 =        SCC4PB+$4C   | SCC4 Temp storage
TOSEQ4 =        SCC4PB+$4E   | SCC4 TX out of sequence Character
CCHAR14 =       SCC4PB+$50   | SCC4 Control Character 1
CCHAR24 =       SCC4PB+$52   | SCC4 Control Character 2
CCHAR34 =       SCC4PB+$54   | SCC4 Control Character 3
CCHAR44 =       SCC4PB+$56   | SCC4 Control Character 4
CCHAR54 =       SCC4PB+$58   | SCC4 Control Character 5
CCHAR64 =       SCC4PB+$5A   | SCC4 Control Character 6
CCHAR74 =       SCC4PB+$5C   | SCC4 Control Character 7
CCHAR84 =       SCC4PB+$5E   | SCC4 Control Character 8
RCCM4  =        SCC4PB+$60   | SCC4 RX Control Character Mask
RCCR4  =        SCC4PB+$62   | SCC4 RX Control Character
RLBC4  =        SCC4PB+$64   | SCC4 RX Last Break Character

* SMC1, UART Specific Parameters
MAXIDLA =       SMC1PB+$28   | SMC1 MAX IDLe cchars
IDLCA  =        SMC1PB+$2A   | SMC1 temp IDLe Counter
BRKLA  =        SMC1PB+$2C   |SMC1 lastReceivedBReaKcharlength
BRKECA =        SMC1PB+$2E   |SMC1receiveBReaKConditionCounter
BRKCRA =        SMC1PB+$30   | SMC1 BReaK Count Register (TX)
```

PLX9080.i

Assembly language include file for the PCI9080.

```
*
* PCI9080
* PLX Technology, Inc.
* 6/10/97
* Note that the Variable names have been retained
* from the Pci9080 for this release
*
* PCI Configuration Registers
* Local and PCI CFG offsets

Pci9080DevId    =       $00
Pci9080VId      =       $02
Pci9080Stat     =       $04
Pci9080Cmd      =       $06
Pci9080CCode    =       $08
Pci9080RevId    =       $0b
Pci9080BIST     =       $0c
Pci9080HType    =       $0d
Pci9080LTmr     =       $0e
Pci9080CLSz     =       $0f
Pci9080PBAMMRR=         $10
Pci9080PBAIORR=         $14
Pci9080PBALAS0=         $18
Pci9080PBALAS1=         $1c
Pci9080SubDevID=        $2c
Pci9080SubVid   =       $2e
Pci9080PBALXR=          $30
Pci9080MaxLat   =       $3c
Pci9080MinGnt   =       $3d
Pci9080IntPin   =       $3e
Pci9080IntLin   =       $3f

* Local Registers offset from PCI Registers
Pci9080LRegOff=         $80

* Local Configuration Registers
* Note Local Reg Offset from PCI

Pci9080R4P2LAS0=        $80
Pci9080LBA4P2L0=        $84
Pci9080R4P2LXR=         $90
Pci9080LBA4P2LB=        $94
```

```
Pci9080BRD4P2LA=        $98
Pci9080R4DM2P=          $9c
Pci9080LA4DM2PM=        $a0
Pci9080LA4DM2PI=        $a4
Pci9080PBA4DM2P=        $a8
Pci9080PCA4DM2P=        $ac

* Shared Run Time Registers
* Note Local Reg Offset from PCI

Pci9080MBR0  =          $c0
Pci9080MBR1  =          $c4
Pci9080MBR2  =          $c8
Pci9080MBR3  =          $cc
Pci9080MBR4  =          $d0
Pci9080MBR5  =          $d4
Pci9080MBR6  =          $d8
Pci9080MBR7  =          $dc
Pci9080P2LDoor=         $e0
Pci9080L2PDoor=         $e4
Pci9080IntCtlS  =       $e8
Pci9080EepromC=         $ec


* Local DMA Registers
* Local Access only

Pci9080DmaC0M=          $100
Pci9080DmaC0PA=         $104
Pci9080DmaC0LA=         $108
Pci9080DmaC0TC=         $10c
Pci9080DmaC0DP=         $110
Pci9080DmaC1M=          $114
Pci9080DmaC1PA=         $118
Pci9080DmaC1LA=         $11c
Pci9080DmaC1TC=         $120
Pci9080DmaC1DP=         $124
Pci9080DmaCStat=        $128
Pci9080DmaAR0=          $12c
Pci9080DmaAR1=          $130
```

PMC334.i

```
*
* PTI PMC334 address defines.
*
*

*
* board equates
*

ramst                           =       $00400000       | Dram
Start Address, CS1
ramend                          =       ramst+$8fc
sstck                           =       ramst+$8f8
ustck                           =       ramst+$7fc

reg_space       =               $00100000       | CS5
plx9080                         =       reg_space
* was plx9060 = reg_space in PCI334 code   CER
clk_str_tx      =               reg_space+$10200
clk_str_rx      =               reg_space+$10300
mvme762                         =       reg_space+$400

stat_reg        =               reg_space+$1000   | CS6
quicc_ir        =               reg_space+$1100
pci_ir                          =       reg_space+$1200
misc_reg        =               reg_space+$1300
brdinfo_reg     =               reg_space+$1400
sp_conf2        =               reg_space+$1500
conf_reg        =               reg_space+$1600
prom_wen        =               reg_space+$1700


src_buf  =      $00480000       | source address for scc testing
dest_buf =      $00490000       | destination address ...

_1MEG           =               $00100000
_2MEG           =               $00200000
_4MEG           =               $00400000
_8MEG           =               $00800000
_16MEG          =               $01000000
_32MEG          =               $02000000

_1MEG_MASK =                    $1ff00001
_2MEG_MASK =                    $1fe00001
```

```
_4MEG_MASK =            $1fc00001
_8MEG_MASK =            $1f800001
_16MEG_MASK=            $1f000001
_32MEG_MASK=            $1e000001


* sbs334 residue XXX
* sbs_rstat =    $00be0000      | dram io with sbus for diags
* sbs_wstat =    $00be0002      | dram io with sbus for diags
* sbs_vir    =                  $00bfffec      | ptbug status delyjob

* sbus_size =    $00010000      | also in FCode
* dmabuf     =                  $00a00000      | used for si-64 DMA Space.
* tst_size  =    $00010000
```

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP